偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT7518 / WT7518L / WT7518D

PC POWER SUPPLY SUPERVISOR

Data Sheet

REV. 2.10

November 26, 2002

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GENERAL DESCRIPTION

The WT7518 series provides four or two protection circuits for over current detector (OCD), fault voltage level output and external delay control signal glitches for 14pins package.

The current detector level setting by ISn and RI pin.

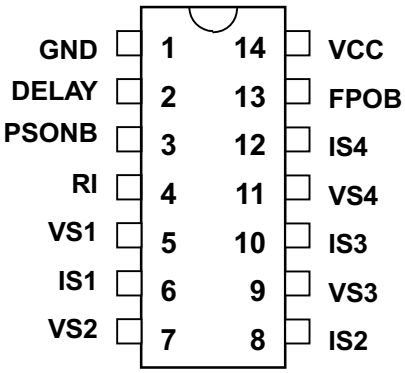
FEATURES

- The Over Current Detector (OCD) monitors IS1~IS4 input current sense.
- Fault protection (FPOB) are Open Drain Output, and latch for 141/143/145/147, un–latch for 140/142/144/146.
- 75 ms time delay for OCD.
- 38 ms for PSONB input signal De–bounce.
- Adjustable internal signal De–glitches by DELAY pin only for 14pins package.
- Under voltage lockout with hysteresis

PIN ASSIGNMENT AND PACKAGE TYPE

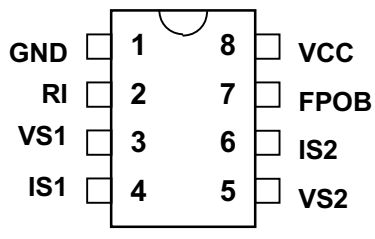
Pin assignment

WT7518 / WT7518L



Package type	14–Pin Plastic DIP	14–Pin Plastic SOP
ORDERING	WT7518–N140WT	WT7518–S140WT
	WT7518–N141WT	WT7518–S141WT
	WT7518–N142WT	WT7518–S142WT
	WT7518–N143WT	WT7518–S143WT
	WT7518–N144WT	WT7518–S144WT
	WT7518–N145WT	WT7518–S145WT
	WT7518–N146WT	WT7518–S146WT
	WT7518–N147WT	WT7518–S147WT
	WT7518L–N140WT	WT7518L–S140WT
	WT7518L–N143WT	WT7518L–S143WT
	WT7518L–N144WT	WT7518L–S144WT
	WT7518L–N147WT	WT7518L–S147WT

WT7518D



Package type	8–Pin Plastic DIP	8–Pin Plastic SOP
ORDERING	WT7518D–N080WT	WT7518D–S080WT

PIN DESCRIPTION

Pin Name	TYPE	Description
GND	**P**	Ground
DELAY	**IO**	Adjust OCD de–glitch time by connect CAP. to ground
PSONB	**I**	On/Off switch input
RI	**I**	Current sense adjust input
VS1	**I**	1st over current protection sense input
IS1	**I**	1st over current protection sense input
VS2	**I**	2nd over current protection sense input
IS2	**I**	2nd over current protection sense input
VS3	**I**	3rd over current protection sense input
IS3	**I**	3rd over current protection sense input
VS4	**I**	4th over current protection sense input
IS4	**I**	4th over current protection sense input
FPOB	**O**	Fault protection output pin, open drain output
VCC	**P**	Power supply

FUNCTION DESCRIPTION

ORDERING		UVLO	LATCH	FPL power on state
WT7518	**N140/S140**	4.5V/3.3V	un–latch	High
	N141/S141	10V/8V	latch	High
	N142/S142	10V/8V	un–latch	High
	N143/S143	4.5V/3.3V	latch	High
	N144/S144	4.5V/3.3V	un–latch	Low
	N145/S145	10V/8V	latch	Low
	N146/S146	10V/8V	un–latch	Low
	N147/S147	4.5V/3.3V	latch	Low
WT7518L	**N140/S140**	4.5V/3.3V	un–latch	High
	N143/S143	4.5V/3.3V	latch	High
	N144/S144	4.5V/3.3V	un–latch	Low
	N147/S147	4.5V/3.3V	latch	Low
WT7518D	**N080/S080**	10V/8V	un–latch	Low

ABSOLUTE MAXIMUM RATINGS

Parameter		Min.	Max.	Unit
Supply voltage, VCC	WT7518, WT7518D	–0.3	16	V
	WT7518L	–0.3	7	V
Input voltage	PSONB	–0.3	7	V
	VS1, VS2, VS3, VS4	–0.3	VCC+0.3	V
	IS1, IS2, IS3, IS4	–0.3	VCC+0.3	V
Output voltage	FPOB	–0.3	VCC+0.3	V
Operating temperature		-40	125	℃
Storage temperature		-55	150	℃

*Note: Stresses above those listed may cause permanent damage to the devices

RECOMMENDED OPERATING CONDITIONS

Parameter		Conditions	Min.	Typ.	Max.	Unit
Supply voltage, VCC	WT7518, WT7518D			12	15	V
	WT7518L			5	7	V
Input voltage	PSONB				7	V
	VS1, VS2, VS3, VS4				VCC	V
	IS1, IS2, IS3, IS4				VCC	V
Output voltage	FPOB				VCC	V
Output sink current	FPOB				30	mA
VCC rising time			1			ms
Output current for RI	RI		10		65	uA

ELECTRICAL CHARACTERISTICS, at Ta=25°C and V_{CC}=5V

PSONB

Parameter	Condition	Min.	Typ.	Max.	Unit
Input pull–up current	PSONB= 0V		150		uA
High–level input voltage		2.2			V
Low–level input voltage				0.6	V

UNDER VOLTAGE LOCKOUT

Parameter	Condition	Min.	Typ.	Max.	Unit
Start voltage	140/143/144/147		4.5		V
	141/142/145/146/080		10		V
Min. operating voltage after turn on	140/143/144/147		3.3		V
	141/142/145/146/080		8		V

TOTAL DEVICE

Parameter	Condition	Min.	Typ.	Max.	Unit
Icc Supply current	PSONB= 5V			1	mA
$I_{LEAKAGE}$ Leakage current (FPOB)	V(FPOB) = 5V		5		uA
V_{OL} Low level output voltage (FPOB)	I_{sink} =10mA		0.3		V
	I_{sink} =30mA		0.7		

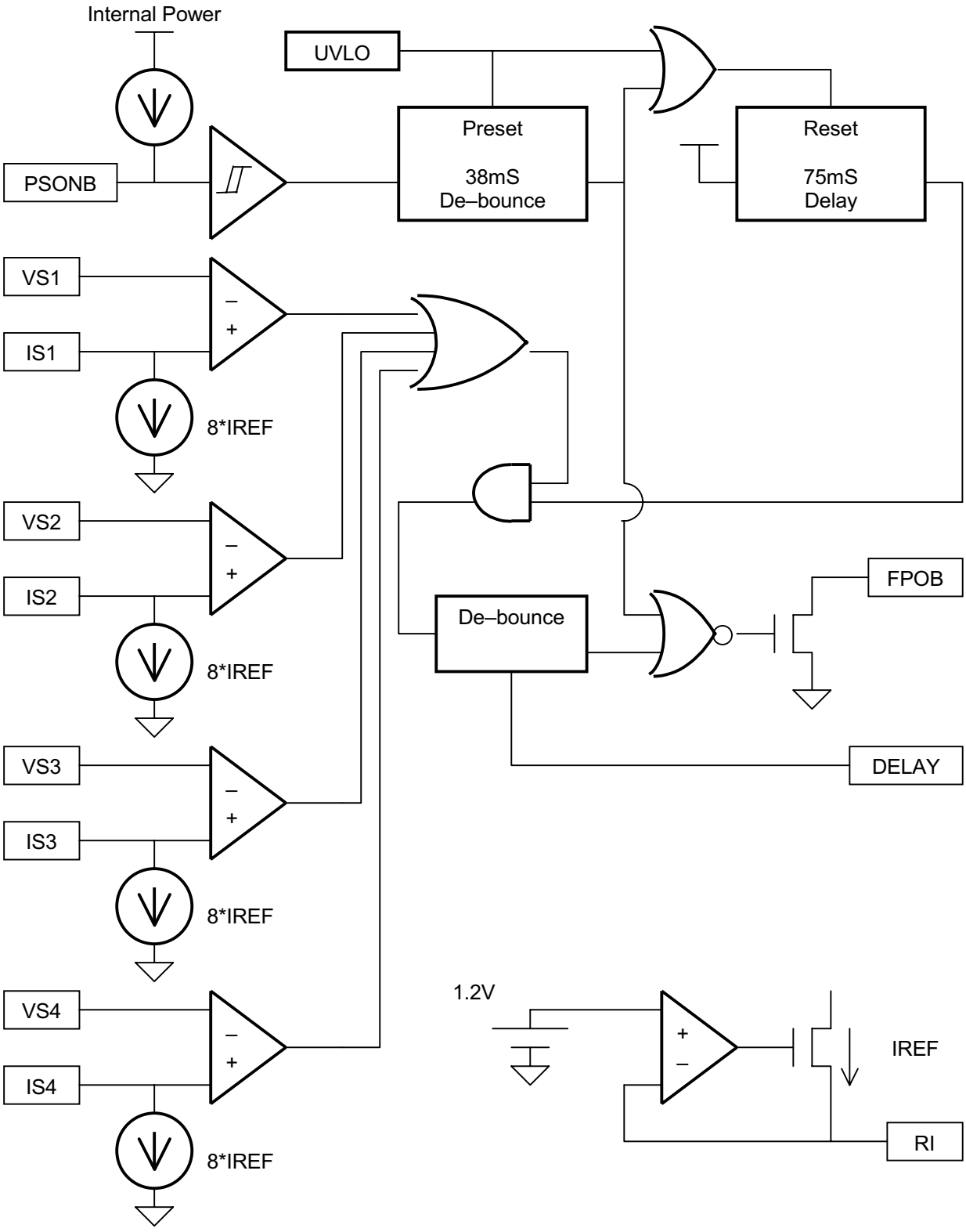
SWITCHING CHARACTERISTICS, Vcc=5V

Parameter	Condition	Min.	Typ.	Max.	Unit
t_{db1} De–bounce time (PSONB)		32	38	61	ms
t_{db2} De–bounce time (PSONB)		32	38	61	ms
t_{g1} De–glitch time for OCD state active	WT7518, WT7518L DELAY=47pF, note1	64	80	96	us
	WT7518D	120	150	180	us
t_{g2} De–glitch time for OCD state release	WT7518, WT7518L DELAY=47pF, note1	128	160	192	us
	WT7518D	240	300	360	us
t_{delay3} Internal OCD delay time	after FPOB go low	65	75	122	ms

note1：Please refer to Fig.1 for the relation of OCD De–glitch time and delay cap.

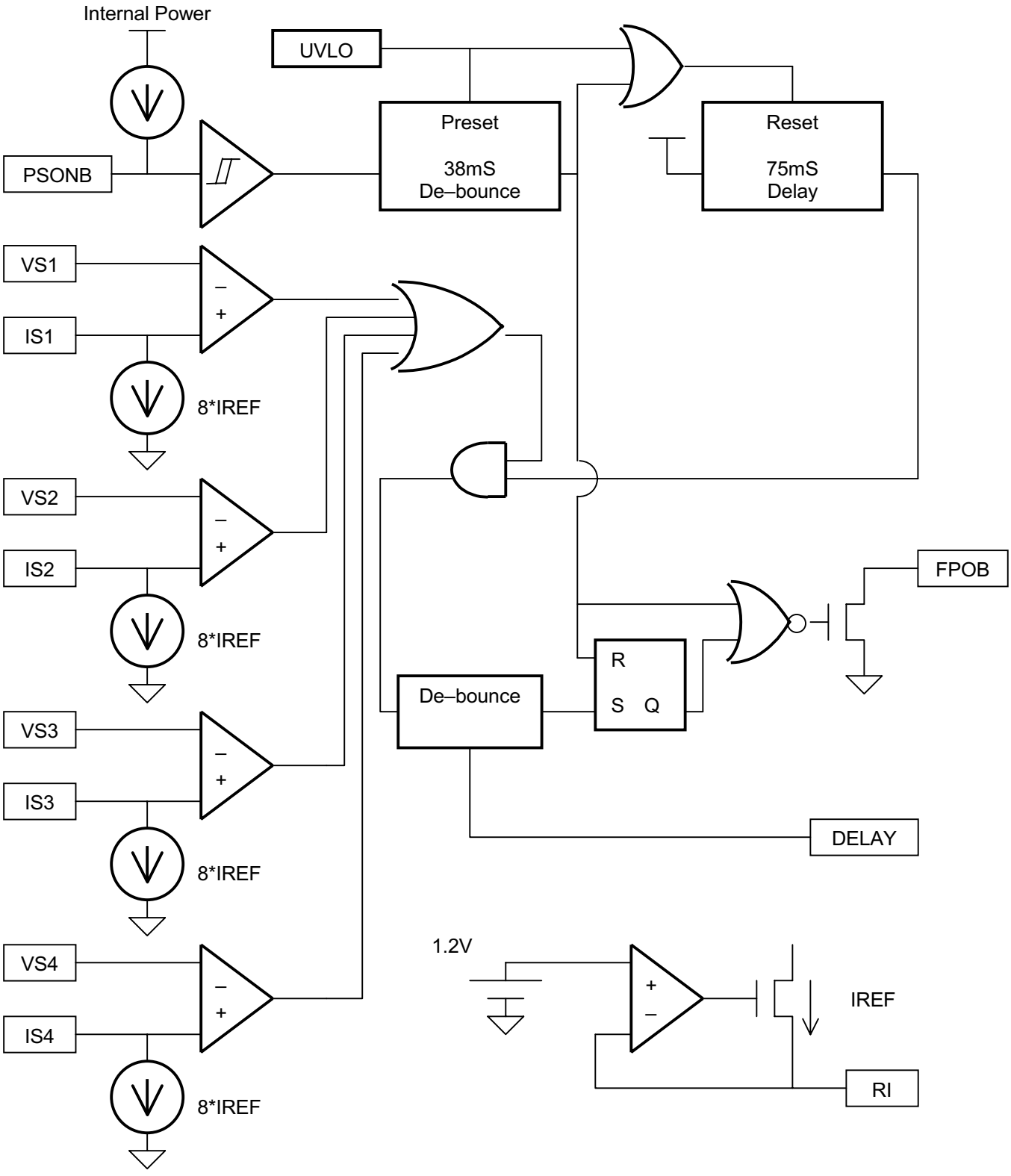
BLOCK DIAGRAM

140/142 (without latch and FPL power on state “high”)



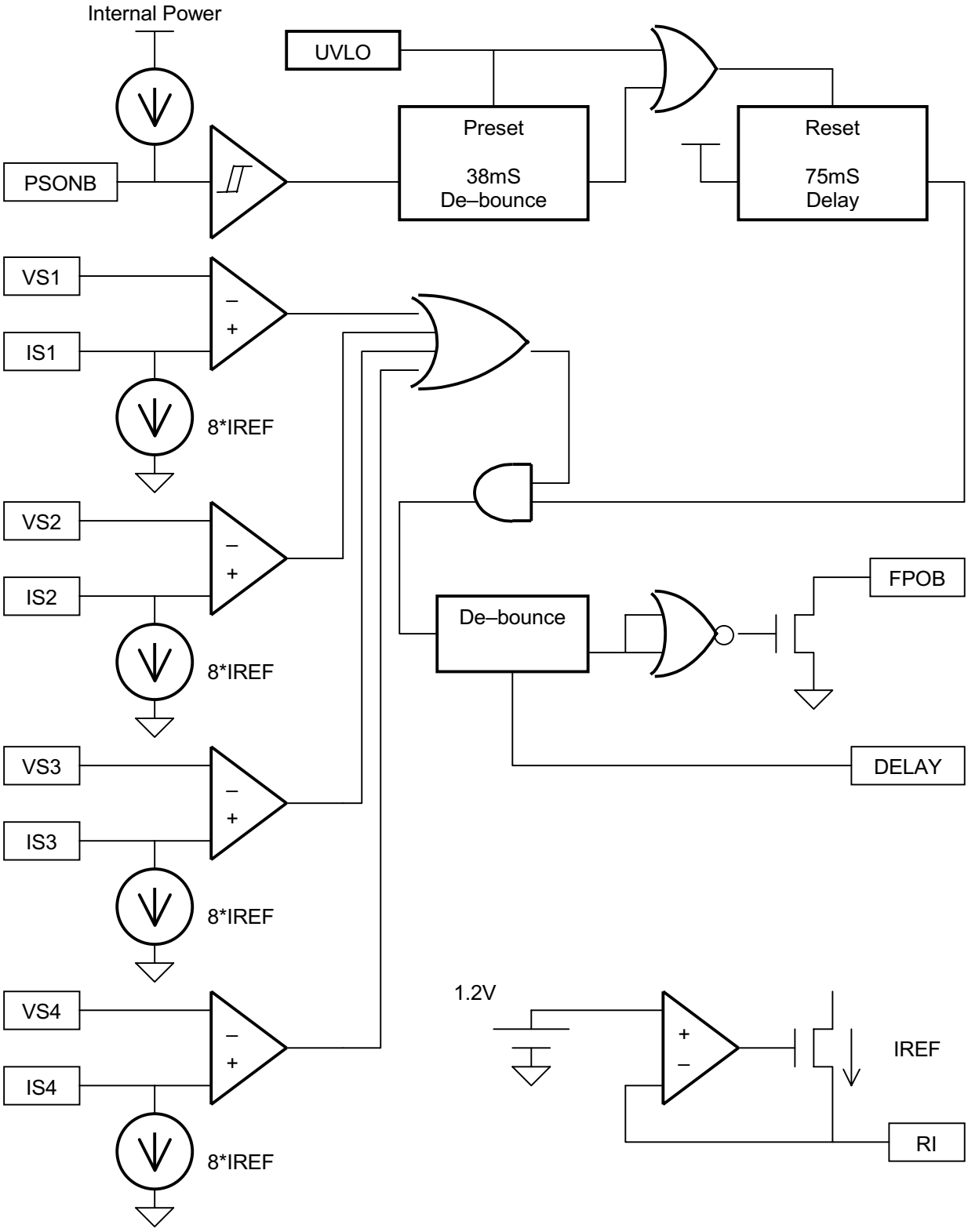
BLOCK DIAGRAM

141/143 (with latch and FPL power on state “high”)



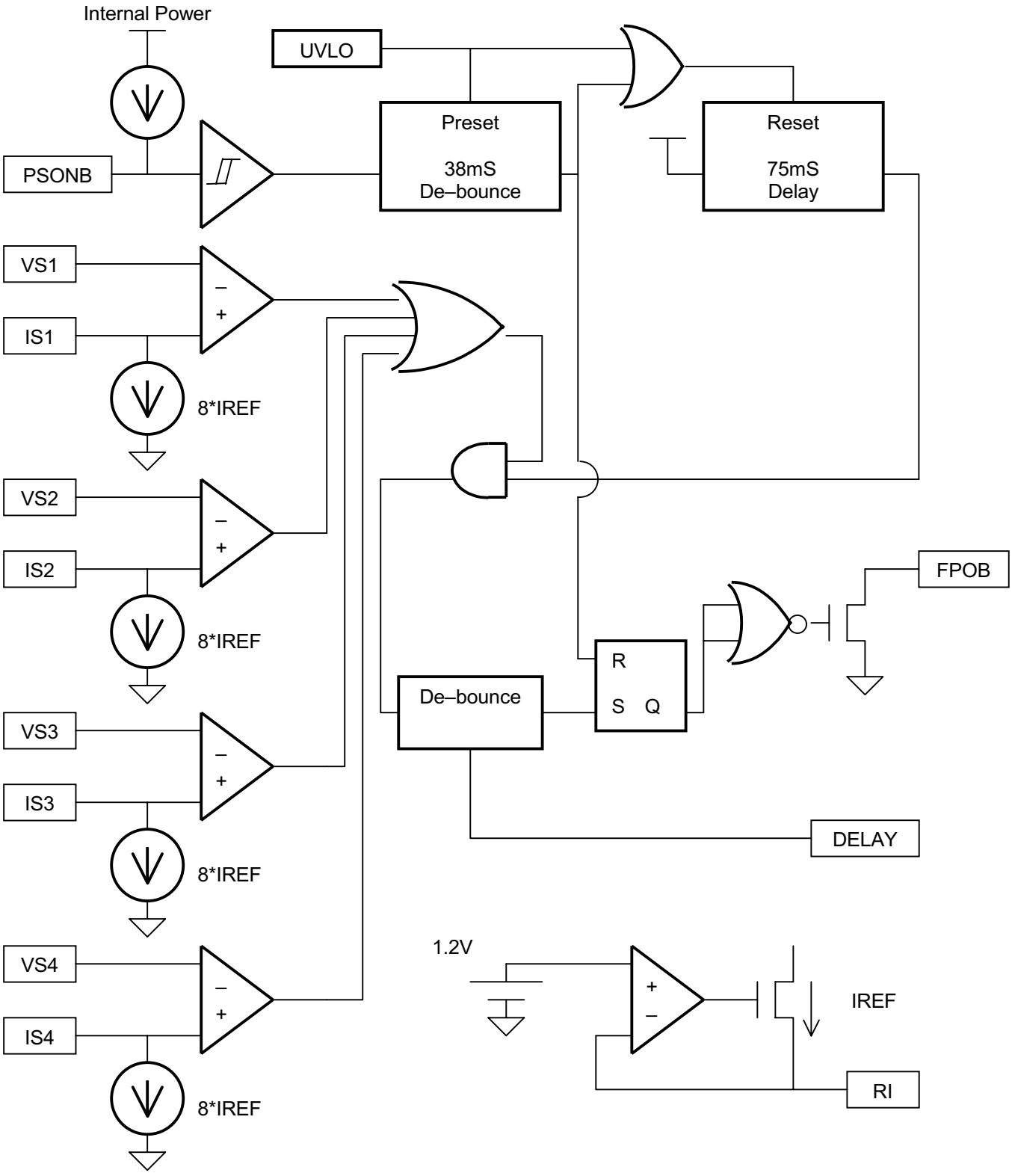
BLOCK DIAGRAM

144/146 (without latch and FPL power on state “low”)



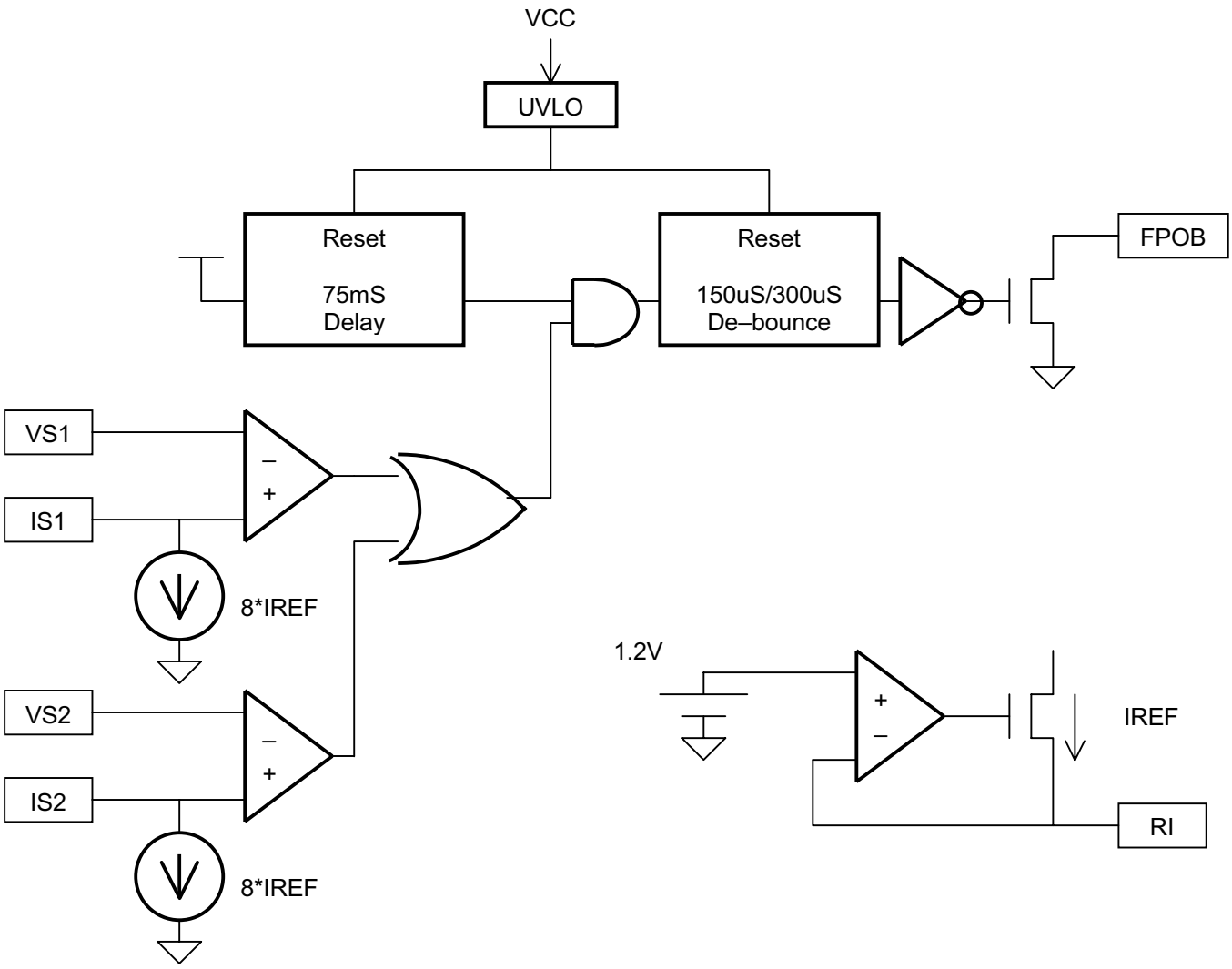
BLOCK DIAGRAM

145/147 (with latch and FPL power on state “low”)

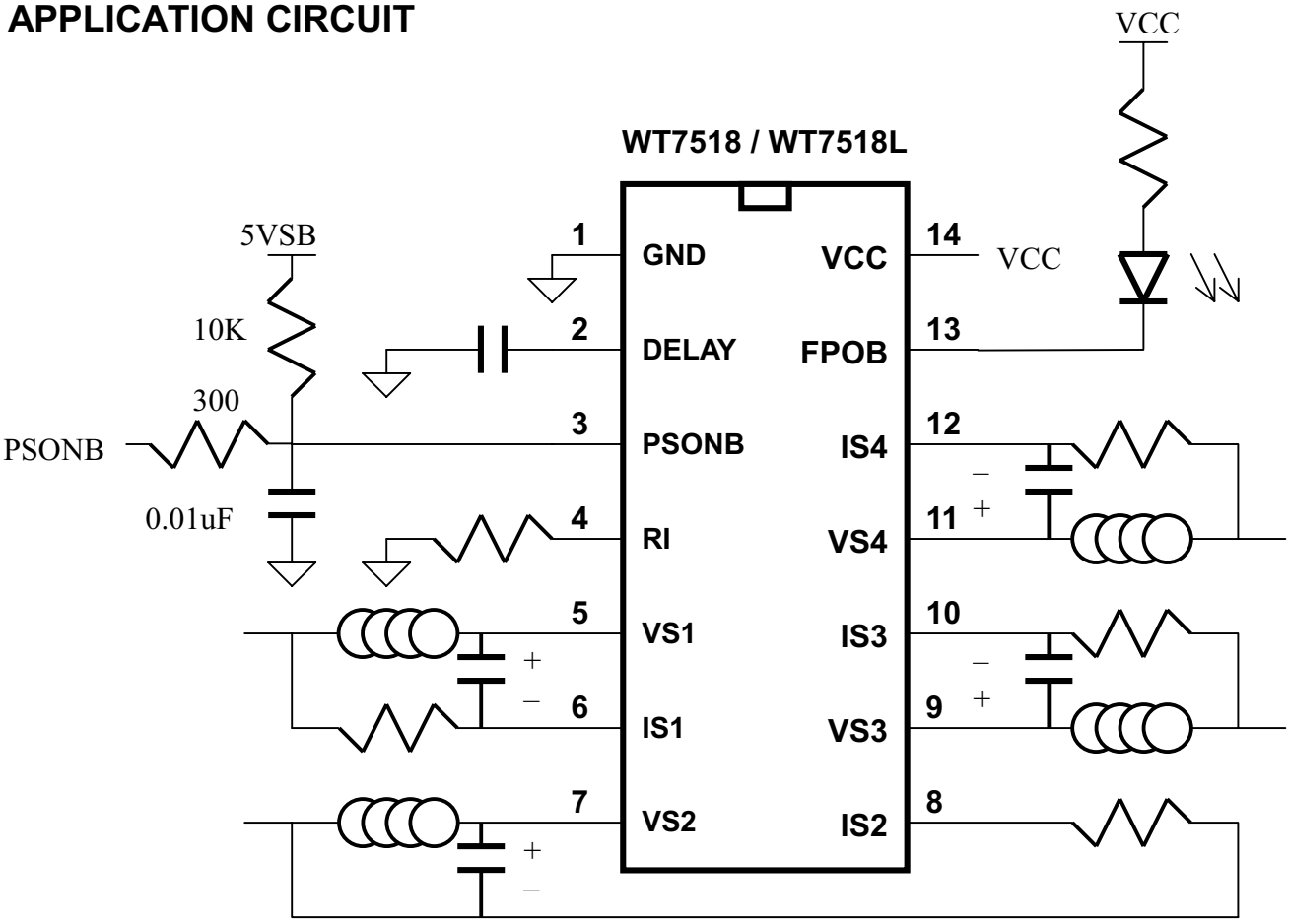


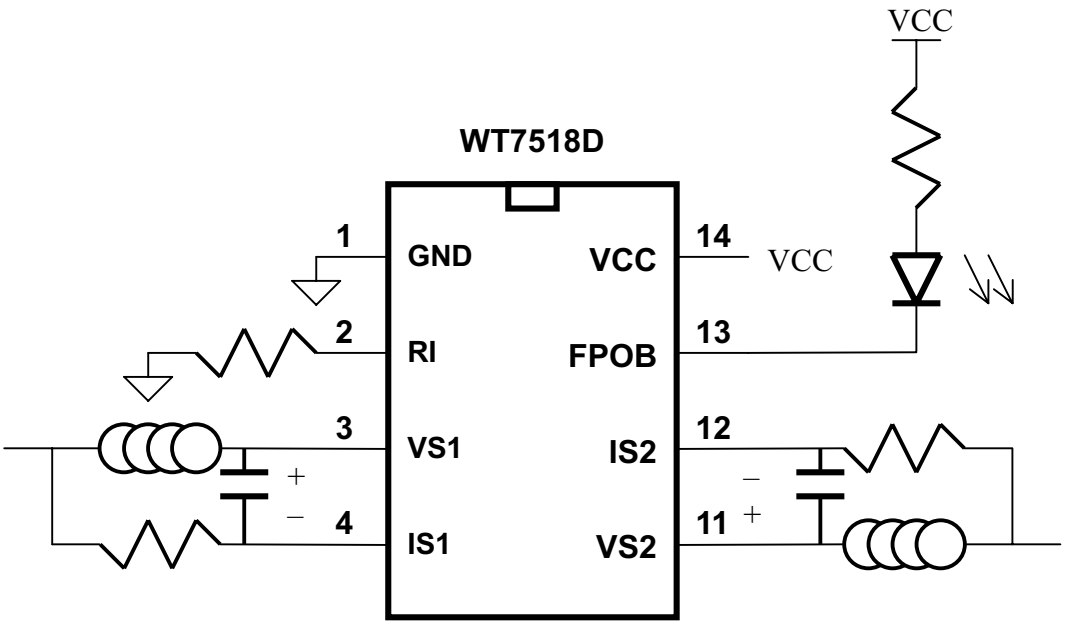
BLOCK DIAGRAM

080 (without latch and FPL power on state “low”)

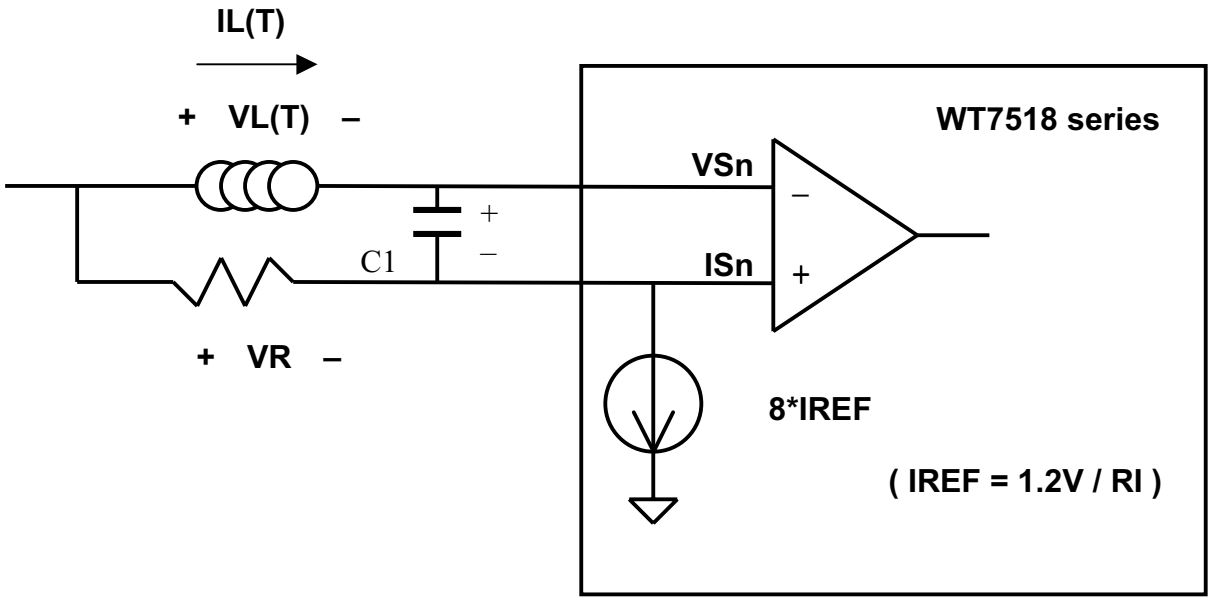


APPLICATION CIRCUIT





APPLICATION NOTE



When the current cross inductor raised immediately, inductor voltage raised.
And when inductor voltage exceeded resistor voltage, the OCP active.
We can setup OCP point by the following equation
VL(T) = VR
L * [d IL(T) / dT] = (8*1.2/RI) * R
d IL(T) / dT = (8*1.2/RI) * R/ L …..(1)

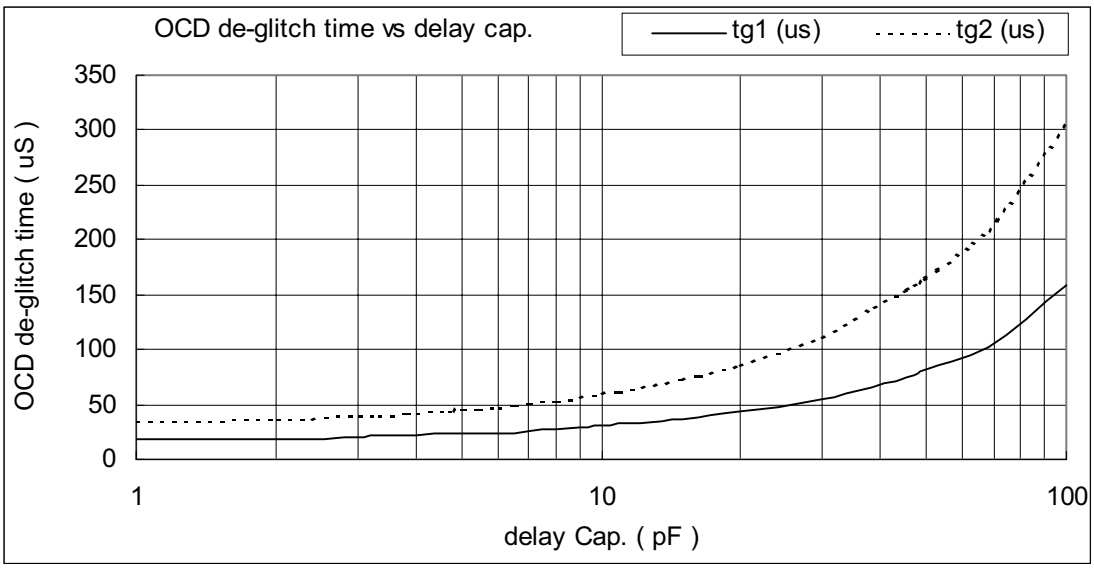
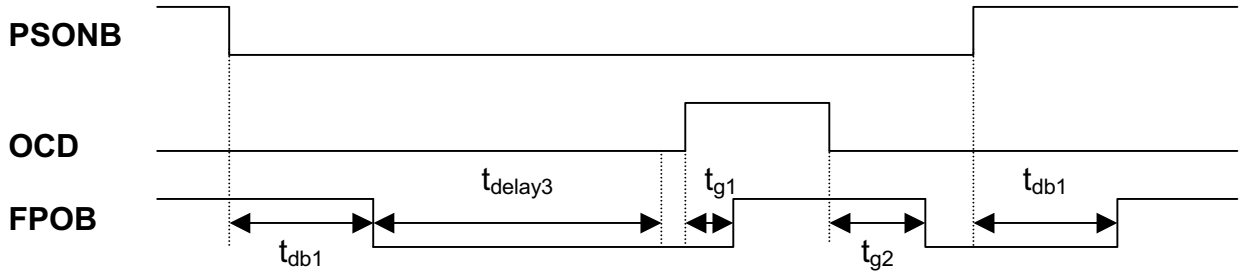


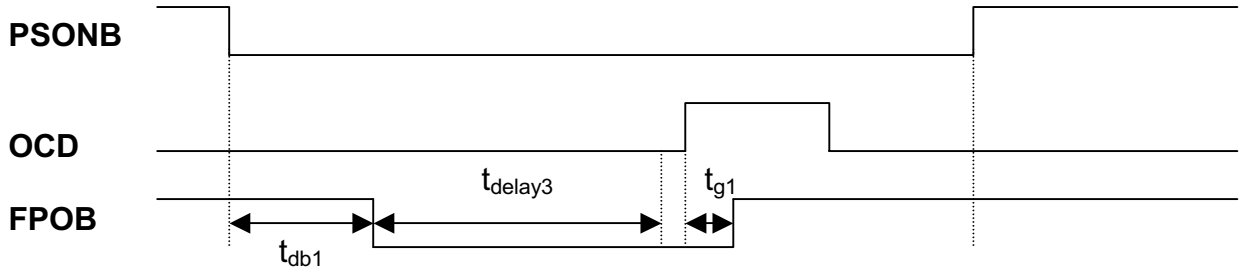
Fig.1 OCD de–glitch time vs delay cap.

APPLICATION TIMMING

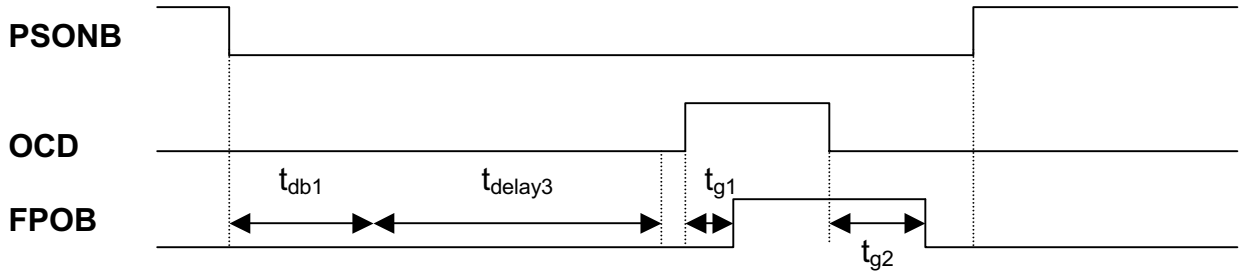
For 140/142 – FPOB without lacth and FPL power on state "high"



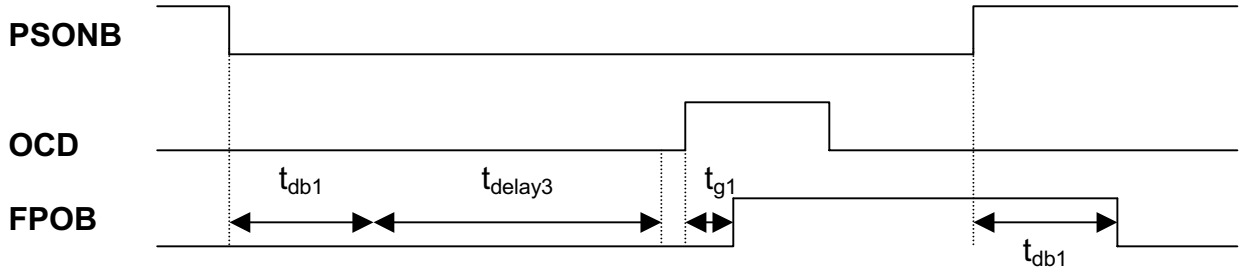
For 141/143 – FPOB with lacth and FPL power on state "high"



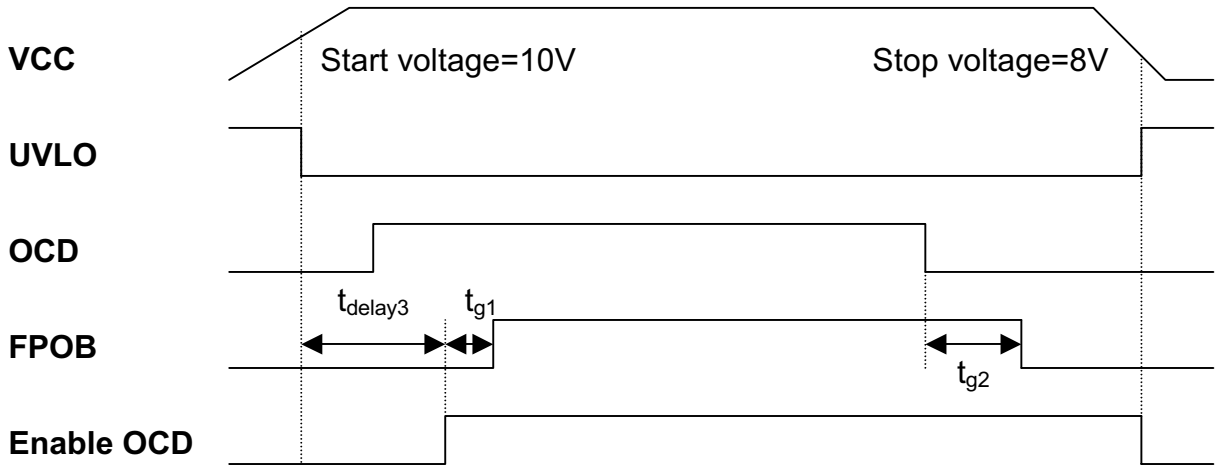
For 144/146 – FPOB without lacth and FPL power on state "low"



For 145/147 – FPOB with lacth and FPL power on state "low"



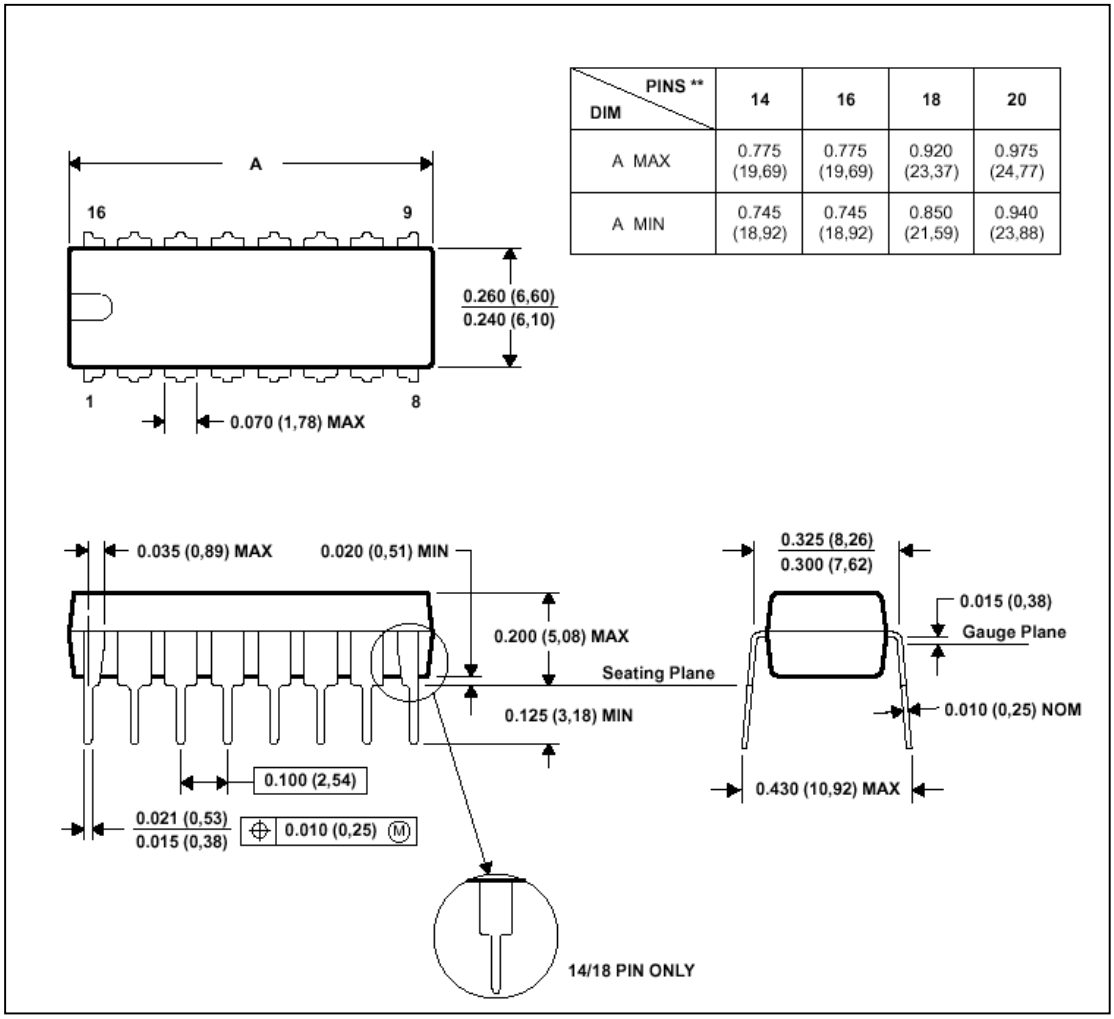
For 080 – FPOB without lacth and FPL power on state "low"



MECHANICAL INFORMATION

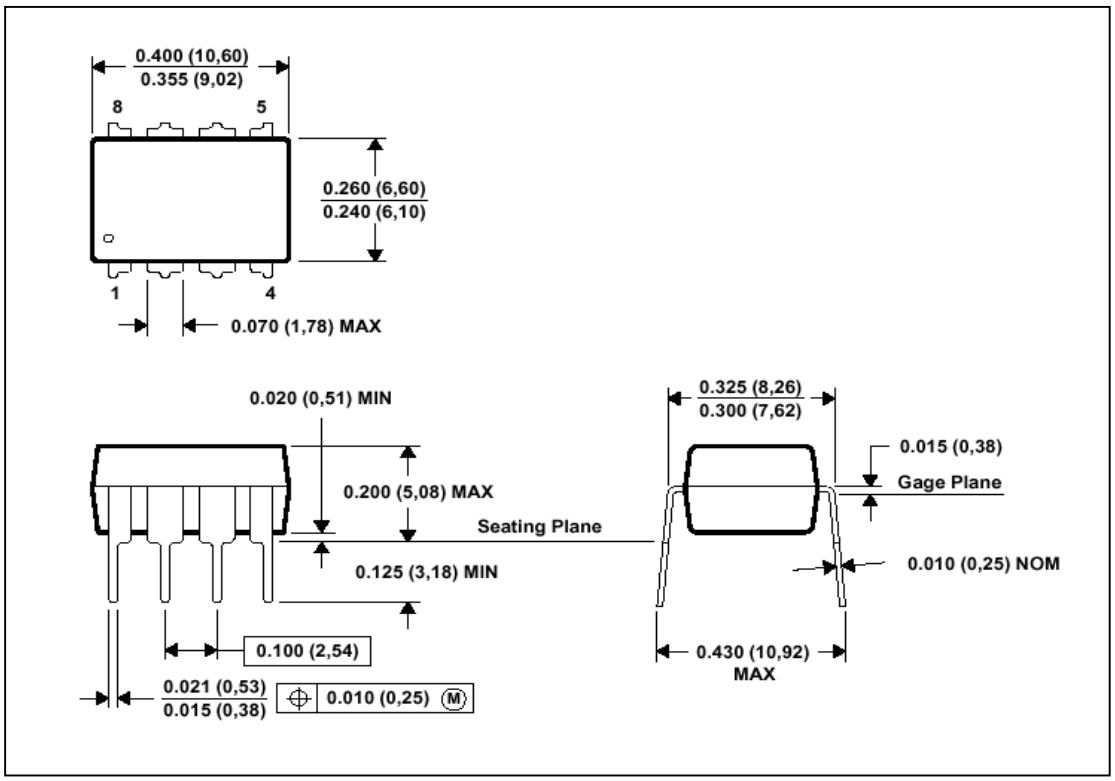
PLASTIC DUAL–IN–LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



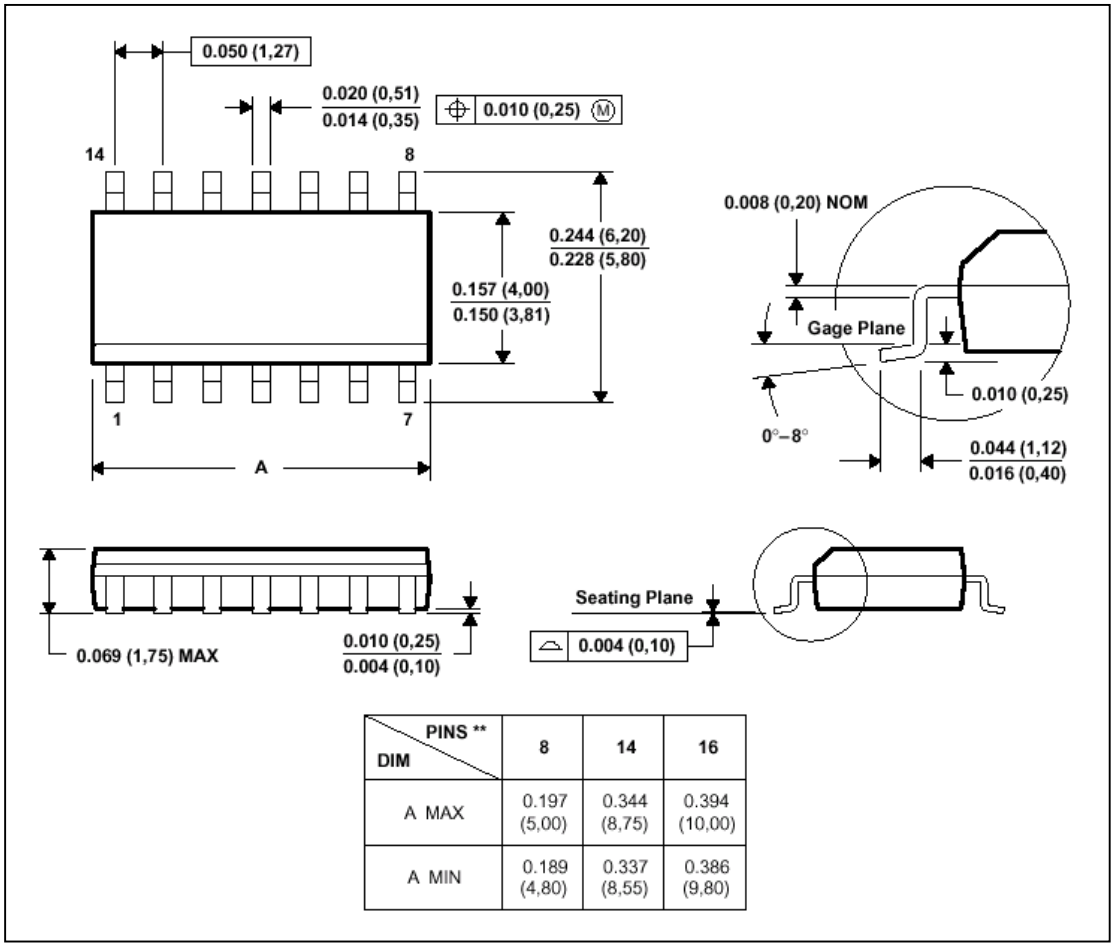
NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–001

PLASTIC DUAL–IN–LINE PACKAGE



NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–001

PLASTIC SMALL–OUTLINE PACKAGE



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–012