偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT7518

PC POWER SUPPLY SUPERVISOR

Data Sheet

REV. 1.00

January 30, 2002

WT7518

Rev. 1.00

GENERAL DESCRIPTION

The WT7518 provides four protection circuits for over current detector (OCD), fault voltage level output and external delay control signal glitches.

The current detector level setting by ISn and RI pin.

FEATURES

- The Over Current Detector (OCD) monitors IS1~IS4 input current sense.
- Fault protection (FPOB) are Open Drain Output, and latch for 141/143, no–latch for 140/142.
- 75 ms time delay for OCD.
- 38 ms for PSONB input signal De–bounce.
- Adjustable internal signal De–glitches by DELAY pin.
- Under voltage lockout with hysteresis

PIN ASSIGNMENT AND PACKAGE TYPE

Pin assignment

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              WT7518
GND   [  1      14  ]  VCC
DELAY [  2      13  ]  FPOB
PSONB [  3      12  ]  IS4
RI    [  4      11  ]  VS4
VS1   [  5      10  ]  IS3
IS1   [  6       9  ]  VS3
VS2   [  7       8  ]  IS2
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Package type	ORDERING INFORMATION
14–Pin Plastic DIP	WT7518–N140WT
14–Pin Plastic DIP	WT7518–N141WT
14–Pin Plastic DIP	WT7518–N142WT
14–Pin Plastic DIP	WT7518–N143WT

Package type	ORDERING INFORMATION
14–Pin Plastic SOP	WT7518–S140WT
14–Pin Plastic SOP	WT7518–S141WT
14–Pin Plastic SOP	WT7518–S142WT
14–Pin Plastic SOP	WT7518–S143WT

PIN DESCRIPTION

Pin Name	TYPE	Description
GND	P	Ground
DELAY	IO	Adjust OCD de–glitch time by connect CAP. to ground
PSONB	I	On/Off switch input
RI	I	Current sense adjust input
VS1	I	1 over current protection sense input
IS1	I	1 over current protection sense input
VS2	I	2 over current protection sense input
IS2	I	2 over current protection sense input
VS3	I	3 over current protection sense input
IS3	I	3 over current protection sense input
VS4	I	4 over current protection sense input
IS4	I	4 over current protection sense input
FPOB	O	Fault protection output pin, open drain output
VCC	P	Power supply

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ABSOLUTE MAXIMUM RATINGS

Parameter		Min.	Max.	Unit
Supply voltage, VCC		−0.3	16	V
Input voltage	PSONB	−0.3	7	V
	VS1, VS2, VS3, VS4	−0.3	VCC+0.3	
	IS1, IS2, IS3, IS4	−0.3	VCC+0.3	V
Output voltage	FPOB	−0.3	VCC+0.3	V
Operating temperature		-40	125	℃
Storage temperature		-55	150	℃

*Note: Stresses above those listed may cause permanent damage to the devices

RECOMMENDED OPERATING CONDITIONS

Parameter		Conditions	Min.	Typ.	Max.	Unit
Supply voltage, VCC				12	15	V
Input voltage	PSONB				7	V
	VS1, VS2, VS3, VS4				15	
	IS1, IS2, IS3, IS4				15	V
Output voltage	FPOB				15	V
Output sink current	FPOB				30	mA
VCC rising time				1		ms
Output current for RI	RI			10	65	uA

ELECTRICAL CHARACTERISTICS, at Ta=25°C and V_{cc}=5V and V12A=12V.

PSONB

Parameter	Condition	Min.	Typ.	Max.	Unit
Input pull–up current	PSONB= 0V		150		uA
High–level input voltage		2.2			V
Low–level input voltage				0.6	V

UNDER VOLTAGE LOCKOUT

Parameter	Condition	Min.	Typ.	Max.	Unit
Start voltage	140/143		4.5		V
	141/142		10		V
Min. operating voltage after turn on	140/143		3.3		V
	141/142		8		V

TOTAL DEVICE

Parameter	Condition	Min.	Typ.	Max.	Unit
Icc Supply current	PSONB= 5V			1	mA
$I_{LEAKAGE}$ Leakage current (FPOB)	V(FPOB) = 5V		5		uA
V_{OL} Low level output voltage (FPOB)	I_{sink} =10mA		0.3		V
	I_{sink} =30mA		0.7		

SWITCHING CHARACTERISTICS, Vcc=5V

Parameter	Condition	Min.	Typ.	Max.	Unit
t_{db1} De–bounce time (PSONB)		32	38	61	ms
t_{db2} De–bounce time (PSONB)		32	38	61	ms
t_{g1} De–glitch time for OCD state active	DELAY=47pF	64	80	96	us
t_{g2} De–glitch time for OCD state release	DELAY=47pF	128	160	192	us
t_{delay3} Internal OCD delay time	after FPOB go low	65	75	122	ms

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BLOCK DIAGRAM – 140/142 (WITHOUT LATCH)

Internal Power

UVLO

PSONB

Preset

38mS
De–bounce

Reset

75mS
Delay

VS1

IS1

8*IREF

VS2

IS2

8*IREF

De–bounce

FPOB

VS3
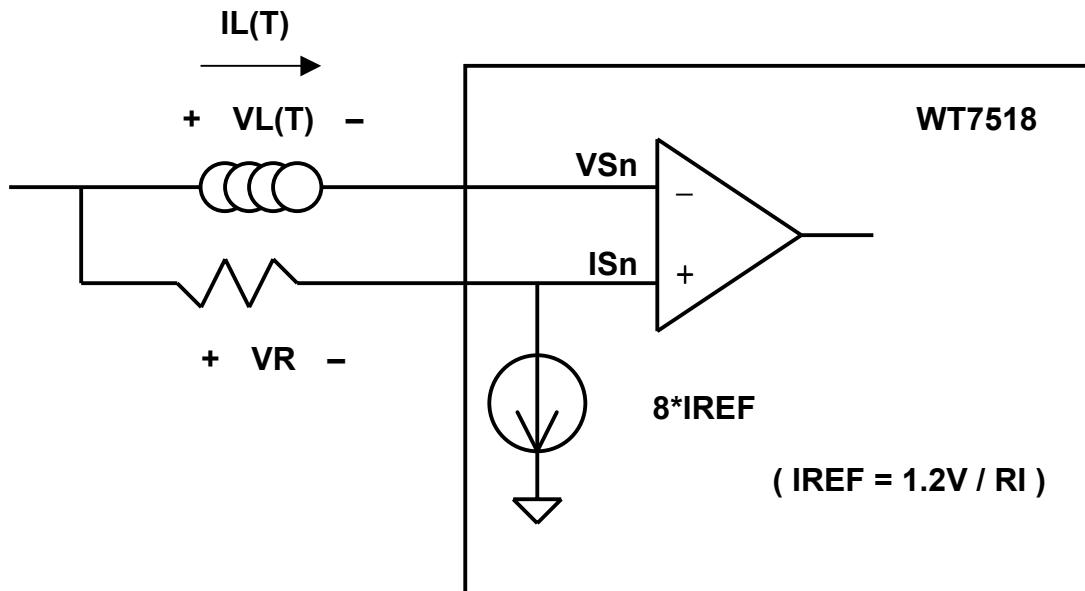
IS3

8*IREF

DELAY

VS4

IS4

1.2V

IREF

RI

8*IREF
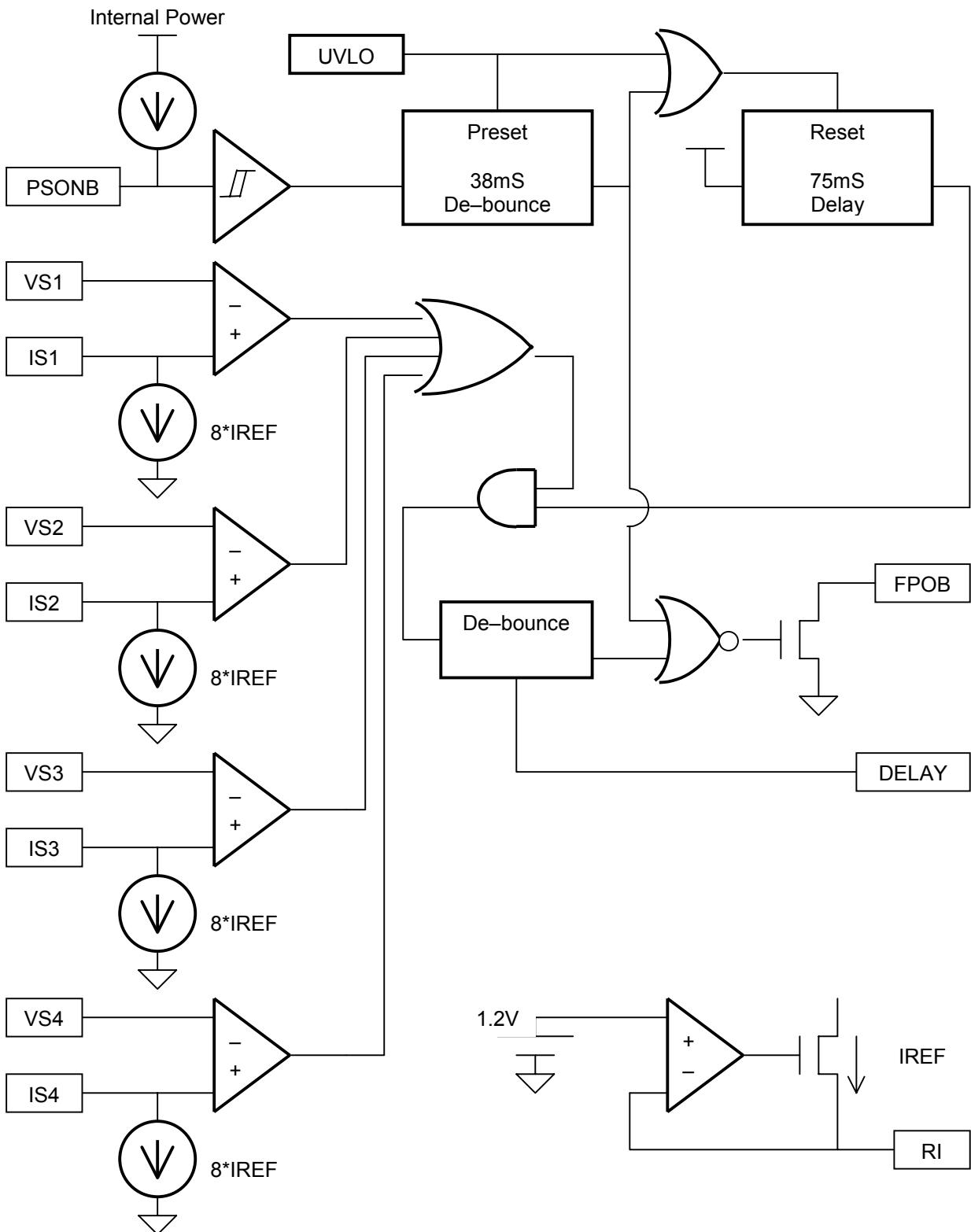
BLOCK DIAGRAM – 141/143 (WITH LATCH)
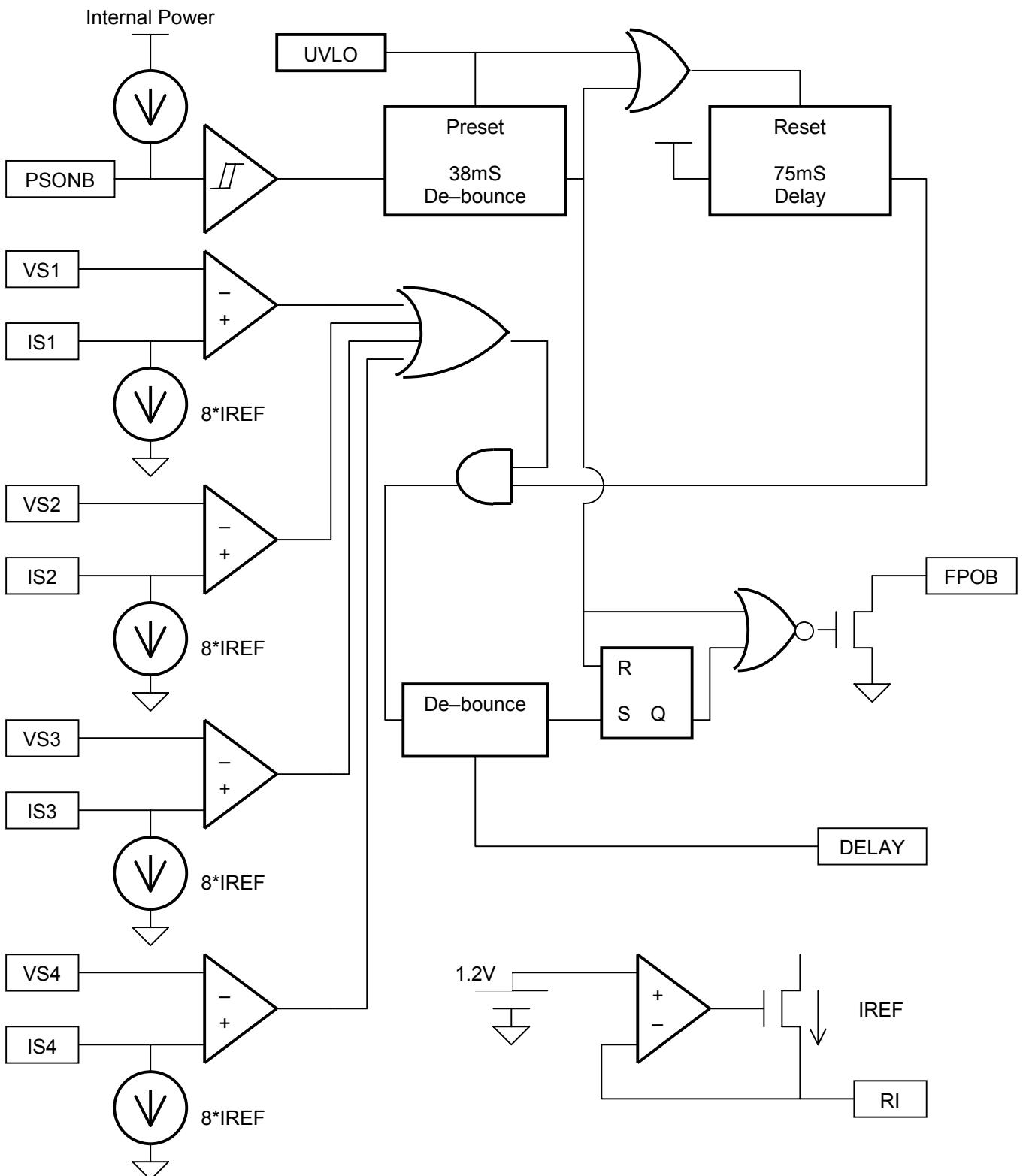
APPLICATION CIRCUIT
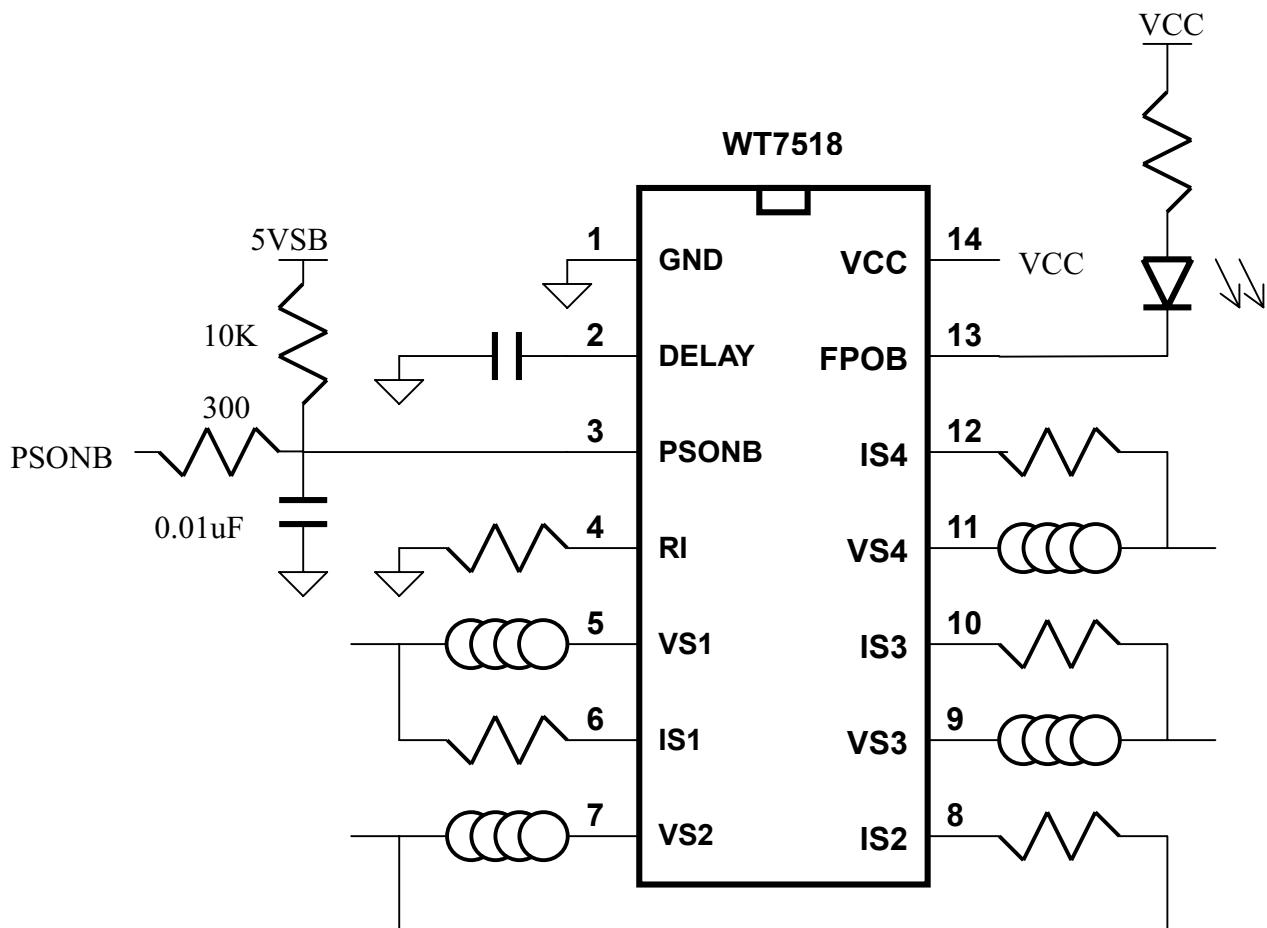
APPLICATION NOTE

When the current cross inductor raised immediately, inductor voltage raised.
And when inductor voltage exceeded resistor voltage, the OCP active.
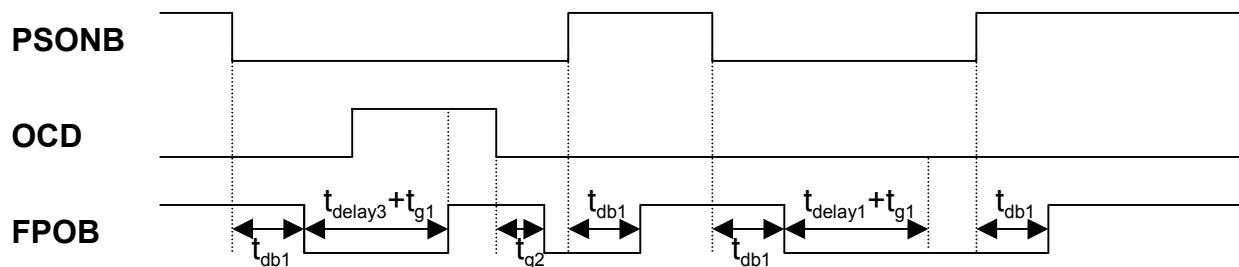We can setup OCP point by the following equation
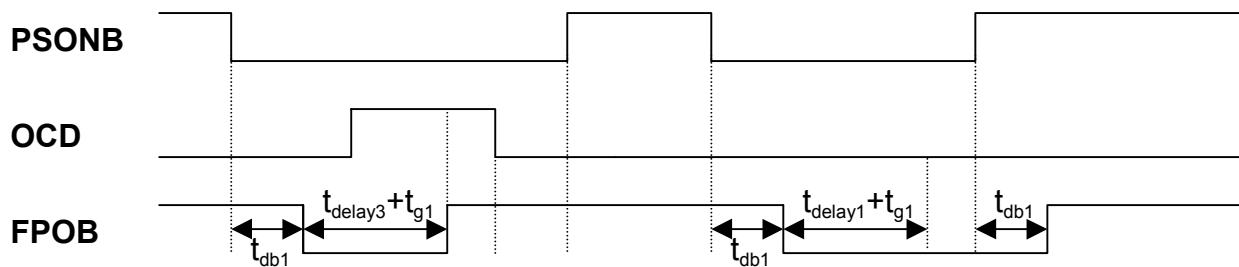
$VL(T) = VR$

$L * [d\ IL(T) / dT] = (8*1.2/RI) * R$

$d\ IL(T) / dT = (8*1.2/RI) * R/ L$ …..(1)

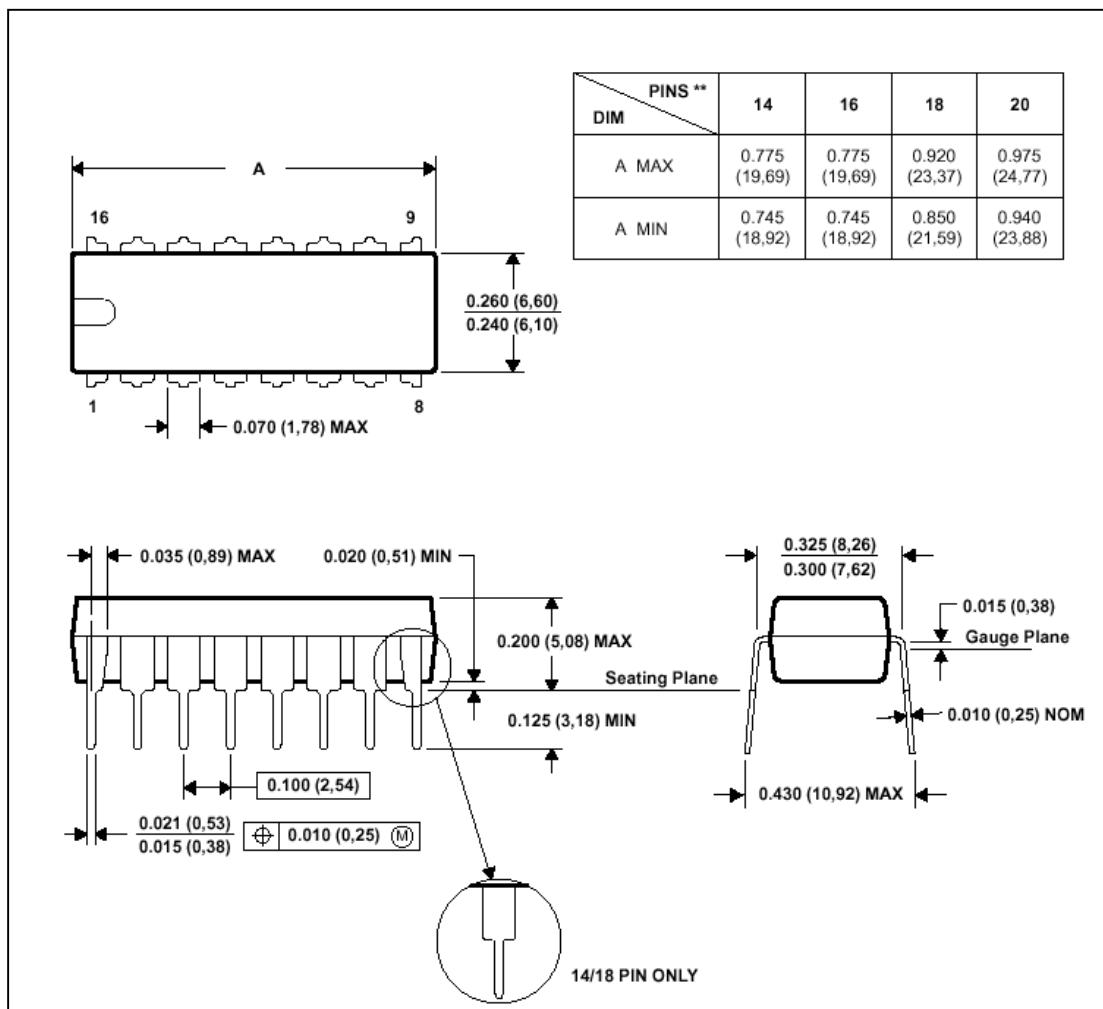
APPLICATION TIMMING

For 140/142 – FPOB without lacth

PSONB

OCD

FPOB

t_{db1} $t_{delay3}+t_{g1}$ t_{g2} t_{db1} t_{db1} $t_{delay1}+t_{g1}$ t_{db1}

For 141/143 – FPOB with lacth

PSONB

OCD

FPOB

t_{db1} $t_{delay3}+t_{g1}$ t_{db1} $t_{delay1}+t_{g1}$ t_{db1}

MECHANICAL INFORMATION

PLASTIC DUAL–IN–LINE PACKAGE

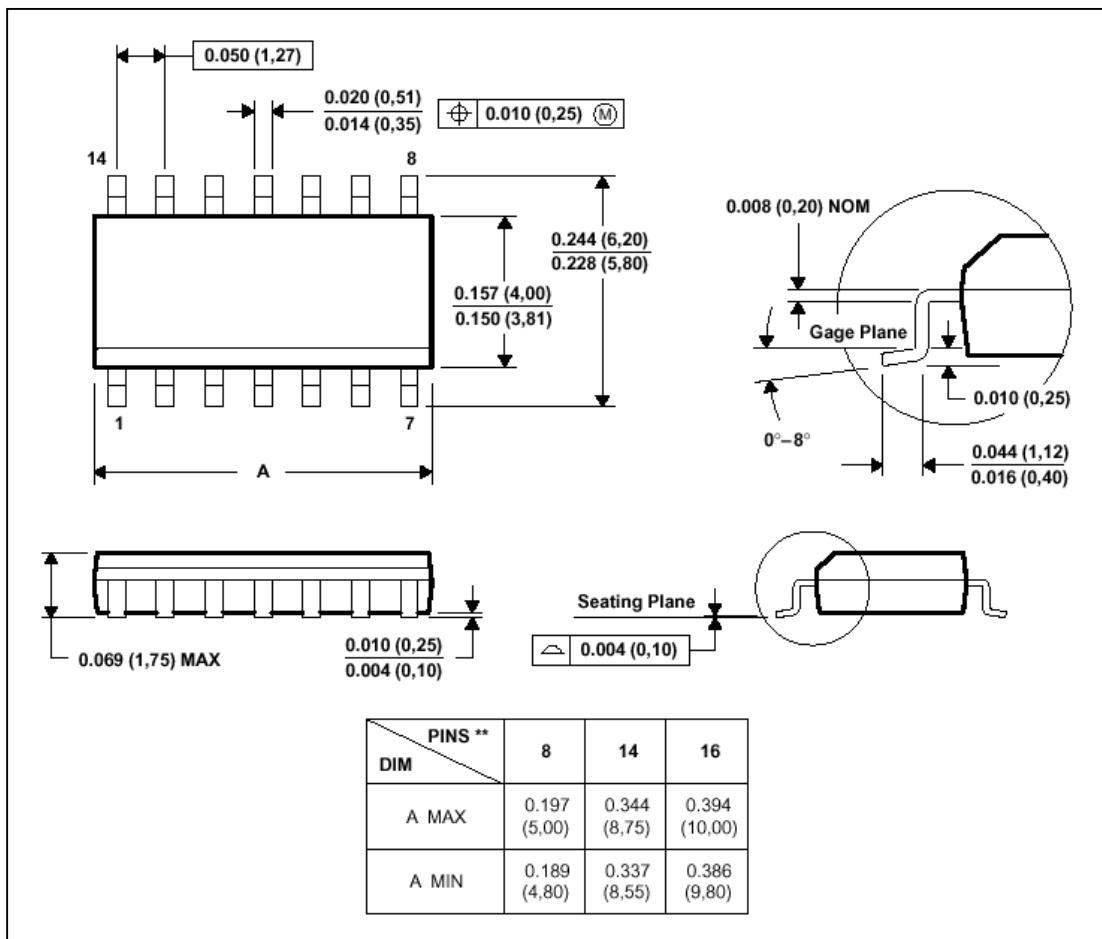| DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)

NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–001

PLASTIC SMALL–OUTLINE PACKAGE

PINS ** DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–012