2012 S-Series Richie 13.3"
UMA/DIS Muxless Schematic

Intel Chief River Platform
Ivy Bridge (rPGA989)
Panther Point PCH

REV:-1
2012-03-15

<Core Design>

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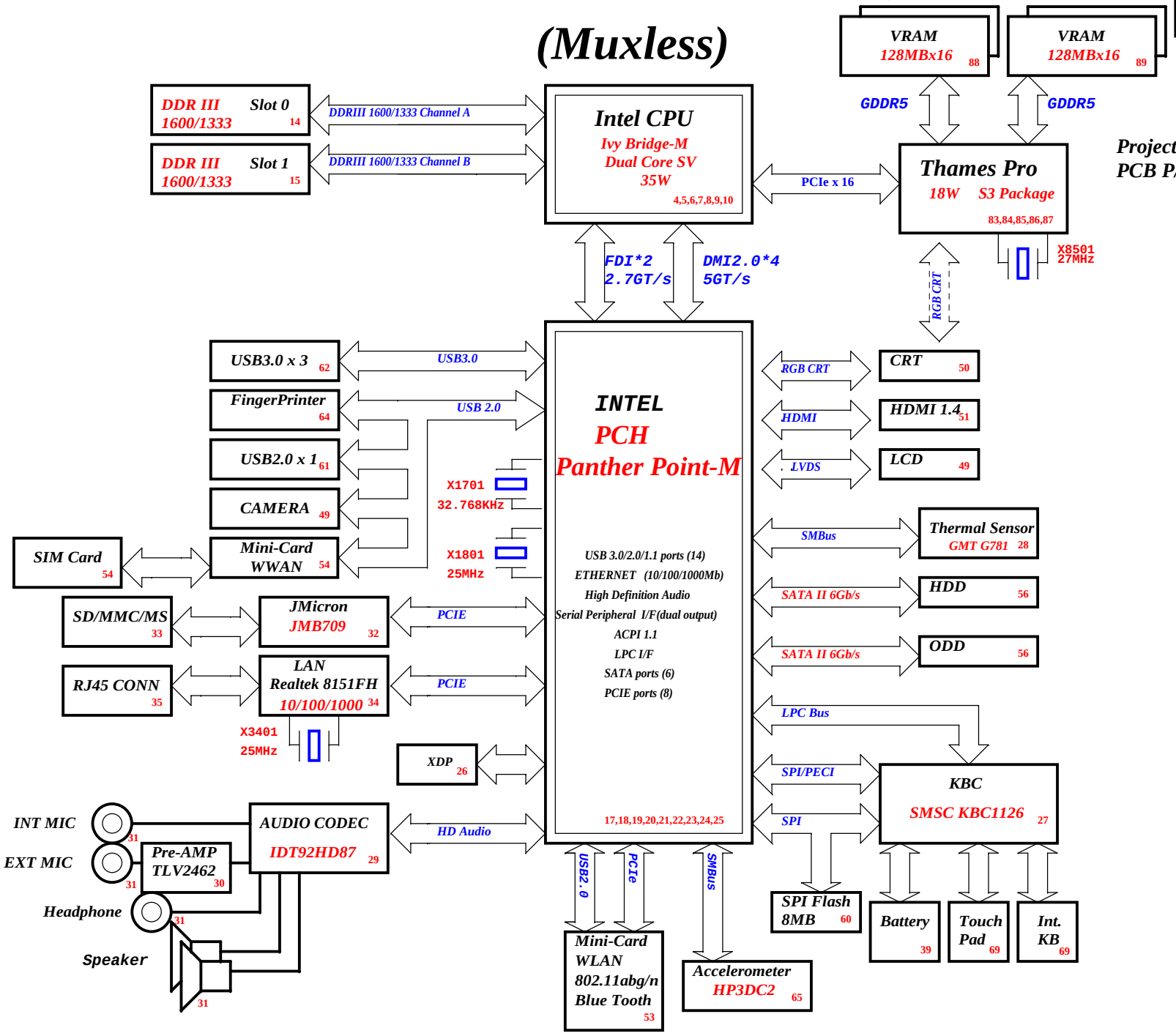
DY:No stuff
DIS_PX:Only DIS install

S-Series Richie Block Diagram (Muxless)



Project code:91.4RS01.001
PCB P/N:11241

SYSTEM DC/DC TPS51461RGER 48

INPUTS	OUTPUTS
DCBATOUT	+VCCSA

CPU DC/DC ISL95832HRTZ 42~44

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51211DSCR 45

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51123RGER 41

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51216RUKR 46

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC ISL95832HRTZ 42~44

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA UP1527QQDD 92

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24736RGRR 40

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8068AZQWID 47

INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC FDMC7696 93

INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0

Switches

INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB 8 LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Bottom

PCB LAYER

L1:Top	L5:Vcc
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

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Title: Block Diagram

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PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation: DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kOhms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kOhms ±5% pull-up resistor to PCH VccDFTERM.
SATA1GP/ GPIO19	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel? HD Audio dock signals to the corresponding Cougar Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform.
GPIO15	TLS Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected When '1'- Port B is detected; When '0'- Port B is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. Note: This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft trap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1K ohm resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2] CFG2 is for the 16x	**PCIe Static x16 Lane Numbering Reversal.**	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	1
CFG[4]	**Display Port Presence strap**	1:Disabled - No Physical Display Port attached to Embedded DisplayPort 0:Enabled - An external Display Port device is connected to the Embedded Display Port Pull down to GND through a 1KΩ ± 5% resistor to enable port	1
CFG[6:5]	**PCIE Port Bifurcation Straps**	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	11
CFG[17:7]	**Reserved configuration lands. A test point may be placed on the board for these lands.**		

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE VGA_CORE 1D8V_VGA_S0 3D3V_VGA_S0 1D5V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
1D5V_S3 DDR_VREF_S3	5V 1.5V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-14.1V 9V-19.5V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

PCIe Routing

LANE1	X
LANE2	X
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	LAN
LANE7	X
LANE8	X

USB 2.0 Table

Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

USB3.0 Table

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	N/A
3	N/A
4	N/A
5	N/A

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
DIMM1 DIMM2 Touch-Pad				PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA
N/A				PCH_SML0_CLK/PCH_SML0_DATA
KBC G781_Thermal IC GPU_Thames PRO G-Sensor		 1001100 0X41 0X52		PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA

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CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

DP Compensation, within 500mil

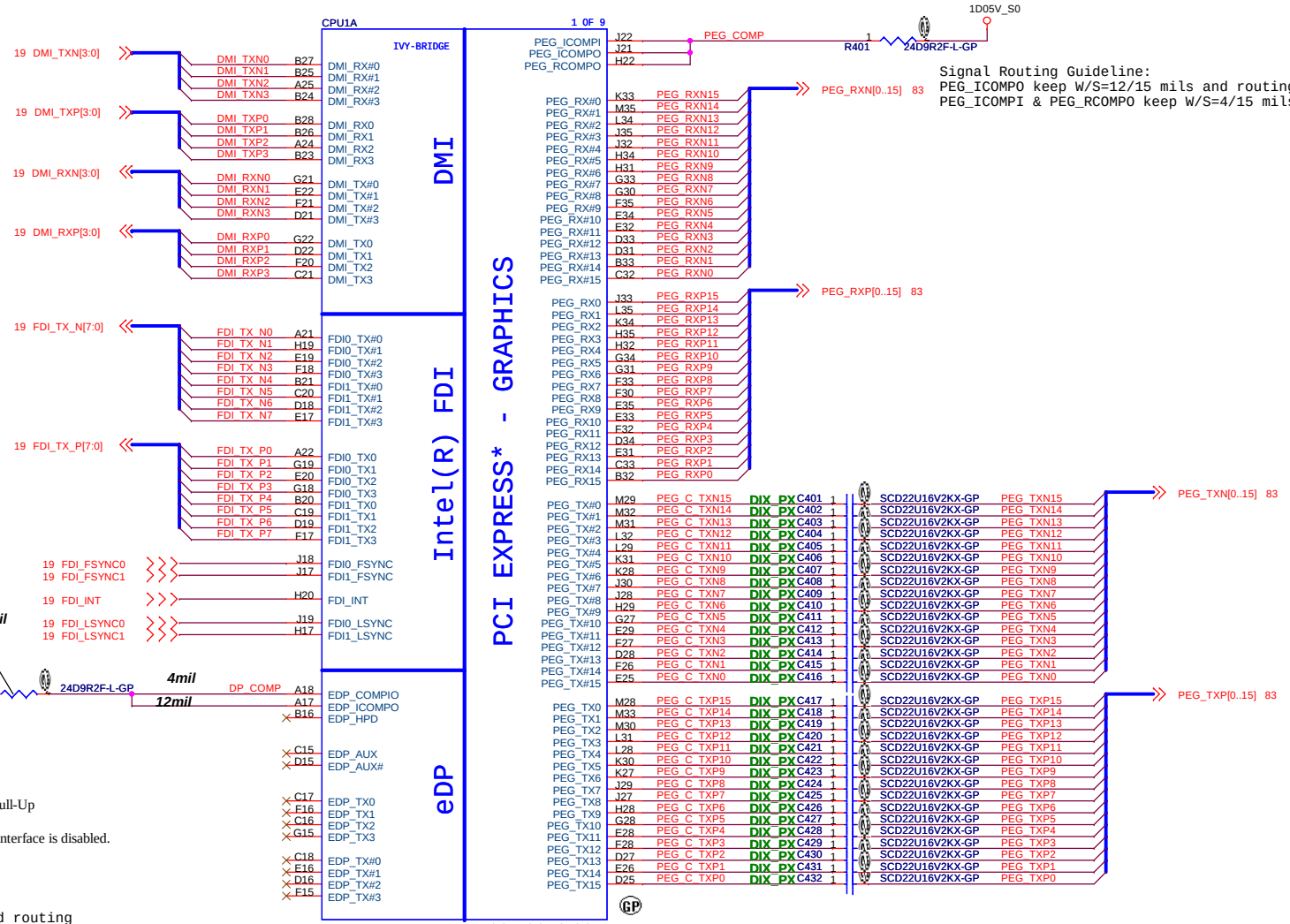
NOTE: EDP_HPD
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns.
If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

PEG Compensation

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



62.10040.821
1ST = 62.10055.551
2nd = 62.10055.321
3rd = 62.10055.731

BOM Note:1st/2nd/3rd Add in BOM

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Title: CPU(1/7): DMI/PEG/FDI

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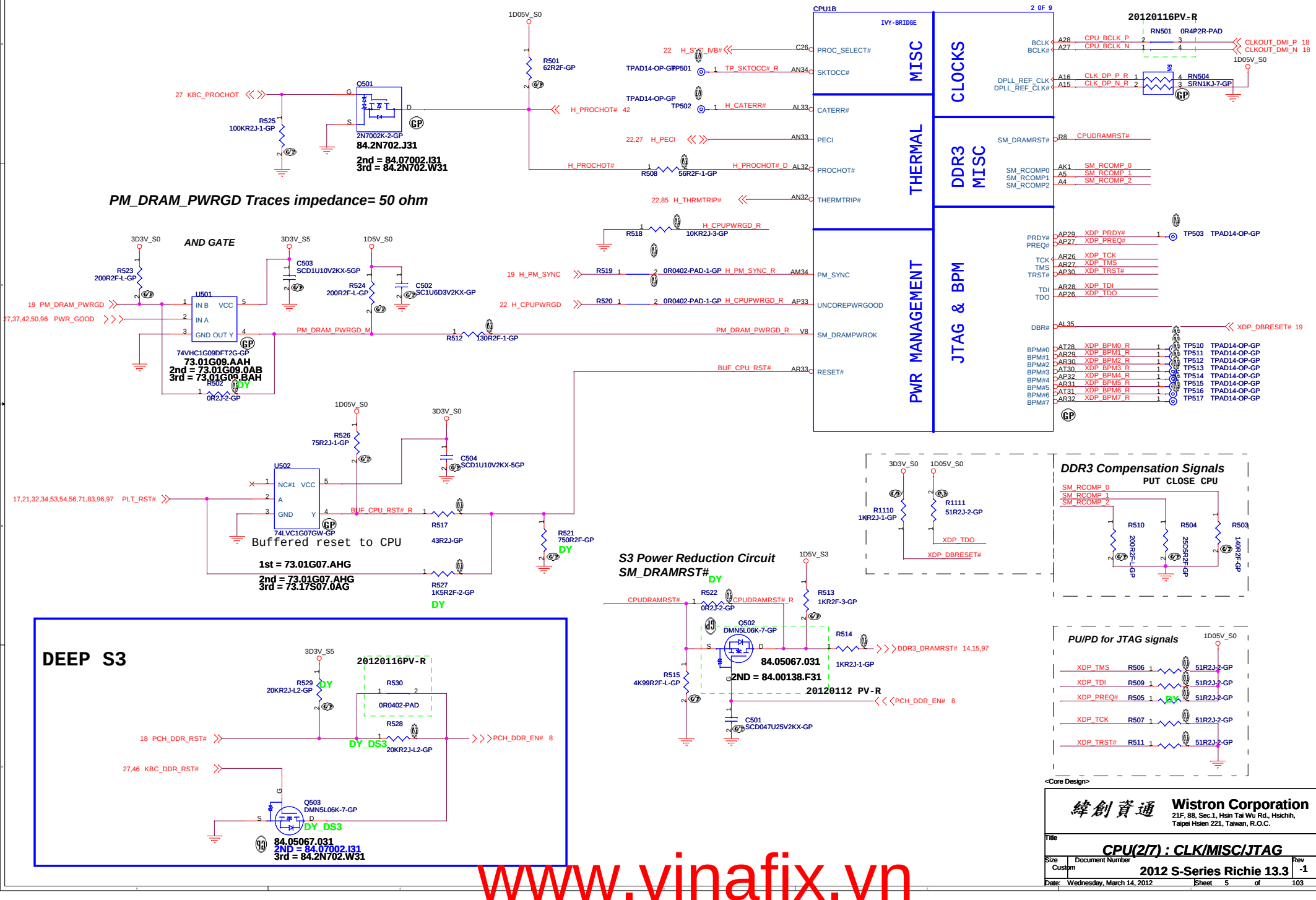
CPU(2/7)

IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



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Title: CPU(2/7) : CLK/MISC/JTAG

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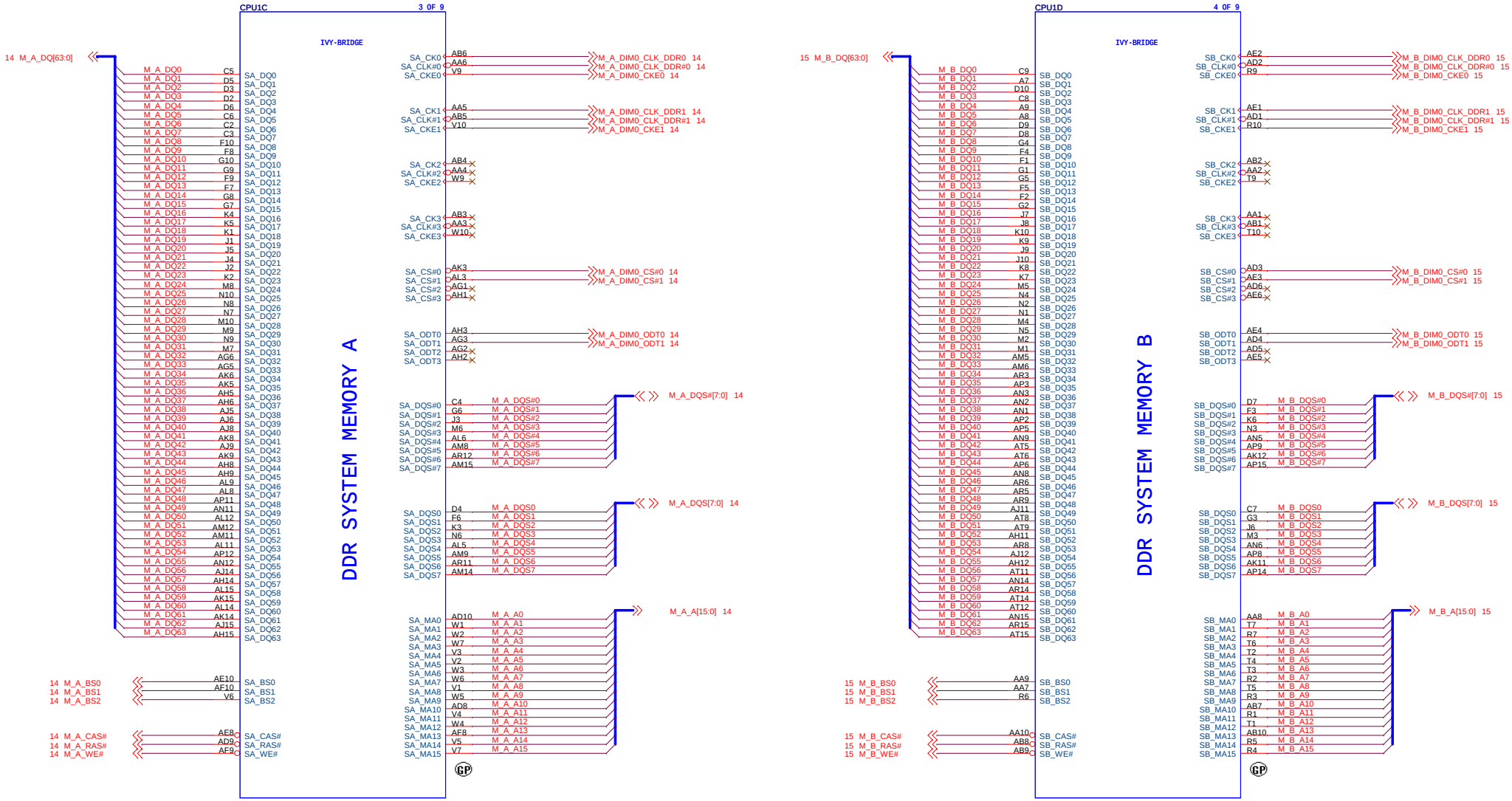
CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



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Title: CPU(3/7) : DDR3

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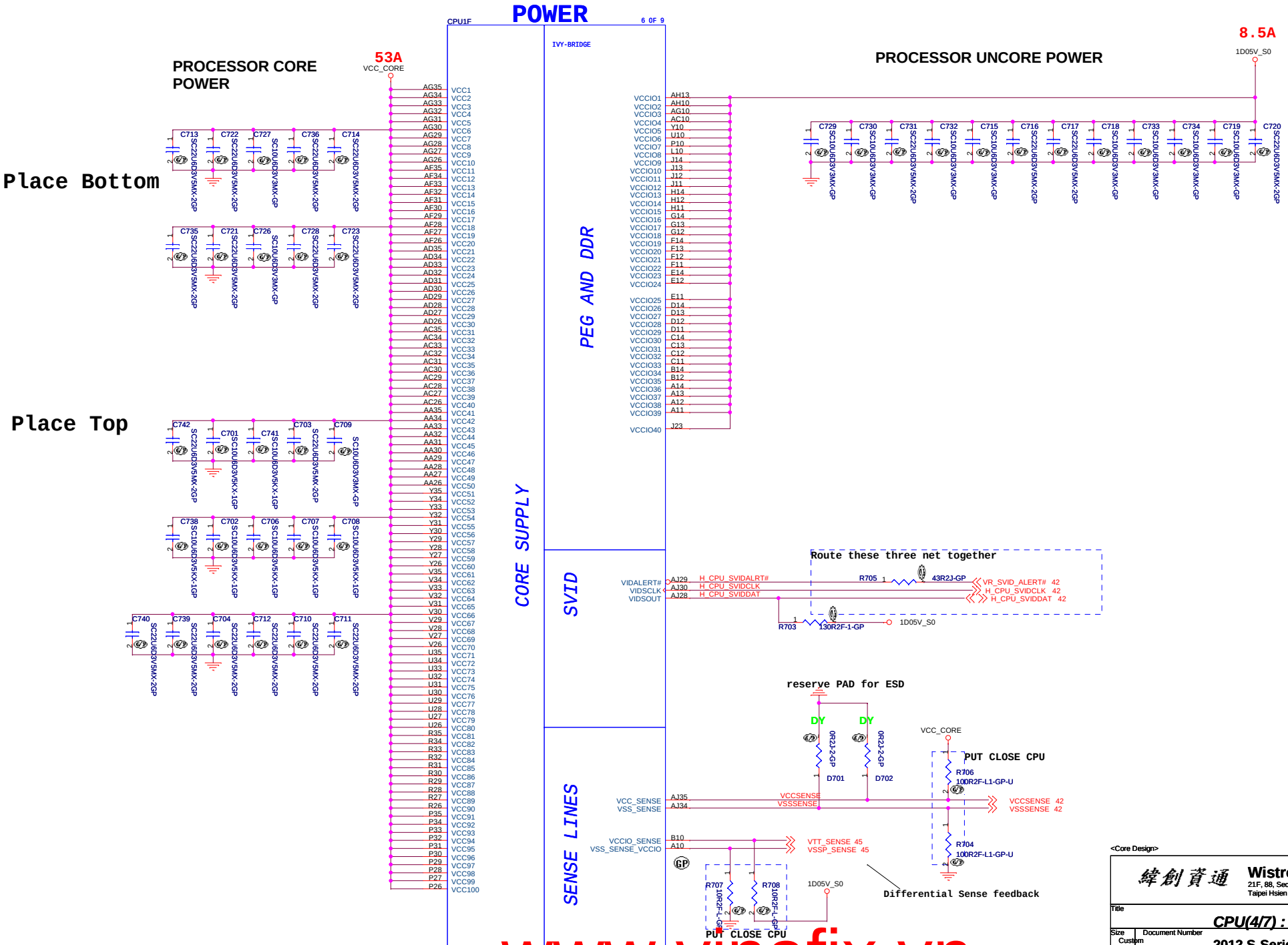
CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)



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CPU(5/7)

IVY BRIDGE PROCESSOR (GRAPHICS POWER)

33A

POWER

M3 - Processor Generated SO-DIMM VREF_DQ

CPU1G 7 OF 9

IVY-BRIDGE

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

GRAPHICS

VCC_GFXCORE

Under Socket and Closed to CPU

C820 SC22U6D3V5MX-2GP
C821 SC22U6D3V5MX-2GP
C822 SC22U6D3V5MX-2GP
C823 SC10U6D3V5KX-1GP
C824 SC22U6D3V5MX-2GP
C825 SC22U6D3V5MX-2GP

VCC_GFXCORE

Closed to CPU Socket

C826 SC10U6D3V5KX-1GP
C827 SC22U6D3V5MX-2GP
C828 SC22U6D3V5MX-2GP
C829 SC22U6D3V5MX-2GP
C830 SC22U6D3V5MX-2GP
C831 SC22U6D3V5MX-2GP

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

VAXG_SENSE AK35
VSSAXG_SENSE AK34

VCCGT_SENSE 42
VSSGT_SENSE 42

R820 100R2F-L1-GP-U
R819 100R2F-L1-GP-U

VCCGT_SENSE
VSSGT_SENSE

D801 0R2J-2-GP DY
D802 0R2J-2-GP DY

reserve PAD for ESD

CAD Note: +V_SM_VREF should have 10 mil trace width

SM_VREF AL1 +V_SM_VREF_CNT

B4:VREF_DQ CHA
D1:VREF_DQ CHB

SA_DIMM_VREFDQ B4 DDR_VREF_S3_B4
SB_DIMM_VREFDQ D1 DDR_VREF_S3_D1

R815 1KR2F-3-GP DY
R816 1KR2F-3-GP DY

C801 SC2D2U10V2ZY-2GP DY
C802 SC2D2U10V2ZY-1GP

14 M_VREF_DQ_DIMM0
15 M_VREF_DQ_DIMM1

20120112 PV-R

1st = 84.05067.031
2nd = 84.00138.F31
3rd = 84.05067.031

PCH_DDR_EN# G
Q802 AP2302GN-HF-GP
R810 0R2J-2-GP DY

Q803 AP2302GN-HF-GP
R814 0R2J-2-GP DY

DDR_VREF_S3_B4
DDR_VREF_S3_D1

5 PCH_DDR_EN#

12~16A

1D5V_S0

330U*1 10U*6

VDDQ1 AE7
VDDQ2 AE4
VDDQ3 AE1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

C803 SC10U6D3V5MX-GP
C804 SC10U6D3V5KX-1GP
C805 SC10U6D3V5KX-1GP
C806 SC10U6D3V5KX-1GP
C807 SC10U6D3V5KX-1GP
C808 SC10U6D3V5KX-1GP

TC803 ST330U2D5VBM-1-GP
80.3371V.A2L
2nd = 77.22771.00L
20120131PVR

6A

VCCSA

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

C813 SC10U6D3V5KX-1GP
C814 SC10U6D3V5KX-1GP
C815 SC10U6D3V5KX-1GP
TC802 SE330U2D5VDM-1GP DY

1st = 77.23371.13L
2ND = 79.33719.L01

VCCSA

R0801 need be close to pin H23.

R801 100R2J-2-GP DY

VCCSA_SENSE H23
VCCUSA_SENSE

VCCUSA_SENSE 48

1.5A

1D8V_S0

B6 VCCPLL1
A6 VCCPLL2
A2 VCCPLL3

C819 SC10U6D3V5KX-1GP DY
C816 SC10U6D3V5KX-1GP
C817 SC1U10V2KX-1GP
C818 SC1U10V2KX-1GP

VCCSA_VID0 C22
VCCSA_VID1 C24

H_FC_C22
VCCSA_SEL

H_FC_C22 48
VCCSA_SEL 48

R804 1KR2J-1-GP
R806 1KR2J-1-GP

VCCIO_SEL A19 H_VCCP_SEL

SNB: No Connect
IVB: VSS

R817 0R2J-2-GP DY
R818 0R2J-2-GP DY

H_SNB_IVB#_PWRCTRL 45

H_VCCP_SEL	Voltage
1	1.05V
0	1.0V

S3 Power Reduction Circuit Processor VREF_DQ Implementation

1D5V_S3
R821 1KR2F-3-GP DY
R822 1KR2F-3-GP DY

DDR_VREF_S3
20120112 PV-R
R807 0R0402-PAD

R811 0R2J-2-GP DY

Q801 DMN5L06K-7-GP

+V_SM_VREF
84.05067.031
1st = 84.2N702.J31
2ND = 84.07002.I31
3rd = 84.2N702.W31

+V_SM_VREF_CNT

R803 100KR2J-1-GP

R802 0R2J-2-GP DY

5 PCH_DDR_EN#

20120112 PV-R

R823 0R0402-PAD

C832 SC470P50V2KX-2GP

19,27,29,34,35,36,37,45,46,47,48,92,93 PM_SLP_S3#

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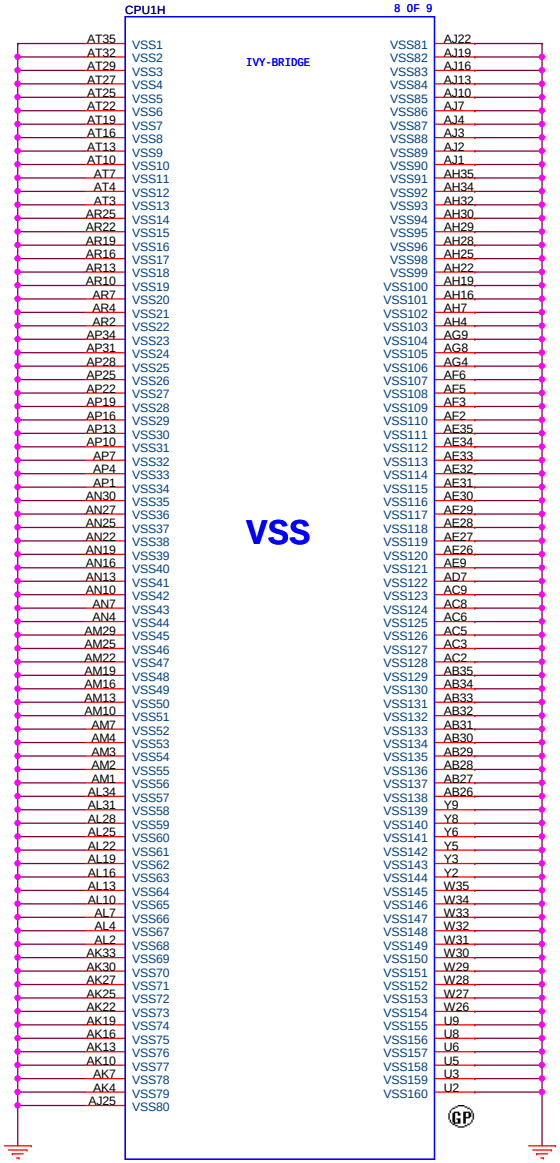
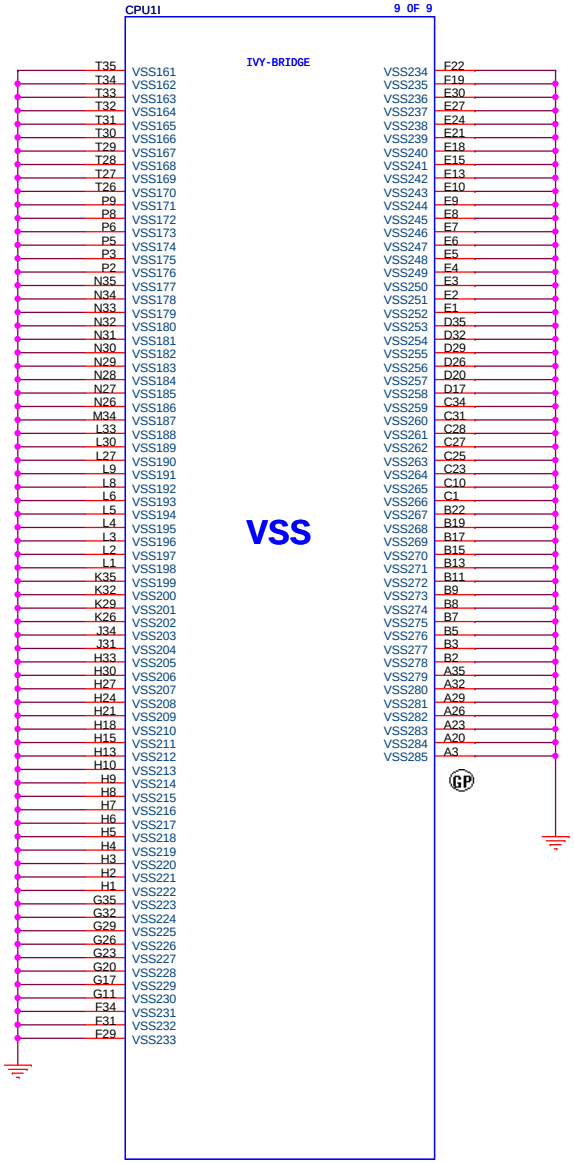
CPU(6/7)

IVY BRIDGE PROCESSOR (GND)





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Title: **CPU(6/7) : GND**

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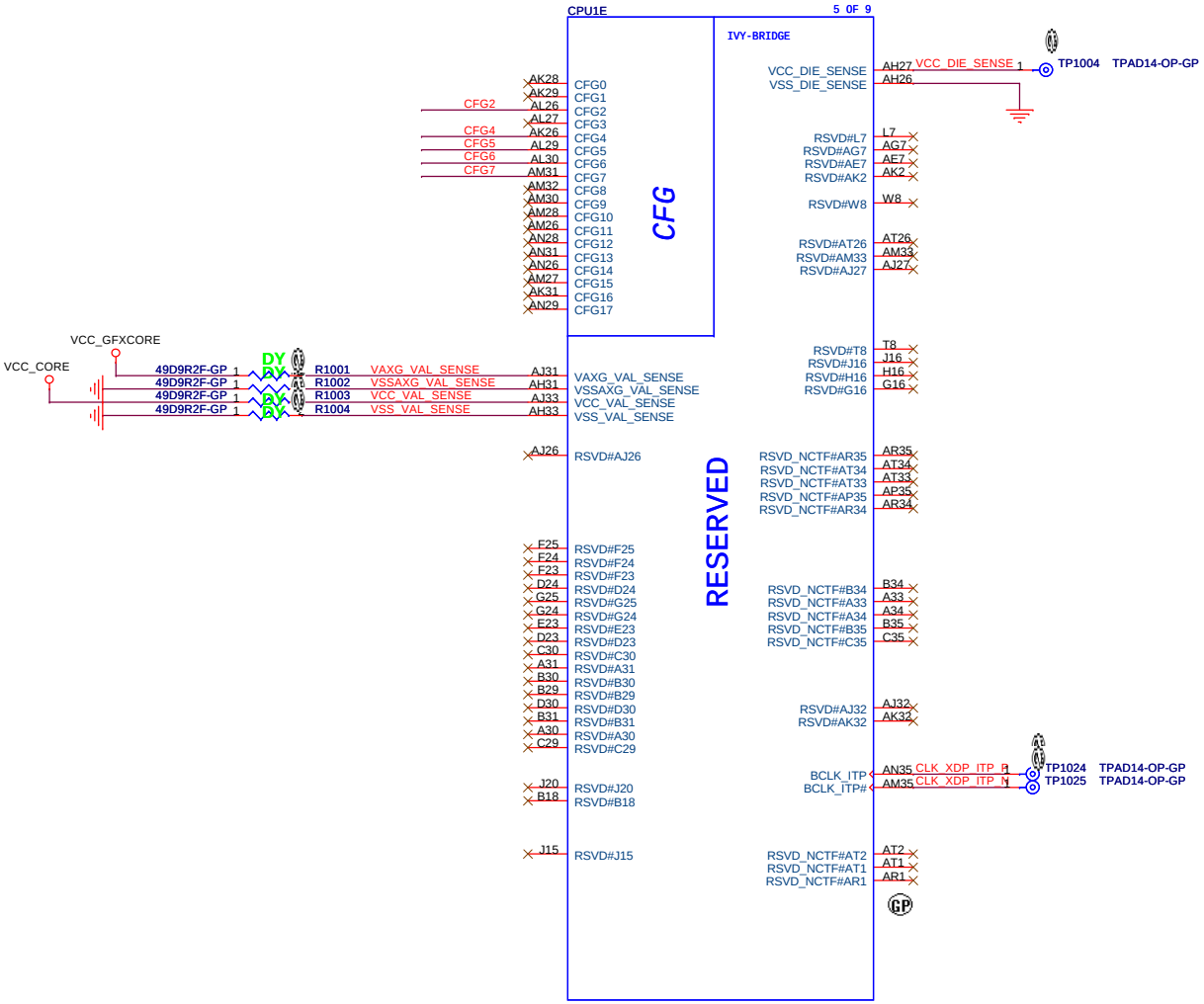
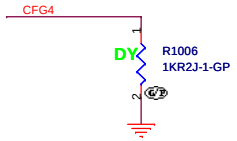
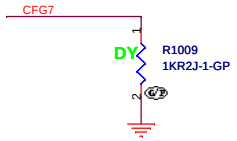
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)

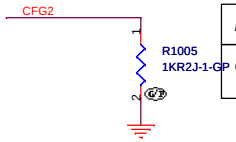




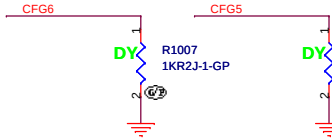
Display Port Presence Strap	0:Enable eDP
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Title: CPU(7/7): CFG/RSVD/DDR3_VREF

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 10 of 103

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<Core Design>

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Title: CPU XDP

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 11 of 103

(Blanking)

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Title: RESERVED

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 12 of 103

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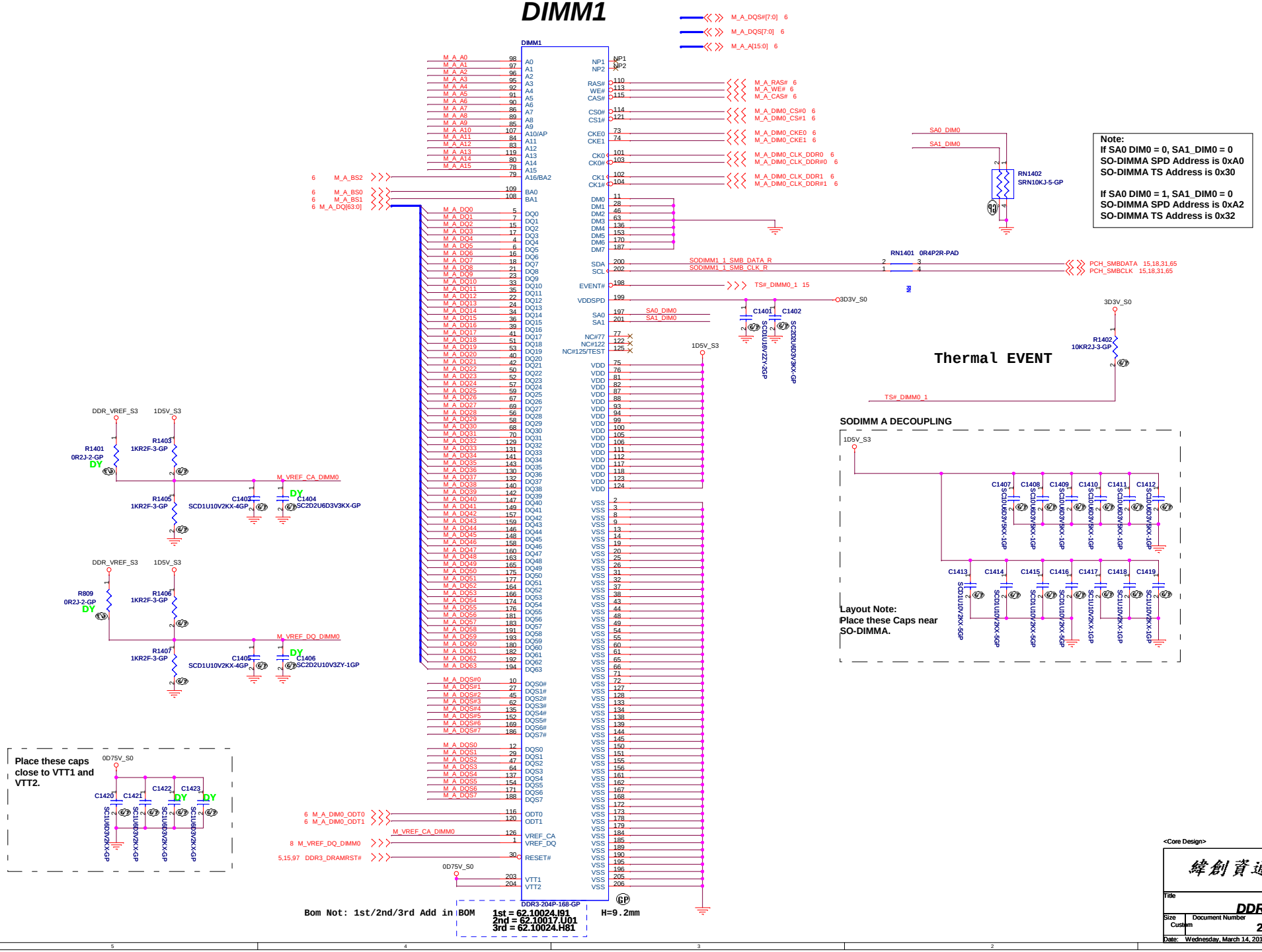
Title: RESERVED

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 13 of 103

DIMM1



<Core Design>

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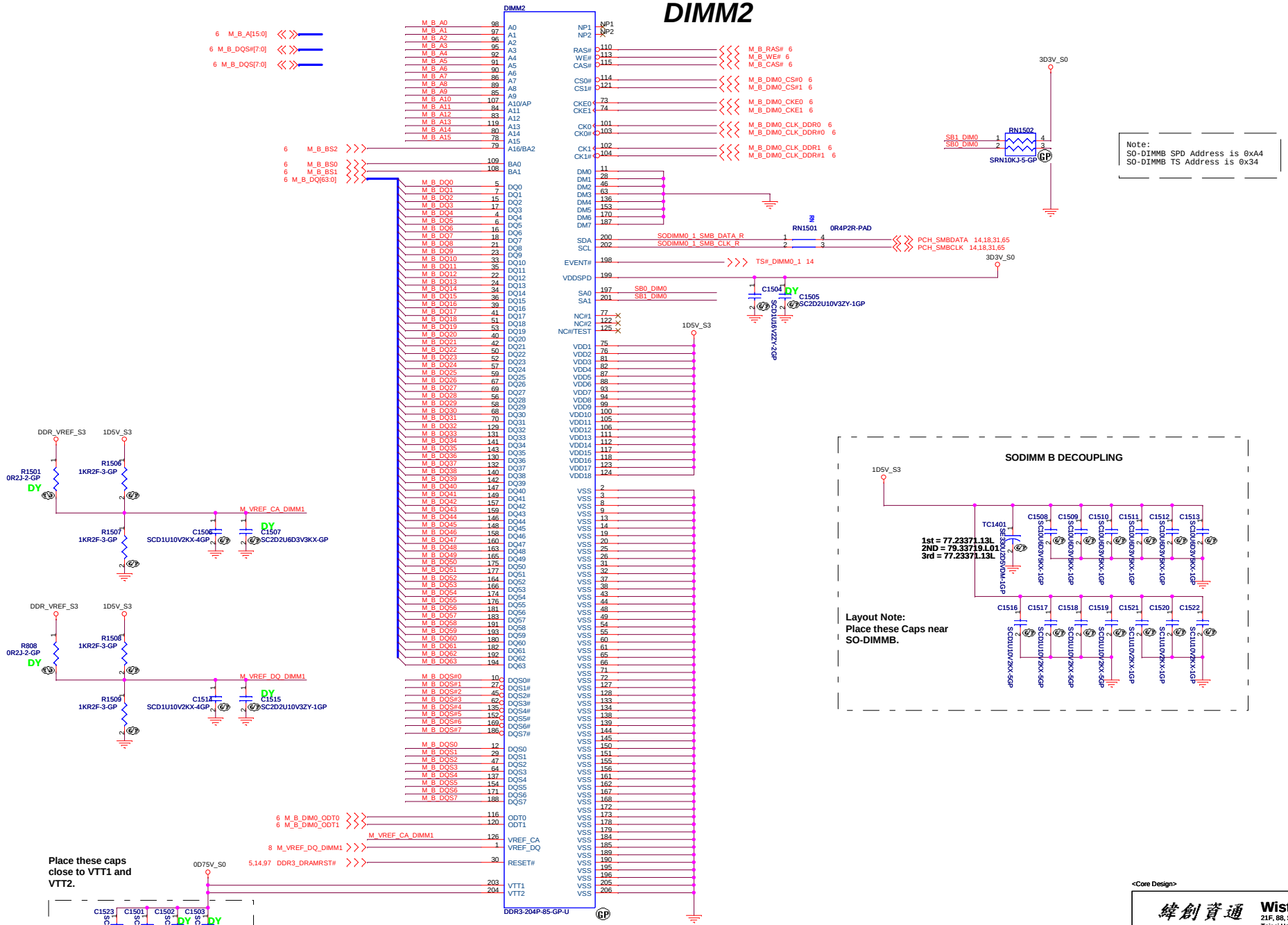
Title: DDR3 SO-DIMM1

Size: Custom | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 14 of 103

DIMM2



<Core Design>

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Title: DDR3 SO-DIMM2

Size	Document Number	Rev
Custom	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 15 of 103

(Blanking)

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Title: ***RESERVED***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 16 of 103

PCH(1/9)

INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable internal VRs

PCH1A — 1 OF 10 — PANTHER-GP-NF

RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN

LPC_AD[3:0] 27,71
FWH0/LAD0 C38 LPC_AD0
FWH1/LAD1 A38 LPC_AD1
FWH2/LAD2 B37 LPC_AD2
FWH3/LAD3 C37 LPC_AD3
FWH4/LFRAME# D36 LPC_FRAME# R 1 R1726 22R2J-2-GP LPC_FRAME# 27,71
LDRQ0# E36
LDRQ1#/GPIO23 K36 PCH_GPIO23 1 TP1701 TPAD14-OP-GP
SERIRQ V5 SIRQ 27,71

HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
PCH_HDA_SPKR T10 SPKR
PCH_HDA_RST# K34 HDA_RST#
HDA_SYNC_C
E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
HDA_SDO_R
HDA_SDO A36 HDA_SDO
HDD_HALTLED_R C36 HDA_DOCK_EN#/GPIO33
ISO_PREP# N32 HDA_DOCK_RST#/GPIO13

SATA0RXN AM3 SATA_RXN0 56
SATA0RXP AM1 SATA_RXP0 56
SATA0TXN AP7 SATA_TXN0 56
SATA0TXP AP5 SATA_TXP0 56 HDD
SATA1RXN AM10 SATA_RXN1 56
SATA1RXP AM8 SATA_RXP1 56
SATA1TXN AP11 SATA_TXN1 56
SATA1TXP AP10 SATA_TXP1 56 ODD
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP R1713 1 2 37D4R2F-GP 1D05V_S0
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP R1714 1 2 49D9R2F-GP 1D05V_S0
SATA3RBIAS AH1 RBIAS_SATA3 1 R1715 750R2F-GP
NEED TO PLACE CLOSE TO PCH
SATALED# P3 SATA_LED# 3D3V_S0 R1716 10KR2J-3-GP SATA_LED# 68
SATA0GP/GPIO21 V14 SATA0GP_GPIO21 22
SATA1GP/GPIO19 P1 SATA_ODD_DET# 56

PCH_JTAG_TCK_BUF J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO

60 PCH_SPI_CLK T3 SPI_CLK
60 PCH_SPI_CS#0 Y14 SPI_CS0#
27,71 SPI_CS1# T1 SPI_CS1#
60 PCH_SPI_MOSI V4 SPI_MOSI
60 PCH_SPI_MISO U3 SPI_MISO

X1701 X-32D768KHZ-34GPU
C1702 C1703 7pF20PPM SC6P50V2CN-1GP
82.30001.661
2ND = 82.30001.B21
20120312MV

R1706 10MR2J-L-GP
RTC_AUX_S5 R1705 20KR2J-L2-GP C1701 SC1U10V2KX-1GP
R1707 DY PCH_INTVRMEN 330KR2J-L1-GP
RTC_AUX_S5 R1708 20KR2J-L2-GP C1704 SC1U10V2KX-1GP G1701 GAP-OPEN
54,97 INTRUDER#
RTC_AUX_S5 R1709 1MR2J-1-GP R1710 330KR2J-L1-GP PCH_INTVRMEN
RN1701 SRN33J-7-GP
R1711 0R0402-PAD
20120112 PV-R

29,97 HDA_SDOUT_CODEC
29,97 HDA_BITCLK_CODEC
29,97 HDA_RST#_CODEC
29 HDA_SYNC_CODEC
29 HDA_SPKR
29 HDA_SDIN0_CODEC
68 HDD_HALTLED
R1712 1KR2J-1-GP

3D3V_S5 R1725 1KR2J-1-GP
BAT_GRNLED# S
BAT_GRNLED# D
10KR2J-3-GP R1701
27,82 BAT_GRNLED# G
84.00084.F31
2nd = 84.BSS84.B31
BSS84-7-F-GP Q1701

10KR2J-3-GP R1702
5,21,32,34,53,54,56,71,83,96,97 PLT_RST# G
84.00084.F31
2nd = 84.BSS84.B31
BSS84-7-F-GP Q1702

3D3V_S5 R1724 1KR2J-1-GP HDA_SYNC
R1729 10KR2J-3-GP ISO_PREP#

For Flash Descriptor Security Override HW strap

RTC Battery

RTC1 PWR GND NP1 NP2 BAT-060003HA002M213ZL-GP-U
62.70014.001
2nd = 62.70001.061
20120314 MV
20120315 MV

+RTC_VCC R1720 RTC_PWR 1KR2J-1-GP
3D3V_AUX_S5 U1701 CH715FGP-GP-U
RTC_AUX_S5 C1705 SC1U10V3ZY-6GP
83.R0304.D81
2ND = 83.00040.E81
20120210PV-R

NO REBOOT STRAP

No Reboot Strap R710	
HDA_SPKR	Low = Default High = No Reboot

3D3V_S0 R1722 10KR2J-3-GP HDA_SPKR DY
R1723 10KR2J-3-GP SIRQ

5V_S0 RN1702 SRN10KJ-5-GP
HDA_SDO_G U1704 2N7002KDW-GP
HDA_SYNC_C HDA_SYNC
HDA_SDO HDA_SDO_R
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F

3D3V_S5
PCHXDP R1717 210R2F-L-GP PCH_JTAG_TMS
PCHXDP R1718 210R2F-L-GP PCH_JTAG_TDO
PCHXDP R1719 210R2F-L-GP PCH_JTAG_TDI
RN1703
PCHXDP PCH_JTAG_TDO PCH_JTAG_TDI PCH_JTAG_TMS
SRN100J-4-GP
PCHXDP R1721 51R2J-2-GP PCH_JTAG_TCK_BUF
R1727 DY 1KR2J-1-GP HDD_HALTLED_R
R1728 20KR2J-L2-GP HDA_SDO

LAYOUT NOTE:
JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
JTAG_TCK TERMINATIONS NEED TO BE PLACED NEAR PCH

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Title: PCH(1/9) : HDA/JTAG/SATA
Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1
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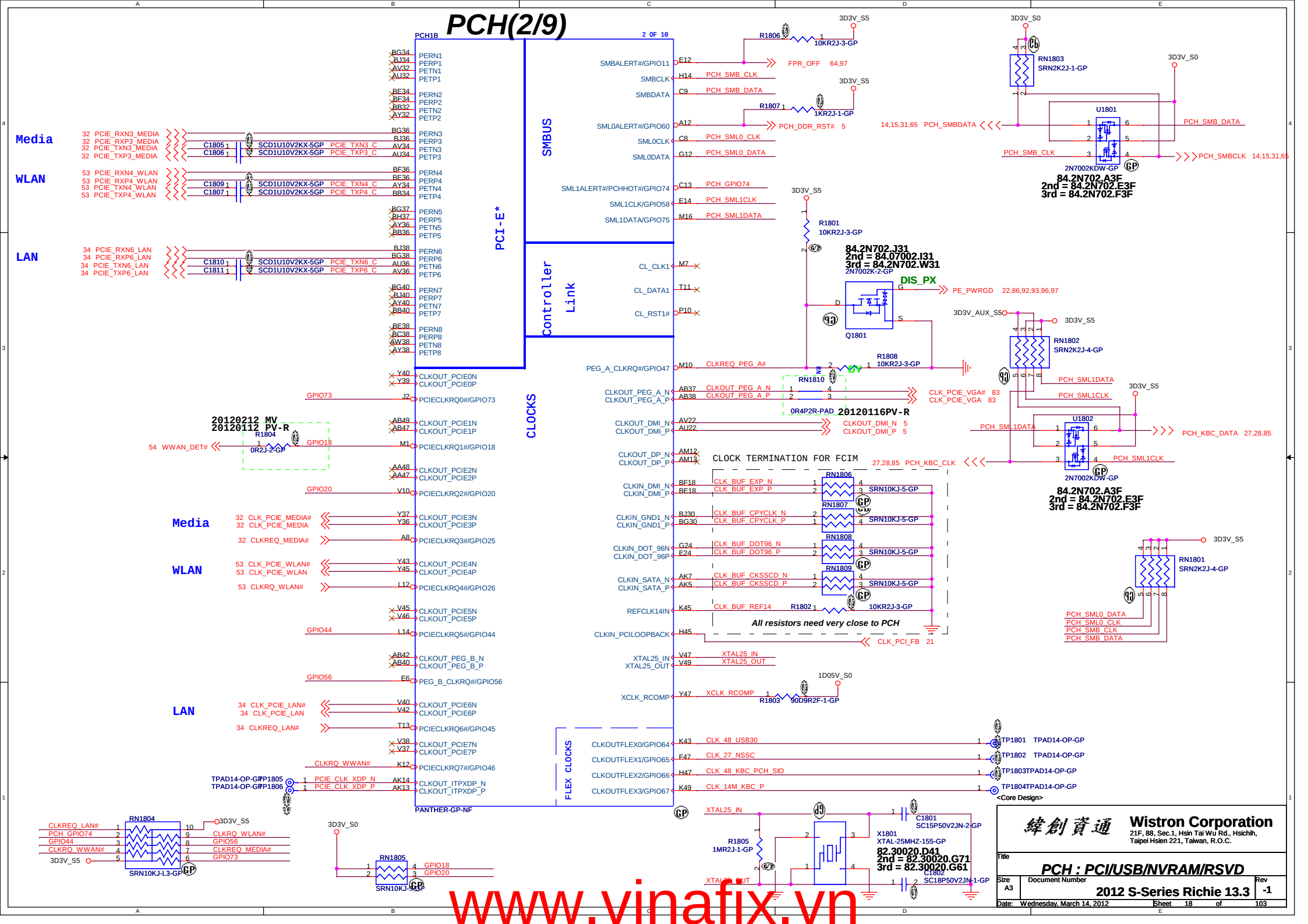
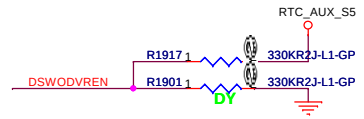
PCH(2/9)



PCH(3/9)

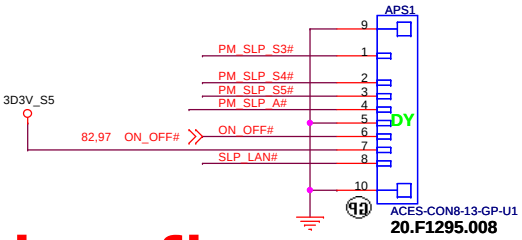
DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED	Enabled (DEFAULT)
LOW (R1901 STUFFED, R1917 UNSTUFFED	Disabled



Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecrive.

AMT/ME COMPLIANCY TEST CONN.



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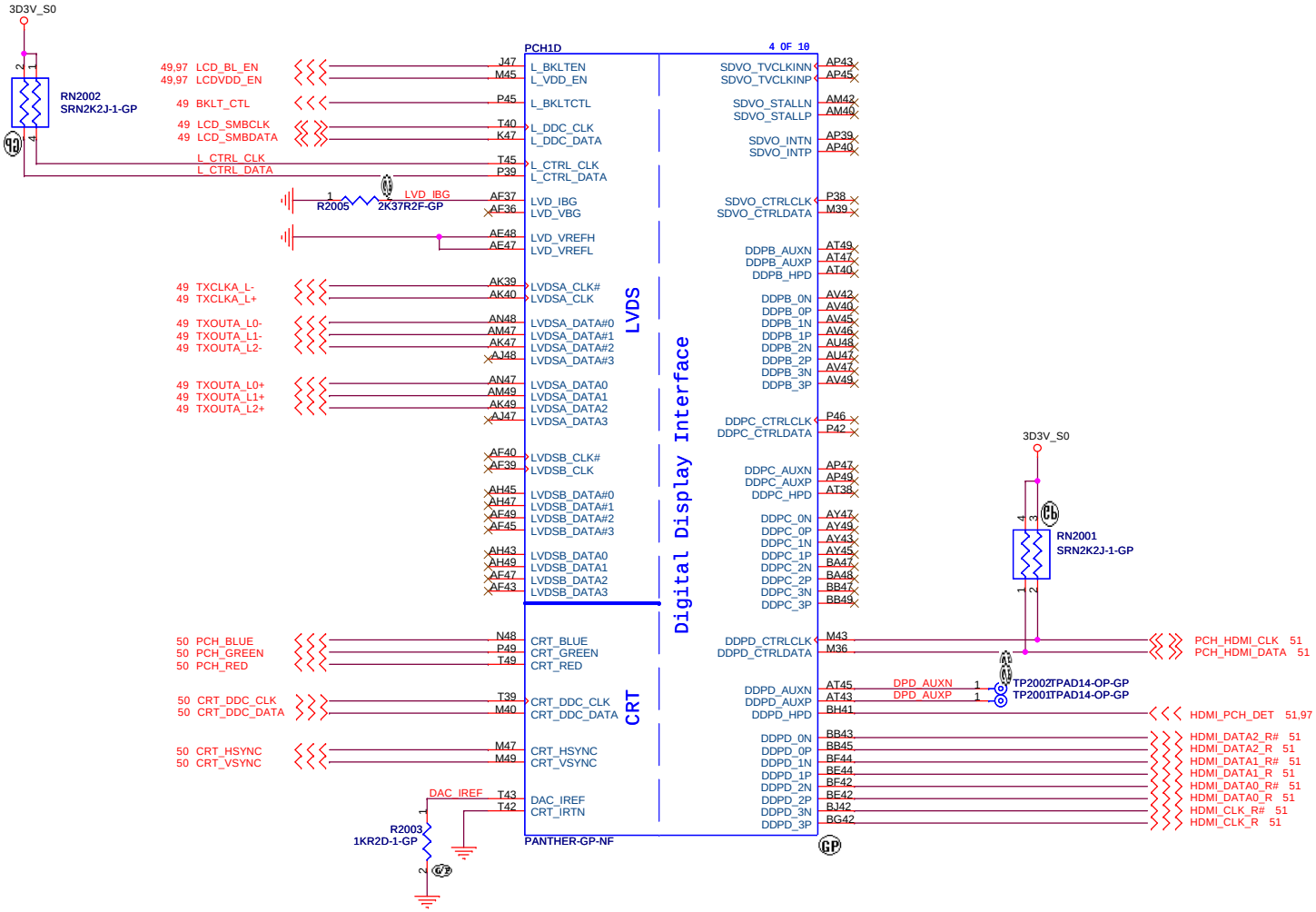
Title: PCH(3/9) : DMI/FDI/PM

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 19 of 103

PCH(4/9)



<Core Design>

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Title: **PCH(4/9) : LVDS/CRT/DDI**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 20 of 103

PCH(5/9)

GPIO Table

S 2012 Chief River	PCH GPIO 52
Richie U&D (13 inches)	1
Rocky U&D (14 inches)	1
Rocky U&D (15/17 inches)	0

Boot BIOS Strap

GNT1#/GPIO51	SATA1GP#/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

USB3.0 Table

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

USB2.0 Table

USB	
Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

PCH1E 5 OF 10

RSVD: RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 RSVD15 RSVD16 RSVD17 RSVD18 RSVD19 RSVD20 RSVD21 RSVD22 RSVD23 RSVD24 RSVD25 RSVD26 RSVD27 RSVD28 RSVD29

TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24

USB3RN1 USB3RN2 USB3RN3 USB3RN4 USB3RP1 USB3RP2 USB3RP3 USB3RP4 USB3TN1 USB3TN2 USB3TN3 USB3TN4 USB3TP1 USB3TP2 USB3TP3 USB3TP4

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P

USB 3.0 Conn. 1 — USB_PN1 62, USB_PP1 62
USB 3.0 Conn. 2 — USB_PN2 62, USB_PP2 62
USB 3.0 Conn. 3 — USB_PN3 62, USB_PP3 62
BT WLAN combo — USB_PN5 53, USB_PP5 53
Fingerprint — USB_PN8 64, USB_PP8 64
USB 2.0 Conn. 1 — USB_PN9 61, USB_PP9 61
Camera — USB_PN10 49, USB_PP10 49
WWAN — USB_PN12 54, USB_PP12 54

USB_BIAS, R2101 22D6R2F-L1-GP

PIRQA# PIRQB# PIRQC# PIRQD# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54 GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55 PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5 PME# PLTRST#

CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO9 OC6#/GPIO10 OC7#/GPIO14 — LANLINK_STATUS 35

PANTHER-GP-NF

PCI bus, USB bus

20120112 PV-R

R2106 0R0402-PAD PCH_GPIO50 PLT_DET_R PE_GPIO1

R2102 PME# 10KR2J-3-GP

R2103 R2105 22R2J-2-GP TPAD14-OP-GP TP2108 TP2106 R2107 22R2J-2-GP CLK_PCI_SIO_R CLK_PCI_FB_R CLK_OUT_PCI2 CLK_OUT_PCI3 CLK_PCI_KBC_R

R2113 R2109 R2112 10KR2J-3-GP PCH_GPIO51 PE_GPIO0

R2110 10KR2J-3-GP CAMERA_ON

RN2101 SRN8K2J-GP ACCEL_INT NMI_SMI_DBG#

RN2102 SRN8K2J-2-GP INT_PIRQA# INT_PIRQD# INT_PIRQB# INT_PIRQC# PE_GPIO1 PCH_GPIO2 PLT_DET_R PCH_GPIO50

U2101 AND GATE U74LVC1G08G-AL5-R-GP-U 73.01G08.EHG 2nd = 73.7SZ08.EAH 3rd = 73.01G08.L04

R2104 0R2J-2-GP PLT_RST# 5,17,32,34,53,54,56,71,83,96,97

R2108 100KR2J-1-GP

RN2104 SRN10KJ-6-GP OC4# GPIO43 OC1# GPIO40 OC2# GPIO41 OC3# GPIO42

RN2103 SRN10KJ-6-GP OC5# GPIO9 LANLINK_STATUS OC7# GPIO14 OC0# GPIO59

<Core Design>

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Title: PCH(5/9) : PCI/USB/NVM

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 21 of 103

PCH(6/9)

VRAM ID TABLE

PCH_GPIO39	PCH_GPIO38	VENDER
0	1	Samsung
1	0	Hynix
1	1	Elpida
0	0	UMA

GDDR5/DDR3 TABLE

20110822SI

2012 Chief River	PCH GPIO 12
Richie U&D (13 inches)	0 (13") GDDR5
Rocky U&D (14 inches)	1(14",15",17")DDR3
Rocky U&D (15/17 inches)	1(14",15",17")DDR3

PROC_SELECT

DMI & FDI Termination Voltage

DF_TVS	SNB: "1" IVB: "0"

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

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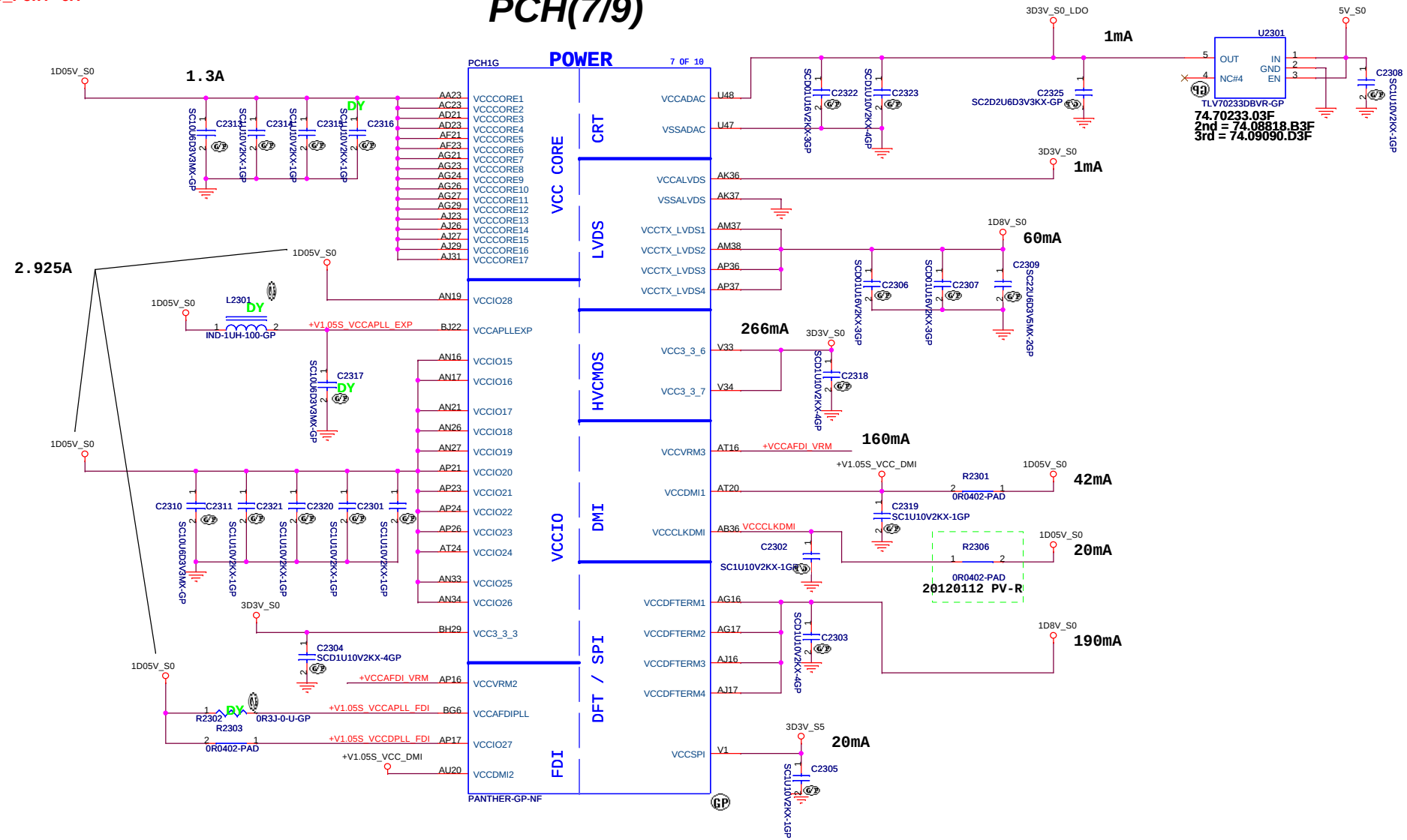
Title: PCH(6/9) : GPIO/NTCF/RSVD
Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1
Date: Wednesday, March 14, 2012 | Sheet 22 of 103

VCC_PCH: 6A

PCH(7/9)



<Core Design>

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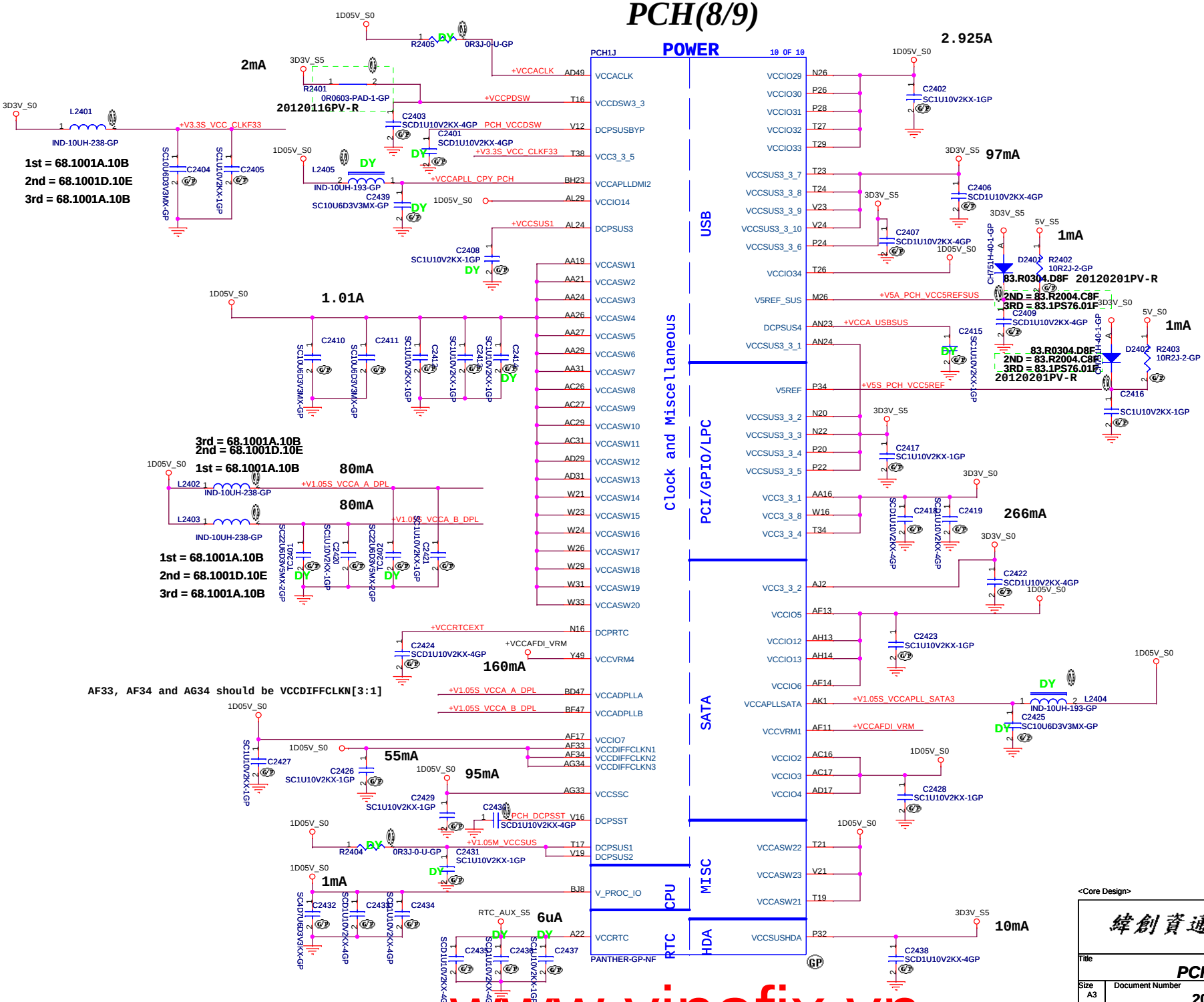
Title: PCH(7/9) : PWR1

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 23 of 103

PCH(8/9)



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(8/9) : PWR2

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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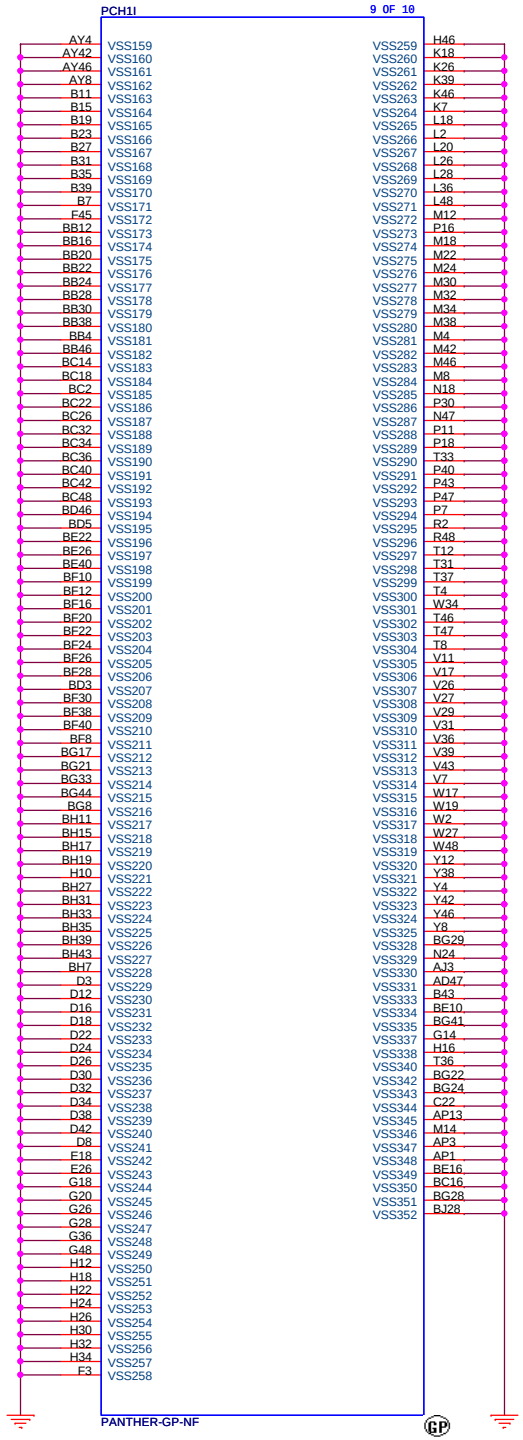
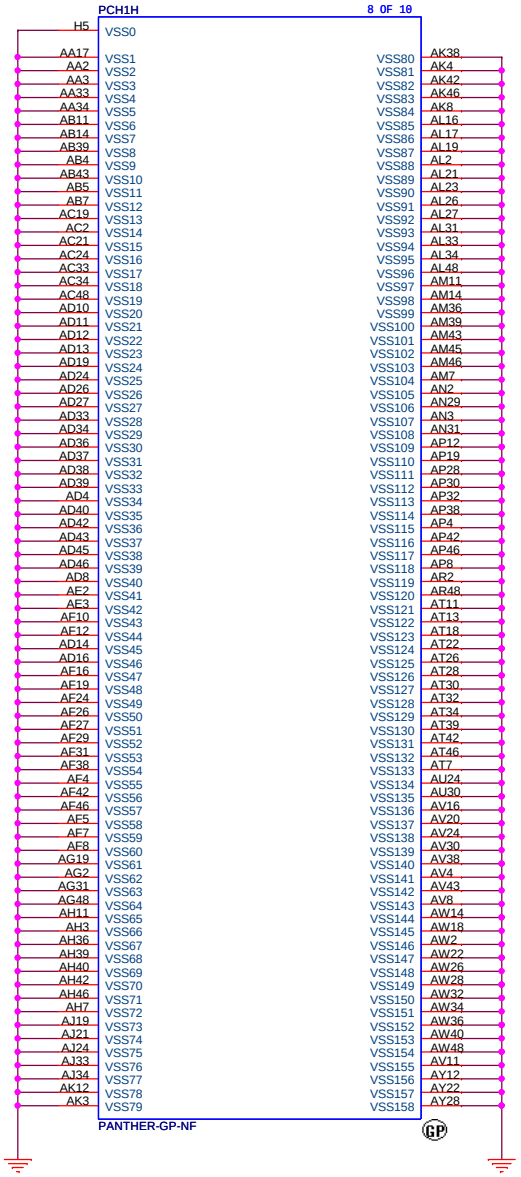
PCH(9/9)





<Core Design>

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Title: PCH(9/9) : GND

Size	Document Number	Rev
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(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: PCH XDP

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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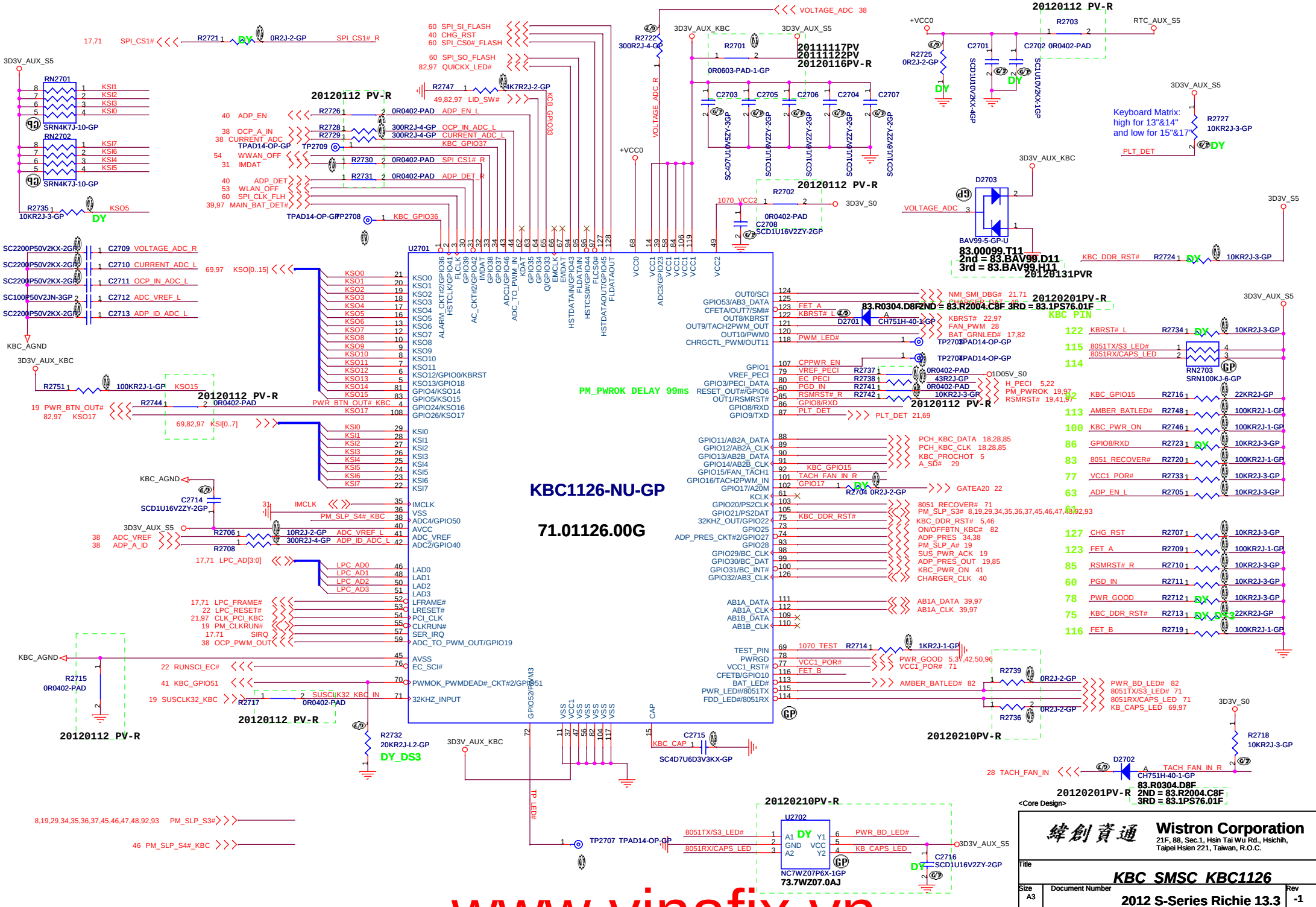
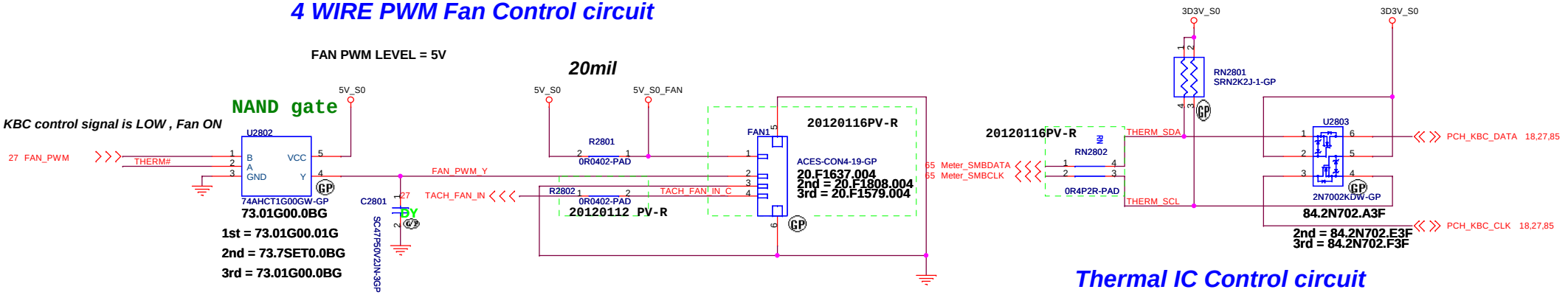
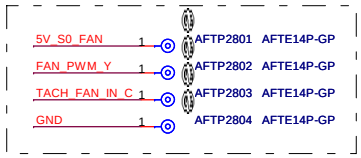


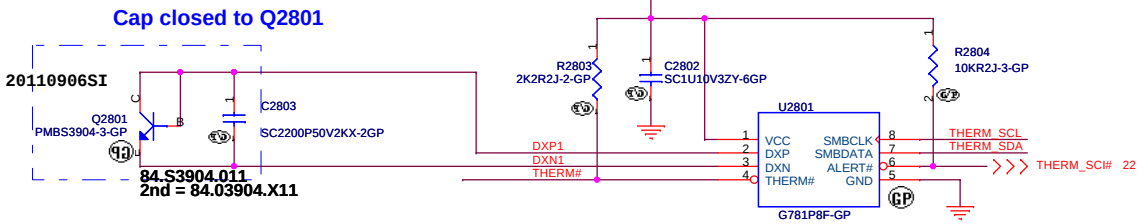
4 WIRE PWM Fan Control circuit



A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

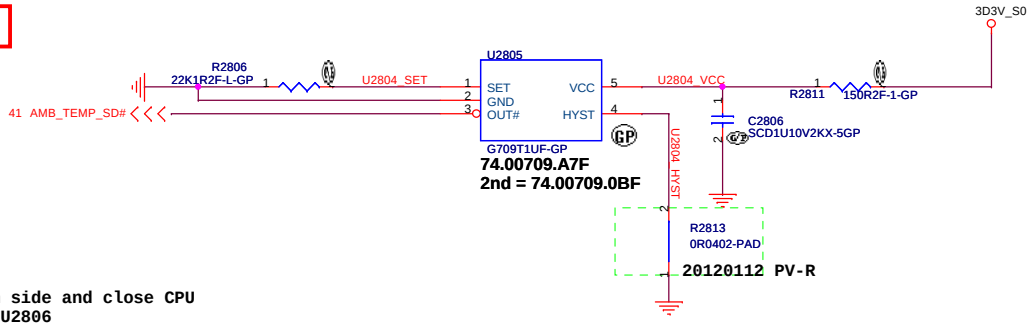


Thermal IC Control circuit



T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K



Layout: PUT U2805 Bottom side and close CPU
PUT R2806 Close U2806

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal G781 / FAN

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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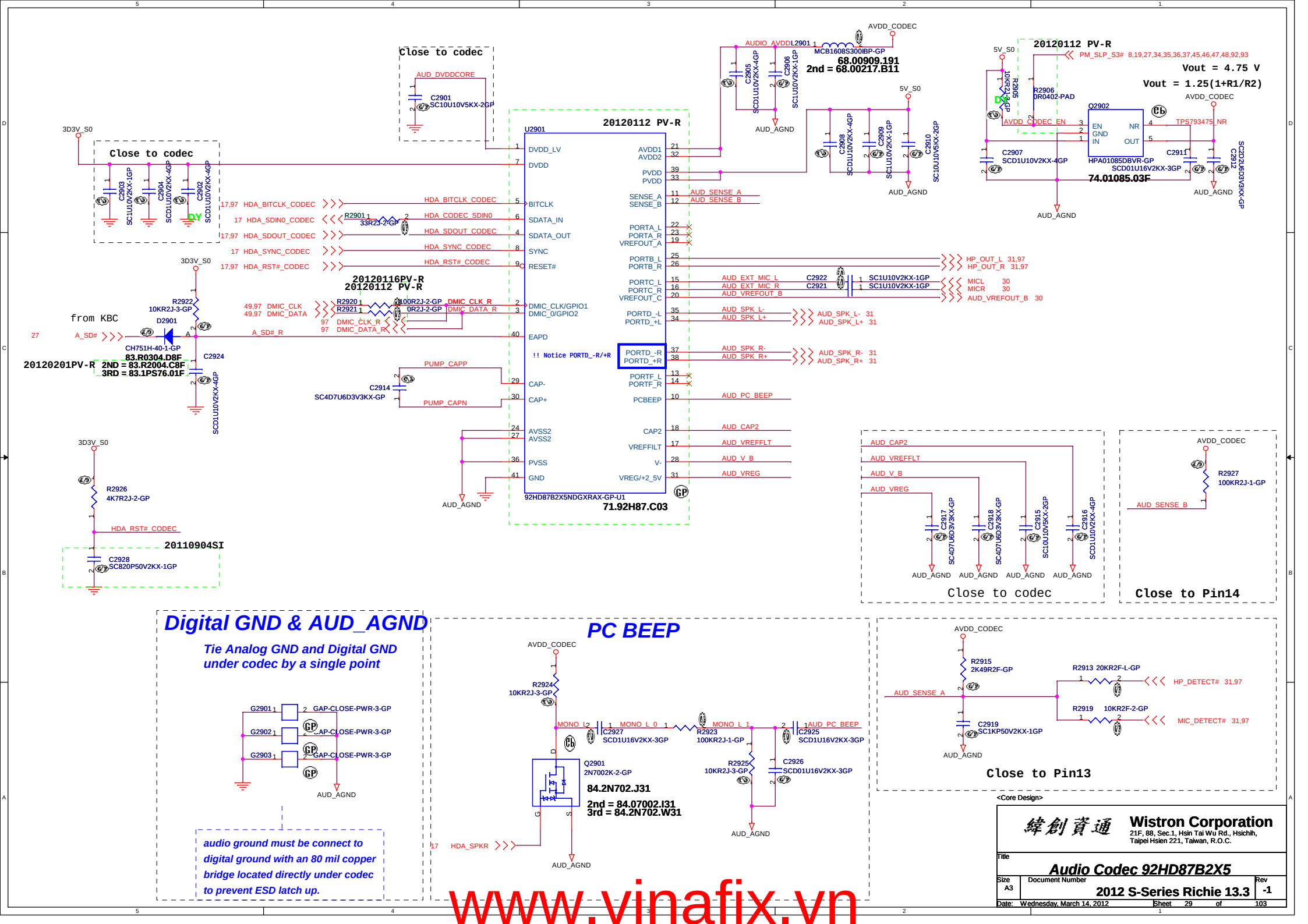
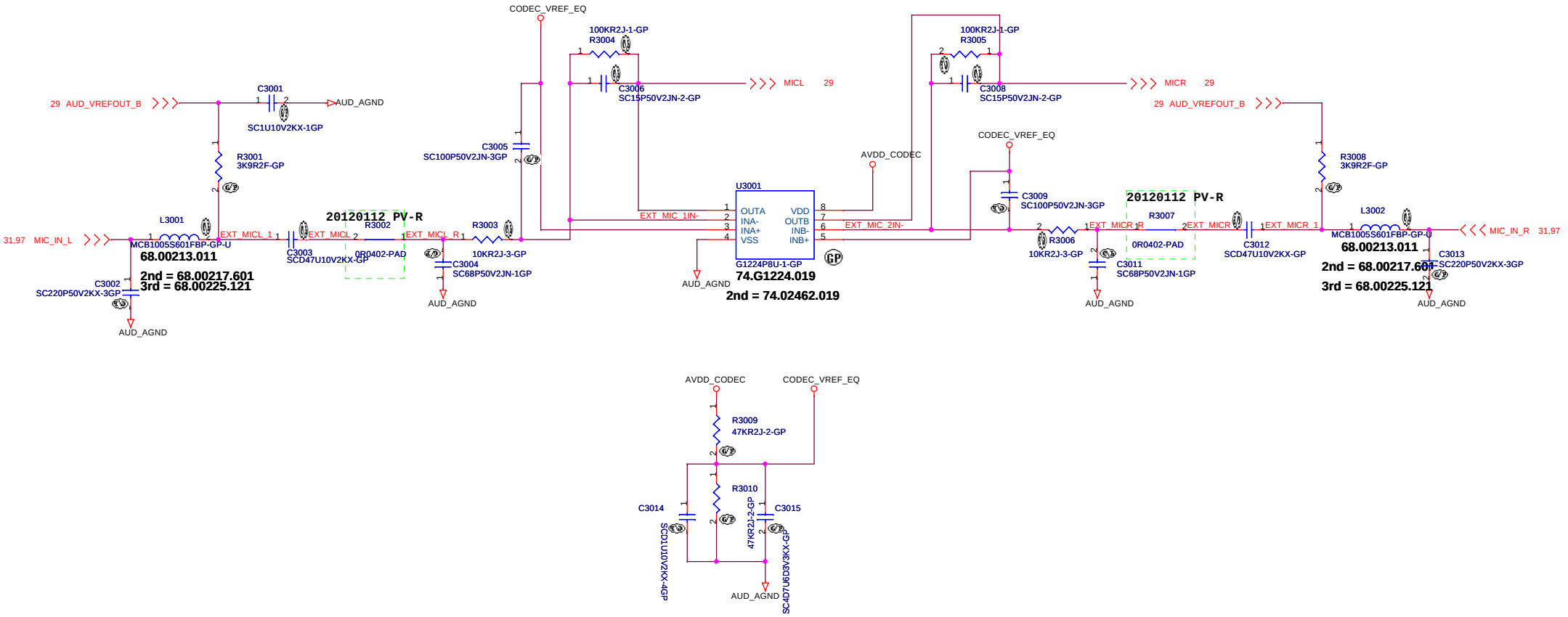


Pre-AMP. for External MIC



<Core Design>

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Title: ***External MIC Pre-Amp***

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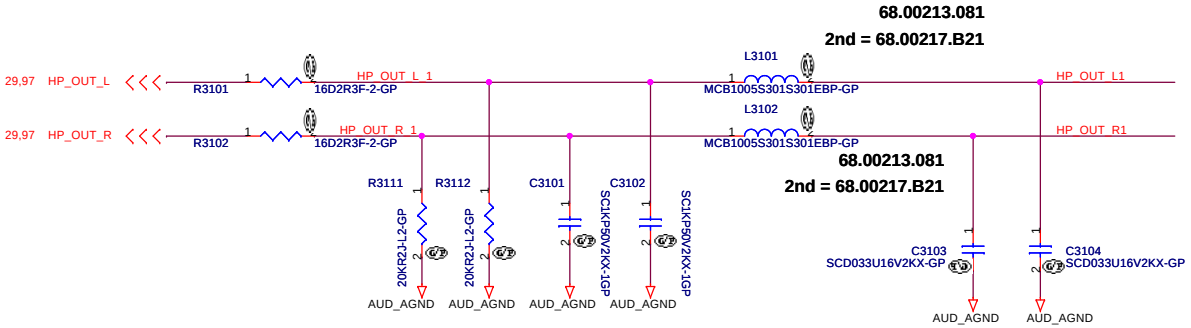
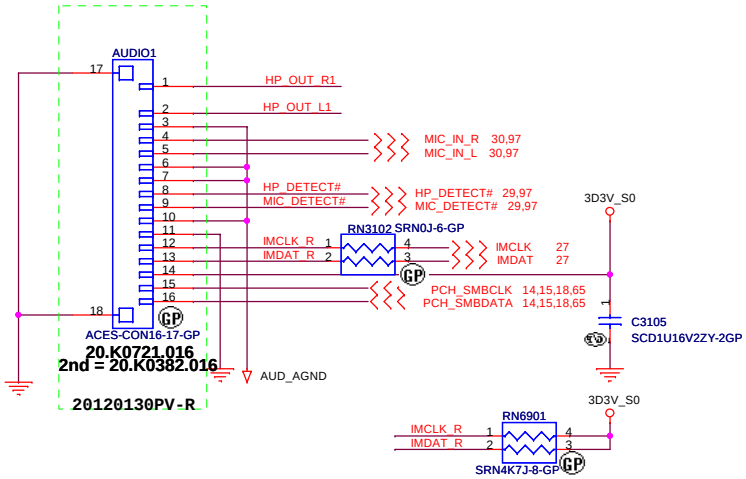
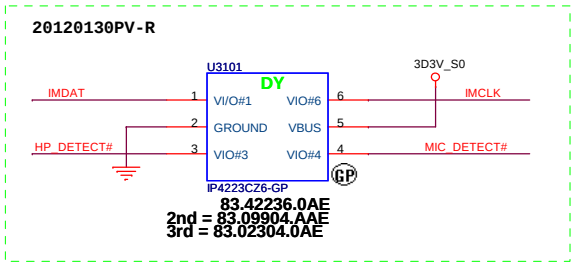
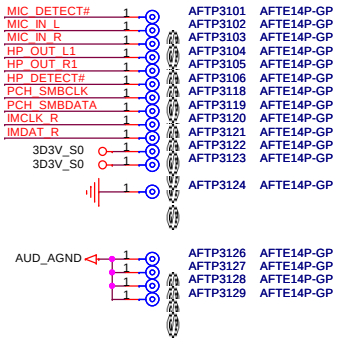
HeadPhone OUT



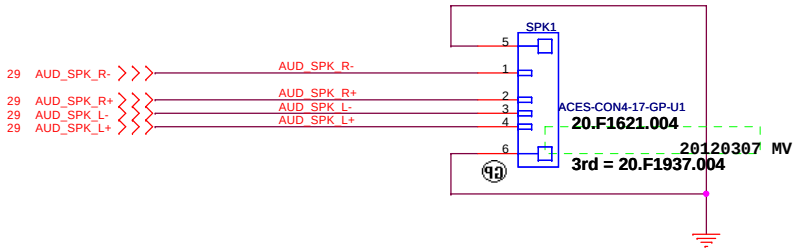
Audio Board +Touch Pad Connector

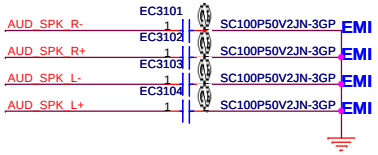


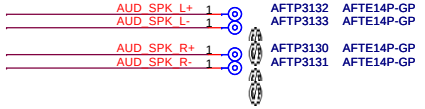




Speaker Connector







<Core Design>

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Title: AUDIO Connector

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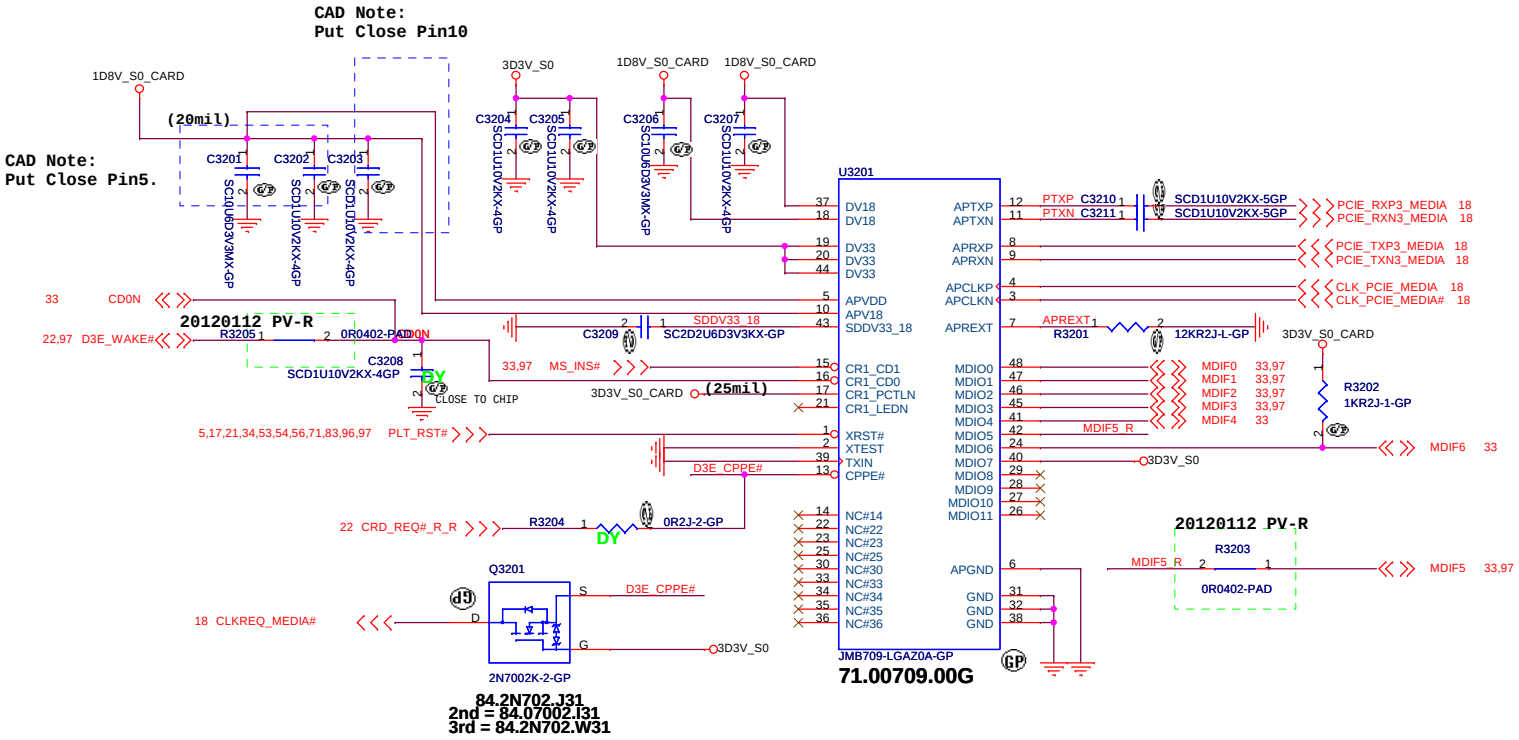
CardReader JMicron JMB709



84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

D3E Detection Table

D3E_CPPE#	Status
H	D3E mode
L	Normal mode

CR1_CDxN Detection Table

CR1_CDxN		Card Type
1	0	
H	H	(No Card)
H	L	SD Card/MMC
L	H	MemoryStick
L	L	XD Card

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Title: Card Reader-JMB 709

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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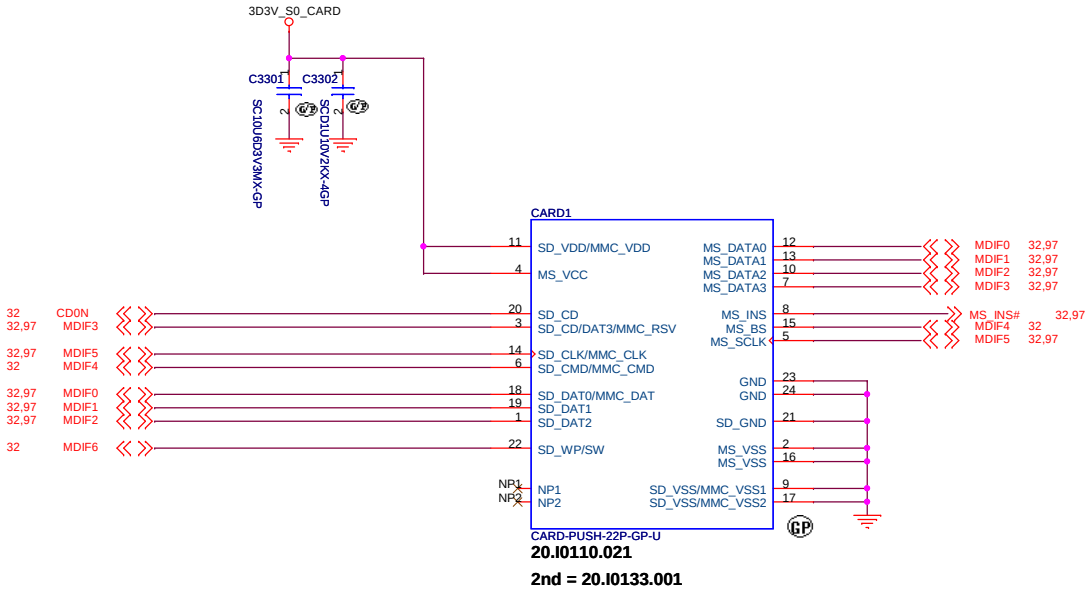

Pin Name	Default Mode	SD/MMC Card	MS Card
MDIO0	SD/MMC/MS	SD1_DAT0	MS1_DAT0
MDIO1		SD1_DAT1	MS1_DAT1
MDIO2		SD1_DAT2	MS1_DAT2
MDIO3		SD1_DAT3	MS1_DAT3
MDIO4		SD1_CMD	MS1_BS
MDIO5		SD1_CLK	MS1_CLK
MDIO6		SD1_WP	
MDIO7			
MDIO8		MMC_DAT4	MS1_DAT4
MDIO9		MMC_DAT5	MS1_DAT5
MDIO10		MMC_DAT6	MS1_DAT6
MDIO11		MMC_DAT7	MS1_DAT7
CR1_LEDN		SD1_LED#	MS1_LED#
CR1_PCTLN		SD1_PCTL#	MS1_PCTL#
CR1_CD0		SD1_CD#	
CR1_CD1			MS1_CD#

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SD/MS/MMC CONNECTOR***

Size	Document Number	Rev
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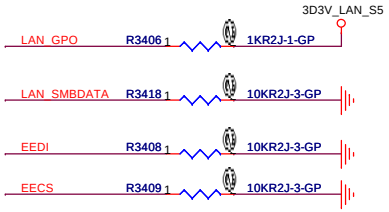
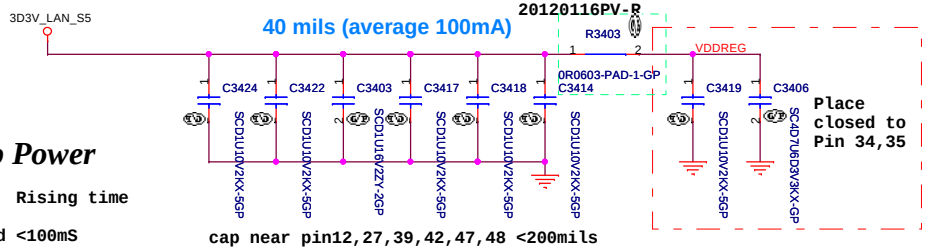
LAN CHIP-RTL8151FH

USE EFuse No ASF

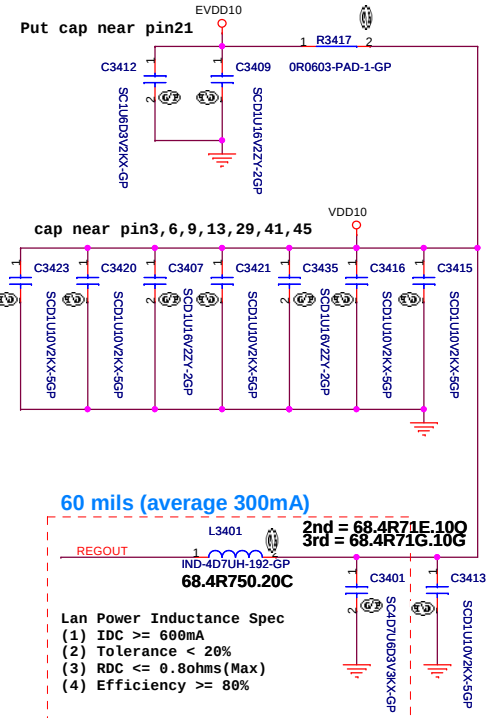


LanChip Power

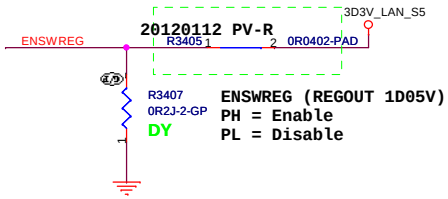
+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS



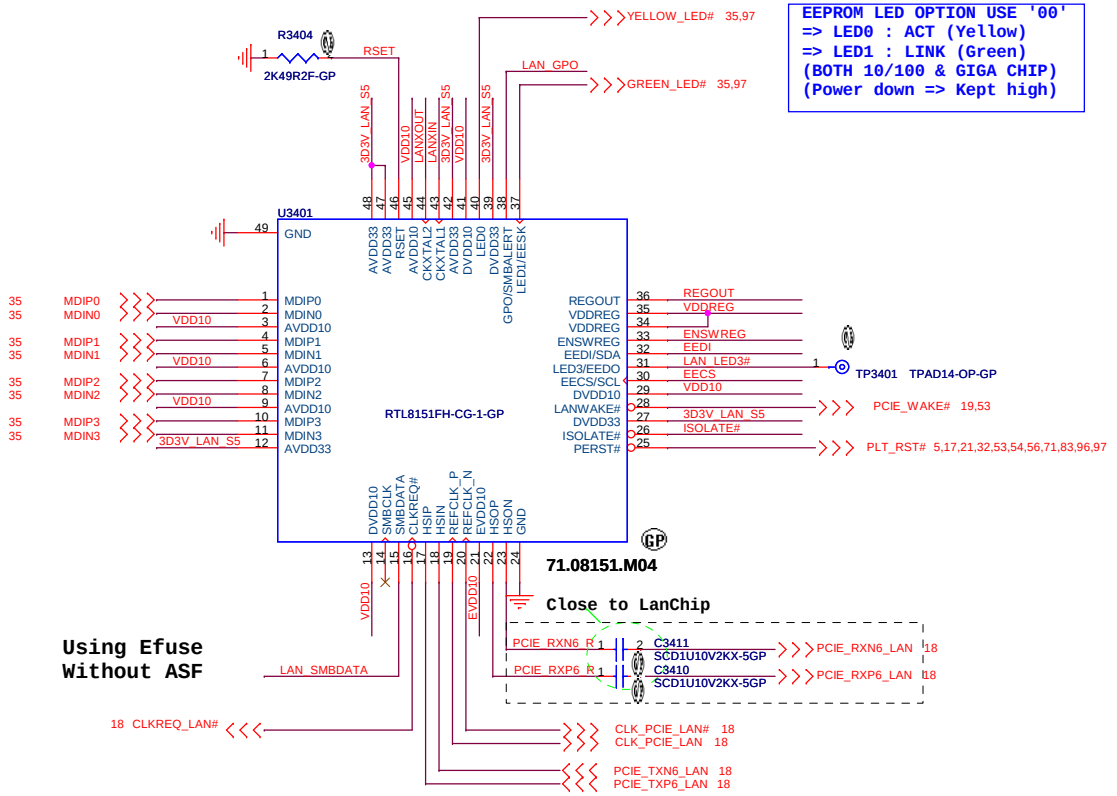
Regout power plane(1D05V)

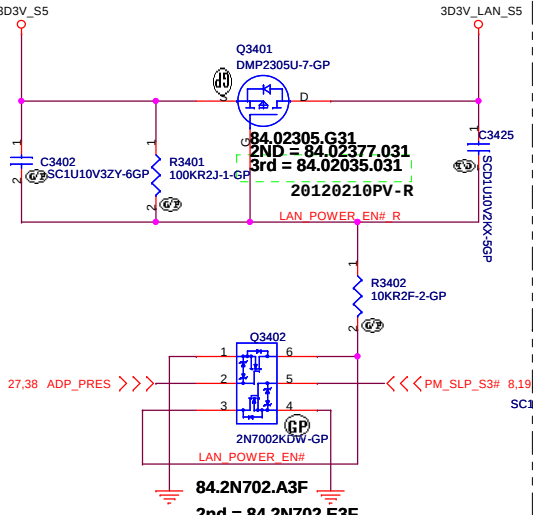


Regout Switch



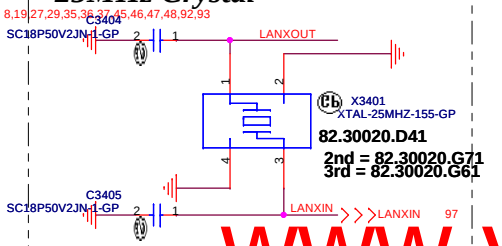
EEPROM LED OPTION USE '00'
=> LED0 : ACT (Yellow)
=> LED1 : LINK (Green)
(BOTH 10/100 & GIGA CHIP)
(Power down => Kept high)



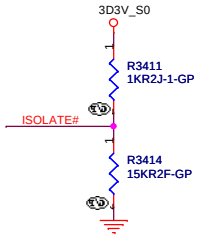


Using Efuse Without ASF

25MHz Crystal



Isolate Strap Pin



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Title: Lan Realtek 8151FH

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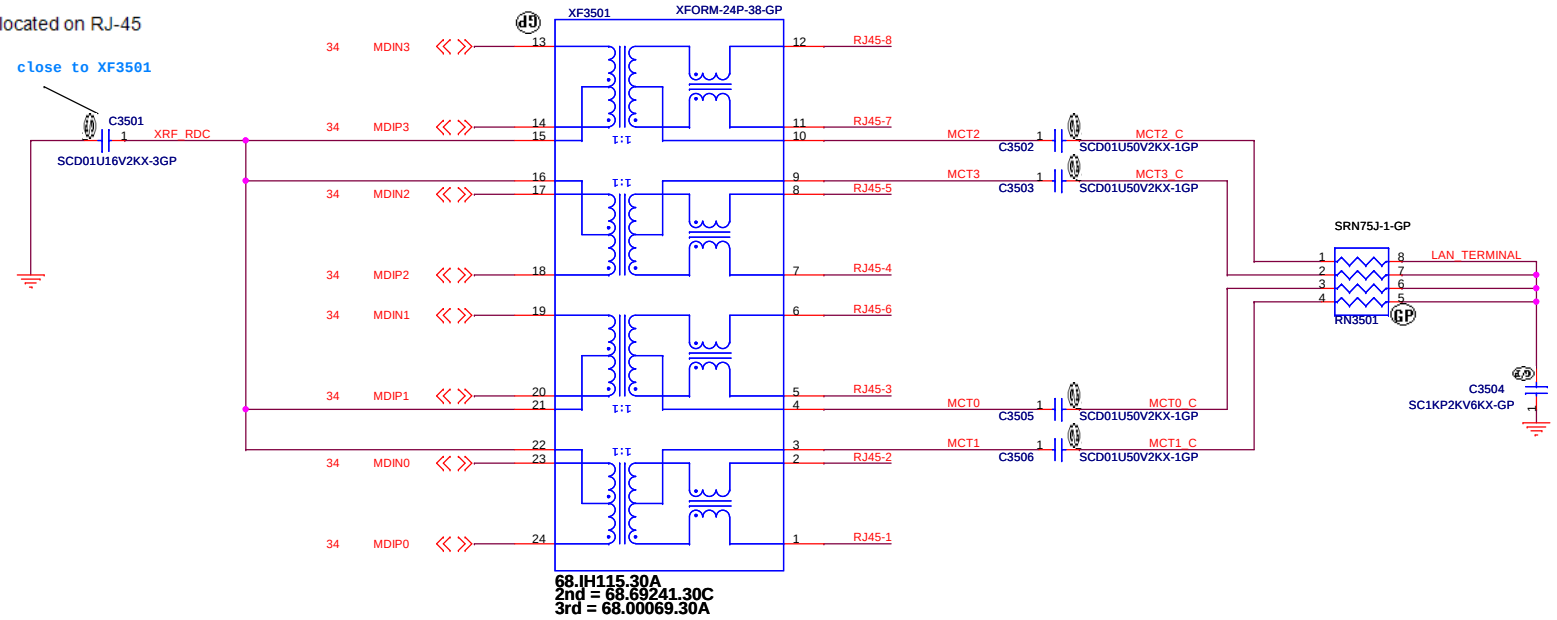
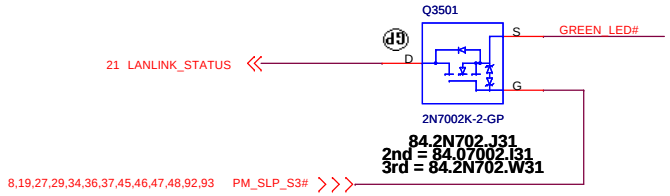
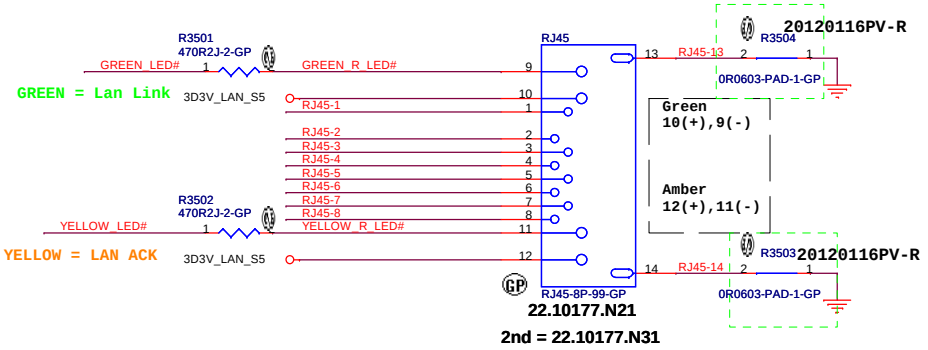
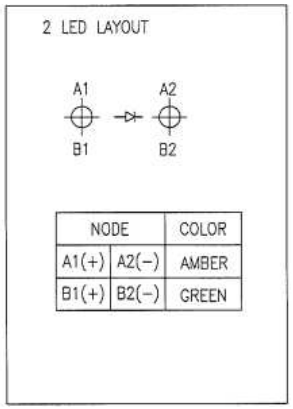
White LED for connectivity and Amber LED for activity located on RJ-45 connector

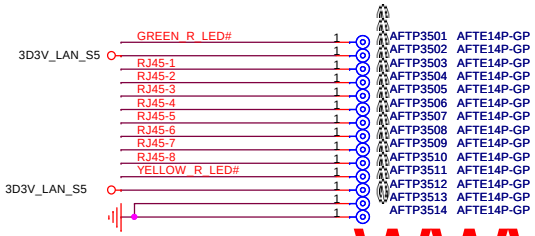


RJ45 Connector









(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.

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Title: LAN RJ45

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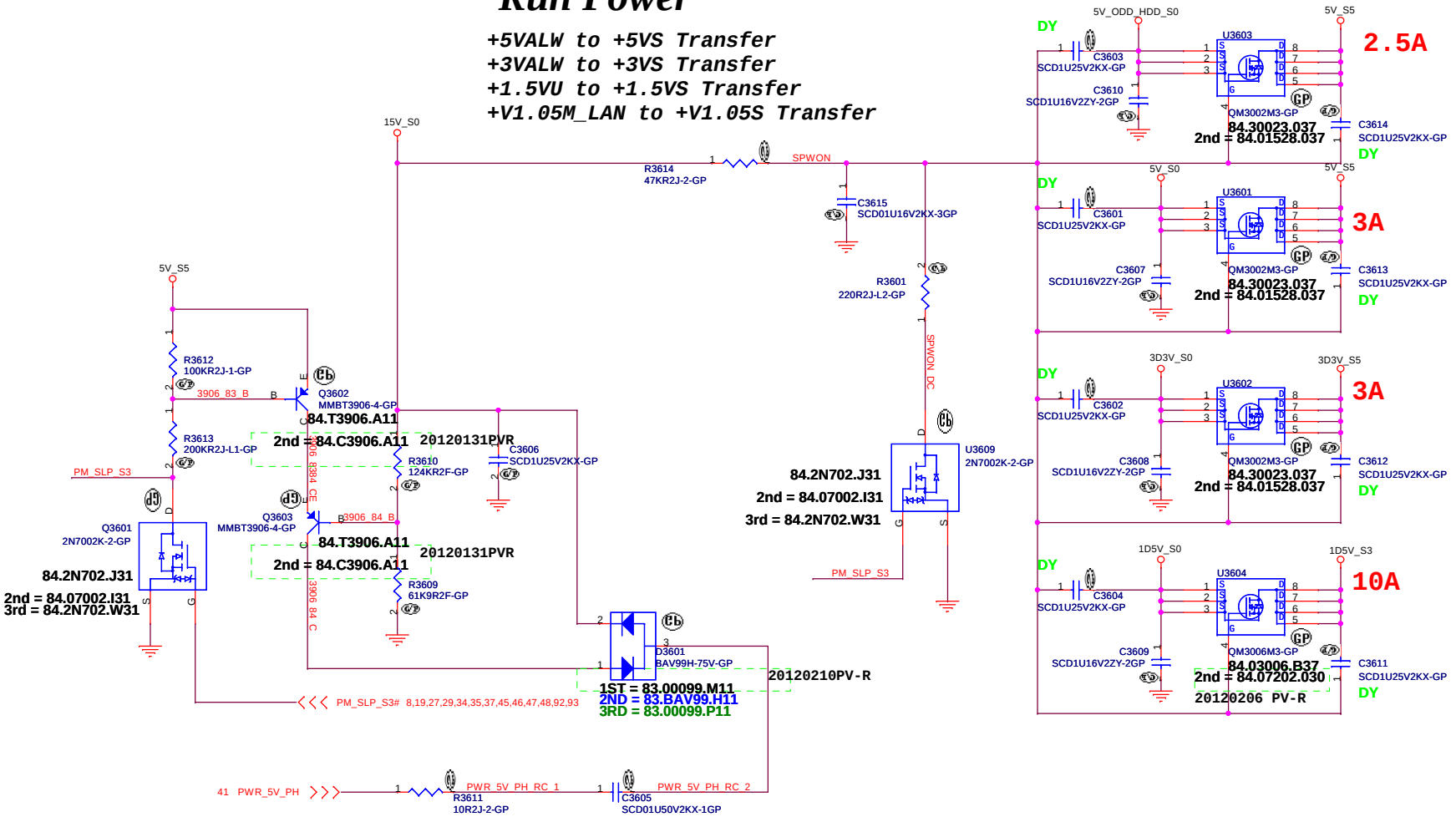
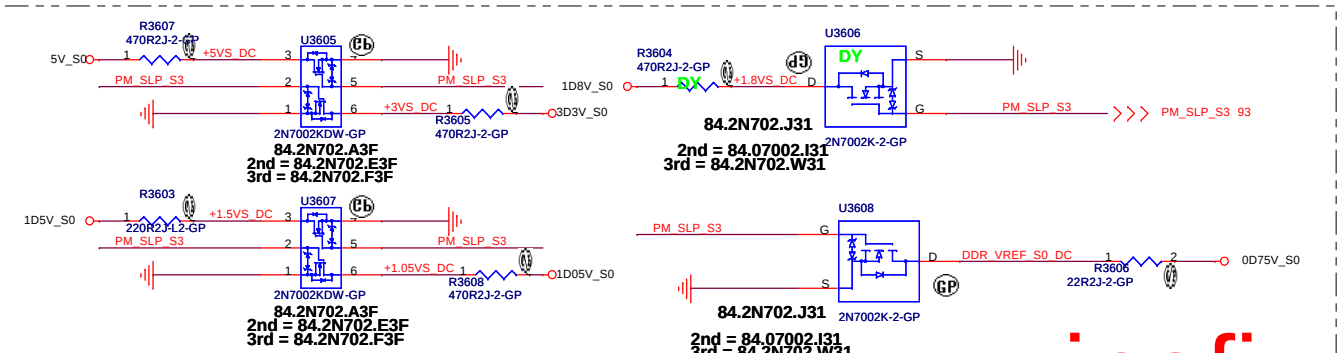
Run Power

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+1.5VU to +1.5VS Transfer
+V1.05M_LAN to +V1.05S Transfer





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Title: Power Plane Enable

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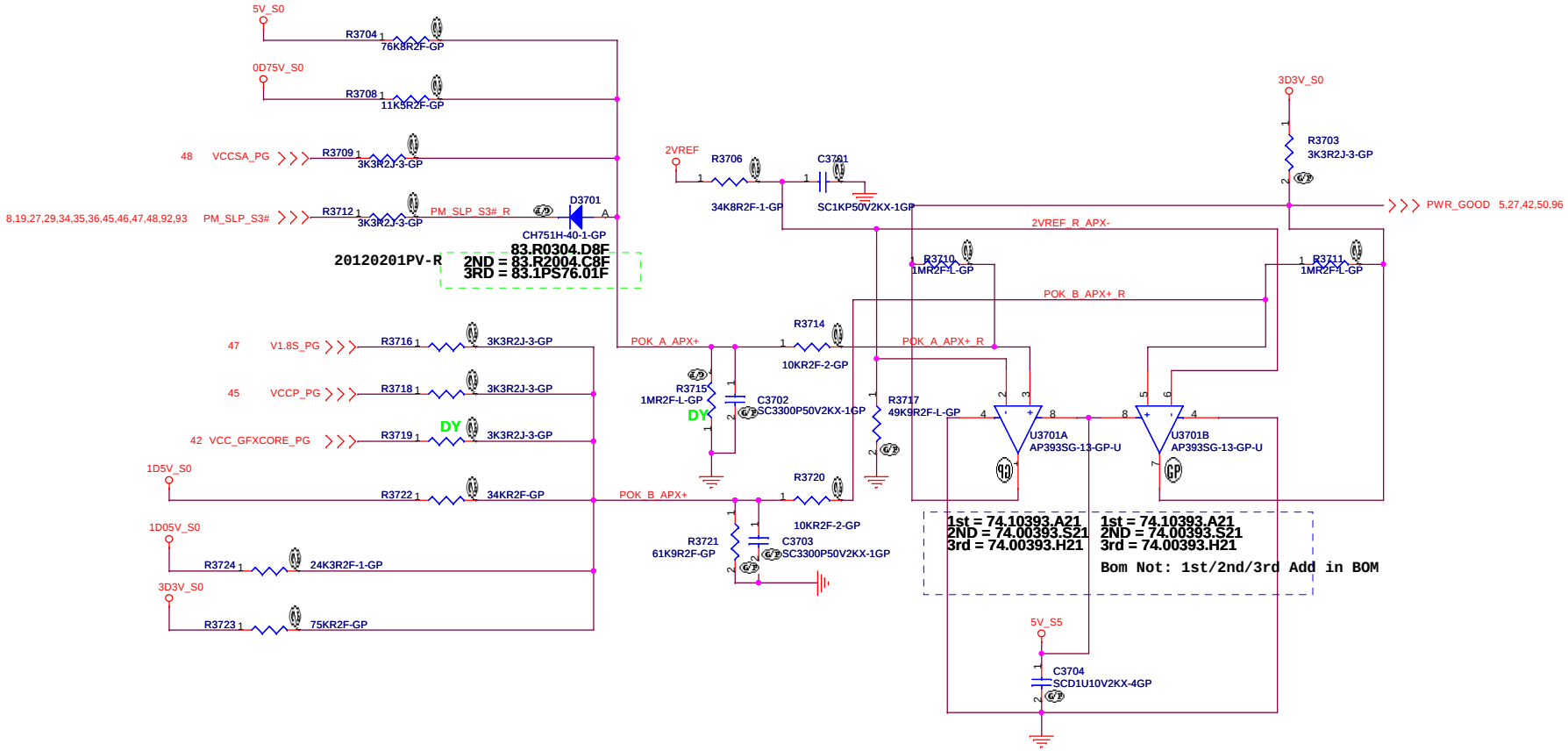
POK



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Title			
POK			
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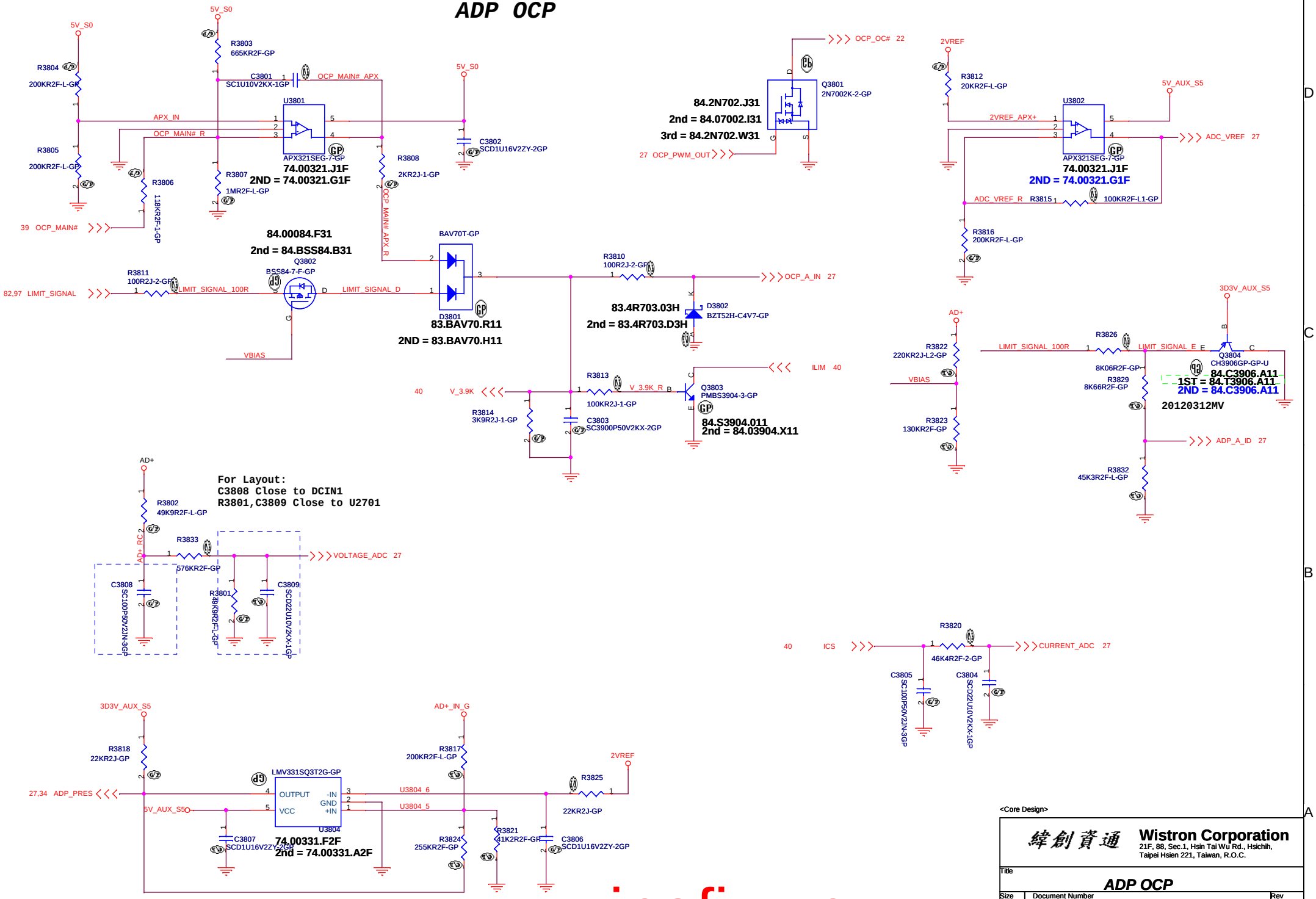
ADP OCP



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Title: ADP OCP

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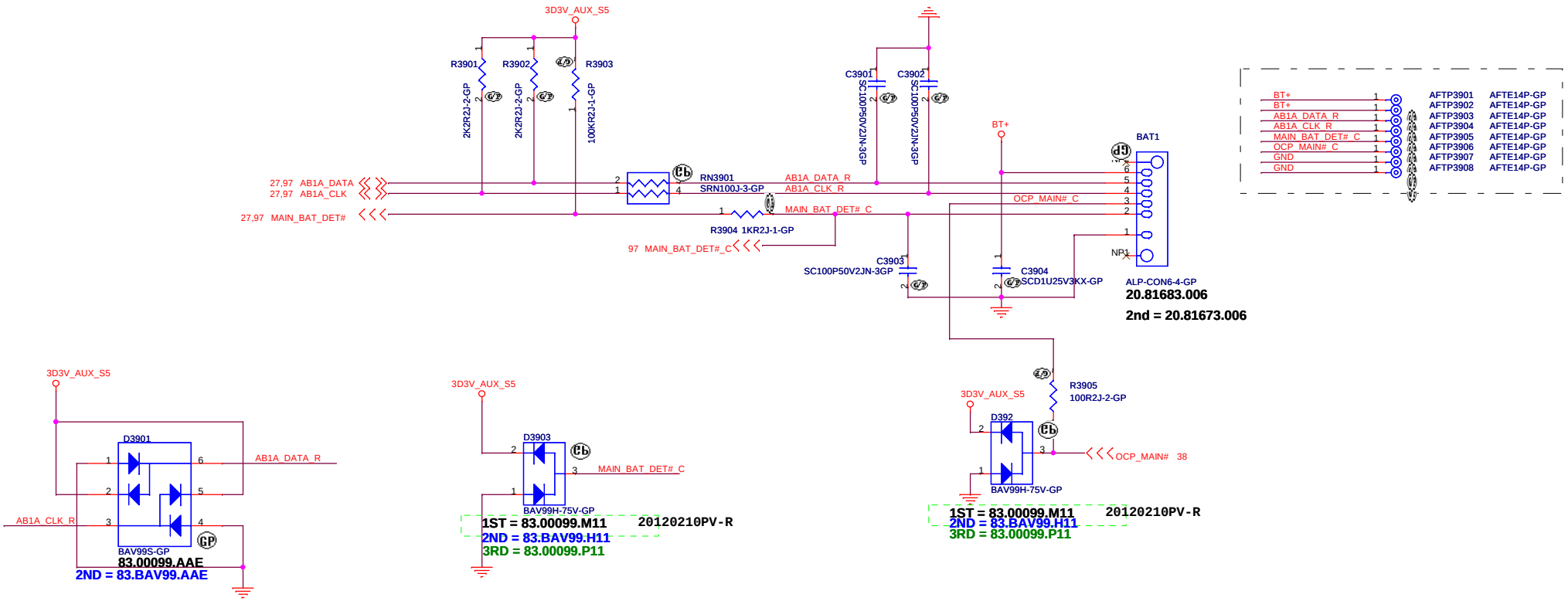
Battery Connector



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Title: BATT CONN

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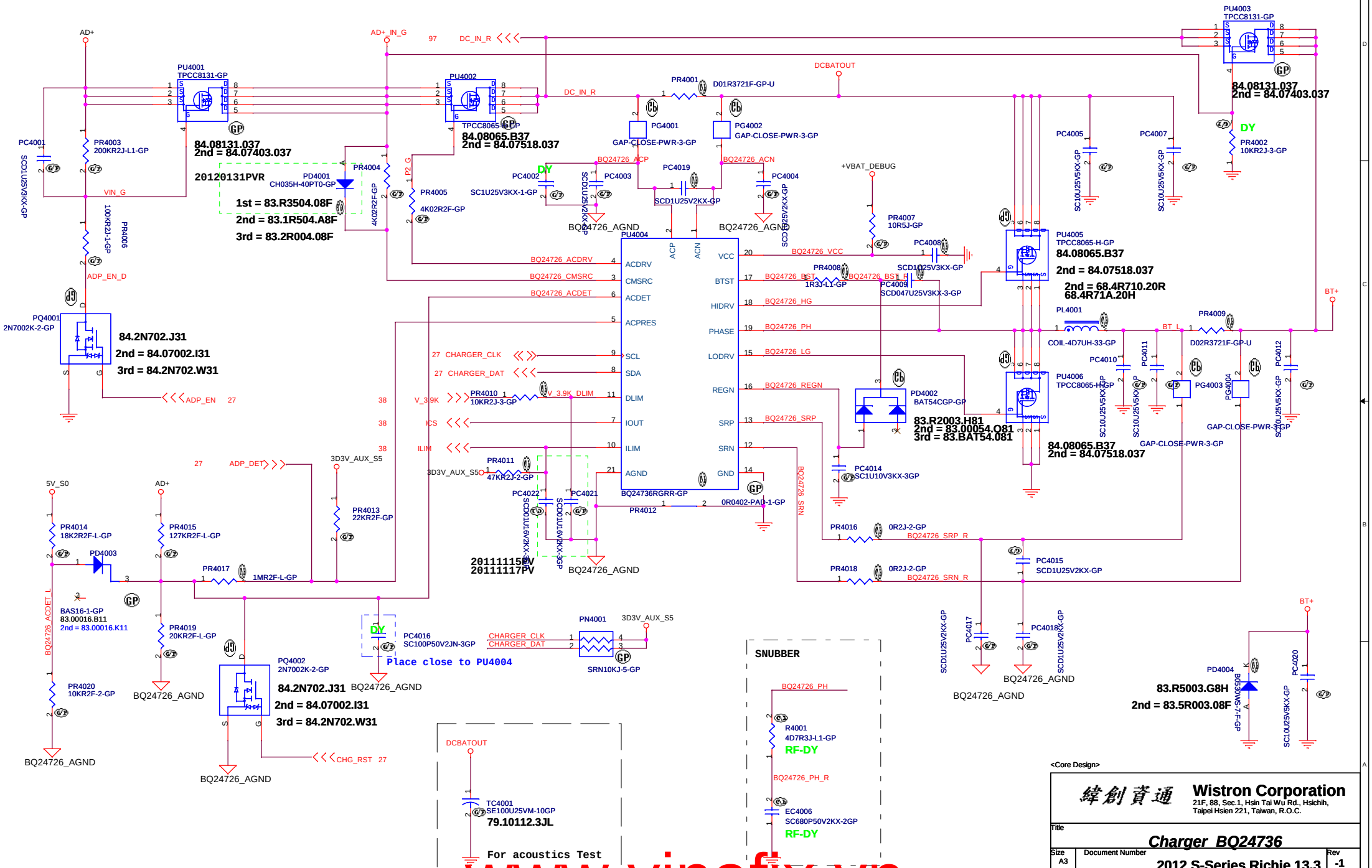
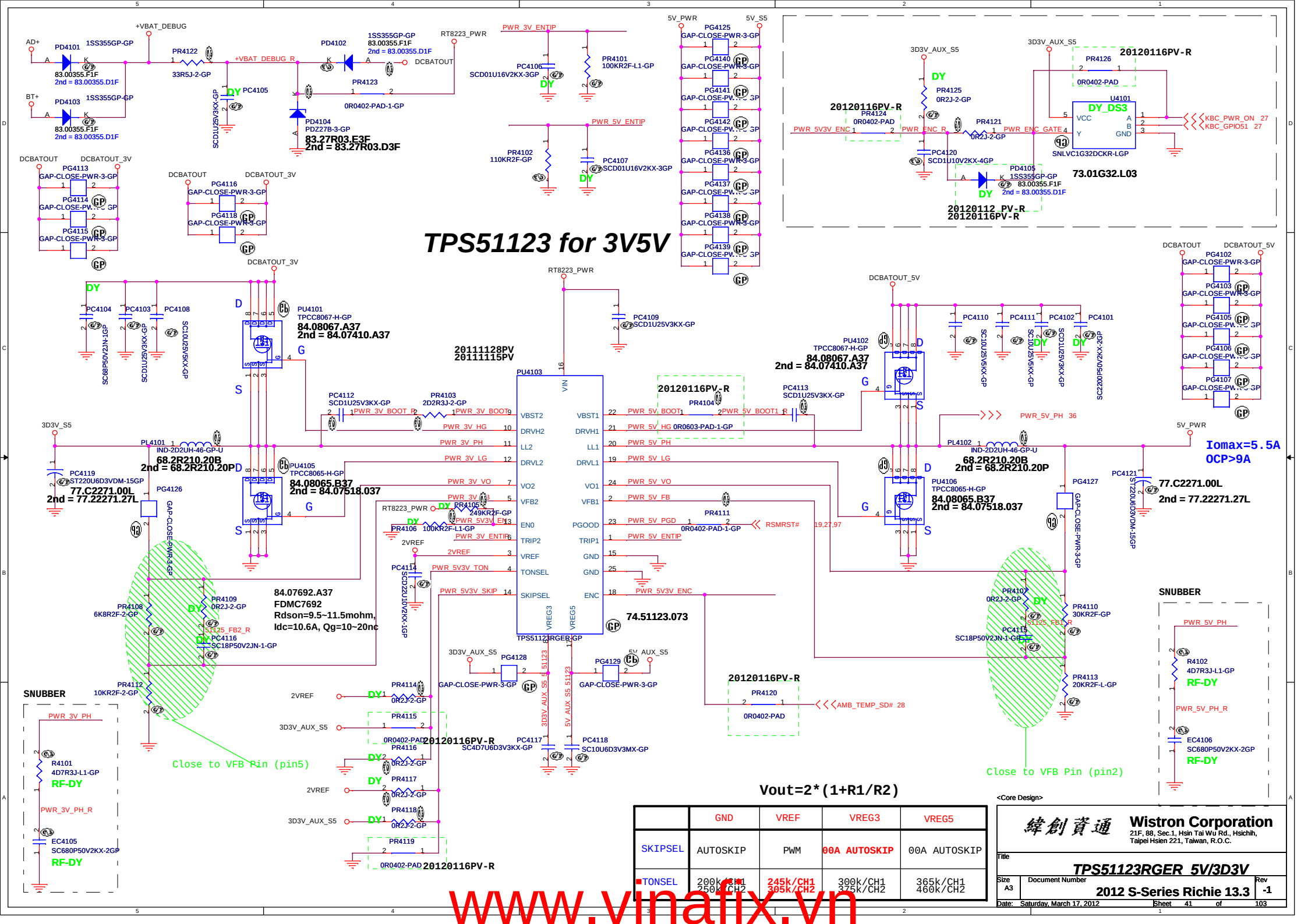
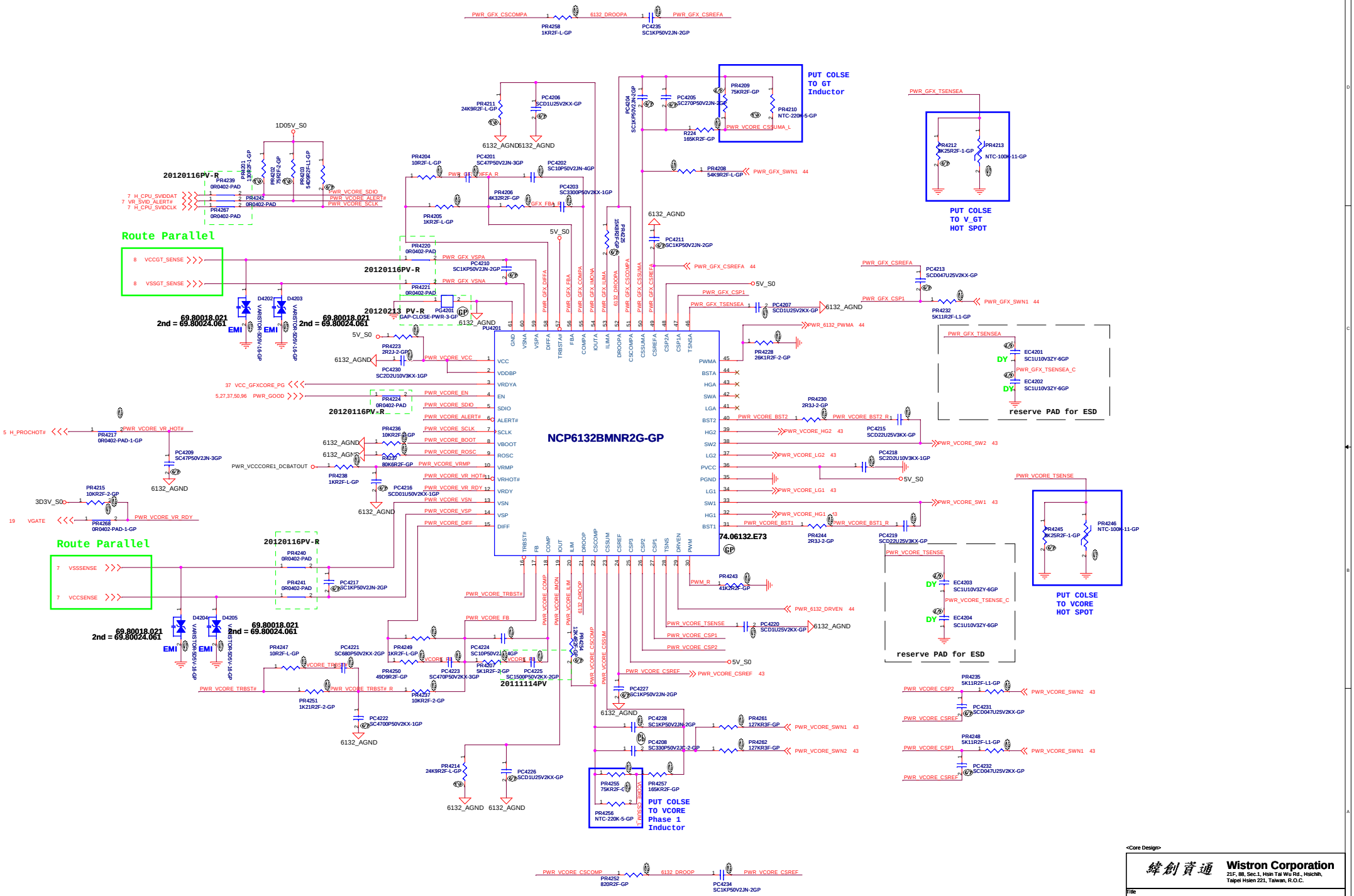
BQ24736 for CHARGER




TPS51123 for 3V5V
Vout=2*(1+R1/R2)
Iomax=5.5A
OCP>9A
74.51123.073
84.07692.A37
FDMC7692
Rdson=9.5~11.5mohm,
Idc=10.6A, Qg=10~20nc
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
SNUBBER
SNUBBER
TPS51123RGER-GP
PU4103
PU4101 TPCC8067-H-GP 84.08067.A37 2nd = 84.07410.A37
PU4102 TPCC8067-H-GP 84.08067.A37 2nd = 84.07410.A37
PU4105 TPCC8065-H-GP 84.08065.B37 2nd = 84.07518.037
PU4106 TPCC8065-H-GP 84.08065.B37 2nd = 84.07518.037
PL4101 IND-2D2UH-46-GP-U 68.2R210.20B 2nd = 68.2R210.20P
PL4102 IND-2D2UH-46-GP-U 68.2R210.20B 2nd = 68.2R210.20P
PD4101 1SS355GP-GP 83.00355.F1F 2nd = 83.00355.D1F
PD4102 1SS355GP-GP 83.00355.F1F 2nd = 83.00355.D1F
PD4103 1SS355GP-GP 83.00355.F1F 2nd = 83.00355.D1F
PD4104 PDZ27B-3-GP 83.27R03.E3F 2nd = 83.27R03.D3F
PD4105 1SS355GP-GP 83.00355.F1F 2nd = 83.00355.D1F
20120116PV-R
20120112 PV-R
20120116PV-R
73.01G32.L03
20111128PV
20111115PV
84.07692.A37
FDMC7692
Rdson=9.5~11.5mohm,
Idc=10.6A, Qg=10~20nc
Vout=2*(1+R1/R2)
GND
VREF
VREG3
VREG5
AUTOSKIP
PWM
00A AUTOSKIP
200k/CH1 250k/CH2
245k/CH1 305k/CH2
300k/CH1 375k/CH2
365k/CH1 460k/CH2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51123RGER 5V/3D3V
2012 S-Series Richie 13.3
Saturday, March 17, 2012
www.vinafix.vn

SSID = CPU.Regulator



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Title: ISL95832 IMVP7-1/3

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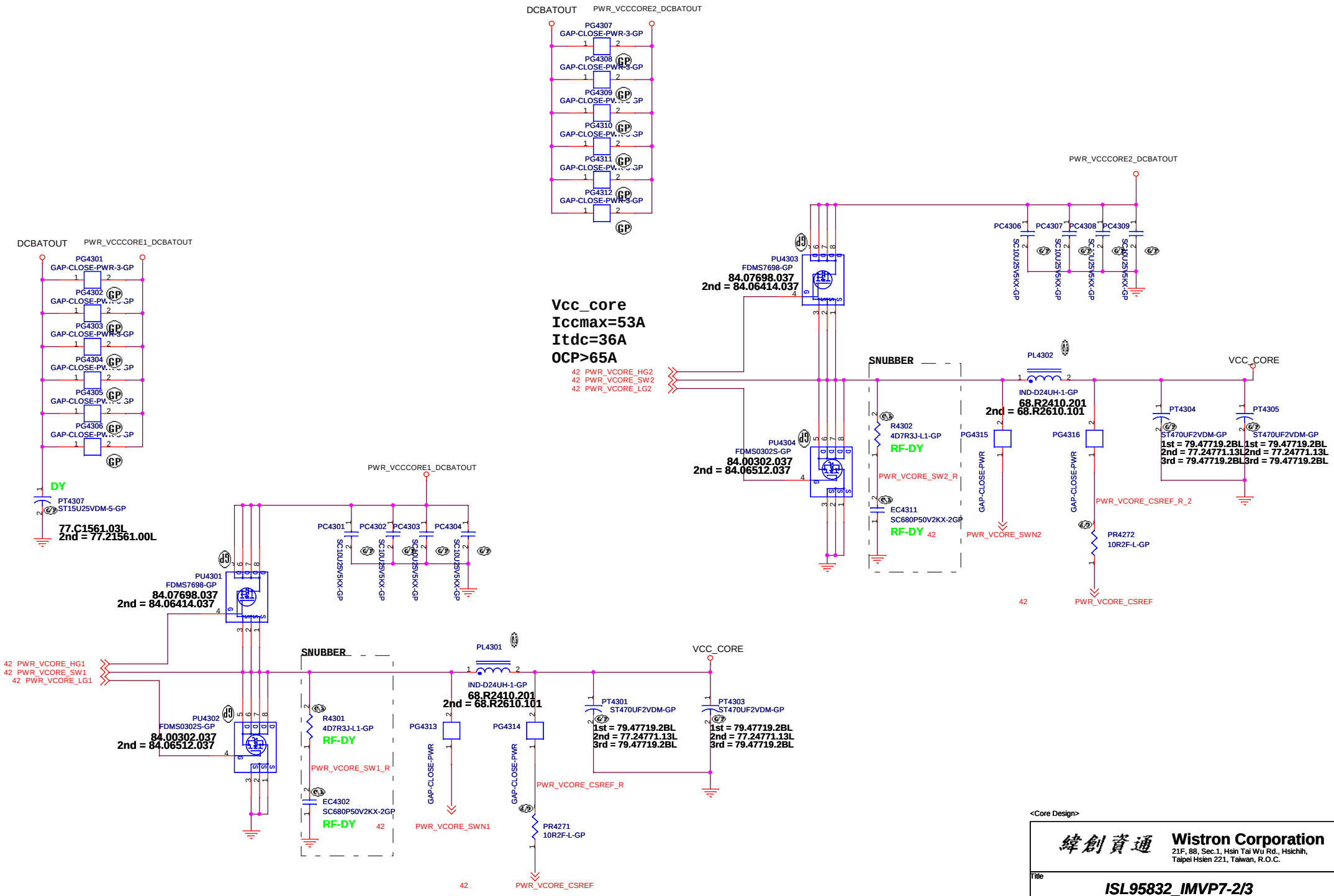

<Core Design>

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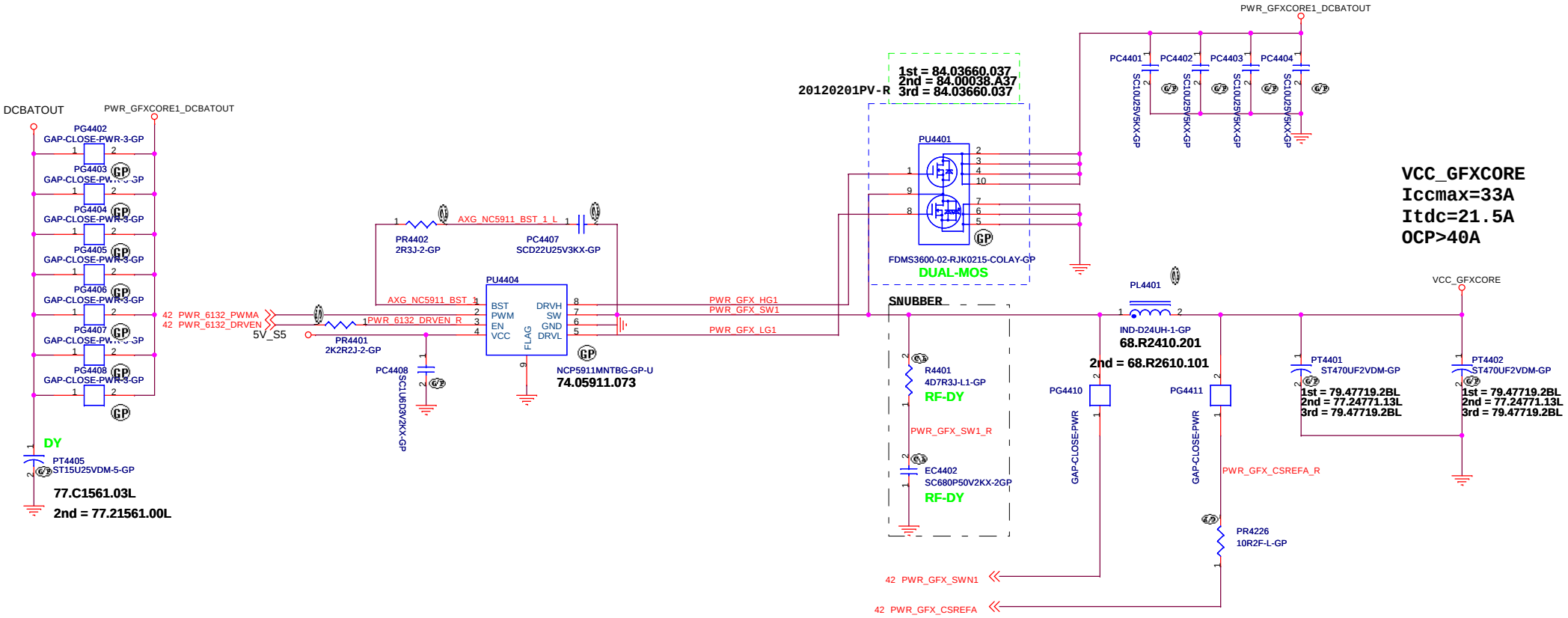
Title: ISL95832_IMVP7-2/3		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
Date: Wednesday, March 14, 2012	Sheet 43 of 103	



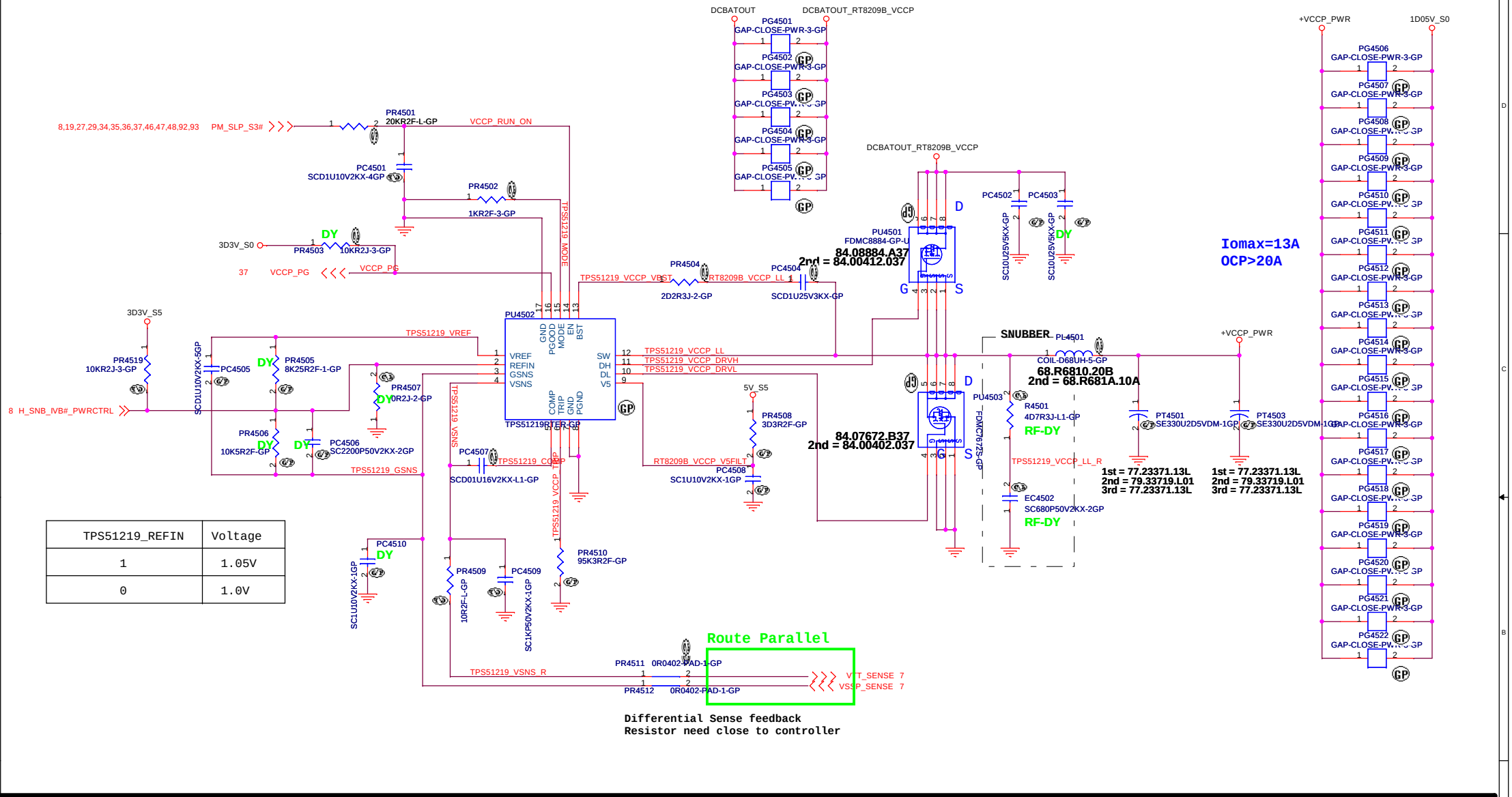
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95832_IMVP7-3/3

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Monday, March 19, 2012 Sheet 44 of 103



TPS51219_REFIN	Voltage
1	1.05V
0	1.0V

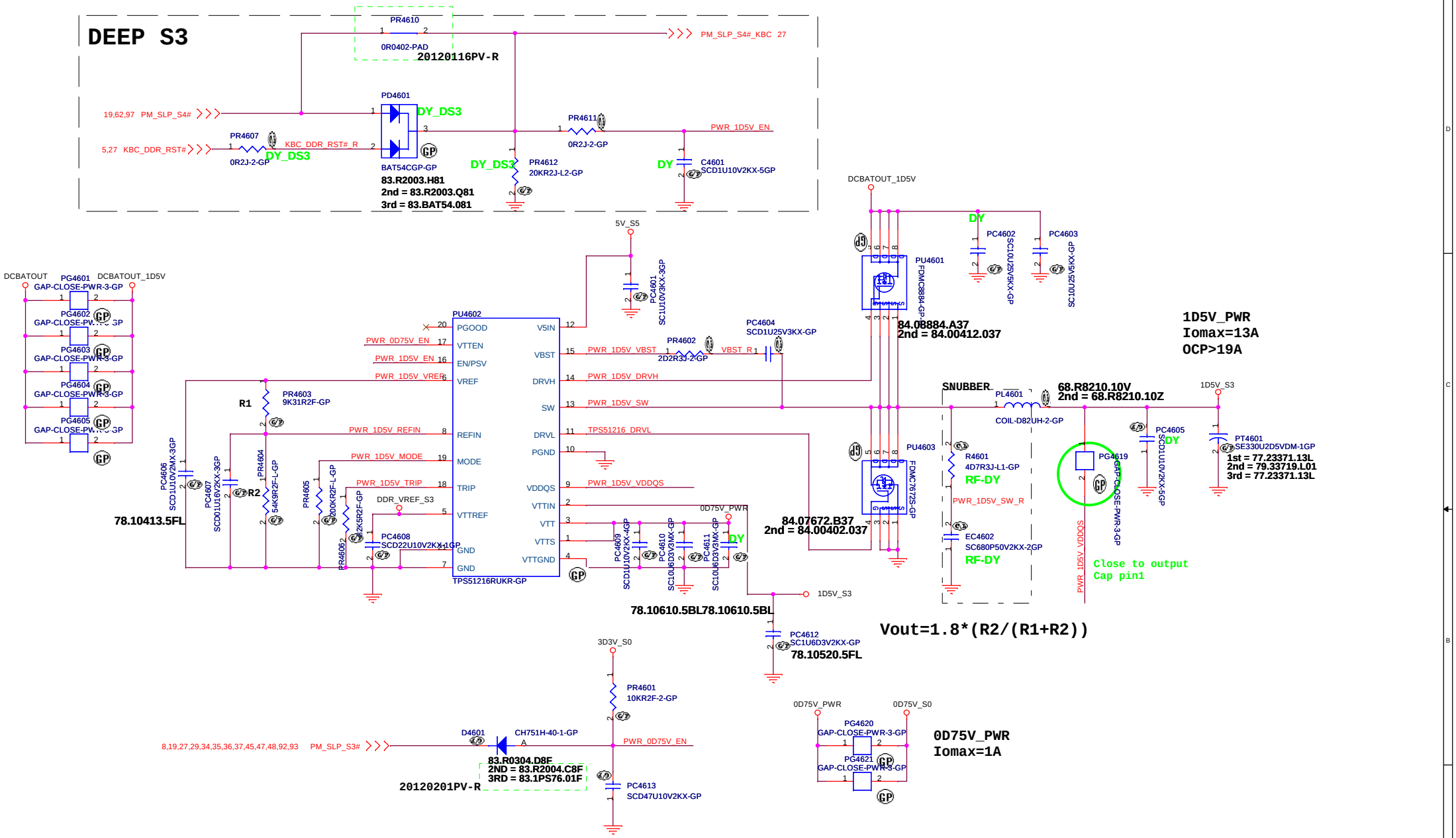
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_1D05V / 1D0V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 45 of 103



<Core Design>

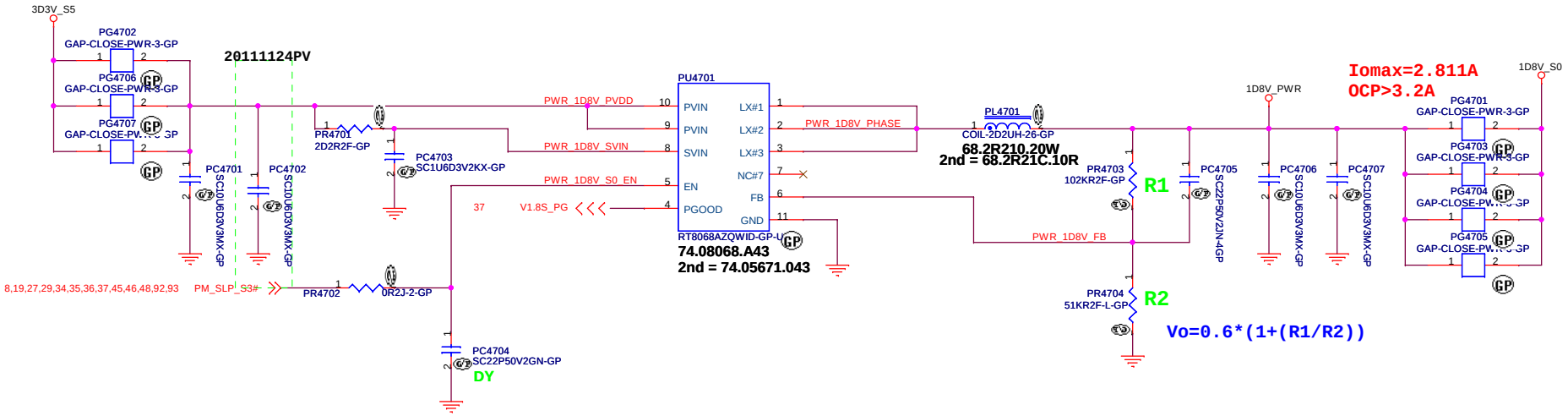
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UP1561_1D5V&0D75V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 46 of 103

RT8068A for 1D8V_S0



<Core Design>

緯創資通 Wistron Corporation
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Title: 1D8V_S0

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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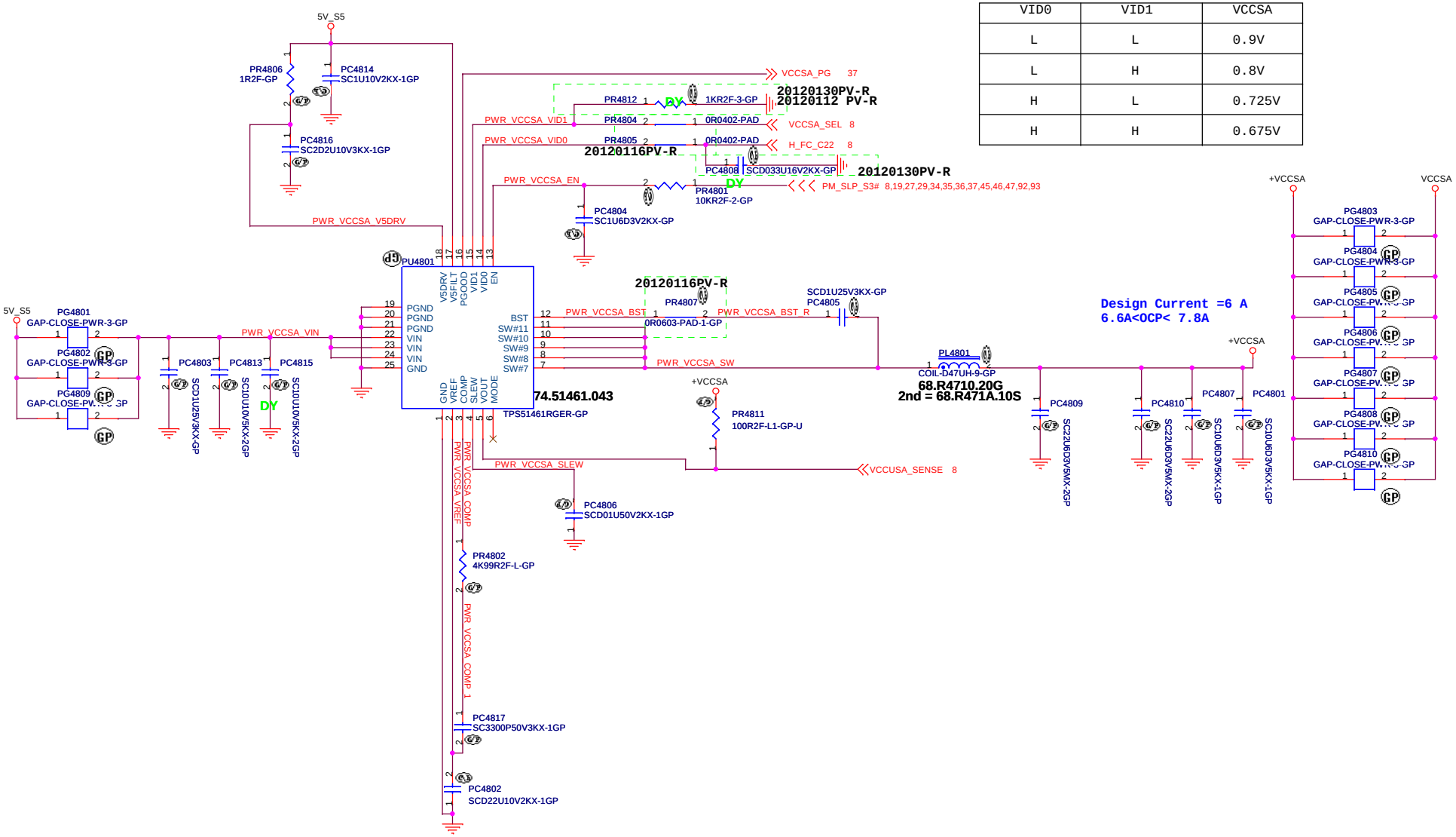
TPS51461 for VCCSA

VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V



<Core Design>

緯創資通 **Wistron Corporation**
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Title: ISL95870A VCCSA

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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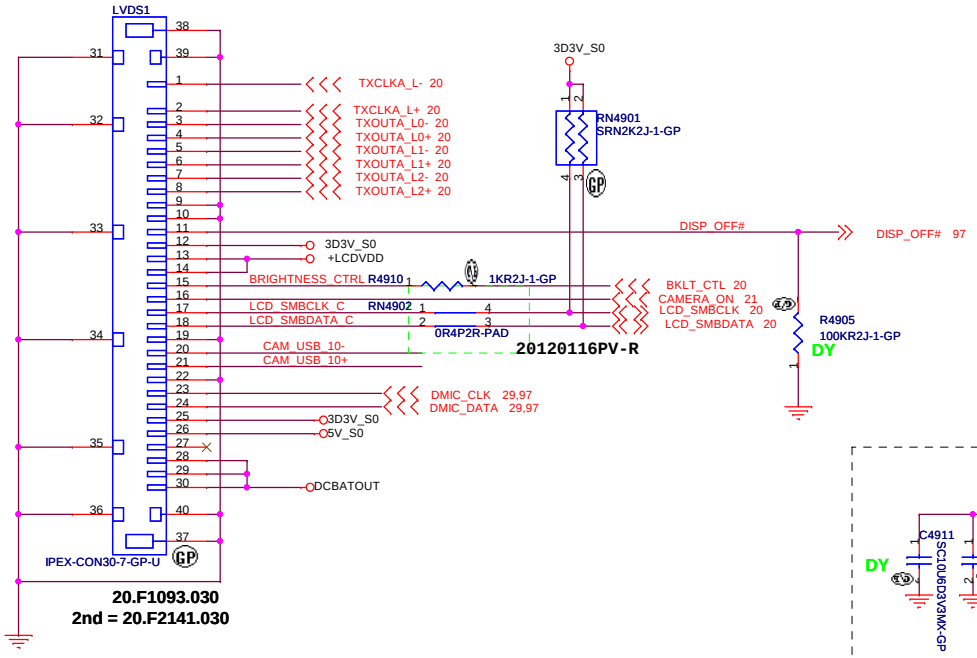
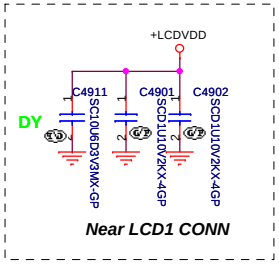
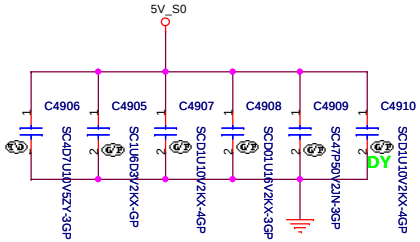
LCD Connector

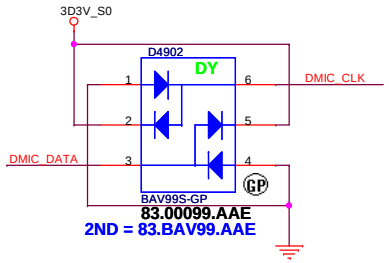
CARMER PINDEFINE

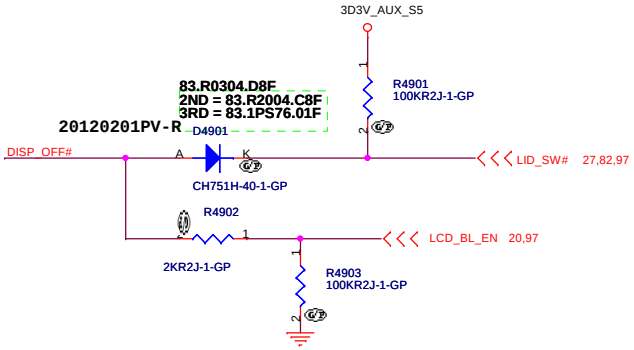
No.	Signal
1	DMIC_CLK
2	DMIC_DATA
3	GND
4	3.3V_MIC
5	5V_KBL
6	EN
7	VCC_5V
8	GND
9	D+
10	D-



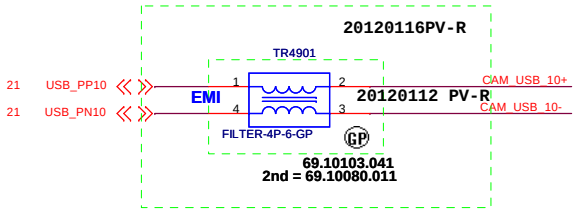




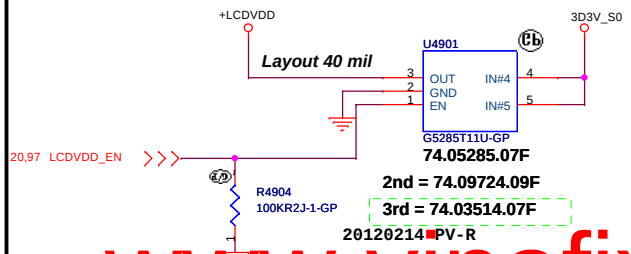




CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER

<Core Design>

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Title: LCD Connector

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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CRT Connector

CRT1
Transmission line characteristic impedance for RGB signals Zo = 37.5 Ohm

Transmission line characteristic impedance Zo= 50 Ohm

CRT RGB

68.00084.B61
2nd = 68.00245.051
3rd = 68.00226.141

L5001 BLM18BB470SN1D-GP
L5002 BLM18BB470SN1D-GP
L5003 BLM18BB470SN1D-GP

MUX_R MUX_G MUX_B
MUX_L_R MUX_L_G MUX_L_B
R5011 R5012 R5013 0R2J-2-GP
CRT_R CRT_G CRT_B

R1
R5001 R5002 R5003 75R2F-2-GP
C5001 C5002 C5003 SC22P50V2JN-4GP
C5004 C5005 C5006 SC22P50V2JN-4GP
C5007 C5008 C5009 SC22P50V2JN-4GP

DY DY DY 20120112 PV-R 20120116PV-R

Place these resistors as the closest components to connector CRT1

Transmission line characteristic impedance Zo = 50 Ohm

5V_S0
F5001 FUSE-1D1A6V-4GP-U
1.1A/8V
+5VS_CRT_F2

Q5002 DMP2305U-7-GP
84.02305.G31
2nd = 84.02377.031
3rd = 84.02035.031
20120210PV-R

69.50007.691
2nd = 69.50007.771
3rd = 69.60040.011

CRTVDD_EN# 1
R5020 10KR2J-3-GP
R5019 10KR2J-3-GP
CRTVDD_EN#

5V_S0_CRT
C5020 SC4D7U10V5ZY-3GP DY
C5022 SCD1U16V2ZY-2GP

RN5001 SRN2K2J-1-GP

Q5001 2N7002K-2-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

5,27,37,42,96 PWR_GOOD

C5019 SCD1U16V2ZY-2GP DY

CRT1
NC#4 NC#11
VCC_CRT
DDCDATA_ID1 DDCCLK_ID3
CRT_RED CRT_GREEN CRT_BLUE
VSYNC HSYNC
GND GND GND GND GND GND GND GND
DDC_DATA_CON
DDC_CLK_CON
CRT_R CRT_G CRT_B
CRT_VSYNC_CON_1
CRT_HSYNC_CON_1
D-SUB-15-123-GP
20.20938.015
2nd = 20.20984.015

C5023 C5021 DY DY SC22P50V2JN-4GP
C5024 C5025 DY DY SC33P50V2JN-3GP

DDC&HSYNC&VSYNC

3D3V_S0
RN5007 SRN10KJ-5-GP
M_HSYNC
M_VSYNC

20120116PV-R
20120112 PV-R
20 PCH_RED R5006 0R0402-PAD MUX_R
20 PCH_GREEN R5007 0R0402-PAD MUX_G
20 PCH_BLUE R5008 0R0402-PAD MUX_B

5V_S0_CRT
C5016 SCD1U16V2ZY-2GP

73.1G125.D0G
2nd = 73.07125.0AG
3rd = 73.1G125.0JH
U5001 U74AHCT1G125G-AL5-R-GP-U
U5002 U74AHCT1G125G-AL5-R-GP-U
OE# VCC A GND Y

20120116PV-R
RN5002 0R4P2R-PAD
20 CRT_HSYNC
20 CRT_VSYNC
M_HSYNC
M_VSYNC

5V @ ext. CRT side
RN5003 SRN33J-5-GP
HSYNC_5 VSYNC_5
CRT_HSYNC_CON_1
CRT_VSYNC_CON_1

C5018 C5017 DY DY SC10P50V2JN-4GP

DDC

5V_S0_CRT
D5004 BAV99S-GP DY
CRT_VSYNC_CON_1
CRT_HSYNC_CON_1
83.00099.AAE
2ND = 83.BAV99.AAE

AFTP5001 AFTE14P-GP
AFTP5002 AFTE14P-GP
AFTP5003 AFTE14P-GP
AFTP5004 AFTE14P-GP
AFTP5005 AFTE14P-GP
AFTP5006 AFTE14P-GP
AFTP5007 AFTE14P-GP
AFTP5009 AFTE14P-GP
AFTP5011 AFTE14P-GP
AFTP5008 AFTE14P-GP
AFTP5010 AFTE14P-GP
AFTP5012 AFTE14P-GP

5V_S0_CRT
D5005 BAV99S-GP DY
DDC_CLK_CON
DDC_DATA_CON
83.00099.AAE
2ND = 83.BAV99.AAE

3D3V_S0
D5006 BAV99S-GP DY
CRT_R
CRT_G
83.00099.AAE
2ND = 83.BAV99.AAE

3D3V_S0
RN5004 SRN2K2J-1-GP
20120116PV-R
2011102PV
20120116PV-R
RN5008 0R4P2R-PAD
20 CRT_DDC_DATA
20 CRT_DDC_CLK
CRT_DDC_DATA_R
CRT_DDC_CLK_R
Q5003 2N7002KDW-GP
DDC_DATA_CON
DDC_CLK_CON
84.2N702.A3F
2nd = 84.2N702.F3F
3rd = 84.2N702.P4F

3D3V_S0
D5003 BAV99-5-GP DY
CRT_B
83.00099.T11
2nd = 83.BAV99.D11
3rd = 83.BAV99.H11

3D3V_S0
C5010 SCD1U10V2KX-4GP DY

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Title: CRT Connector
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HDMI Connector

HDMI CONN

20120130PV-R

TR5101
HDMI_CLK_R_C
HDMI_CLK_R_C#
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5103
HDMI_DATA1_R_C
HDMI_DATA1_R_C#
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5102
HDMI_DATA0_R_C
HDMI_DATA0_R_C#
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5104
HDMI_DATA2_R_C
HDMI_DATA2_R_C#
HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

HDMI_PLL_GND
DY
R5123
0R2J-2-GP
Q5103
2N7002K-2-GP
3D3V_S0
DY
R5113
100KR2J-1-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

HDMI1
SKT-HDMI23-54-GP
22.10296.721
2nd = 22.10296.761
HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_S0_CRT
C5102
SCD1U10V2KX-5GP
HPD_HDMI_CON

Close to PCH

20 HDMI_CLK_R#
20 HDMI_CLK_R
C5103
C5104
SCD1U10V2KX-5GP
HDMI_CLK_R_C#
HDMI_CLK_R_C

20 HDMI_DATA0_R#
20 HDMI_DATA0_R
C5105
C5106
SCD1U10V2KX-5GP
HDMI_DATA0_R_C#
HDMI_DATA0_R_C

20 HDMI_DATA1_R#
20 HDMI_DATA1_R
C5110
C5107
SCD1U10V2KX-5GP
HDMI_DATA1_R_C#
HDMI_DATA1_R_C

20 HDMI_DATA2_R#
20 HDMI_DATA2_R
C5108
C5109
SCD1U10V2KX-5GP
HDMI_DATA2_R_C#
HDMI_DATA2_R_C

Close to HDMI Connector

RN5106
SRN680J-GP
RN5107
SRN680J-GP
HDMI_PLL_GND

3D3V_S0
Q5102
PMBS3904-1-GP
84.03904.L06
2nd = 84.03904.X11
HDMI_HPD_B1
R5111
150KR2J-L1-GP
DY
R5110
200KR2J-L1-GP
HDMI_HPD_R1
R5128
0R0402-PAD
HDMI_PCH_DET 20,97
R5112
20KR2F-L-GP
20120116PV-R

5V_S0_CRT
3D3V_S0
RN5101
SRN2K2J-1-GP
Q5104
2N7002KDW-GP
20 PCH_HDMI_CLK
20 PCH_HDMI_DATA
DDC_CLK_HDMI
DDC_DATA_HDMI
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.P3F

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

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Title: HDMI Level Shifter/Conn
Size: A3
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<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
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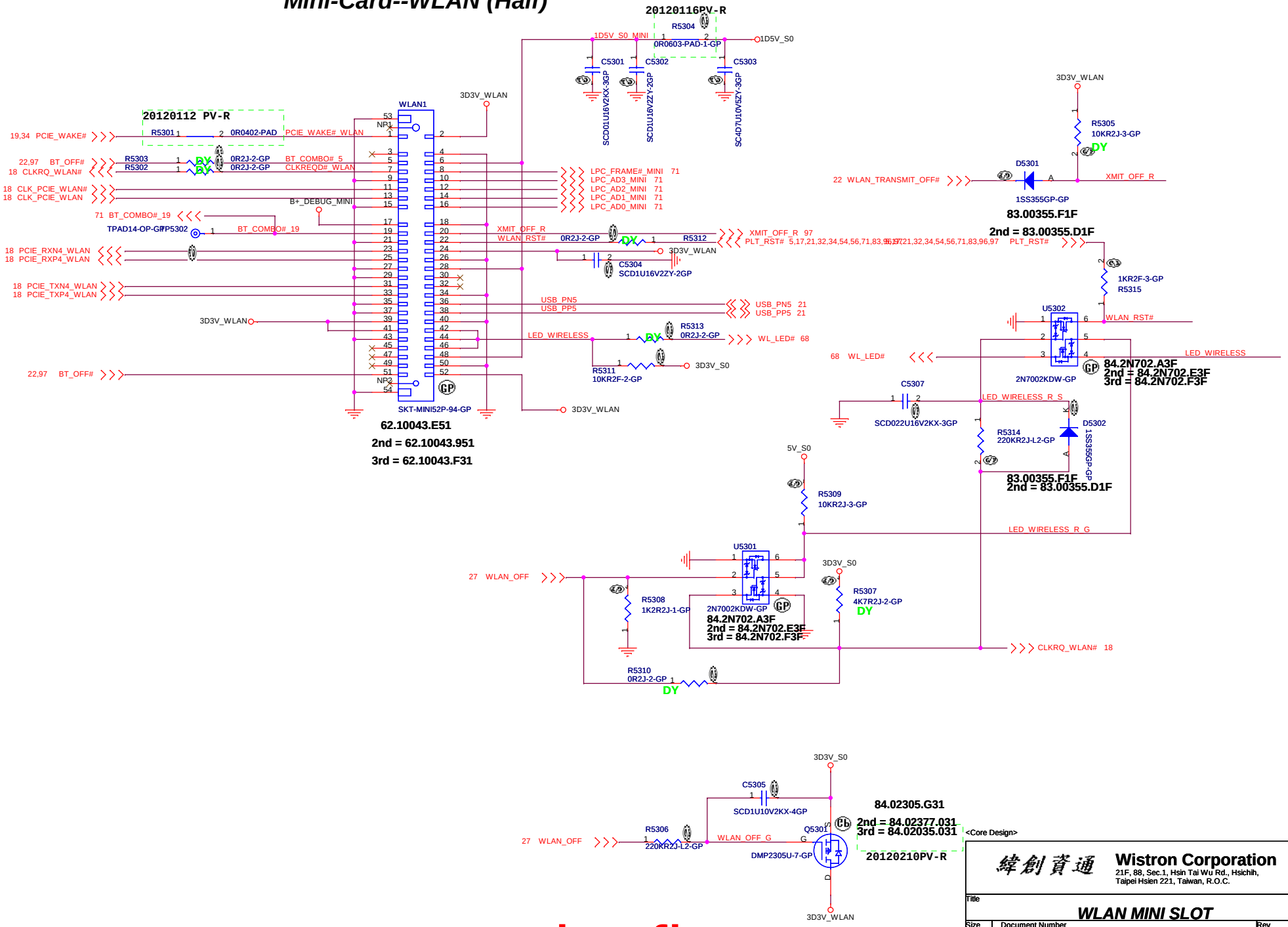
WLAN Connector

Mini-Card--WLAN (Half)



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Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN MINI SLOT

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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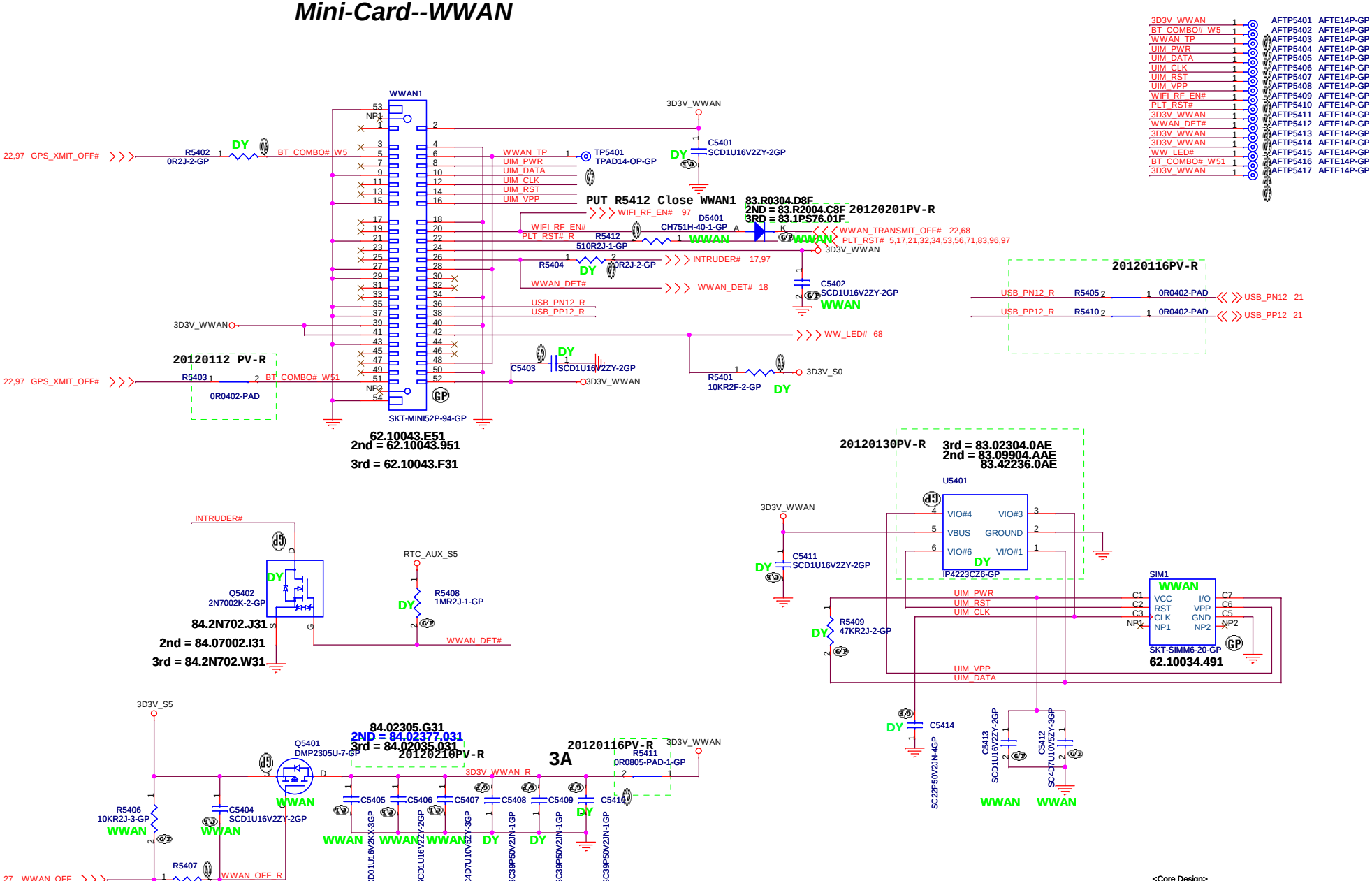
WWAN Connector

Mini-Card--WWAN



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **WWAN MINI SLOT/SIM**

Size	Document Number	Rev
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<Core Design>

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Title: *Reserved*

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A3	2012 S-Series Richie 13.3	-1

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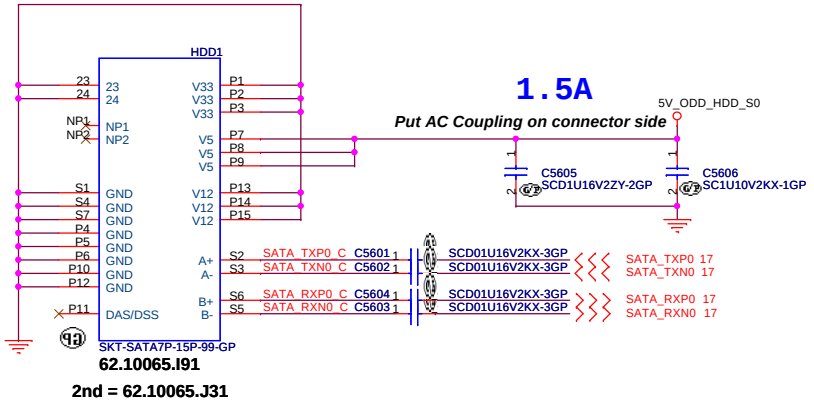
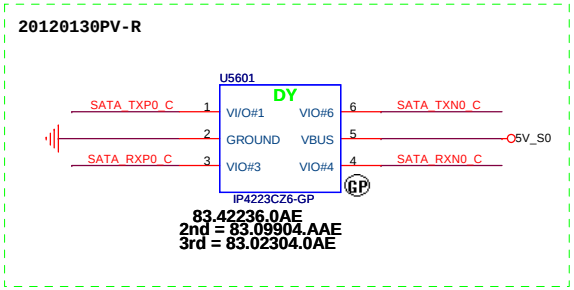
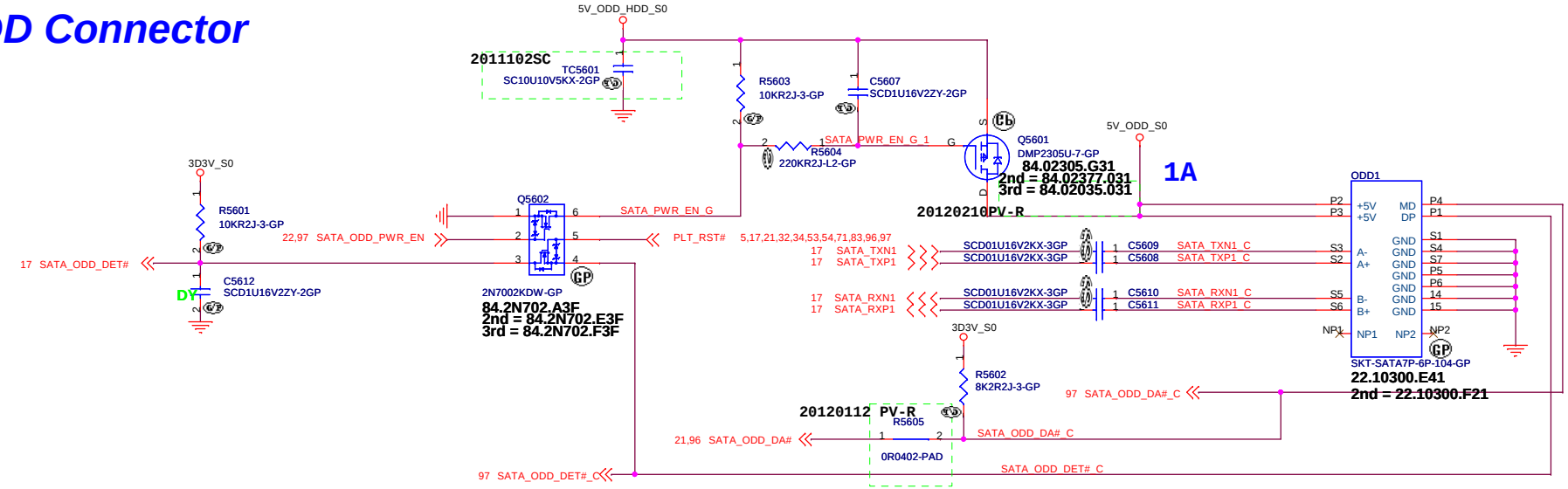
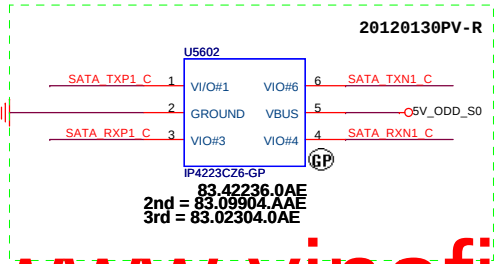
HDD Connector





ODD Connector





<Core Design>

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Title: HDD/ODD

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<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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<Core Design>

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Title: *Reserved*

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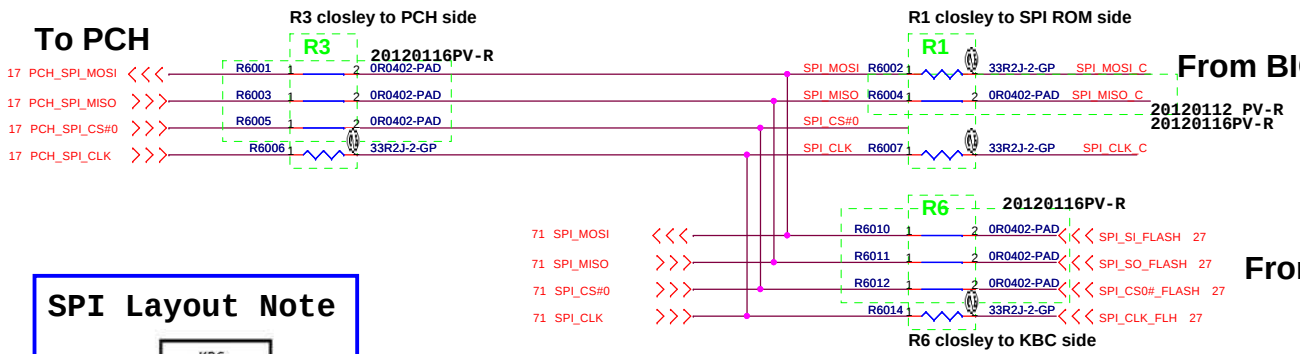
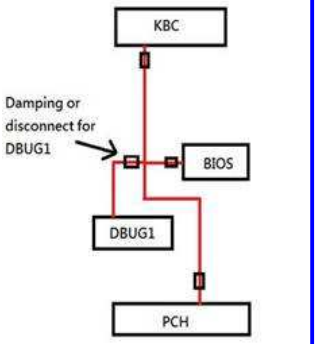
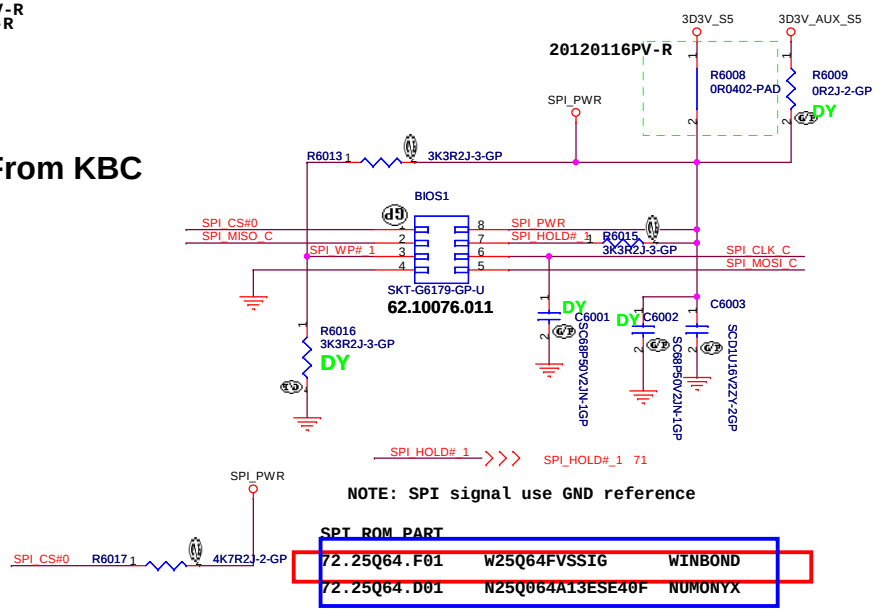
SSID = Flash.ROM



SPI Layout Note



SYSTEM SPI ROM Socket



NOTE: SPI signal use GND reference

SPI ROM PART

72.25Q64.F01	W25Q64FVSSIG	WINBOND
72.25Q64.D01	N25Q064A13ESE40F	NUMONYX

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash

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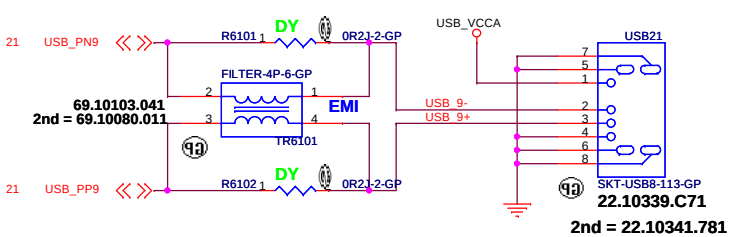
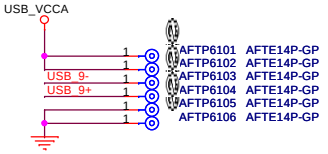
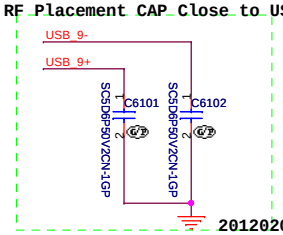
Right Side USB 2.0 Connector

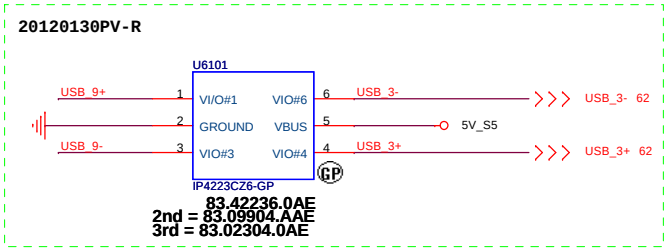
Right Side USB 2.0





For RF Placement CAP Close to USB21





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Title: USB Power SW

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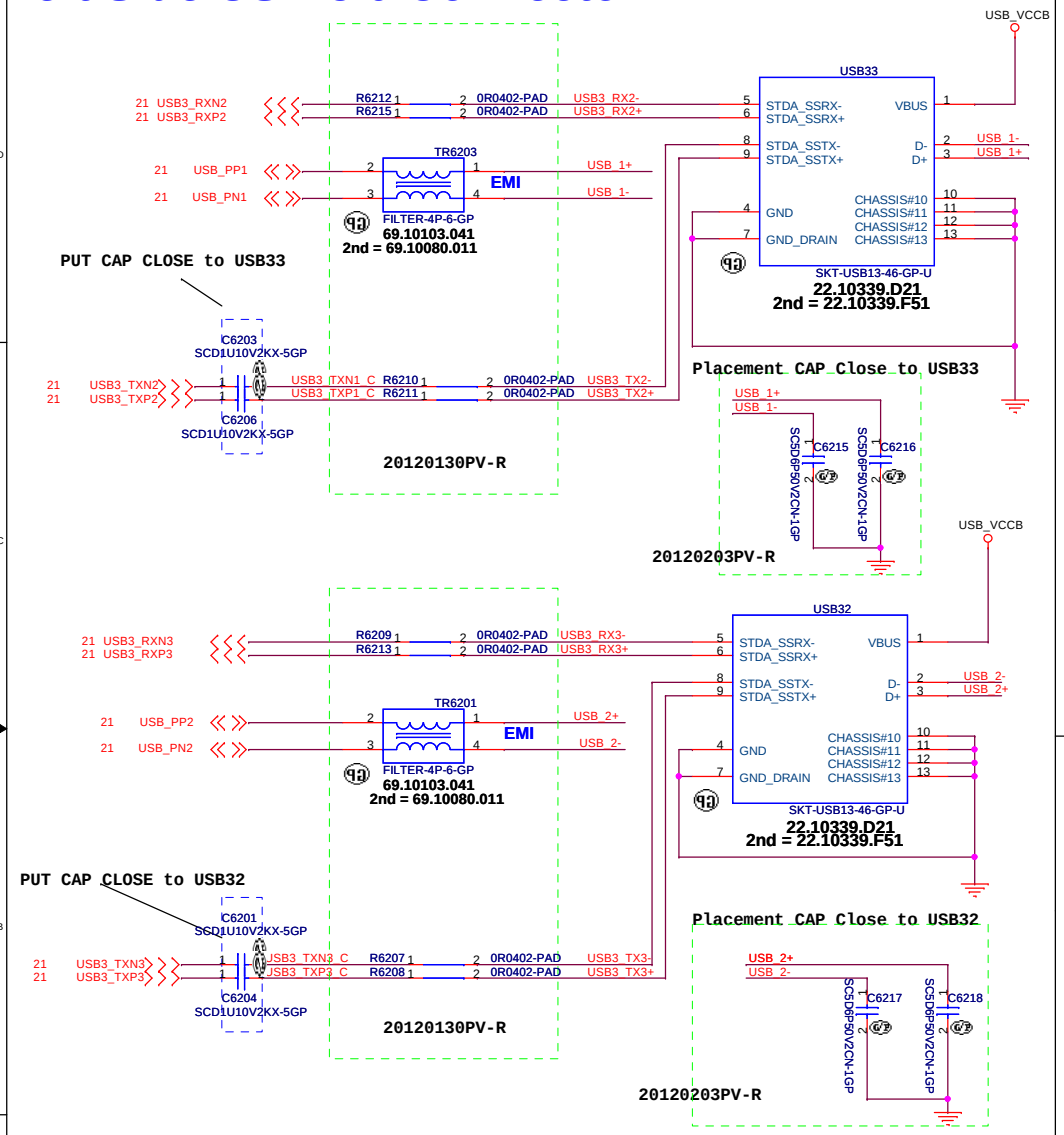
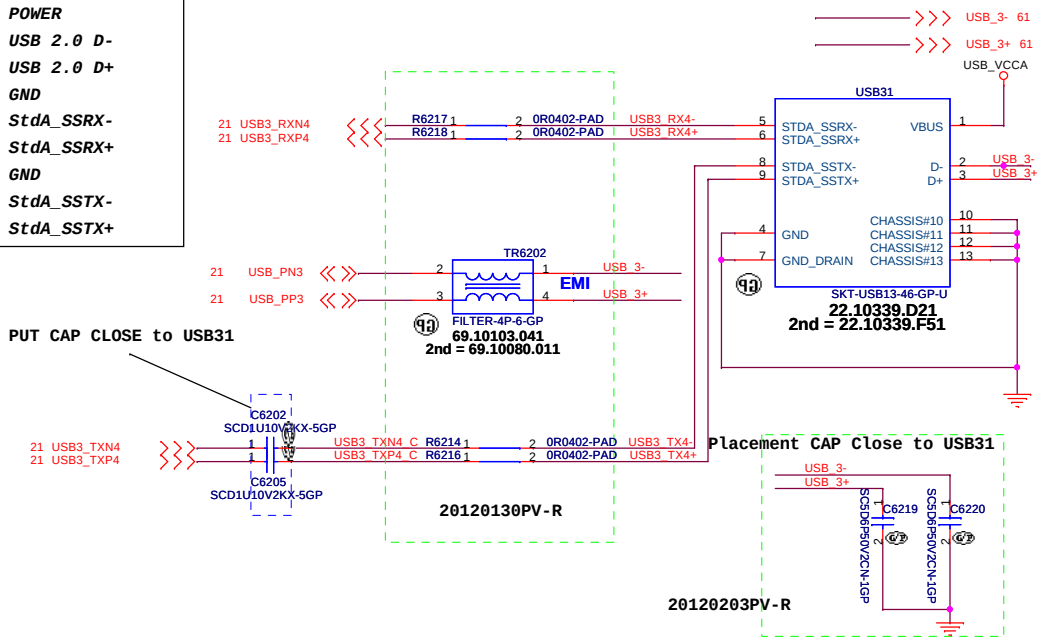
Left Side USB 3.0 Connector

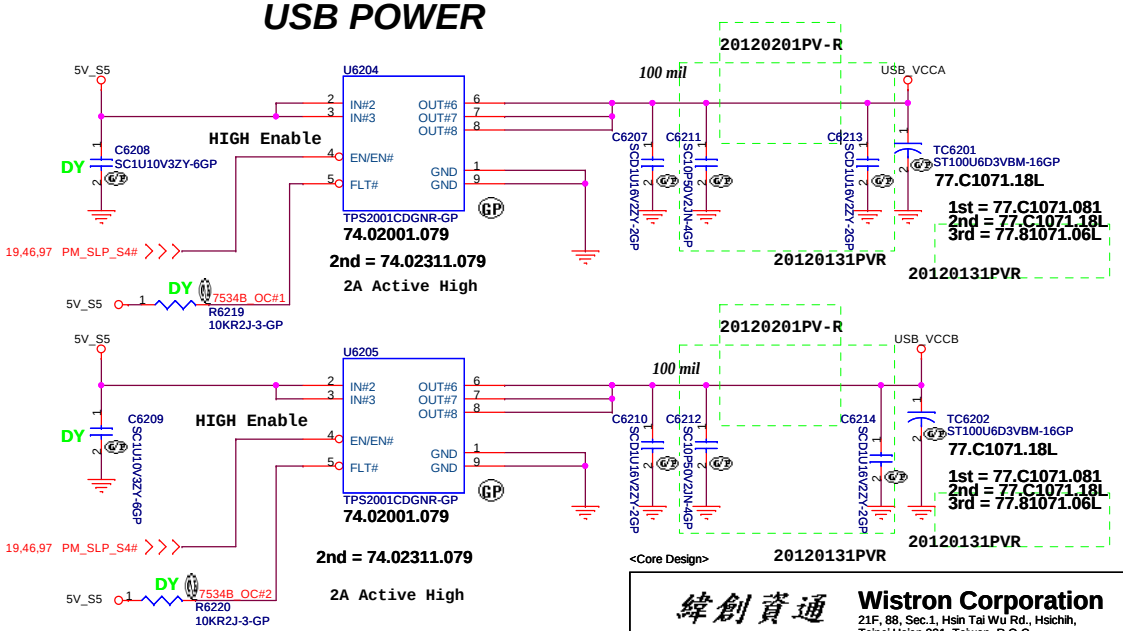


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

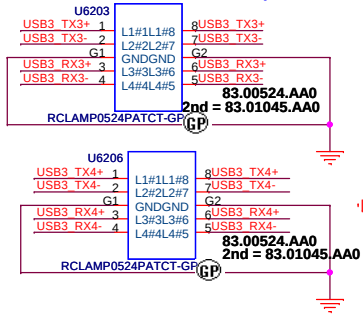
Right Side USB 3.0 Connector



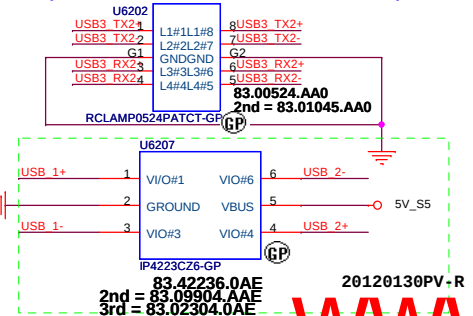
USB POWER



Ultra Low Capacitance TVS Arrays
(Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays
(Pin5.6.7.8 No Internal Connection)



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Title: **USB3.0**

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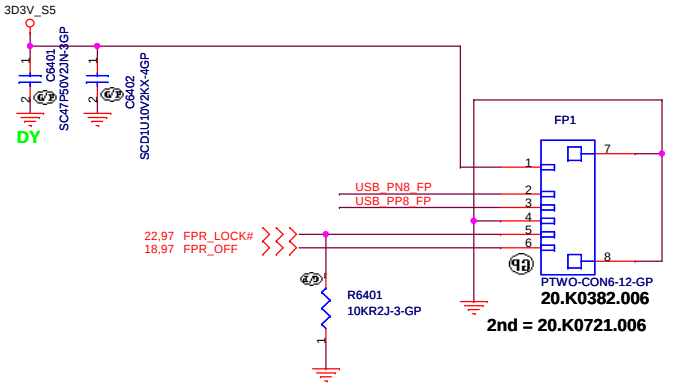
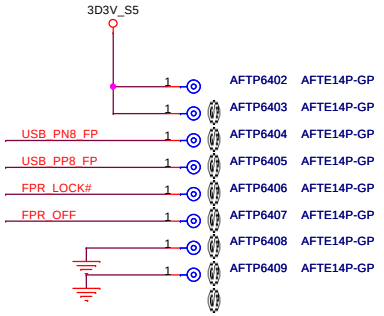
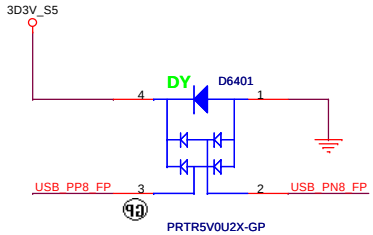
Finger Printer Connector







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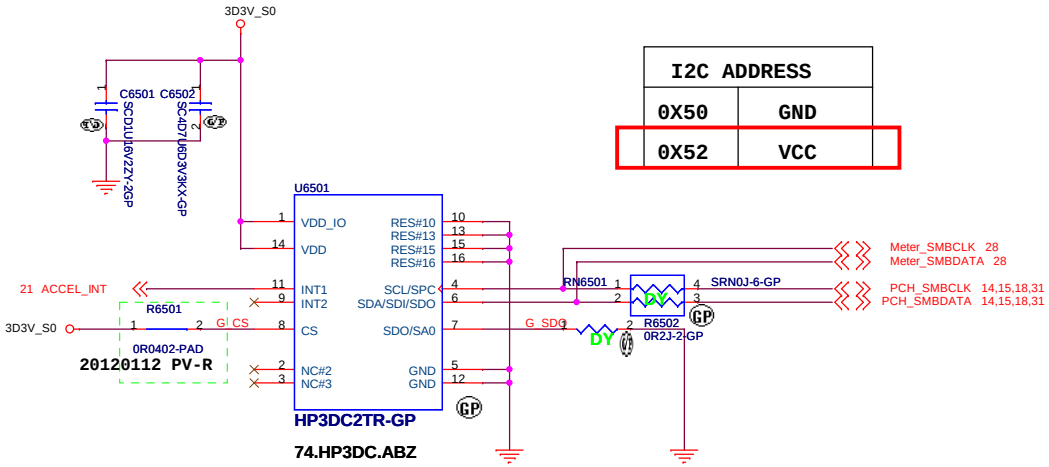
ACCELEROMETER



I2C ADDRESS	
0X50	GND
0X52	VCC

Must be placed in the center of the system

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Title: ACCELEROMETER

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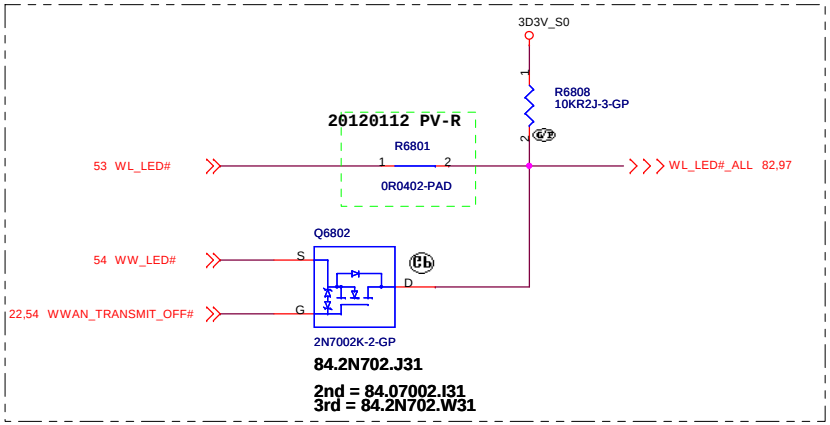
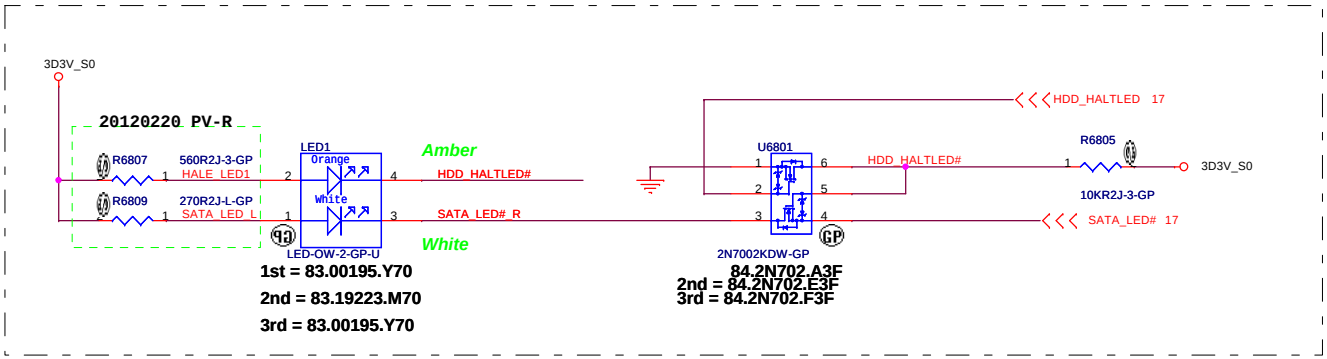
WLAN / WWAN POWER LED



HDD LED



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Title: LED Control

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A3	2012 S-Series Richie 13.3	-1

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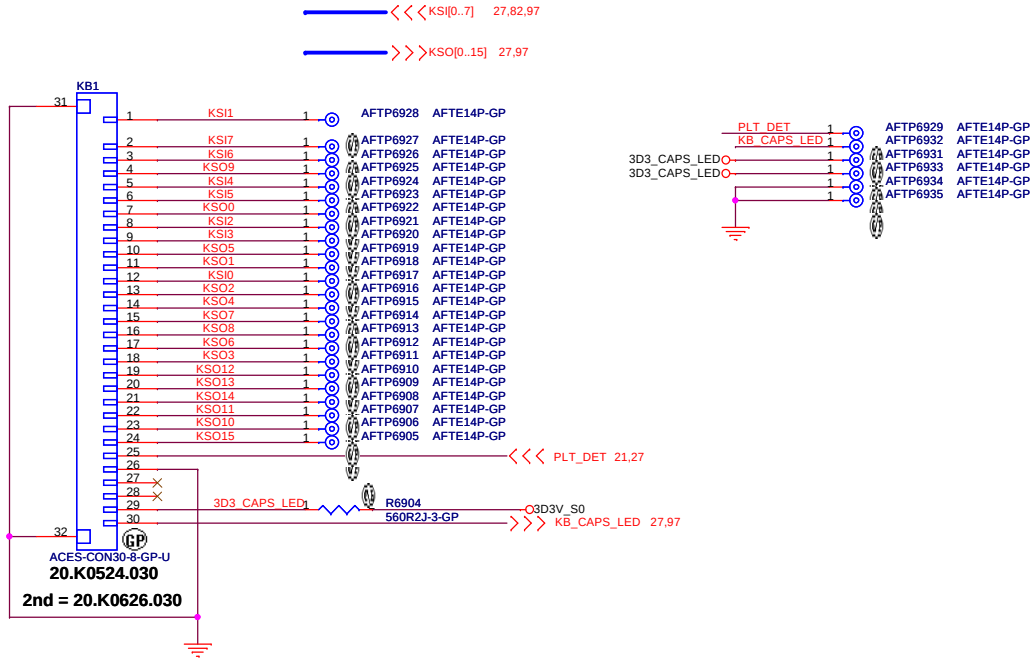
Keyboard Connector



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Title: ***Key Board/Touch Pad***

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A3	2012 S-Series Richie 13.3	-1

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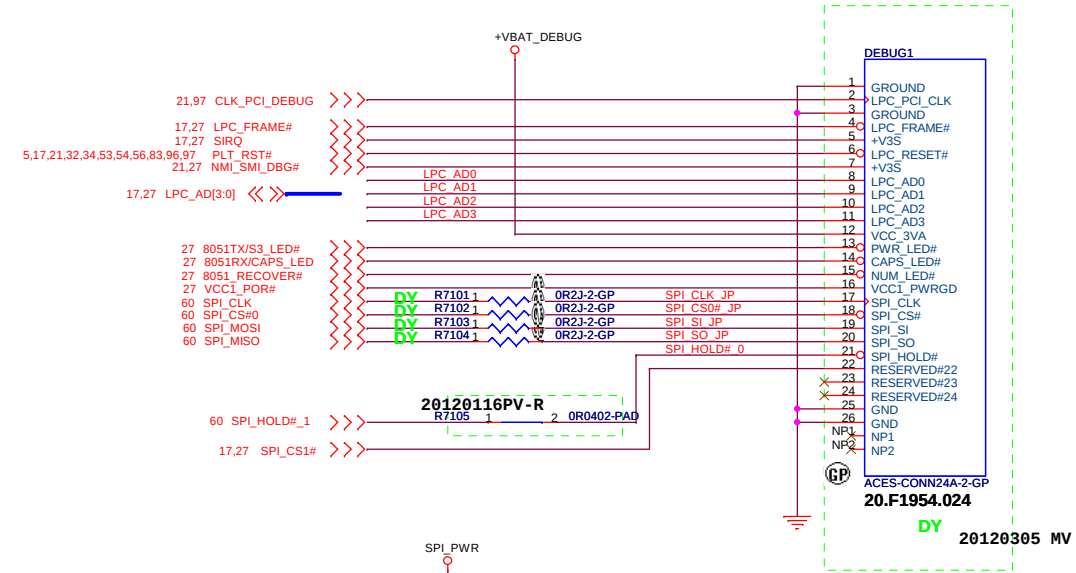
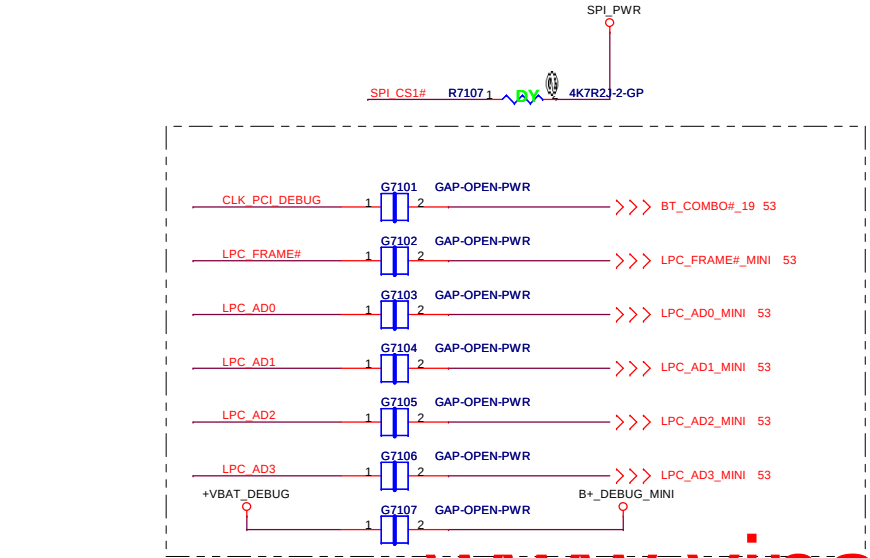
24 PIN LPC DEBUG CONN.





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Title: ***Dubug connector***

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Title: TPM

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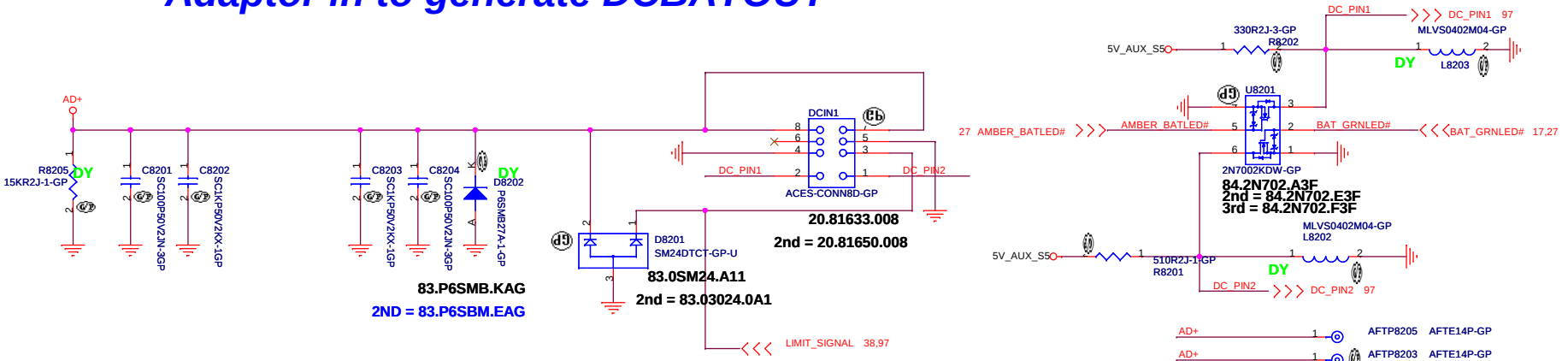
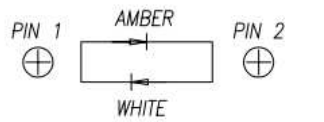
Adaptor in to generate DCBATOUT



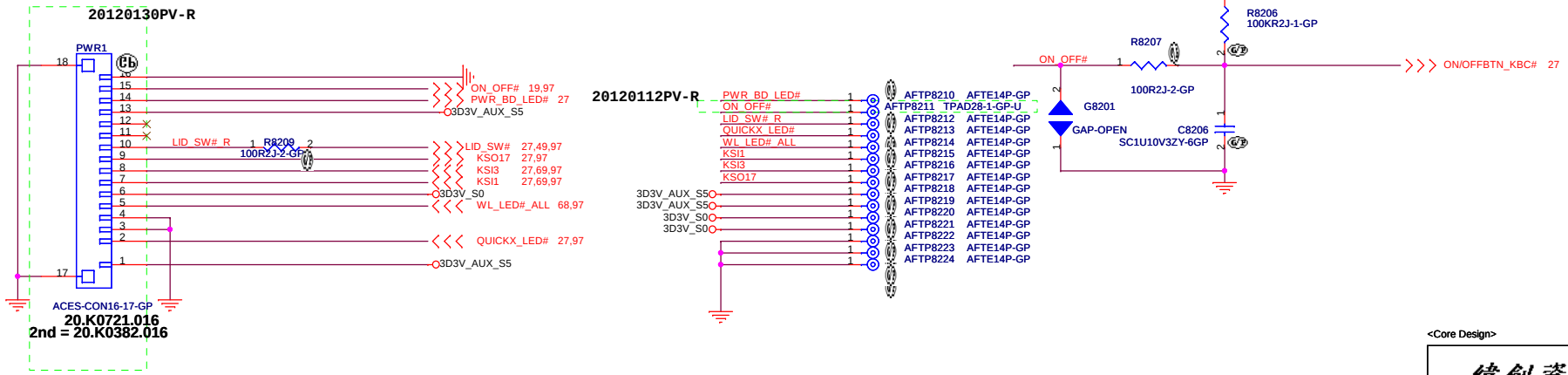
LED TYPE



NODE		COLOR
PIN1(+)	PIN2(−)	AMBER
PIN1(−)	PIN2(+)	WHITE

	KBC pin 120 BAT_GRNLED#	KBC pin 113 AMBER_BATLED#
Amber	High	Low
White	Low	High
LED OFF	Low	Low

Power Button +Quick Lanch board



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Title: POWER Button/ DCIN Connector

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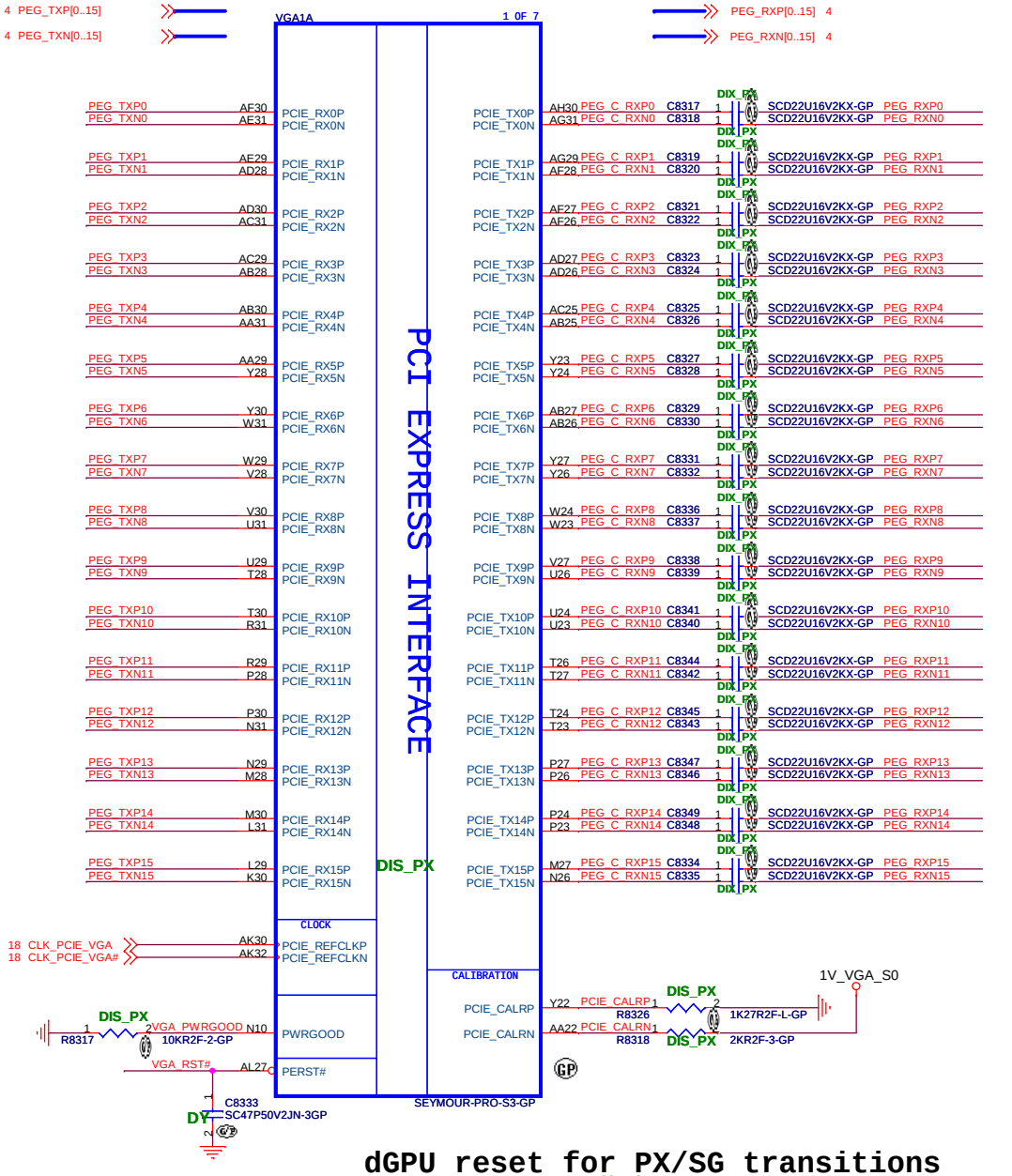
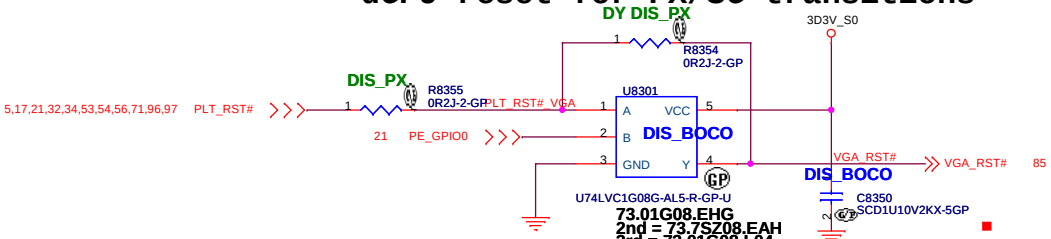


dGPU reset for PX/SG transitions

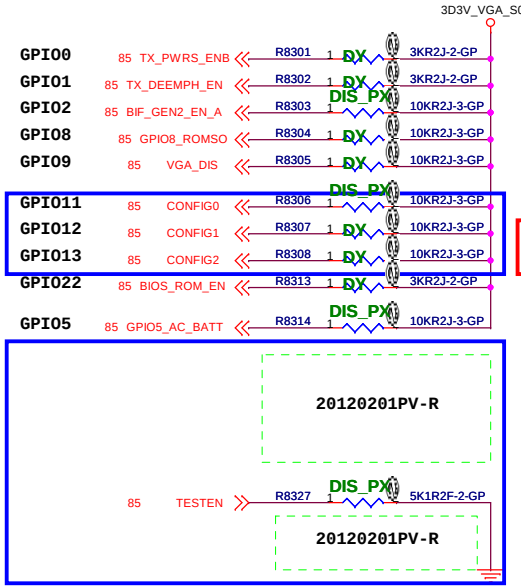


CONFIGURATION STRAPS

ALLOW FOR PULL-UP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1



GPIO_13	GPIO_12	GPIO_11	Memory Aperture Size
0	0	1	512MB/256MB memory aperture (Default)
1	1	0	reserved

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

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Title: GPU PCIE/STRAPPING(1/5)

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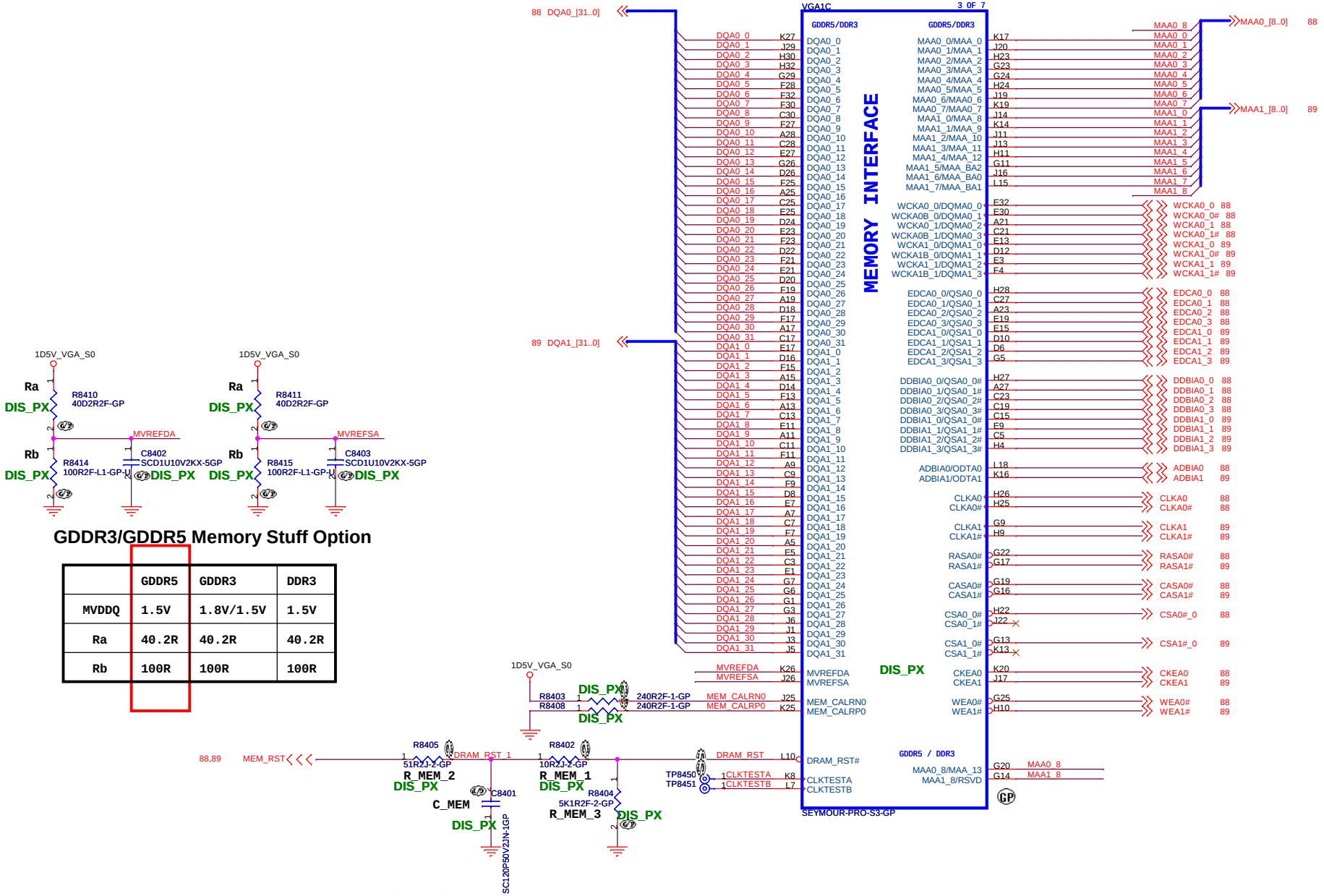

GDDR3/GDDR5 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

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Title: GPU Memory(2/5)

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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VRAM ID TABLE

MEM ID3	MEM ID2	MEM ID1	MEM ID0	MEM ID VALUE	Vendor & PN	DIE Ver
NC	NC	0	0	0	Samsung(128X16) K4G20325FC-HC04	C
NC	NC	1	0	2	Samsung(128X16) K4G20325FD-FC04	D
NC	NC	0	1	1	Hynix(128MX16) H5GQ2H24MFR-T2C	M
NC	NC	1	1	3	Hynix(128MX16) H5GQ2H24AFR-T2C	A
NC	NC	0	0	0	Elpida(128MX16) EDW2032BBBG-50-F	B
NC	NC	NC	NC	NC	UMA	

Reserve Pul-High Resistor for MEM_ID2/MEM_ID3

B= Old Die
1= New Die

VBIOS 1 : Samsung
VBIOS 2 : Hynix
VBIOS 3 : Elpida

GPU Power ID Table

GPU SIDE		UP1527QQDD
GPIO_15_PWRCNTL_0	GPIO_20_PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V

LVDS Interface

VGA1F — 6 OF 7

LVDS CONTROL: VARY_BL, DIGON

LVTMDP: TXCLK_UP_DPF3P/N, TXOUT_U0P_DPF2P/N, TXOUT_U1P_DPF1P/N, TXOUT_U2P_DPF0P/N, TXOUT_U3P/N, TXCLK_LP_DPE3P/N, TXOUT_L0P_DPE2P/N, TXOUT_L1P_DPE1P/N, TXOUT_L2P_DPE0P/N, TXOUT_L3P/N

SEYMOUR-PRO-S3-GP

CTF setpoint is 118°C, and is programmed during ASIC initialization.

Intel is H_THERMTRIP#

SSEL1 (Pin 3)	SSEL0 (Pin 7)	Spread Percent (%) SSCLK (Pin 5)
Low (VSS)	Low (VSS)	Spread Off (No Spread)
Low (VSS)	Middle (Floating)	-0.50%
Low (VSS)	High (VDD)	-2.5%
Middle (Floating)	Low (VSS)	-0.25%
Middle (Floating)	Middle (Floating)	-0.75%
Middle (Floating)	High (VDD)	-1.0%
High (VDD)	Low (VSS)	-1.5%
High (VDD)	Middle (Floating)	-2.0%
High (VDD)	High (VDD)	-3.0%

Recommended Clock-Input Configurations

Memory Type	Description
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

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Title: GPU_DP/LVDS/CRT/GPIO(3/5)

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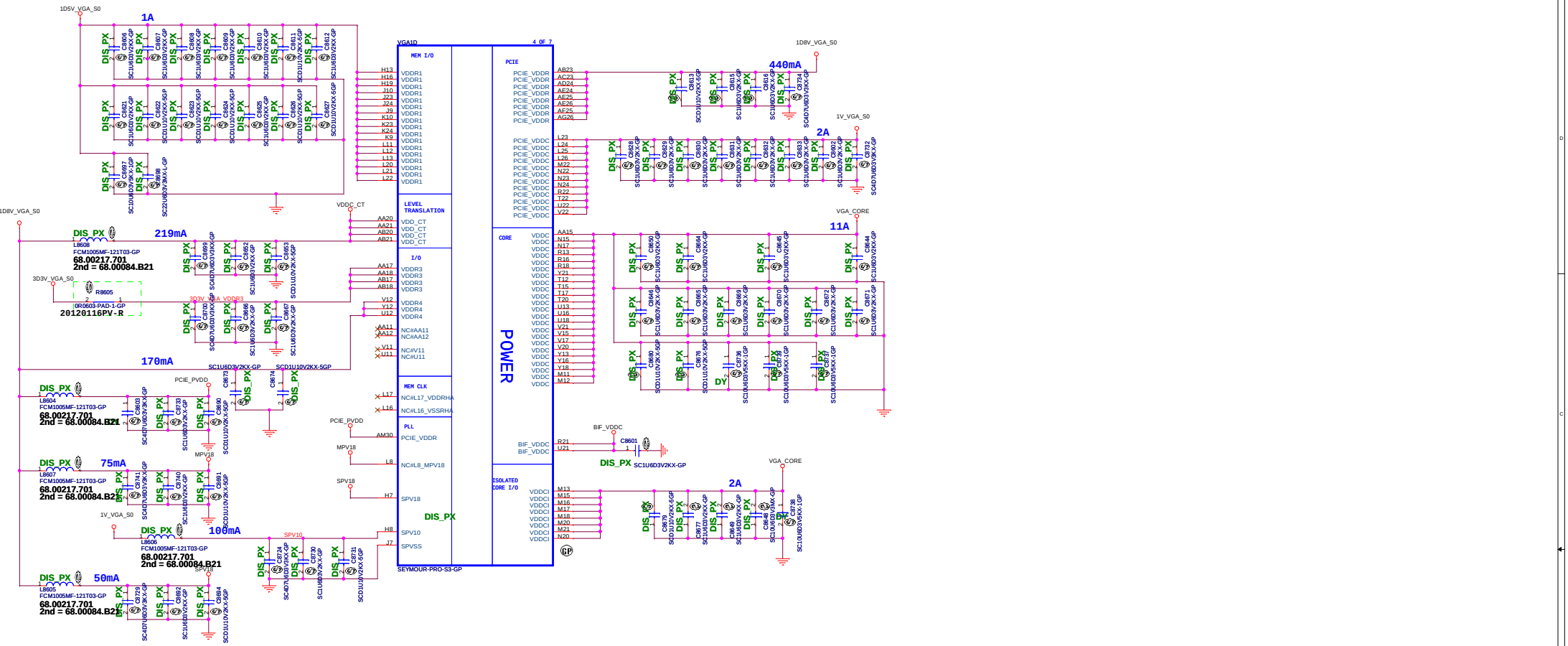
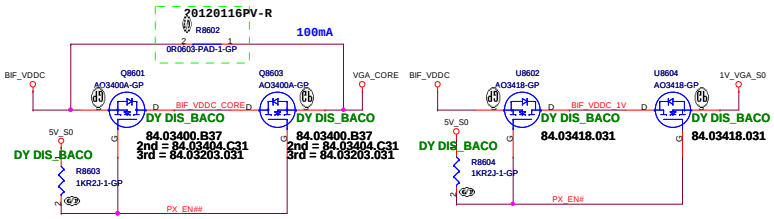
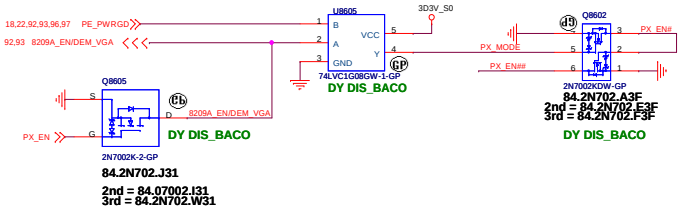




	PX_EN	8209A_EN/DEM_VGA	PX_MODE	PX_EN#	PX_EN##	BIF_VDDC
Non-BACO	0	1	1	0	1	VGA_Core
BACO	1	0	0	1	0	1V_VGA

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN## = High, BIF_VDDC = VGA_CORE



PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

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Title: GPU_POWER(4/5)

Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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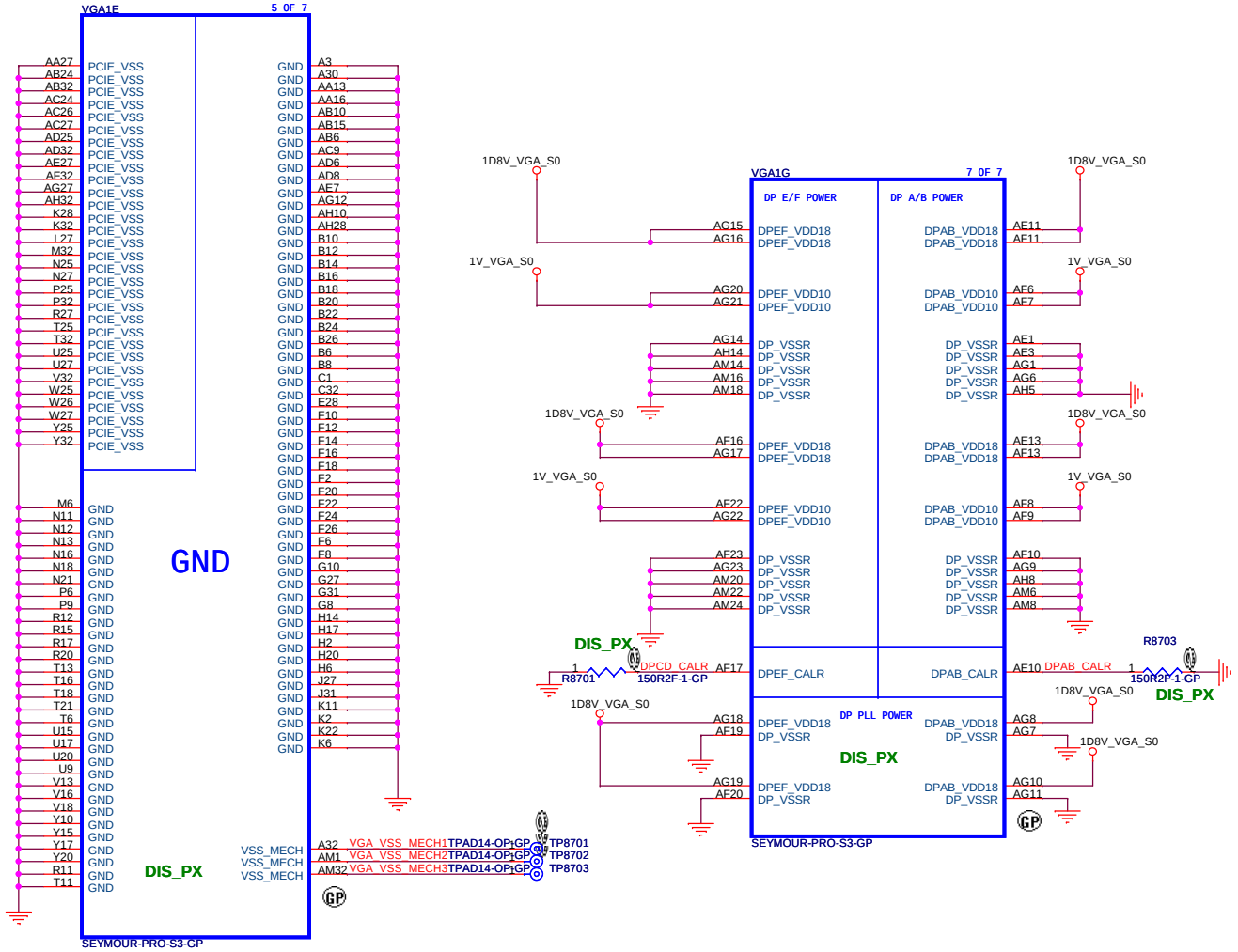

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Title: GPU_DPPWR/GND(5/5)

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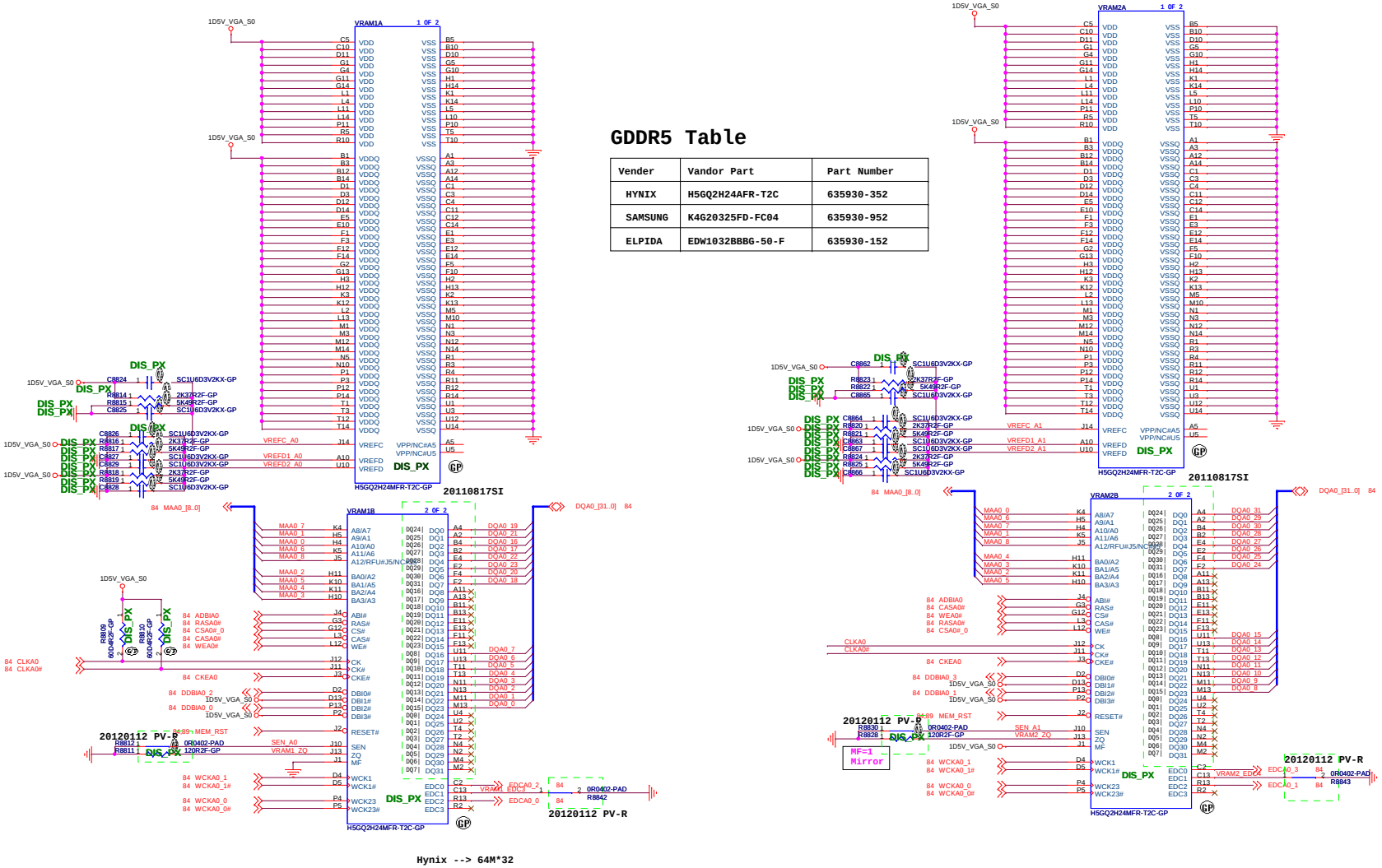
GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24AFR-T2C	635930-352
SAMSUNG	K4G20325FD-FC04	635930-952
ELPIDA	EDW1032BBBG-50-F	635930-152



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Title: GPU-VRAM1,2 (1/4)

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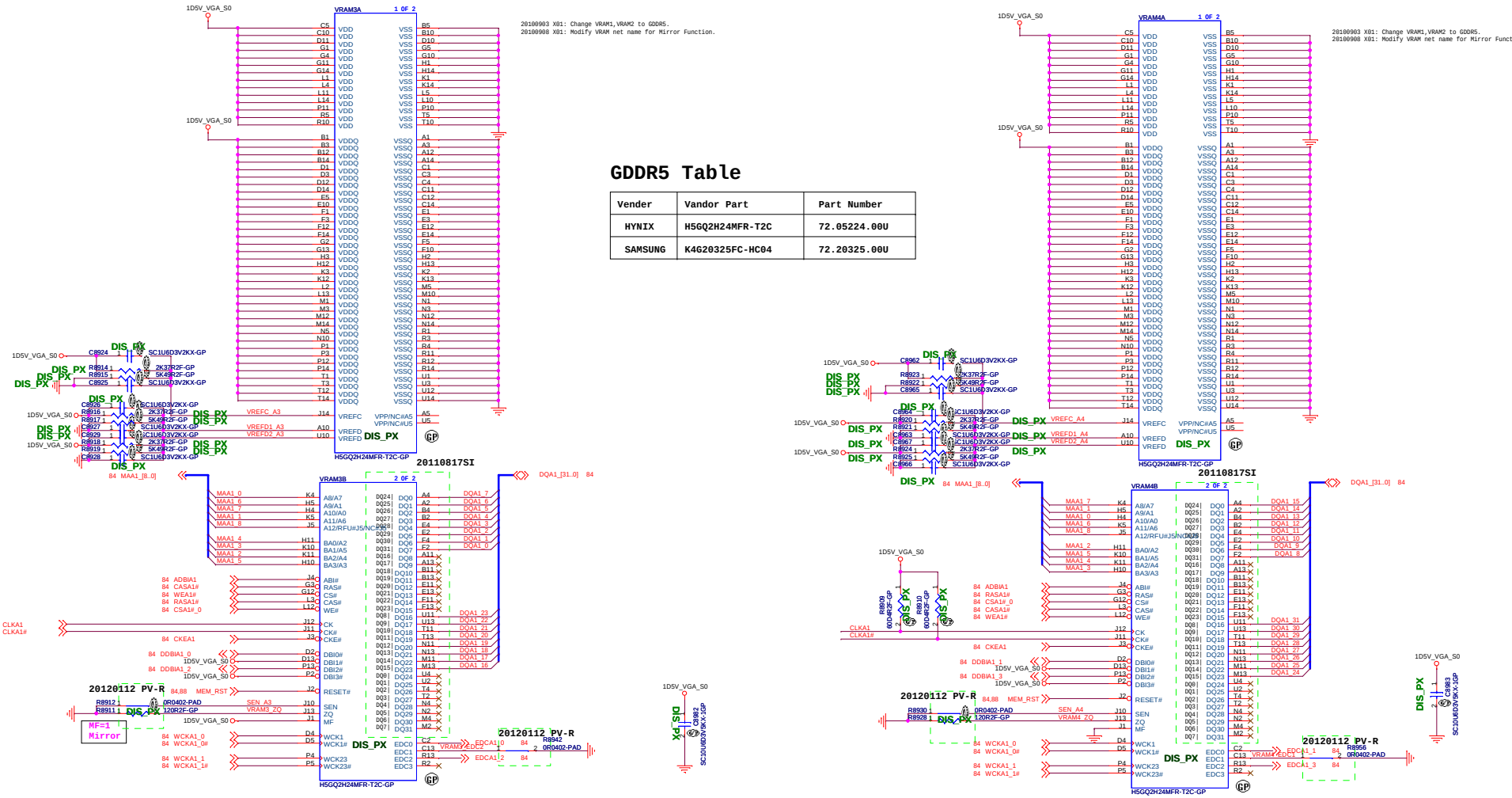

GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24MFR-T2C	72.05224.00U
SAMSUNG	K4G20325FC-HC04	72.20325.00U

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Title: GPU-VRAM3,4 (2/4)

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Title: *(Reserved) GPU-VRAM5,6 (3/4)*

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Title: *(Reserved) GPU-VRAM7,8 (4/4)*

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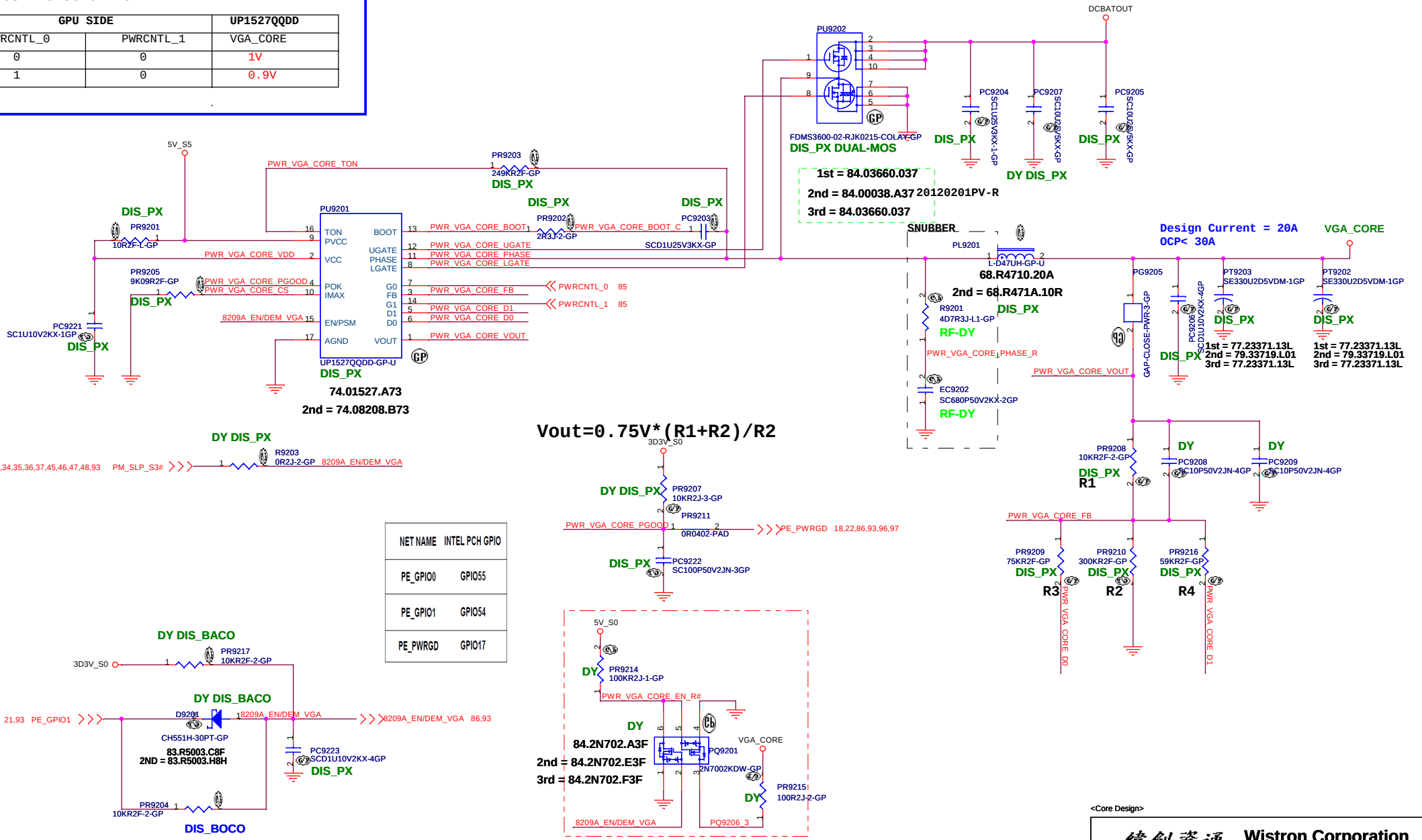
+VGA_CORE

GPU Power ID Table

Thames Pro S3 GDDR5

GPU SIDE		UP1527QQDD
PWRCNTL_0	PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V



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Title: VGA_ISL95870

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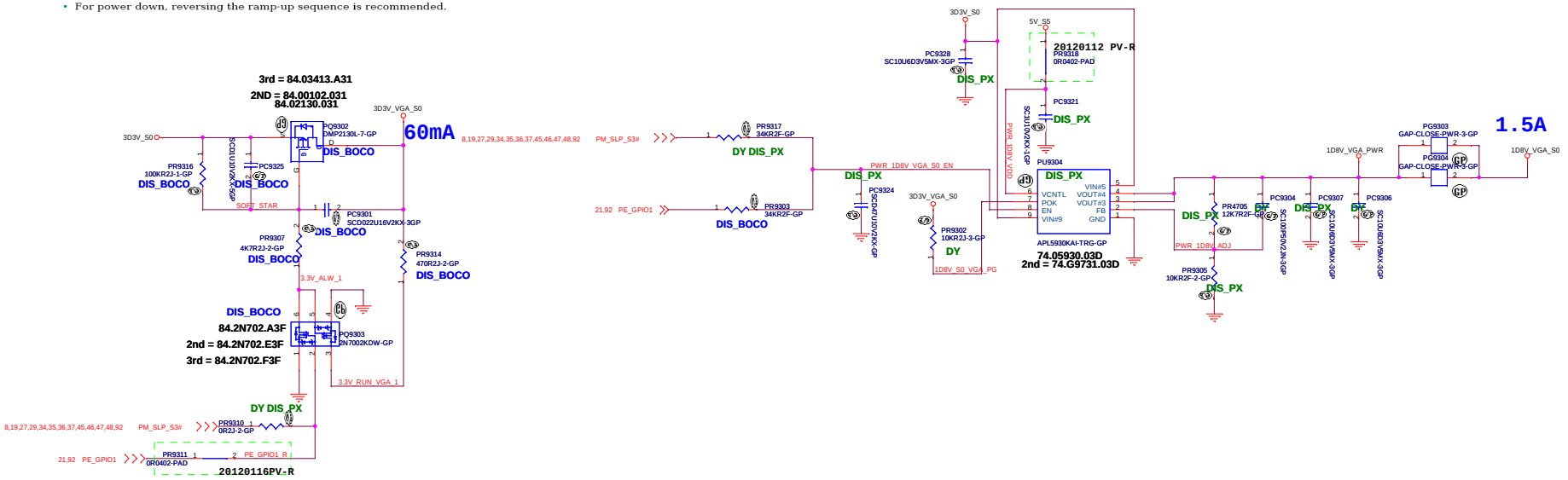
5.3 Power-Up/Down Sequence

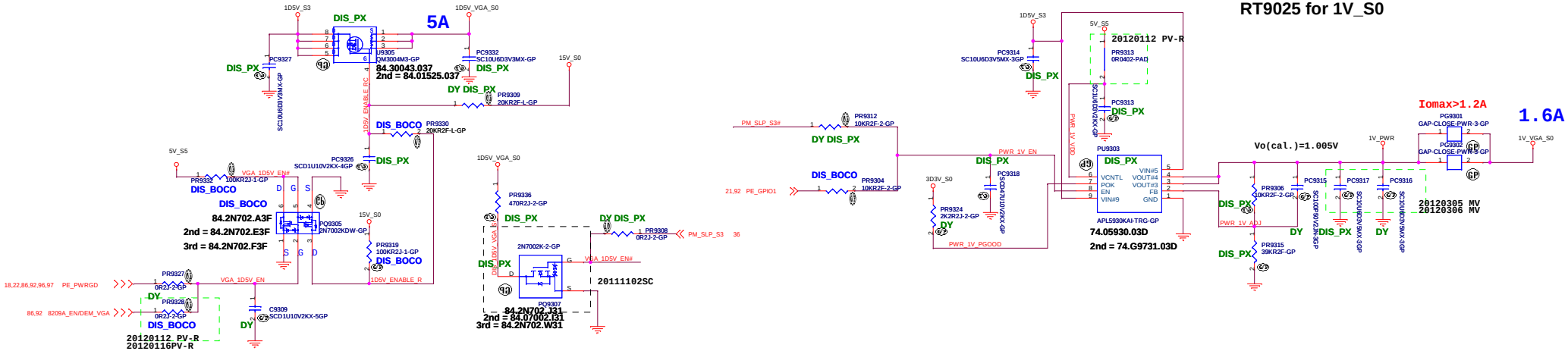
Seymour has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for **VDDR3**, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of **VDDR3** relative to other power rails.
- The external pull-up resistors on the **DDC/AUX** signals (if applicable) should ramp up before or after both **VDDC** and **VDD_CT** have ramped up.
- **VDDC** and **VDD_CT** should not ramp up simultaneously. For exmaple, **VDDC** should reach 90% before **VDD_CT** starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

3D3V_VGA_S0 > VGA_CORE > 1V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0



1D5V_VGA_S0



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Title: DISCRETE VGA POWER

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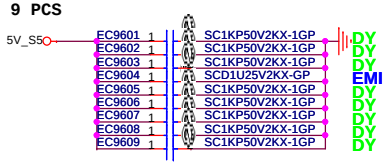
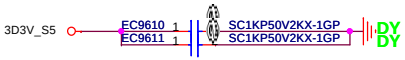
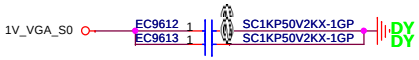
5V_S5 9 PCS



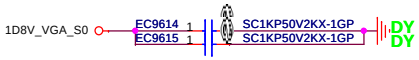
1D8V_PWR 2 PCS



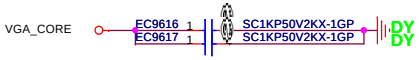
1V_VGA_S0 2 PCS



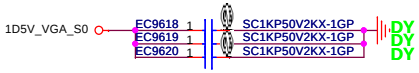
1D8V_VGA_S0 2 PCS



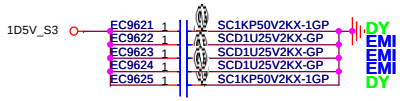
VGA_CORE 2 PCS



1D5V_VGA_S0 2 PCS

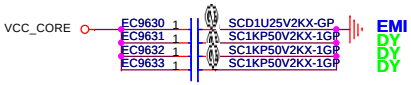


1D5V_S3 8 PCS

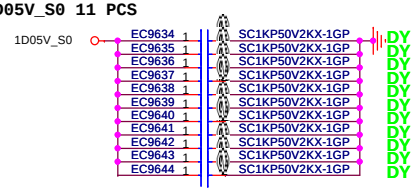


VCCSA 1 PCS

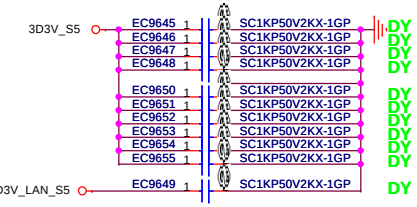
VCC_CORE 4 PCS



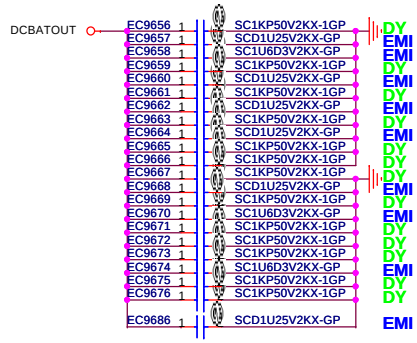
1D05V_S0 11 PCS

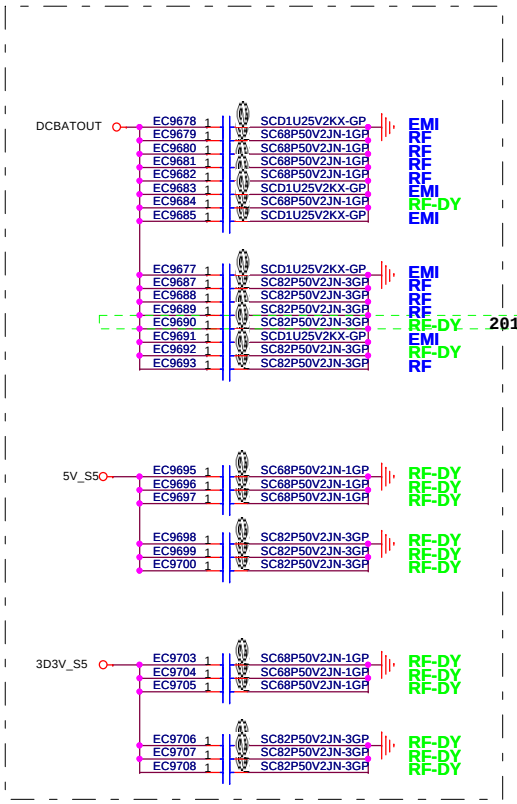


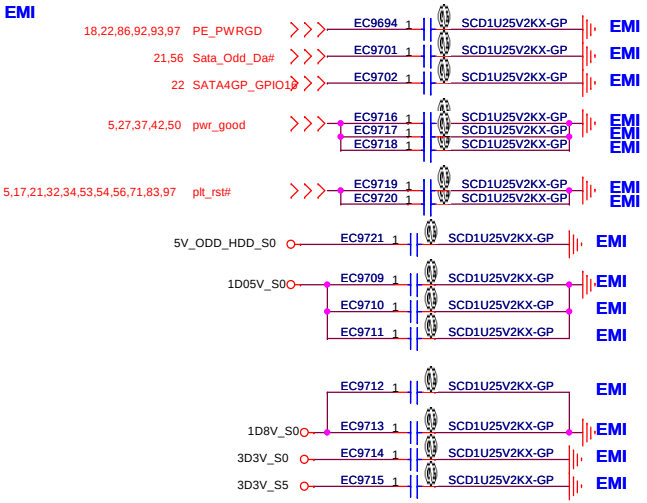
3D3V_S5 11 PCS



DCBATOUT 21 PCS







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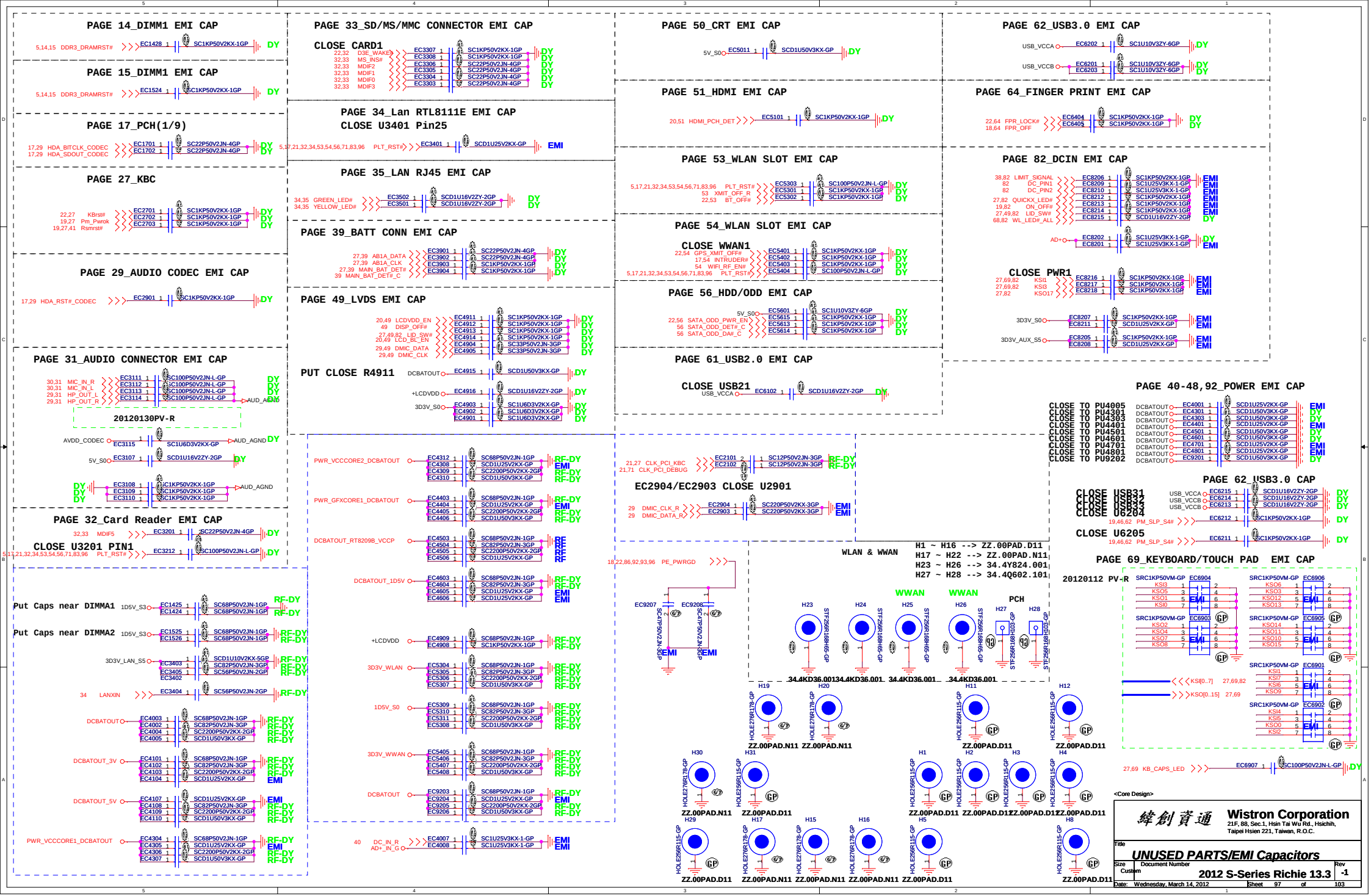

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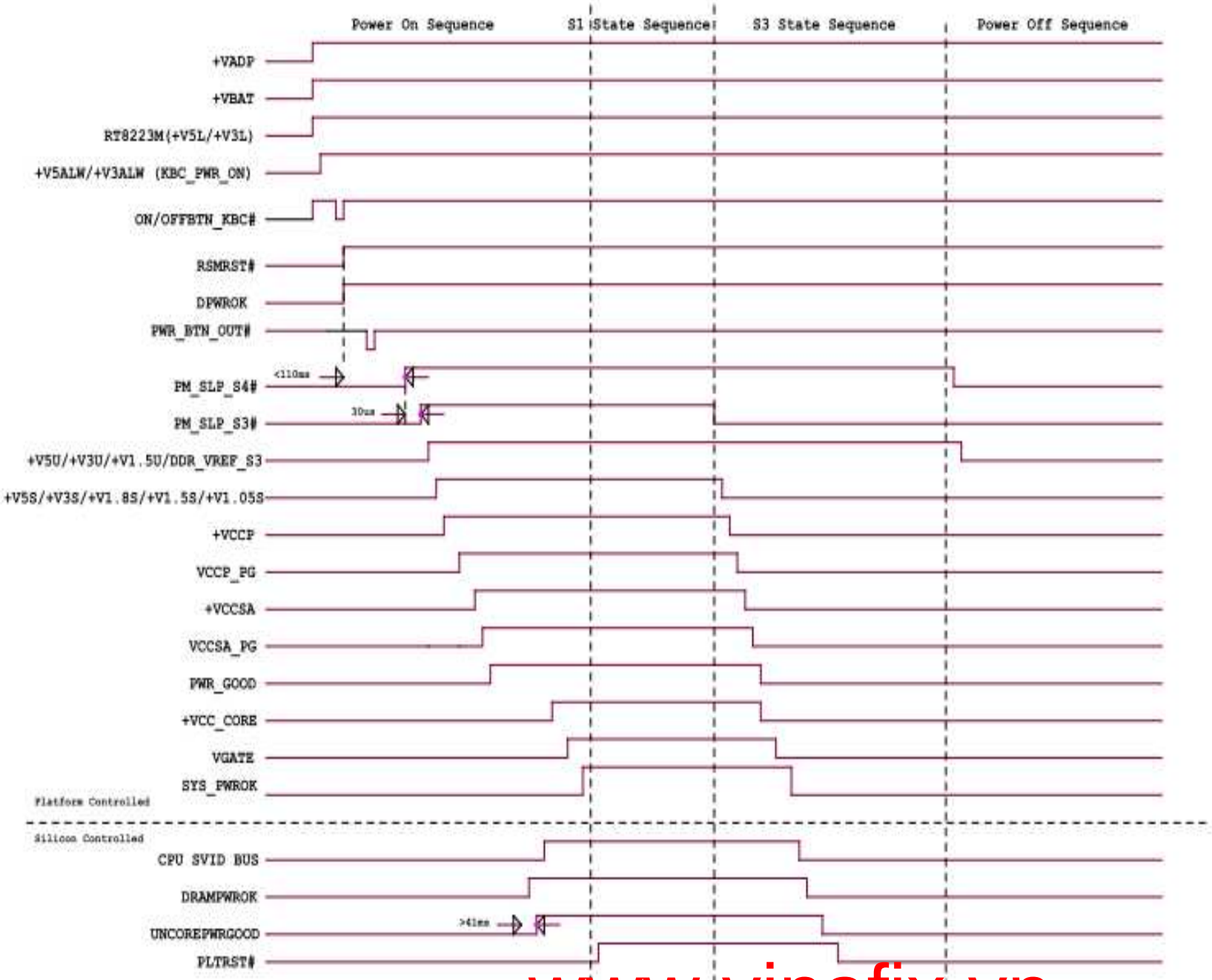
S-Series Power Sequence and Reset Signal Timing



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Title: *Power Sequence*

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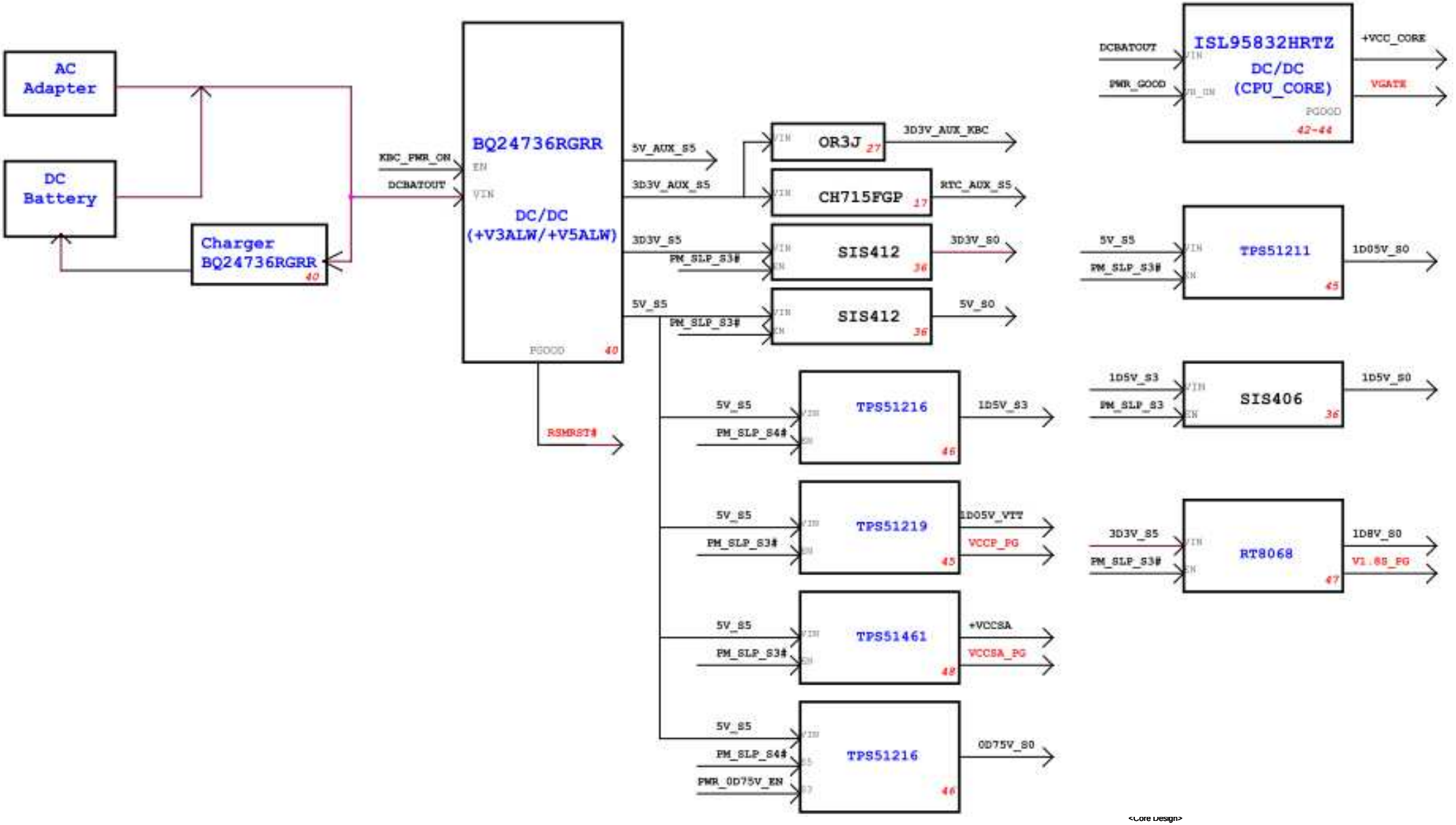
S-Series POWER BLOCK DIAGRAM



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Title: Power Block Diagram

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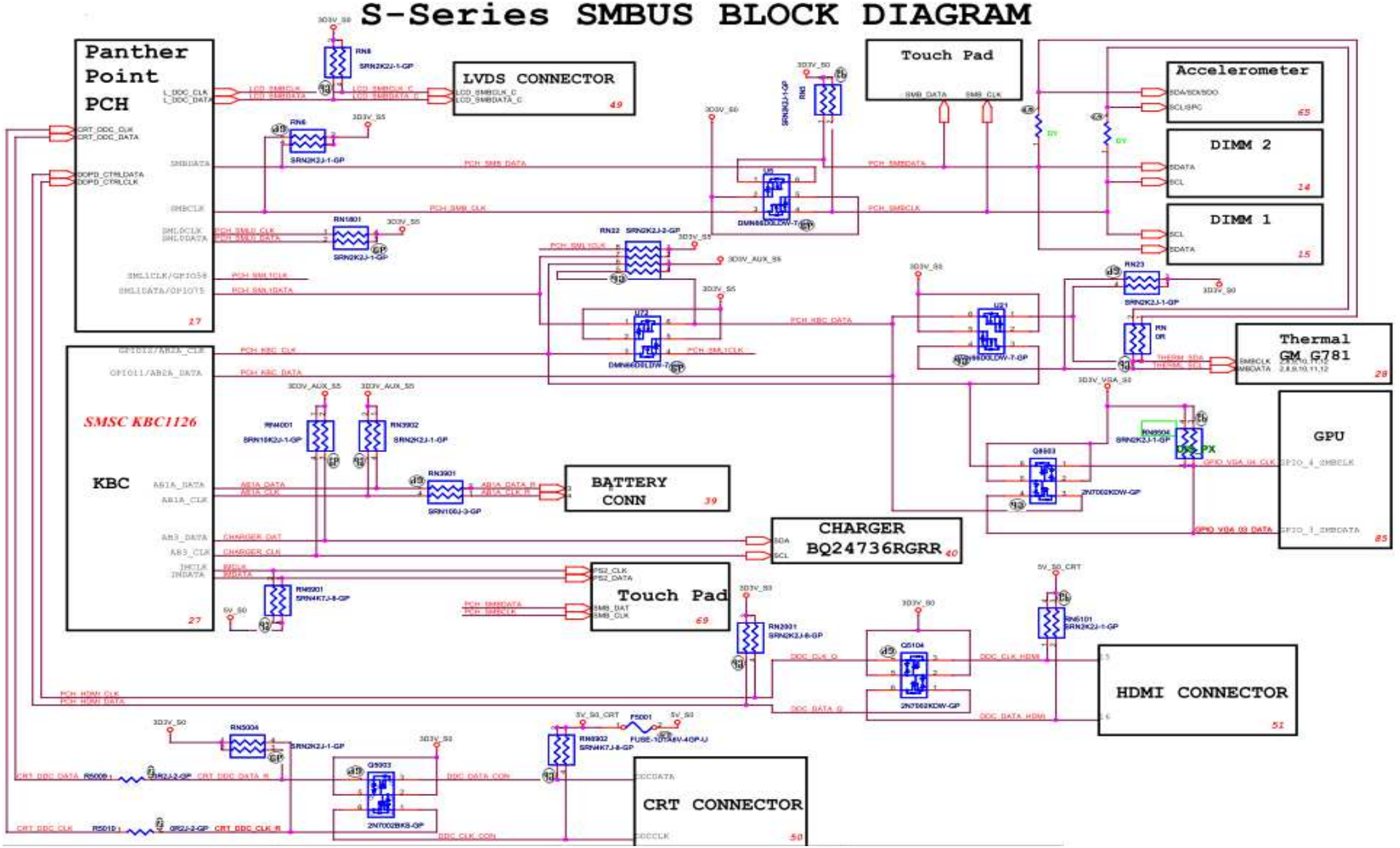
S-Series SMBUS BLOCK DIAGRAM



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Title: SMBUS Block Diagram

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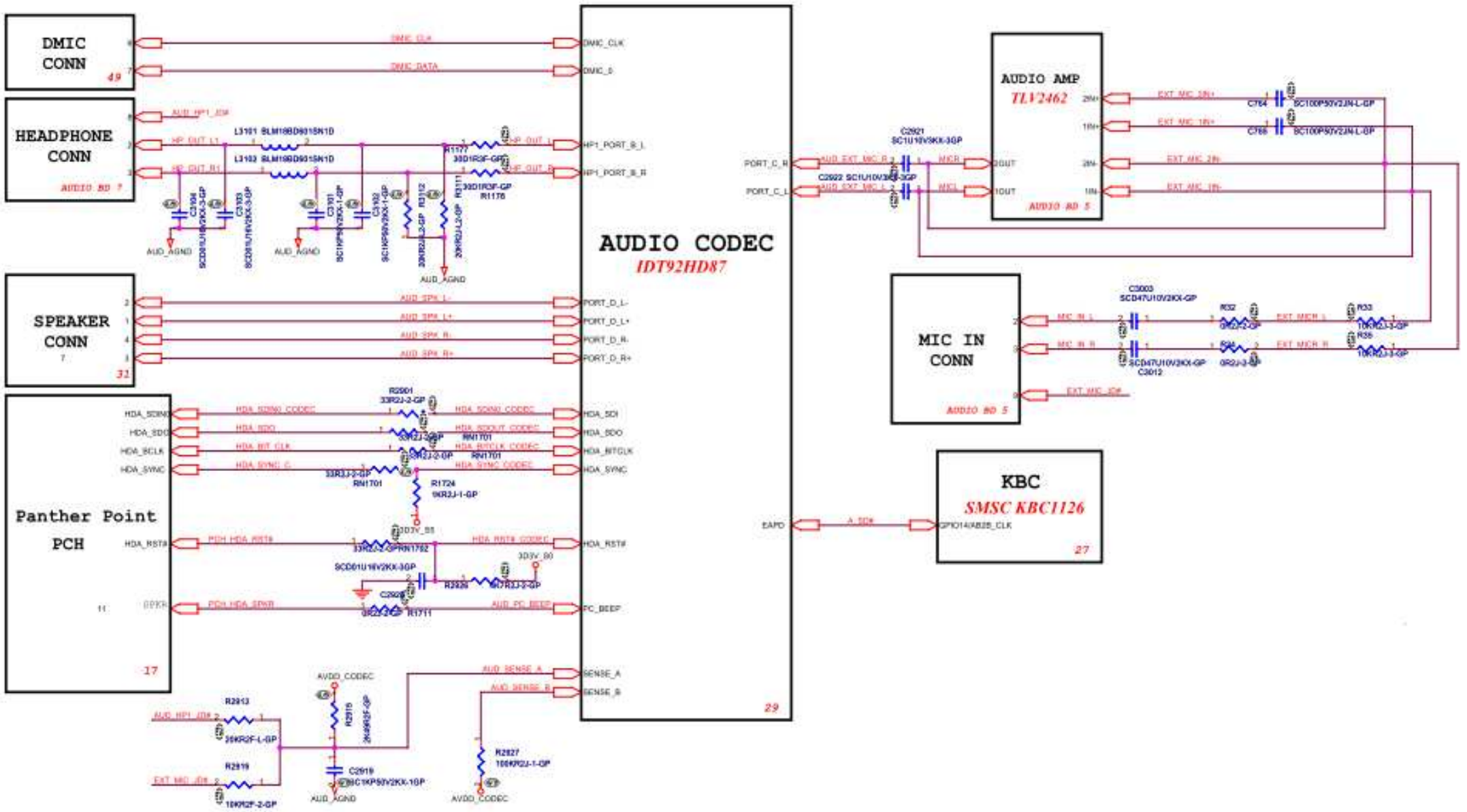
S-Series AUDIO BLOCK DIAGRAM



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Title: Thermal/Audio Block Diagram

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Title: mSATA

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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