Dual-Input Triple-Output Power Multiplexer in PSOP-8L for USB High Side Switch

General Description

The uP7535 is a current limited, dual-input triple-output power multiplexer acting as a high side switch for USB applications where heavy capacitive loads and short-circuits are likely to be encountered. It switches output voltages to 5VSB at S3/S4/S5 states with 500mΩ switches and 400mA capacity; to 5VCC at S0/S1/S2 states with 150mΩ switches and 1.2A capacity. The outputs can be parallelled to provide totally 3.0A output current at S0/S1/S2 states.

Optimal switch logic according to S3# and 5VCC status ensures seamless output voltage transition.

When the output load exceeds the current-limit threshold or a short is present, the uP7535 asserts over current protection and limits the output current to a safe level by driving the power switches into saturation mode.

Other features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present. The uP7535 is available in PSOP-8L package.

Applications

- Notebook and Desktop PCs
- USB Power Management
- ACPI Power Distribution
- Hot-Plug Power Supplies

Features

- Compliant to USB Specifications
- Operating Range: 4.5 V to 5.5 V
- Output Voltage Switch to 5VSB at S3/S4/S5
  - 400mA Continuous Load Current
  - 500mΩ High Side Switch
- Output Voltage Switch to 5VCC at S0/S1/S2
  - 1.2A Continuous Load Current
  - 150mΩ High Side Switch
- Low Quiescent Current: 100uA Typical
- Slow Turn On and Fast Turn Off
- Enable Active-High
- Pb-Free (RoHS Compliant)
- UL Approved: E338429
- TuV EN60950-1 Certification

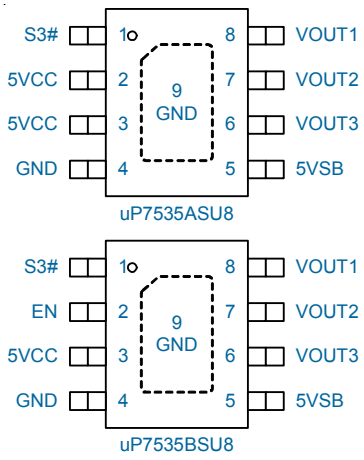
Ordering Information

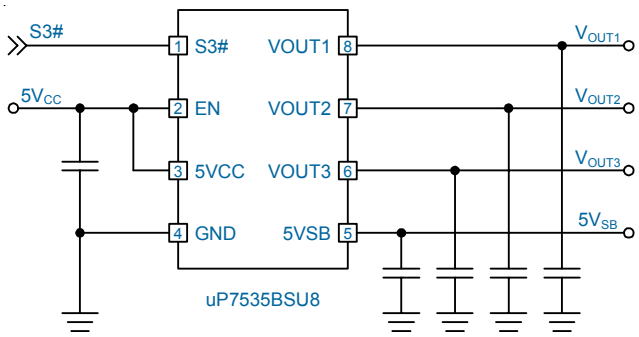
Order Number	Package Type	Top Marking
uP7535ASU8	PSOP-8L	uP7535S8
uP7535BSU8	PSOP-8L	uP7535BS8

Note :
uP7535ASU8 has EN pin.
uP7535BSU8 has no EN pin

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration & Typical Application Circuit

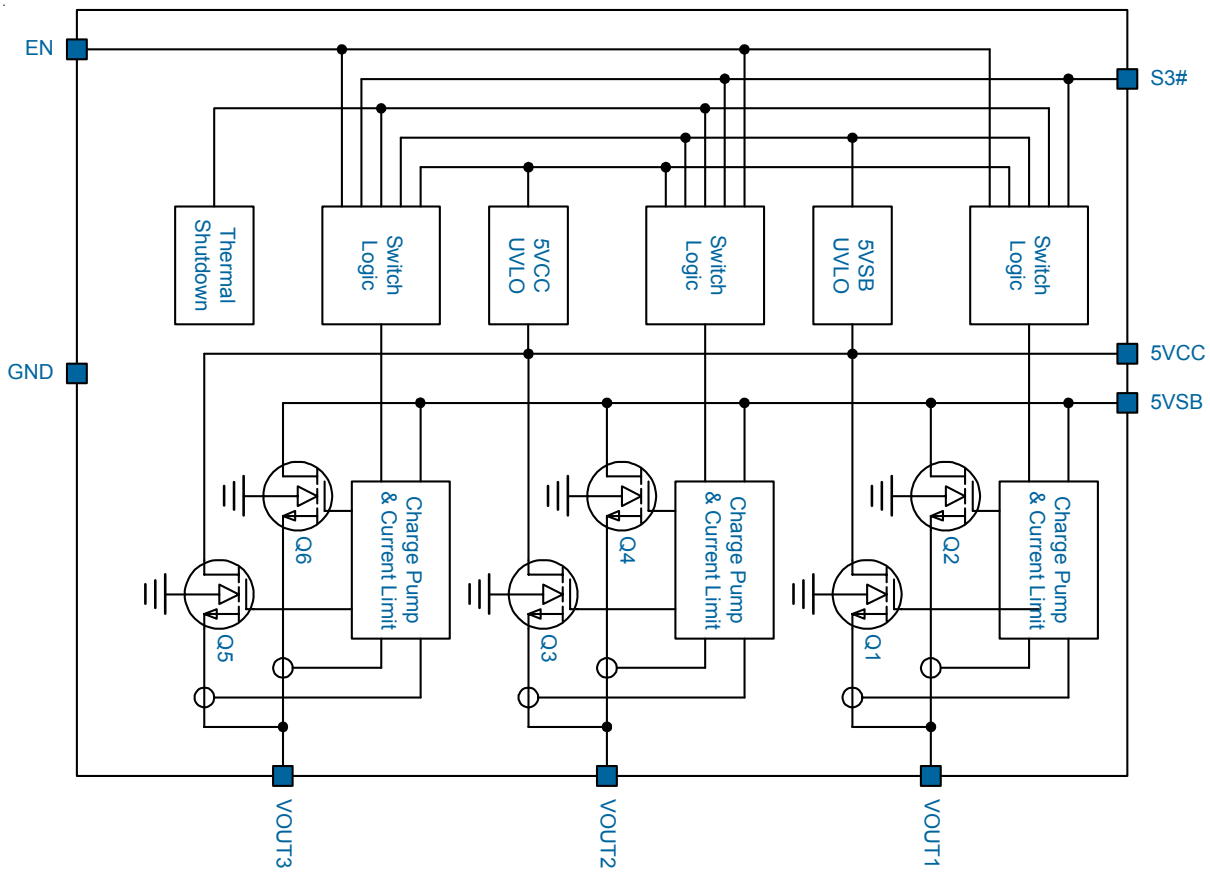




Functional Pin Description

Pin Name	Pin Function
S3#	**Sleep State Control Pin.** This pin along with the 5VCC status controls the switching configuration.
EN	**Chip Enable.** Logic high enables the output voltages.
5VCC	**Supply Input from 5VCC.** This pin is the N-Channel MOSFET Drain that supplies output current at S0/S1/S2 states and should be connected to 5VCC. Bypss this pin with a minimum 10uF capacitors to ground.
GND	**Ground.**
5VSB	**Supply Input.** This pin is the N-Channel MOSFET Drain that supplies output current at S3/S4/S5 states and should be connected to 5VSB. This pin also supplies operating current for the device. Bypass this pin with a minimum 10uF capacitor to ground.
VOUT3	**Output Voltage3.** This pin is output from N-Channel MOSFET Sources. Bypass this pin with a minimum 10uF capacitor to ground.
VOUT2	**Output Voltage2.** This pin is output from N-Channel MOSFET Sources. Bypass this pin with a minimum 10uF capacitor to ground.
VOUT1	**Output Voltage1.** This pin is output from N-Channel MOSFET Sources. Bypass this pin with a minimum 10uF capacitor to ground.

Functional Block Diagram



Functional Description

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Optimal switch logic according to S3# and 5VCC status ensures seamless output voltage transition.

When the output load exceeds the current-limit threshold or a short is present, the uP7535 asserts overcurrent protection and limits the output current to a safe level by driving the power switches into saturation mode.

Other features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present. The uP7535 is available in PSOP-8L package.

Power Switches

Each output contains two N-Channel MOSFETs Q1/Q3/Q5 and Q2/Q4/Q6 as power switches that supply output current to VOUT pins. The sources of Q1/Q3/Q5 and Q2/Q4/Q6 are connected together to the VOUT1/VOUT2/VOU3 respectively, the drain of Q1/Q3/Q5 are connected to 5VCC pins and the drain of Q2/Q4/Q6 are connected to 5VSB pin. The MOSFETs are without body diode and prevent current flows when turned off.

Q2/Q4/Q6 are 500mΩ MOSFETs with 400mA capacity and Q1/Q3/Q5 are 150mΩ MOSFETs with 1.2A capacity. The power switches are driven by internal charge pumps and controlled by S3# and 5VCC status. The uP7535 switches the output voltages to 5VSB through Q2/Q4/Q6 at S3/S4/S5 states, to 5VCC through Q1/Q3/Q5 at S0/S1/S2 states.

Charge Pumps and Drivers

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

Chip Enable and Soft Start

Pulling the EN pin lower than 0.4V disables the output voltages and reduces its quiescent current down to 1uA typically. Pulling the EN pin higher than 1.5V enables the output voltages. The uP7535 features soft start function to eliminate the inrush current into downstream and voltage droop of upstream when hot-plug-in with capacitive loads. The soft start interval is 1.3ms typically. The input current to charge up the load capacitor is proportional to its capacitance. The uP7535 current limit function may be active during the plug-in of extreme large capacitive load.

Over Current Limit

The uP7535 continuously monitors the output current for over current protection to protect the system power, the power switch, and the load from damage during output short

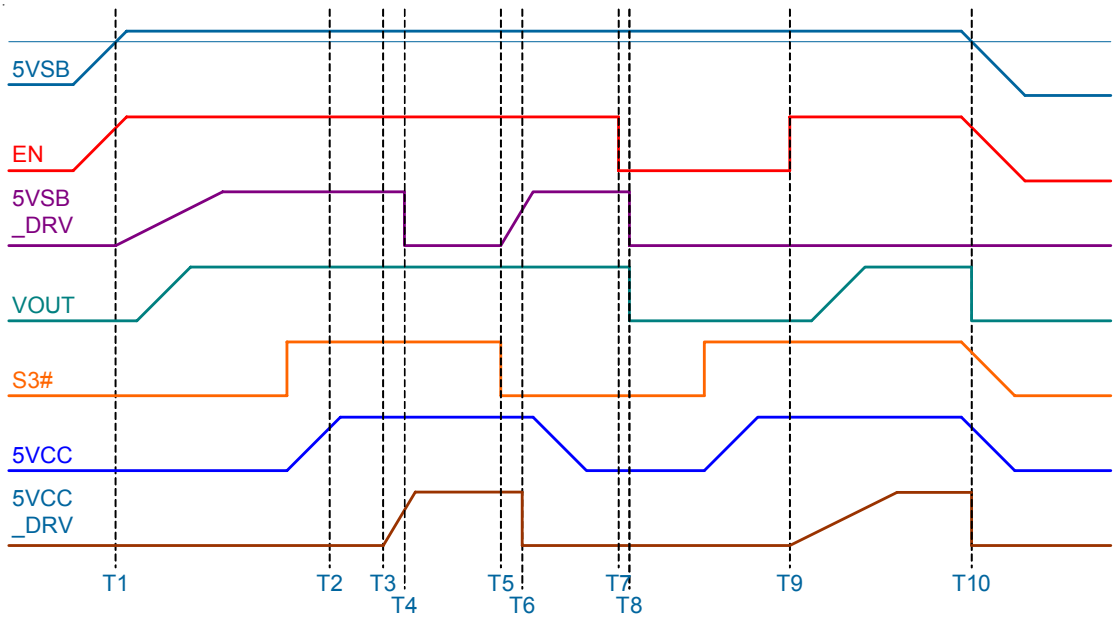


Figure 1. Typical Timing Diagram

circuit or soft start interval. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load. The current limit level is typical 1.8A when the power switch operates in linear region and is typical 1.5A in saturation region.

Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 4.3V, a control signal turns off the power switch.

Overtemperature Protection

The uP7535 continuously monitor the operating temperature of the power switch for overtemperature protection. The uP7535 asserts overtemperature and turns off the power switch to prevent the device from damage if the junction temperature rises to approximately 135^{O}C due overcurrent or short-circuit conditions. Hysteresis is built into the thermal sense, the switch will not turns back on until the device has cooled approximately 20 degrees. If the fault condition is not removed, the switch will pulse on and off as the temperature cycles between these limits.

Absolute Maximum Rating

Supply Input Voltage, 5VSB (Note 1) ---------- -0.3V to +5.7V
Supply Input Voltage, 5VSB Compliant with LPS (Limited Power Source) Requirement ---------- < 8A/100VA
Other Pins ---------- -0.3V to +5.7V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
PSOP-8L θ_{JA} ---------- 50°C/W
Power Dissipation, P_D @ T_A = 25°C
PSOP-8L ---------- 2.0W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, 5VSB ---------- +4.5V to +5.5V

Electrical Characteristics

($5V_{SB}$ = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input 5VSB						
Suppy Input Voltage Range			4.5	--	5.5	V
Supply Input Current			--	2.25	4.5	A
Under Voltage Lockout	V_{UVLO}	5VSB rising	--	4.3	4.5	V
UVLO Hysteresis			--	200	--	mV
Quiescent Current	I_Q	No load on VOUTx, S3# = 0, 5VCC = 0V	--	100	150	uA
Quiescent Current	I_Q	No load on VOUTx, S3# = 5VCC = 5V	--	200	300	uA
Shutdown Current	I_{SHDN}	EN = 0V, S3# = 5VCC = 5V.	--	1	5	uA
Supply Input 5VCC						
Supply Input Voltage Range			4.5	--	5.5	V
Supply Input Current			--	5.4	10.8	A
Under Voltage Lockout	V_{UVLO}	5VCC rising	--	4.3	4.5	V
UVLO Hysteresis			--	200	--	mV
Power Switch for 5VSB (Q2/Q4/Q6)						
N-MOSFET ON Restiance	$R_{DS(ON)}$	I_{OUT} = 300mA	--	500	750	mΩ
Reverse Leakge Current		V_{OUT} = 5.5V, 5VSB = 0V	--	--	1	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power Switches for 5VCC (Q1/Q3/Q5)						
N-MOSFET ON Resistance	$R_{DS(ON)}$	I_{OUT} = 1A	--	150	225	mΩ
Reverse Leakage Current		V_{OUT} = 5.5V, 5VCC = 0V	--	--	1	uA
Current Limit						
Current Limit Threshold for Q2/Q4/Q6		uP7535ASU8	--	0.75	1.5	A
		uP7535BSU8		0.5	1.0	A
Current Limit Threshold for Q1/Q3/Q5			--	1.8	3.6	A
Output Voltage						
Output Voltage Range			4.5	--	5.5	V
Soft Start						
Output Voltage Ramp Up Time		S3# = 0V, C_{OUT} = 10uF, No Load	--	1.3	--	ms
		S3# = 5VCC = 5V, C_{OUT} = 10uF, No Load	--	1.3	--	ms
S3# Input						
Input High	V_{IH}		1.4	--	--	V
Input Low	V_{IL}		--	--	0.4	V
S3# Low to High Delay Time	T_{LH}		--	10	--	ms
S3# High to Low Delay Time	T_{HL}		--	30	--	us
EN Input						
Input High	V_{IH}		1.4	--	--	V
Input Low	V_{IL}		--	--	0.4	V
EN Low to High Delay Time	T_{LH}		--	150	--	us
Over Temperature Protection						
Thermal Shutdown Threshold Level		By Design	--	135	--	°C
Thermal Shutdown Hysteresis		By Design	--	30	--	°C

Note 1. Stresses beyond those listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operation Condition* section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

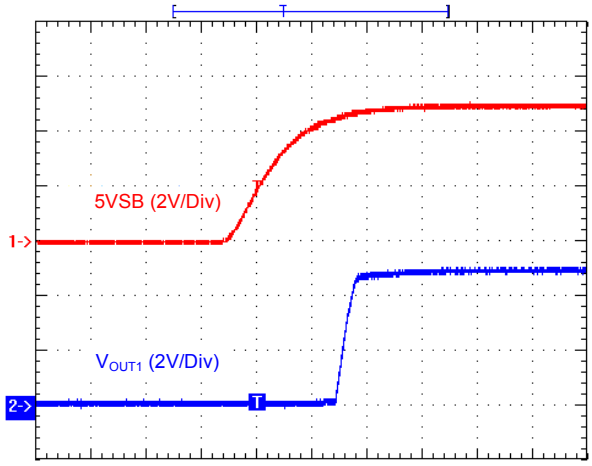
Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. These items are not tested in production, specified by design.

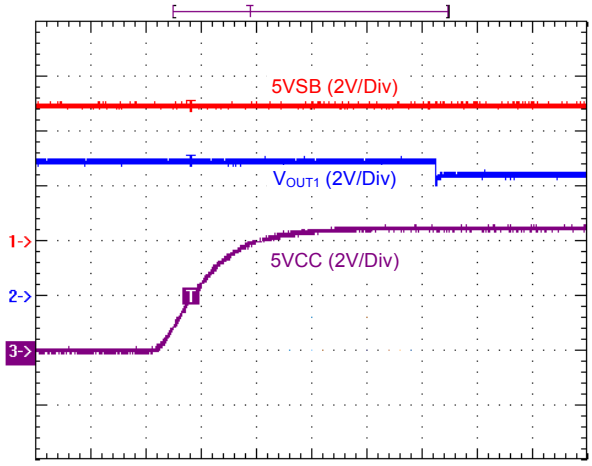
Typical Operation Characteristics

Power On by 5VSB



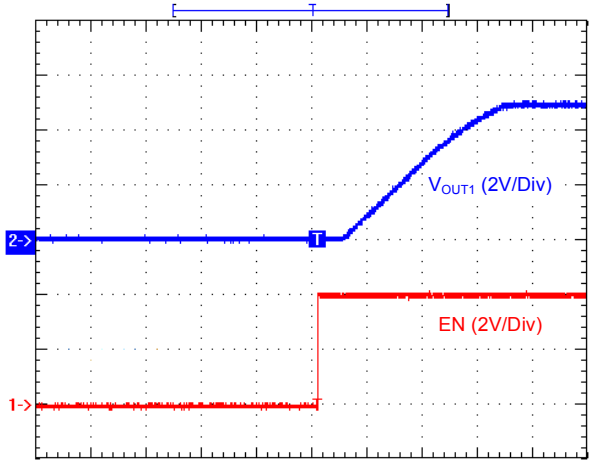
Time (4ms/Div)
C_{OUT1} = 10uF, S3# = 0V

Power On by 5VCC



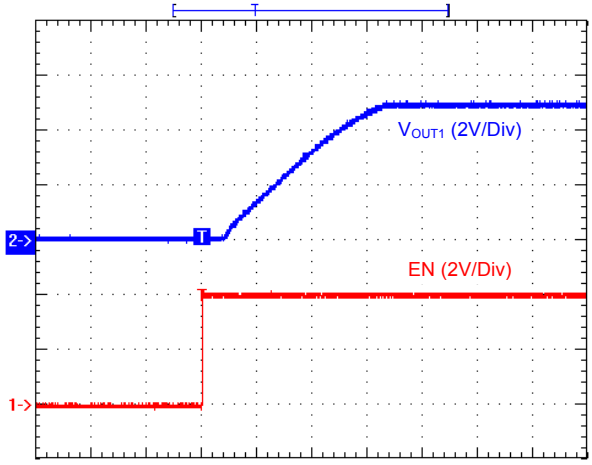
Time (4ms/Div)
C_{OUT} = 10uF, 5VSB = S3# = 5V, 5VCC = 4.5V

Turn On with S3# = Low



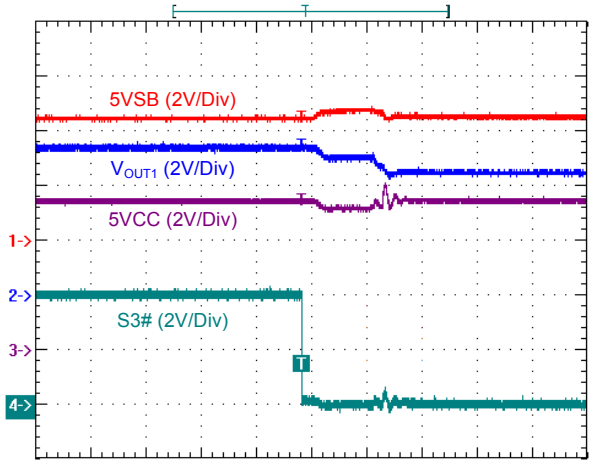
Time (400us/Div)
5VSB = 5V, C_{OUT1} = 10uF, I_{OUT1} = 100mA

Turn On with S3# = High



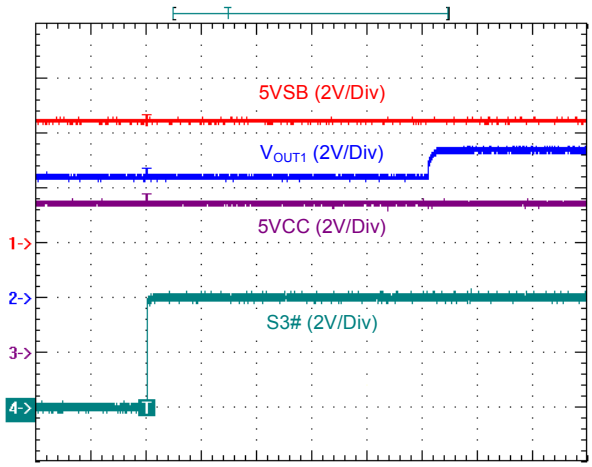
Time (400us/Div)
5VSB = 5VCC = 5V, C_{OUT1} = 10uF, I_{OUT1} = 100mA

S3# from High to Low



Time (100us/Div)
5VSB = 4.5V, 5VCC = 5.5V, C_{OUT1} = 10uF

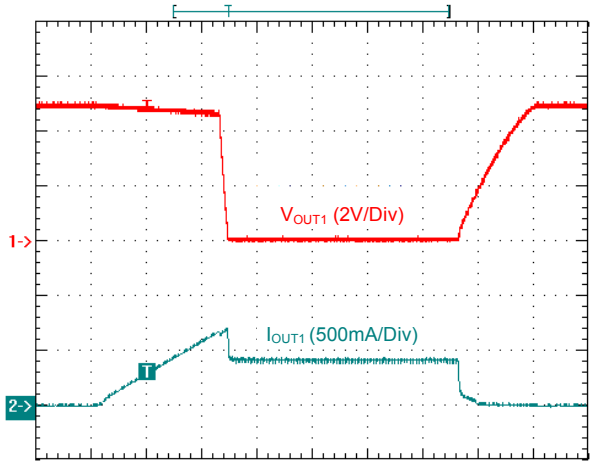
S3# from Low to High



Time (2ms/Div)
5VSB = 4.5V, 5VCC = 5.5V, C_{OUT1} = 10uF

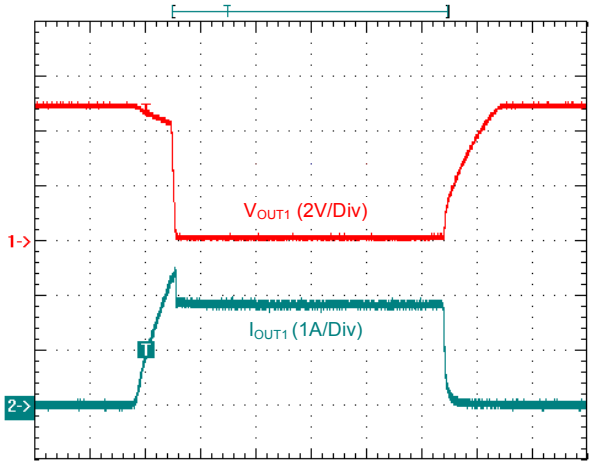
Typical Operation Characteristics

OCP for 5VSB



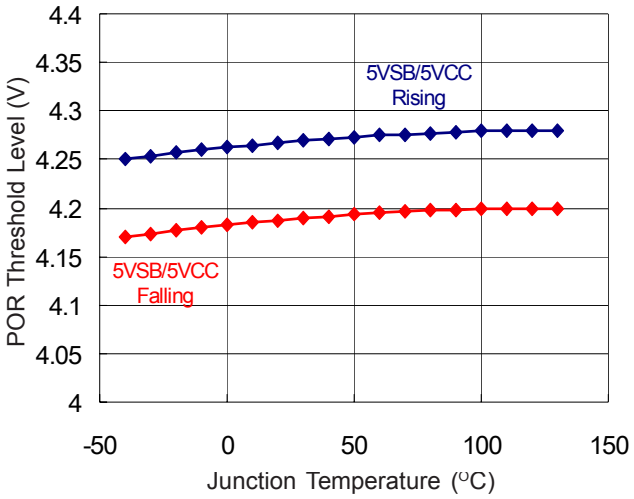
Time (1ms/Div)
C_{OUT} = 10uF, S3# = 0V

OCP for 5VCC

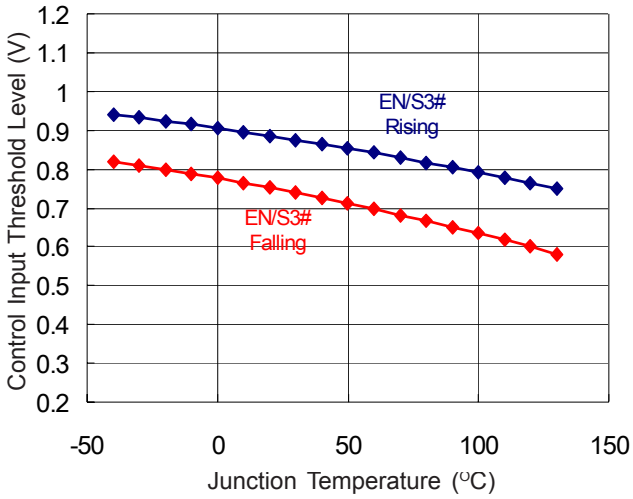


Time (1ms/Div)
C_{OUT} = 10uF, S3# = 5V

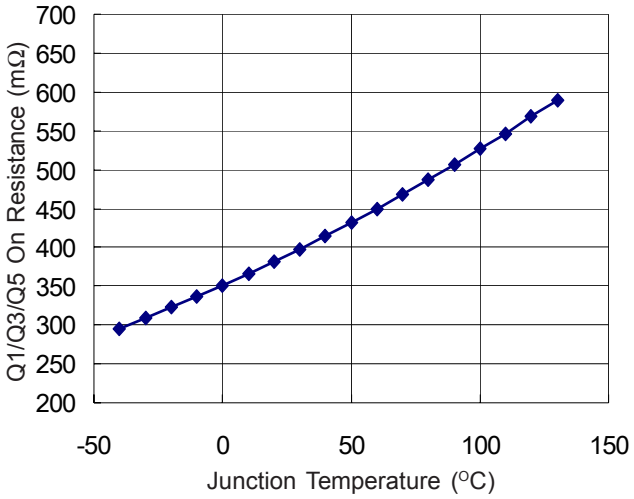
POR Threshold Level vs. Temperature



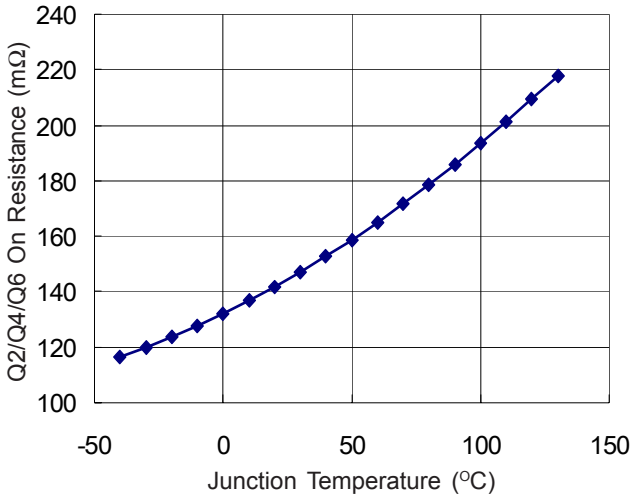
Control Input Level vs. Temperature



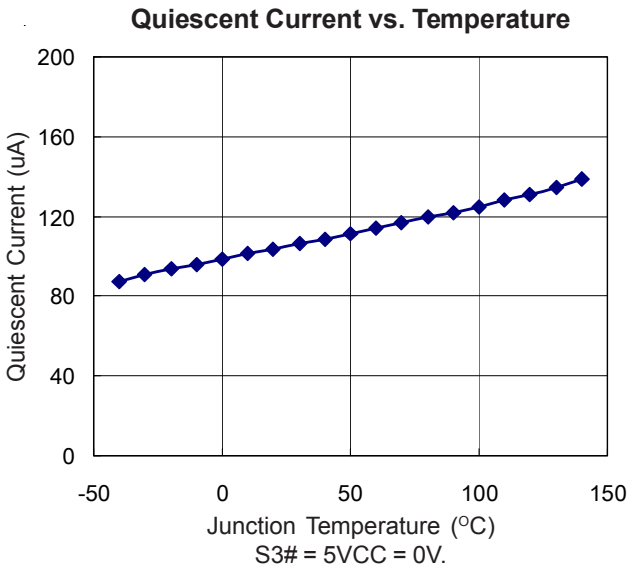
Q1/Q3/Q5 On Resistance vs. Temperature



Q2/Q4/Q6 On Resistance vs. Temperature



Typical Operation Characteristics



Application Information

The uP7535 is a current limited, dual-input triple-output power multiplexer acting as a high side switch for USB applications where heavy capacitive loads and short-circuits are likely to be encountered. It switches output voltages to 5VSB at S3/S4/S5 states with 600mΩ switch and 200mA capacity; to 5VCC at S0/S1/S2 states with 180mΩ switch and 1.5A capacity. The outputs can be parallel to provide totally 3.0A output current at S0/S1/S2 states.

Optimal switch logic according to S3# and 5VCC status ensures seamless output voltage transition.

When the output load exceeds the current-limit threshold or a short is present, the uP7535 asserts overcurrent protection and limits the output current to a safe level by driving the power switches into saturation mode.

Other features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present. The uP7535 is available in PSOP-8L package.

Input and output capacitors

Bypass the supply input pins with a single 4.7uF capacitor as close as possible to the uP7535. A 4.7uF output capacitor at the output pin is recommended even much larger output capacitors are already available at the output of the uP7535, especially if the output capacitors are more than 2 inches away on the PCB. The inrush current to charge the output capacitors is calculated as:

$$I_{IN} = C_{OUT} \times \frac{V_{OUT}}{T_{SS}} \text{ (A)}$$

Special care should be paid to large output capacitor applications. Take C_{OUT} = 1000uF as example, the inrush current is I_{IN} = 1000uF x 5V / 1.3ms = 3.8A. This is higher than the current limit threshold of Q1/Q3/Q5 and Q2/Q4/Q6. In this case, the output voltage ramp up time is controlled by the current limit function of Q1/Q3/Q5 and Q2/Q4/Q6 as shown in Figure 1. Note that output voltage ramping up slew rates are different due to different outupt capacitors.

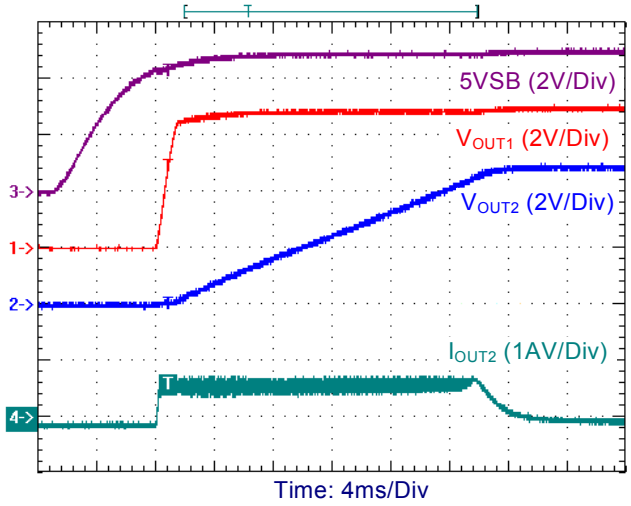


Figure 1. Turn on into 5VSB C_{OUT2} = 1500uF, C_{OUT1} = 10uF.

The output voltage undergoes an abrupt drop when a device with large input capacitors is hot plugged into the output of uP7535 as shown in Figure 2, where a device with 1500uF is hot plugged into uP7535 output with 470uF output capacitor. The output voltage ramp up time is controlled by the current limit level.

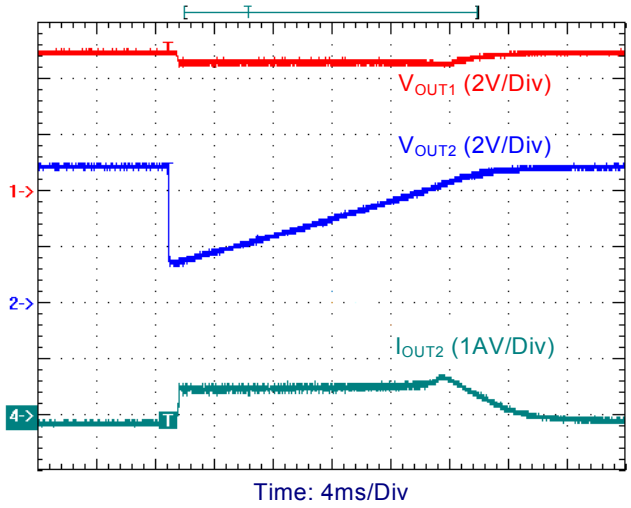


Figure 2. Hot plug application with S3# = 0V.

Thermal Consideration

Temperature effect should be well considered when dealing with voltage drop and power dissipation. The maximum $R_{DS(ON)}$ of the power switch is 160mΩ of Q2 under 25°C junction temperature. If the device is expected to operate at 125°C junction temperature, the $R_{DS(ON)}$ of Q2 will become

160mΩ * (1 + (125°C - 25°C) * 0.5%/°C) = 240mΩ

where 0.5%/°C is the approximated temperature coefficient of the $R_{DS(ON)}$.

If the maximum load current is expected to be 1.2A, the maximum voltage will become

1.2A * 240mΩ = 288mV

This in turn will cause power dissipation as

1.2A * 288mV = 346mW

The temperature raise is calculated as

346mW * 50°C/W = 17°C

The junction temperature is calculated as T_A + 17°C, where T_A is the expected maximum ambient temperature. A few iterations are required until get final solutions.

The thermal resistance θ_{JA} highly depends on the PCB design. Copper plane under the exposed pad is an effective heatsink and is useful for improving thermal conductivity. Figure 3 show the relationship between thermal resistance θ_{JA} vs. copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at T_A = 25°C. A 50mm² copper plane reduces θ_{JA} from 75°C/W to 50°C/W and increases maximum power dissipation from 1.33W to 2W.

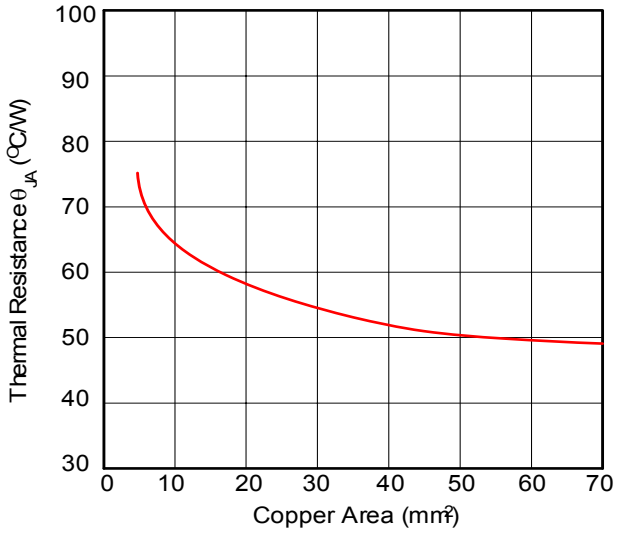
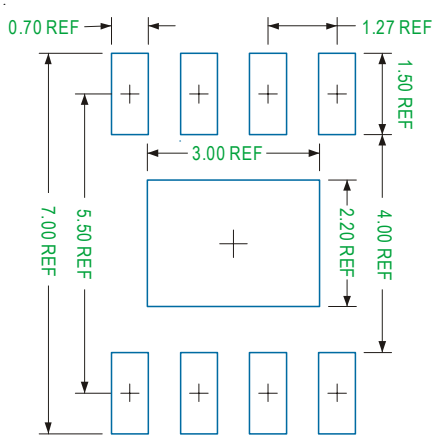


Figure 3. Thermal Resistance è$_{JA}$ vs. Copper Area

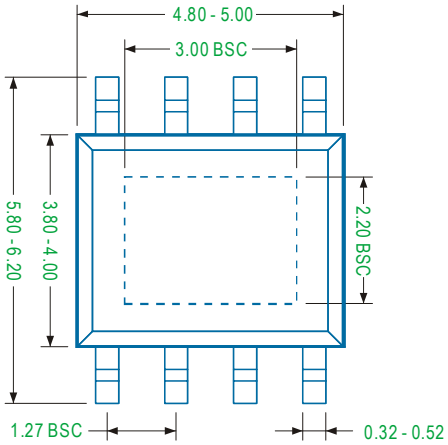
PCB Layout Consideration

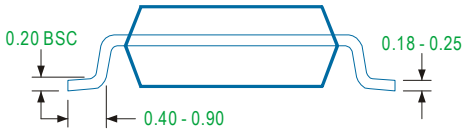
- Place the uP7535 as close to the USB connector as possible to minimize the parasitic elements.
- Place local bypass capacitors as closed as possible to the 5VSB and 5VCC pins. Use short and wide traces to minimize parasitic resistance and inductance.
- The exposed pad should be soldered on GND plane with maximum area and with multiple vias to inner layer of ground place for improved thermal performance.
- Keep the power trace short and wide to minimize the parasitic resistance along the trace.

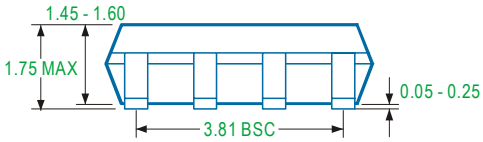
Package Information



Recommended Solder Pad Layout







Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.