

12 Phase Synchronous-Rectified Buck Controller for Next Generation CPU Core Power

General Description

The uP6208 12-phase PWM control IC provides a precision voltage regulation system for advanced microprocessors. It can work with Intel VR11/VR10 and AMD 5/6-bit VID table. The controller also includes programmable no-load offset and active voltage positioning functions to adjust the output voltage as a function of the load current, so it is optimally positioned for a load current transient. Continuous DCR current sensing is used for load line programming and channel current balance. The uP6208 also provides accurate and reliable over current protection, over voltage protection and a delayed power good output. The uP6208 includes an I²C interface, allowing the controller to communicate with other devices over an I²C bus. Signals sent over this bus can command the uP6208 to adjust output voltage, switching frequency and operating phase number in different load current state.

Ordering Information

Order Number	Package Type	Remark
uP6208ALAM	LQFP7x7 - 64L	

Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

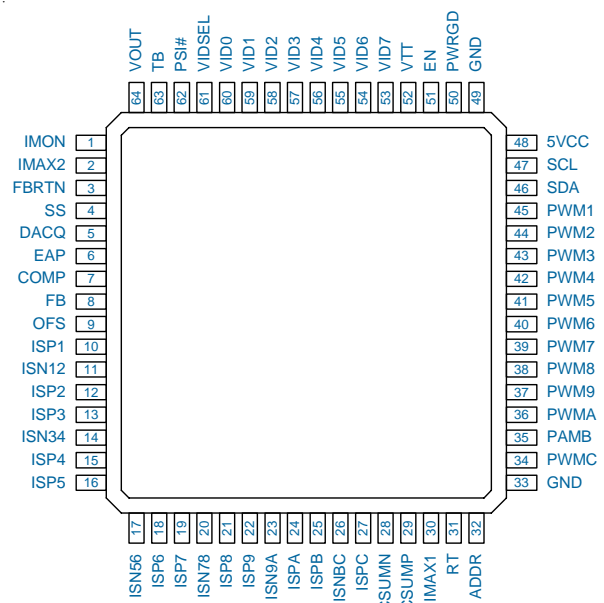
Applications

- Desktop PC Core Power Supplies

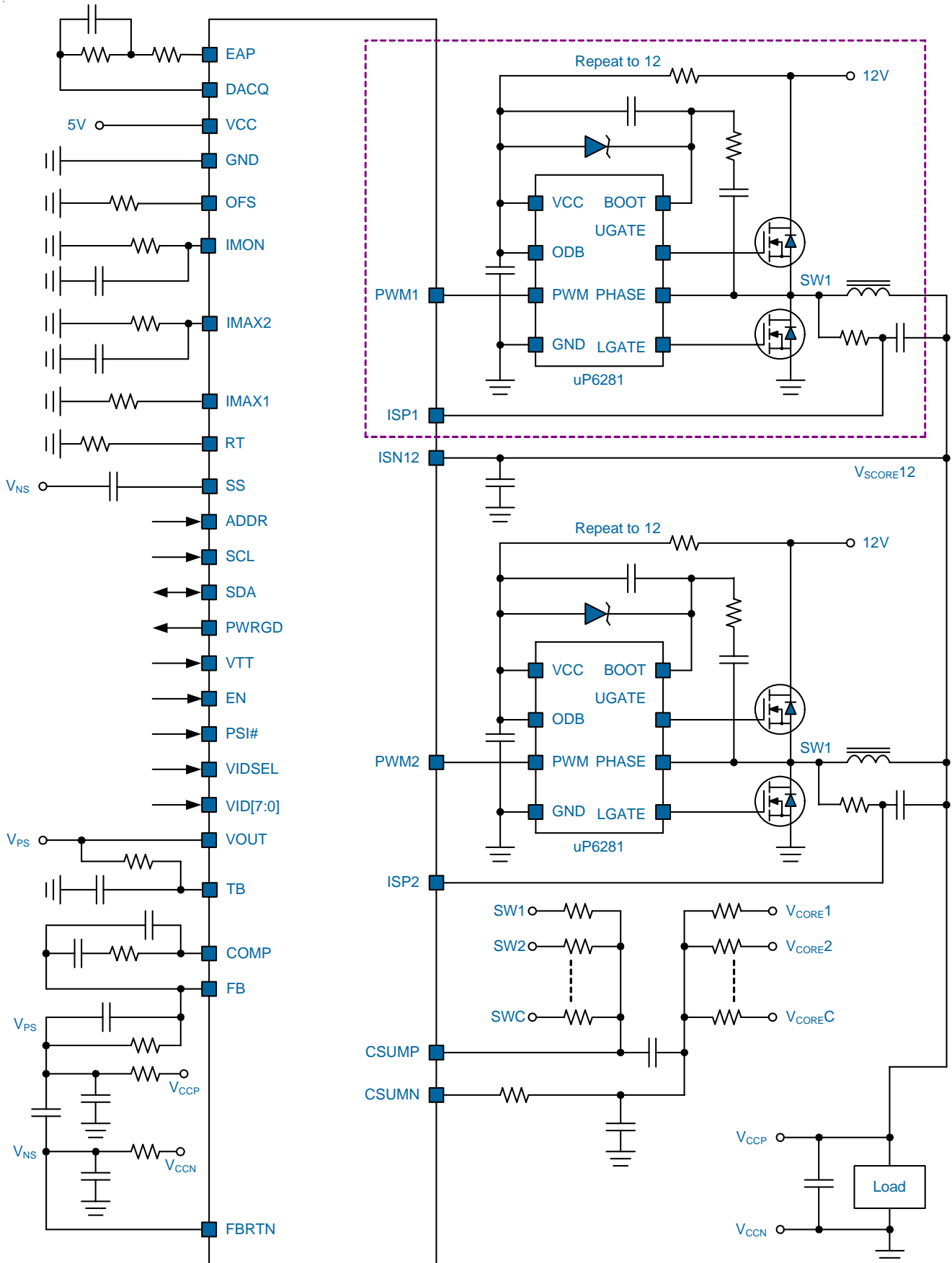
Features

- Selectable 12/8-phase Operation by Hardware Setting
- Precision Core Voltage Regulation
- Differential Remote Voltage Sensing
- Adjustable Reference Voltage Offset
- Continuous Inductor DCR Current Sensing
- I²C Interface
 - Voltage Adjustment
 - Switching Frequency Adjustment
 - Operating Phase Number Adjustment
- Microprocessor VID Inputs
 - 8-Bit DAC
 - Selectable between Intel VR11/10 and AMD
 - 5/6-bit DAC Tables
- Over-current Protection
- Over-voltage Protection
- Soft-Start
- Selectable Operation Frequency from 100kHz to 1.5MHz per Phase

Pin Configuration



Typical Application Circuit



Functional Pin Description

No.	Name	Pin Function
1	IMON	Output Current Indication. Analog output representing total load current. Output current of IMON is proportional to total load current. Connect a resistor between IMON and GND then the voltage of IMON is proportional to total load current. A capacitor may be connected between IMON and GND also to adjust the response time of IMON. IMON voltage is clamped to be lower than VTT.
2	IMAX2	Total Load Current OCP Setting Input. Output current of IMAX2 is proportional to total load current. Connect a resistor between IMAX2 and GND then the voltage of IMAX2 is proportional to total load current. If IMAX2 voltage is higher than 1.2V, OCP will be triggered. Resistor between IMAX2 and GND can adjust OCP level. Capacitor between IMAX2 and GND can filter load current ripple to avoid OCP mis-trigger.
3	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
4	SS	Soft Start. A capacitor connected between SS and GND sets the soft start ramp-up time. Pull this pin to GND will shut down the controller.
5	DACQ	DAC Output.
6	EAP	Non-Inverting Input of the Error Amplifier. A resistor between EAP and the DACQ sets the load line.
7	COMP	Compensation Output. Error amplifier output and compensation point.
8	FB	Feedback Pin. Feedback input. Error amplifier inverting input for remote sensing of the output voltage. FB, COMP and output voltage are tied together through external R-C networks to compensate the regulator.
9	OFS	Zero Current Offset. Connect a resistor between OFS and GND to generate an offset voltage across the resistor between FB and output voltage. The offset current is generated via the external resistor and a precision internal voltage. For no offset, the OFS pin should be left unconnected.
10	ISP1	Non-inverting Input of the Current Sensing GM Amplifier for Phase 1. The pin is used for differentially sensing channel 1 output currents. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
11	ISN12	Inverting Input of the Current Sensing GM Amplifier for Phase1 and 2. Common inverting input of channel 1 and channel 2 current sensing. Tie the pin to the midway of VCORE side of channel 1 and channel 2 sensing capacitor. The VCORE side of channel 1 inductor and channel 2 inductor should be placed as close as possible. The resistance between ISN12 to the VCORE side of inductor 1 and inductor 2 should be as equal as possible. PCB trace resistance should be taken into consideration.
12	ISP2	Non-inverting Input of the Current Sensing GM Amplifier for Phase 2. The pin is used for differentially sensing channel 2 output currents. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
13	ISP3	Non-inverting Input of the Current Sensing GM Amplifier for Phase 3. The pin is used for differentially sensing channel 3 output currents. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
14	ISN34	Inverting Input of the Current Sensing GM Amplifier for Phase 3 and 4. Function is the same as ISN12 except the respective channels are 3 and 4.

Functional Pin Description

No.	Name	Pin Function
15	ISP4	Non-inverting Input of the Current Sensing GM Amplifier for Phase 4. The pin is used for differentially sensing channel 4 output currents. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
16	ISP5	Non-inverting Input of the Current Sensing GM Amplifier for Phase 5. The pin is used for differentially sensing channel 5 output currents. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
17	ISN56	Inverting Input of the Current Sensing GM Amplifier for Phase 5 and 6. Function is the same as ISN12 except the respective channels are 5 and 6.
18	ISP6	Non-inverting Input of the Current Sensing GM Amplifier for Phase 6. The pin is used for differentially sensing channel 6 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
19	ISP7	Non-inverting Input of the Current Sensing GM Amplifier for Phase 7. The pin is used for differentially sensing channel 7 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
20	ISN78	Inverting Input of the Current Sensing GM Amplifier for Phase 7 and 8. Function is the same as ISN12 except the respective channels are 7 and 8.
21	ISP8	Non-inverting Input of the Current Sensing GM Amplifier for Phase 8. The pin is used for differentially sensing channel 8 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
22	ISP9	Non-inverting Input of the Current Sensing GM Amplifier for Phase 9. The pin is used for differentially sensing channel 9 output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
23	ISN9A	Inverting Input of the Current Sensing GM Amplifier for Phase 9 and A. Function is the same as ISN12 except the respective channels are 9 and A. Besides, connecting ISN9A to VCC will program the controller for 8-phase operation.
24	ISPA	Non-inverting Input of the Current Sensing GM Amplifier for Phase A. The pin is used for differentially sensing channel A output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
25	ISPB	Non-inverting Input of the Current Sensing GM Amplifier for Phase B. The pin is used for differentially sensing channel B output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.
26	ISNBC	Inverting Input of the Current Sensing GM Amplifier for Phase B and C. Function is the same as ISN12 except the respective channels are B and C.
27	ISPC	Non-inverting Input of the Current Sensing GM Amplifier for Phase C. The pin is used for differentially sensing channel C output current. The sensed current is used for channel current balancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor.

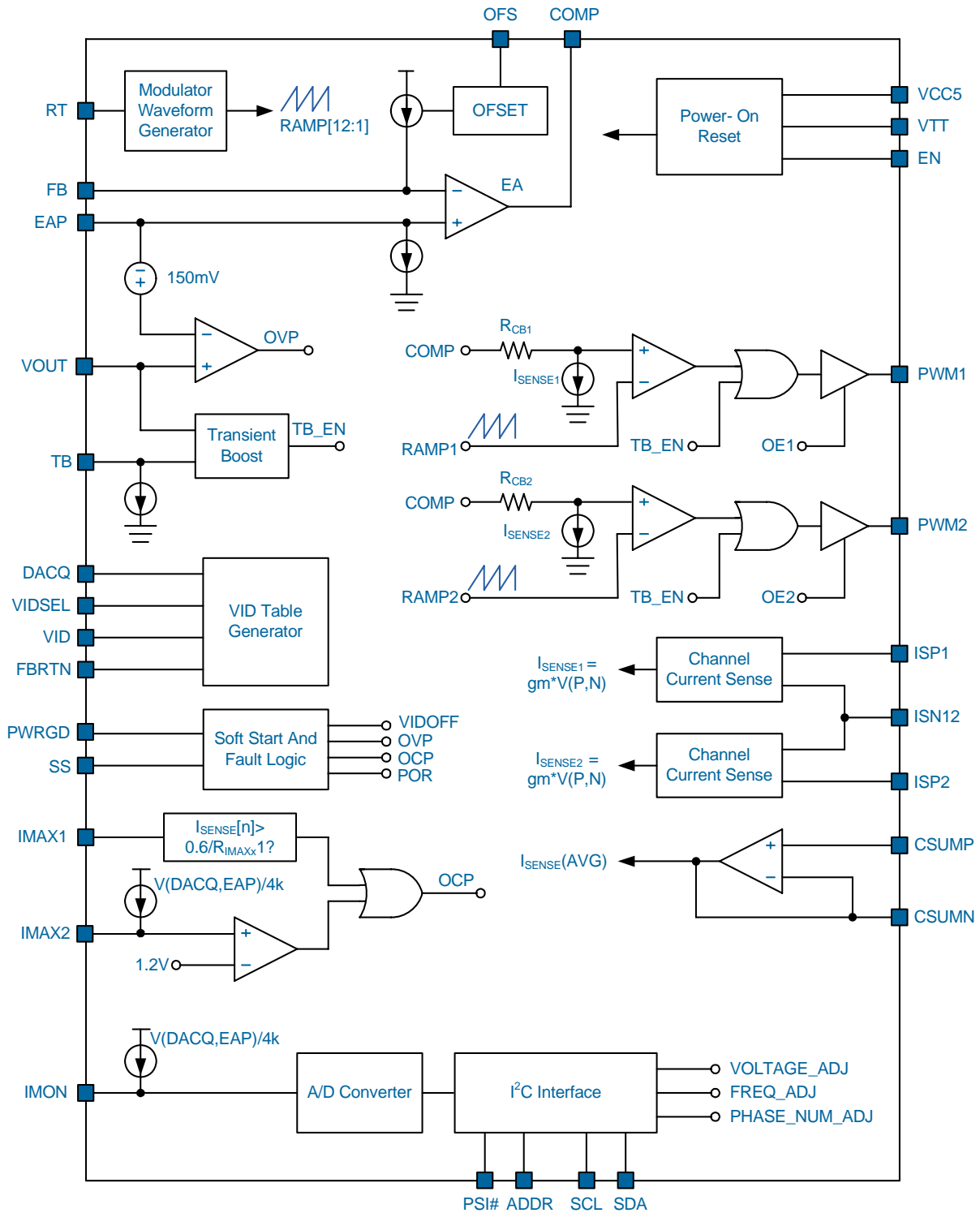
Functional Pin Description

No.	Name	Pin Function
28	CSUMN	Inverting Input of the Current Sensing Amplifier for Total Current. Total load current sense inverting input. Connect a resistor between CSUMN and the VCORE side of all output inductors. The selected VCORE point should have equal resistance to the VCORE side of all inductors. PCB trace resistance should be taken into consideration.
29	CSUMP	Non-inverting Input of the Current Sensing GM Amplifier for Total Current. Channel current averaging node. Resistors from each switch node to this pin average the inductor currents on the capacitor between CSUMP and VCORE.
30	IMAX1	Connect a resistor between IMAX1 and GND to generate a reference current for channel current OCP. The reference current is generated via the external resistor and a precision internal voltage.
31	RT	Switching Frequency Programming. Connect a resistor from this pin to GND to set the switching frequency.
32	ADDR	Address Selection for I²C Interface. Connect a voltage divider from VCC to ADDR to GND to set the I ² C address. The pin selects which of the three 8-bit Slave I ² C addresses will be used by the controller. Connecting this pin to GND will choose address (1000_110x). Connecting this pin to VCC will choose address (1000_110x). Connecting this pin to VCC/2 will choose address (1000_101x).
33	GND	Ground. GND is the bias and reference ground for the IC.
34	PWMC	PWM Output for Phase C. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
35	PWMB	PWM Output for Phase B. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
36	PWMA	PWM Output for Phase A. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
37	PWM9	PWM Output for Phase 9. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
38	PWM8	PWM Output for Phase 8. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
39	PWM7	PWM Output for Phase 7. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
40	PWM6	PWM Output for Phase 6. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
41	PWM5	PWM Output for Phase 5. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
42	PWM4	PWM Output for Phase 4. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
43	PWM3	PWM Output for Phase 3. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
44	PWM2	PWM Output for Phase 2. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.
45	PWM1	PWM Output for Phase 1. Pulse width modulation output. Each output is connected to the input of external MOSFET driver such as the uP6281.

Functional Pin Description

No.	Name	Pin Function
46	SDA	Data for I²C Interface. Connect SDA to the bidirectional data line of the I ² C bus.
47	SCL	Clock for I²C Interface. Connect SCL to the clock signal for the I ² C bus.
48	5VCC	Supply Input fo the IC. Connect this pin to a 5V voltage source with RC filter. Voltage power supply of the IC. Connect this pin to a 5V supply and decouple using a 0.1uF ceramic capacitor.
49	GND	Ground.
50	PWRGD	Power Good Indication. This open-drain output is set to high impedance. Power good output. Open drain output that indicates the soft start process is complete and no fault happens.
51	EN	Chip Enable. Pulling low this pin disables the uP6208. Enable input of the controller. Voltage of this pin higher than 1.1V enables the controller. Lower than 1.0V disables the controller. It is recommended to use this pin to detect whether MOSFET driver power supply is ready.
52	VTT	Enable input of the controller. Voltage of this pin higher than 0.85V enables the controller. Lower than 0.75V disables the controller. It is recommended to use this pin to detect whether VTT power is ready.
53	VID7	Bit 7 of DAC Input. Voltage ID DAC inputs.
54	VID6	Bit 6 of DAC Input. Voltage ID DAC inputs.
55	VID5	Bit 5 of DAC Input. Voltage ID DAC inputs.
56	VID4	Bit 4 of DAC Input. Voltage ID DAC inputs.
57	VID3	Bit 3 of DAC Input. Voltage ID DAC inputs.
58	VID2	Bit 2 of DAC Input. Voltage ID DAC inputs.
59	VID1	Bit 1 of DAC Input. Voltage ID DAC inputs.
60	VID0	Bit 0 of DAC Input. Voltage ID DAC inputs.
61	VIDSEL	VID Table Selection. VR select input. Connect this pin to VTT(1.2V) to select the VR11 DAC table. Ground this pin to select the VR10 DAC table. Connect this pin to VCC(5V) to select AMD DAC table.
62	PS#	Power state indicator input from CPU. PS# is an active low signal, asserted when the CPU current is in the range of ~<25A. When PS# goes low, controller will reduce the operating phase number to improve light load efficiency.
63	TB	Transient Boost. This pin along with the VOUT pin set the transient boost behavior. Transient boost. This pin along with the VOUT pin set the transient boost behavior.
64	VOUT	Output voltage detection input. Voltage of this pin is used for setting transient boost behavior and OVP detection.

Functional Block Diagram



Functional Description

The uP6208 is a 12/8-phase, multimode (voltage control, current balance control, loadline control), fixed frequency PWM synchronous buck power converters. The internal VIDDAC is designed for Intel VR11/VR10 and AMD 5/6-bit interface.

Power Ready Detection

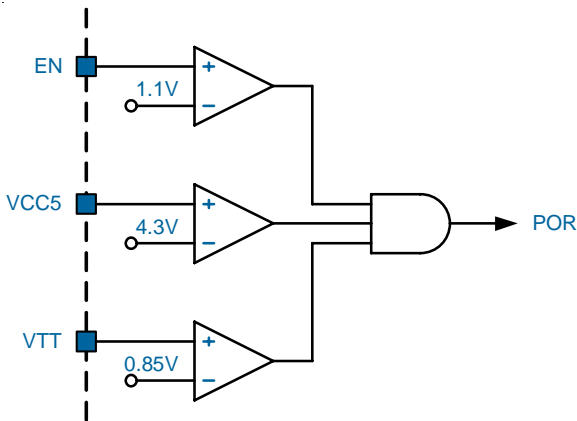


Figure1. Circuit for Power Ready Detection

During start-up, the uP6208 will detect V_{CC5} , V_{TT} and EN. When $V_{CC5} > 4.3V$, $V_{TT} > 0.85V$ and $EN > 0.85V$, POR (Power On Reset) will go high. POR is the internal signal to indicate all voltage powers are ready to let the uP6208 and the companioned MOSFET drivers to work properly. When POR = Low, the uP6208 will try to turn off both high side and low side MOSFETs.

Phase Detection

The number of operational phases is determined by the internal circuitry that monitors the ISN9A voltages during start up. Normally, the uP6208 operates as a 12-phase PWM controller. Pull ISN9A to V_{CC5} programs 8-phase operation. The uP6208 detects the voltage of ISN9A at POR rising edge. At the rising edge, the uP6208 detects whether the voltage of ISN9A is higher than $V_{CC5} - 1V$ to decide how many phases should be active. Phase detection is only active during start up. When POR = High, the number of operational phases is determined and latched.

Phase Switching Frequency

The phase switching frequency of the the uP6208 is set by an external resistor connected between RT pin and GND. The frequency follows the graph in Figure 2.



Figure2. R_{RT} vs Phase Switching Frequency

V_{DAC} Generator

The uP6208 builds a precise bandgap reference circuit inside. The output voltage of bandgap reference is 2.1V referred to FBRTN. In Figure 3, the uP6208 uses plural resistors to generate precise reference voltages ranging from 0.5V to 2.1V. All the voltages connect to a multiplexer (MUX). According to the VID inputs and I²C command, multiplexer outputs the selected voltage, V_{DAC} . Please be careful that all the voltage values in Figure 3 are referred to FBRTN.

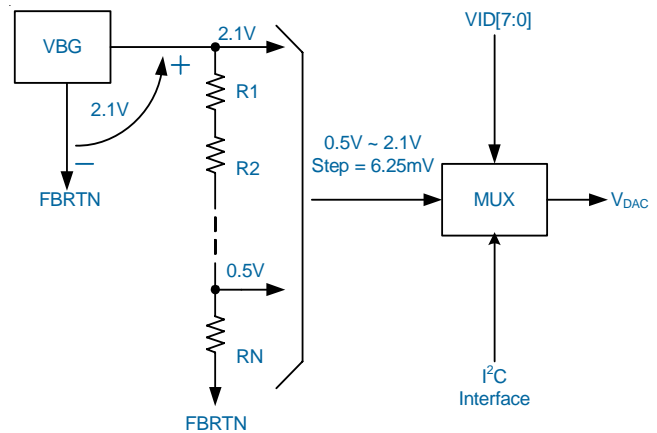


Figure3. V_{DAC} Generator Circuit

Soft Start

Output current of OPSS (I_{SS}) is limited within +/- 32uA (normal state) or +/- 320uA (VID OTF).

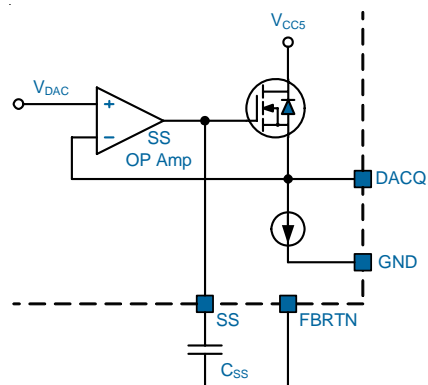


Figure 4. Circuit for Soft Start and Dynamic VID.

The V_{OUT} start-up time is set by a capacitor from the SS pin to FBRTN. In power_on_reset state (POR = Low), the SS pin is held at GND. After power_on_reset state (POR = High) and an extra delay 1600uS, V_{SS} and V_{EAP} begin to

Functional Description

rise till $V_{EAP} = V_{BOOT}$. When $V_{EAP} = V_{BOOT}$, the uP6208 stays in this state for 800uS waiting for valid VID code sent by CPU. After receiving the valid VID code, V_{OUT} continues ramping up or down to the voltage specified by VID code. The typical soft start waveform is shown in Figure 5.

connects FB pin and the positive remote sense pin of the CPU V_{CCP} . FBRTN pin connects to the negative remote sense pin of CPU V_{CCN} directly. The error amplifier compares $EAP (= DACQ - I_{SENSE} \times R_{LL})$ with the V_{FB} to regulate the output voltage.

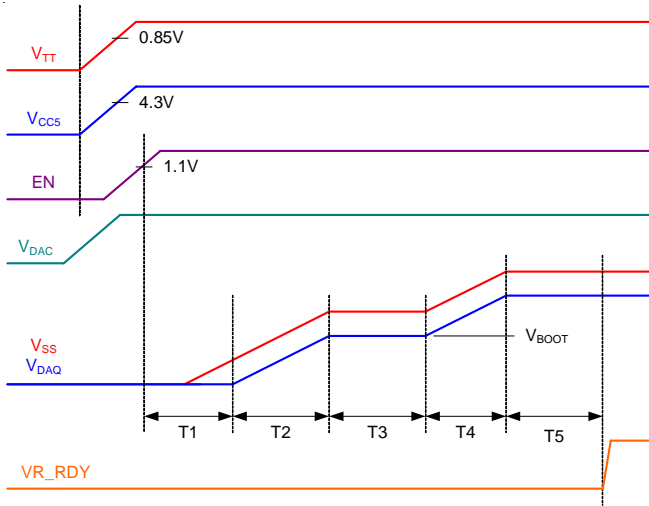


Figure 5. Soft Start Waveforms.

V_{OUT} will trace V_{EAP} which is the non-inverting input of error amplifier. T1 is the delay time from power_on_reset state to the beginning of V_{OUT} rising.

$$T1 \sim 1600\mu s + 0.7V \times C_{SS} / 32\mu A \quad (1)$$

T2 is the soft start time from $V_{OUT} = 0$ to $V_{OUT} = V_{BOOT}$

$$T2 \sim V_{BOOT} \times C_{SS} / 32\mu A \quad (2)$$

T3 is the dwelling time for $V_{OUT} = V_{BOOT}$. T3 $\sim 800\mu s$. T4 is the soft start time from $V_{OUT} = V_{BOOT}$ to $V_{OUT} = V_{VID}$.

$$T4 \sim |V_{VID} - V_{BOOT}| \times C_{SS} / 32\mu A \quad (3)$$

T5 is the power good delay time, T5 $\sim 1600\mu s$.

Dynamic VID

The uP6208 can accept VID input changing while the controller is running. This allows the output voltage V_{OUT} to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF may occur under either light or heavy load conditions. This change can be positive or negative. During VID OTF, V_{DAC} is a staircase waveform. In the uP6208, C_{SS} is also used to filter the V_{DAC} . By properly selecting C_{SS} , VID OTF performance can be improved.

Output Voltage Differential Sensing

The uP6208 uses differential sensing by a high gain low offset error amplifier as shown in Figure 6. The CPU voltage is sensed between the FB and FBRTN pins. A resistor R_{FB}

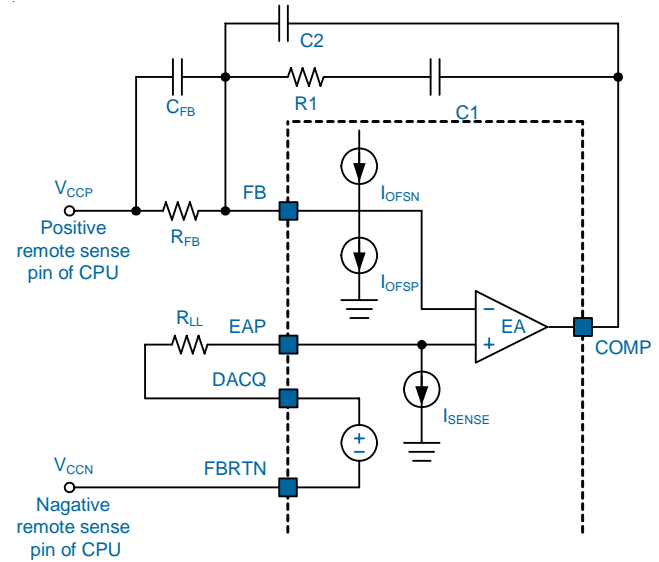


Figure 6. Circuit for V_{OUT} Differential Sensing and No Load Offset

No Load Offset

In Figure 6, I_{OFSN} and I_{OFSP} are used to generate no-load offset. Either I_{OFSN} or I_{OFSP} is active during normal operation. Connect a resistor R_{OFS} between OFS pin and GND to generate negative no-load offset voltage V_{OFSN} .

$$V_{OFSN} = I_{OFSN} \times R_{FB} = 1.2 \times R_{FB} / R_{OFS} \quad (4)$$

Connect a resistor R_{OFS} between OFS pin to V_{CC5} to generate positive no-load offset voltage V_{OFSP} .

$$V_{OFSP} = I_{OFSP} \times R_{FB} = 1.6 \times R_{FB} / R_{OFS} \quad (5)$$

Load Transient Boost

In steady state, the voltage at VOUT pin V_{VOUT} is higher than V_{TB} by the voltage of $I_{TB} \times R_{TB}$. While a load step transient from light load to heavy load could cause V_{VOUT} temporarily lower than V_{TB} . The uP6208 detects load transient by comparing V_{VOUT} and V_{TB} . If V_{VOUT} drops below V_{TB} . The quick response indicator TB_EN rises up. When TB_EN = High, the uP6208 turns on all high side MOSFETs and turn off all low side MOSFETs. The sensitivity of this transient boost behavior can be adjusted by the values of C_{TB} and R_{TB} . Smaller R_{TB} will make transient boost behavior

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easier to be triggered while larger C_{FB} will make transient boost behavior sustain longer. Figure 7 is the circuit and typical waveforms.

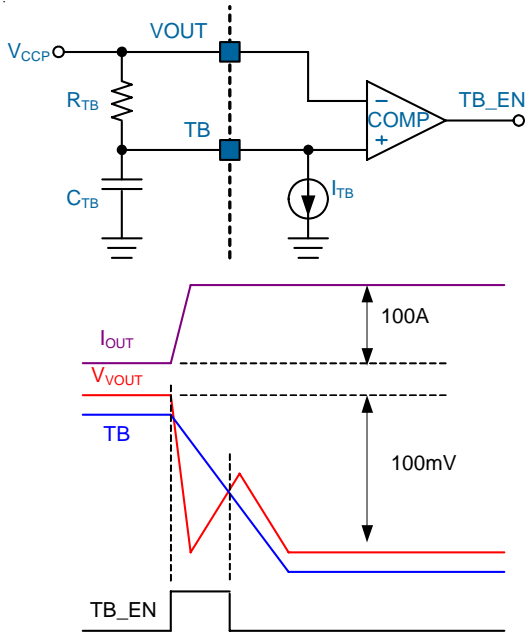


Figure 7. Load Transient Boost

Total Load Current Sensing

The uP6208 provides low input offset current sense amplifier (CSA) to monitor the total load current flowing through inductor as shown in Figure 8. Output current of CSA (I_{SUM}) is used for active voltage positioning (AVP), load current monitoring and over current protection. In this inductor current sensing topology, R_{SW} and C_{SUM} must be selected according to the equation below:

$$L/DCR = k \times R_{SW} \times C_{SUM} / 12 \tag{6}$$

Theoretically, k should be equal to 1 to sense the instantaneous total load current. But in real application usually 1.2 ~ 1.8 is better for transient response.

$$I_{SUM} = I_{L,TOTAL} \times DCR / R_{SUM} \tag{7}$$

In order to minimize to sensing error induced by PCB trace, the PCB trace resistance between V_{CORE12} and inductor 1 should be as equal as possible to the PCB trace resistance between V_{CORE12} and inductor 2. Besides, placement of inductor 1 and inductor 2 should be as close as possible. All other channels should follow these rules also.

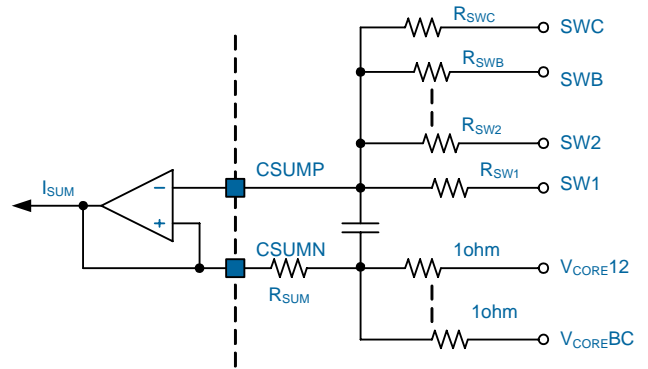


Figure 8. Total Load Current Sensing.

Loadline

I_{SENSE} in Figure 6 is a mirror of I_{SUM} in Figure 8. I_{SENSE} flows through R_{LL} and makes V_{EAP} equal to $V_{DACQ} - I_{SENSE} \times R_{LL}$. In steady state, output voltage is equal to V_{EAP} . Thus, the output voltage decreasing linearly with I_{OUT} is obtained. The loadline is defined as

$$LL(\text{loadline}) = \Delta V_{OUT} / \Delta I_{OUT} = DCR \times R_{LL} / R_{CSN} \tag{8}$$

Channel Current Sensing

The uP6208 provides low input offset voltage control current source (VCCS) to sense the individual inductor current as shown in Figure 9. Output current of VCCS ($I_{SENSE}[N]$) is used for channel current balance. Unlike prior circuits designed by many other manufacturers that use instantaneous inductor current for both AVP and channel current balance, the uP6208 can use different RC time constant for channel current balance and AVP. Using instantaneous current for AVP is necessary to get good transient response while using instantaneous current for channel current balance is not necessary and may deteriorate transient response and loop stability. It is recommended to select larger RC time constant for channel current balance. That is

$$L/DCR = k \times R_S \times C_S, k = 2 \sim 10 \tag{9}$$

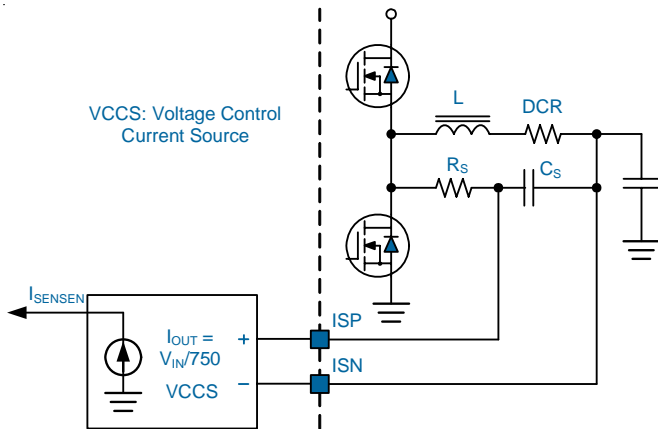


Figure 9. Channel Current Sensing

Current Balance

In Figure 9, $I_{SENSE}[N]$ is the current signal which is proportional to current flowing through channel N. Larger $I_{SENSE}[N]$ will lower the positive input voltage of the corresponding PWM comparator and decrease the PWM duty of the corresponding channel as shown in Figure 10. Eventually, current flowing through each channel will be balanced.

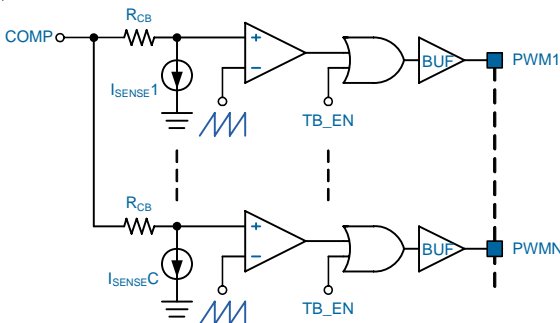


Figure 10. Current Balance

Over Current Protection

The uP6208 provides both channel current OCP and total current OCP as shown in Figure 11. R_{IMAX1} and R_{IMAX2} set the OCP levels respectively. Once OCP is triggered, it will be latched. Only re-start up can release the latch. uP6208 will turn off both high side MOSFET and low side MOSFET of all channels. 20uS delay is used in channel current OCP detection and 80uS delay is use in total current OCP detection to prevent false trigger. It is recommended to use total current OCP as an accurate steady state over current protection while using channel current OCP as short circuit protection.

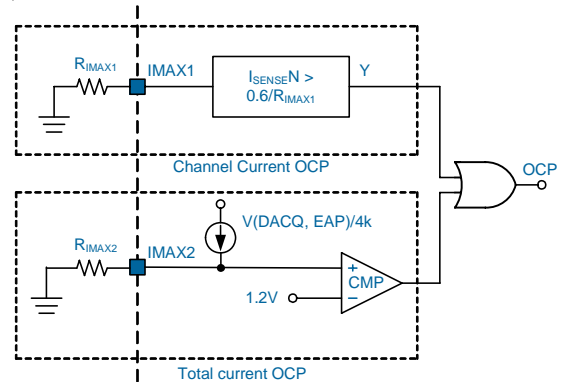


Figure 11. Over Current Protection

Control Loop

A high gain and low input offset error amplifier (EA) is used for the control loop. The positive input of EA is set via the VID logic according to the voltages listed in V_{DAC} table of INTEL VR11/VR10 or AMD K8. This voltage is then shifted by a voltage proportional to total load current for active voltage positioning. The output of the EA is the COMP pin. V_{COMP} is shifted by a voltage proportional to channel current. Then the voltage is compared with internal ramp to generate PWM signal. The negative input (FB) is tied to the positive remote sense pin of CPU through a resistor R_{FB} for sensing and controlling the output voltage. The main loop compensation is incorporated into the feedback network between FB and COMP. A type-3 compensation network like Figure 6 is recommended. The values of R, C in type-3 compensation need complex calculation and fine tune. We simplify the problem by providing a design tool to our customers. Our design tool contains a spreadsheet which can generate the R, C values according to customer's requirement. The design tool does not provide the optimal R, C values but provides a proper starting R, C values for fine tune.

Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the VOUT pin. Once V_{VOUT} exceeds $V_{EAP} + 150mV$, OVP is triggered and latched. The uP6208 will try to turn on low side MOSFET and turn off high side MOSFET to protect CPU. A 20uS delay is used in OVP detection circuit to prevent false trigger. Only re-start up can release OVP latch.

I²C Interface

The uP6208 includes an I²C interface. The main purpose of the I²C interface is to adjust output voltage, switching frequency and operating phase number of VR controller

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according to the total load current. We call it AUTOPHASE. The target of AUTOPHASE is an optimal VR design for both power conversion efficiency and CPU performance. Operating parameters that can be adjusted through the I²C are:

1. Define the 4 load current states (LCS0, LCS1, LCS2, LCS3): V(IMON) is converted to an 8-bit digital value and compared with 3 I²C programmable registers (VM0[7:0], VM1[7:0], VM2[7:0]). LCS0, LCS1, LCS2 and LCS3 are defined as

LCS0: V(IMON) > V(VM0[7:0]), highest load current.
 LCS1: V(VM0[7:0]) > V(IMON) > V(VM1[7:0])
 LCS2: V(VM1[7:0]) > V(IMON) > V(VM2[7:0])
 LCS3: V(VM2[7:0]) > V(IMON), lowest load current.

2. Voltage offset of the 4 load current states: 4 I²C programmable registers (VS0[7:0], VS1[7:0], VS2[7:0], VS3[7:0]) define the voltage offset in LCS0, LCS1, LCS2 and LCS3 respectively.

3. Frequency adjust of the 4 load current states: IICF0[1:0], IICF1[1:0], IICF2[1:0] and IICF3[1:0] define the frequency offset in LCS0, LCS1, LCS2 and LCS3 respectively. F0 is the frequency set by resistor between RT pin and GND.

IICFn[1:0] = [00] => 1.0*F0
 IICFn[1:0] = [01] => 1.2*F0
 IICFn[1:0] = [10] => 1.4*F0
 IICFn[1:0] = [11] => 0.8*F0

4. Operating phase number of the 4 load current states: IICP0[1:0], IICP1[1:0], IICP2[1:0] and IICP3[1:0] define the operating phase number in LCS0, LCS1, LCS2 and LCS3 respectively.

IICPn[1:0] = [00] => 12-phase
 IICPn[1:0] = [01] => 6-phase
 IICPn[1:0] = [10] => 2-phase
 IICPn[1:0] = [11] => undefined

5. 8-bit A/D conversion result of V(IMON): The result is stored in register IMONAD[7:0]

V(IMON)=IMON[7:0]*6.25mV
 but IMONAD[7:0] = [11xxxxxx] means V(IMON) > 1.2V only.

6. Read VID input logic value through I²C interface: The value is stored in register IICVID[7:0]

7. Read which VID table is used now through I²C interface: The value is stored in register IICVR[1:0]

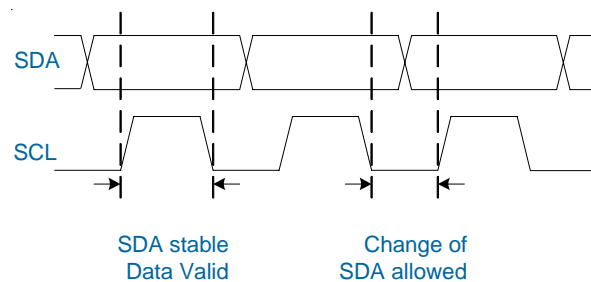
IICVR[1:0] = [00] => AMD 6-bit
 IICVR[1:0] = [01] => AMD 5-bit
 IICVR[1:0] = [10] => VR10

IICVR[1:0] = [11] => VR11

8. Read operating phase number through I²C interface: The value is stored in register IICP12, IICP6 and IICP2. Always, only one of them is H.
9. Enable/disable the AUTOPHASE function.

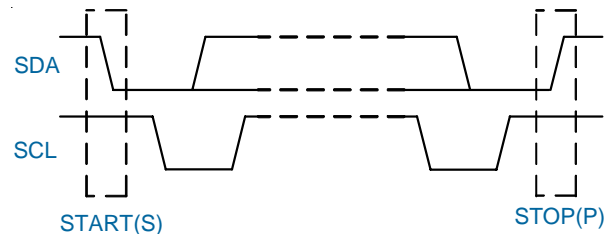
Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to the figure below.



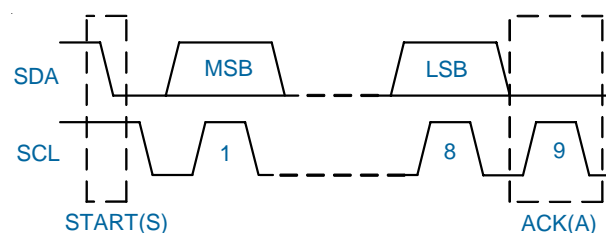
START and STOP Conditions

A START (S) condition is a HIGH to LOW transition of SDA while SCL is HIGH. The STOP (P) condition is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition must be sent before each START condition.



Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the acknowledge bit (A). After the start condition, the master sends 7 slave address bits and a R/W bit during the next 8 clock pulses. During the ninth clock pulse, the device that recognizes its own address pulls SDA low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.



Read and Write Protocol

Write to a Single Register

S	slave_addr+W	AS	reg_addr	AS	reg_data	AS	P
---	--------------	----	----------	----	----------	----	---

Read from a Single Register

S	slave_addr+W	AS	reg_addr	NA	P
---	--------------	----	----------	----	---

S = START, P = STOP, AS = ACK from slave, AM = ACK from master, NA = No ACK

Register Map

reg_addr = 01h

	VM0[7:0]
Type	R/W
Default Value	00h

reg_addr = 02h

	VM1[7:0]
Type	R/W
Default Value	00h

reg_addr = 03h

	VM2[7:0]
Type	R/W
Default Value	00h

reg_addr = 04h

	VS0[7:0]
Type	R/W
Default Value	00h

reg_addr = 05h

	VS1[7:0]
Type	R/W
Default Value	00h

Functional Description

reg_addr = 06h

	VS2[7:0]
Type	R/W
Default Value	00h

reg_addr = 07h

	VS3[7:0]
Type	R/W
Default Value	00h

reg_addr = 08h

	IICF0[1]	IICF0[0]	IICF1[1]	IICF1[0]	IICF2[1]	IICF2[0]	IICF3[1]	IICF3[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0

reg_addr = 09h

	IICP0[1]	IICP0[0]	IICP1[1]	IICP1[0]	IICP2[1]	IICP2[0]	IICP3[1]	IICP3[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0

reg_addr = 0Ah

	IMONAD[7:0]
Type	R
Default Value	xxh

reg_addr = 0Bh

	IICVID[7:0]
Type	R
Default Value	xxh

reg_addr = 0Ch

	IICVR[1]	IICVR[0]	IICP12	IICP6	IICP2	x	x	x
Type	R	R	R	R	R	x	x	x
Default Value	x	x	x	x	x	x	x	x

reg_addr = 0Dh

Functional Description

	AUTO PHASE	x	x	x	x	x	x	x
Type	R/W	x	x	x	x	x	x	x
Default Value	0	x	x	x	x	x	x	x

AUTOPHASE, 1: enable, 0: disable

reg_addr = 0Eh

	MISC[7]	MIS[6]	MISC[5]	MISC[4]	x	x	x	x
Type	R/W	R/W	R/W	R/W	x	x	x	x
Default Value	0	x	0	0	x	x	x	x

MISC[7], 1: enable watch dog timer, 0: disable

MISC[6], set to 1 when watch dog time out, reset to 0 after reading.

MISC[5:4], watch dog time out selector, [11]: 3200mS, [10]: 1600mS, [01]: 800mS, [00]: 400mS.

reg_addr = 0Fh

	VER[7:0]
Type	R
Default Value	00h

reg_addr = B2h

	CHIPID[7:0]
Type	R
Default Value	01h

Functional Description

VSN[7:0]

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Voffset(mv)
0	0	0	0	0	0	0	0	0.00
0	0	0	0	0	0	0	1	6.25
0	0	0	0	0	0	1	0	12.50
0	0	0	0	0	0	1	1	18.75
0	0	0	0	0	1	0	0	25.00
0	0	0	0	0	1	0	1	31.25
0	0	0	0	0	1	1	0	37.50
0	0	0	0	0	1	1	1	43.75
0	0	0	0	1	0	0	0	50.00
0	0	0	0	1	0	0	1	56.25
0	0	0	0	1	0	1	0	62.50
0	0	0	0	1	0	1	1	68.75
0	0	0	0	1	1	0	0	75.00
0	0	0	0	1	1	0	1	81.25
0	0	0	0	1	1	1	0	87.50
0	0	0	0	1	1	1	1	93.75
0	0	0	1	0	0	0	0	100.00
0	0	0	1	0	0	0	1	106.25
0	0	0	1	0	0	1	0	112.50
0	0	0	1	0	0	1	1	118.75
0	0	0	1	0	1	0	0	125.00
0	0	0	1	0	1	0	1	131.25
0	0	0	1	0	1	1	0	137.50
0	0	0	1	0	1	1	1	143.75
0	0	0	1	1	0	0	0	150.00
0	0	0	1	1	0	0	1	156.25
0	0	0	1	1	0	1	0	162.50
0	0	0	1	1	0	1	1	168.75
0	0	0	1	1	1	0	0	175.00
0	0	0	1	1	1	0	1	181.25
0	0	0	1	1	1	1	0	187.50
0	0	0	1	1	1	1	1	193.75
0	0	1	0	0	0	0	0	200.00
0	0	1	0	0	0	0	1	206.25
0	0	1	0	0	0	1	0	212.50
0	0	1	0	0	0	1	1	218.75
0	0	1	0	0	1	0	0	225.00
0	0	1	0	0	1	0	1	231.25
0	0	1	0	0	1	1	0	237.50
0	0	1	0	0	1	1	1	243.75
0	0	1	0	1	0	0	0	250.00
0	0	1	0	1	0	0	1	256.25
0	0	1	0	1	0	1	0	262.50

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Voffset(mv)
0	0	1	0	1	0	1	1	268.75
0	0	1	0	1	1	0	0	275.00
0	0	1	0	1	1	0	1	281.25
0	0	1	0	1	1	1	0	287.50
0	0	1	0	1	1	1	1	293.75
0	0	1	1	0	0	0	0	300.00
0	0	1	1	0	0	0	1	306.25
0	0	1	1	0	0	1	0	312.50
0	0	1	1	0	0	1	1	318.75
0	0	1	1	0	1	0	0	325.00
0	0	1	1	0	1	0	1	331.25
0	0	1	1	0	1	1	0	337.50
0	0	1	1	0	1	1	1	343.75
0	0	1	1	1	0	0	0	350.00
0	0	1	1	1	0	0	1	356.25
0	0	1	1	1	0	1	0	362.50
0	0	1	1	1	0	1	1	368.75
0	0	1	1	1	1	0	0	375.00
0	0	1	1	1	1	0	1	381.25
0	0	1	1	1	1	1	0	387.50
0	0	1	1	1	1	1	1	393.75
0	1	0	0	0	0	0	0	400.00
0	1	0	0	0	0	0	1	406.25
0	1	0	0	0	0	1	0	412.50
0	1	0	0	0	0	1	1	418.75
0	1	0	0	0	1	0	0	425.00
0	1	0	0	0	1	0	1	431.25
0	1	0	0	0	1	1	0	437.50
0	1	0	0	0	1	1	1	443.75
0	1	0	0	1	0	0	0	450.00
0	1	0	0	1	0	0	1	456.25
0	1	0	0	1	0	1	0	462.50
0	1	0	0	1	0	1	1	468.75
0	1	0	0	1	1	0	0	475.00
0	1	0	0	1	1	0	1	481.25
0	1	0	0	1	1	1	0	487.50
0	1	0	0	1	1	1	1	493.75
0	1	0	1	0	0	0	0	500.00
0	1	0	1	0	0	0	1	501.25
0	1	0	1	0	0	1	0	512.50
0	1	0	1	0	0	1	1	518.75
0	1	0	1	0	1	0	0	525.00
0	1	0	1	0	1	0	1	531.25

Functional Description

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Voffset(mv)
0	1	0	1	0	1	1	0	537.50
0	1	0	1	0	1	1	1	543.75
0	1	0	1	1	0	0	0	550.00
0	1	0	1	1	0	0	1	556.25
0	1	0	1	1	0	1	0	562.50
0	1	0	1	1	0	1	1	568.75
0	1	0	1	1	1	0	0	575.00
0	1	0	1	1	1	0	1	581.25
0	1	0	1	1	1	1	0	587.50
0	1	0	1	1	1	1	1	593.75
0	1	1	0	0	0	0	0	600.00
0	1	1	0	0	0	0	1	606.25
0	1	1	0	0	0	1	0	612.50
0	1	1	0	0	0	1	1	618.75
0	1	1	0	0	1	0	0	625.00
0	1	1	0	0	1	0	1	631.25
0	1	1	0	0	1	1	0	637.50
0	1	1	0	0	1	1	1	643.75
0	1	1	0	1	0	0	0	650.00
0	1	1	0	1	0	0	1	656.25
0	1	1	0	1	0	1	0	662.50
0	1	1	0	1	0	1	1	668.75
0	1	1	0	1	1	0	0	675.00
0	1	1	0	1	1	0	1	681.25
0	1	1	0	1	1	1	0	687.50
0	1	1	0	1	1	1	1	693.75
0	1	1	1	0	0	0	0	700.00
0	1	1	1	0	0	0	1	706.25
0	1	1	1	0	0	1	0	712.50
0	1	1	1	0	0	1	1	718.75
0	1	1	1	0	1	0	0	725.00
0	1	1	1	0	1	0	1	731.25
0	1	1	1	0	1	1	0	737.50
0	1	1	1	0	1	1	1	743.75
0	1	1	1	1	0	0	0	750.00
0	1	1	1	1	0	0	1	756.25
0	1	1	1	1	0	1	0	762.50
0	1	1	1	1	0	1	1	768.75
0	1	1	1	1	1	0	0	775.00
0	1	1	1	1	1	0	1	781.25
0	1	1	1	1	1	1	0	787.50
0	1	1	1	1	1	1	1	793.75
1	0	0	0	0	0	0	0	0.00

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Voffset(mv)
1	0	0	0	0	0	0	1	-6.25
1	0	0	0	0	0	0	1	-12.50
1	0	0	0	0	0	0	1	-18.75
1	0	0	0	0	0	1	0	-25.00
1	0	0	0	0	0	1	0	-31.25
1	0	0	0	0	0	1	1	-37.50
1	0	0	0	0	0	1	1	-43.75
1	0	0	0	0	1	0	0	-50.00
1	0	0	0	0	1	0	0	-56.25
1	0	0	0	0	1	0	1	-62.50
1	0	0	0	0	1	0	1	-68.75
1	0	0	0	0	1	1	0	-75.00
1	0	0	0	0	1	1	0	-81.25
1	0	0	0	0	1	1	1	-87.50
1	0	0	0	0	1	1	1	-93.75
1	0	0	0	1	0	0	0	-100.00
1	0	0	0	1	0	0	0	-106.25
1	0	0	0	1	0	0	1	-112.50
1	0	0	0	1	0	0	1	-118.75
1	0	0	0	1	0	1	0	-125.00
1	0	0	0	1	0	1	0	-131.25
1	0	0	0	1	0	1	1	-137.50
1	0	0	0	1	0	1	1	-143.75
1	0	0	0	1	1	0	0	-150.00
1	0	0	0	1	1	0	0	-156.25
1	0	0	0	1	1	0	1	-162.50
1	0	0	0	1	1	0	1	-168.75
1	0	0	0	1	1	1	0	-175.00
1	0	0	0	1	1	1	0	-181.25
1	0	0	0	1	1	1	1	-187.50
1	0	0	0	1	1	1	1	-193.75
1	0	0	1	0	0	0	0	-200.00
1	0	0	1	0	0	0	0	-206.25
1	0	0	1	0	0	0	1	-212.50
1	0	0	1	0	0	0	1	-218.75
1	0	0	1	0	0	0	1	-225.00
1	0	0	1	0	0	1	0	-231.25
1	0	0	1	0	0	1	1	-237.50
1	0	0	1	0	0	1	1	-243.75
1	0	0	1	0	1	0	0	-250.00
1	0	0	1	0	1	0	0	-256.25
1	0	0	1	0	1	0	1	-262.50
1	0	0	1	0	1	0	1	-268.75

Functional Description

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Voffset(mv)
1	0	1	0	1	1	0	0	-275.00
1	0	1	0	1	1	0	1	-281.25
1	0	1	0	1	1	1	0	-287.50
1	0	1	0	1	1	1	1	-293.75
1	0	1	1	0	0	0	0	-300.00
1	0	1	1	0	0	0	1	-306.25
1	0	1	1	0	0	1	0	-312.50
1	0	1	1	0	0	1	1	-318.75
1	0	1	1	0	1	0	0	-325.00
1	0	1	1	0	1	0	1	-331.25
1	0	1	1	0	1	1	0	-337.50
1	0	1	1	0	1	1	1	-343.75
1	0	1	1	1	0	0	0	-350.00
1	0	1	1	1	0	0	1	-356.25
1	0	1	1	1	0	1	0	-362.50
1	0	1	1	1	0	1	1	-368.75
1	0	1	1	1	1	0	0	-375.00
1	0	1	1	1	1	0	1	-381.25
1	0	1	1	1	1	1	0	-387.50
1	0	1	1	1	1	1	1	-393.75
1	1	0	0	0	0	0	0	-400.00
1	1	0	0	0	0	0	1	-406.25
1	1	0	0	0	0	0	1	-412.50
1	1	0	0	0	0	1	1	-418.75
1	1	0	0	0	1	0	0	-425.00
1	1	0	0	0	1	0	1	-431.25
1	1	0	0	0	1	1	0	-437.50
1	1	0	0	0	1	1	1	-443.75
1	1	0	0	1	0	0	0	-450.00
1	1	0	0	1	0	0	1	-456.25
1	1	0	0	1	0	1	0	-462.50
1	1	0	0	1	0	1	1	-468.75
1	1	0	0	1	1	0	0	-475.00
1	1	0	0	1	1	0	1	-481.25
1	1	0	0	1	1	1	0	-487.50
1	1	0	0	1	1	1	1	-493.75
1	1	0	1	0	0	0	0	-500.00
1	1	0	1	0	0	0	1	-506.25
1	1	0	1	0	0	1	0	-512.50
1	1	0	1	0	0	1	1	-518.75
1	1	0	1	0	1	0	0	-525.00
1	1	0	1	0	1	0	1	-531.25

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Voffset(mv)
1	1	0	1	0	1	1	0	-537.50
1	1	0	1	0	1	1	1	-543.75
1	1	0	1	1	0	0	0	-550.00
1	1	0	1	1	0	0	1	-556.25
1	1	0	1	1	0	1	0	-562.50
1	1	0	1	1	0	1	1	-568.75
1	1	0	1	1	1	0	0	-575.00
1	1	0	1	1	1	0	1	-581.25
1	1	0	1	1	1	1	0	-587.50
1	1	0	1	1	1	1	1	-593.75
1	1	1	0	0	0	0	0	-600.00
1	1	1	0	0	0	0	1	-606.25
1	1	1	0	0	0	1	0	-612.50
1	1	1	0	0	0	1	1	-618.75
1	1	1	0	0	1	0	0	-625.00
1	1	1	0	0	1	0	1	-631.25
1	1	1	0	0	1	1	0	-637.50
1	1	1	0	0	1	1	1	-643.75
1	1	1	0	1	0	0	0	-650.00
1	1	1	0	1	0	0	1	-656.25
1	1	1	0	1	0	1	0	-662.50
1	1	1	0	1	0	1	1	-668.75
1	1	1	0	1	1	0	0	-675.00
1	1	1	0	1	1	0	1	-681.25
1	1	1	0	1	1	1	0	-687.50
1	1	1	0	1	1	1	1	-693.75
1	1	1	1	0	0	0	0	-700.00
1	1	1	1	0	0	0	1	-706.25
1	1	1	1	0	0	1	0	-712.50
1	1	1	1	0	0	1	1	-718.75
1	1	1	1	0	1	0	0	-725.00
1	1	1	1	0	1	0	1	-731.25
1	1	1	1	0	1	1	0	-737.50
1	1	1	1	0	1	1	1	-743.75
1	1	1	1	1	0	0	0	-750.00
1	1	1	1	1	0	0	1	-756.25
1	1	1	1	1	0	1	0	-762.50
1	1	1	1	1	0	1	1	-768.75
1	1	1	1	1	1	0	0	-775.00
1	1	1	1	1	1	0	1	-781.25
1	1	1	1	1	1	1	0	-787.50
1	1	1	1	1	1	1	1	-793.75

Absolute Maximum Rating

Supply Input Voltage, 5VCC (Note 1)	-----	-0.3V to +6V
Other Pins	-----	-0.3V to +6V
Storage Temperature Range	-----	-65°C to +150°C
Junction Temperature	-----	150°C
Lead Temperature (Soldering, 10 sec)	-----	260°C
ESD Rating (Note 2)		
HBM (Human Body Mode)	-----	2kV
MM (Machine Mode)	-----	200V

Thermal Information

Package Thermal Resistance (Note 3)		
LQFP7x7 - 64L θ_{JA}	-----	43.6°C/W
Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$		
LQFP7x7 - 64L θ_{JA}	-----	2.3W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4)	-----	-40°C to +125°C
Operating Ambient Temperature Range	-----	-40°C to +85°C
Supply Input Voltage, V_{CC5}	-----	4.5V to 5.5V

Electrical Characteristics

(5VCC = 5V, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Input Voltage	V_{CC5}		4.5	--	5.5	V
V_{CC5} POR Threshold			4.1	4.3	4.5	V
V_{CC5} POR Hysteresis		5VCC Falling.	--	0.1	--	V
Supply Current	I_{CC5}	No Switching	--	5	--	mA
Error Amplifier						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Input Bias Current	I_{EA}		-10	--	10	nA
Gain Bandwidth Product	GBW_{EA}		--	10	--	MHz
Voltage Accuracy						
DAC Output Accuracy	V_{FB}	1.0V to 1.6V	-0.5	--	0.5	%
		0.8V to 1.0V	-8	--	8	mV
		0.5V to 0.8V	-10	--	10	mV
Soft Start						
Soft Start Current	I_{SS}	Normal	--	32	--	uA
VTT Input						
Input Low	$V_{IL(VTT)}$		--	0.75	--	V
Input High	$V_{IH(VTT)}$		--	0.85	--	V

For Internal Discussion Only. uPI may make changes to specifications and product descriptions at any time, without notice.

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Rev. C00, File Name: uP6208-DS-C0000

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VTT Input						
Input Current	I_{VTT}		-3	--	3	uA
EN Input						
Input Low	V_{ILEN}		--	1	--	V
Input High	V_{IHEN}		--	1.1	--	V
Input Current	I_{EN}		-1	--	1	uA
VID Input						
Input Low	$V_{IL(VID)}$	VTT = 1.2V	0.5	--	--	V
Input High	$V_{IH(VID)}$	VTT = 1.2V	--	--	0.7	V
Input Current	I_{VID}		-1	--	1	uA
VIDOFF Delay Time	T_{VIDOFF}		--	20	--	us
Oscillator						
Frequency Range	F_{SW}		100	--	1000	kHz
Frequency Variation		$R_{RT} = 26k\Omega$	270	300	330	kHz
Max Duty		$R_{RT} = 26k\Omega$	--	50	--	%
Output Voltage	V_{RT}		1.1	1.2	1.3	V
Current Sense Amplifier						
Offset Voltage	$V_{OS(CSA)}$	No Load, Guaranteed by Design	-1	--	1	mV
Input Bias Current			-10	--	10	nA
Gain Bandwidth Product	$G_{BW(CSA)}$		--	10	--	MHz
Current Balance Voltage Control Current Source (VCCS)						
Offset Voltage	$V_{OS(VCCS)}$		-2	--	2	mV
Transconductance	GM_{VCCS}		--	1.33	--	1/k Ω
Gain Bandwidth Product	$G_{BW(VCCS)}$		--	10	--	MHz
PWM Output						
Output Low Voltage	$V_{OL(PWM)}$	$I_{SINK} = 4mA$	--	--	0.2	V
Output High Voltage	$V_{OH(PWM)}$	$I_{SOURCE} = 4mA$	4.7	--	--	V
PWRGD Output						
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{SINK} = 4mA$	--	--	0.2	V
Current Monitoring						
IMON Output Voltage		I_I	--	--	1.1	V
IMON Voltage Variation		Full Load	-10	--	10	%

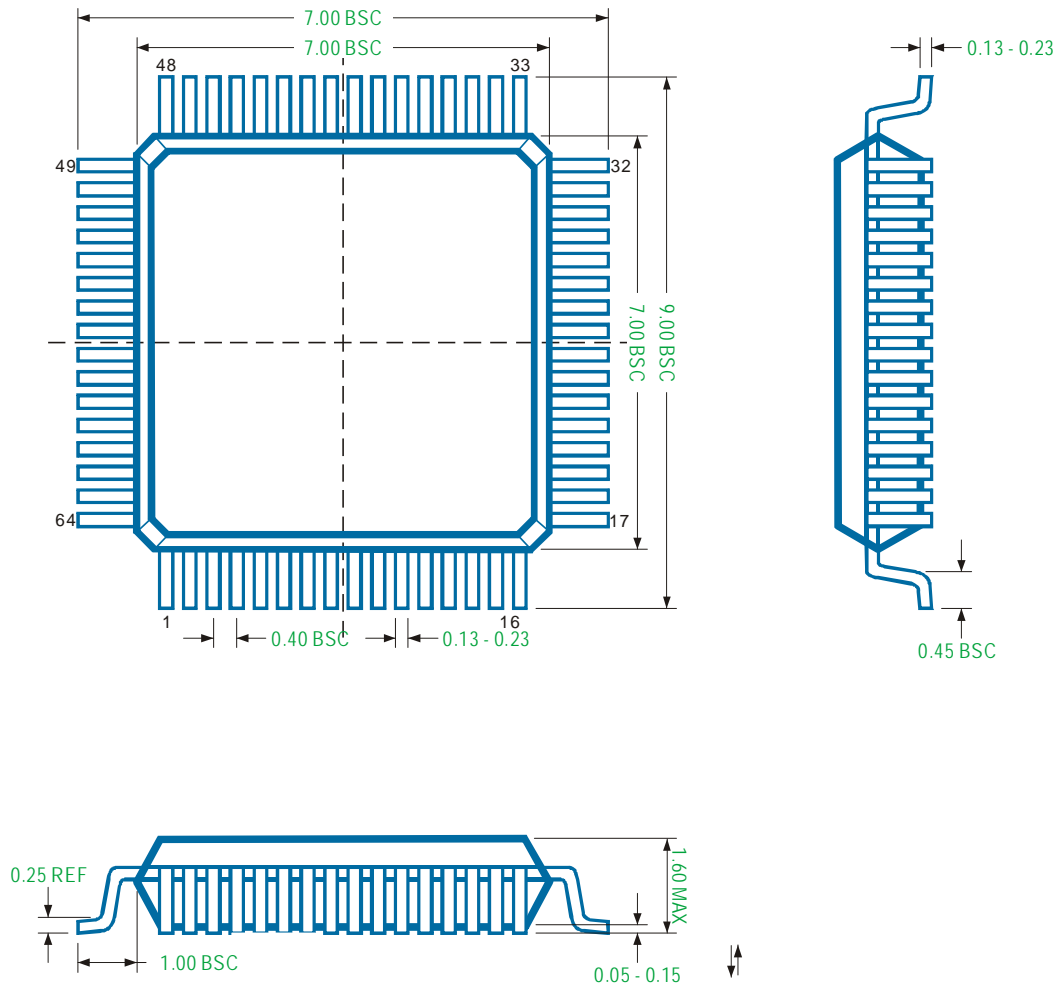
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection						
OVP Threshold	V_{OVP}	$V_{OUT} - V_{EAP}$	--	150	--	mV
OVP Dealy	T_{OVP}		--	20	--	us
IMAX1 Output Voltage			1.1	--	1.3	V
Channel Current OCP Daly	T_{OCP1}		--	20	--	us
IMAX Input Threshold			1.1	--	1.3	V
Total Current OCP Dealy	T_{OCP2}		--	20	--	us

- Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
- Note 2.** Devices are ESD sensitive. Handling precaution recommended.
- Note 3.** θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.
- Note 4.** The device is not guaranteed to function outside its operating conditions.

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Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.