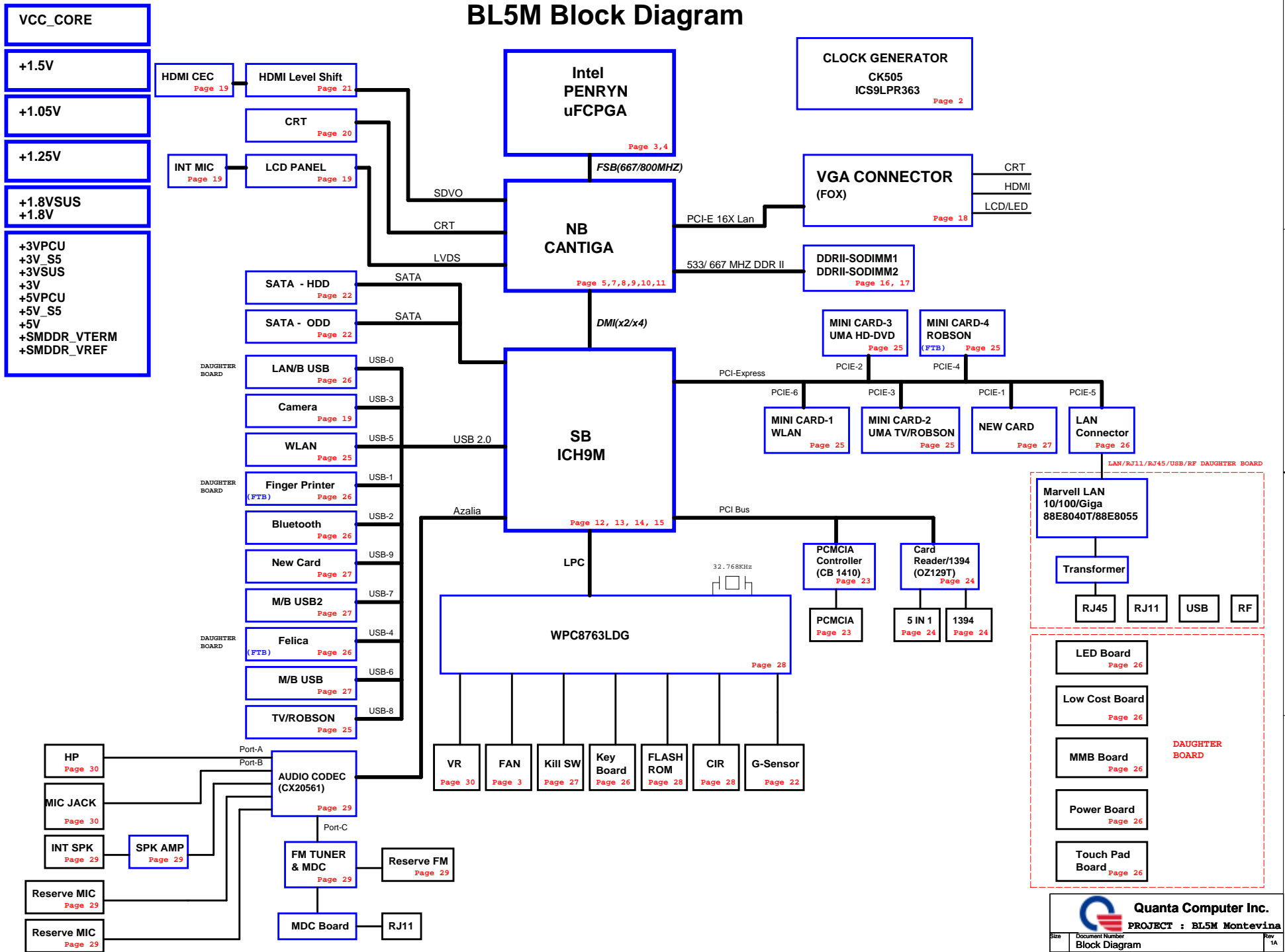
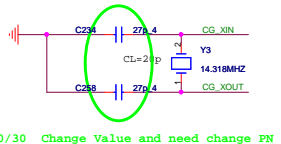
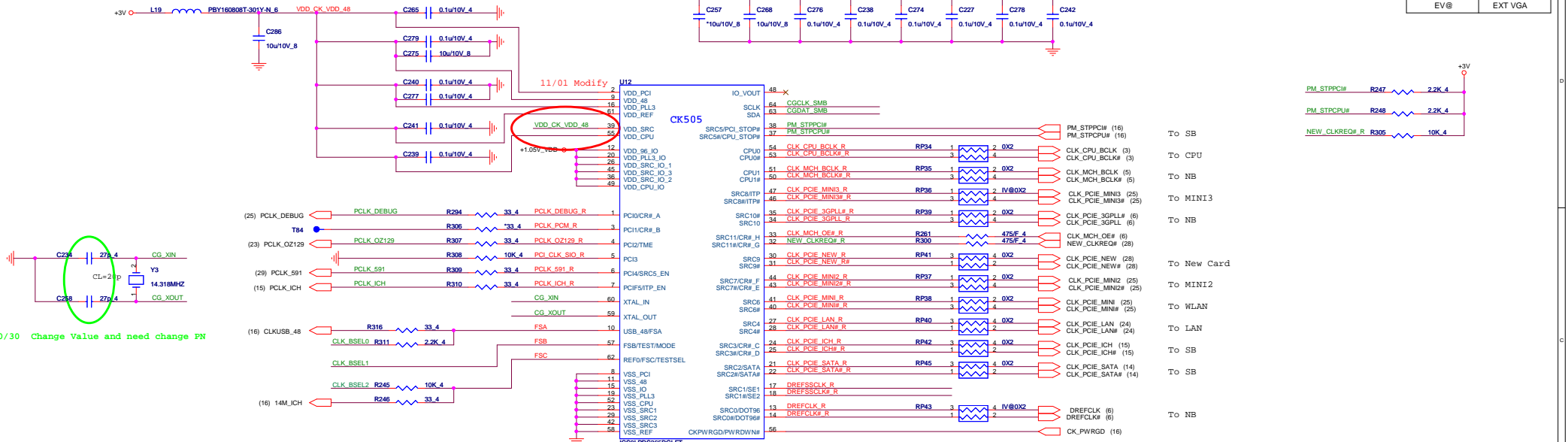


# BL5M Block Diagram

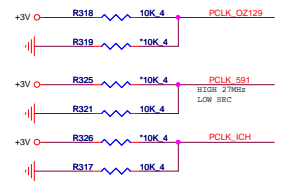


# Clock Generator

BOM Option Table	
Reference	Description
IV@	INT VGA
EV@	EXT VGA



Pin	IC59LPRS365BGLFT	Pin	IC59LPRS365BGLFT	Function
Pin 4	PCI2/TME	Pin 17	PCI-4/27M_SEL	Internal PD
Pin 5	PCI-3/SRCS_EN	Pin 17/18	IS SRC/DOT	Internal PD
Pin 6	PCI-4/27M_SEL	Pin 46/47	IS CPU/ITP	Internal PD
Pin 7	PCIP-5/ITP_EN			

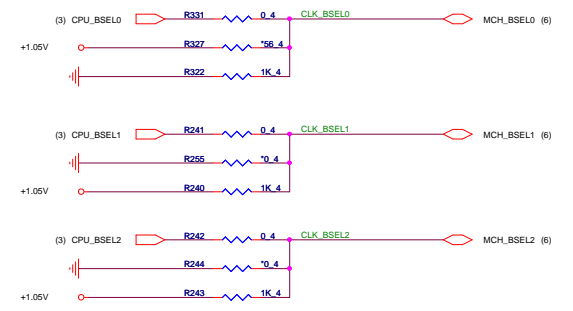


<MAIN>:IC59LPRS365BGLFT QCI:ALPRS365K13  
 <SECOND>:SLG8SP512TTR: QCI:AL8SP512K05

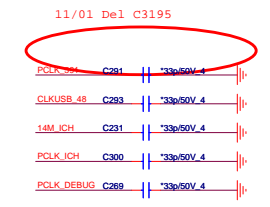
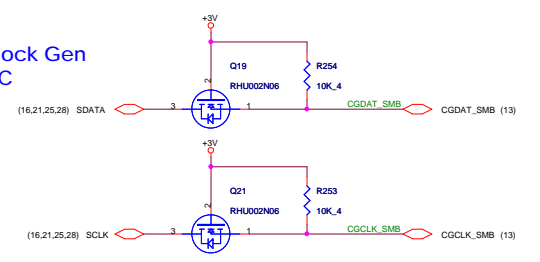
## FREQ. SEL TABLE

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

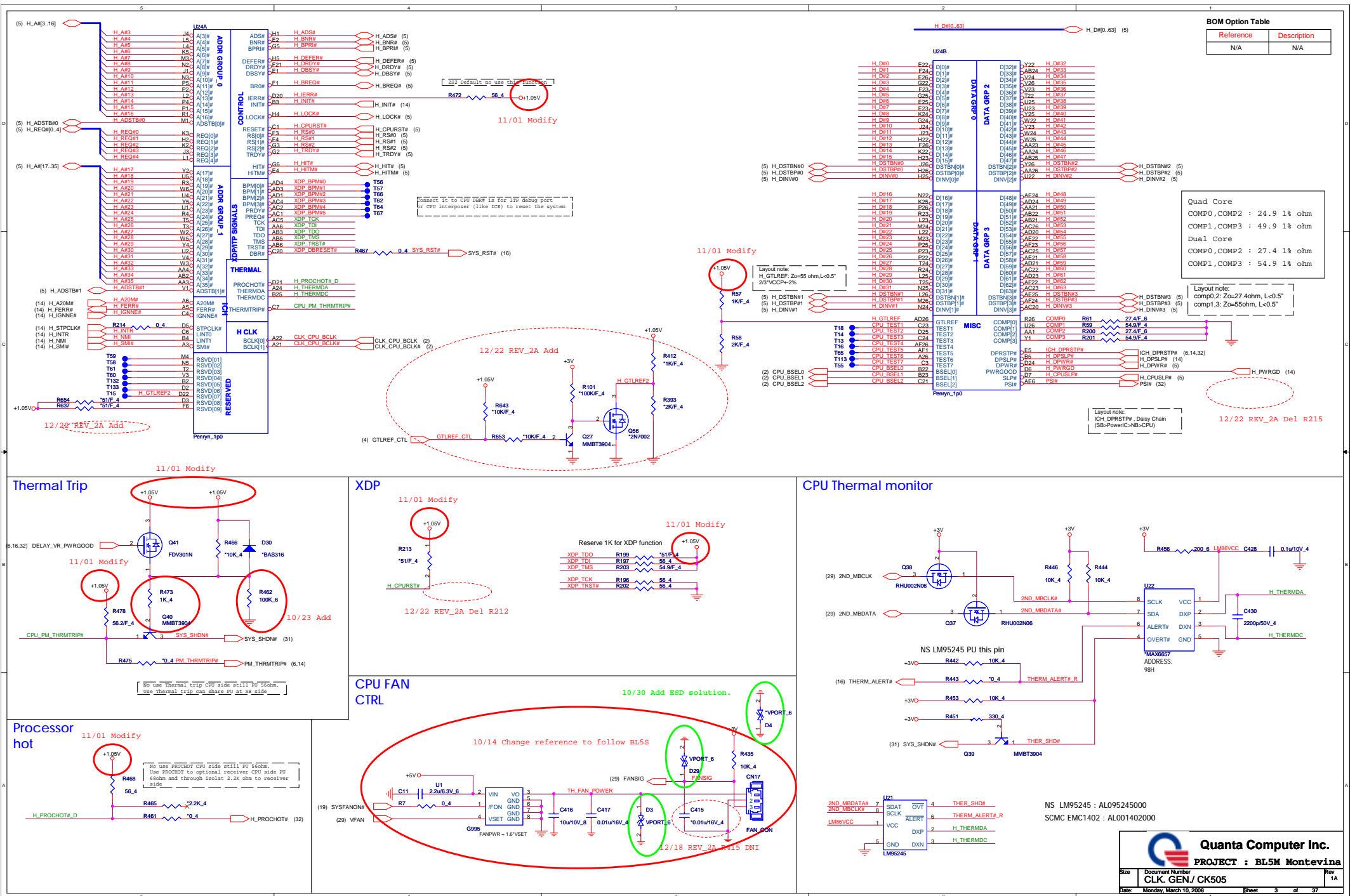


## Clock Gen I2C



**Quanta Computer Inc.**  
 PROJECT : BL5M Montevina

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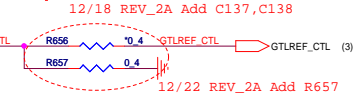
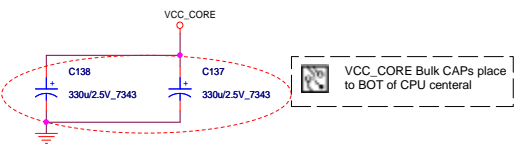
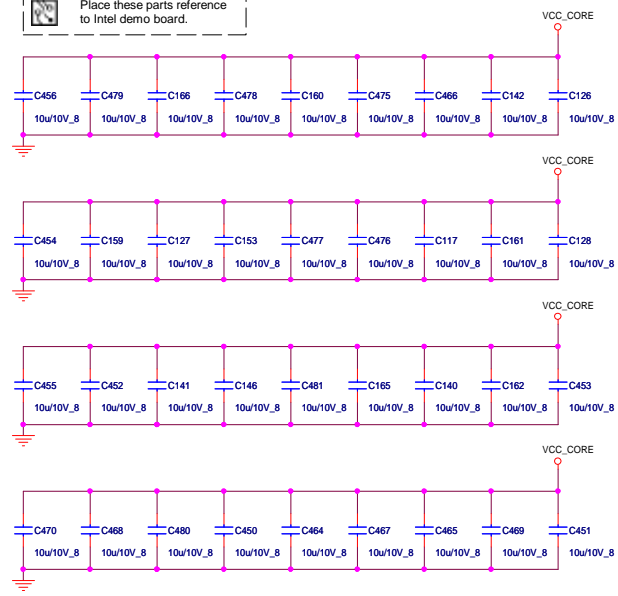
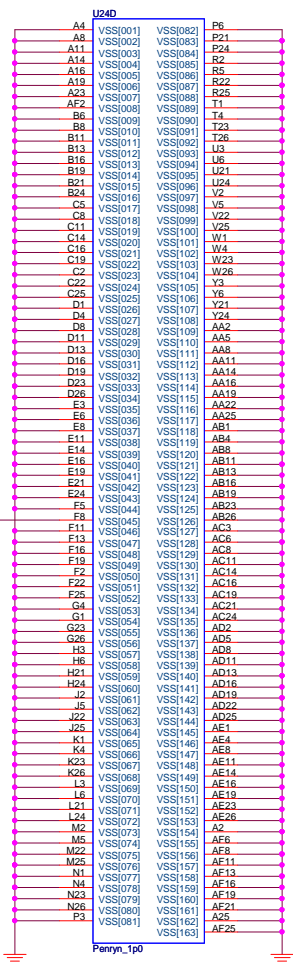
**BOM Option Table**

Reference	Description
N/A	N/A

Need NC 20PCS 10u before A1 BOM released(A0 all stuff)

Place these parts reference to Intel demo board.

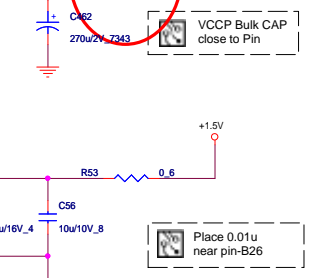
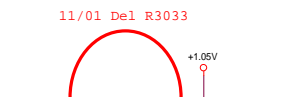
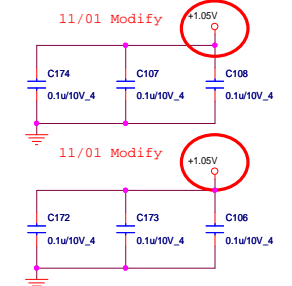
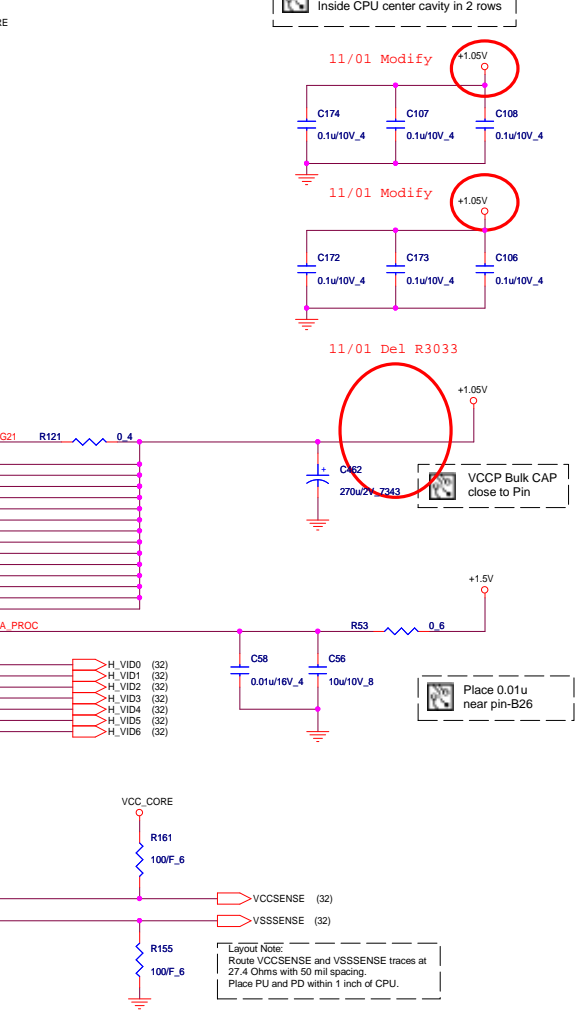
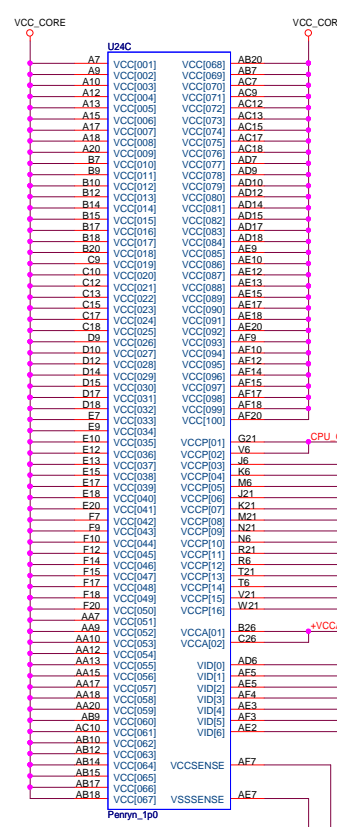
Layout Note:  
Inside CPU center cavity in 2 rows



**Penryn CPU Power Status and max current table**

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	47A	Standard Voltage CPU
VCC_CORE	O	X	X	VID	50A	SV Design Target
VCC_CORE	O	X	X	VID	TBD	Extreme Edition CPU
VCC_CORE	O	X	X	VID	67A	EE Design Target
VCCA	O	X	X	+1.5V	130mA	
VCCP	O	X	X	+1.05V	4.5A	Before VCC Stable
VCCP	O	X	X	+1.05V	2.5A	After VCC Stable

(See Penryn EMTS Rev:1.0 Table 7,8 for voltage and current)  
(See Penryn EMTS Rev:1.0 Table-3 for VID table)



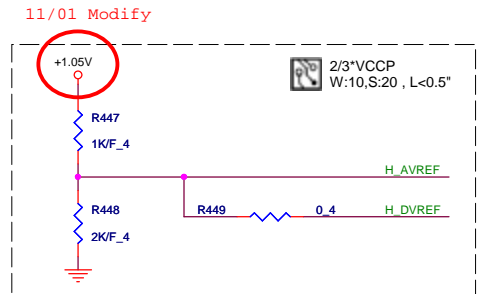
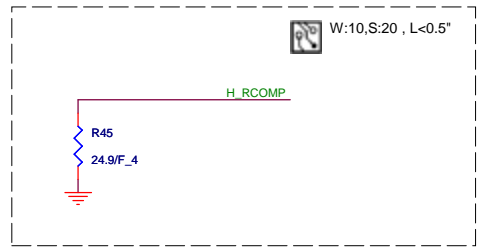
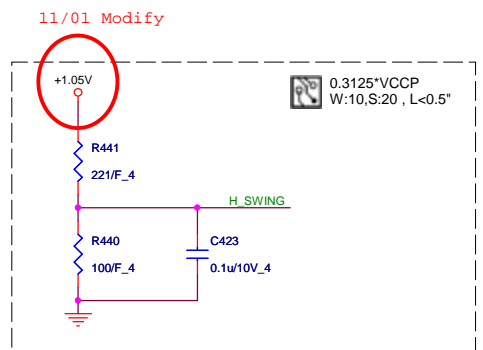
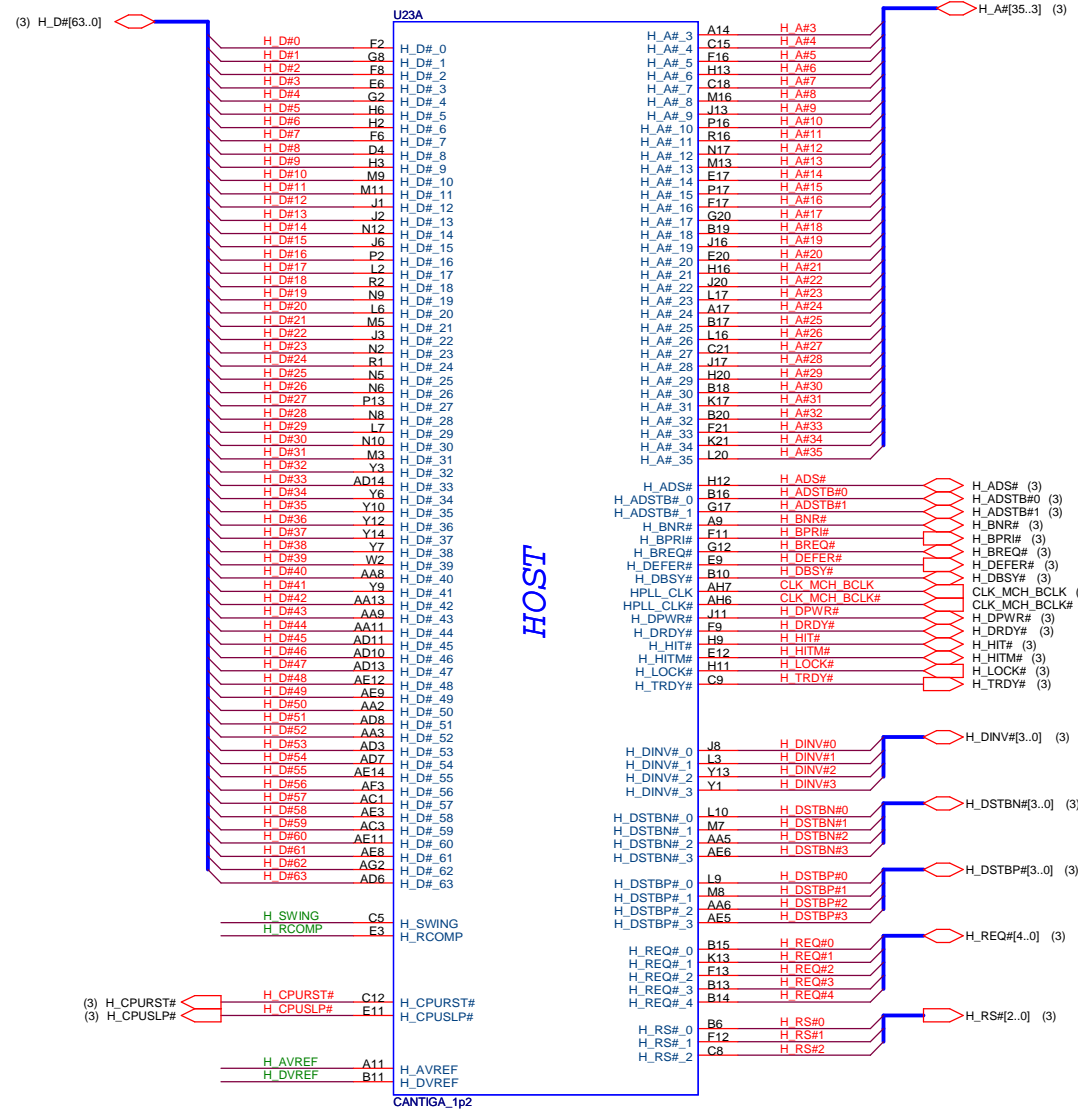
Layout Note:  
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of CPU.

**Quanta Computer Inc.**  
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BOM Option Table

Reference	Description
N/A	N/A

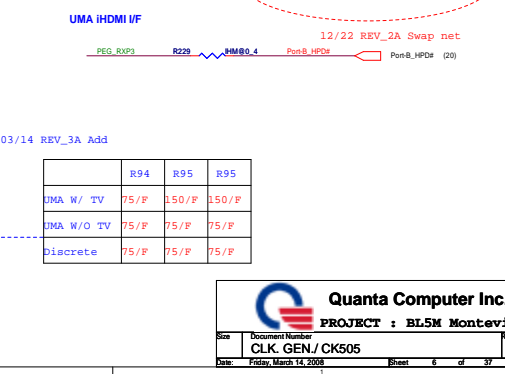
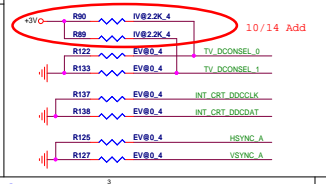
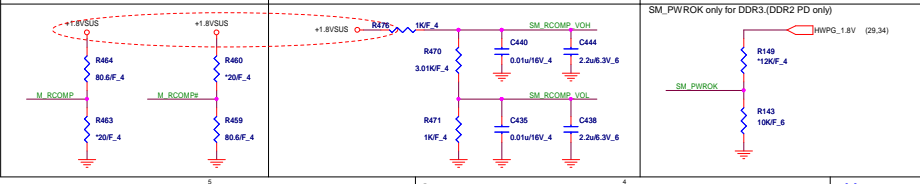
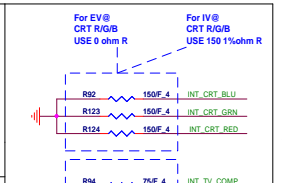
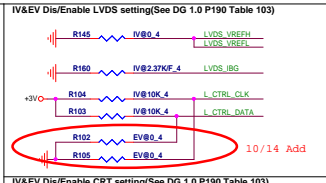
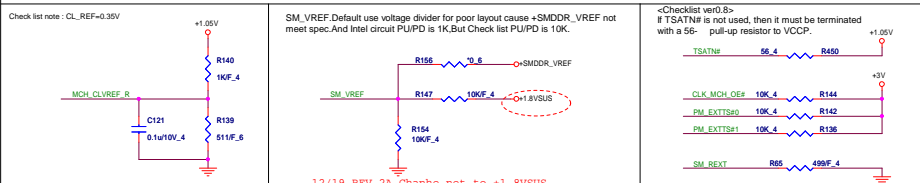
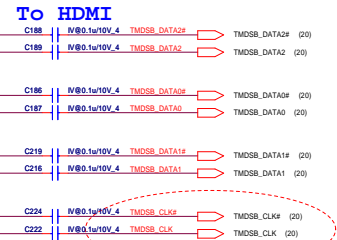
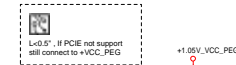
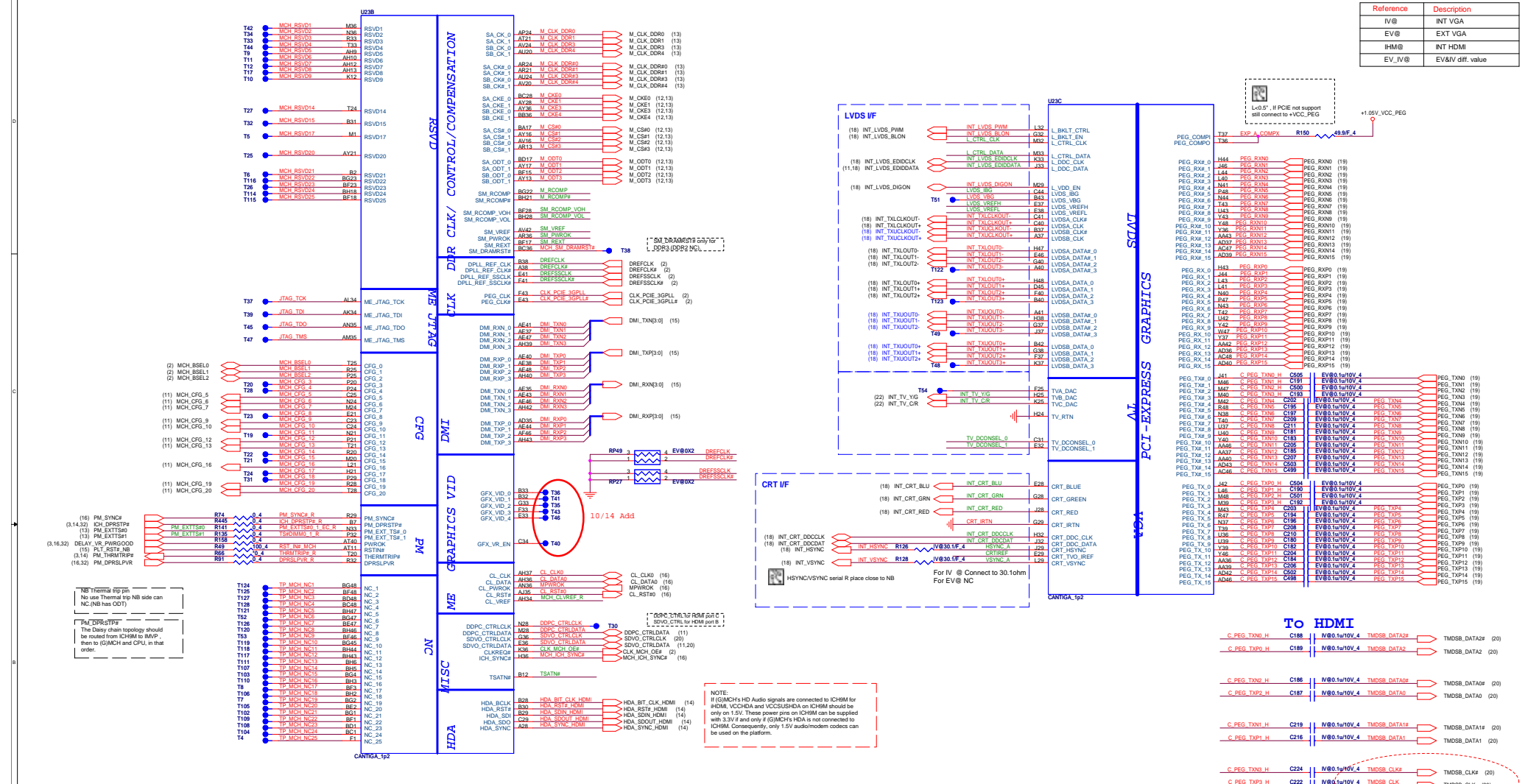


**Quanta Computer Inc.**  
PROJECT : BL5M Montevina

Size	Document Number	Rev
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**BOM Option Table**

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV@ diff. value



BOM Option Table

Reference	Description
N/A	N/A

(13) M\_A\_DQ[63:0]

(13) M\_B\_DQ[63:0]

- U23D**
- M\_A DQ0 AJ38 SA\_DQ\_0
  - M\_A DQ1 AJ41 SA\_DQ\_1
  - M\_A DQ2 AN38 SA\_DQ\_2
  - M\_A DQ3 AM38 SA\_DQ\_3
  - M\_A DQ4 AJ36 SA\_DQ\_4
  - M\_A DQ5 M\_A DQ5# SA\_DQ\_5
  - M\_A DQ6 AM44 SA\_DQ\_6
  - M\_A DQ7 AM42 SA\_DQ\_7
  - M\_A DQ8 AN43 SA\_DQ\_8
  - M\_A DQ9 AN44 SA\_DQ\_9
  - M\_A DQ10 AL40 SA\_DQ\_10
  - M\_A DQ11 AT38 SA\_DQ\_11
  - M\_A DQ12 AN41 SA\_DQ\_12
  - M\_A DQ13 AN39 SA\_DQ\_13
  - M\_A DQ14 AU44 SA\_DQ\_14
  - M\_A DQ15 AL42 SA\_DQ\_15
  - M\_A DQ16 AV39 SA\_DQ\_16
  - M\_A DQ17 AY44 SA\_DQ\_17
  - M\_A DQ18 BA40 SA\_DQ\_18
  - M\_A DQ19 BD43 SA\_DQ\_19
  - M\_A DQ20 AV41 SA\_DQ\_20
  - M\_A DQ21 AY43 SA\_DQ\_21
  - M\_A DQ22 BB41 SA\_DQ\_22
  - M\_A DQ23 BC40 SA\_DQ\_23
  - M\_A DQ24 AY37 SA\_DQ\_24
  - M\_A DQ25 BD38 SA\_DQ\_25
  - M\_A DQ26 AV37 SA\_DQ\_26
  - M\_A DQ27 AT36 SA\_DQ\_27
  - M\_A DQ28 AY38 SA\_DQ\_28
  - M\_A DQ29 BB38 SA\_DQ\_29
  - M\_A DQ30 AV36 SA\_DQ\_30
  - M\_A DQ31 AW36 SA\_DQ\_31
  - M\_A DQ32 RD13 SA\_DQ\_32
  - M\_A DQ33 AU11 SA\_DQ\_33
  - M\_A DQ34 BC11 SA\_DQ\_34
  - M\_A DQ35 BA12 SA\_DQ\_35
  - M\_A DQ36 AU13 SA\_DQ\_36
  - M\_A DQ37 AV13 SA\_DQ\_37
  - M\_A DQ38 BD12 SA\_DQ\_38
  - M\_A DQ39 BC12 SA\_DQ\_39
  - M\_A DQ40 BB9 SA\_DQ\_40
  - M\_A DQ41 BA9 SA\_DQ\_41
  - M\_A DQ42 AU10 SA\_DQ\_42
  - M\_A DQ43 AV9 SA\_DQ\_43
  - M\_A DQ44 BA11 SA\_DQ\_44
  - M\_A DQ45 BD9 SA\_DQ\_45
  - M\_A DQ46 AY8 SA\_DQ\_46
  - M\_A DQ47 BA6 SA\_DQ\_47
  - M\_A DQ48 AV5 SA\_DQ\_48
  - M\_A DQ49 AV7 SA\_DQ\_49
  - M\_A DQ50 AT9 SA\_DQ\_50
  - M\_A DQ51 AN8 SA\_DQ\_51
  - M\_A DQ52 AU5 SA\_DQ\_52
  - M\_A DQ53 AU6 SA\_DQ\_53
  - M\_A DQ54 AT5 SA\_DQ\_54
  - M\_A DQ55 AN10 SA\_DQ\_55
  - M\_A DQ56 AM11 SA\_DQ\_56
  - M\_A DQ57 AM5 SA\_DQ\_57
  - M\_A DQ58 AJ9 SA\_DQ\_58
  - M\_A DQ59 AJ8 SA\_DQ\_59
  - M\_A DQ60 AN12 SA\_DQ\_60
  - M\_A DQ61 AM13 SA\_DQ\_61
  - M\_A DQ62 AJ11 SA\_DQ\_62
  - M\_A DQ63 AJ12 SA\_DQ\_63

**DDR SYSTEM MEMORY A**

- SA\_BS\_0 BD21 M\_A BS#0
- SA\_BS\_1 BG18 M\_A BS#1
- SA\_BS\_2 AT25 M\_A BS#2
- SA\_RAS# BB20 M\_A RAS#
- SA\_CAS# AY20 M\_A CAS#
- SA\_WE# AY20 M\_A WE#
- SA\_DM\_0 AM37 M\_A DM0
- SA\_DM\_1 AT41 M\_A DM1
- SA\_DM\_2 AY41 M\_A DM2
- SA\_DM\_3 AU39 M\_A DM3
- SA\_DM\_4 BB12 M\_A DM4
- SA\_DM\_5 AY6 M\_A DM5
- SA\_DM\_6 AT7 M\_A DM6
- SA\_DM\_7 AJ5 M\_A DM7
- SA\_DQS\_0 AJ44 M\_A DQS0
- SA\_DQS\_1 AT44 M\_A DQS1
- SA\_DQS\_2 BA43 M\_A DQS2
- SA\_DQS\_3 BC37 M\_A DQS3
- SA\_DQS\_4 AW12 M\_A DQS4
- SA\_DQS\_5 BC8 M\_A DQS5
- SA\_DQS\_6 AU8 M\_A DQS6
- SA\_DQS\_7 AM7 M\_A DQS7
- SA\_DQS#\_0 AJ43 M\_A DQS#0
- SA\_DQS#\_1 AT43 M\_A DQS#1
- SA\_DQS#\_2 BA44 M\_A DQS#2
- SA\_DQS#\_3 BD37 M\_A DQS#3
- SA\_DQS#\_4 AY12 M\_A DQS#4
- SA\_DQS#\_5 BD8 M\_A DQS#5
- SA\_DQS#\_6 AU9 M\_A DQS#6
- SA\_DQS#\_7 AM8 M\_A DQS#7
- SA\_MA\_0 BA21 M\_A A0
- SA\_MA\_1 BC24 M\_A A1
- SA\_MA\_2 BG24 M\_A A2
- SA\_MA\_3 BH24 M\_A A3
- SA\_MA\_4 BG25 M\_A A4
- SA\_MA\_5 BA24 M\_A A5
- SA\_MA\_6 BD24 M\_A A6
- SA\_MA\_7 BG27 M\_A A7
- SA\_MA\_8 BF25 M\_A A8
- SA\_MA\_9 AW24 M\_A A9
- SA\_MA\_10 BC21 M\_A A10
- SA\_MA\_11 BG26 M\_A A11
- SA\_MA\_12 BH26 M\_A A12
- SA\_MA\_13 BH17 M\_A A13
- SA\_MA\_14 AY25 M\_A A14
- M\_A\_DM[7:0] (13)
- M\_A\_DQS[7:0] (13)
- M\_A\_DQS#[7:0] (13)
- M\_A\_A[14:0] (12,13)

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- U23E**
- M\_B DQ0 AK47 SB\_DQ\_0
  - M\_B DQ1 AH46 SB\_DQ\_1
  - M\_B DQ2 AP47 SB\_DQ\_2
  - M\_B DQ3 AP46 SB\_DQ\_3
  - M\_B DQ4 AJ48 SB\_DQ\_4
  - M\_B DQ5 M\_B DQ5# SB\_DQ\_5
  - M\_B DQ6 AM48 SB\_DQ\_6
  - M\_B DQ7 AP48 SB\_DQ\_7
  - M\_B DQ8 AU47 SB\_DQ\_8
  - M\_B DQ9 AU46 SB\_DQ\_9
  - M\_B DQ10 BA48 SB\_DQ\_10
  - M\_B DQ11 AY48 SB\_DQ\_11
  - M\_B DQ12 AT47 SB\_DQ\_12
  - M\_B DQ13 AR47 SB\_DQ\_13
  - M\_B DQ14 BA47 SB\_DQ\_14
  - M\_B DQ15 BC47 SB\_DQ\_15
  - M\_B DQ16 BC46 SB\_DQ\_16
  - M\_B DQ17 BC44 SB\_DQ\_17
  - M\_B DQ18 BG43 SB\_DQ\_18
  - M\_B DQ19 BF43 SB\_DQ\_19
  - M\_B DQ20 BE45 SB\_DQ\_20
  - M\_B DQ21 BC41 SB\_DQ\_21
  - M\_B DQ22 BF40 SB\_DQ\_22
  - M\_B DQ23 BF41 SB\_DQ\_23
  - M\_B DQ24 BC38 SB\_DQ\_24
  - M\_B DQ25 BF38 SB\_DQ\_25
  - M\_B DQ26 BH35 SB\_DQ\_26
  - M\_B DQ27 BG35 SB\_DQ\_27
  - M\_B DQ28 BH40 SB\_DQ\_28
  - M\_B DQ29 BG39 SB\_DQ\_29
  - M\_B DQ30 BC34 SB\_DQ\_30
  - M\_B DQ31 BH34 SB\_DQ\_31
  - M\_B DQ32 BH14 SB\_DQ\_32
  - M\_B DQ33 BC12 SB\_DQ\_33
  - M\_B DQ34 BH11 SB\_DQ\_34
  - M\_B DQ35 BG8 SB\_DQ\_35
  - M\_B DQ36 BH12 SB\_DQ\_36
  - M\_B DQ37 BF11 SB\_DQ\_37
  - M\_B DQ38 BF8 SB\_DQ\_38
  - M\_B DQ39 BG7 SB\_DQ\_39
  - M\_B DQ40 BC5 SB\_DQ\_40
  - M\_B DQ41 BC6 SB\_DQ\_41
  - M\_B DQ42 AY3 SB\_DQ\_42
  - M\_B DQ43 AY1 SB\_DQ\_43
  - M\_B DQ44 BF6 SB\_DQ\_44
  - M\_B DQ45 BF5 SB\_DQ\_45
  - M\_B DQ46 BA1 SB\_DQ\_46
  - M\_B DQ47 BC3 SB\_DQ\_47
  - M\_B DQ48 AV2 SB\_DQ\_48
  - M\_B DQ49 AU3 SB\_DQ\_49
  - M\_B DQ50 AR3 SB\_DQ\_50
  - M\_B DQ51 AN2 SB\_DQ\_51
  - M\_B DQ52 AV2 SB\_DQ\_52
  - M\_B DQ53 AV1 SB\_DQ\_53
  - M\_B DQ54 AP3 SB\_DQ\_54
  - M\_B DQ55 AR1 SB\_DQ\_55
  - M\_B DQ56 AL1 SB\_DQ\_56
  - M\_B DQ57 AL2 SB\_DQ\_57
  - M\_B DQ58 AJ1 SB\_DQ\_58
  - M\_B DQ59 AH1 SB\_DQ\_59
  - M\_B DQ60 AM2 SB\_DQ\_60
  - M\_B DQ61 AM3 SB\_DQ\_61
  - M\_B DQ62 AH3 SB\_DQ\_62
  - M\_B DQ63 AJ3 SB\_DQ\_63

**DDR SYSTEM MEMORY B**

- SB\_BS\_0 BC16 M\_B BS#0
- SB\_BS\_1 BB17 M\_B BS#1
- SB\_BS\_2 BB33 M\_B BS#2
- SB\_RAS# AU17 M\_B RAS#
- SB\_CAS# BG16 M\_B CAS#
- SB\_WE# BF14 M\_B WE#
- SB\_DM\_0 AM47 M\_B DM0
- SB\_DM\_1 AY47 M\_B DM1
- SB\_DM\_2 BC40 M\_B DM2
- SB\_DM\_3 BF35 M\_B DM3
- SB\_DM\_4 BG11 M\_B DM4
- SB\_DM\_5 BA3 M\_B DM5
- SB\_DM\_6 AP1 M\_B DM6
- SB\_DM\_7 AK2 M\_B DM7
- SB\_DQS\_0 AL47 M\_B DQS0
- SB\_DQS\_1 AY48 M\_B DQS1
- SB\_DQS\_2 BG41 M\_B DQS2
- SB\_DQS\_3 BG37 M\_B DQS3
- SB\_DQS\_4 BH9 M\_B DQS4
- SB\_DQS\_5 BB2 M\_B DQS5
- SB\_DQS\_6 AU1 M\_B DQS6
- SB\_DQS\_7 AN6 M\_B DQS7
- SB\_DQS#\_0 AV47 M\_B DQS#0
- SB\_DQS#\_1 BH41 M\_B DQS#1
- SB\_DQS#\_2 BH37 M\_B DQS#2
- SB\_DQS#\_3 BG9 M\_B DQS#3
- SB\_DQS#\_4 BC2 M\_B DQS#4
- SB\_DQS#\_5 AT2 M\_B DQS#5
- SB\_DQS#\_6 AN5 M\_B DQS#6
- SB\_DQS#\_7 AV17 M\_B A0
- SB\_MA\_0 BA25 M\_B A1
- SB\_MA\_1 BC25 M\_B A2
- SB\_MA\_2 AU25 M\_B A3
- SB\_MA\_3 AV25 M\_B A4
- SB\_MA\_4 BB28 M\_B A5
- SB\_MA\_5 AU28 M\_B A6
- SB\_MA\_6 AW28 M\_B A7
- SB\_MA\_7 AT33 M\_B A8
- SB\_MA\_8 BC33 M\_B A9
- SB\_MA\_9 BB16 M\_B A10
- SB\_MA\_10 AW33 M\_B A11
- SB\_MA\_11 AY33 M\_B A12
- SB\_MA\_12 BH15 M\_B A13
- SB\_MA\_13 AU33 M\_B A14
- M\_B\_BS#0 (12,13)
- M\_B\_BS#1 (12,13)
- M\_B\_BS#2 (12,13)
- M\_B\_RAS# (12,13)
- M\_B\_CAS# (12,13)
- M\_B\_WE# (12,13)
- M\_B\_DM[7:0] (13)
- M\_B\_DQS[7:0] (13)
- M\_B\_DQS#[7:0] (13)
- M\_B\_A[14:0] (12,13)

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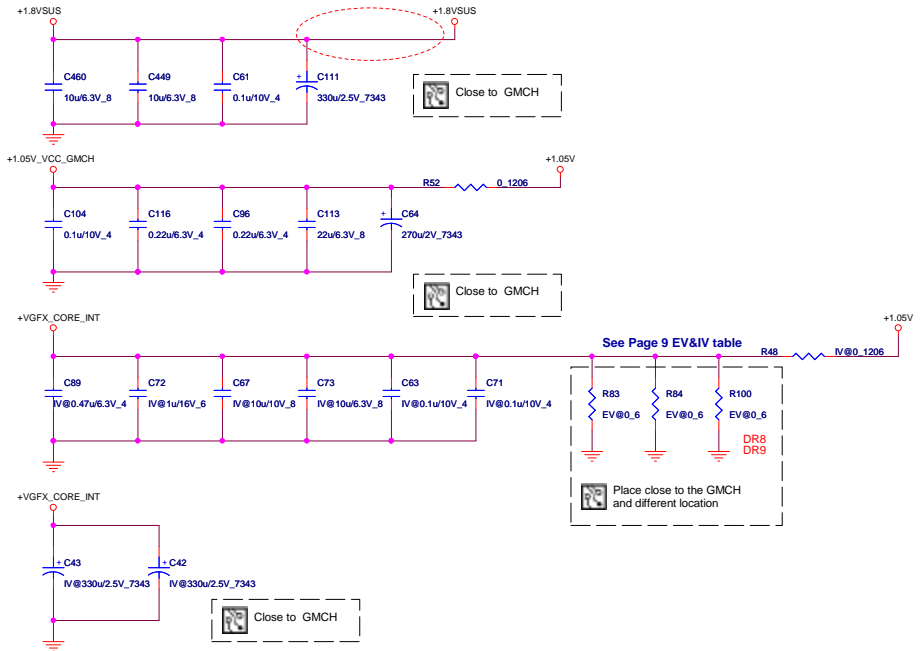
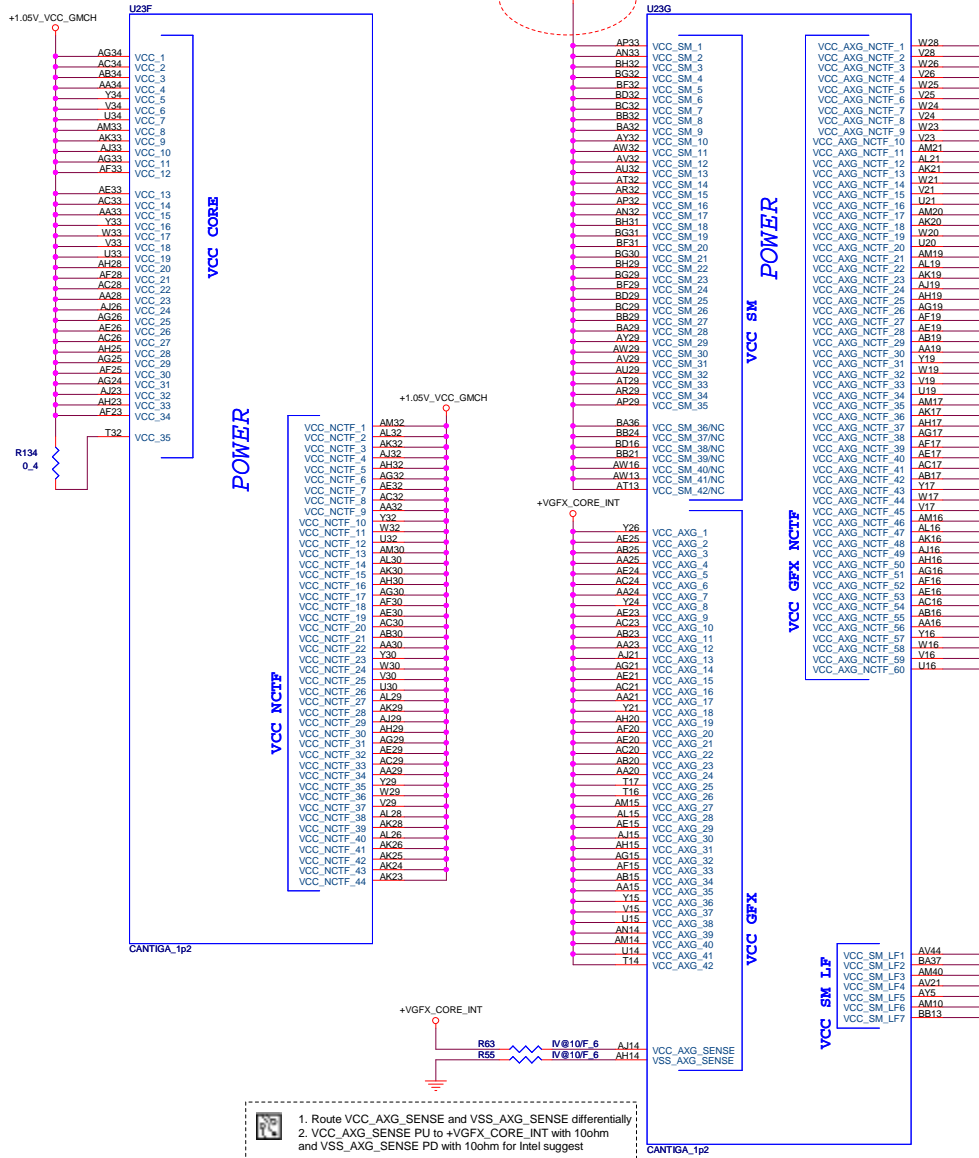
**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**

Size	Document Number	Rev
	CLK_GEN/ CK505	1A
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BOM Option Table	
Reference	Description
IV@	INT VGA
EV@	EXT VGA

12/19 REV\_2A Chanhe net to +1.8VSUS

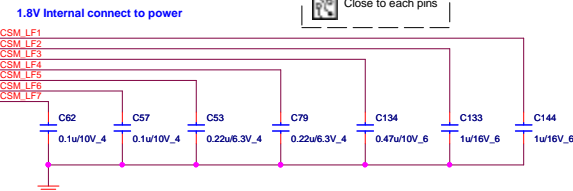
12/19 REV\_2A Del R101



**NB Power Status and max current table(1/3)**

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDR1-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)  
 (See NB EDS Rev:1.0 Section 12.2 for DC voltage)



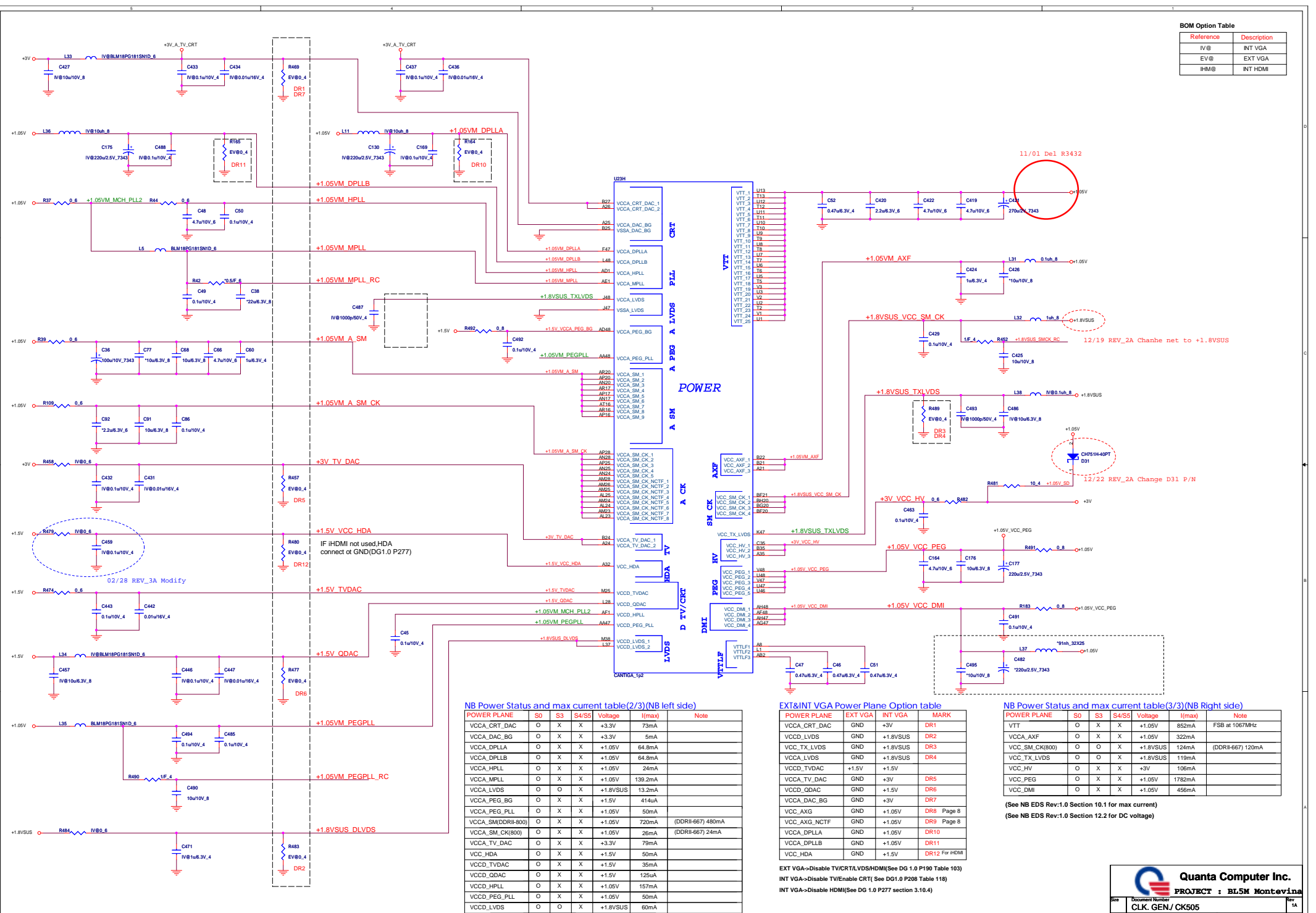
1. Route VCC\_AXG\_SENSE and VSS\_AXG\_SENSE differentially.  
 2. VCC\_AXG\_SENSE PU to +VGFX\_CORE\_INT with 10ohm and VSS\_AXG\_SENSE PD with 10ohm for Intel suggest

**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**  
**CLK\_GEN / CK505**  
 Date: Tuesday, March 04, 2008 Sheet 6 of 37



**BOM Option Table**

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI



**NB Power Status and max current table(2/3)(NB left side)**

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCA_CRT_DAC	O	X	X	+3.3V	73mA	
VCCA_DAC_BG	O	X	X	+3.3V	5mA	
VCCA_DPLLA	O	X	X	+1.05V	64.8mA	
VCCA_DPLLB	O	X	X	+1.05V	64.8mA	
VCCA_HPLL	O	X	X	+1.05V	24mA	
VCCA_MPLL	O	X	X	+1.05V	139.2mA	
VCCA_LVDS	O	O	X	+1.8VSUS	13.2mA	
VCCA_PEG_BG	O	X	X	+1.5V	414uA	
VCCA_PEG_PLL	O	X	X	+1.05V	50mA	
VCCA_SM(DDR1-800)	O	X	X	+1.05V	720mA	(DDR1-667) 480mA
VCCA_SM_CK(800)	O	X	X	+1.05V	26mA	(DDR1-667) 24mA
VCCA_TV_DAC	O	X	X	+3.3V	79mA	
VCC_HDA	O	X	X	+1.5V	50mA	
VCCD_TV_DAC	O	X	X	+1.5V	35mA	
VCCD_QDAC	O	X	X	+1.5V	125uA	
VCCD_HPLL	O	X	X	+1.05V	157mA	
VCCD_PEG_PLL	O	X	X	+1.05V	50mA	
VCCD_LVDS	O	O	X	+1.8VSUS	60mA	

**EXT&INT VGA Power Plane Option table**

POWER PLANE	EXT VGA	INT VGA	MARK
VCCA_CRT_DAC	GND	+3V	DR1
VCCA_LVDS	GND	+1.8VSUS	DR2
VCC_TX_LVDS	GND	+1.8VSUS	DR3
VCCA_TX_LVDS	GND	+1.8VSUS	DR4
VCCD_TV_DAC	+1.5V	+1.5V	
VCCA_TV_DAC	GND	+3V	DR5
VCCD_QDAC	GND	+1.5V	DR6
VCCA_DAC_BG	GND	+3V	DR7
VCCA_A_XG	GND	+1.05V	DR8 Page 8
VCCA_A_XG_NCTF	GND	+1.05V	DR9 Page 8
VCCA_DPLLA	GND	+1.05V	DR10
VCCA_DPLLB	GND	+1.05V	DR11
VCC_HDA	GND	+1.5V	DR12 For IHDMI

**NB Power Status and max current table(3/3)(NB Right side)**

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VTT	O	X	X	+1.05V	852mA	FSB at 1067MHz
VCCA_A_XF	O	X	X	+1.05V	322mA	
VCC_SM_CK(800)	O	O	X	+1.8VSUS	124mA	(DDR1-667) 120mA
VCC_TX_LVDS	O	O	X	+1.8VSUS	119mA	
VCC_HV	O	X	X	+3V	106mA	
VCC_PEG	O	X	X	+1.05V	1782mA	
VCC_DMI	O	X	X	+1.05V	456mA	

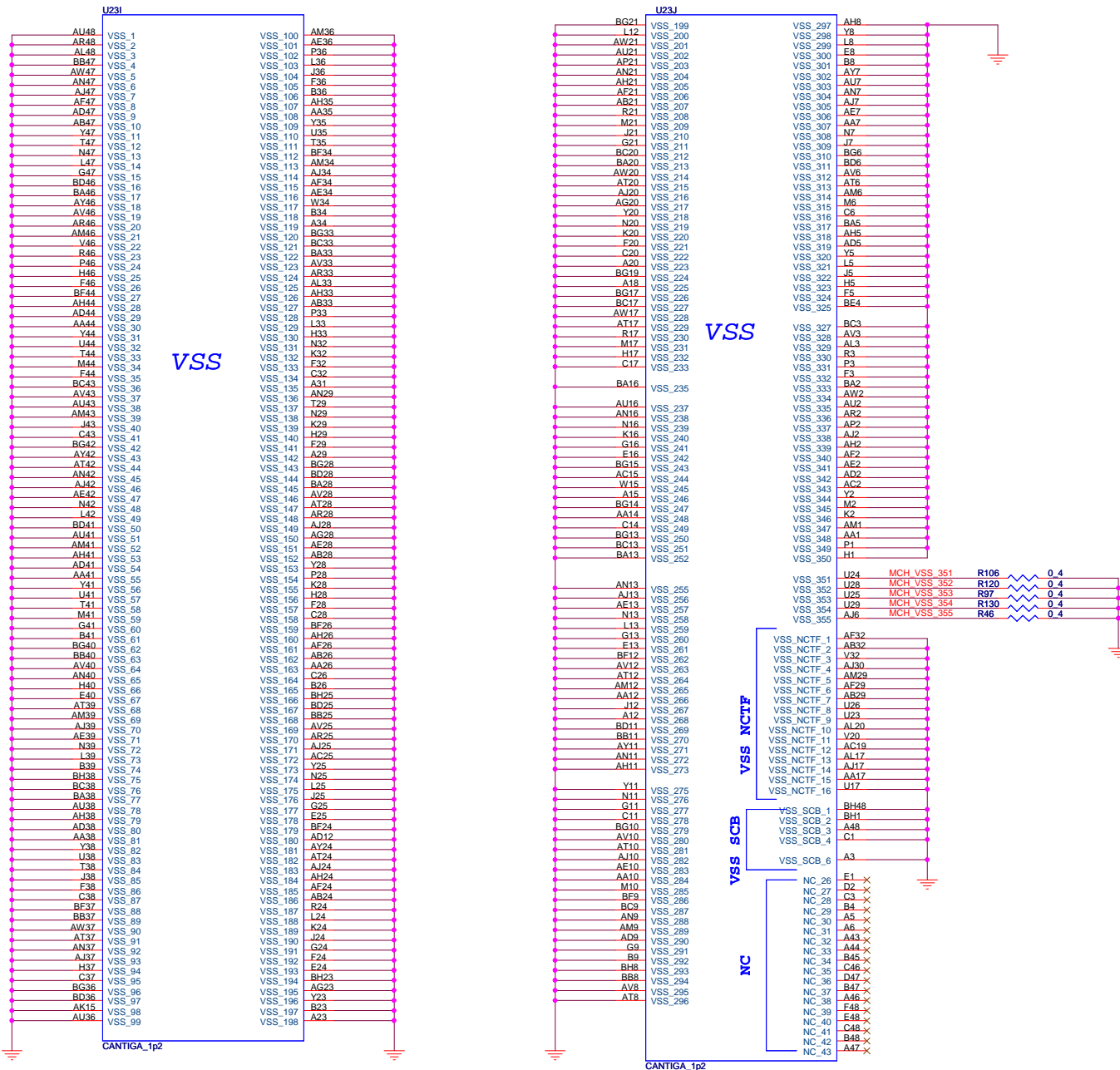
(See NB EDS Rev:1.0 Section 10.1 for max current)  
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

EXT VGA->Disable TV/CRT/LVDS/HDMI(See Dg 1.0 P190 Table 103)  
INT VGA->Disable TV/Enable CRT(See Dg1.0 P208 Table 118)  
INT VGA->Disable HDMI(See Dg 1.0 P277 section 3.10.4)

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PROJECT : BLSM Montevina  
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Sheet 9 of 37

BOM Option Table

Reference	Description
N/A	N/A



**Quanta Computer Inc.**

**PROJECT : BL5M Montevina**

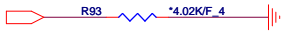
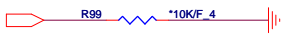
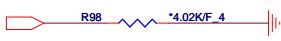

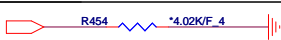
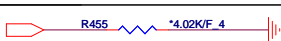
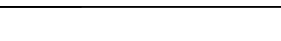
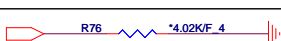
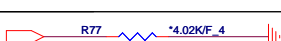
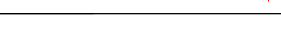
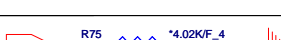
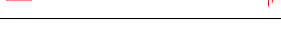
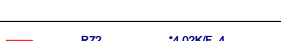
Size	Document Number	Rev
	CLK_GEN / CK505	1A
Date:	Tuesday, March 04, 2008	Sheet 10 of 37

# North Bridge Strap Pin Configuration Table

(See DG 1.0 P295 Table 184)  
(See NB EDS 1.0 P187 Table 74)


BOM Option Table

Reference	Description
N/A	N/A

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	(6) MCH_CFG_5 	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	(6) MCH_CFG_6 	
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	(6) MCH_CFG_7 	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	(6) MCH_CFG_9 	
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)	(6) MCH_CFG_10 	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	(6) MCH_CFG_12 	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	(6) MCH_CFG_13 	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	(6) MCH_CFG_16 	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	(6) MCH_CFG_19 	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	(6) MCH_CFG_20 	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	(6,20) SDVO_CTRLDATA 	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	(6,18) INT_LVDS_EDIDDATA 	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	(6) DDPC_CTRLDATA 	

## Enable iTPM Table

PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin



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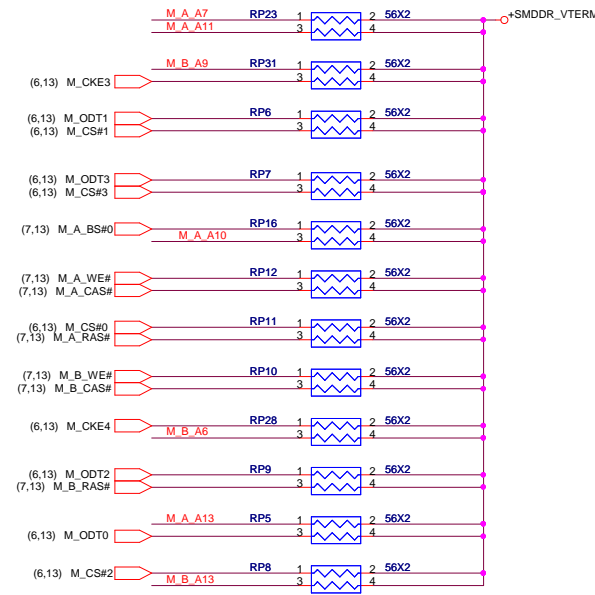
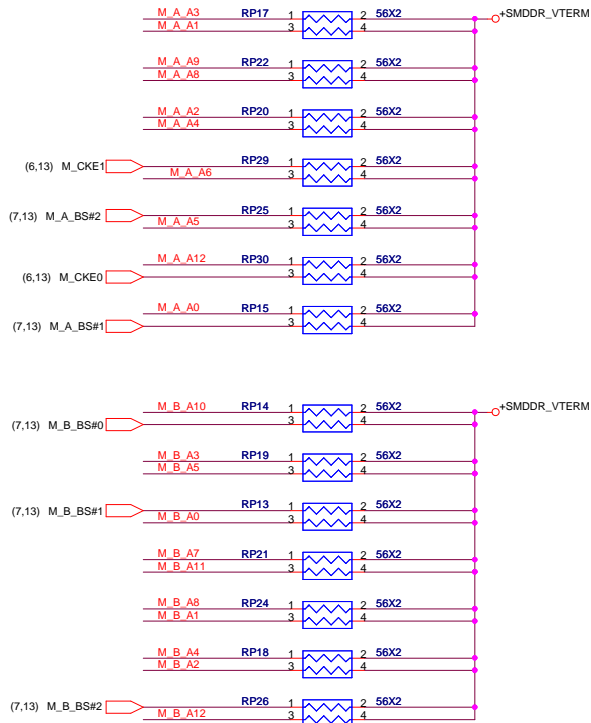
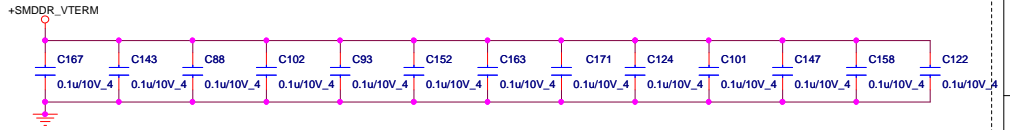
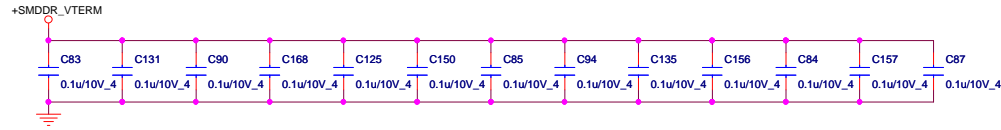
Size	Document Number	Rev
Date: Monday, March 10, 2008	CLK. GEN./ CK505	1A
Sheet	11	of 37


# DDR2 Dual channel A/B PU

## DDRII A CHANNEL

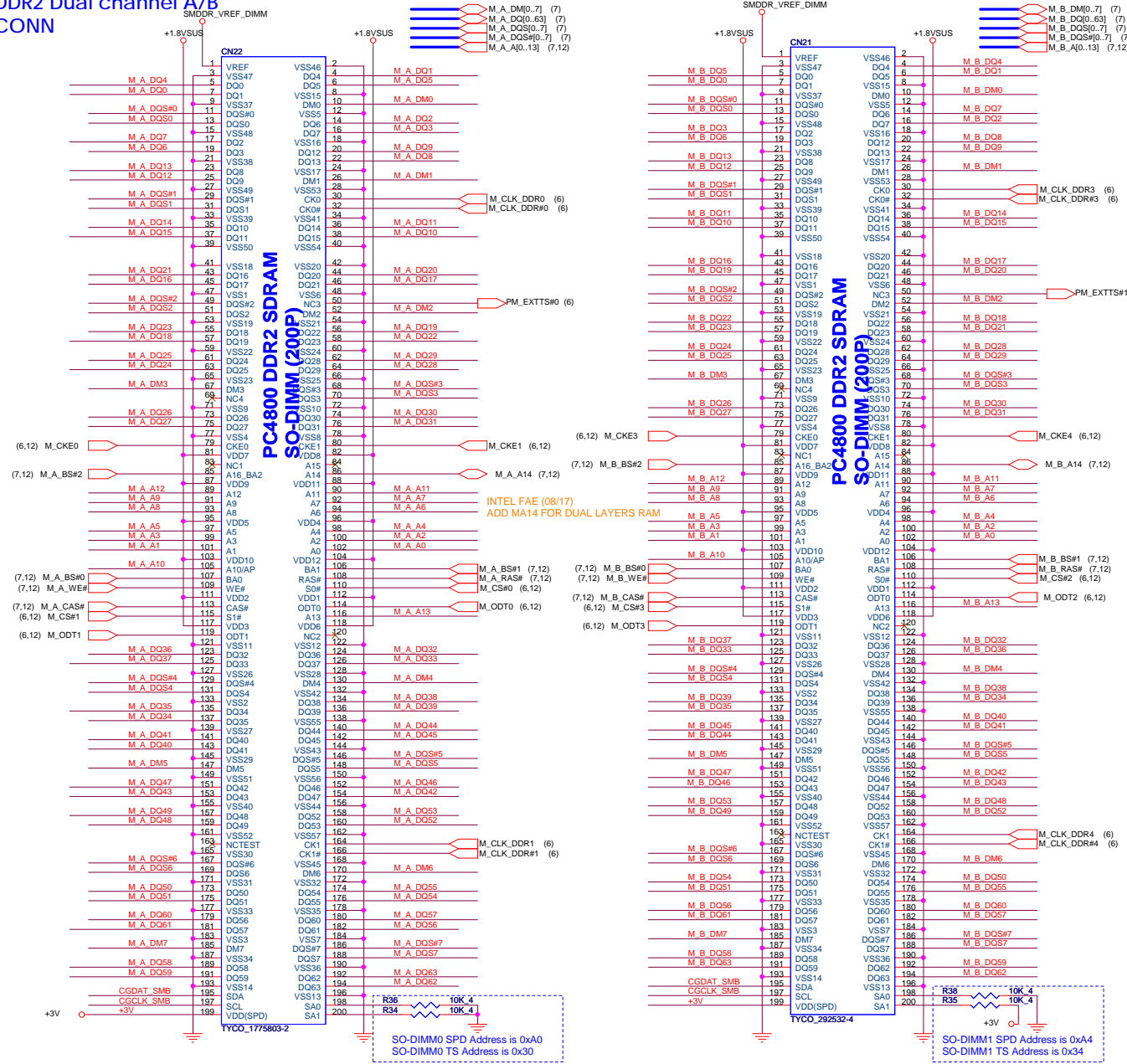
M\_A\_A[13..0] M\_A\_A[13..0] (7,13)  
 M\_B\_A[13..0] M\_B\_A[13..0] (7,13)

## DDRII B CHANNEL



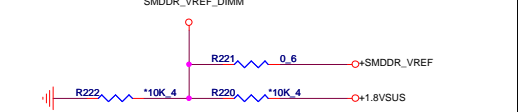
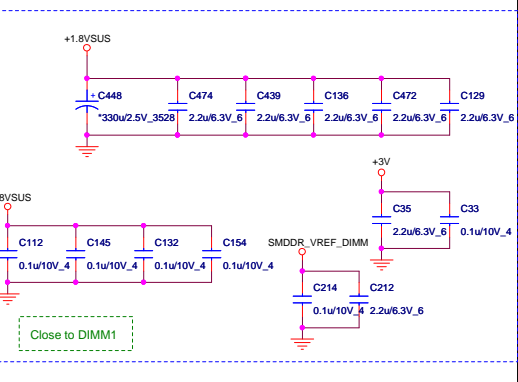
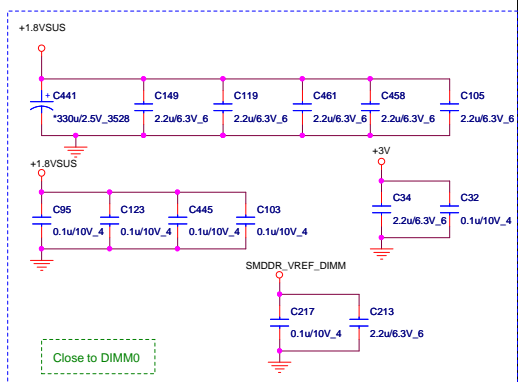
 <b>Quanta Computer Inc.</b> <b>PROJECT : BL5M Montevina</b>		
Size	Document Number	Rev
	<b>DDR RES. ARRAY</b>	<b>1A</b>
Date	Monday, March 10, 2008	Sheet 12 of 37

**DDR2 Dual channel A/B  
CONN**



**Standard Type H: 6.5mm**  
CLOCK 0,1  
CKE 0,1

**Standard Type H: 11mm**  
CLOCK 3,4  
CKE 2,3



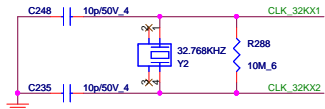
SO-DIMMO SPD Address is 0xA0  
SO-DIMMO TS Address is 0x30

SO-DIMM1 SPD Address is 0xA4  
SO-DIMM1 TS Address is 0x34

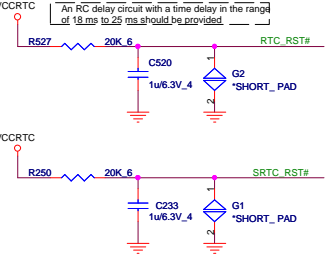
**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**

Size	Document Number	Rev
	<b>DDR SO-DIMM(200P)</b>	1A
Date:	Monday, March 10, 2008	Sheet 13 of 37

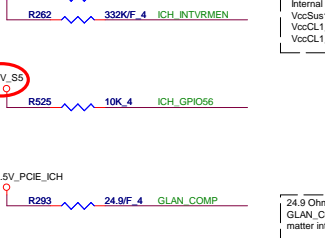
RTC  
CRYSTAL



RESET  
JUMP



VCCRTC



(DG 1.0 Table-292)  
Internal VRM enabled for VccSus1\_05, VccSus1\_5, VccCL1\_5, VccLAN1\_05 and VccCL1\_05.

HD Audio I/F(CODEC& IHDMI)



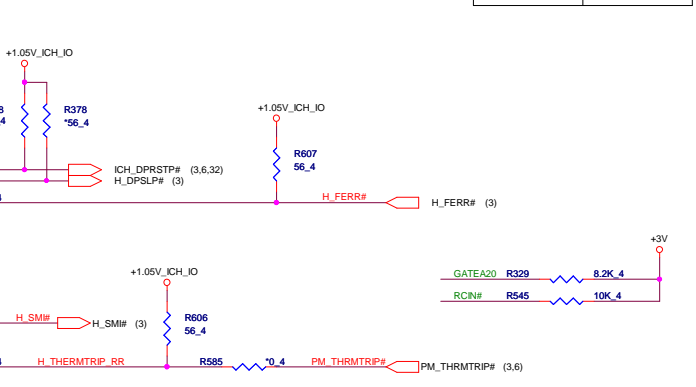
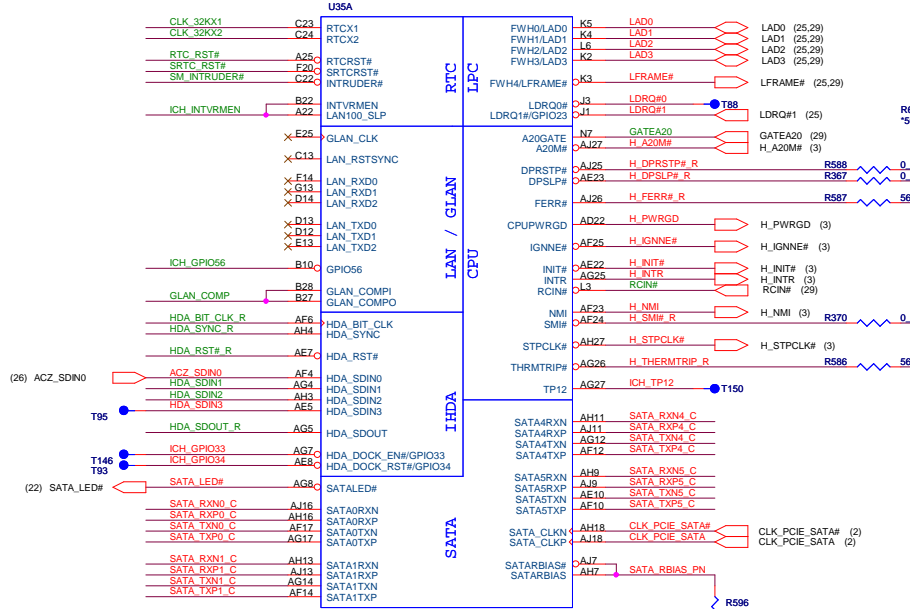
South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD		
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.		
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU			
TP3	XOR Chain Entrance	PWROK	ICH_TP3	Description		
			HDA_SDOUT	Description		
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0	0	RSVD	(16) ICH_TP3  ICH_TP3 R264 *1K_4
			0	1	Enter XOR Chain	
			1	0	Normal operation(Default)	HDA_SDOUT_R R582 *1K_4 +3V_HDA_IO_ICH
			1	1	Set PCIe port config bit 1	PU +1.5V

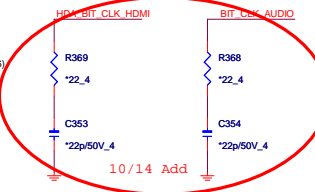
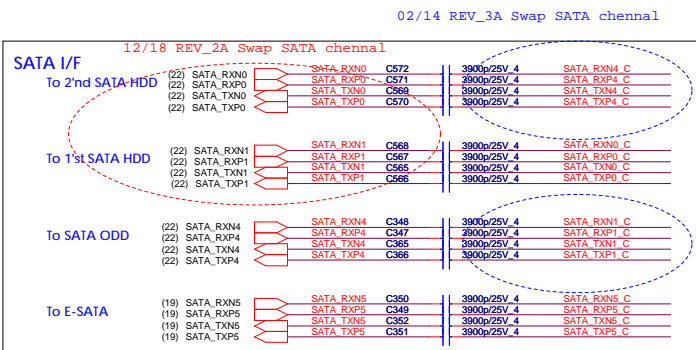
Layout note:  
DPRSTP#, Delay Chain (SB+Power+Nb+CPU)

BOM Option Table

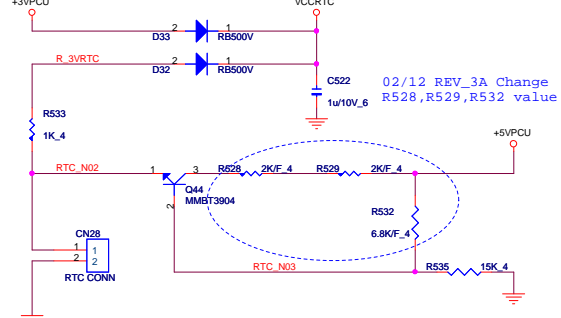
Reference	Description
IHM@	INT HDMI



Layout note:  
PU R needs to be placed within 2" of ICH9-M, series R must be placed within 2" of PU R w/o stub.



RTC  
BATTERY

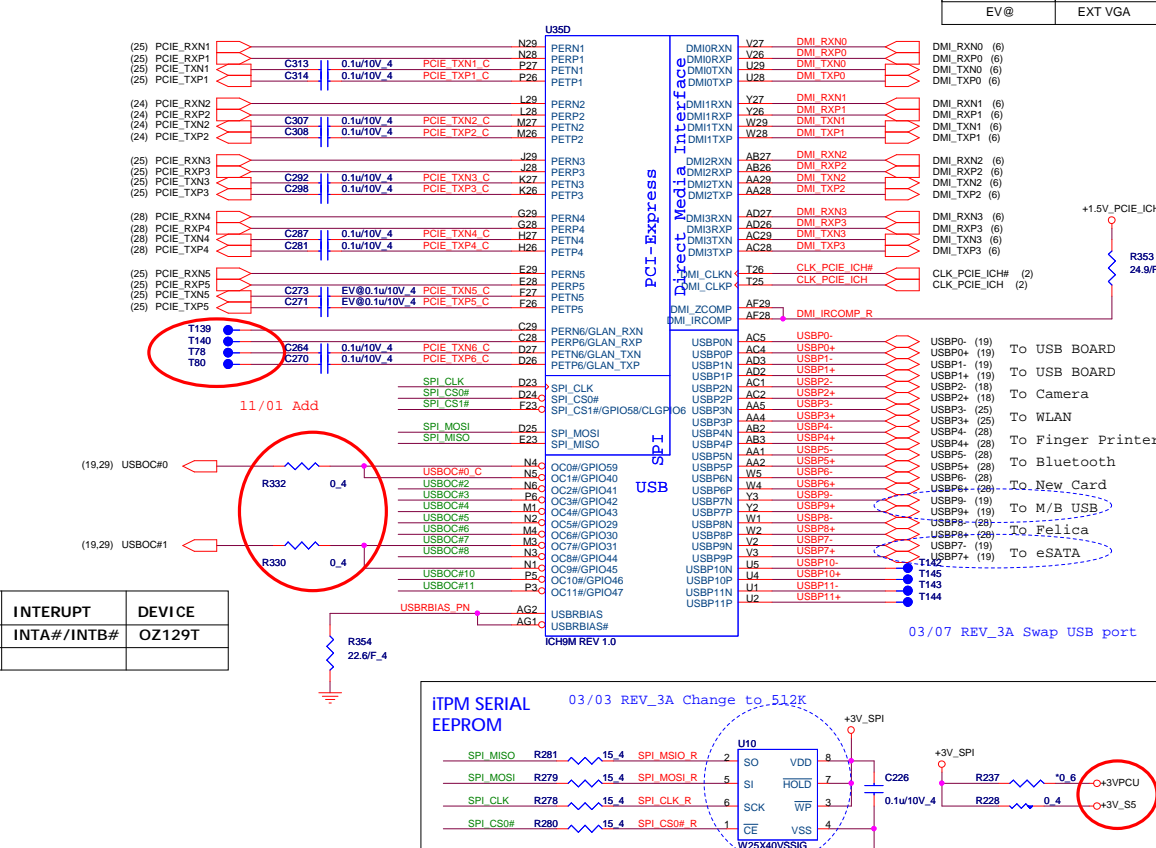
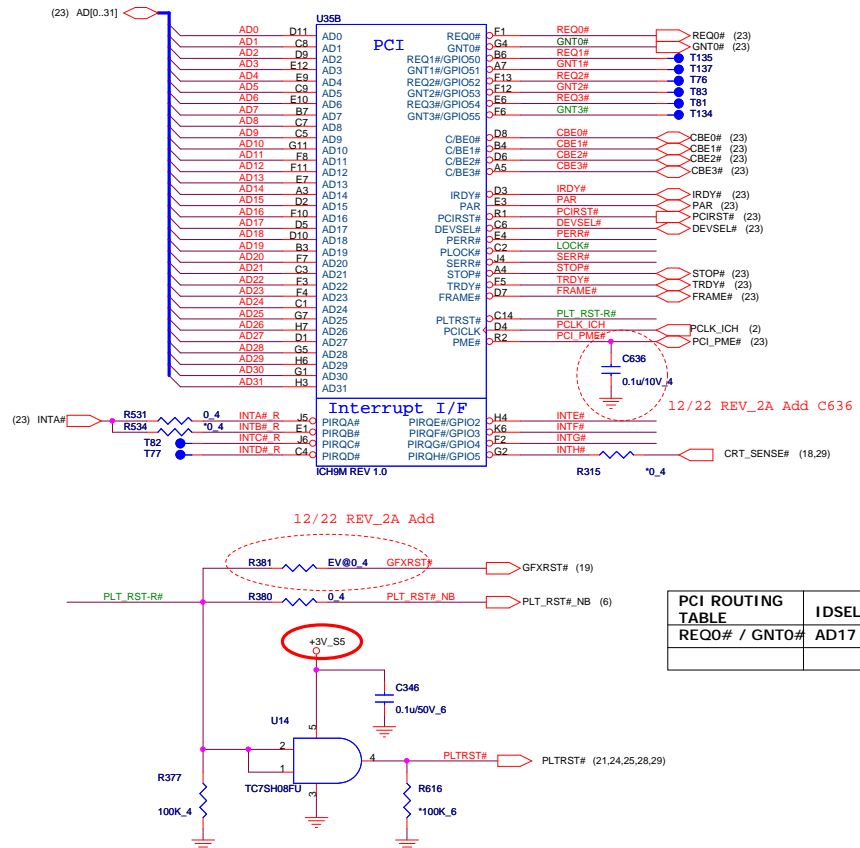


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Date: Monday, March 10, 2008 Sheet 14 of 37

PCI/PCI-E/USB/DMI/SPI

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

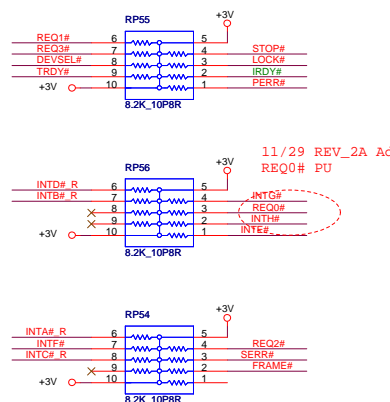


PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#/INTB#	OZ129T

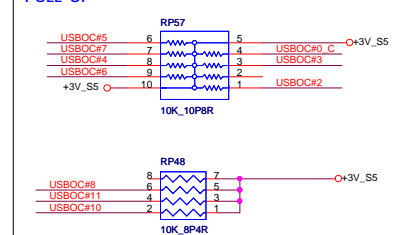
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD												
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0													
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default													
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default													
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R511 *1K_4												
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	Enable iTPM SPI_MOSI R295 *20K_4 >+3V_S5												
GNT0#	Boot BIOS Selection 0	PWROK	<table border="1"> <tr> <td>PC1L_GNT#0</td> <td>SPL_CS#1</td> <td>Boot Location</td> </tr> <tr> <td>0</td> <td>1</td> <td>SPI(Default)</td> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>LPC</td> </tr> </table>	PC1L_GNT#0	SPL_CS#1	Boot Location	0	1	SPI(Default)	1	0	PCI	1	1	LPC	GNT0# R304 *1K_4
PC1L_GNT#0	SPL_CS#1	Boot Location														
0	1	SPI(Default)														
1	0	PCI														
1	1	LPC														
SPL_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPL_CS1# R314 *1K_4												

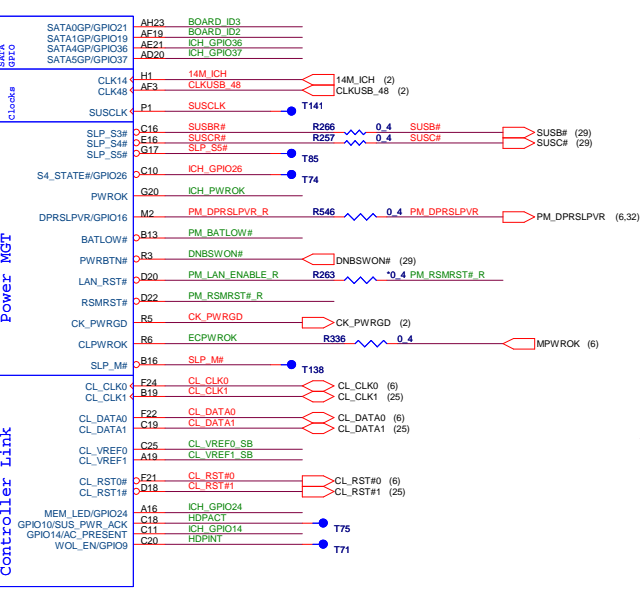
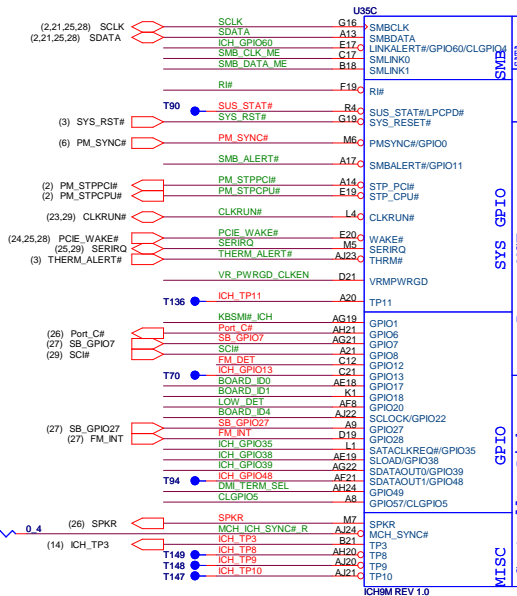
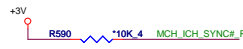
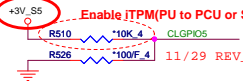
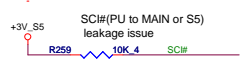
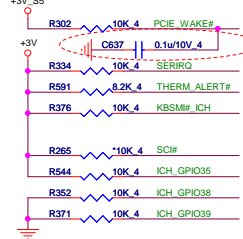
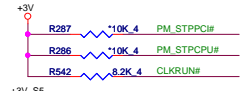
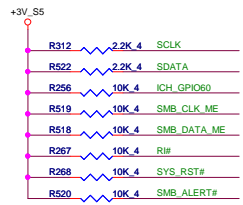
PCI PULL-UP



USBOC# PULL-UP

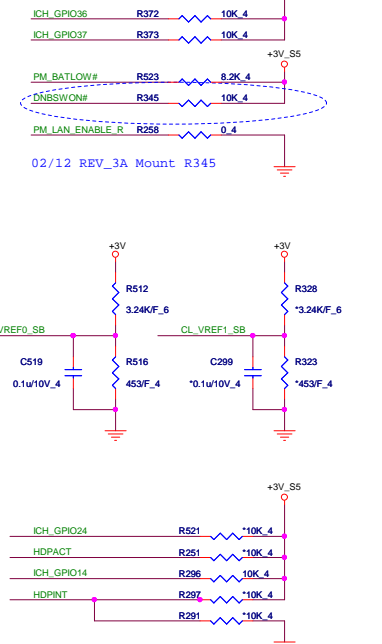


**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**  
 Size: Document Number: Rev 1A  
 CLK\_GEN / CK505  
 Date: Monday, March 10, 2008 Sheet 15 of 37



**BOM Option Table**

Reference	Description
N/A	N/A

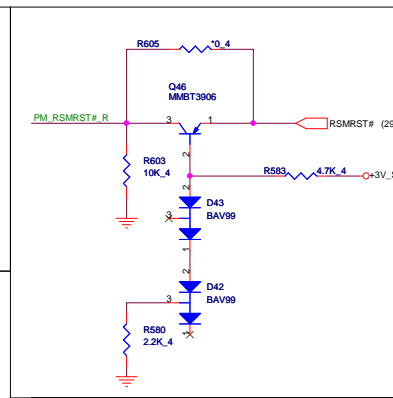
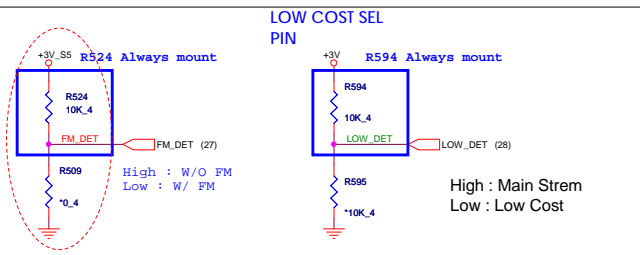
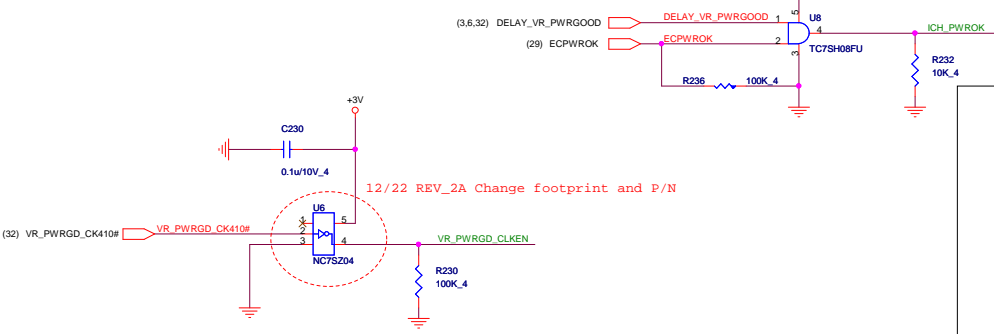


Enable ITPM(PU to PCU or S5?)  
11/29 REV\_2A DNI R510

12/22 REV\_2A Add C637

12/22 REV\_2A Change footprint and P/N

DELAY\_VR\_PWRGOOD need PU 2K to +3V.  
ZS2 PU at power side(NEEED CHECK PWR CKT)

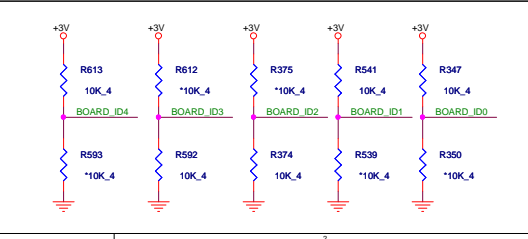


**South Bridge Strap Pin (3/3)**

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R324 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R589 *1K_4

**Board ID Table**

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel					H L
W/ G-SENSOR W/O G-SENSOR				H L	
W/ TV W/O TV			H L		
W/ HDMI W/O HDMI	H L				

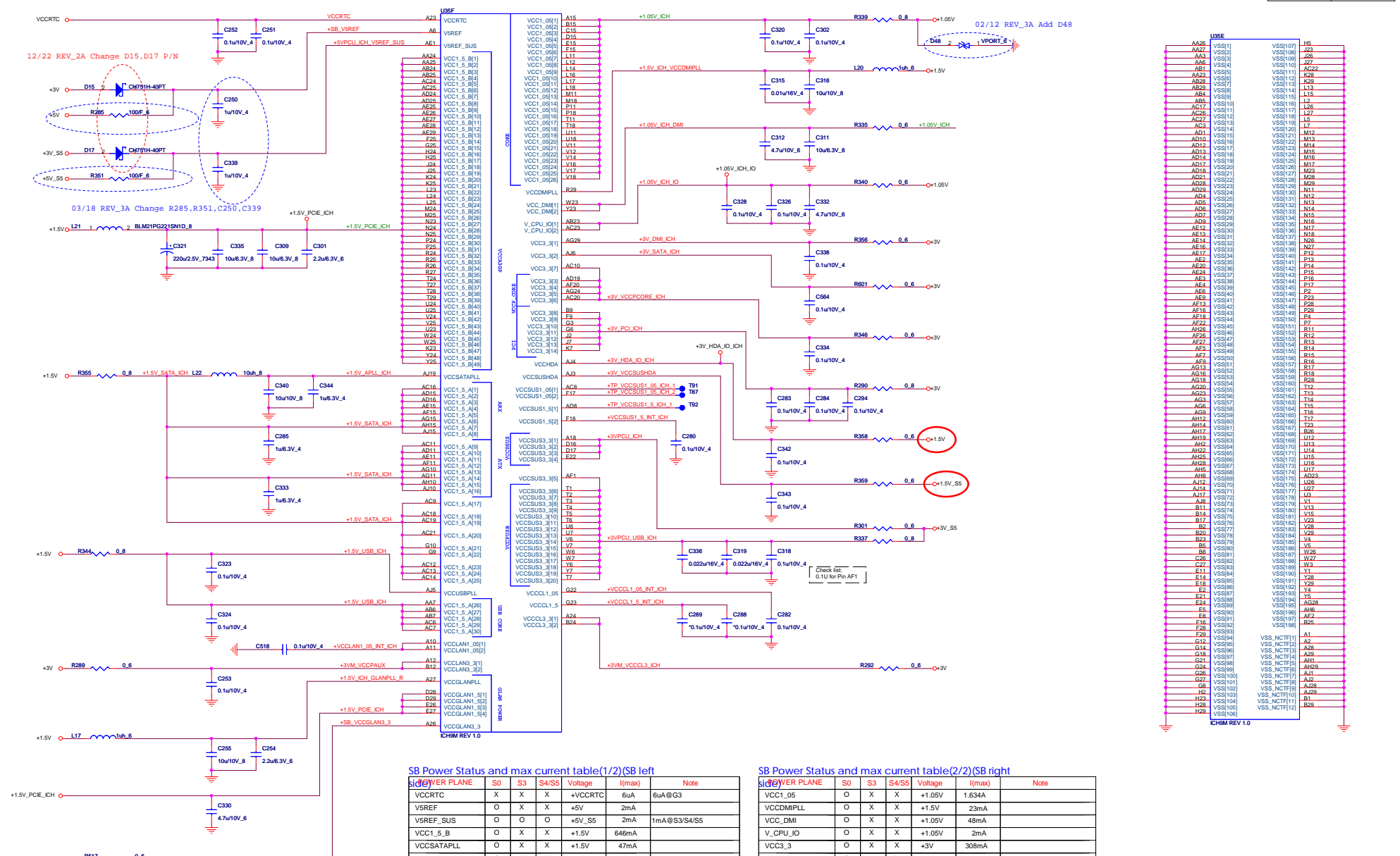


**Quanta Computer Inc.**  
PROJECT : BLSM Montevina  
CLK\_GEN/ CK505  
Rev 1A  
Date: Monday, March 17, 2008 Sheet 16 of 37



BOM Option Table

Reference	Description
N/A	N/A



**SB Power Status and max current table(1/2)(SB left)**

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCRTC	X	X	X	+VCCRTC	6uA	6uA@G3
VSREF	O	X	X	+5V	2mA	
VSREF_SUS	O	O	O	+5V_S5	2mA	1mA@S3/S4/S5
VCC1_5_B	O	X	X	+1.5V	648mA	
VCCSATAPLL	O	X	X	+1.5V	47mA	
VCC1_5_A	O	X	X	+1.5V	1,342A	
VCCUSBPLL	O	X	X	+1.5V_S5	11mA	
VCCLAN1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCLAN3_3	O	X	X	+3V	19mA	Tied to +3V, not +3VSUS
VCCGLANPLL	O	X	X	+1.5V	23mA	
VCCGLAN1_5	O	X	X	+1.5V	80mA	
VCCGLAN3_3	O	X	X	+3V	1mA	

**SB Power Status and max current table(2/2)(SB right)**

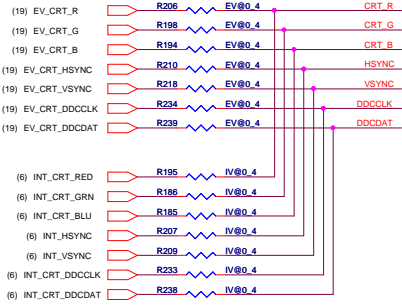
POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_05	O	X	X	+1.05V	1,634A	
VCCDMIPLL	O	X	X	+1.5V	23mA	
VCC_DMI	O	X	X	+1.05V	48mA	
V_CPU_IO	O	X	X	+1.05V	2mA	
VCC3_3	O	X	X	+3V	308mA	
VCCHDA	O	X	X	+1.5V	11mA	
VCCSUSHDA	O	O	O	+1.5V_S5	11mA	1mA@S3/S4/S5
VCCSUS1_05	O	O	O	+1.05V	X	Powered by Vcc1_05 in S0
VCCSUS1_5	O	O	O	+1.5V	X	Powered by Vcc1_5_A in S0
VCCSUS3_3	O	O	O	+3V/S5	212mA	52mA@S3/S4/S5
VCCCL1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCCL1_5	O	X	X	+1.5V	X	Powered by Vcc1_5_A in S0
VCCCL3_3	O	X	X	+3V	19mA	Tied to +3V, not +3VSUS

Note: VCCSUS1\_05, VCCSUS1\_5 are powered by VCCSUS3\_3 in S3/S4/S5

**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**

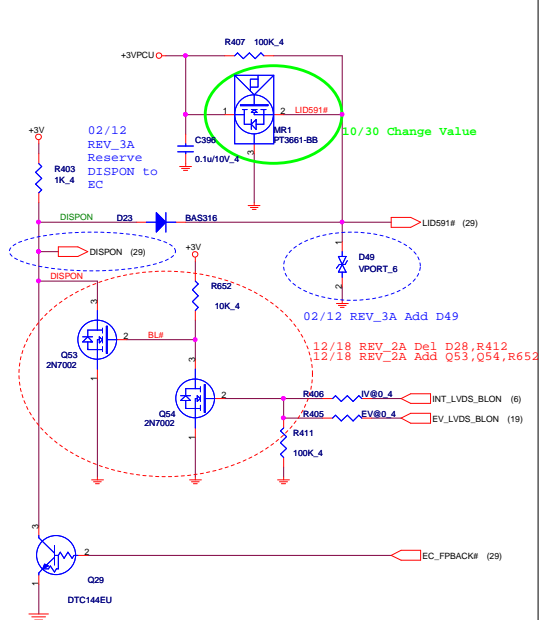
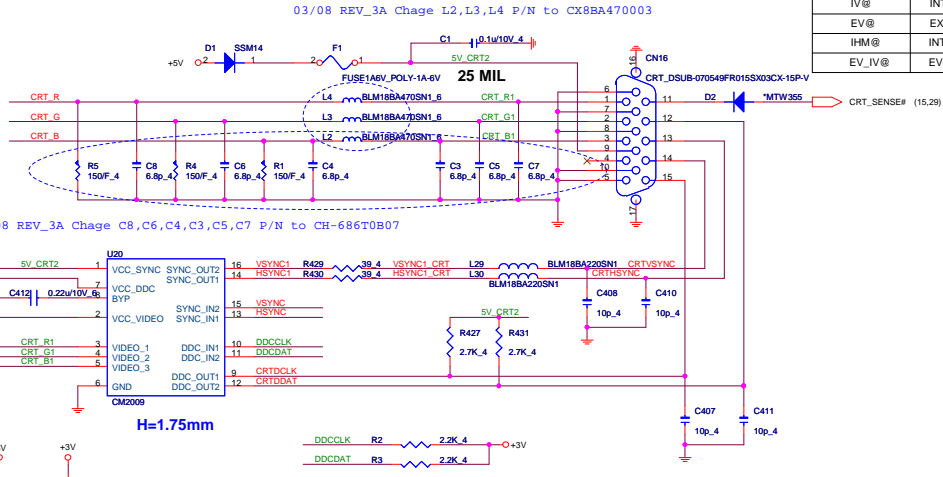
Size: \_\_\_\_\_ Document Number: \_\_\_\_\_ Rev: 1A  
 CLK\_GEN / CK505  
 Date: Tuesday, March 18, 2008 Sheet 17 of 37

# CRT PORT



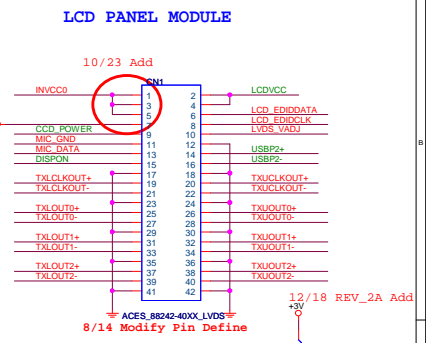
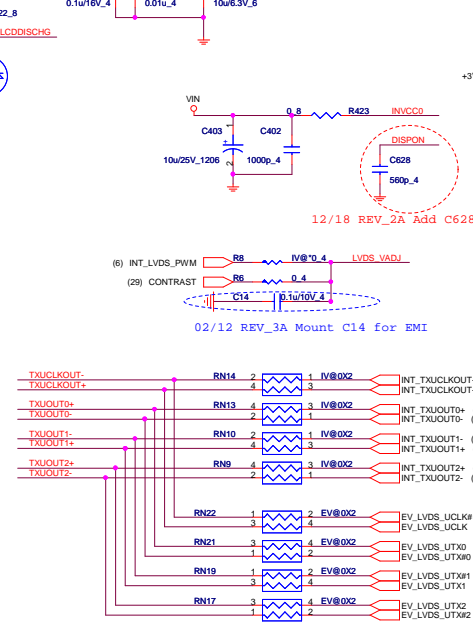
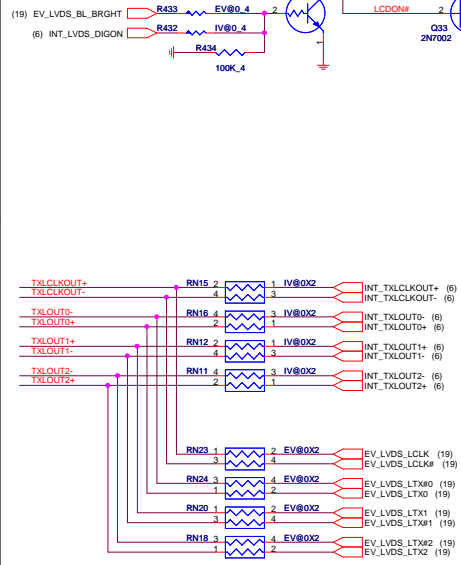
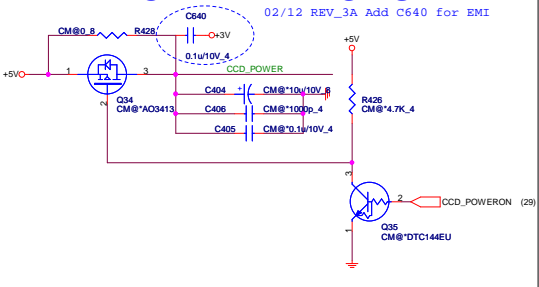
### BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. value



# HALL SENSOR

# CAMERA MODULE



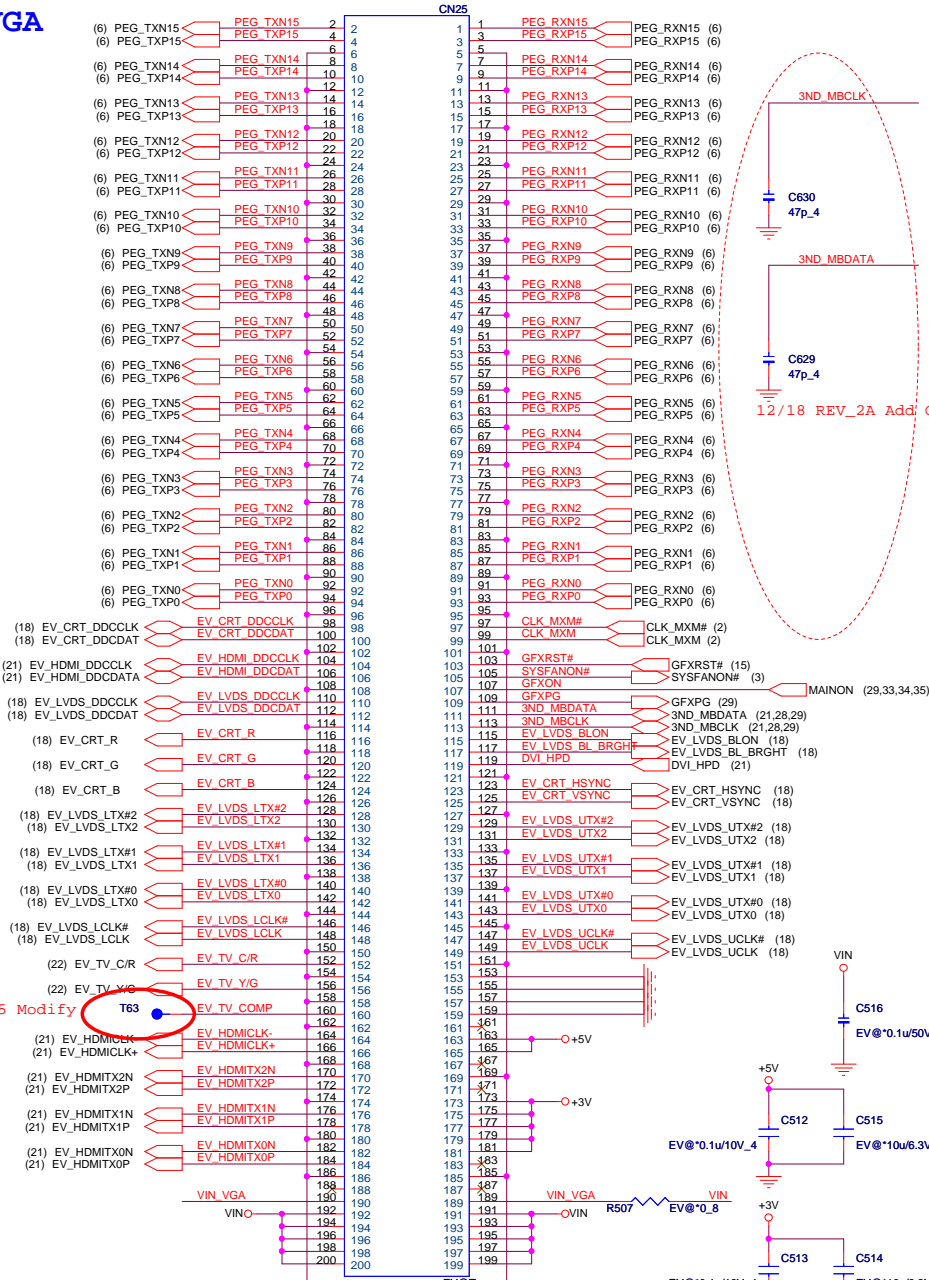
**Quanta Computer Inc.**

PROJECT : BLSM Montevina

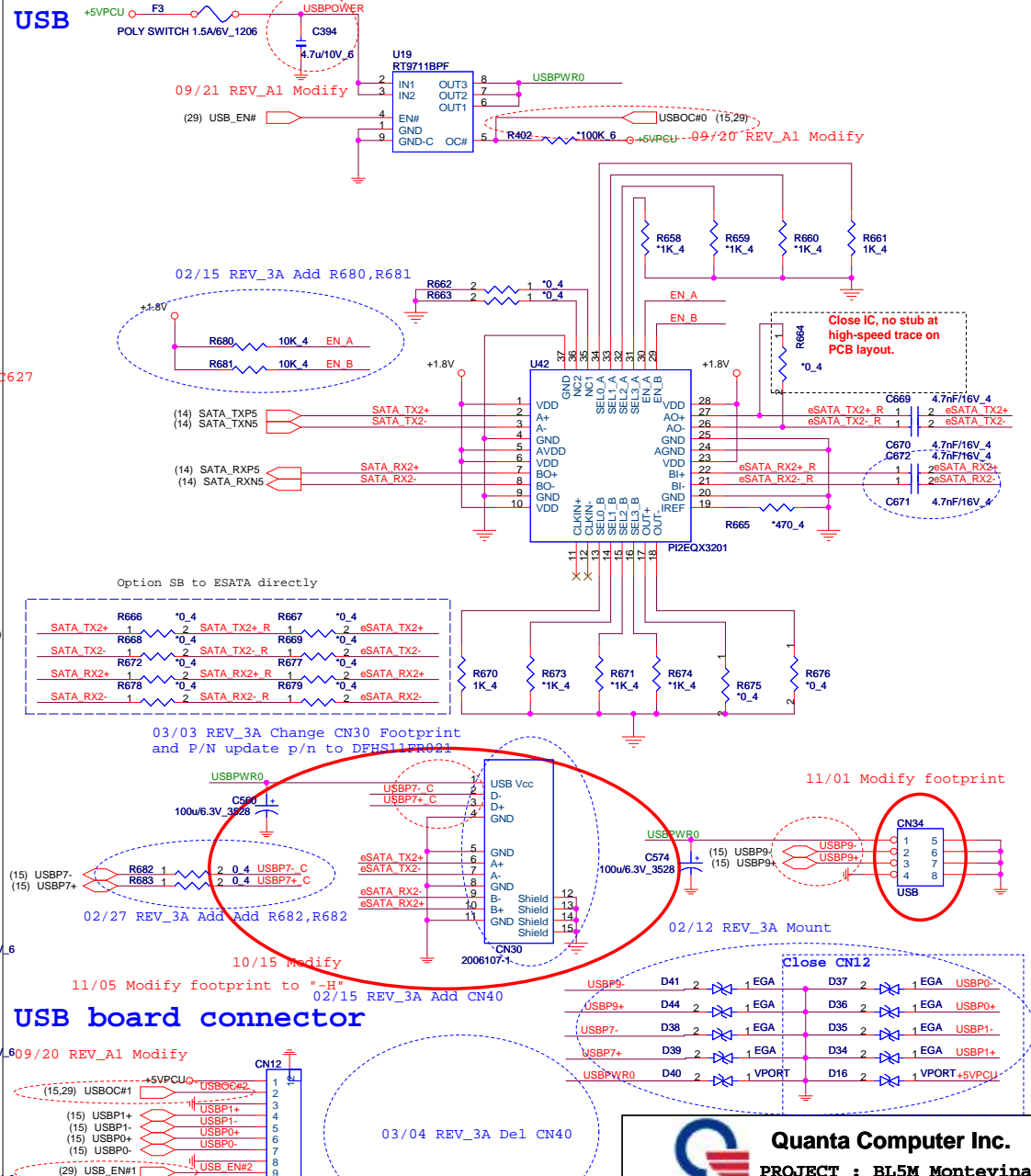
Size: Document Number  
LCD/CRT/LID/CAMERA

Date: Monday, March 10, 2008  
Sheet: 18 of 37

**VGA**



**USB**

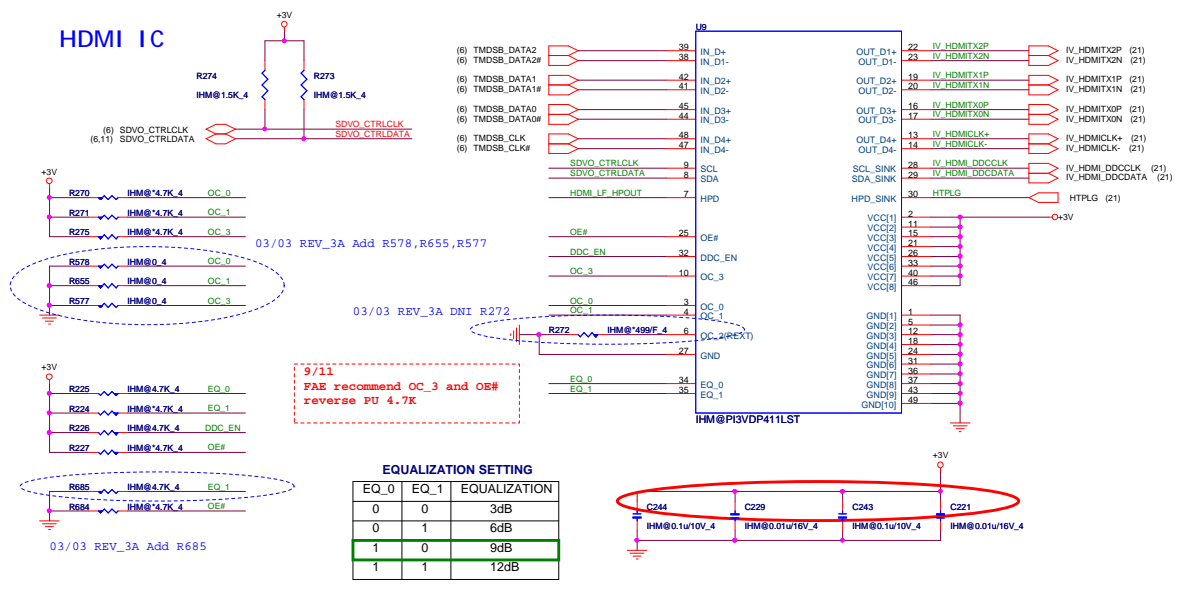


**USB board connector**

**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**

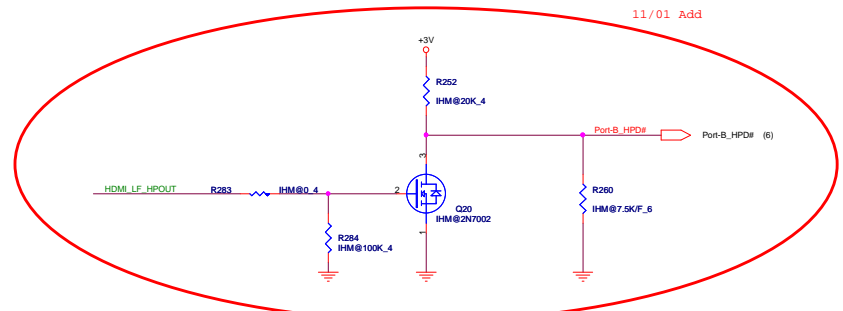
Size	Document Number	Rev
	<b>VGA CONNECTOR/USB/ESATA</b>	1A
Date:	Monday, March 10, 2008	Sheet 19 of 37

HDMI IC



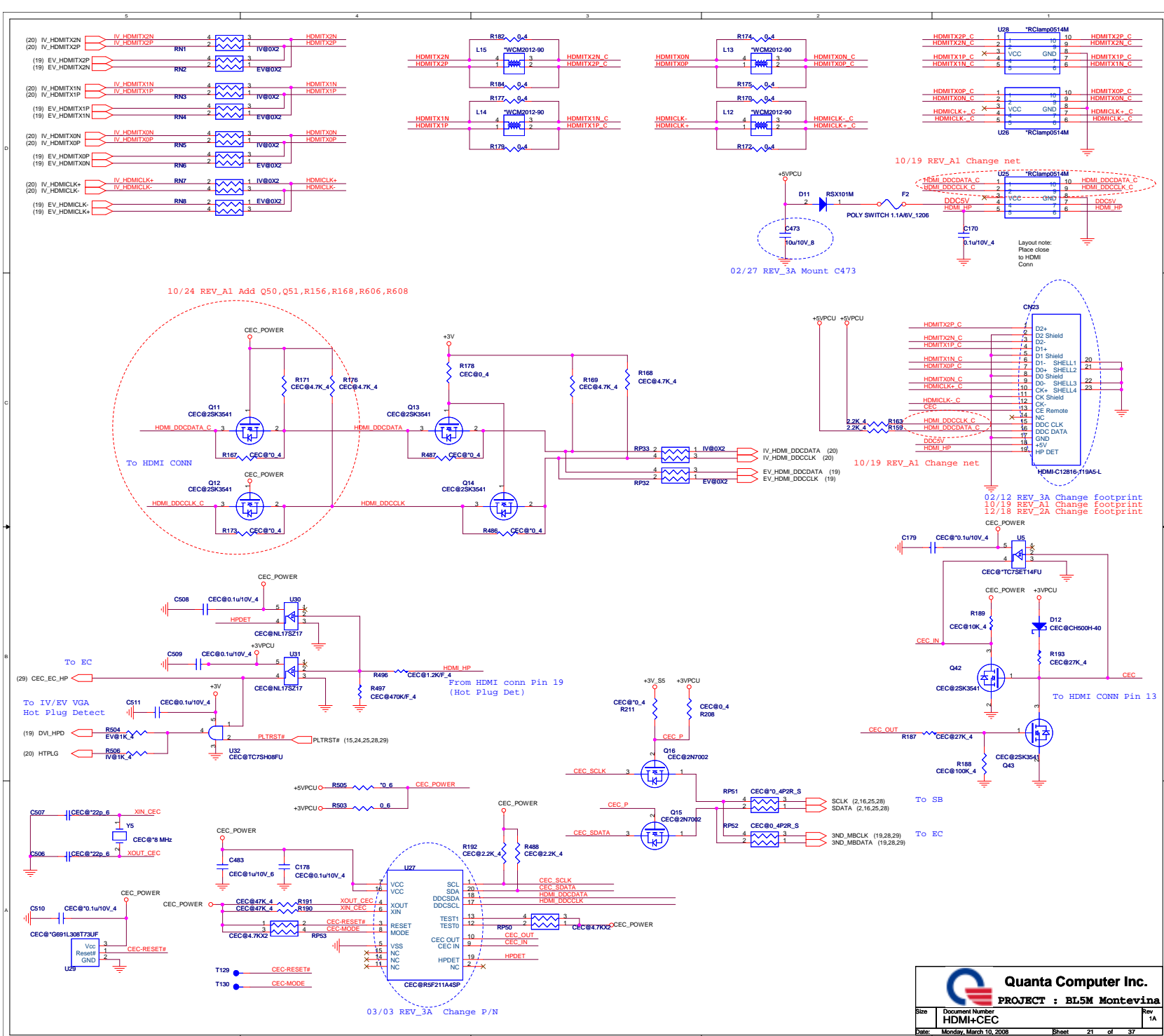
**EQUALIZATION SETTING**

EQ_0	EQ_1	EQUALIZATION
0	0	3dB
0	1	6dB
1	0	9dB
1	1	12dB



**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**

Size: Document Number: PI3VDP411ST(HDMI) Rev 1A  
 Date: Monday, March 17, 2008 Sheet 20 of 37

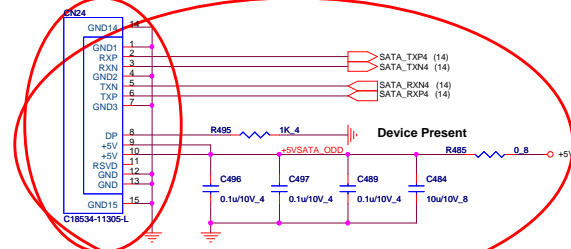


**Quanta Computer Inc.**  
**PROJECT : BLSM Montevina**

Size: Document Number  
**HDMI+CEC** Rev 1A

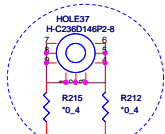
Date: Monday, March 16, 2009 Sheet 21 of 37

# SATA ODD



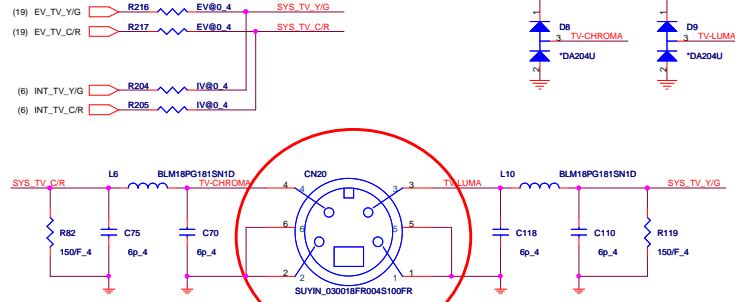
11/02 Modify Footprint

10/15 Add



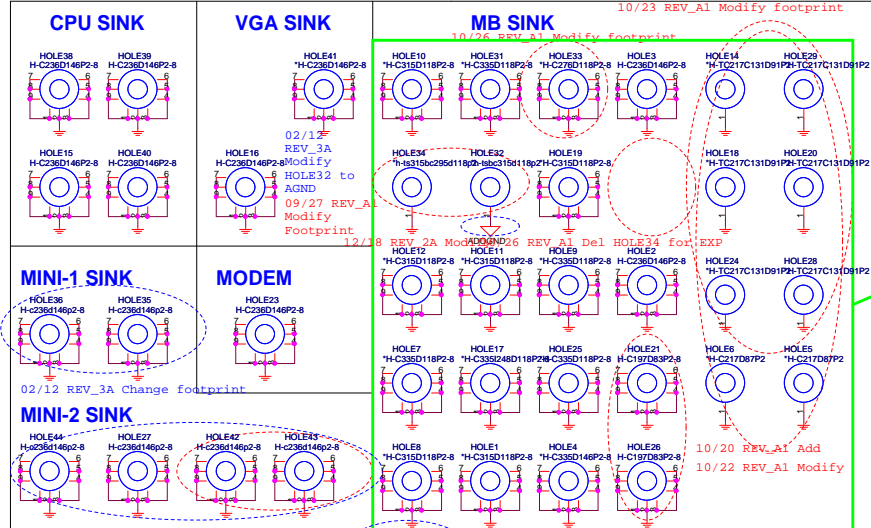
03/05 REV\_3A Reserve R215,R212 fro EMI

# TVOUT



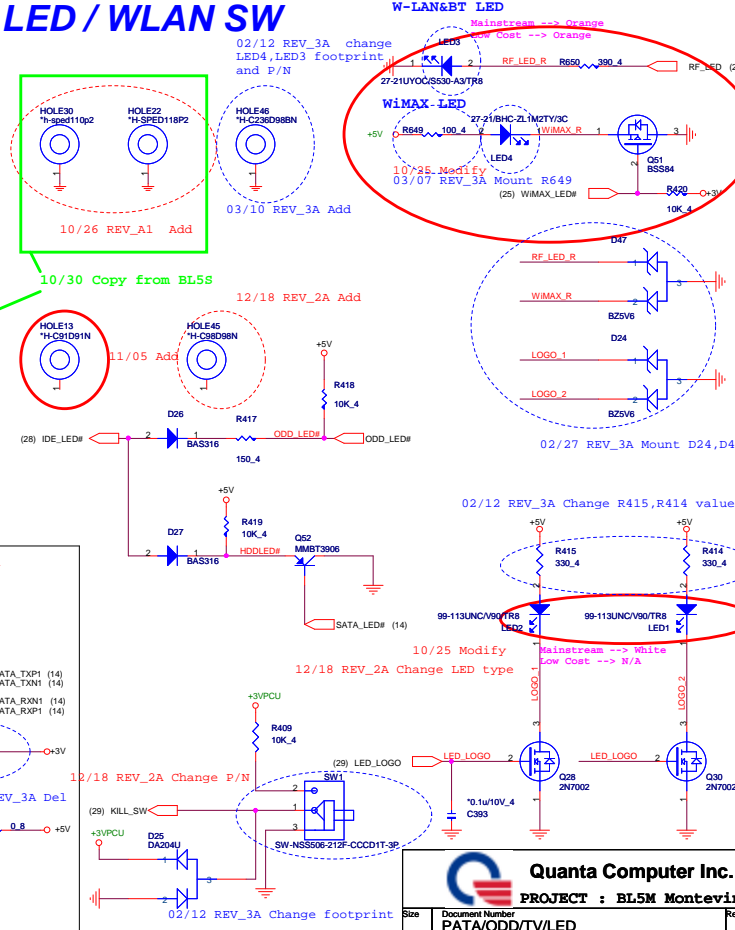
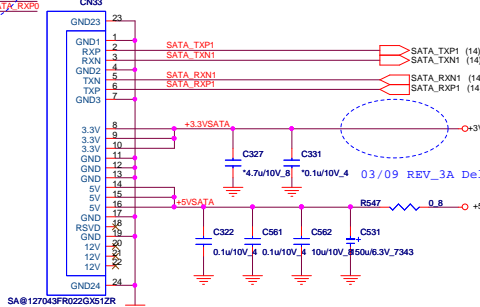
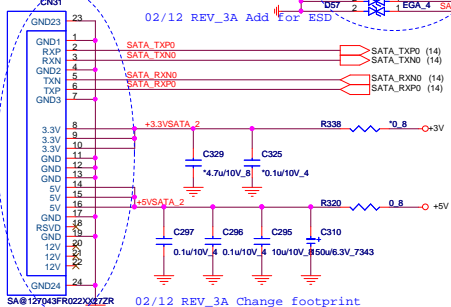
10/25 Modify  
11/01 Modify Footprint

# LED / WLAN SW



# 2'nd SATA HDD

# SATA HDD



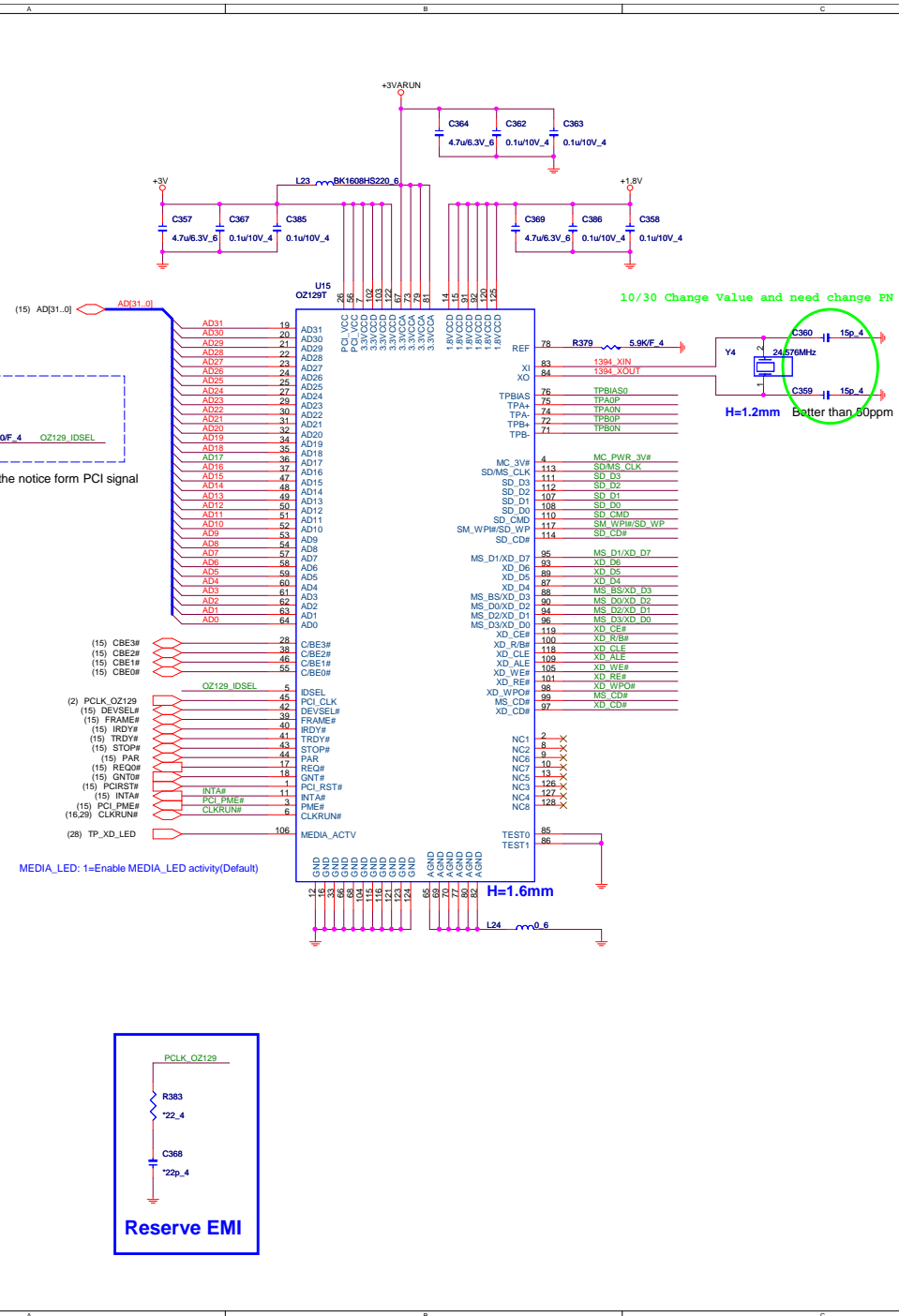
Quanta Computer Inc.

PROJECT : BL5M Montevina

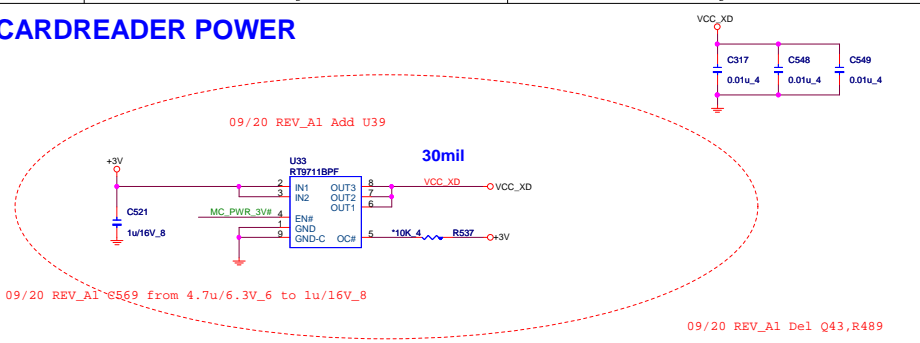
Document Number: SATA/ODD/TV/LED

Date: Monday, March 16, 2009

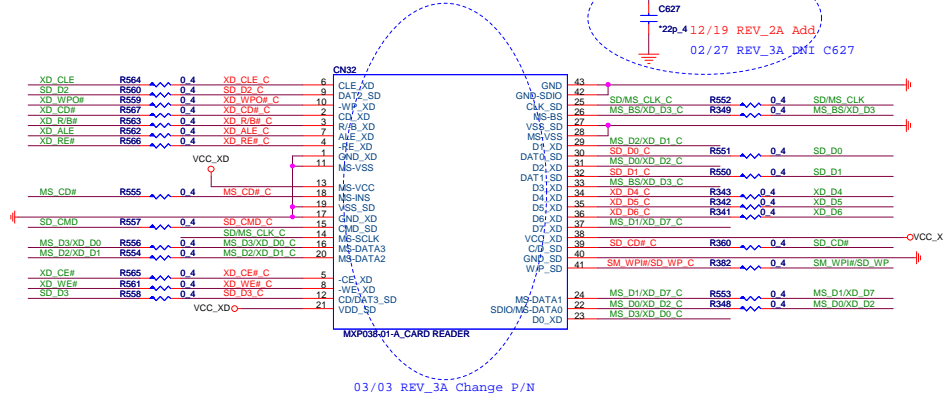
Sheet 22 of 37



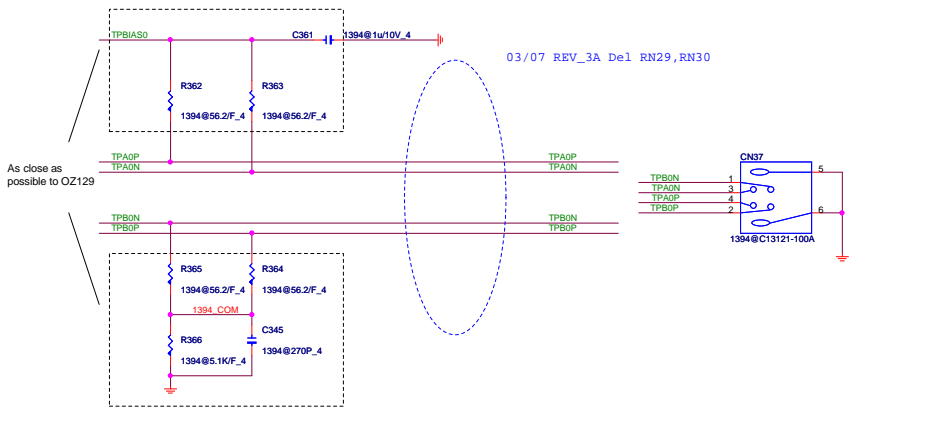
### CARDREADER POWER



### 5 IN 1 CARD READER



### 1394

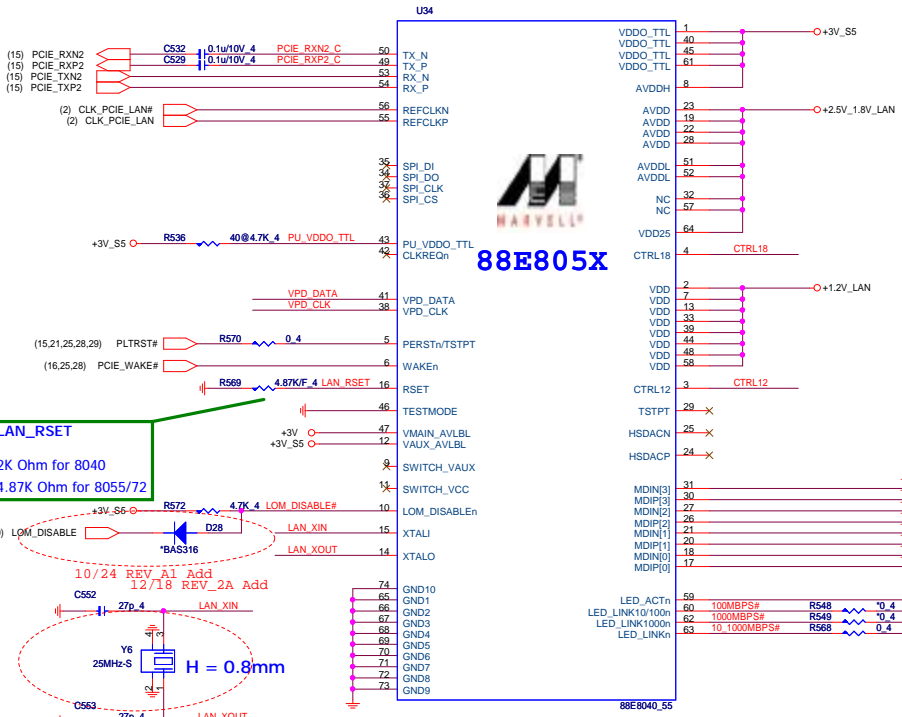


# LAN\_MARVELL\_88E8040/88E8055

**BOM Option Table**

Reference	Description
40@	10/100 : 88E8040
55@	GIGA : 88E8055
55_72@	GIGA : 88E8072

10/100 : 88E8040 P/N : AL008040001  
 GIGA : 88E8055 P/N : AJ080550000  
 GIGA : 88E8072 P/N : AL008072000



**LAN\_RSET**  
 2K Ohm for 8040  
 4.87K Ohm for 8055/72

10/24 REV\_A1 Add  
 12/18 REV\_2A Add

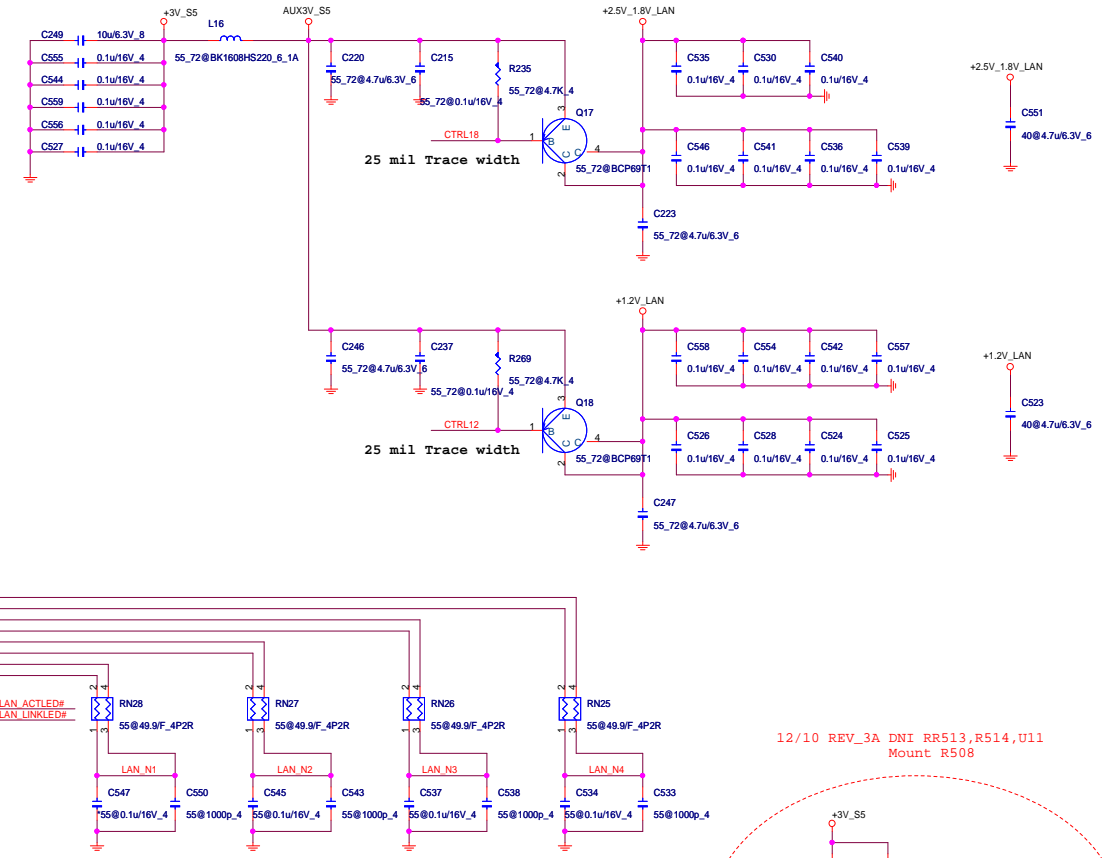
25MHz-S  
 H = 0.8mm

10/24 REV\_A1 Modify

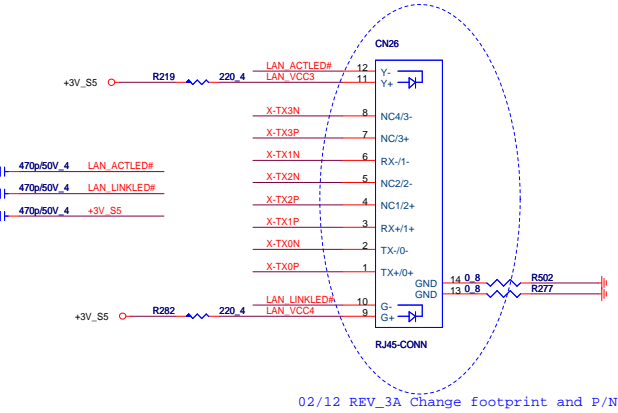
DELTA 10/100 : LFE8696-R P/N : DB0MA8LAN00  
 H = 4mm GIGA : LFE9249-R P/N : DB0ZR1LAN11

HWS 10/100 : HPL-4001B P/N : DB0SA1LAN01  
 H = 4mm GIGA : HPL-5001-3 P/N : DBOZB1LAN12

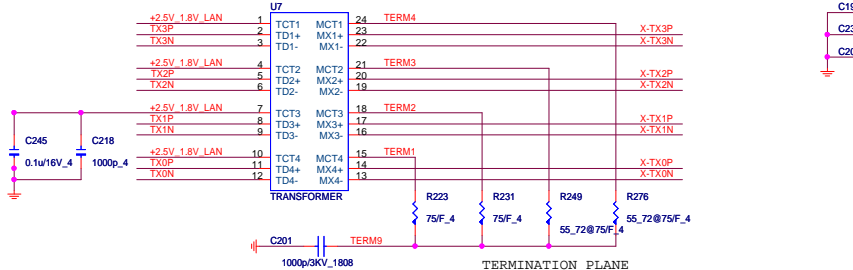
BOTHHAND 10/100 : TST1284 LF P/N : DB0KN7LAN24  
 H = 4mm GIGA : GST5009 LF P/N : DBKN1NLAN03



12/10 REV\_3A DNI R513,R514,U11  
 Mount R508



02/12 REV\_3A Change footprint and P/N



**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**

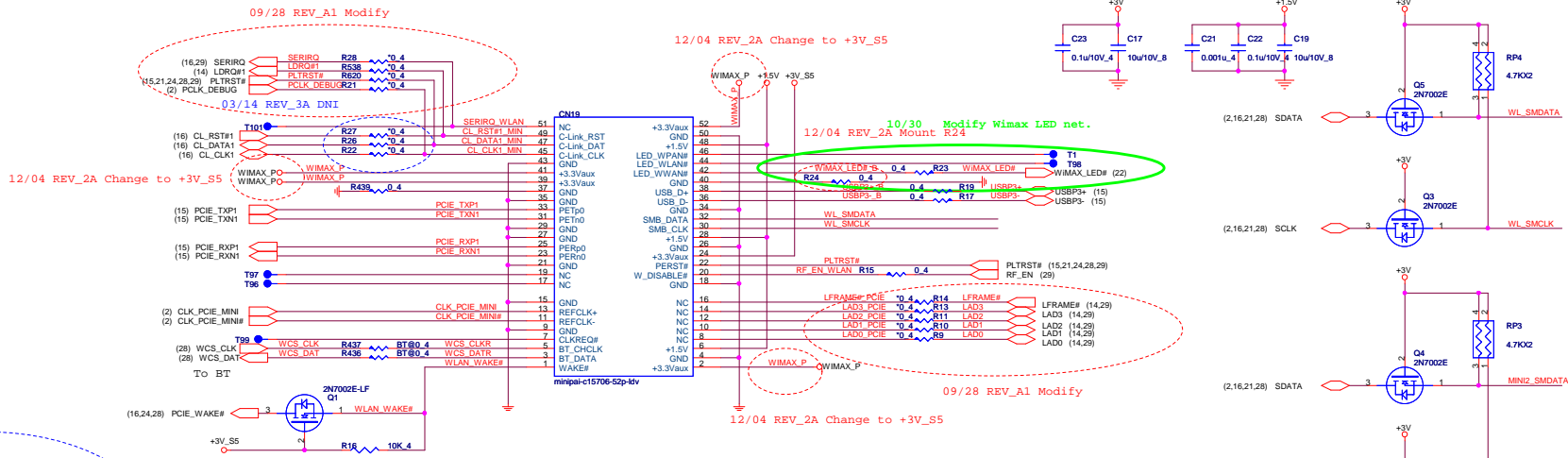
Size Document Number  
**LAN\_Marvell\_8040/8055**

Date: Monday, March 10, 2008 Sheet 24 of 37

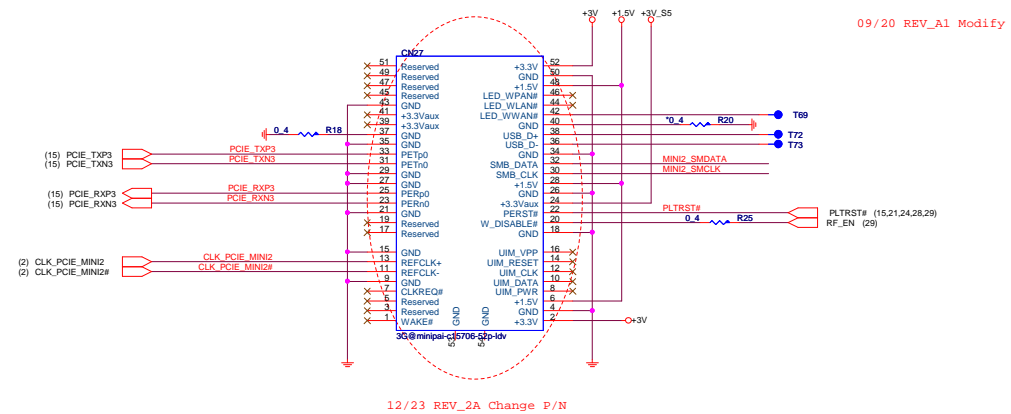


# Mini PCI-E Card WLAN

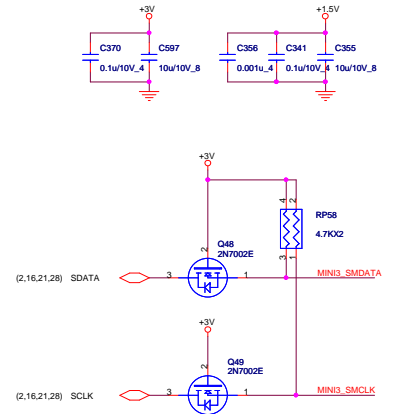
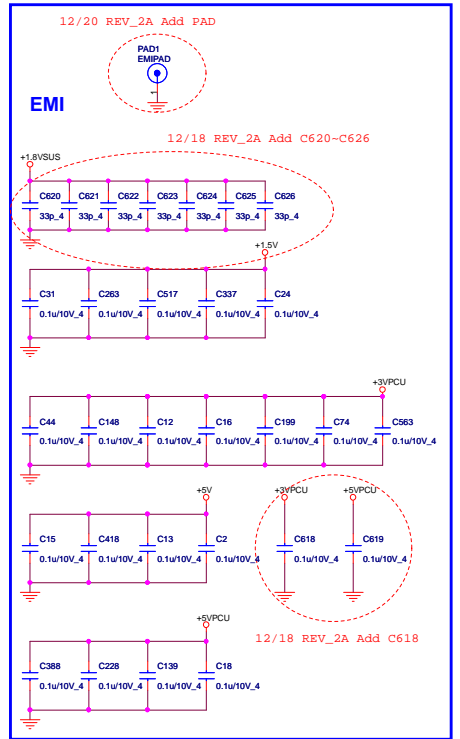
## MINI-Card I



## MINI-Card II



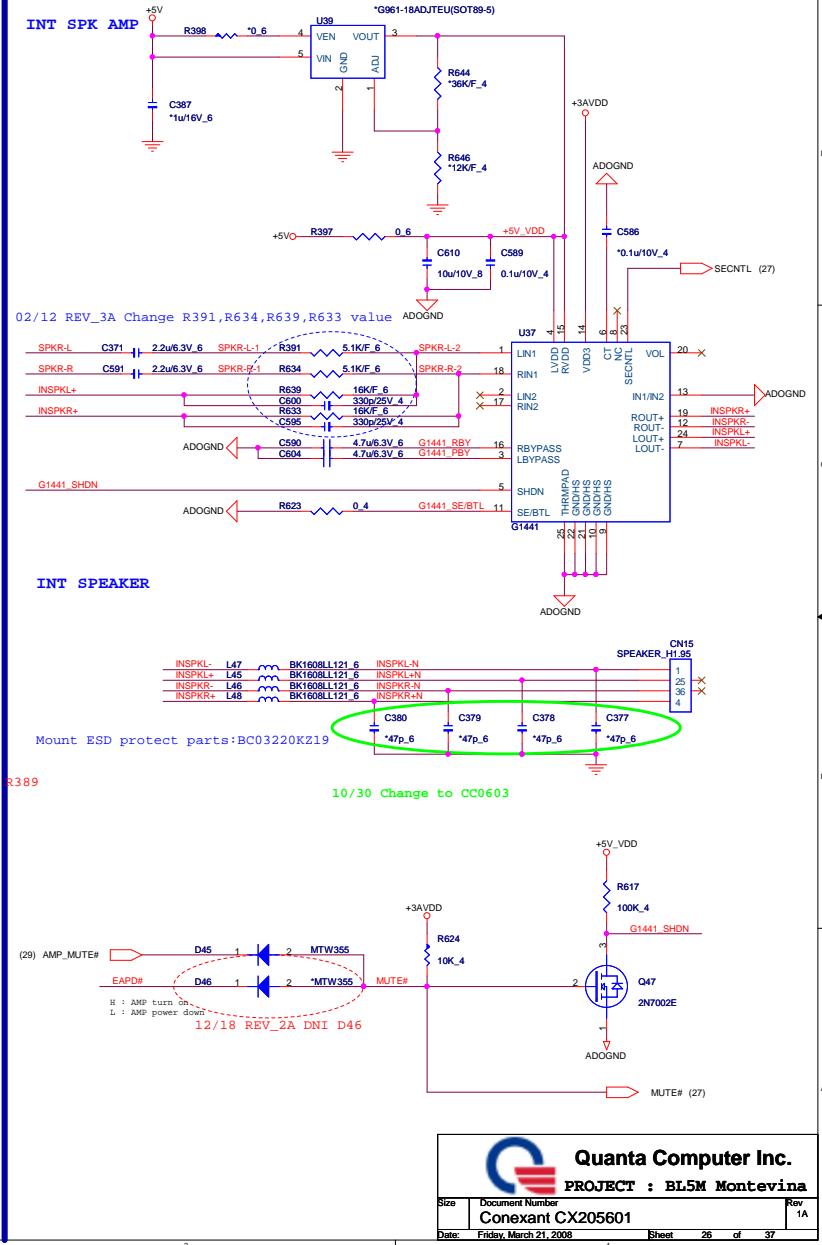
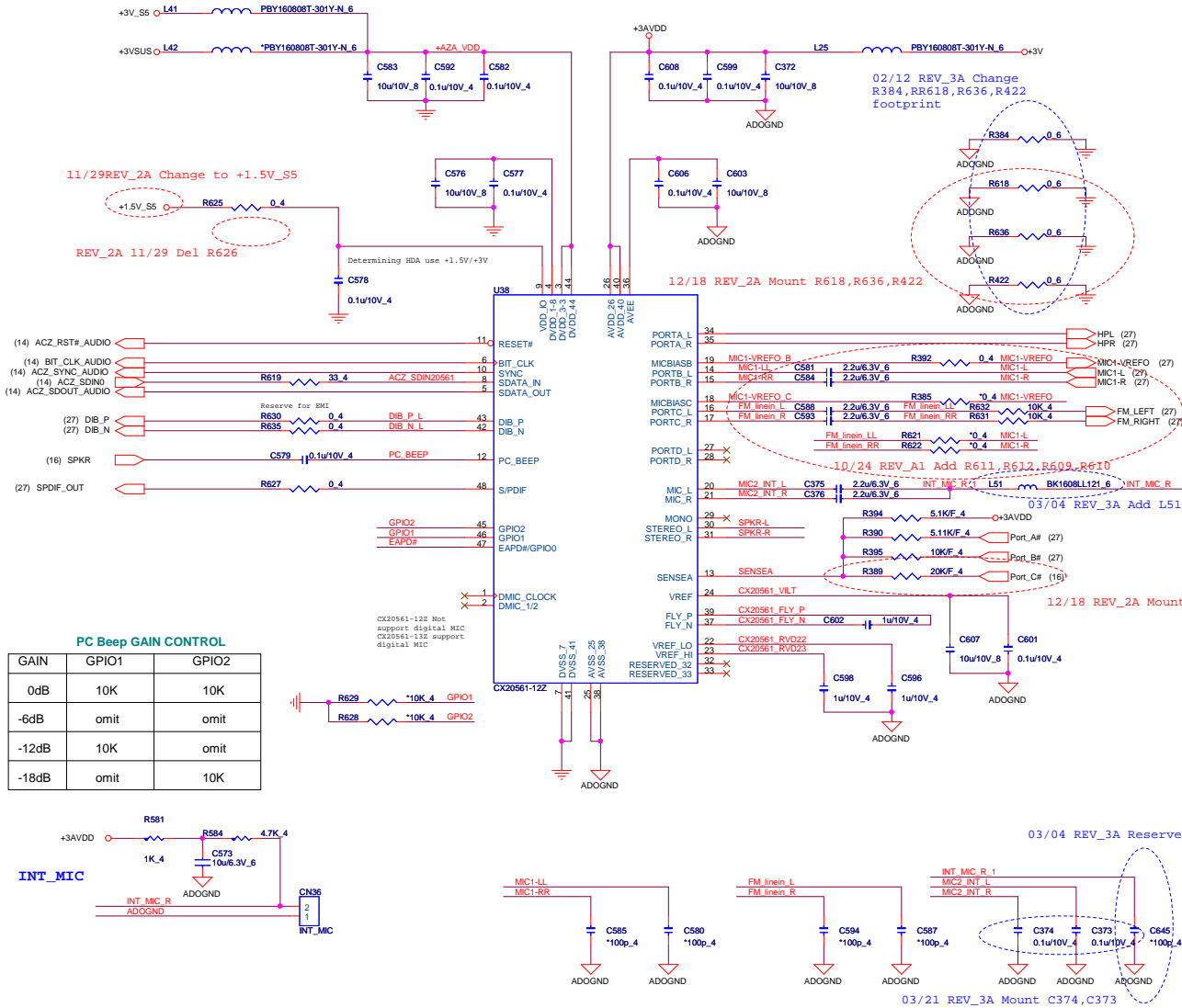
## MINI-Card III



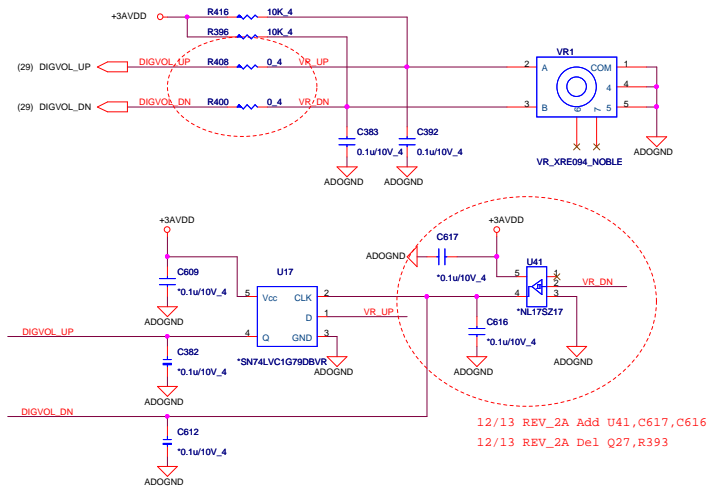
H= 8mm

**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**  
 Size Document Number  
**MINI PCIE/HOLE**  
 Date: Friday, March 14, 2008 Sheet 26 of 37

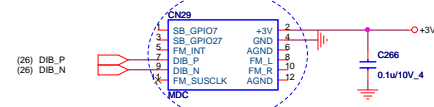
Codec (CX20561)



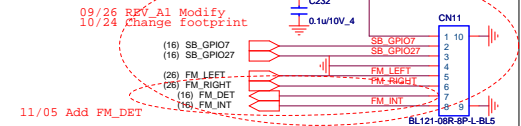
VR



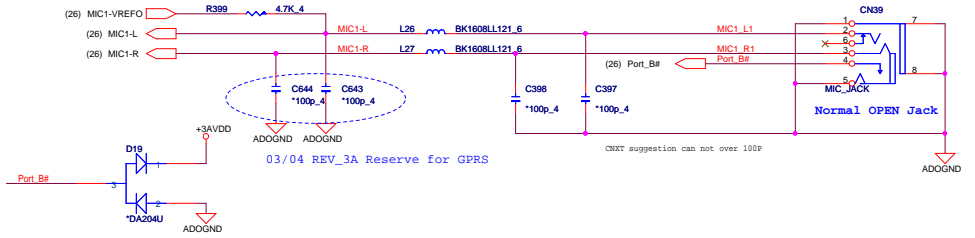
MDC



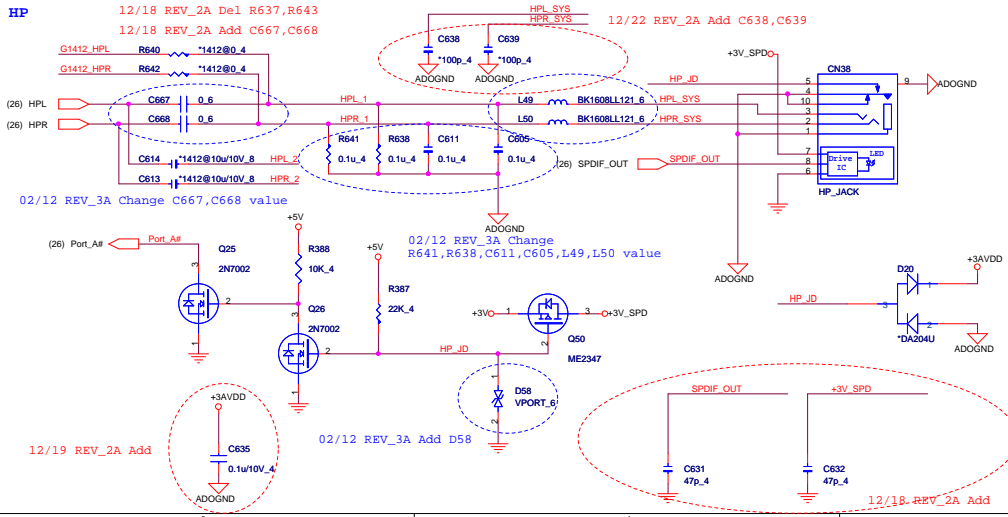
FM Tuner



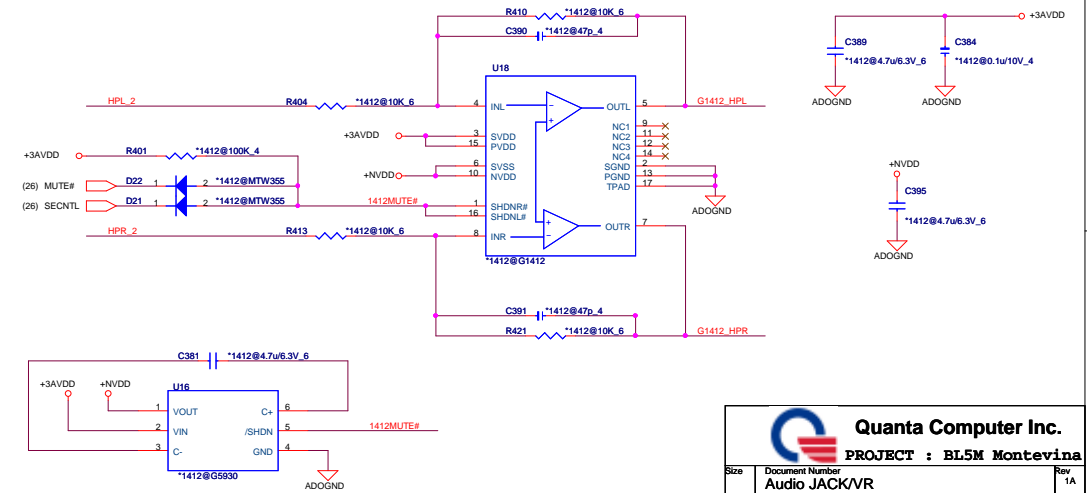
SYSTEM MIC



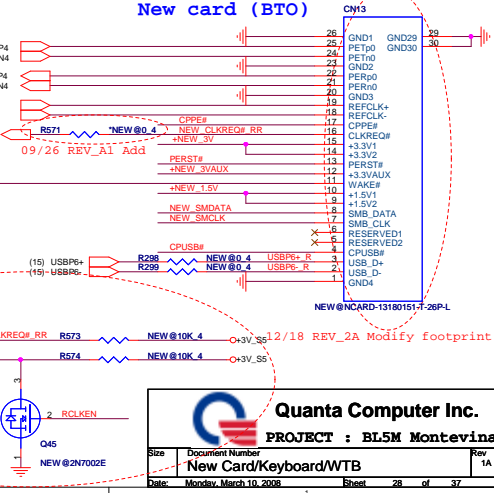
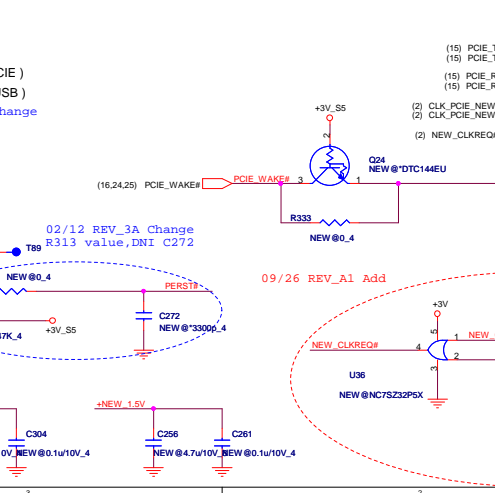
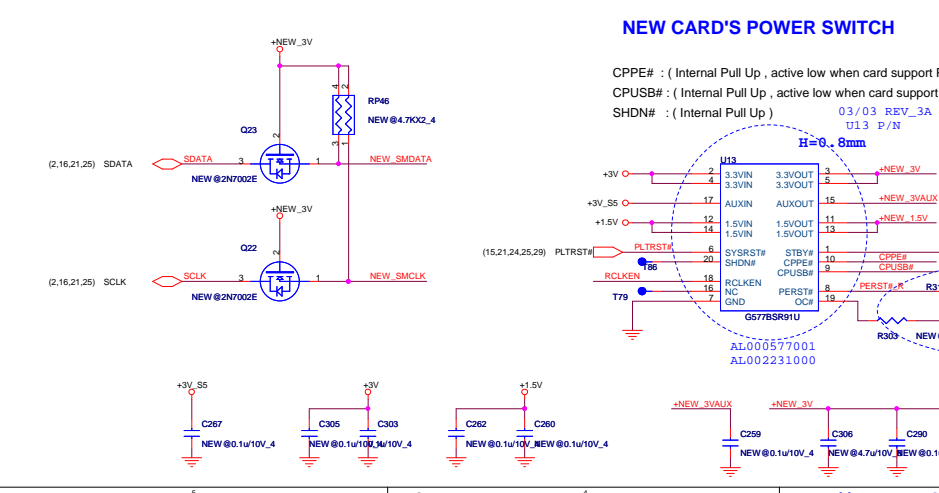
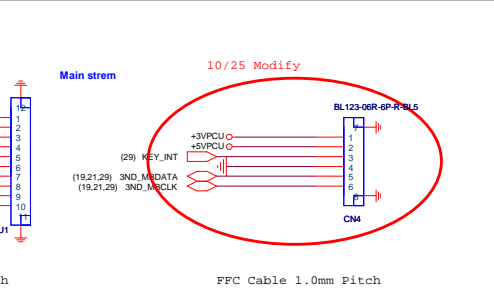
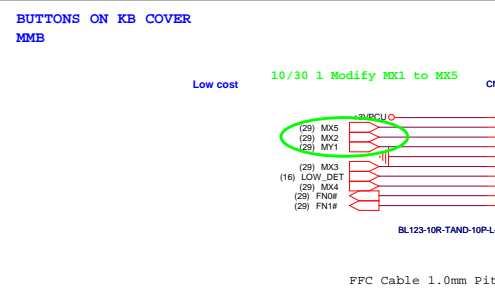
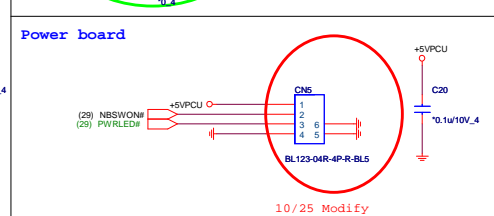
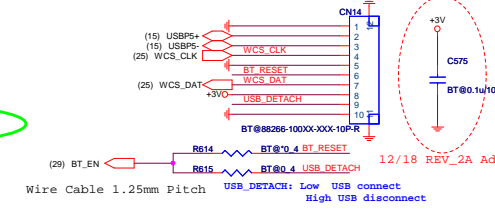
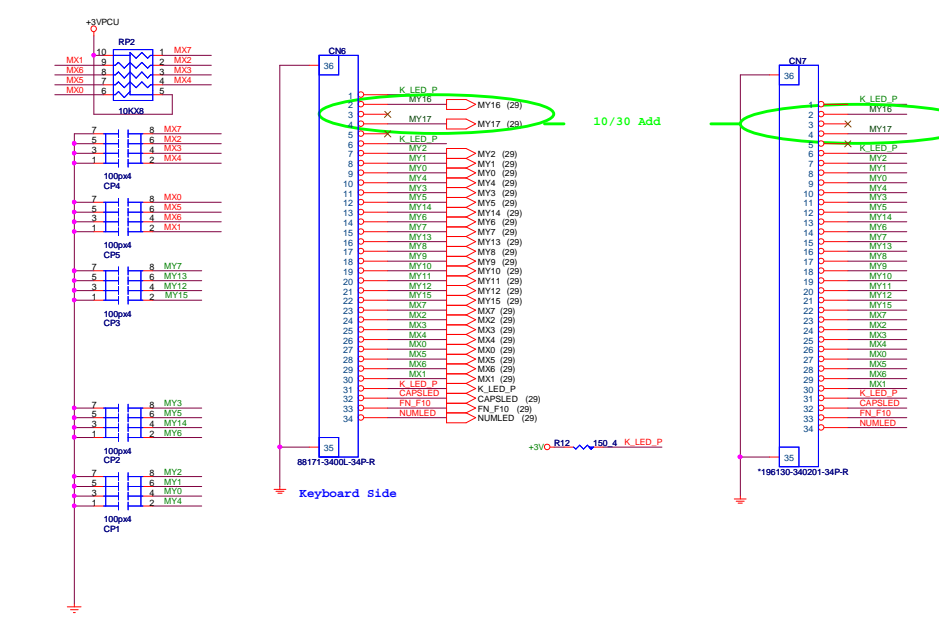
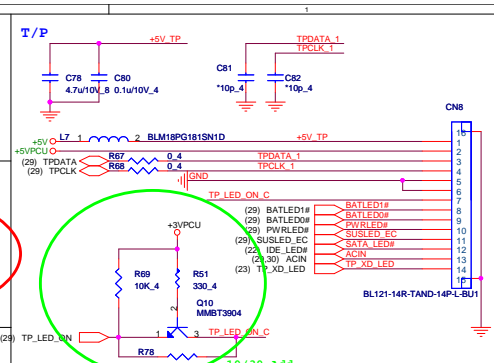
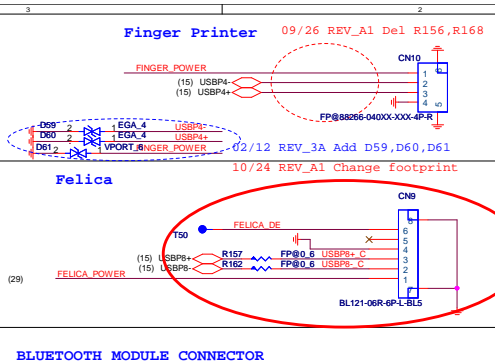
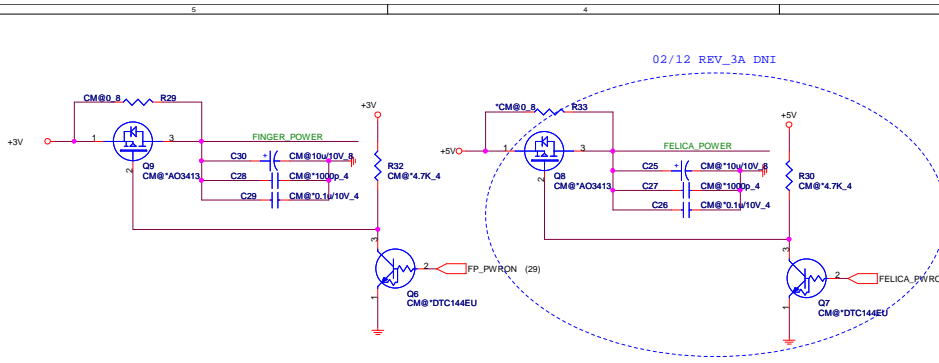
HP



HP Amplifier



**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**  
 Size Document Number  
**Audio JACK/VR** Rev 1A  
 Date: Monday, March 10, 2008 Sheet 27 of 37



**Quanta Computer Inc.**

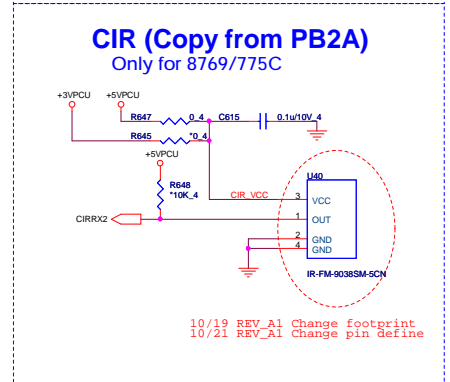
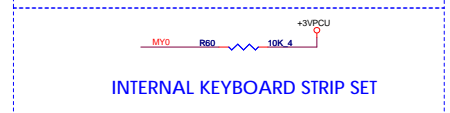
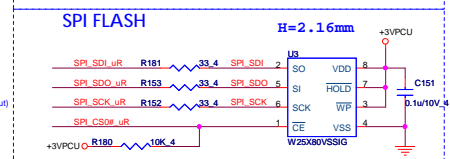
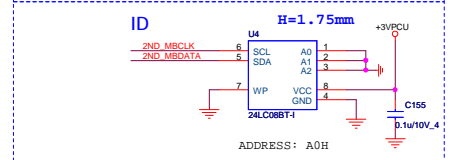
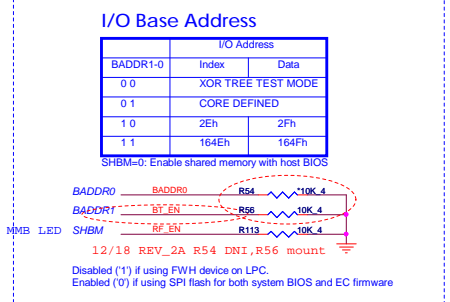
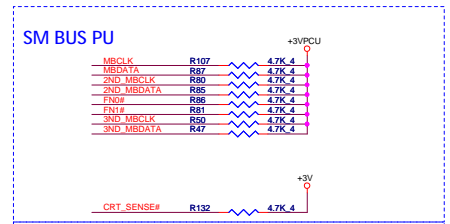
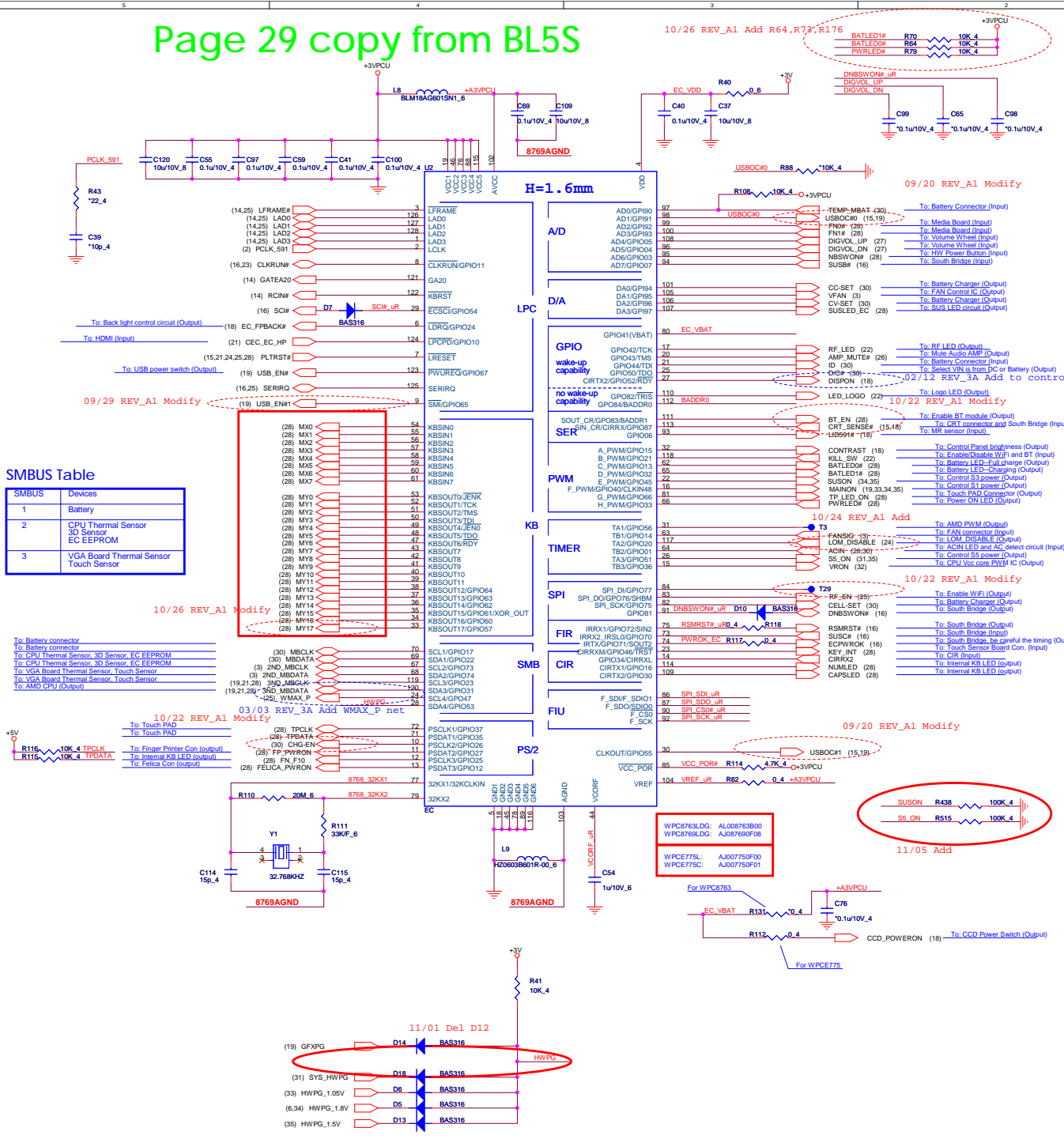
**PROJECT : BL5M Montevina**

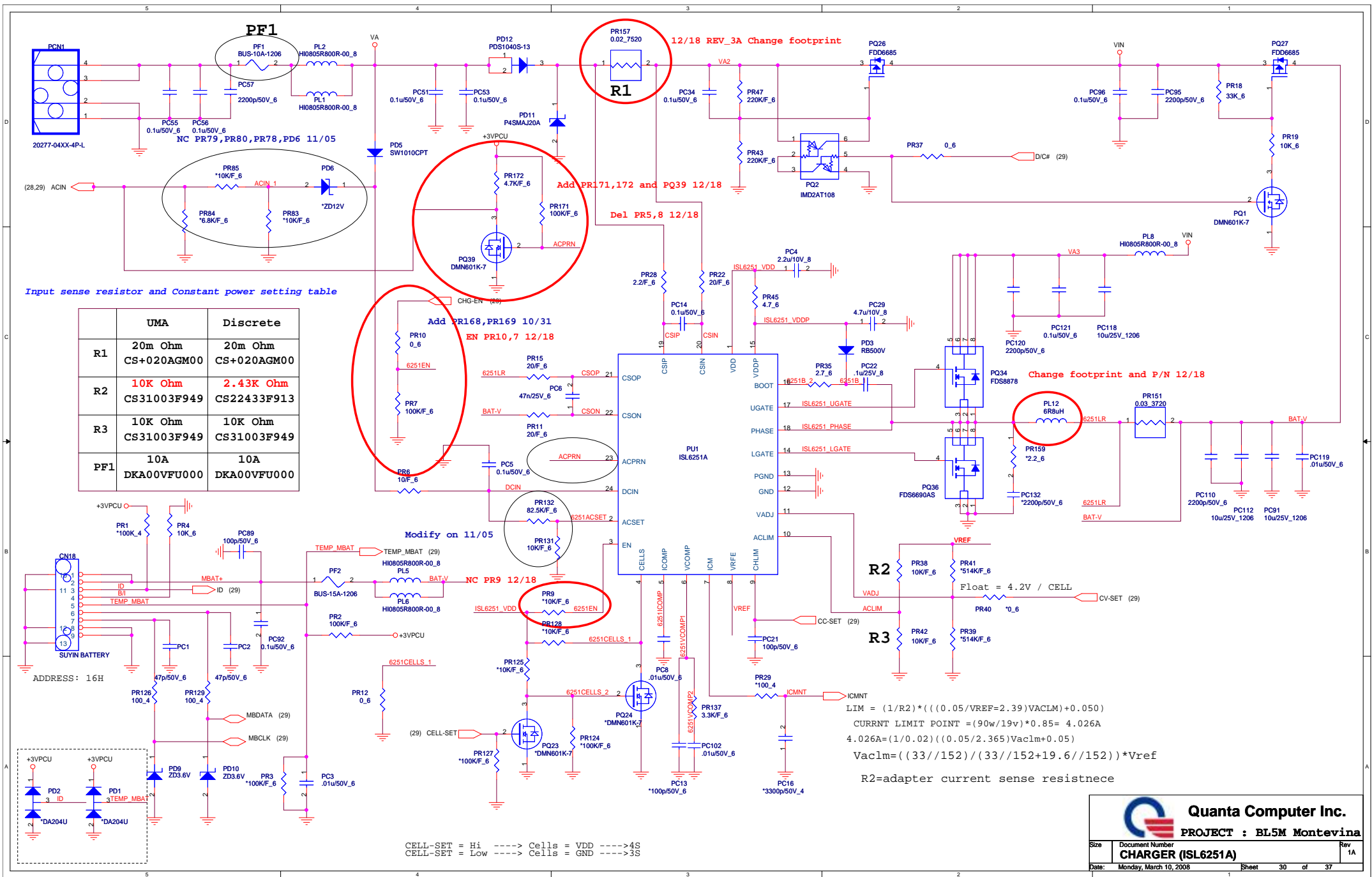
Doc No: **New Card/Keyboard/WTB**

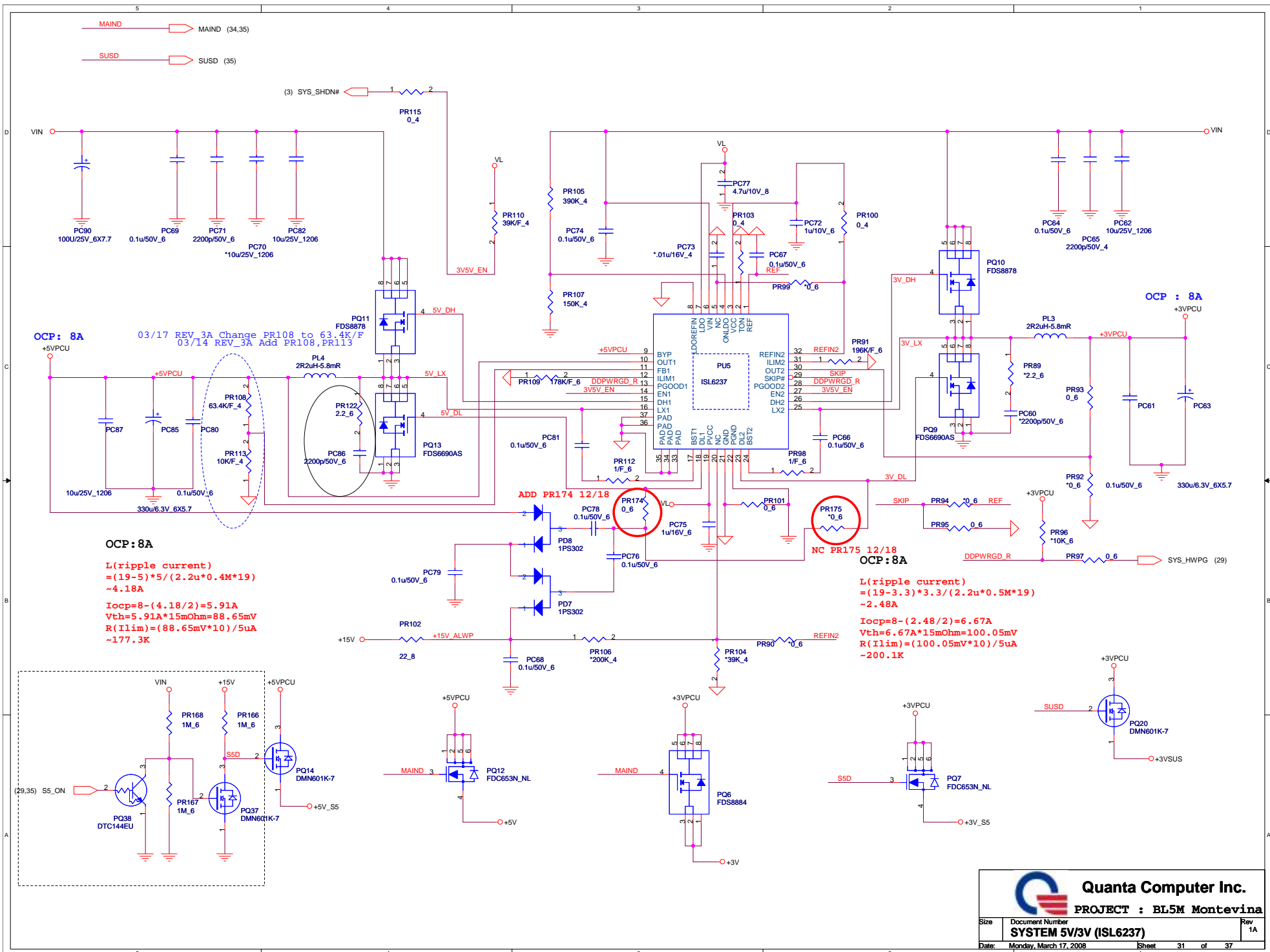
Date: Monday, March 10, 2009

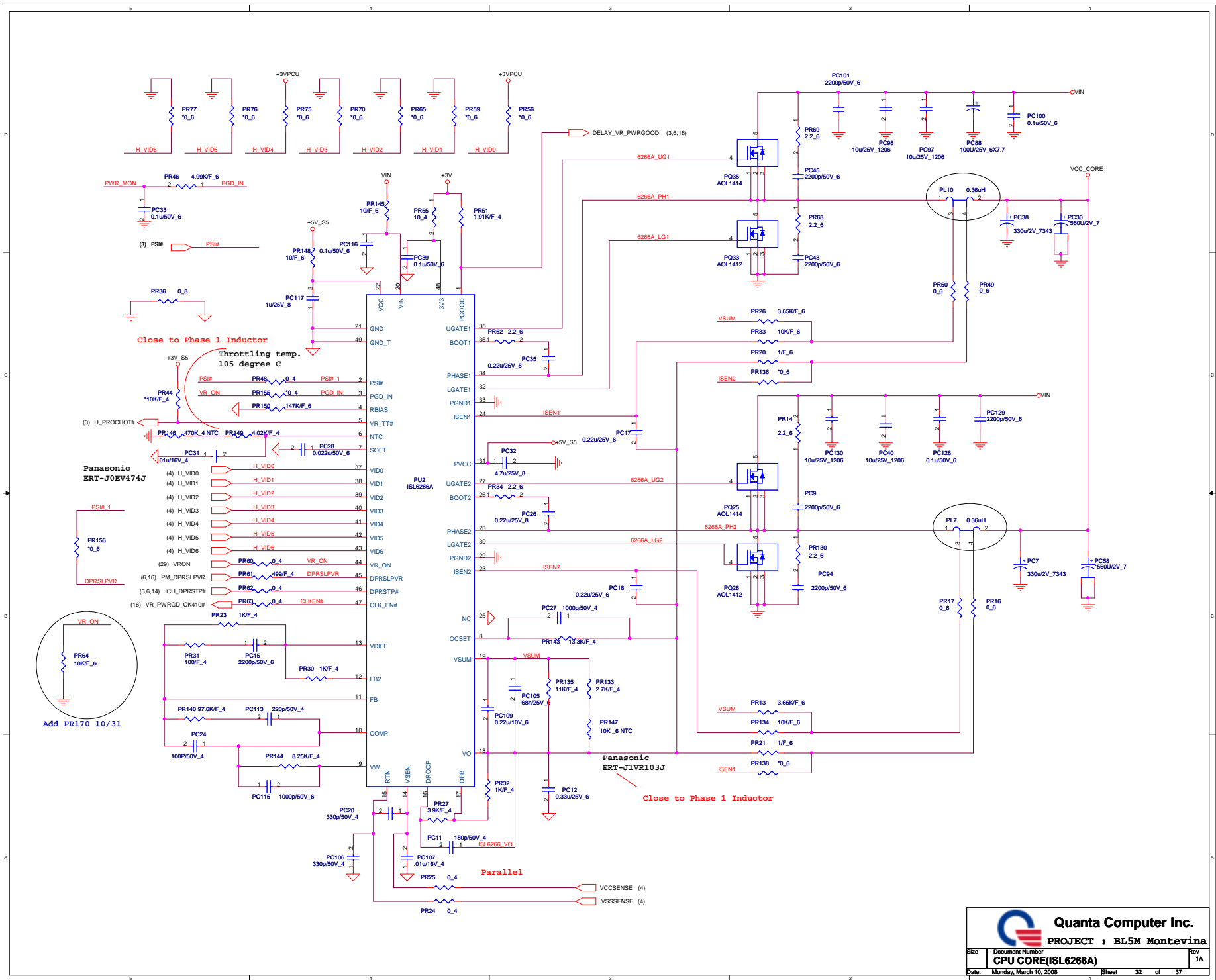
Rev: **1A**


Sheet: 28 of 37



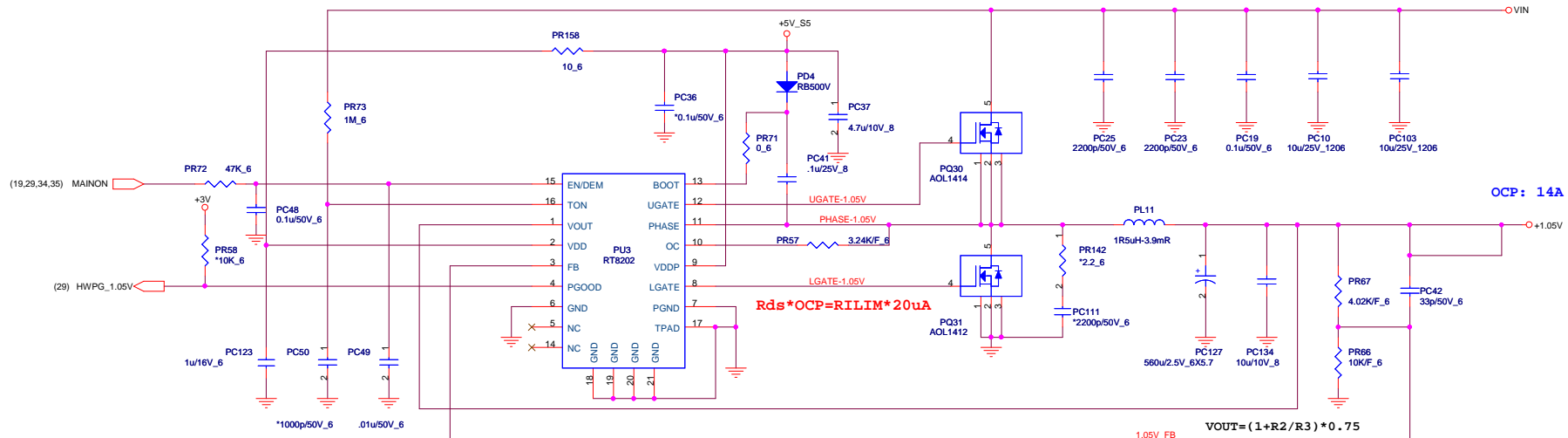







**Quanta Computer Inc.**  
 PROJECT : BL5M Montevina  
 Document Number  
**CPU CORE(ISL6266A)**  
 Date: Monday, March 10, 2008 Sheet 32 of 37




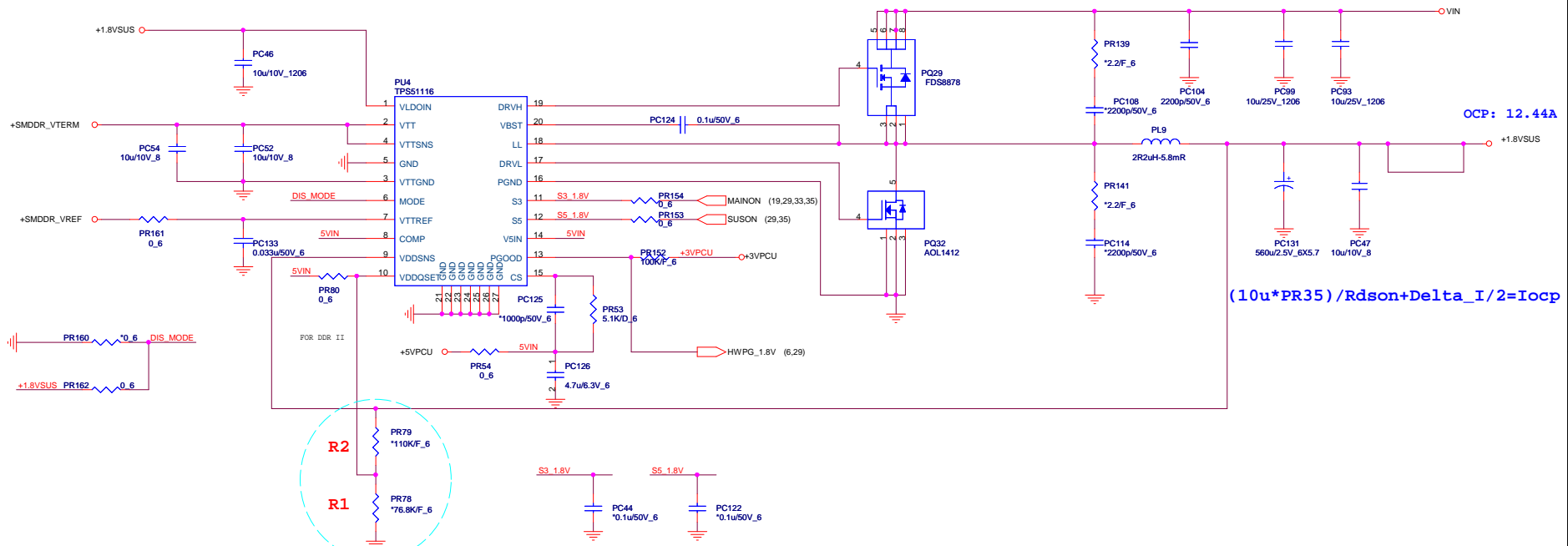


$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

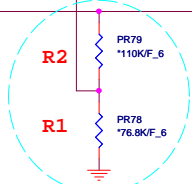
AOL1412 Rds=4.6mOhm  
14A OCP --- OC=3.22K

 <b>Quanta Computer Inc.</b> <b>PROJECT : BL5M Montevina</b>		Rev
		1A
Size	Document Number	
	<b>VTT 1.05V (RT8202)</b>	
Date:	Monday, March 10, 2008	Sheet 33 of 37



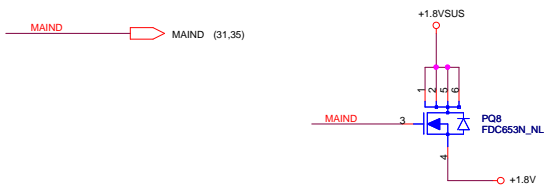
OCP: 12.44A


$$(10u * PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$$



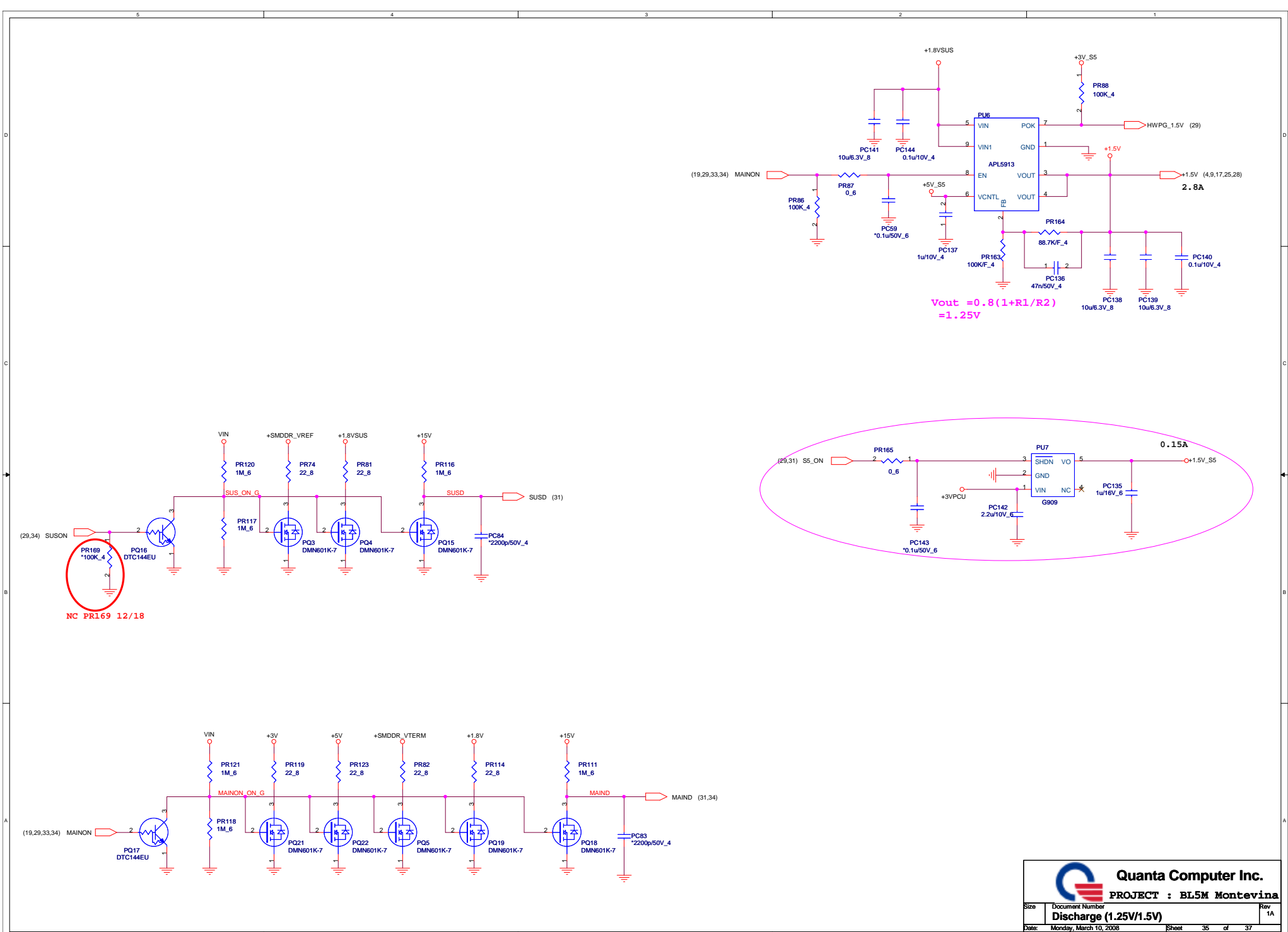
$$R1 = (100 * V_{out} - R2) K$$

if tune Vout PR38 un-mount, PR156 PR165 mount




**Quanta Computer Inc.**  
**PROJECT : BL5M Montevina**

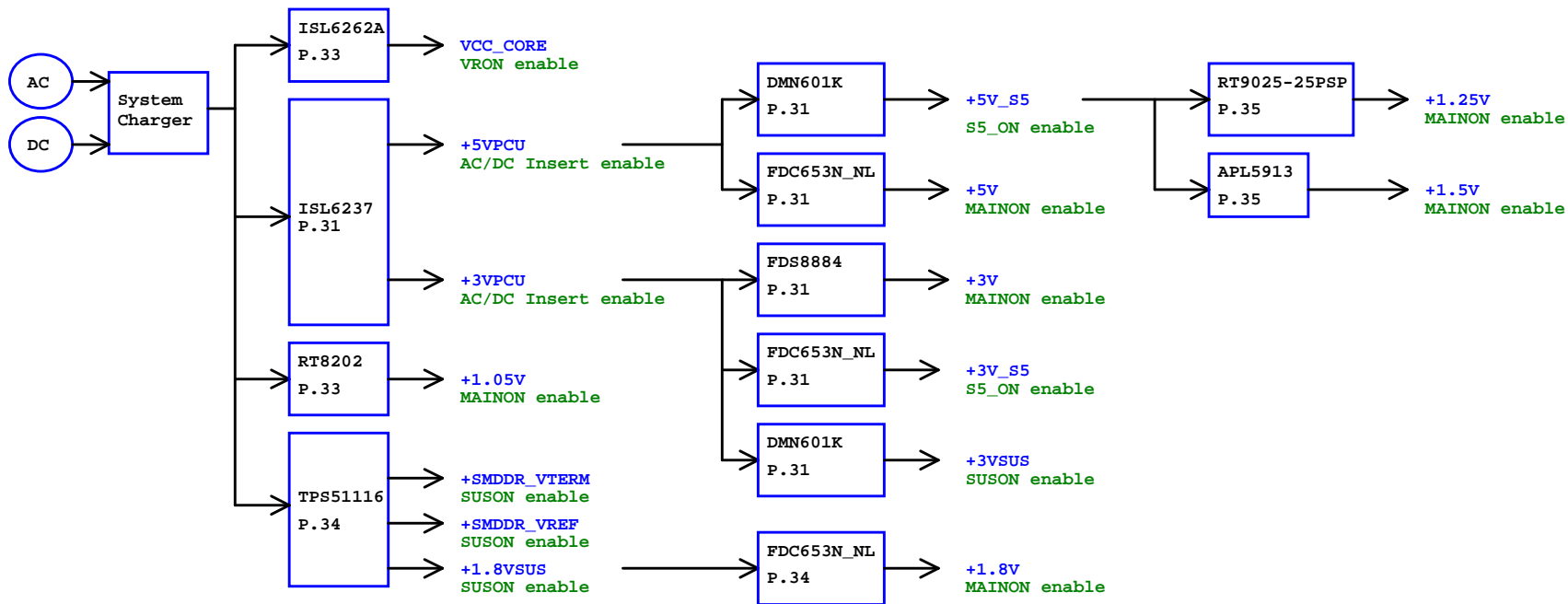
Size	Document Number	Rev
	<b>DDR 1.8V(TPS51116)</b>	<b>1A</b>
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	<b>Discharge (1.25V/1.5V)</b>	1A
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Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T), Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M