

# Compal Confidential

## DCL51 Schematics Document

### Banias uFCBGA/uFCPGA Package with Montara-GM Core Logic

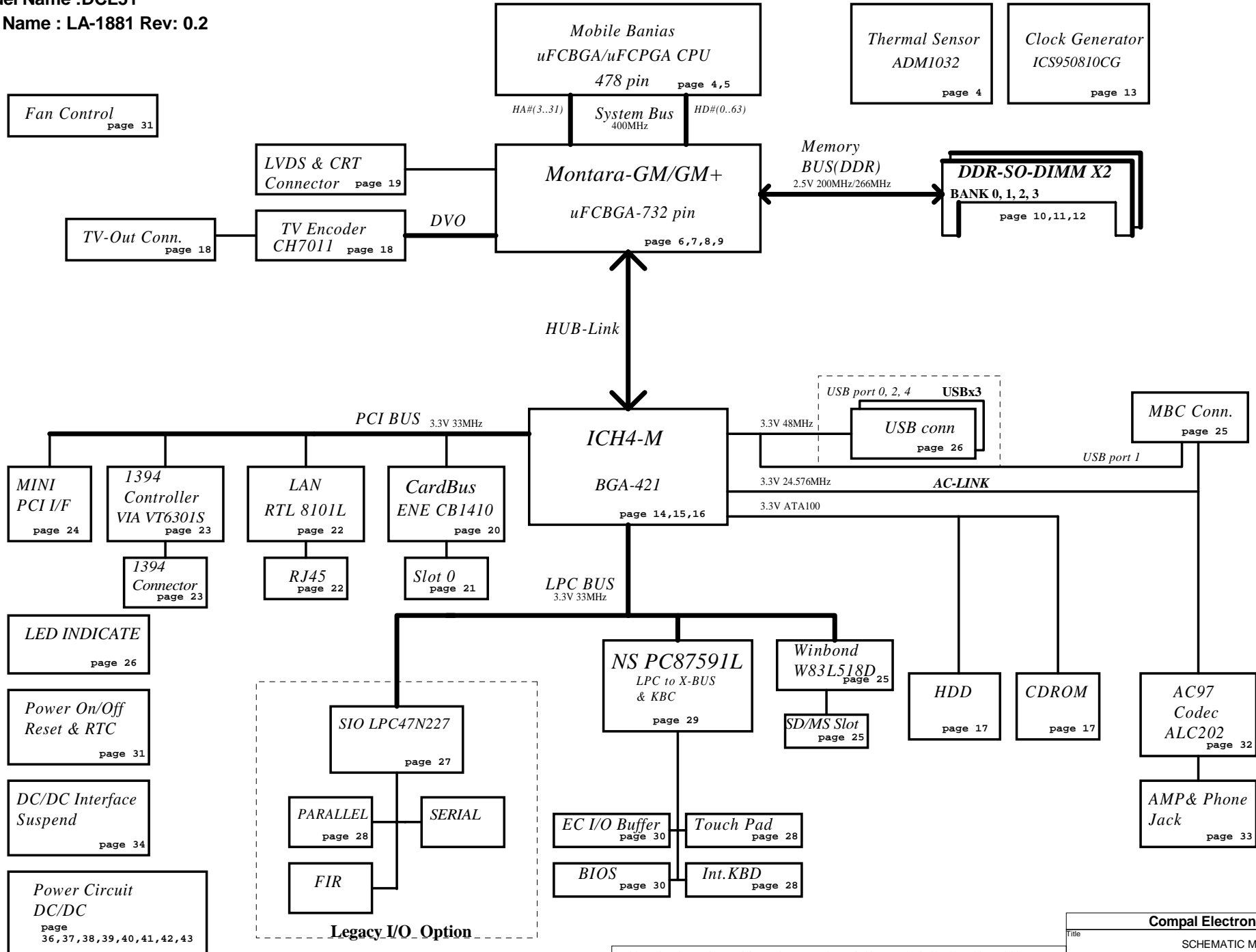
2003-06-12

REV: 1.0

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Title		
SCHEMATIC M/B LA-1881		
Size	Document Number	Rev
	401259	B
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Model Name :DCL51  
File Name : LA-1881 Rev: 0.2



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## Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2V switched power rail for GMCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V power rail for GMCH	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V <b>always</b> on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V <b>always</b> on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V <b>always</b> on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## Board ID Table

BID2	BID1	BID0	PCB Revision
0	0	0	0.1 (For 030)
0	0	1	0.2 (For 030)
0	1	0	0.3 (For 030)
0	1	1	1.0 (For 030)
1	0	0	0.1 (For ABO)
1	0	1	0.2 (For ABO)
1	1	0	0.3 (For ABO)
1	1	1	1.0 (For ABO)

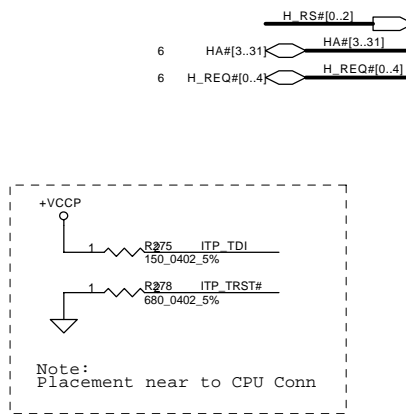
## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18/AD20	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE

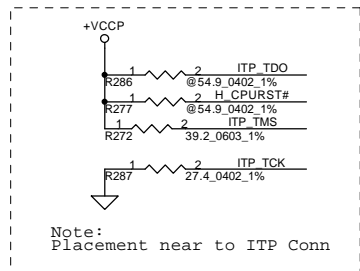
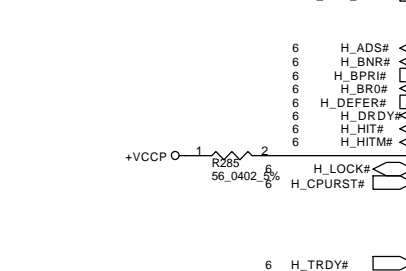
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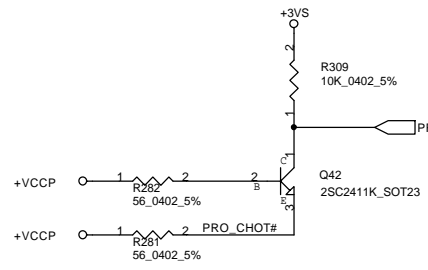
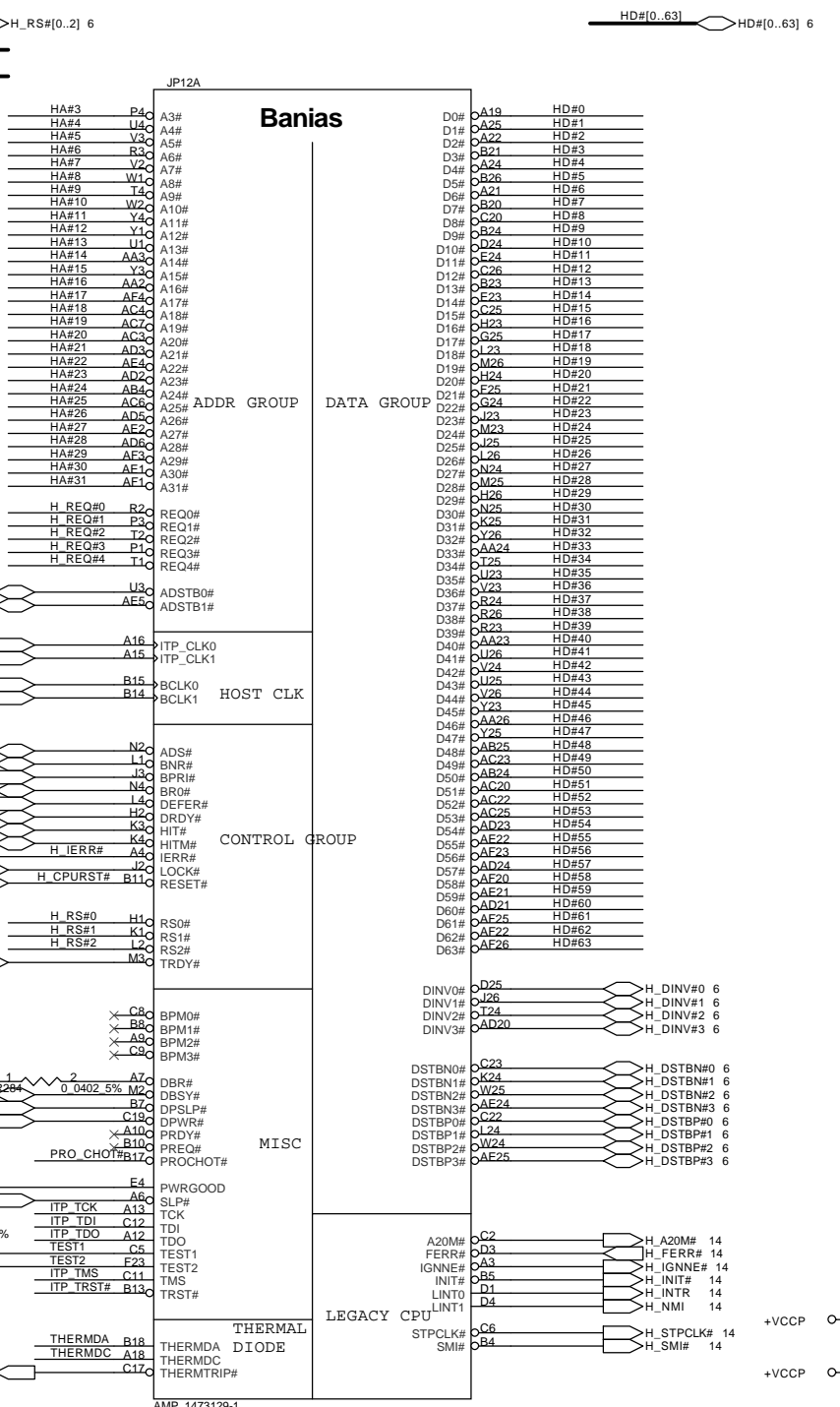
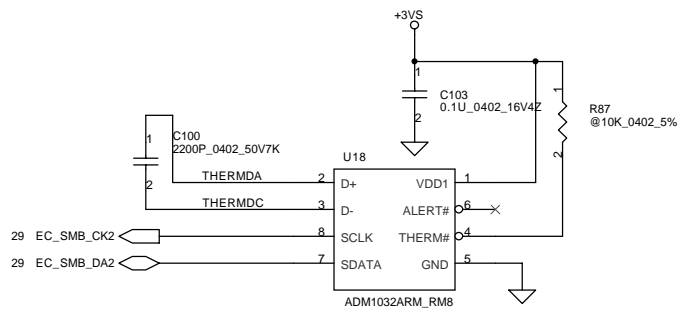
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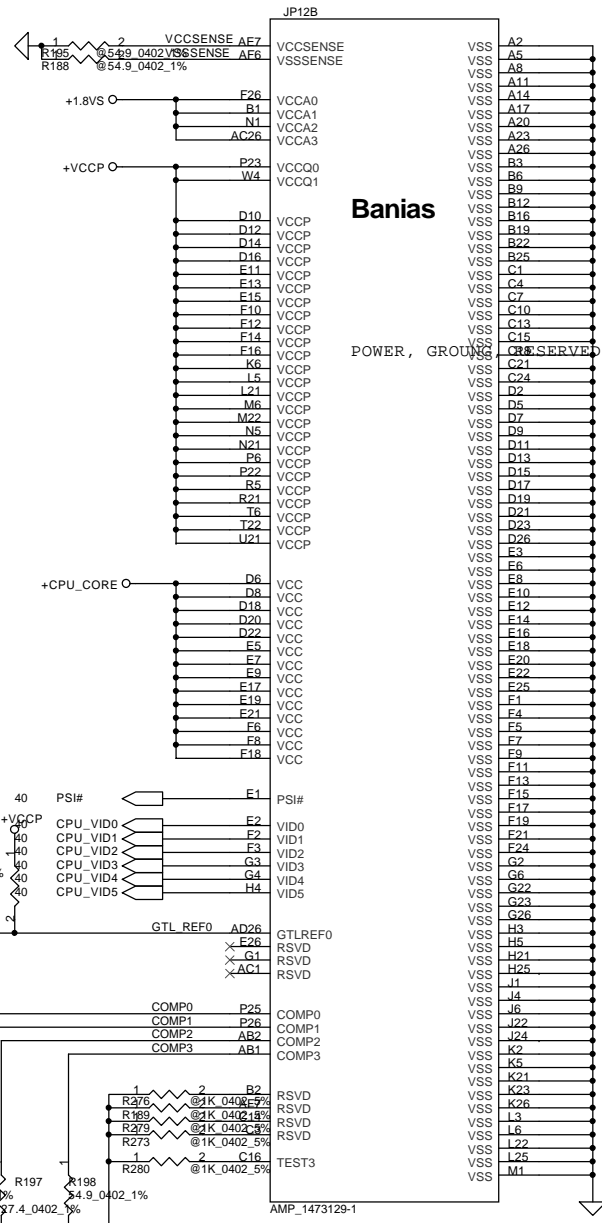


Note:  
Placement near to CPU Conn



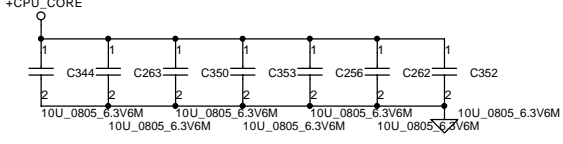
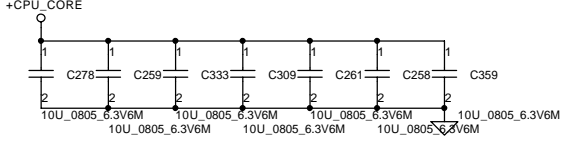
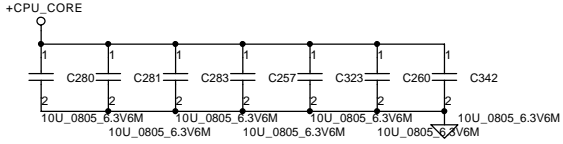
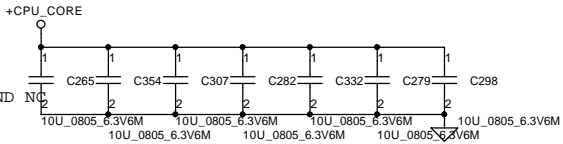
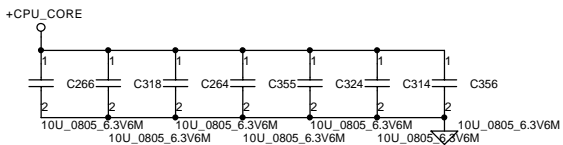
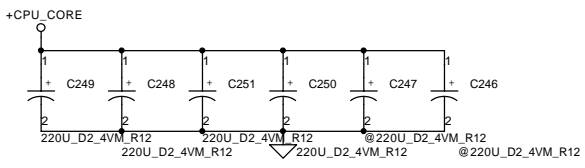
Note:  
Placement near to ITP Conn



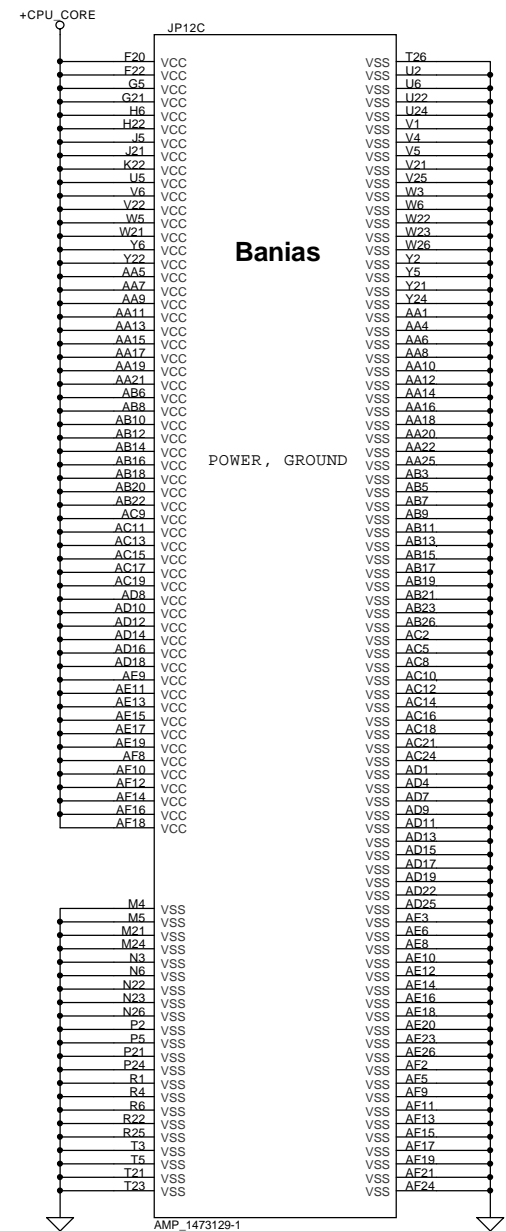
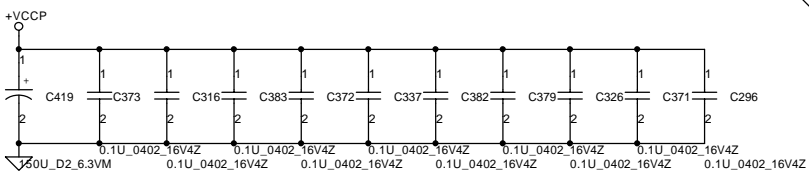
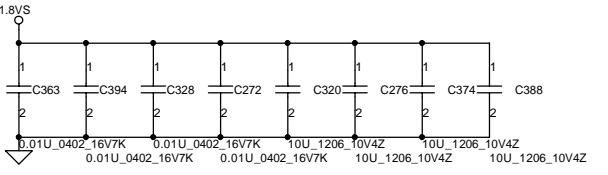


**Banias**

POWER, GROUND RESERVED SIGNALS AND NC



Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



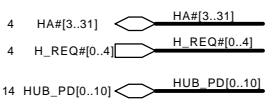
**Banias**

POWER, GROUND

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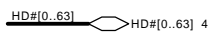
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- HA#4 T25C
- HA#5 T28C
- HA#6 R27C
- HA#7 U23C
- HA#8 U24C
- HA#9 R24C
- HA#10 U28C
- HA#11 V28C
- HA#12 U27C
- HA#13 U27C
- HA#14 U27C
- HA#15 U25C
- HA#16 V26C
- HA#17 Y24C
- HA#18 V25C
- HA#19 V23C
- HA#20 W25C
- HA#21 Y25C
- HA#22 AA27C
- HA#23 W24C
- HA#24 W23C
- HA#25 W27C
- HA#26 Y27C
- HA#27 AA28C
- HA#28 W28C
- HA#29 AB27C
- HA#30 Y26C
- HA#31 AB28C

### Montara-GM(L)

- HA#3
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- HA#11
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- HA#31



- HD#0
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- HD#63

- H\_REQ#0 R28C
- H\_REQ#1 P25C
- H\_REQ#2 R23C
- H\_REQ#3 R25C
- H\_REQ#4 T23C

### HOST

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- H\_ADSTB#1 AA26C
- AD29C
- AE29C
- K21
- J21
- J17
- Y28
- Y22

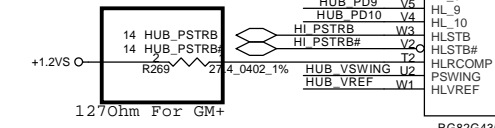
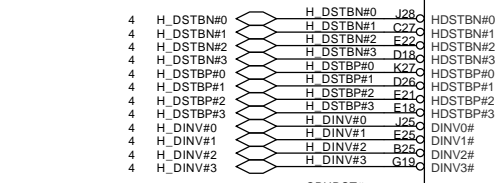
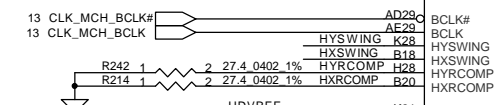
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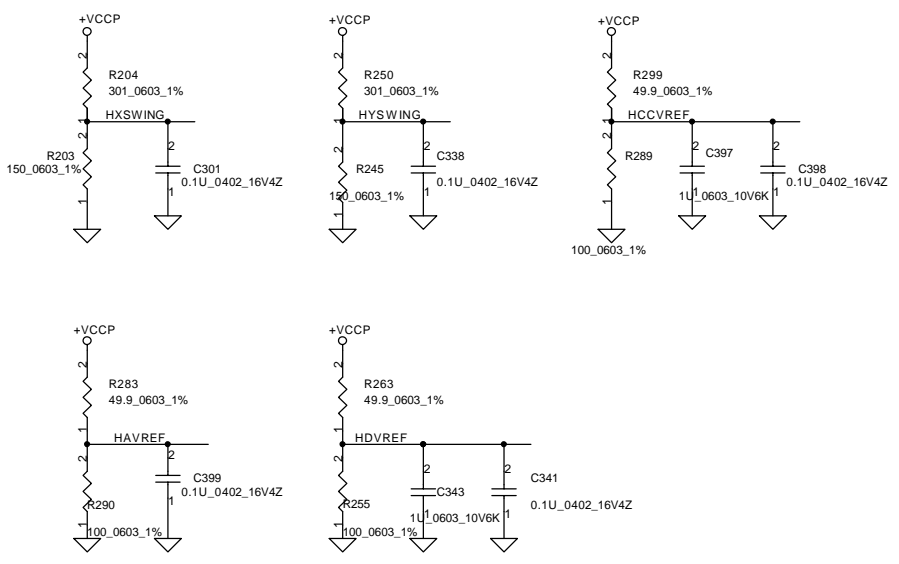
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- HUB\_PD1 U4
- HUB\_PD2 U3
- HUB\_PD3 V3
- HUB\_PD4 W2
- HUB\_PD5 W6
- HUB\_PD6 V6
- HUB\_PD7 W7
- HUB\_PD8 T3
- HUB\_PD9 V5
- HUB\_PD10 V4
- HI\_PSTRB W3
- HI\_PSTRB# V2C
- T2
- HUB\_VSWING U2
- HUB\_VREF W1

### HUB I/F

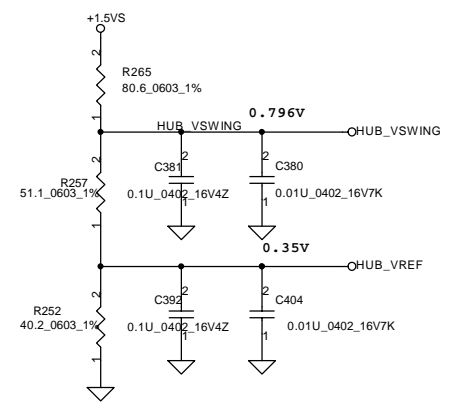
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- DRDY# N24
- DEFER# N28
- HITM# N27
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- BREQ0# M23
- HL\_9 N25
- BNR# P28
- BPR# M26
- DBSY# N23
- RS#0 N26
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- RS#2 M27
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- H\_HITM# 4
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- H\_LOCK# 4
- H\_BR0# 4
- H\_BNR# 4
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- H\_RS#2 4



### HOST REF VOLTAGE



### HUB I/F REF VOLTAGE



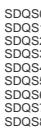
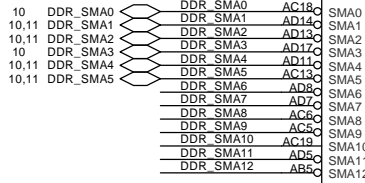
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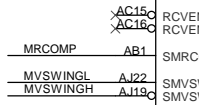
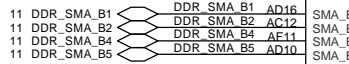
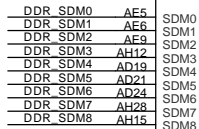
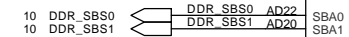
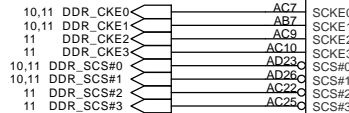
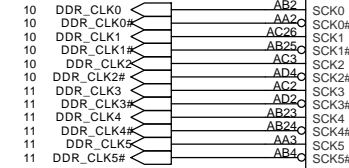
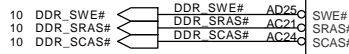


U12C

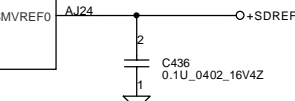
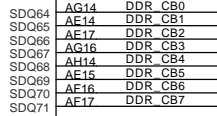
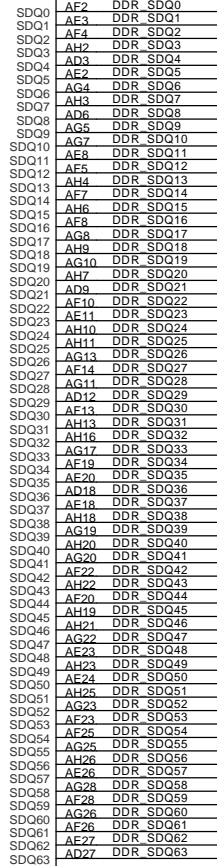
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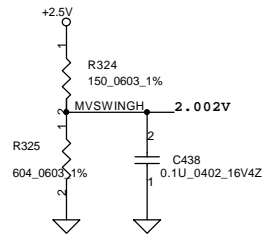
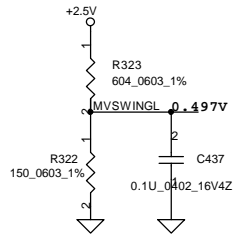
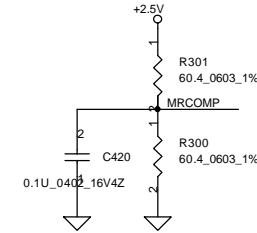
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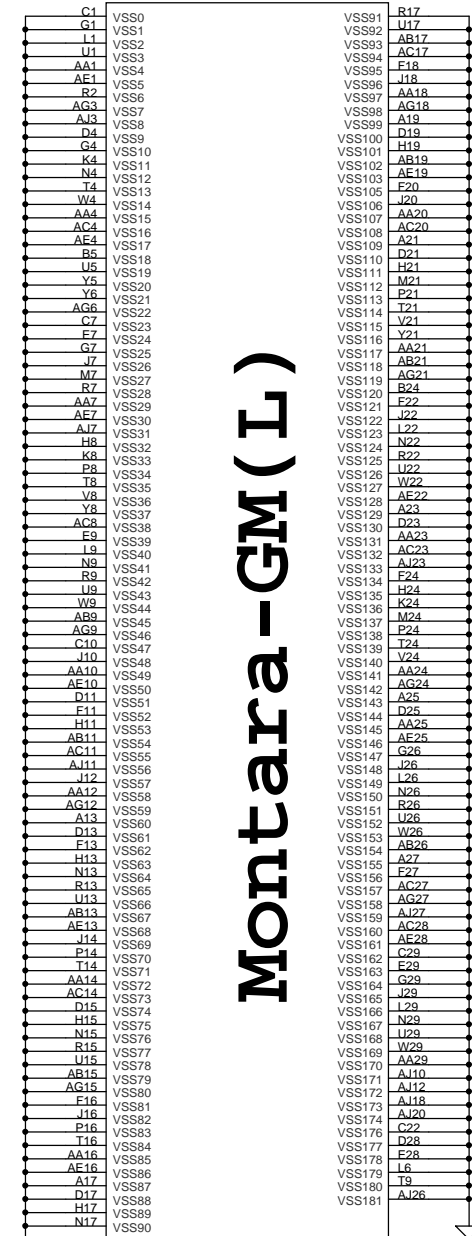
RG82G4350M\_uFCBGA732



### DDR REF & SWING VOLTAGE



U12D



RG82G4350M\_uFCBGA732

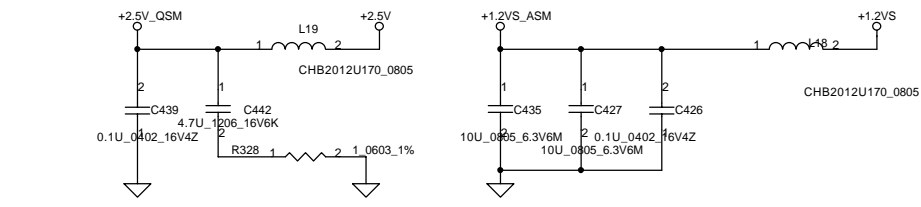
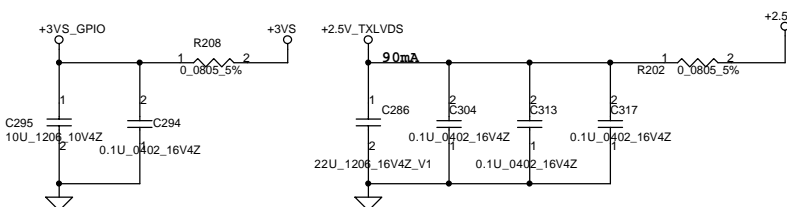
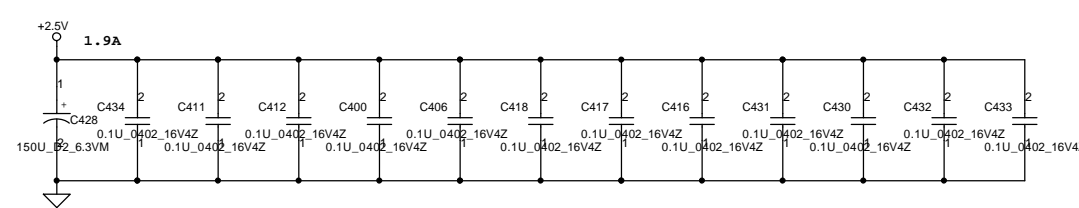
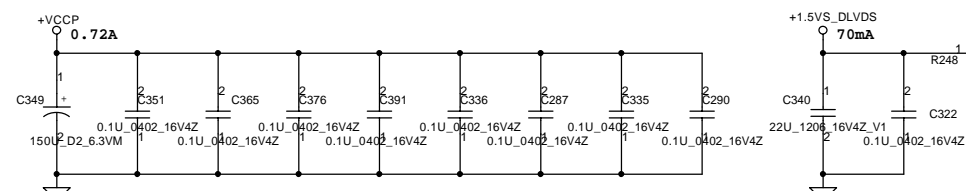
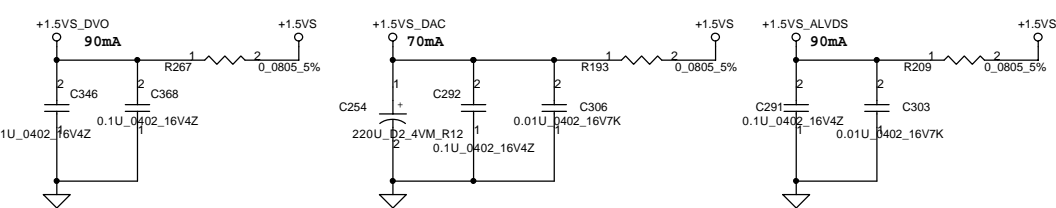
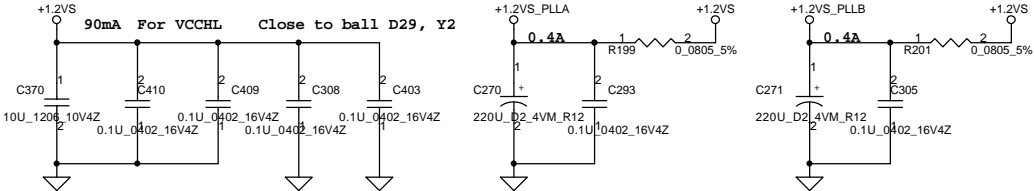
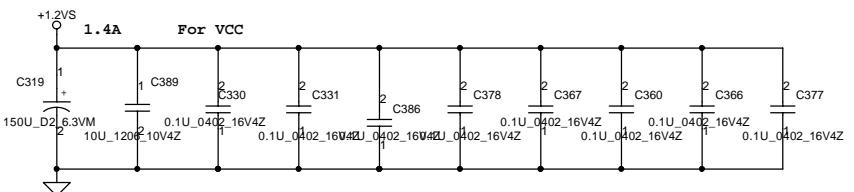
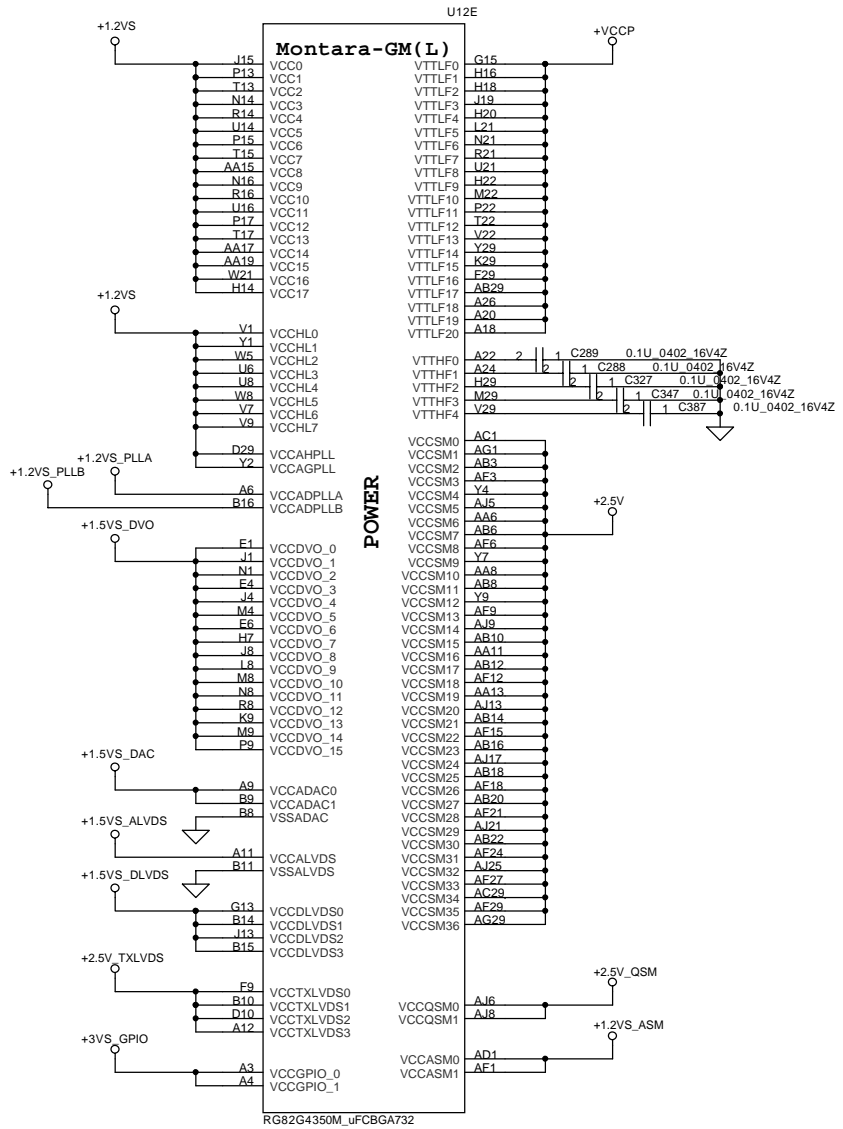
# Montara-GM(L)

### Compal Electronics, Inc.

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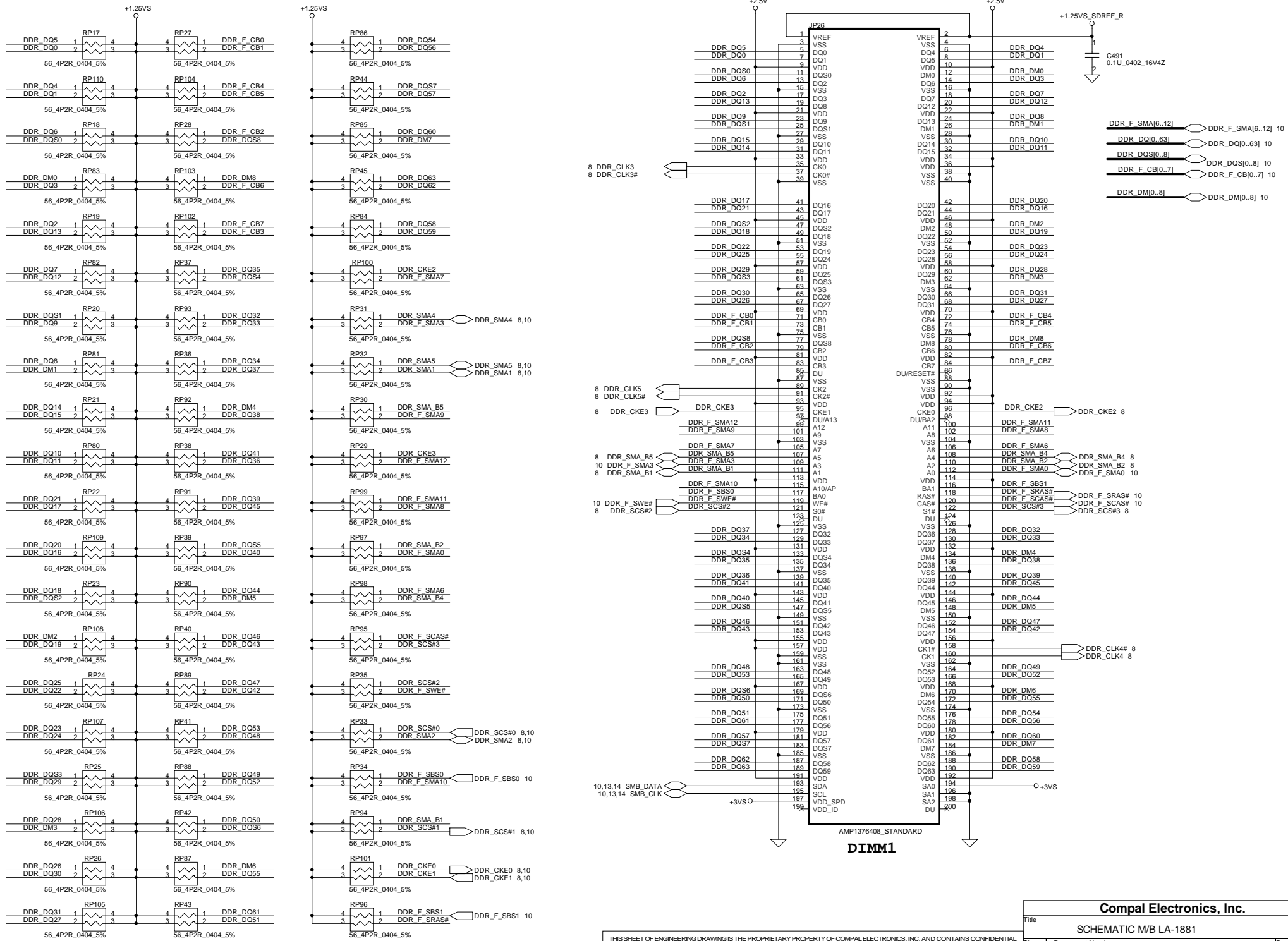




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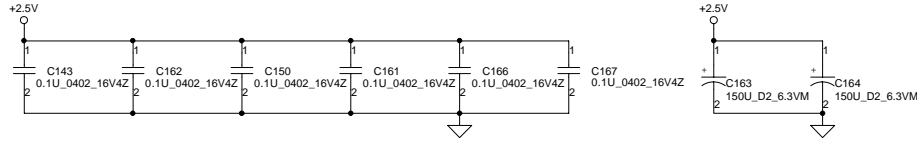
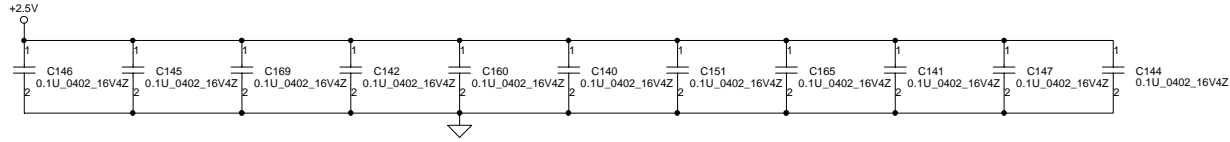
- DDR F\_SMA[6..12] ⇨ DDR\_F\_SMA[6..12] 10
- DDR DQ[0..63] ⇨ DDR\_DQ[0..63] 10
- DDR DQS[0..8] ⇨ DDR\_DQS[0..8] 10
- DDR F\_CB[0..7] ⇨ DDR\_F\_CB[0..7] 10
- DDR DM[0..8] ⇨ DDR\_DM[0..8] 10

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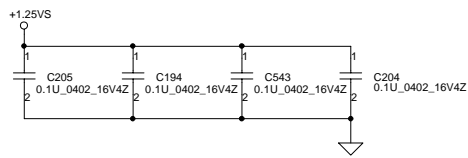
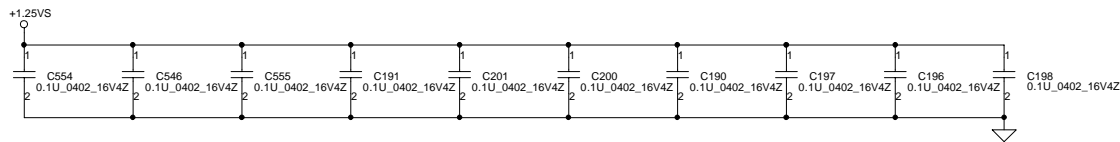
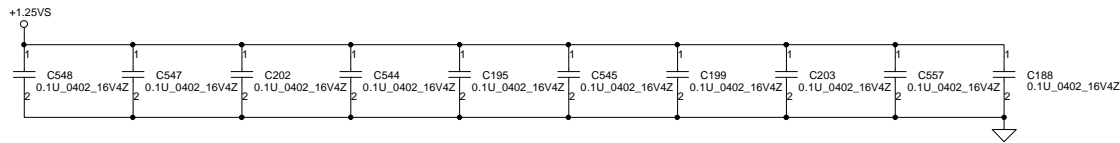
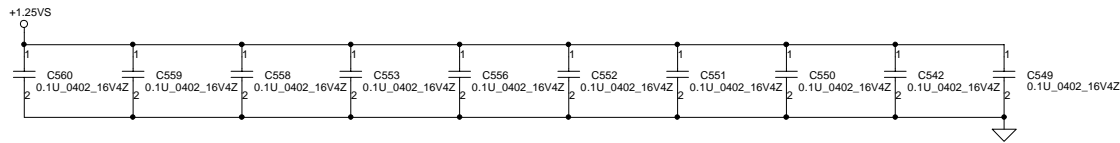
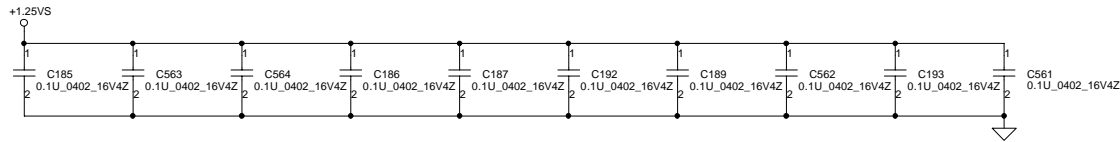
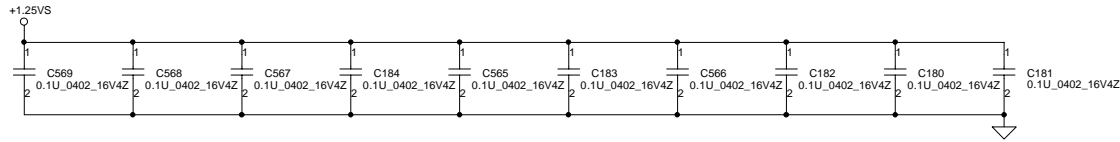
**Layout note :**

Distribute as close as possible to DDR-SODIMM.



**Layout note :**

Place one cap close to every 2 pull up resistors termination to +1.25V



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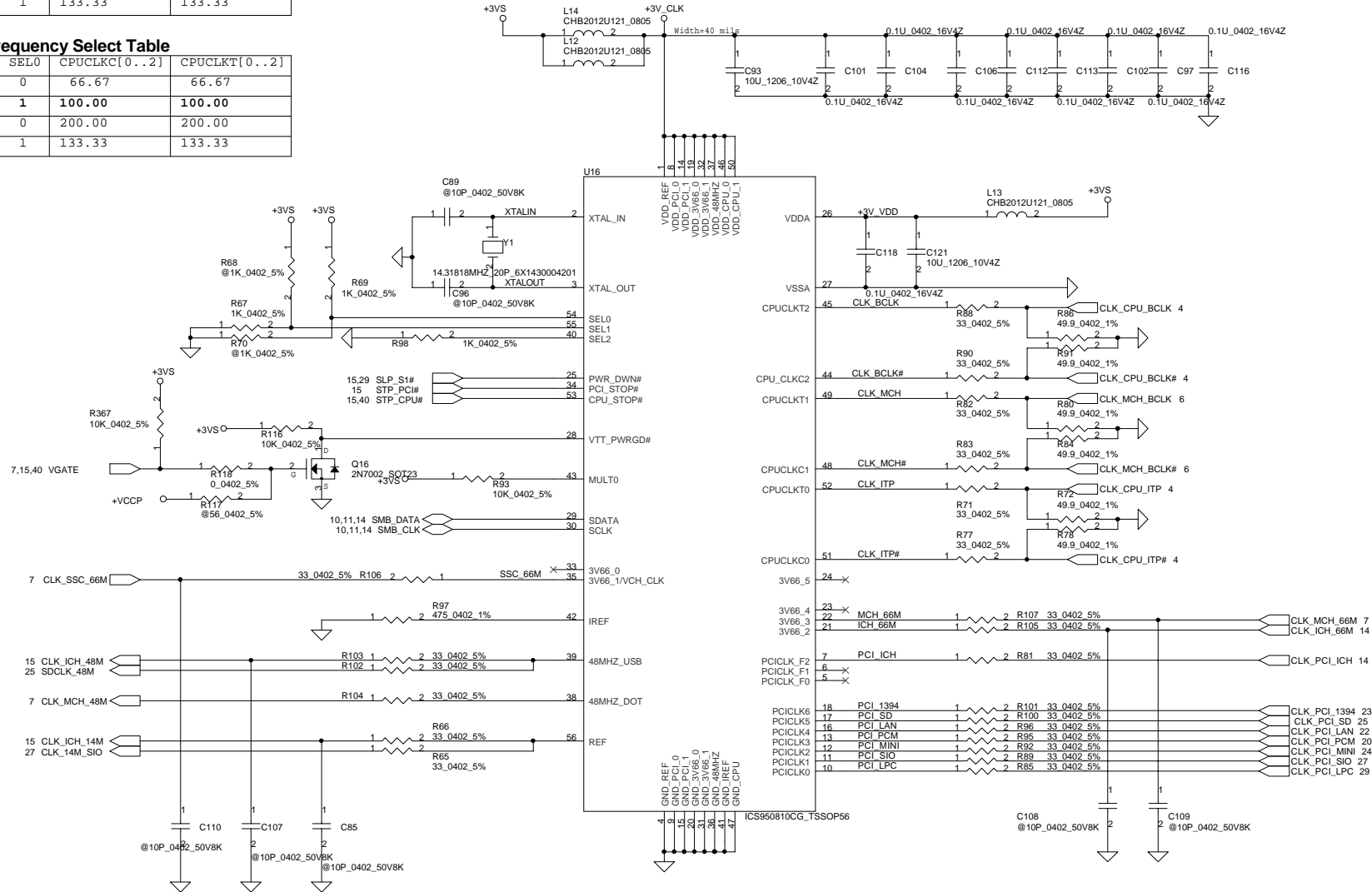
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ICS950810 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

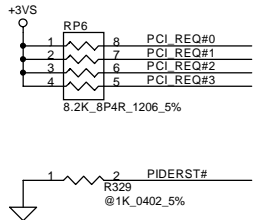
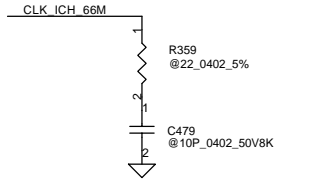
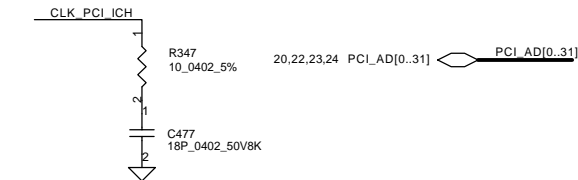
CY28346-2 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

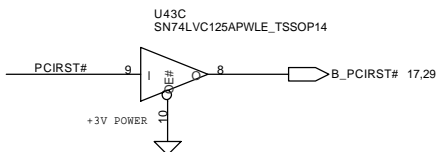
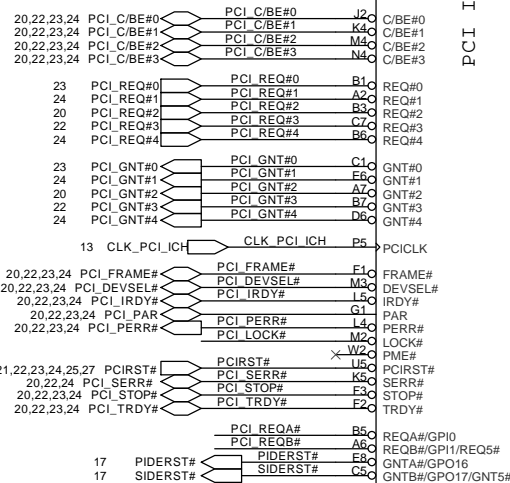
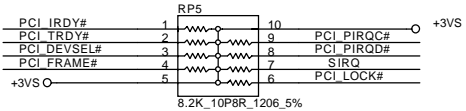
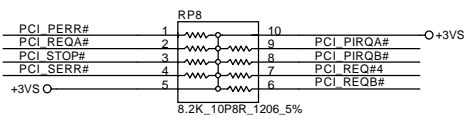


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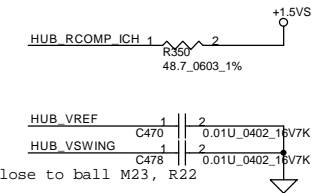
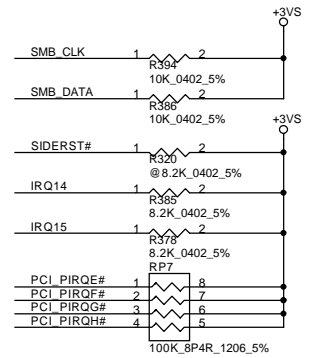
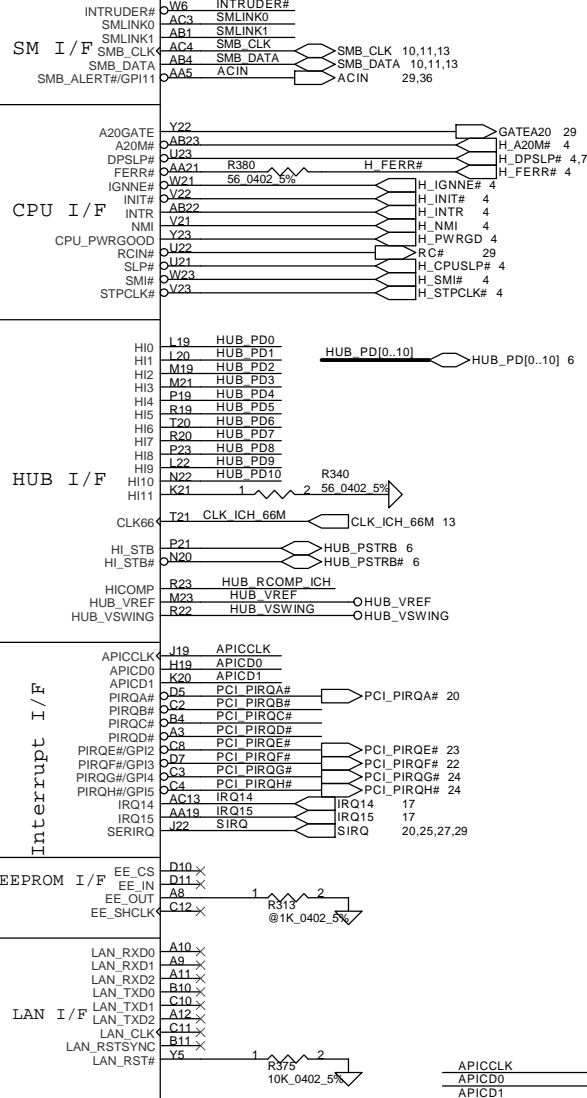
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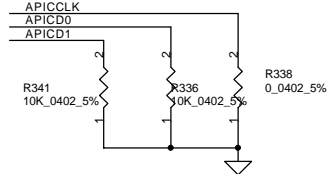
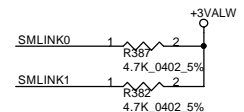
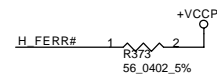
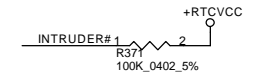
**PCI Pullups**



**ICH4**

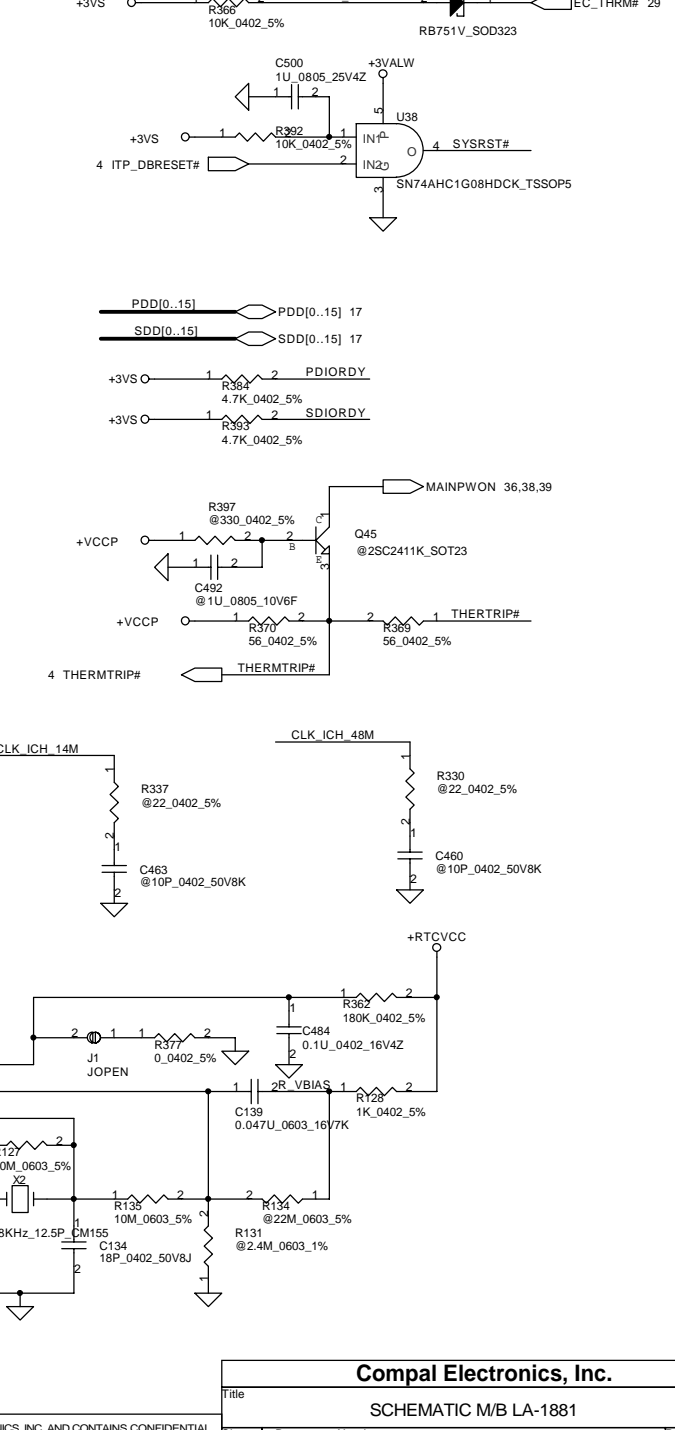
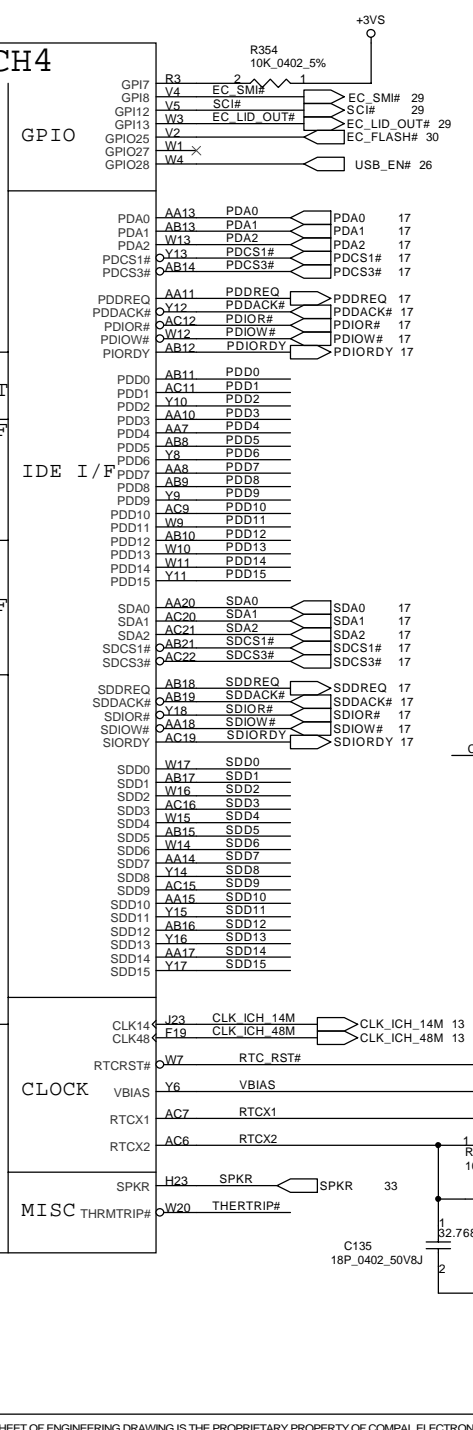
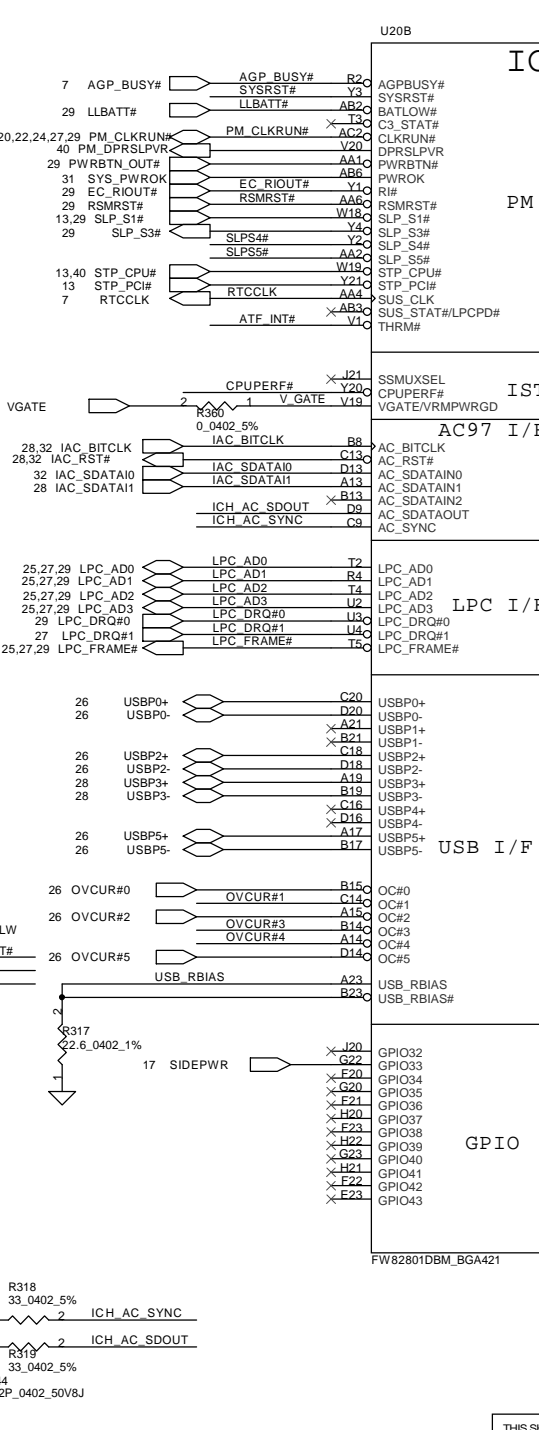
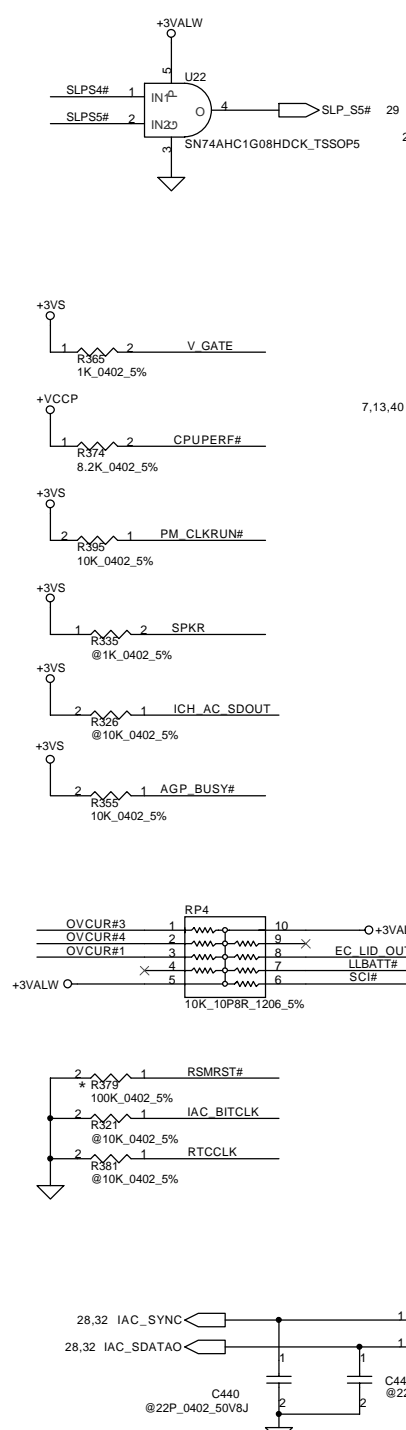


Place close to ball M23, R22

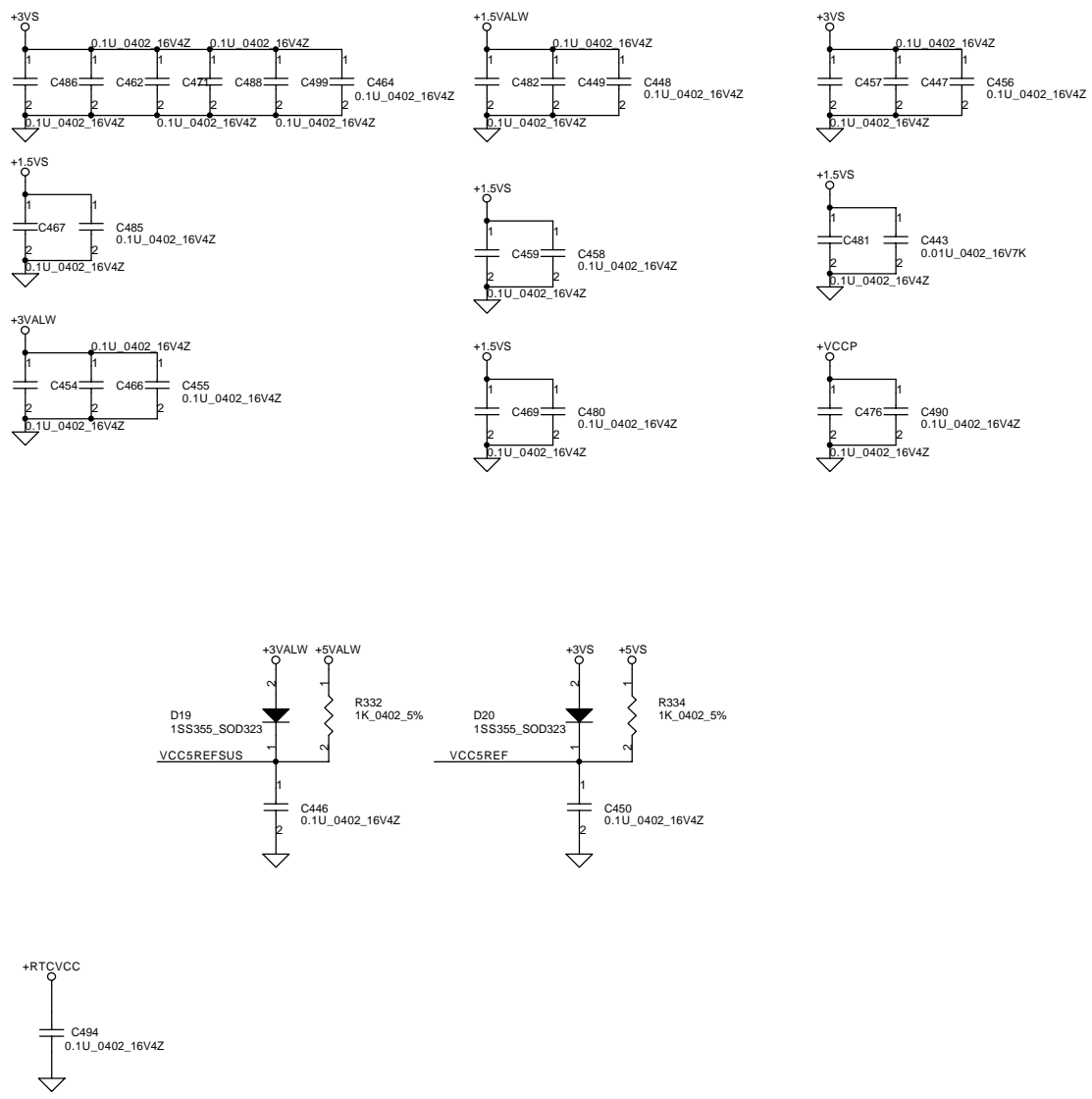
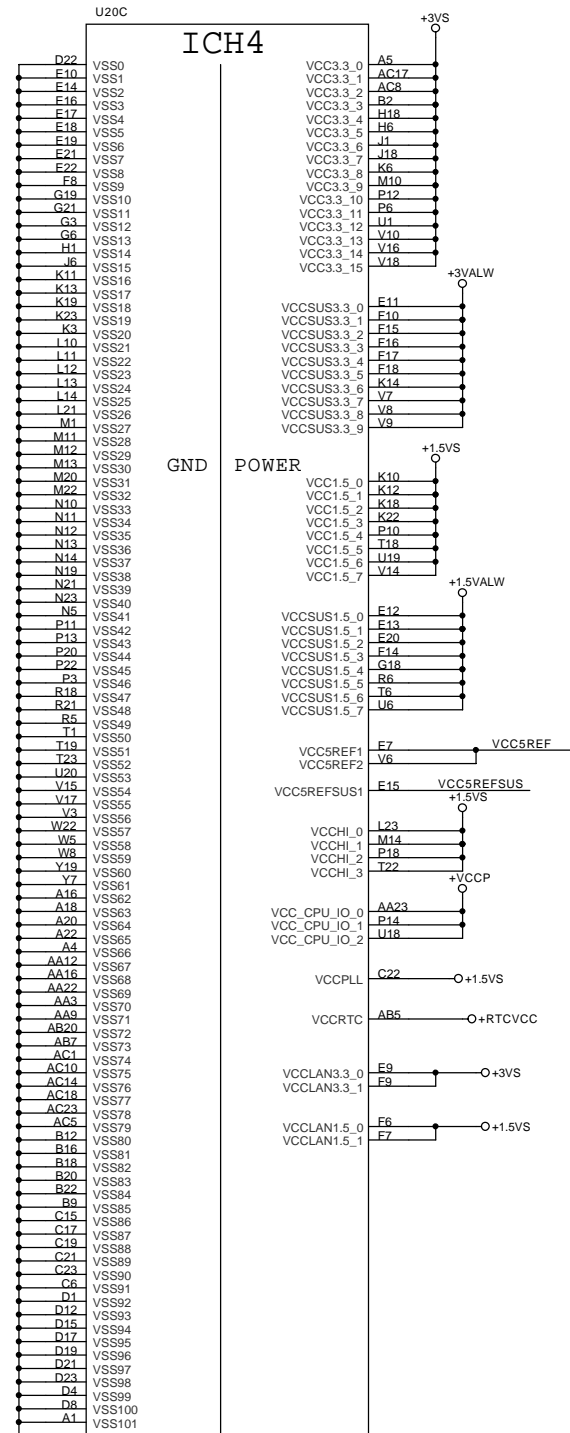


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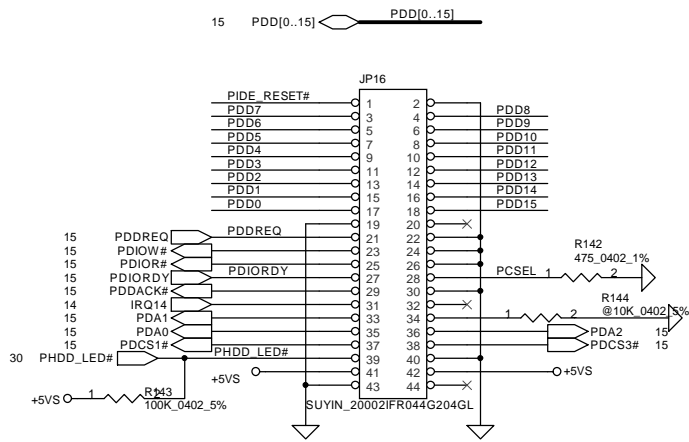
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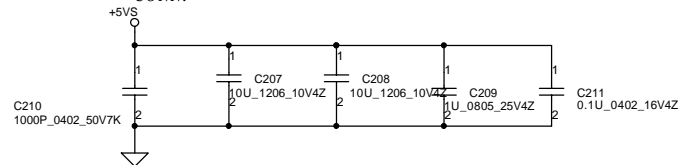
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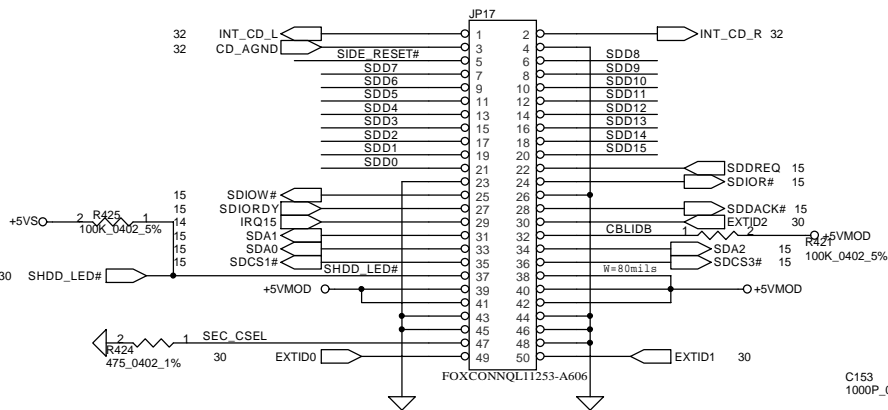
### HDD Connector



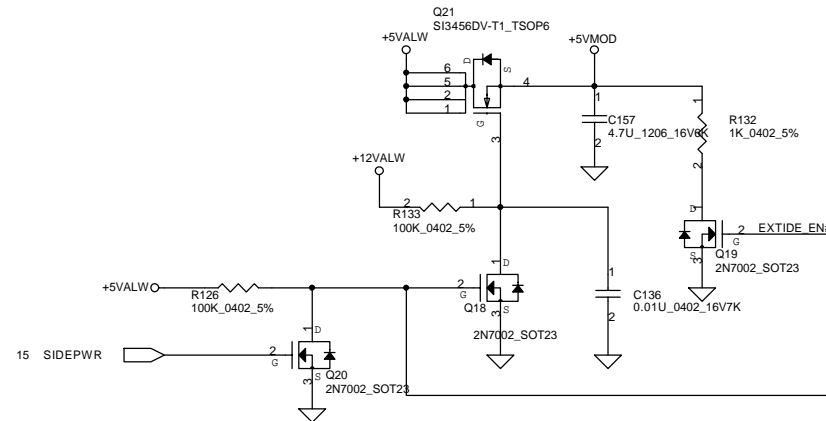
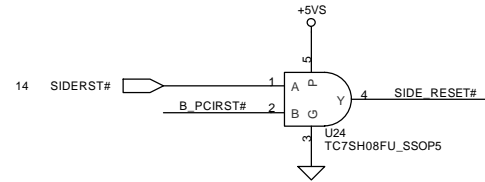
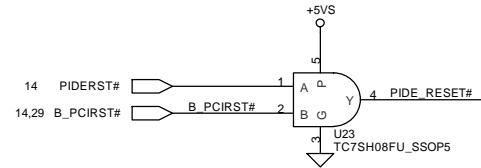
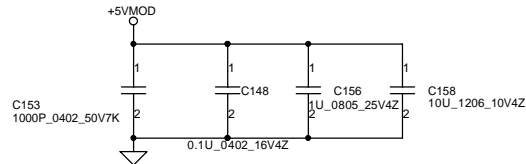
#### Placea caps. near HDD CONN.



### CD-ROM Connector



#### Placea caps. near CDROM CONN.

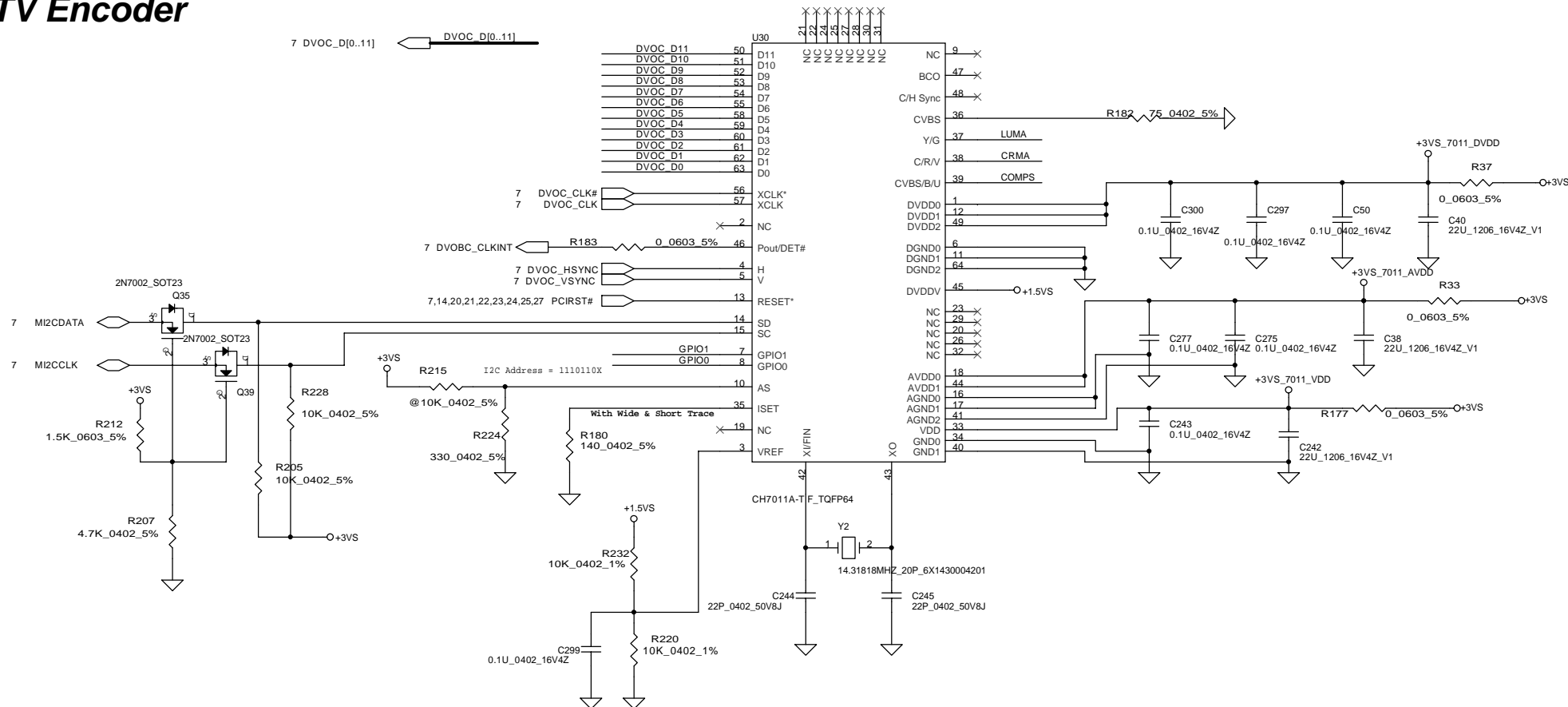


SI3456DV: N CHANNEL  
VGS: 4.5V, RDS: 65 mOHM  
Id(MAX): 5.1A  
VGS,+20V

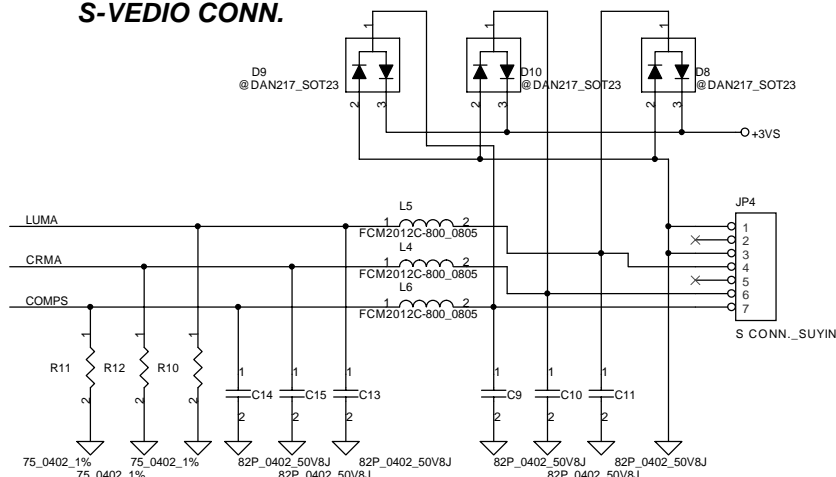
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# TV Encoder



## S-VIDEO CONN.

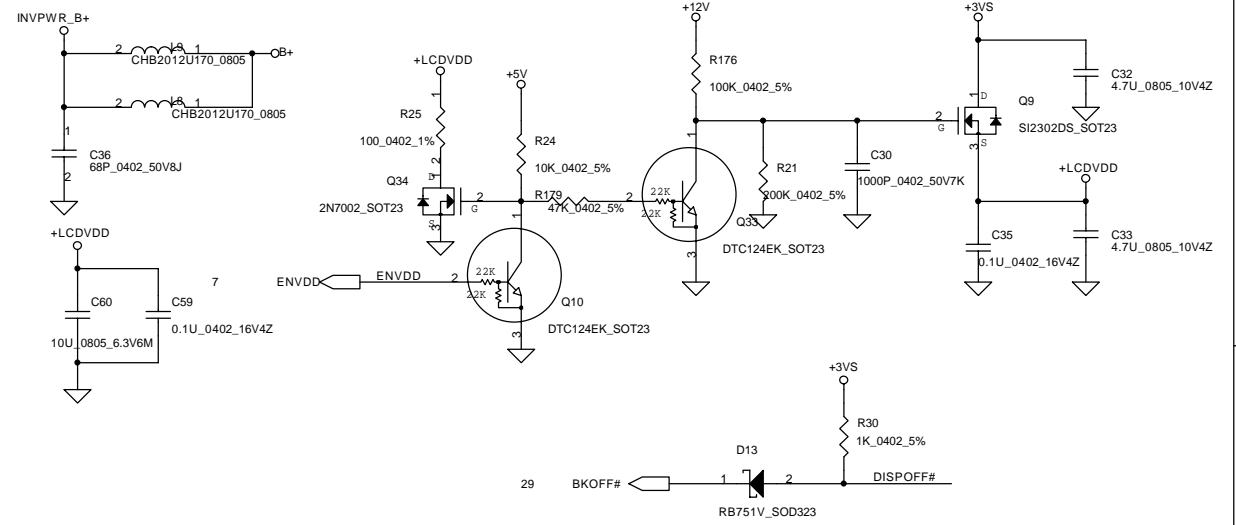
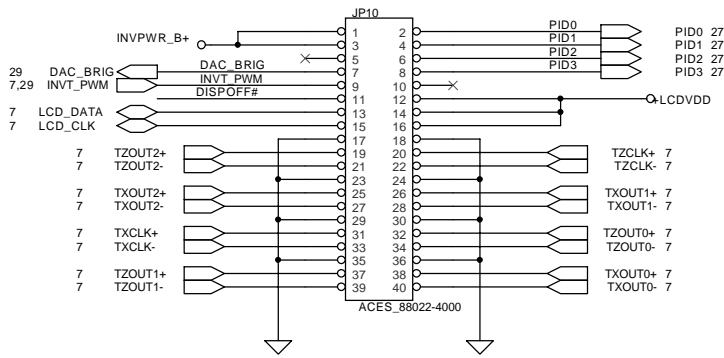


**Pull High: Default PAL**  
**Pull Low: Default NTSC**

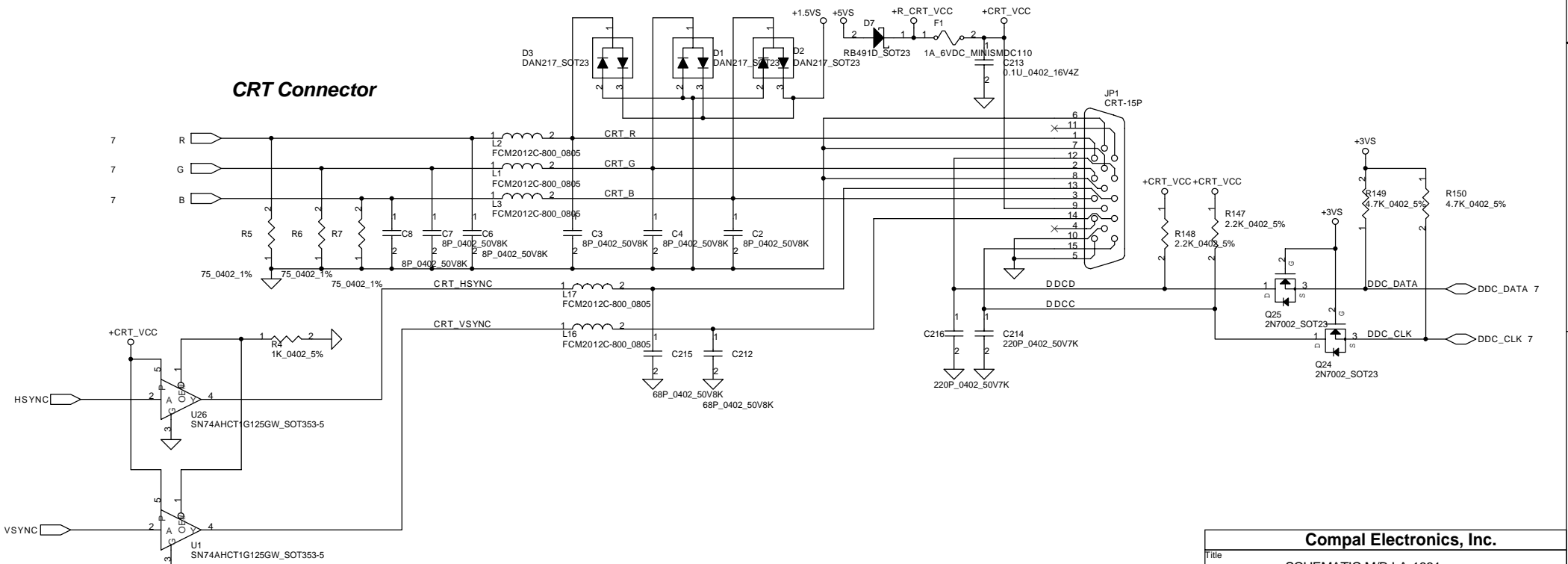
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### LVDS Connector

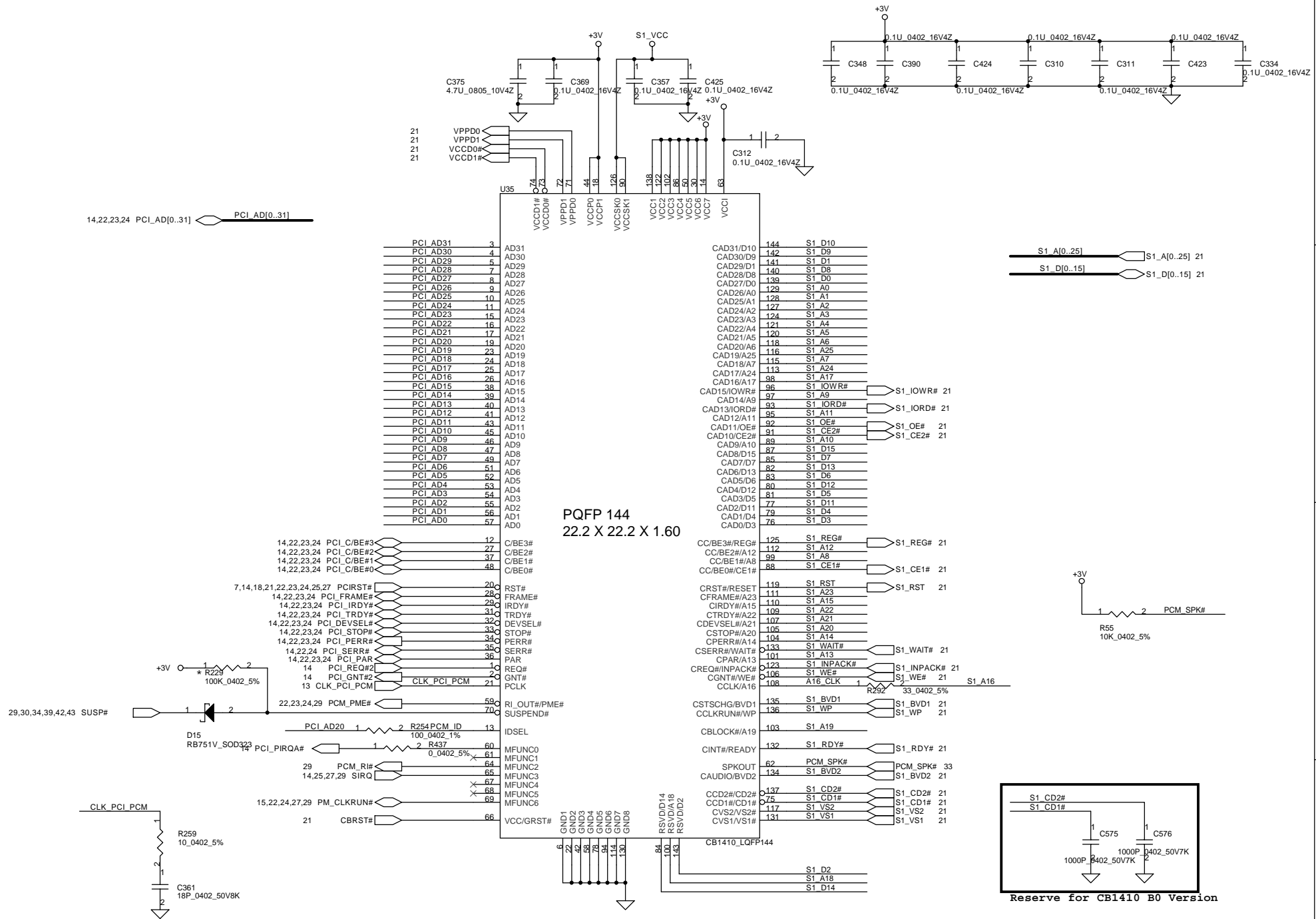


### CRT Connector



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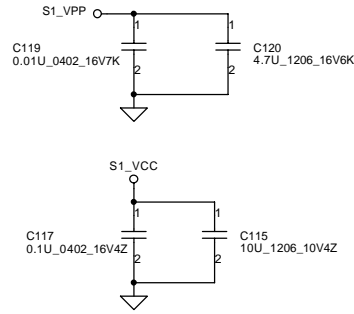
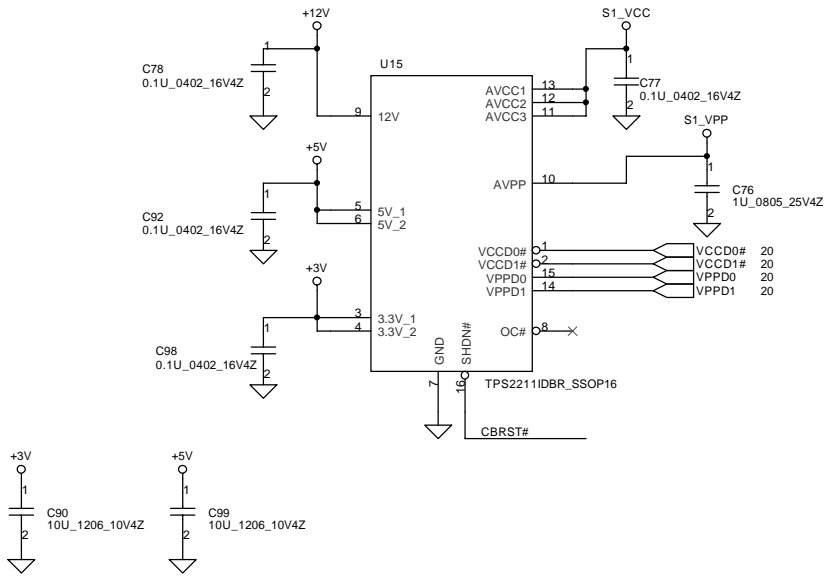


**PQFP 144**  
22.2 X 22.2 X 1.60

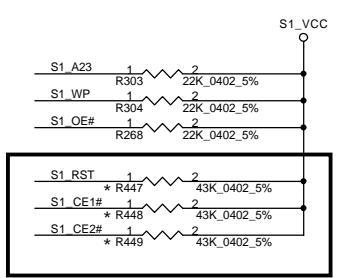
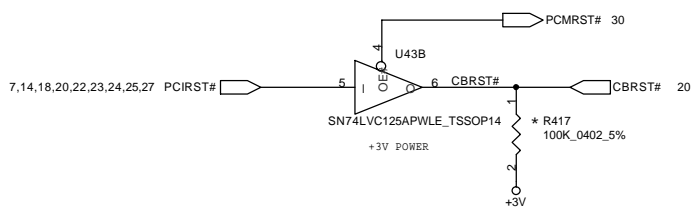
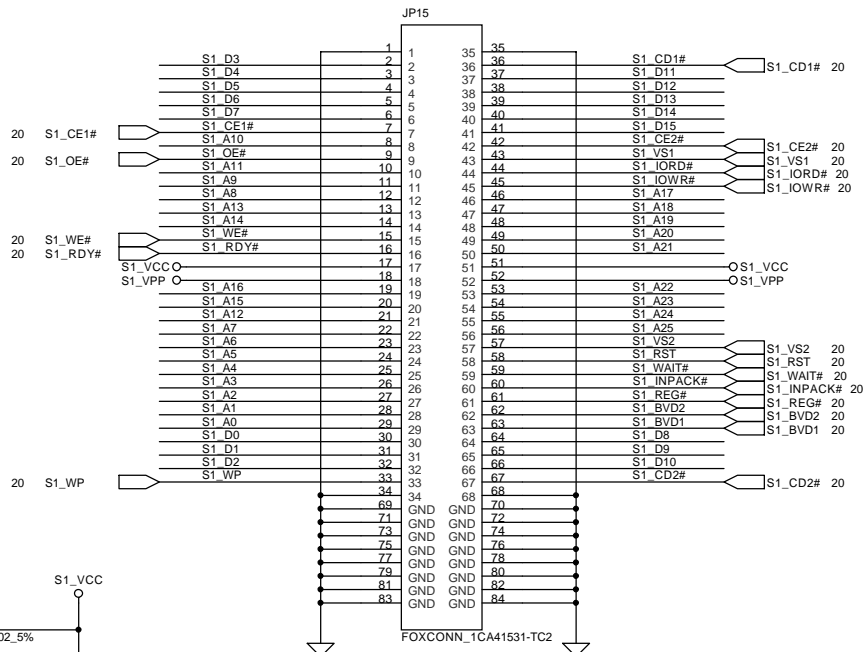
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# PCMCIA Power Controller



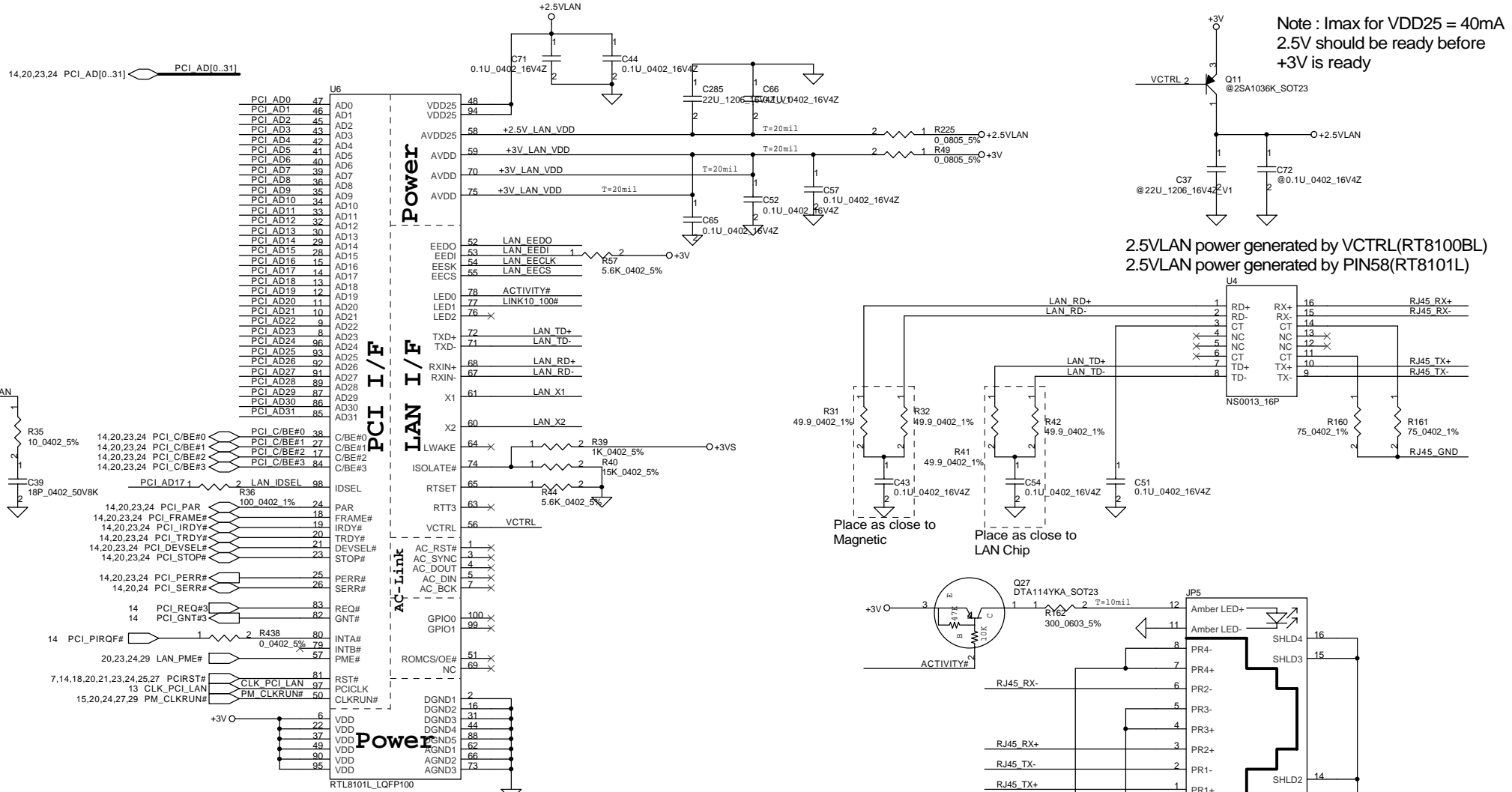
# CardBus Socket



Reserve for CB1410 B0 Version

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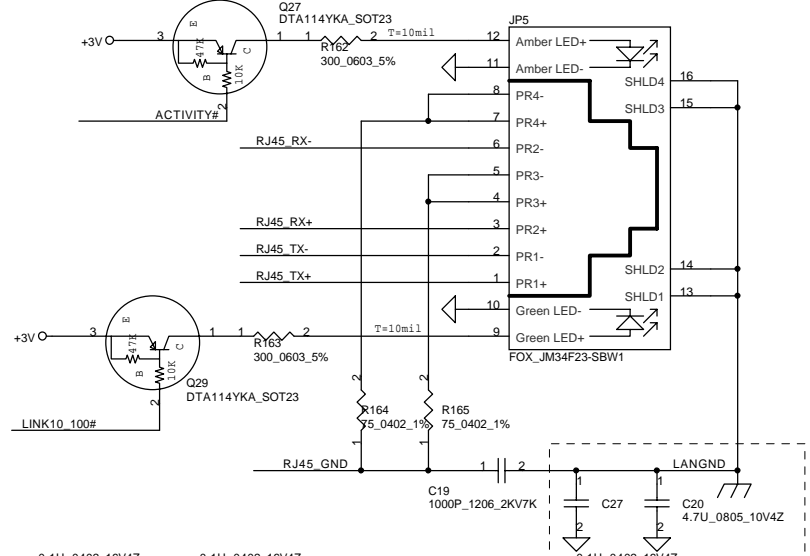


Note : I<sub>max</sub> for VDD25 = 40mA  
2.5V should be ready before  
+3V is ready

2.5VLAN power generated by VCTRL(RT8100BL)  
2.5VLAN power generated by PIN58(RT8101L)

Place as close to  
Magnetic

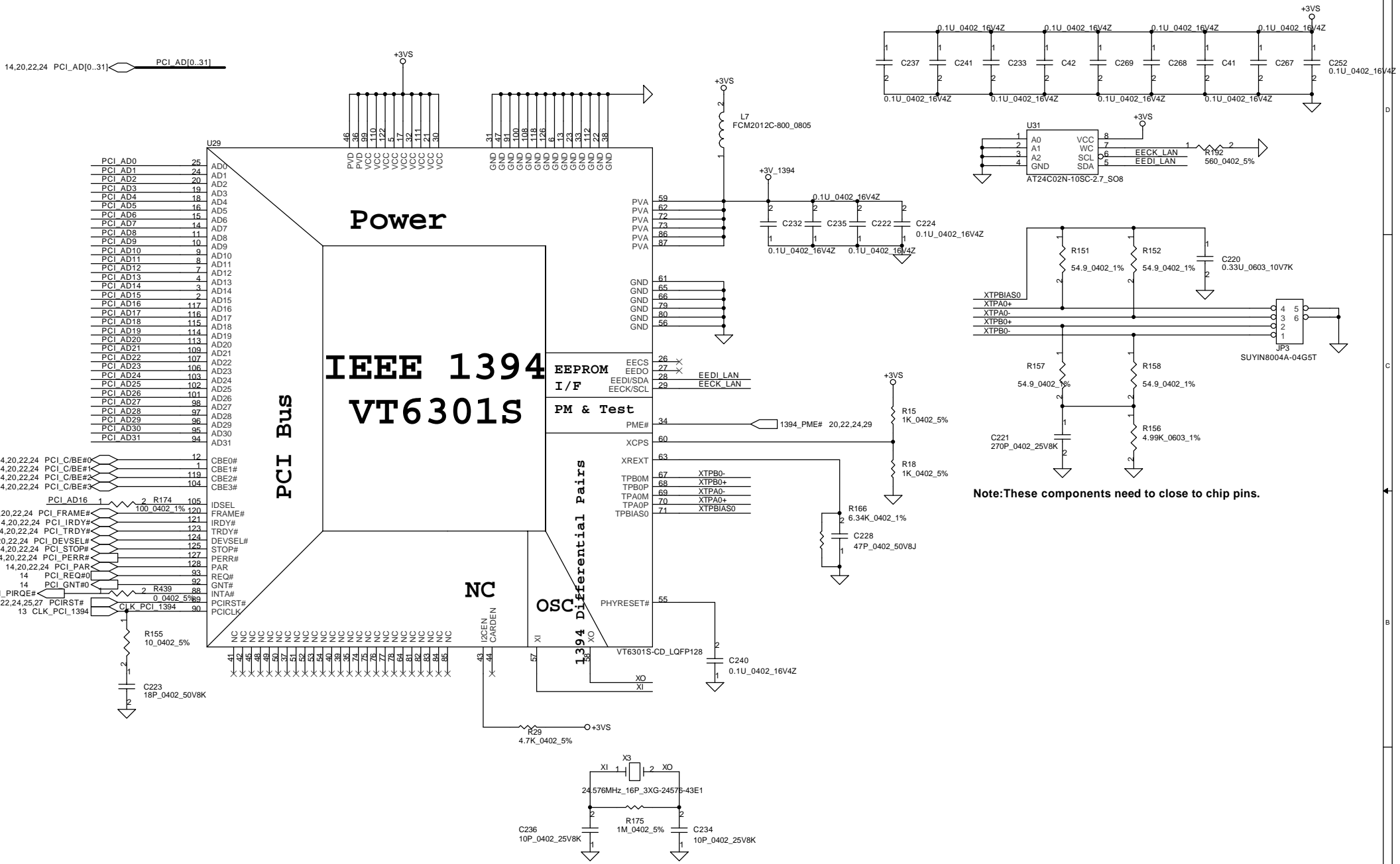
Place as close to  
LAN Chip



Termination plane should be copied to chassis ground and also depends on safety concern

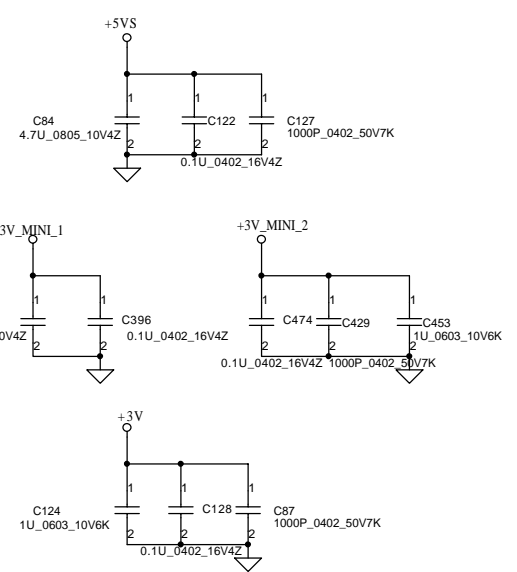
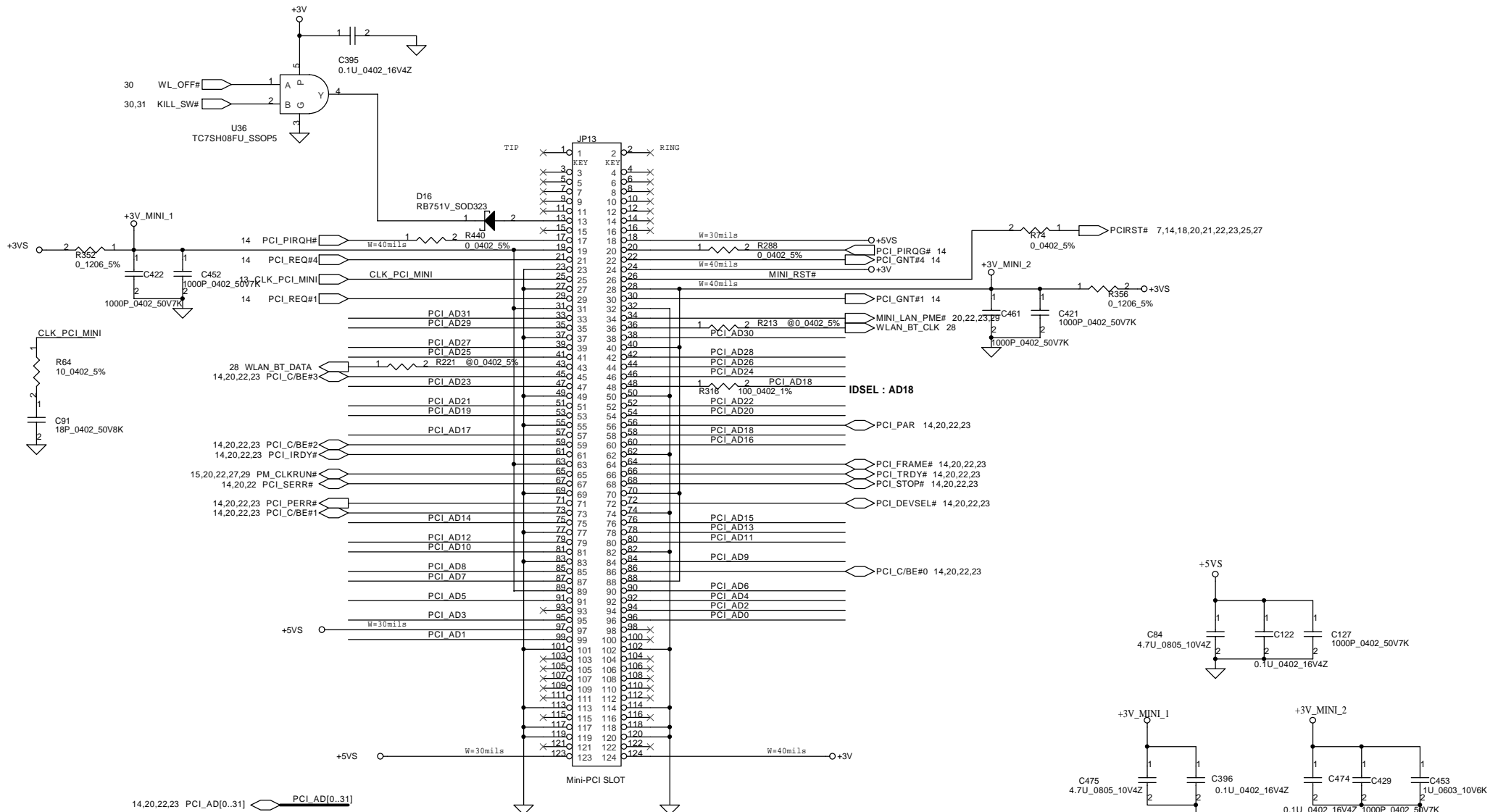
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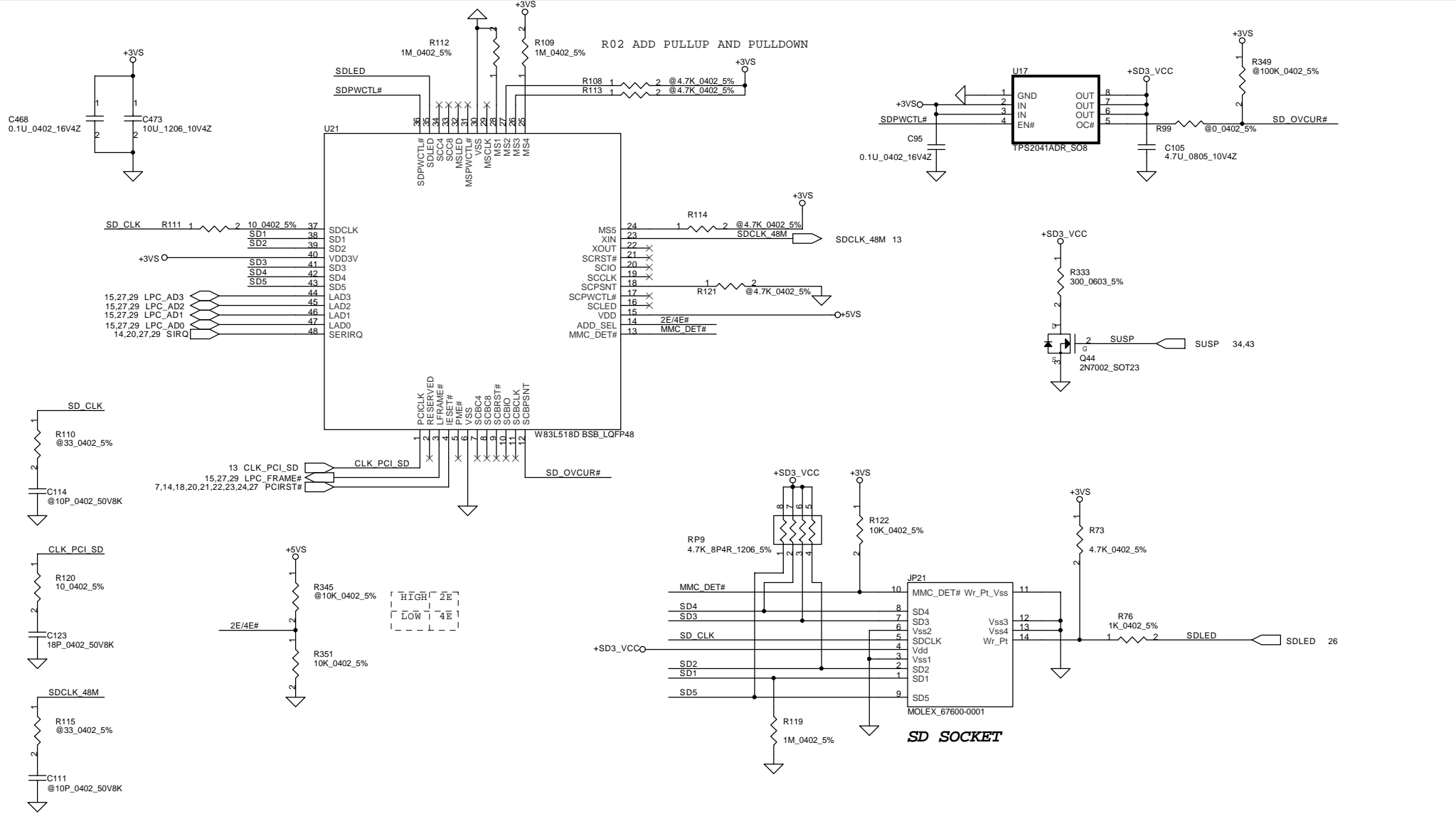
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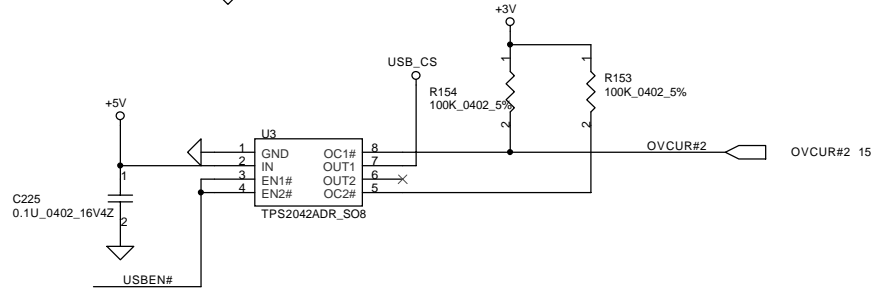
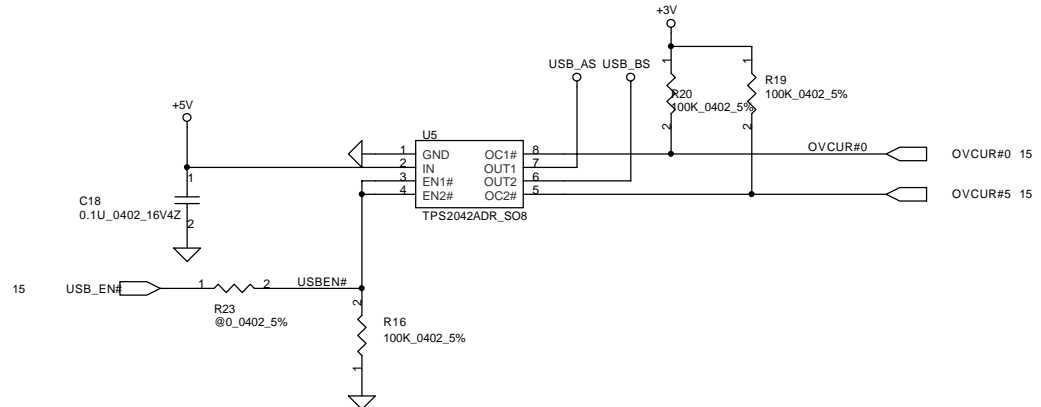
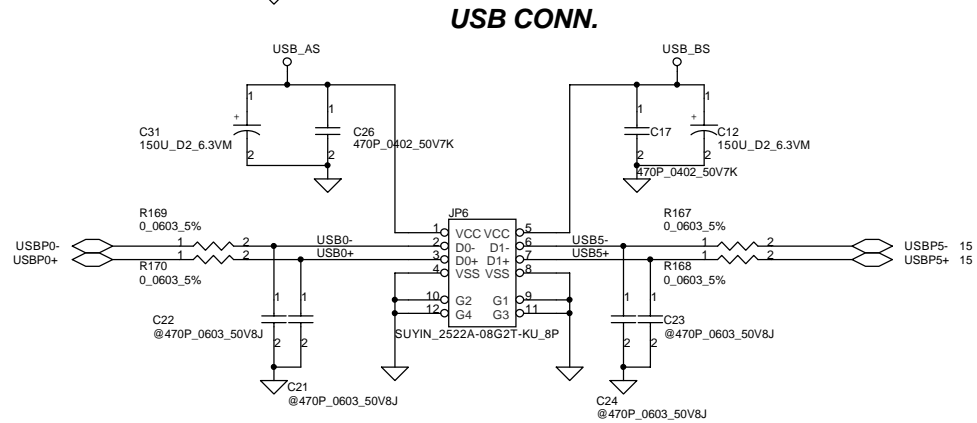
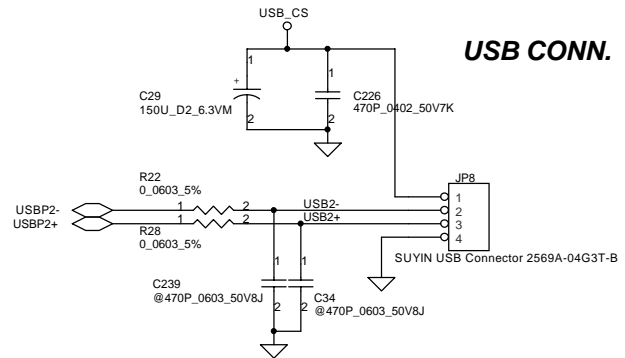
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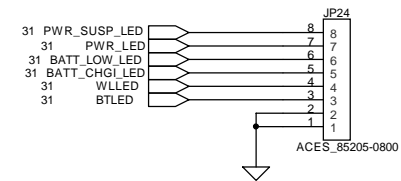
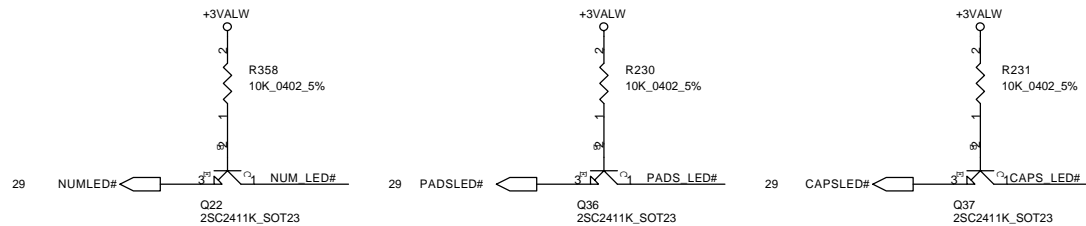


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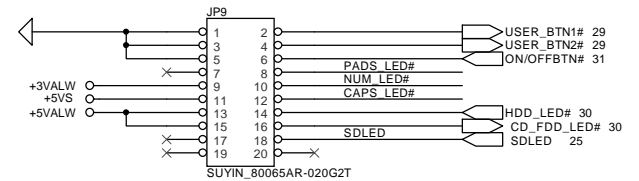
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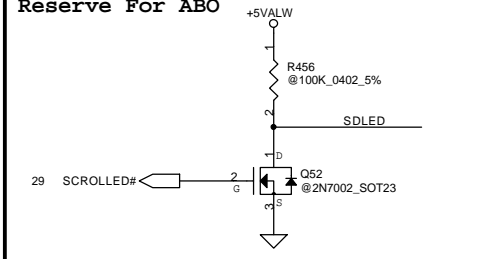
### LED/B CONN.



### POWER/B CONN.



### Reserve For ABO

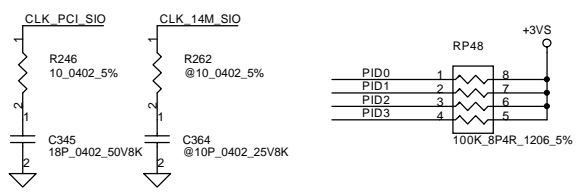
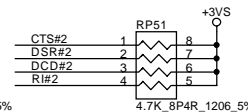
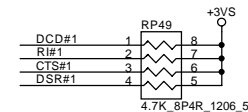
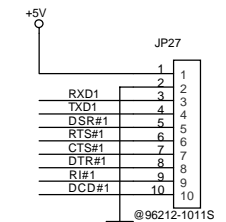
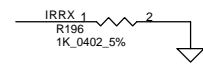
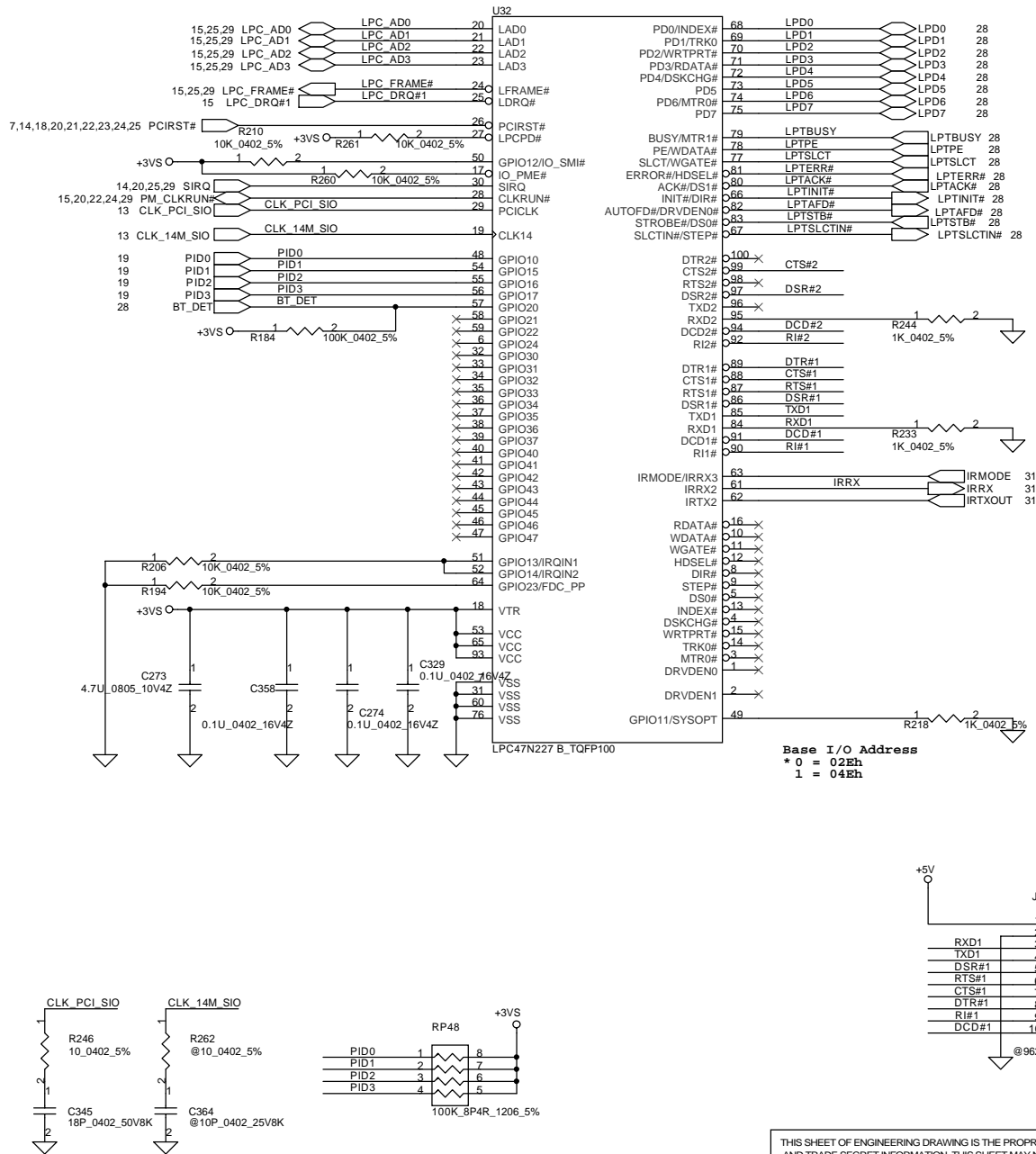


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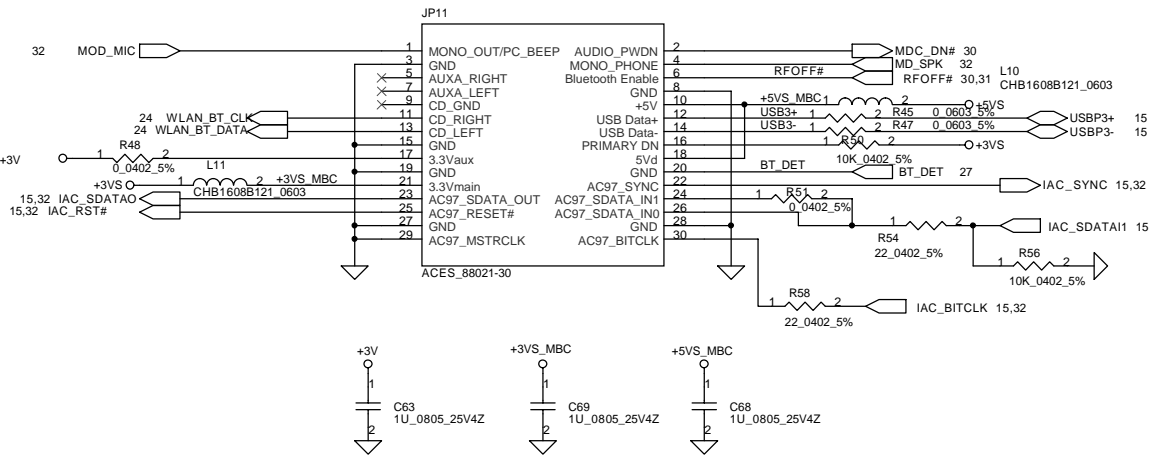
# SUPER I/O SMC FDC47N227



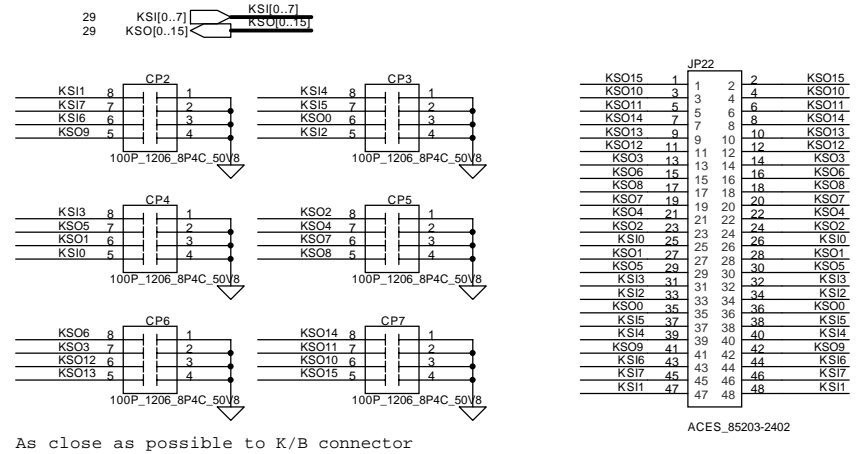
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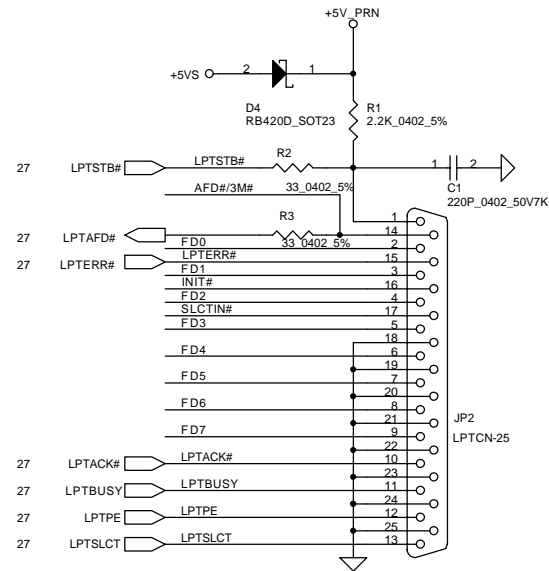
### MBC CONN.



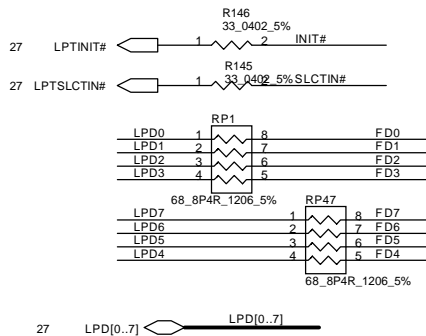
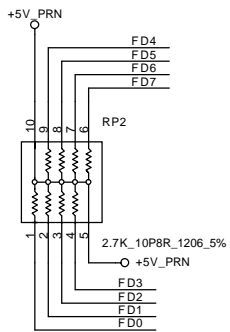
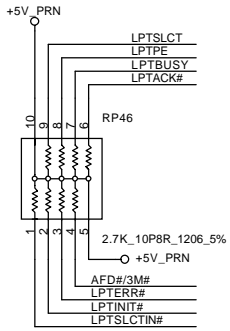
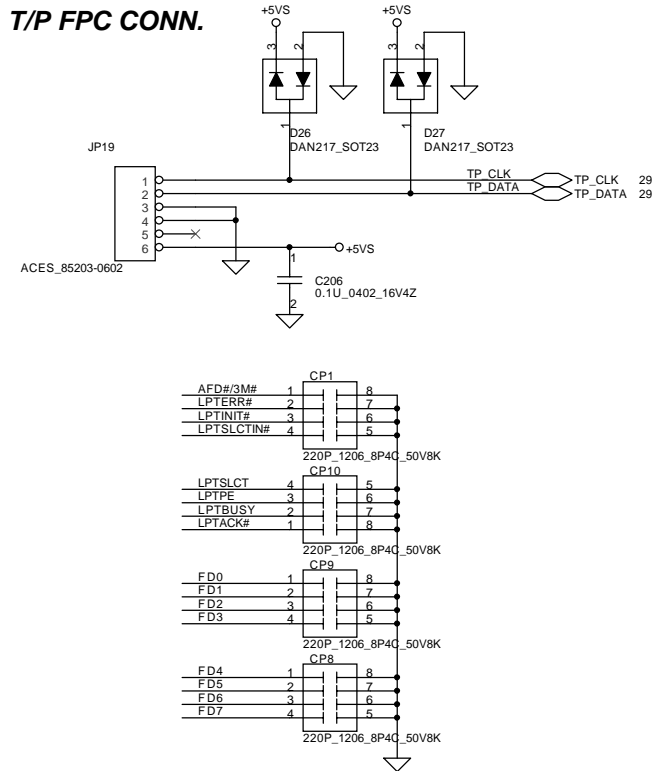
### INT\_KBD CONN.



### PARALLEL PORT



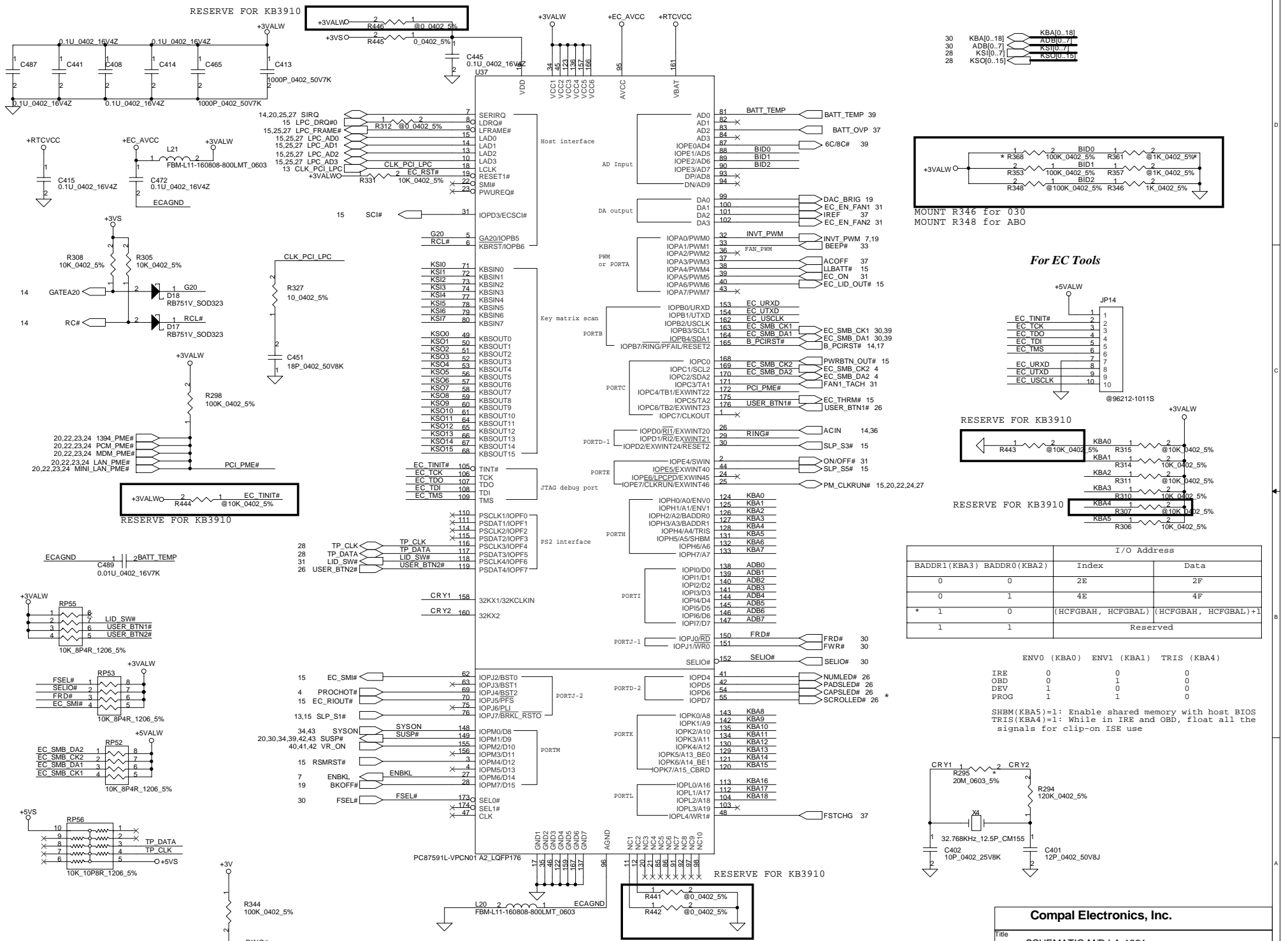
### T/P FPC CONN.



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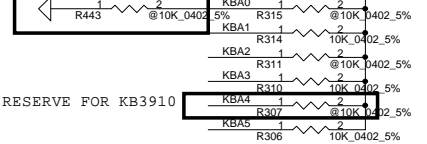
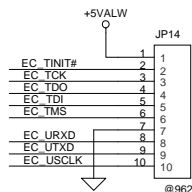
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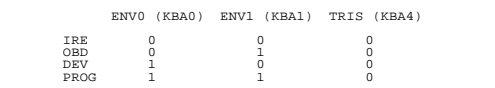


MOUNT R346 For 030  
MOUNT R348 for ABO

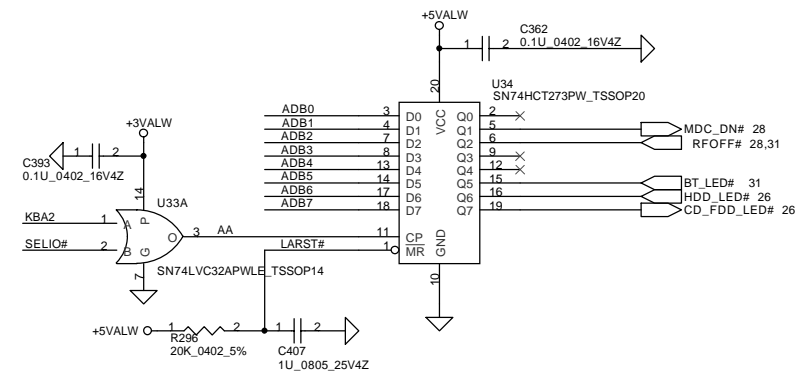
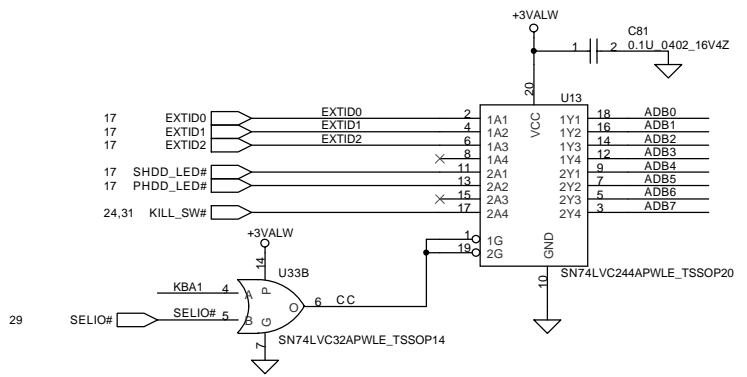
### For EC Tools



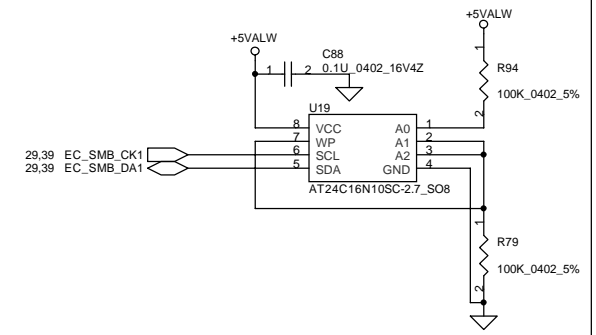
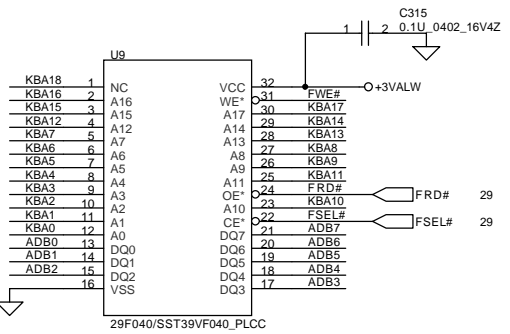
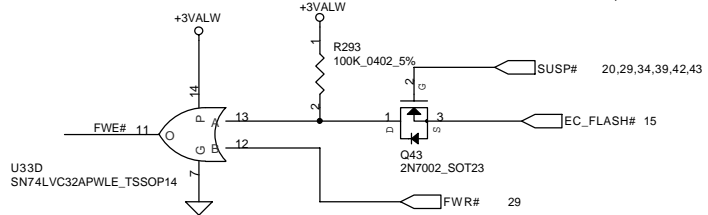
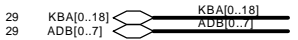
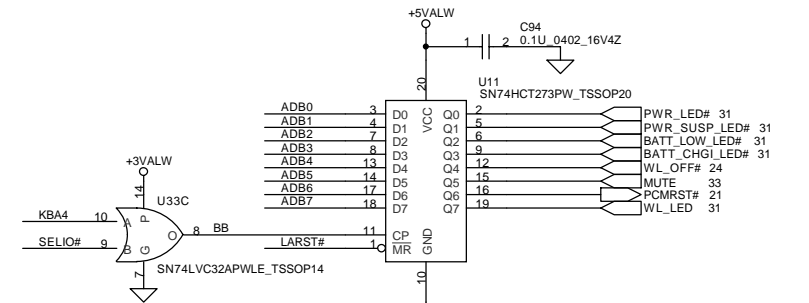
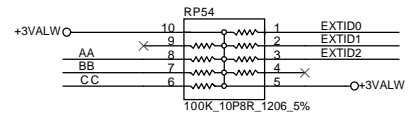
I/O Address		Index	Data
BADDR1 (KBA3)	BADDR0 (KBA2)	2E	2F
0	0	4E	4F
* 1	0	(HCFGBAH, HCFGBAL) (HCFGGBAH, HCFGGBAL)+1	
1	1	Reserved	



SHBM(KBA5)=1: Enable shared memory with host BIOS  
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on use

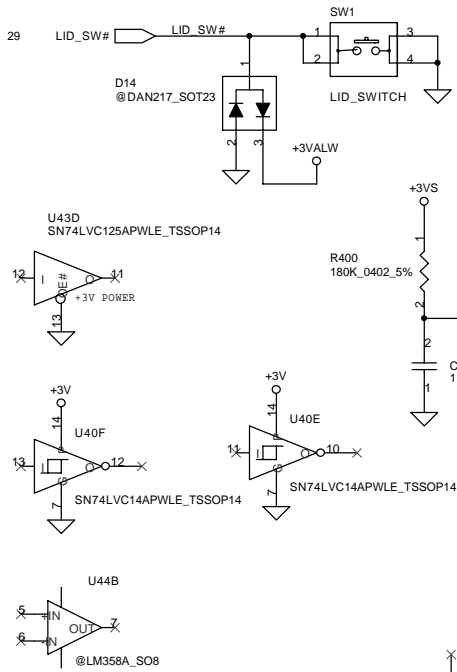


EXTID2	EXTID1	EXTID0	Module
0	0	0	FDD
0	0	1	CDROM
0	1	1	2ndHDD
1	1	1	NO Module

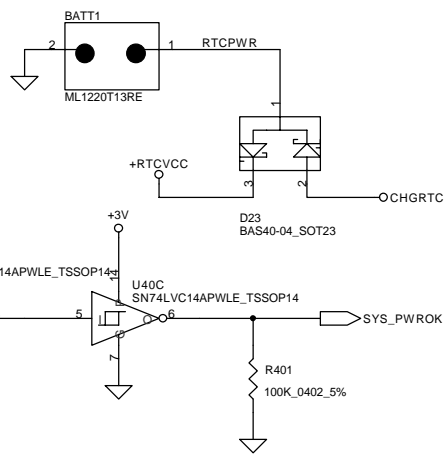


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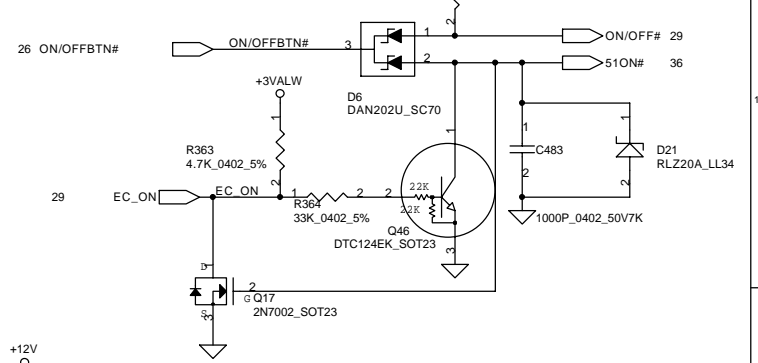
### Power ON Circuit



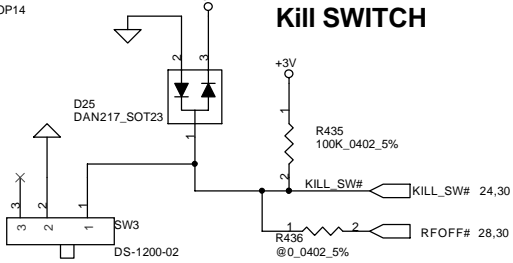
### RTC Battery



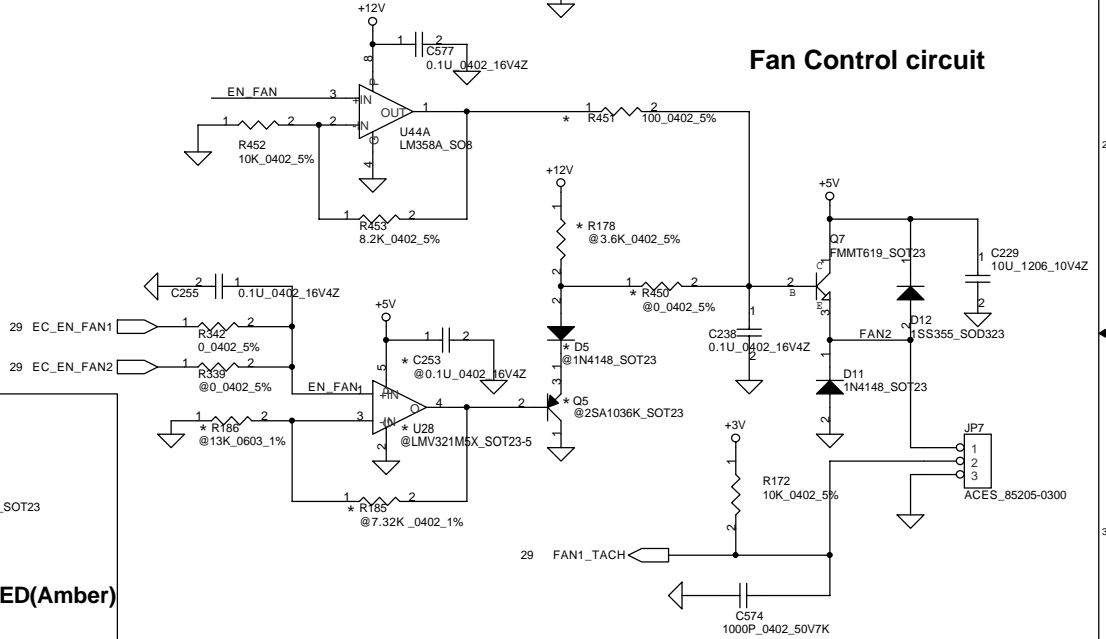
### Power BTN



### Kill SWITCH

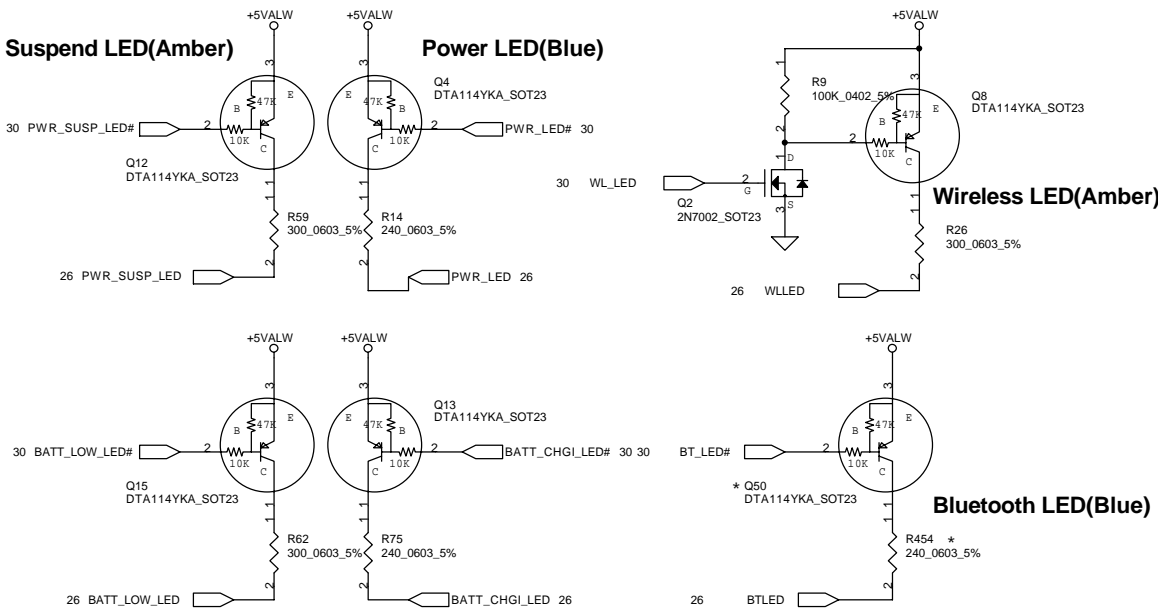


### Fan Control circuit

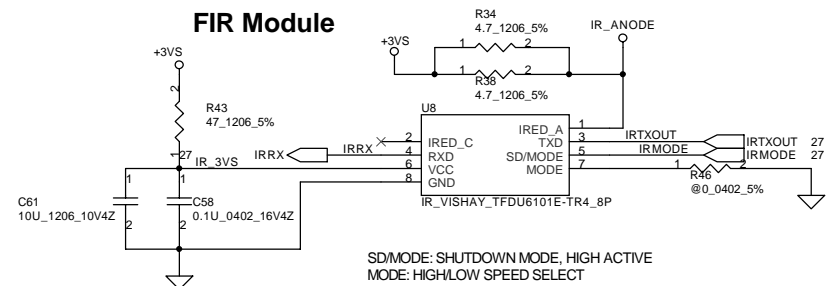


### Suspend LED(Amber)

### Power LED(Blue)



### FIR Module

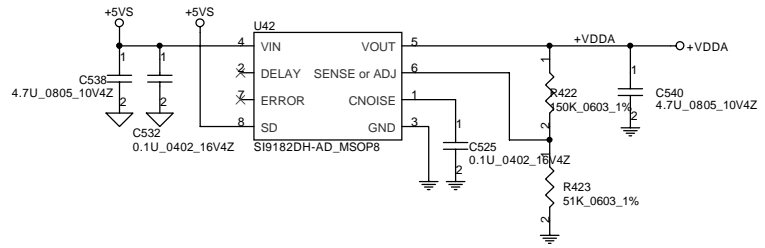


### Compal Electronics, Inc.

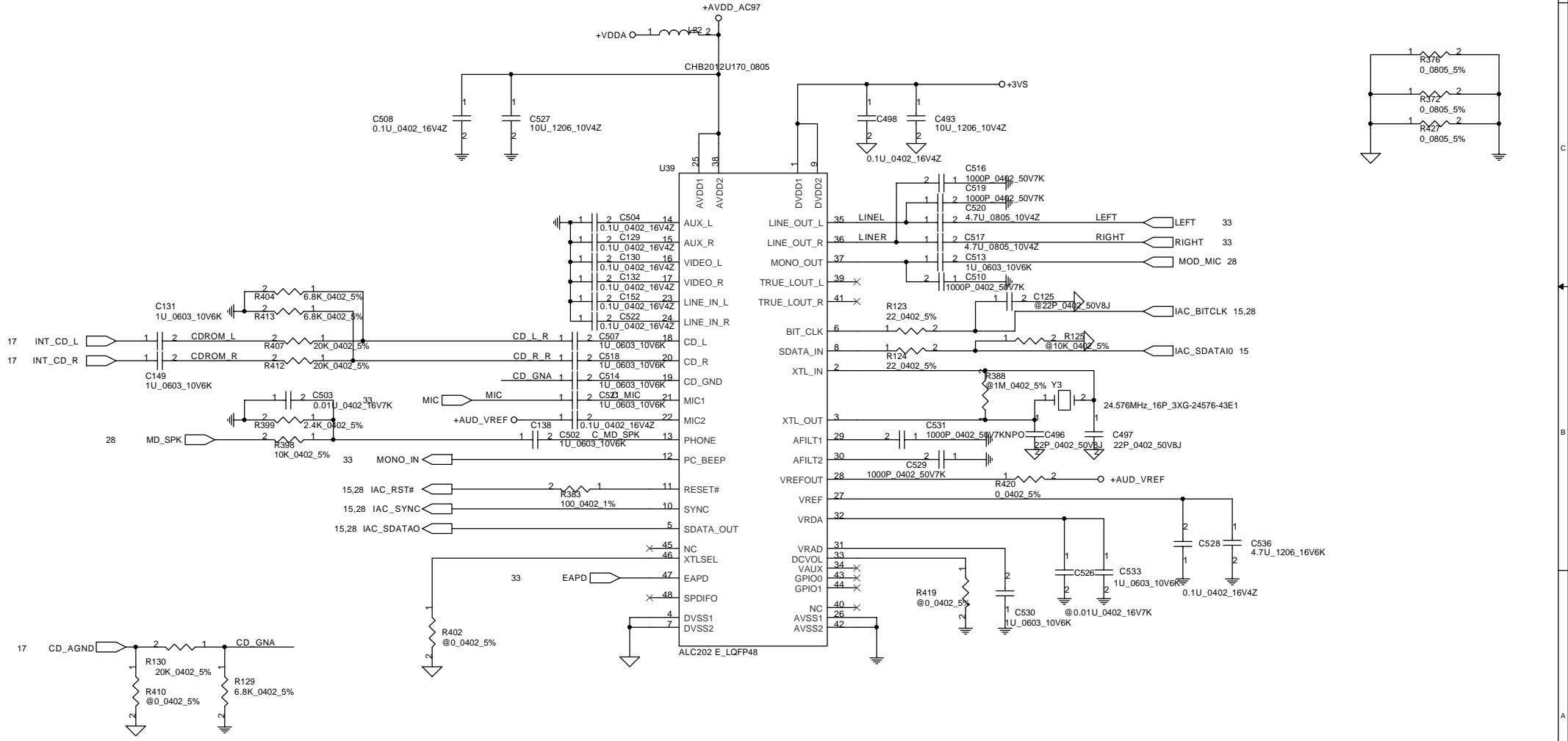
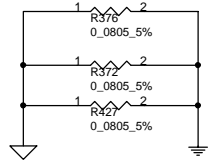
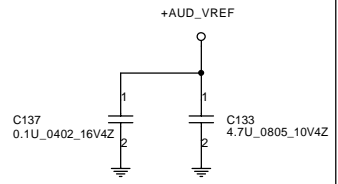
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# AC97 Codec



R402	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck



**Compal Electronics, Inc.**

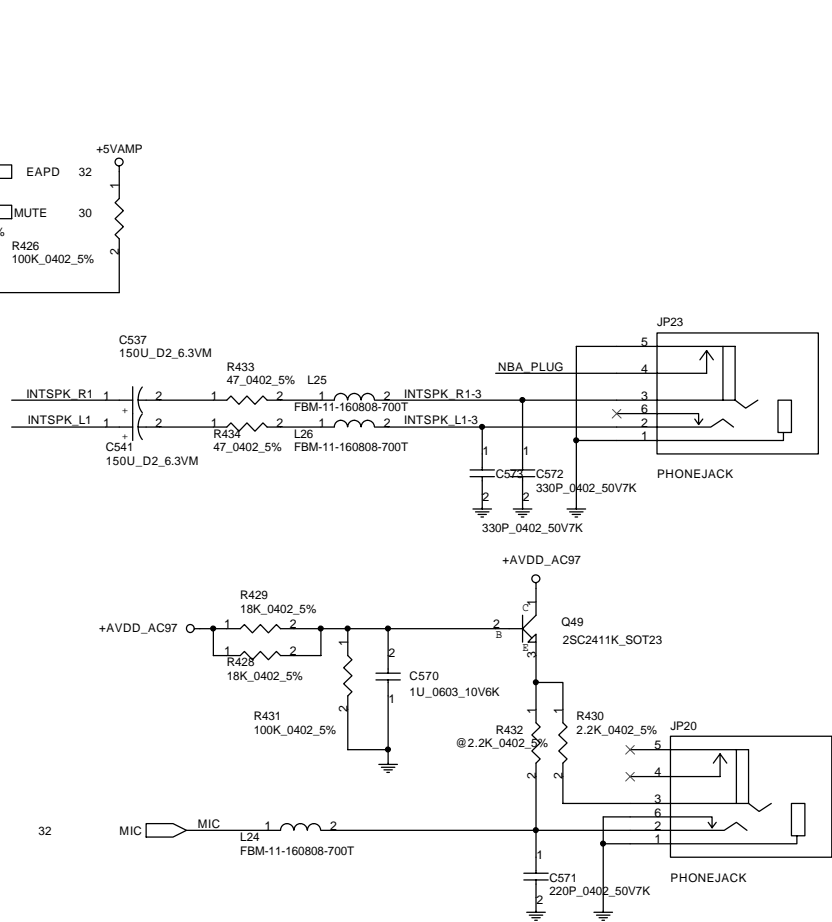
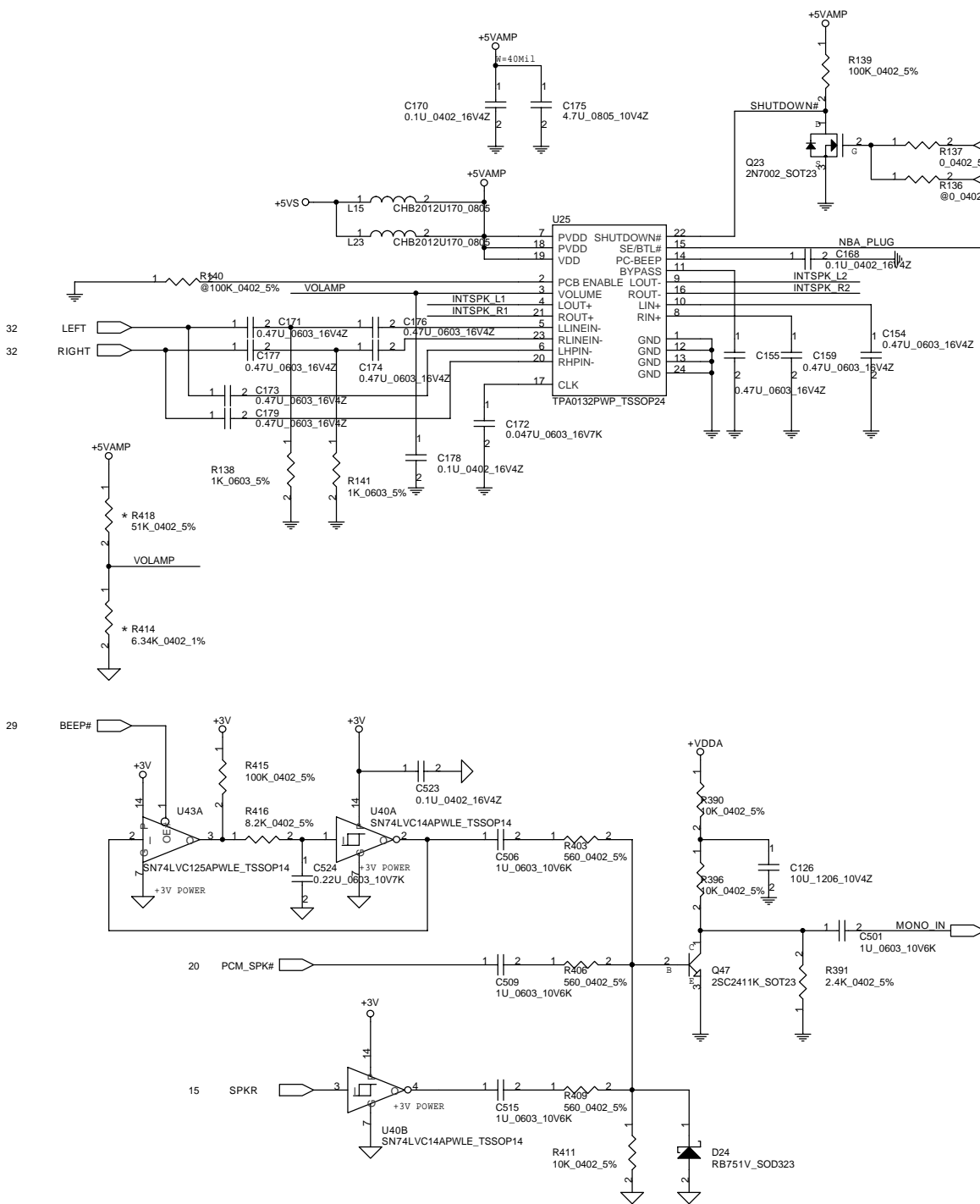
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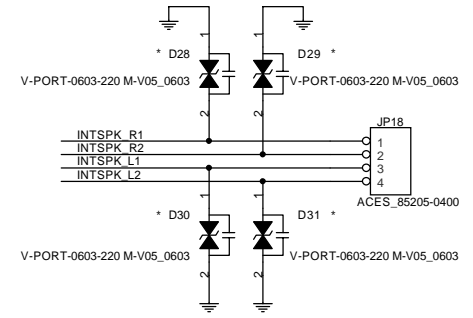
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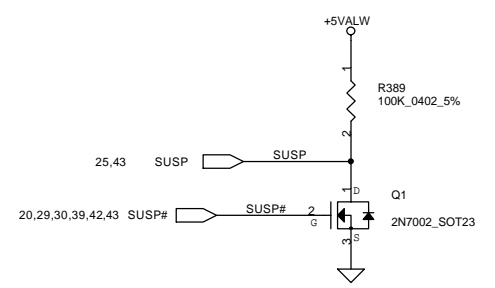
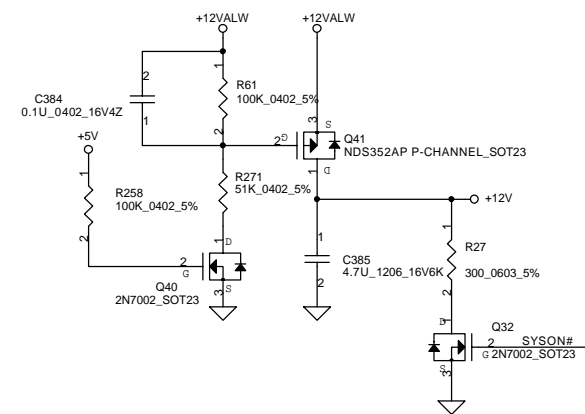
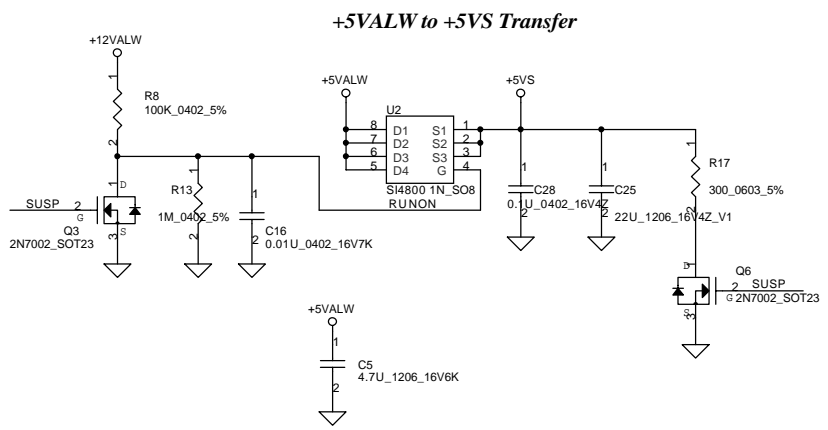
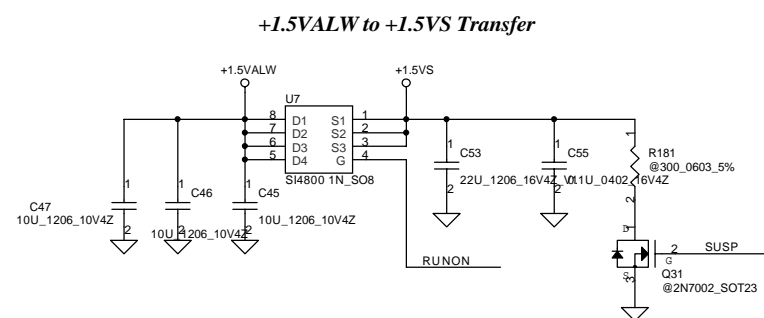
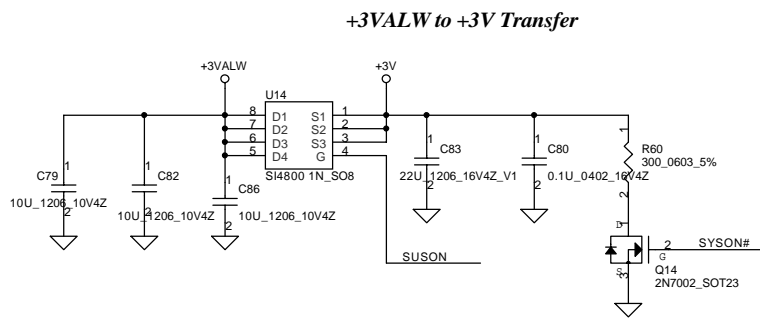
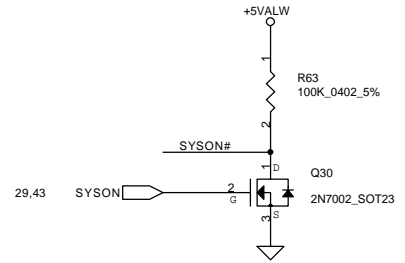
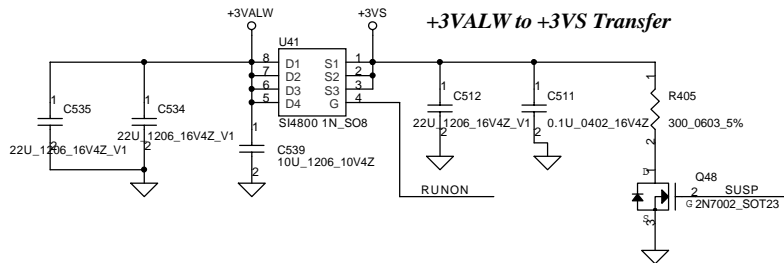
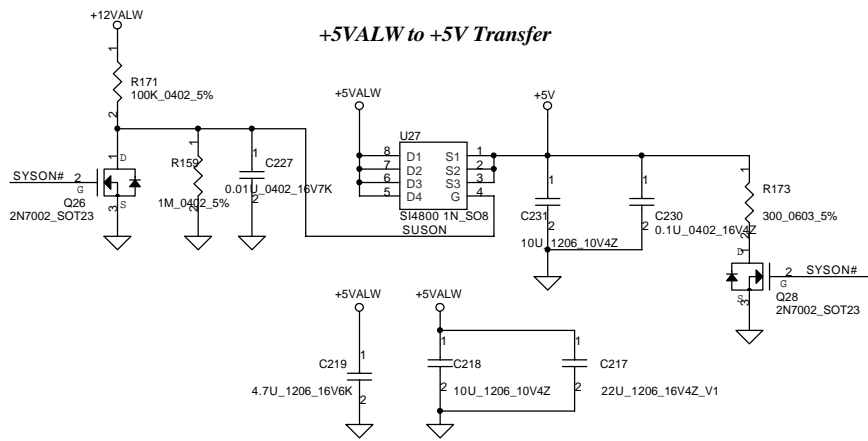


**SPEAKER CONN.**



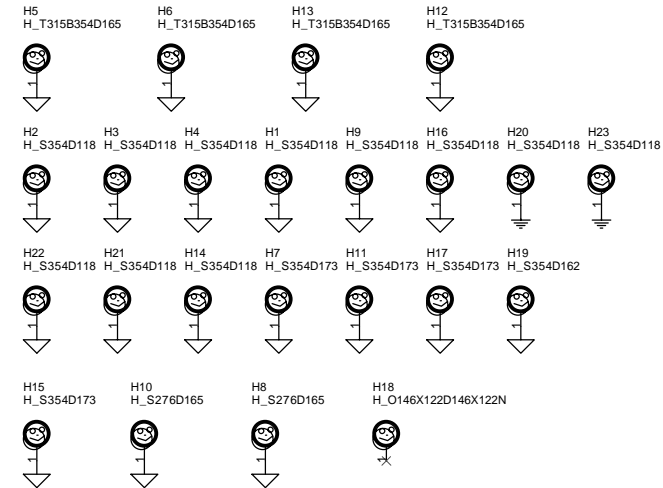
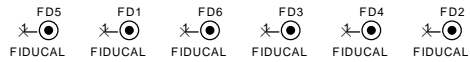
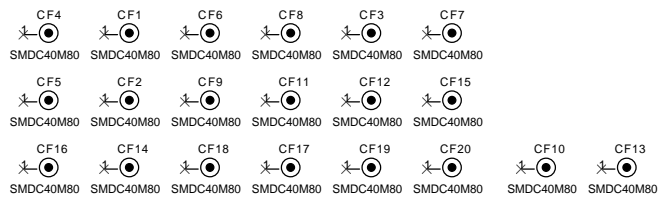
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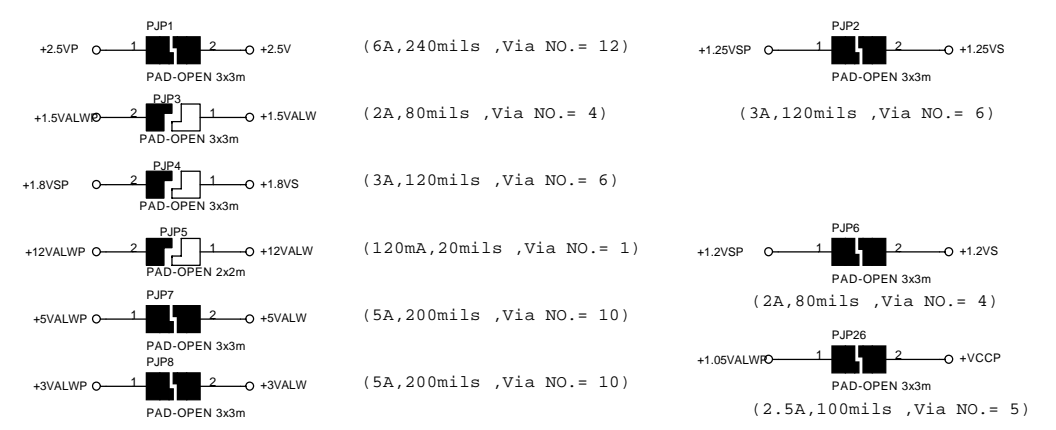
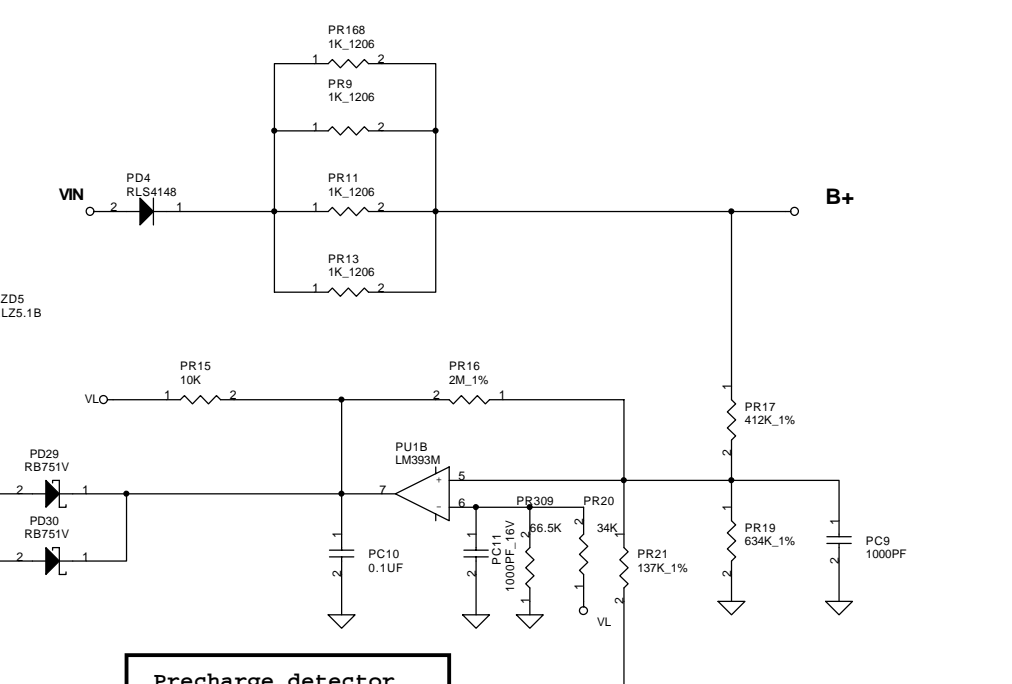
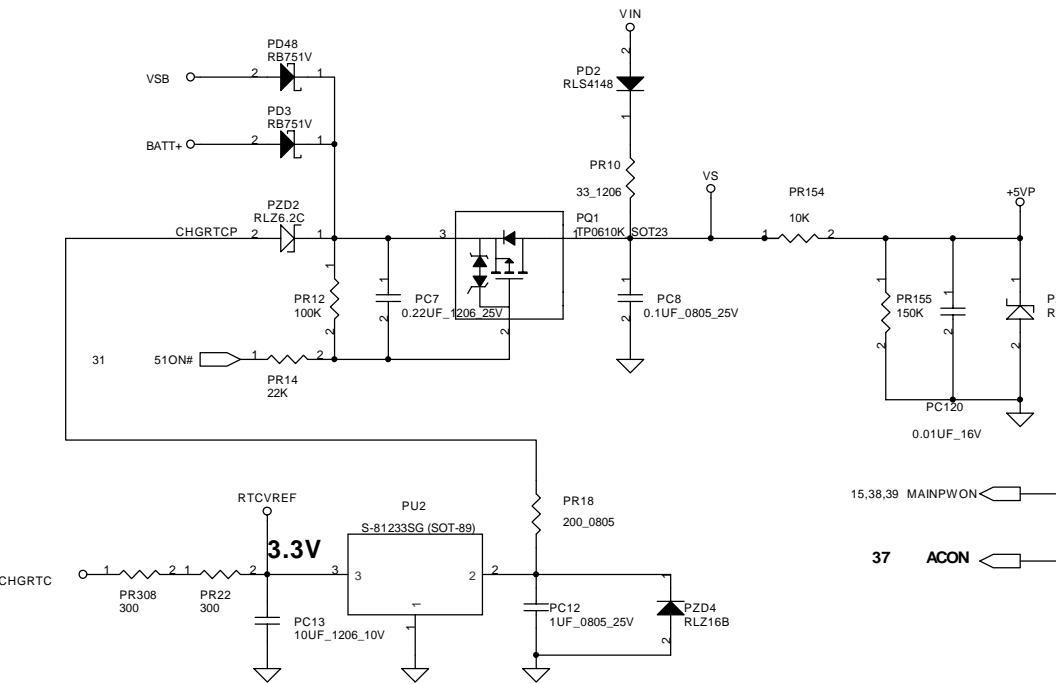
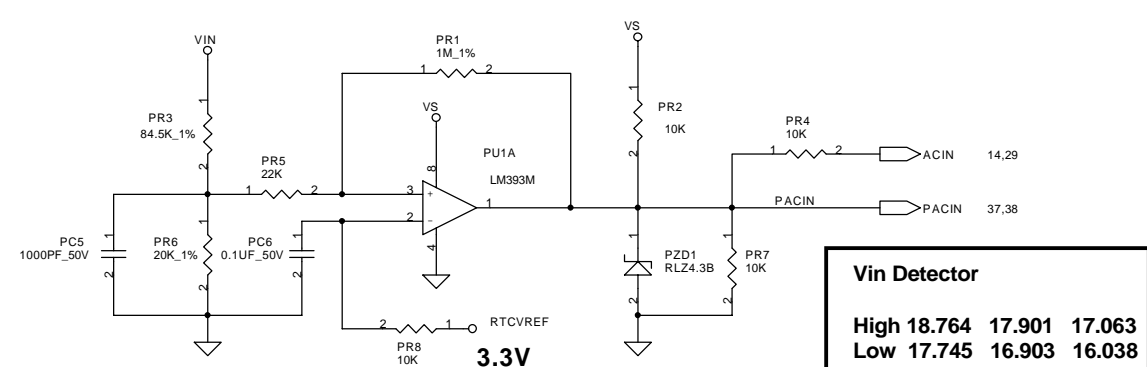
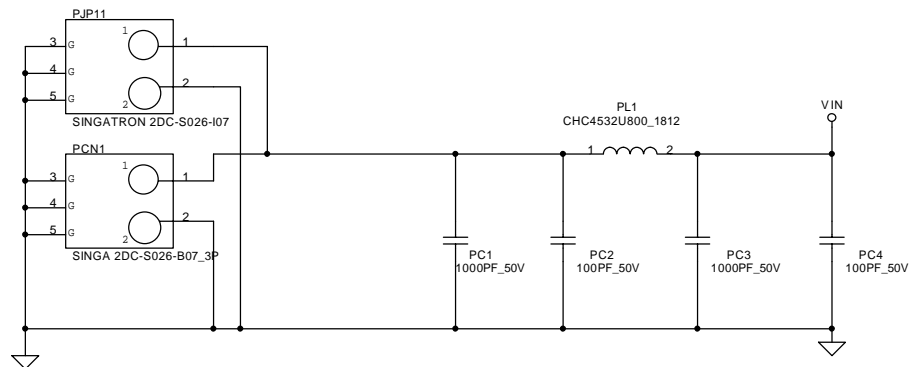
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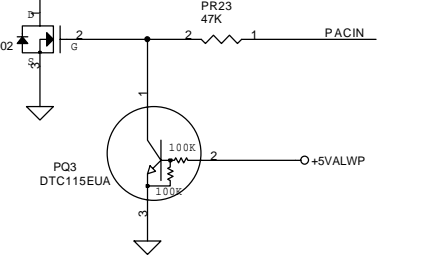
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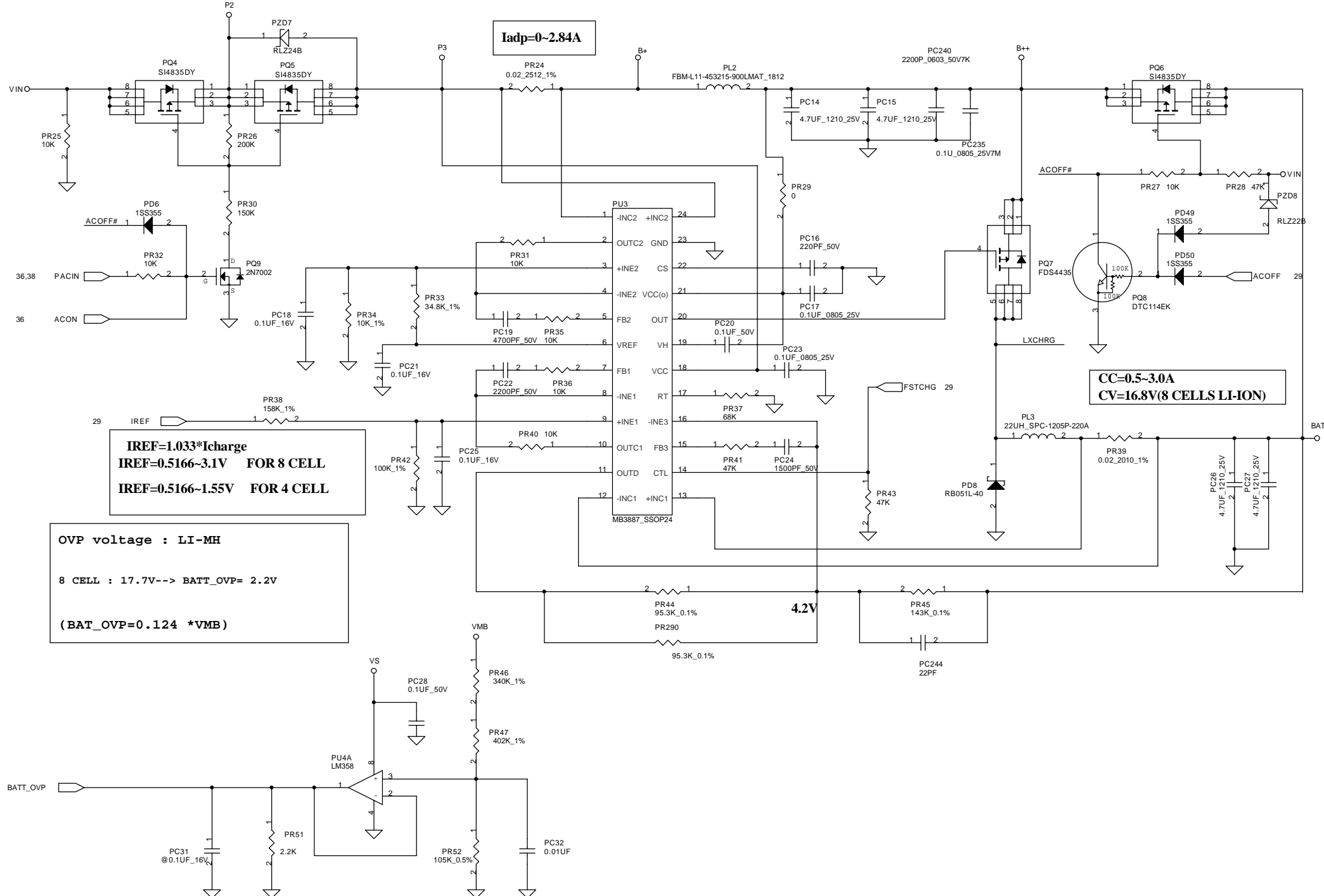


<b>Precharge detector</b>		
<b>AC ADAPTOR</b>		
16.69	16.05	15.42
15.6	15.02	14.35

<b>Precharge detector</b>		
<b>AC ADAPTOR</b>		
6.33	6.12	5.92
5.227	5.09	4.85



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**Iadp=0-2.84A**

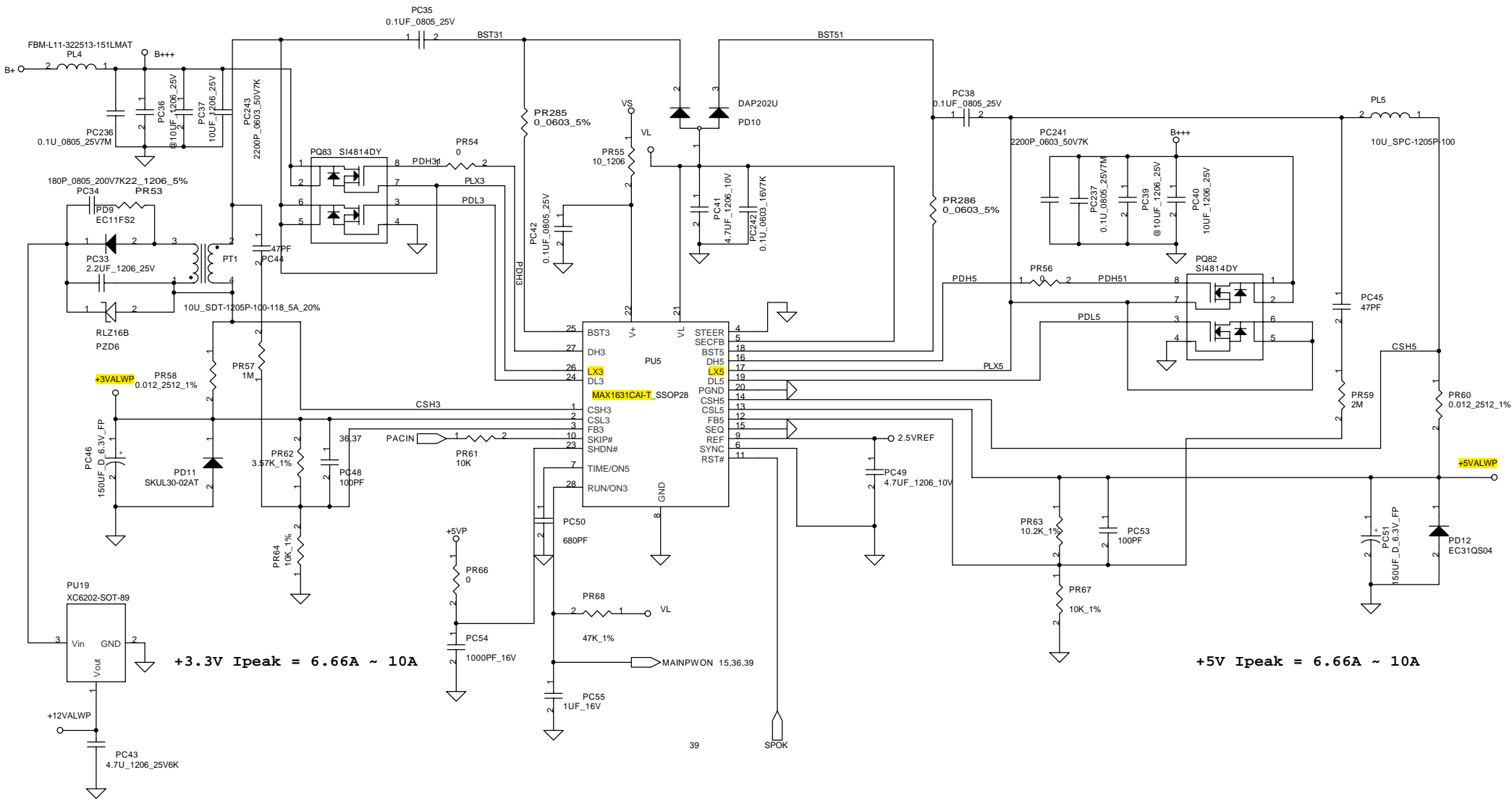
**CC=0.5-3.0A  
CV=16.8V(8 CELLS LI-ION)**

**IREF=1.033\*Icharge  
IREF=0.5166-3.1V FOR 8 CELL  
IREF=0.5166-1.55V FOR 4 CELL**

**OVP voltage : LI-MH**  
**8 CELL : 17.7V--> BATT\_OVP= 2.2V**  
**(BAT\_OVP=0.124 \*VMB)**

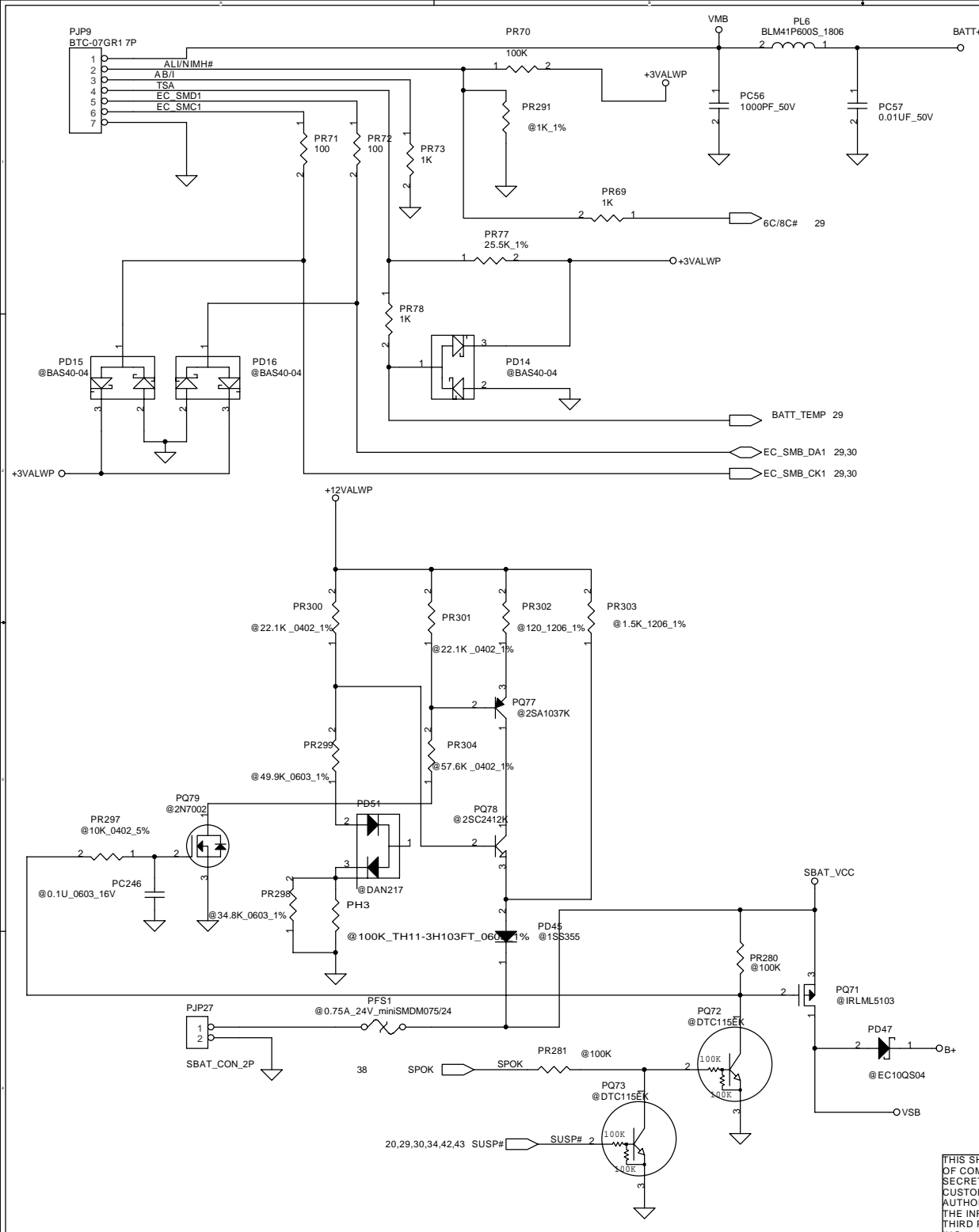
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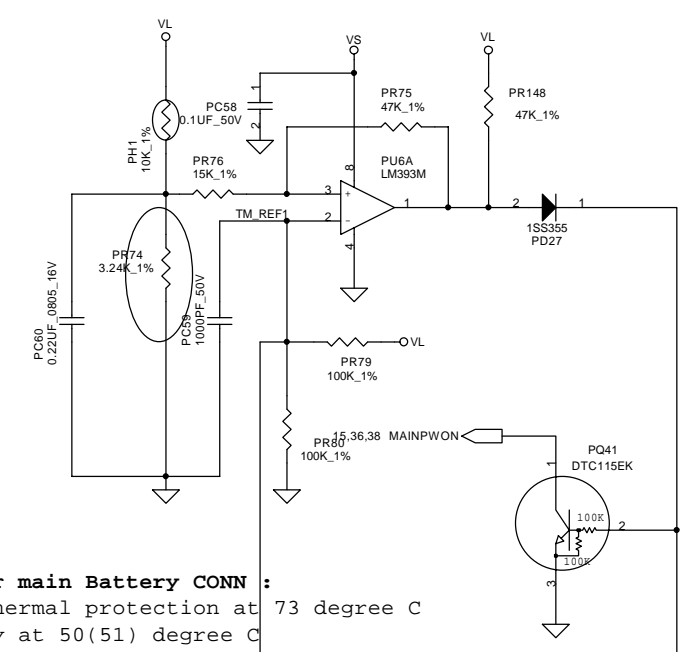


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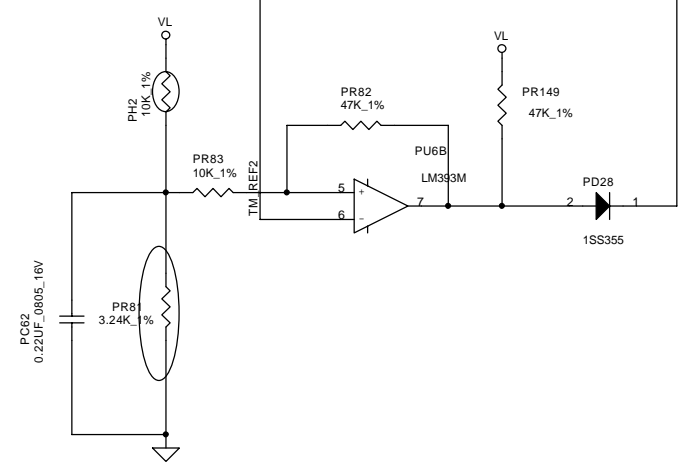
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PH1 under CPU bottom side :  
 CPU thermal protection at 82 degree C  
 Recovery at 48 degree C



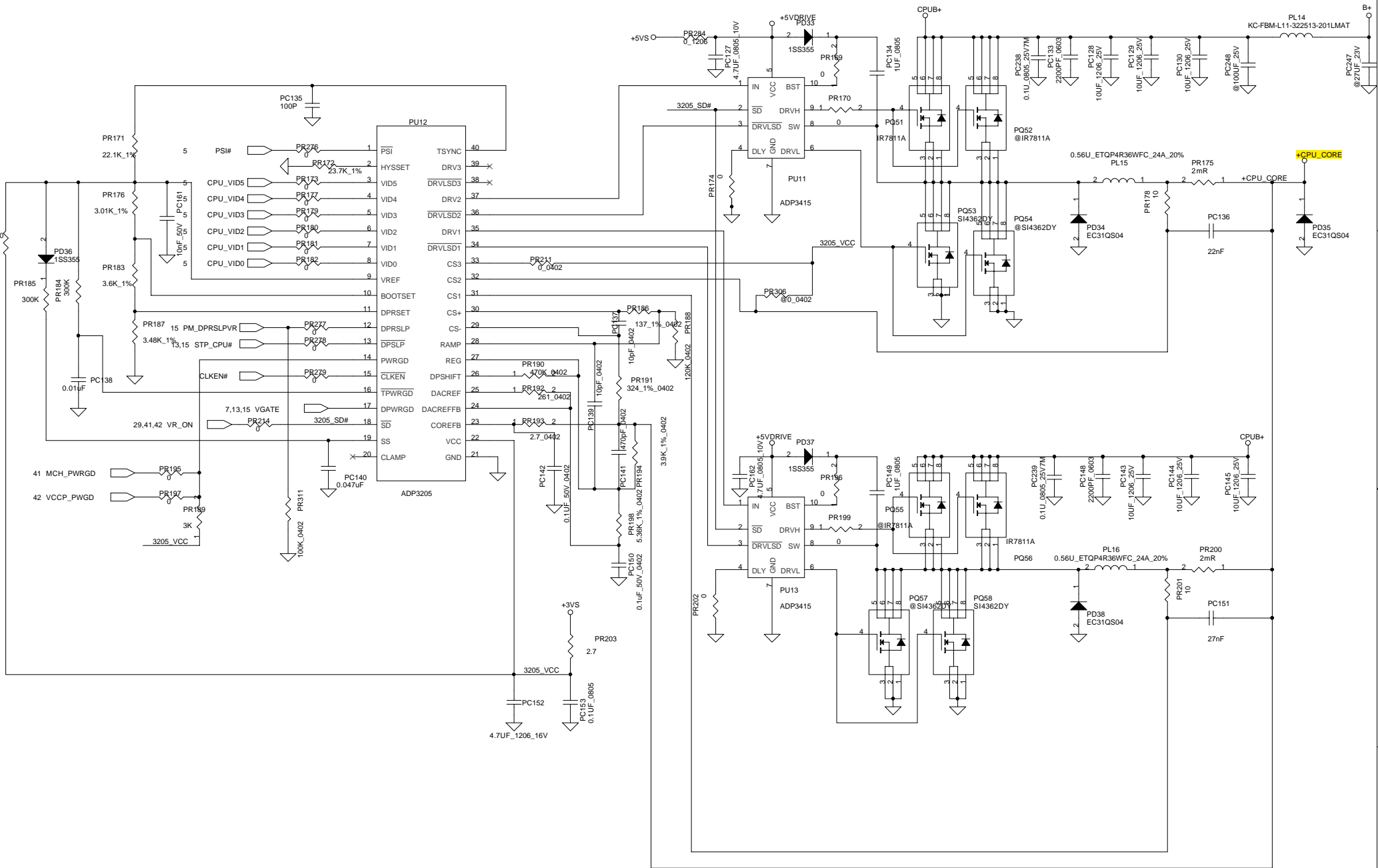
PH2 near main Battery CONN :  
 BAT. thermal protection at 73 degree C  
 Recovery at 50(51) degree C



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# CPU-CORE

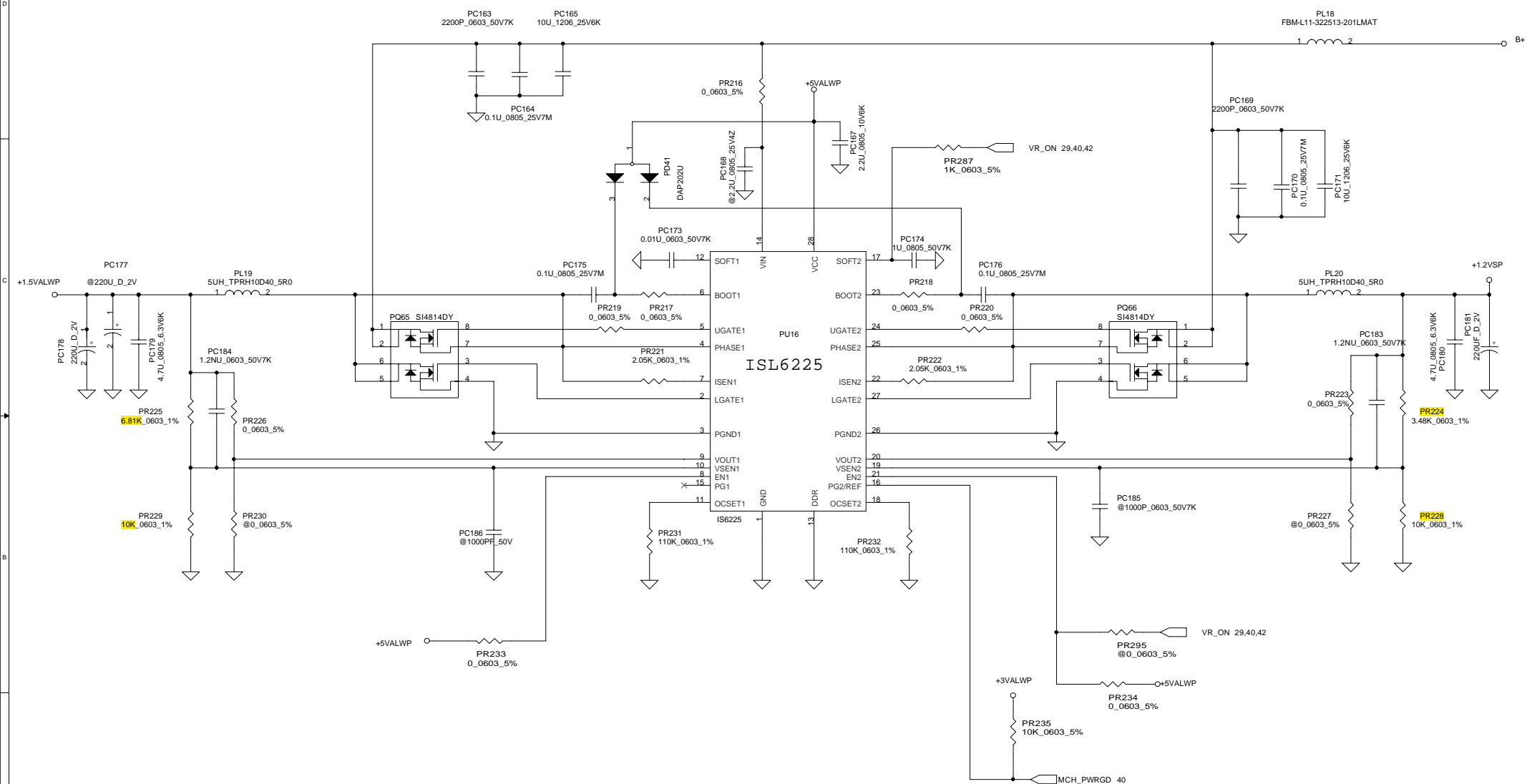


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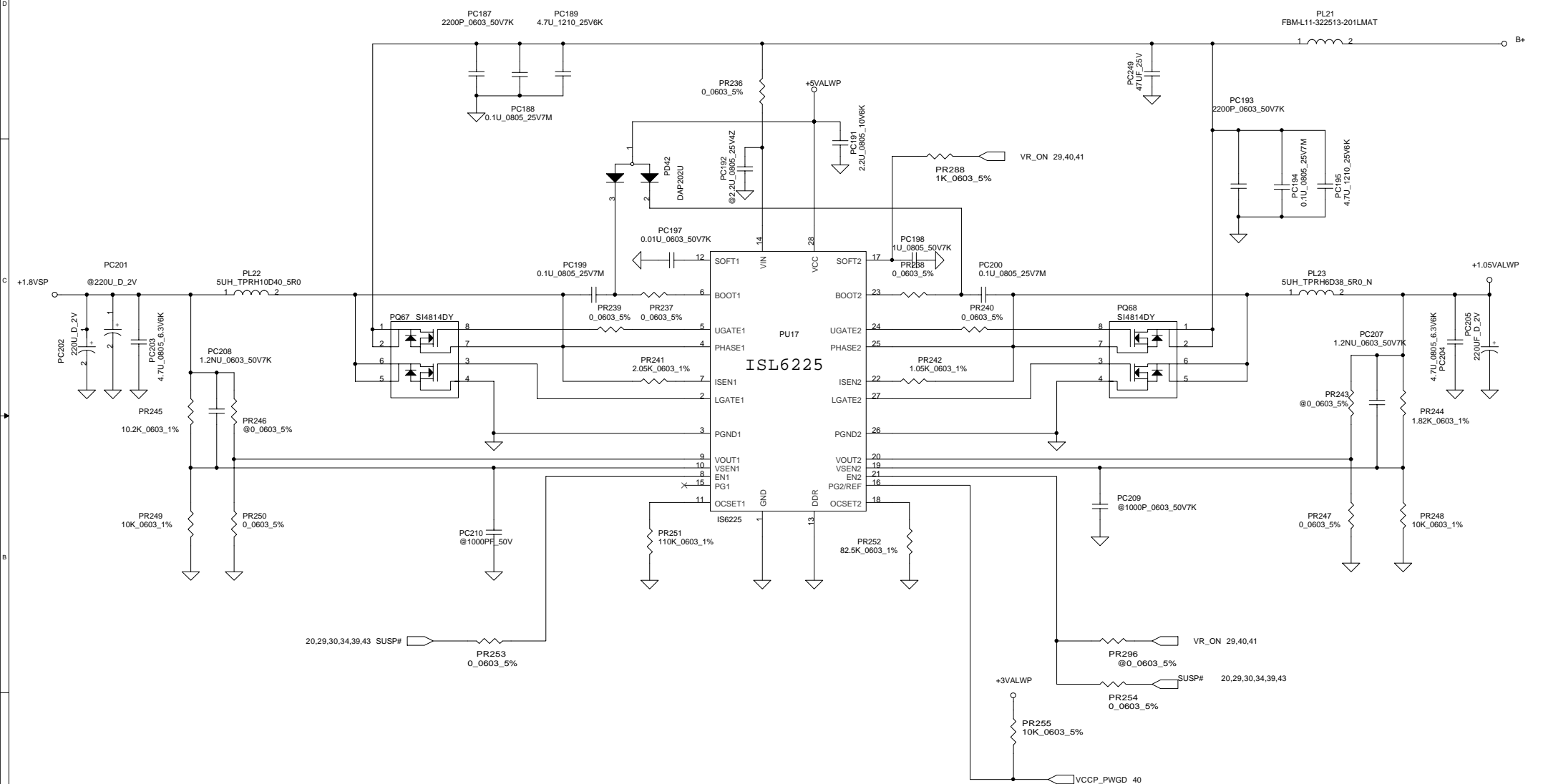
+1.5VALWPV/+1.2VSP



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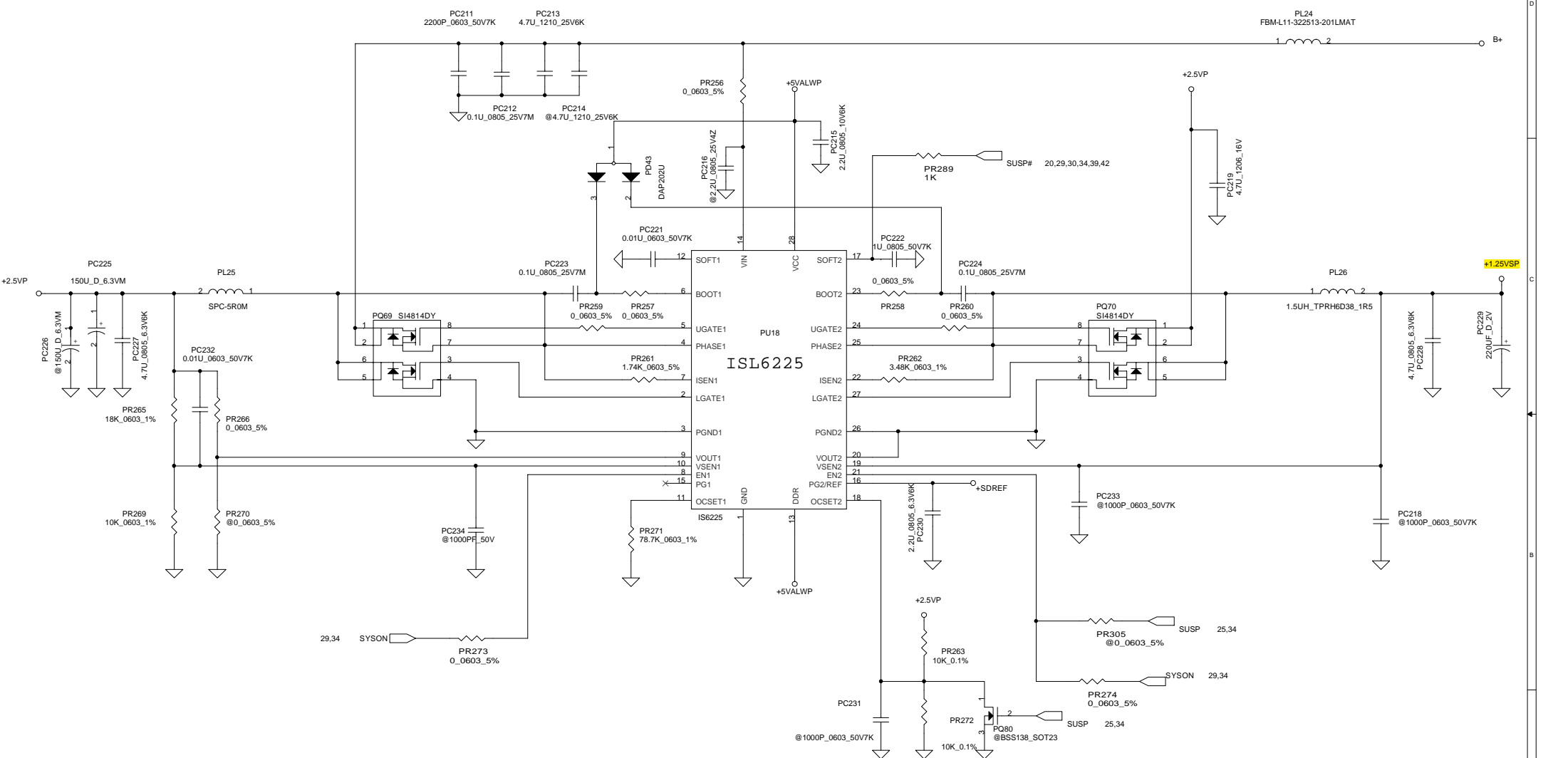
+1.8VALWP/+1.05VALWP



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+2.5VP/+1.25VSP



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1.	+5VMOD leaked when AC-IN	Change EXTIDEPWR# to +5VALW	0.2	P17	Delete EXTIDEPWR# Add +5VALW to R126		DVT
2.	For ESD	For ESD	0.2	P28	Add D26, D27 on TP_DATA, TP_CLK		DVT
3.	For EMI	For EMI	0.2	P31	Add C574 on FAN1_TACH		DVT
4.	Reserve For ENE KB3910	Reserve For ENE KB3910	0.2	P29	Add R441, R442, R443, R444, R445		DVT
5.	Reserve For CB1410 Rev.B0	Reserve For CB1410 Rev.B0	0.2	P20,21	Add C575, C576, R447, R448, R449		DVT
6.	Reserve FAN Control Circuit	Reserve FAN Control Circuit	0.2	P31	Add U44, R450, R451, R452, R453, C577		DVT
7.	Bluetooth LED	Add Bluetooth LED	0.3	P31	Add Q50, R454		PVT
8.	Change LED Wire Connector	Change LED Wire Connector	0.3	P26	Change JP24 Connector Type		PVT
9.	Reserve SCROLL LED Circuit	Add LED Control Circuit	0.3	P26	Add Q51, Q52, R455, R456		PVT
10.	For ESD	For ESD	0.3	P33	Add D28, D29, D30, D31 close to Speaker Connector		PVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		delete 6 cell charger voltage		37	1.delete PQ75,PQ74,PR294,PC245		DVT
2		Adjust charger charge voltage:		37	1. change PU3 from MB3878 to MB3887, PR38 from 118K to 174k,PR33 from 26.1k to 34k, PR44 from 120k_1% to 9.3k_0.1%,PR45 from 243k_1% to 143k_1%, PR290 from 243k_1% to 143k_0.1%		
3		modify 1.5UH CHOKE footprint to be the same as all vender		42	Change PL26 fom old version:1.5UH TPRH6D38 to new version 1.5UH_TPRH6D38-N.		DVT
4		add pull low resistor PR311 to ground for hardware		39	add PR311		DVT
5		for cpu core current balance		40	change pc151 from 22n to 27n		PVT
6		for vender require , new DC JACKbe crease		36	increase PJP11		
7		for 1.2vs soft start rise time		41,42,43	change pc174,pc198,pc222, from 4.7u to 1u		
8		cost down		38,39,40,41	delete PC36,PC39,PC247,PC249 CHANGE PC195,PC189 FROM 10U 1206 TO 4.7U 1210		
9		TP0610C will be phase out		36	change TP0610C to TP0610K		

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