Text Stamp

R12 INTEL UMA/DISCRETE SYSTEM DIAGRAM

+3V/+5V PG.31

+1.05VTT/+1.8V PG.32

CPU Core PG.33

VGACore/+1.1V PG.34

+1.5VSUS PG.35

Charger PG.36

Discharger PG.37

UMA VGACORE PG.38

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A

SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL Arrandale
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.3~6

PCI-E x8

AMD Seymour-XT
23mm X 23mm
TDP 15W
PG.14~18

DDR3 900MHz

VRAM 64Mx16x4,64bit PG.19

14.318MHz

CLOCK GEN PG.2

FDI — DMI

HDD PG.23 — SATA0

ODD PG.23 — SATA1

INTEL PCH
Ibex Peak-m
27mm X 25mm
1071pin FCBGA
TDP 5W
PG.7~11

HDMI Level Shifter PG.21

DP Port B — HDMI PG.21

CRT — CRT PG.22

LVDS — LVDS PG.20

PCI-E x 1

LAN3 — Card reader RTS5219-GR 10/100 PG.24

LAN2 — LAN RTS8165EH 10/100 PG.27

LAN1 — WLAN BT COMBO PG.30

USB 2.0 PORT10

USB2.0 Ports X2 PG.26 — PORT0,1

Webcam PG.20 — PORT4

BT Softbreeze PG.26 — PORT13

USB 2.0

KBC EnE KB3930QF D2 PG.29 — LPC

KB | TP | ROM | FAN

Azalia

AUDIO CODEC IDT92HD80B1 PG.25

Speaker PG.25

HP/MIC PG.26

Analog MIC PG.25

Stackup

TOP
GND
IN1
IN2
VCC
BOT

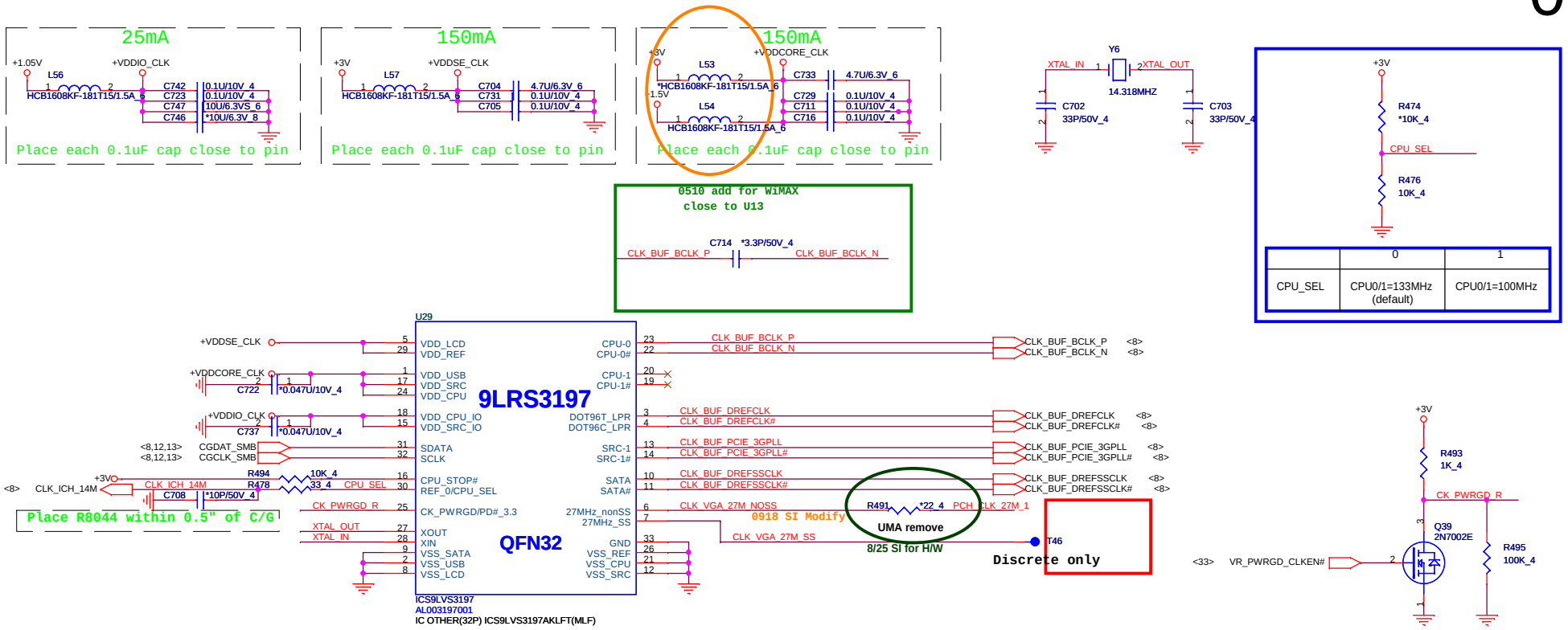
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Tuesday, September 14, 2010 | Sheet 1 of 39

Text Stamp

02



Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197000	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)

+1.05V <7,8,9,11,39>
+1.5V <5,30>
+3V <3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)	1A

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Text Stamp

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

03

U15A

DMI

DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 → DMI_RX#[0] DMI_RX#[1] DMI_RX#[2] DMI_RX#[3]

DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3 → DMI_RX[0] DMI_RX[1] DMI_RX[2] DMI_RX[3]

DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 → DMI_TX#[0] DMI_TX#[1] DMI_TX#[2] DMI_TX#[3]

DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3 → DMI_TX[0] DMI_TX[1] DMI_TX[2] DMI_TX[3]

2.7GT/s data rate

FDI_TXN[7:0] → FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_TXP[7:0] → FDI_TX[0] FDI_TX[1] FDI_TX[2] FDI_TX[3] FDI_TX[4] FDI_TX[5] FDI_TX[6] FDI_TX[7]

FDI_FSYNC0 FDI_FSYNC1 → FDI_FSYNC[0] FDI_FSYNC[1]

FDI_INT → FDI_INT

FDI_LSYNC0 FDI_LSYNC1 → FDI_LSYNC[0] FDI_LSYNC[1]

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI PEG_ICOMPO PEG_RCOMPO PEG_RBIAS

B26 PEG_COMP R288 49.9/F_4

B27

A25 PEG_RBIAS R289 750/F_4

PEG_RX#[0..7] <14>

PEG_RX#[0] … PEG_RX#[15] ← K35 J34 J33 G35 G32 E34 F31 D35 E33 C33 D32 B32 C31 B28 B30 A31

PEG_RX[0..7] <14>

PEG_RX[0] … PEG_RX[15] ← J35 H34 H33 F35 G33 E34 E32 D34 F33 B33 D31 A32 C30 A28 B29 A30

PEG_TX#[0..7] <14>

PEG_TX#[0] … PEG_TX#[15] → L33 M35 M33 M30 L31 K32 M29 J31 K29 H30 H29 F29 E28 D29 D27 C26

C_PEG_TX#0 C543 … C_PEG_TX#7 C582 — 0.1U/10V_4 — PEG_TX#0 … PEG_TX#7

UMA remove

PEG_TX[0..7] <14>

PEG_TX[0] … PEG_TX[15] → L34 M34 M32 L30 M31 K31 M28 H31 K28 G30 G29 F28 E27 D28 C27 C25

C_PEG_TX0 C537 … C_PEG_TX7 C578 — 0.1U/10V_4 — PEG_TX0 … PEG_TX7

IC,AUB_CFD_rPGA,R1P0

U15B

MISC

COMP3 COMP2 COMP1 COMP0 SKTOCC#

R139 20/F_4 H_COMP3 AT23
R142 20/F_4 H_COMP2 AT24
R81 49.9/F_4 H_COMP1 G16
R143 49.9/F_4 H_COMP0 AT26
AH24

THERMAL

H_CATERR# AK14
CATERR# AT15
PECI AN26
PROCHOT# AK15
THERMTRIP#

<10> H_PECI
<29,33> H_PROCHOT#
<10,29> PM_THRMTRIP#

RESET_OBS# AP26
PM_SYNC AL15
VCCPWRGOOD_1 AN14
VCCPWRGOOD_0 AK13
SM_DRAMPWROK
TAPPWRGOOD AM26
VTTPWRGOOD AM15
RSTIN# AL14

T31 H_CPURST#
<9> PM_SYNC
<10> H_PWRGOOD
<9> PM_DRAM_PWRGD
T45 H_PWRGD_XDP
H_VTTPWRGD
CPU_PLTRST#
<8,14,24,27,29,30> PLTRST#
R124 1.5K/F_4
R126 750/F_4

PWR MANAGEMENT

CLOCKS

BCLK BCLK# A16 B16 → CLK_CPU_BCLK <10> CLK_CPU_BCLK# <10>

BCLK_ITP BCLK_ITP# AR30 AT30 → CLK_PCIE_3GPLL <8> CLK_PCIE_3GPLL# <8>

For ITP Clk

PEG_CLK PEG_CLK# E16 D16

Rc

DPLL_REF_SSCLK A18 DREFSSCLK_R → DREFSSCLK <8>
DPLL_REF_SSCLK# A17 DREFSSCLK#_R → DREFSSCLK# <8>

Ra

Rb

DDR3 MISC

SM_DRAMRST# F6 DDR3_DRAMRST#_C

SM_RCOMP[0] AL1 R363 100/F_4
SM_RCOMP[1] AM1 R364 24.9/F_4
SM_RCOMP[2] AN1 R365 130/F_4
R176 10K_4

PM_EXT_TS#[0] AN15 PM_EXT_TS#0 R177 *0_4/S → +1.05V_VTT PM_EXTTS#0 <12,13>
PM_EXT_TS#[1] AP15 PM_EXT_TS#1 R166 *0_4/S → +1.05V_VTT PM_EXTTS#1 <13>
R168 10K_4

JTAG & BPM

PRDY# AT28 XDP_PRDY# → T44
PREQ# AP27 XDP_PREQ# → T28
TCK AN28 XDP_TCLK → T25
TMS AP28 XDP_TMS → T27
TRST# AT27 XDP_TRST# → T32
TDI AT29 XDP_TDI_R → T33
TDO AR27 XDP_TDO_R → T30
TDI_M AR29 XDP_TDI_M → T29
TDO_M AP29 XDP_TDO_M → T26

BPM#[0] AJ22
BPM#[1] AK22
BPM#[2] AK24
BPM#[3] AJ24
BPM#[4] AJ25
BPM#[5] AH22
BPM#[6] AK23
BPM#[7] AH23

DBR# AN25 → XDP_DBRESET# <9>

IC,AUB_CFD_rPGA,R1P0

<14>

+1.05V_VTT

XDP_TDO_R R144 51_4
H_CATERR# R119 49.9/F_4
H_PROCHOT# R130 56.2/F_4
CPU_PLTRST# R123 *68_4
XDP_TMS R138 *51_4
XDP_TDI_R R145 *51_4
XDP_PREQ# R141 *51_4
XDP_TCLK R137 *51_4

U10
MC74VHC1G08DFT2G
+3V
<29,31,32,35,38,39> HWPG
HWPG_1 R170 2K/F_4 H_VTTPWRGD
R164 1K/F_4

JTAG MAPPING

XDP_TDI_R Ra
XDP_TDO_M Rb
Rc R140 0_4
XDP_TDI_M Rd
XDP_TDO_R Re

XDP_TRST# R147 51_4

for S3 power reduction

R62 *0_4
Q6 BSS138_NL
DDR3_DRAMRST#_C
DDR3_DRAMRST# <12,13>
SI modify
R66 100K_4
PCIE_CLK_REQ7# <10>
C98 0.047U/10V_4
R58 10K_4
+3VS5

SI modify

+3VS5 +1.5VSUS
R187 *10K_4
R186 *8.2K_4
R184 *0_4
R178 *0_4
R172 *0_4/S HWPG_1
R179 1.5K/F_4
<32> STAT_1.1
U9
*MC74VHC1G08DFT2G
PM_DRAM_PWRGD
R163 750/F_4

Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/750±1% (to GND) to convert to processor VTT level.

<5,10,11,29,32,33,38> +1.05V_VTT
<5,12,13,34,35,36> +1.5VSUS
<2,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V

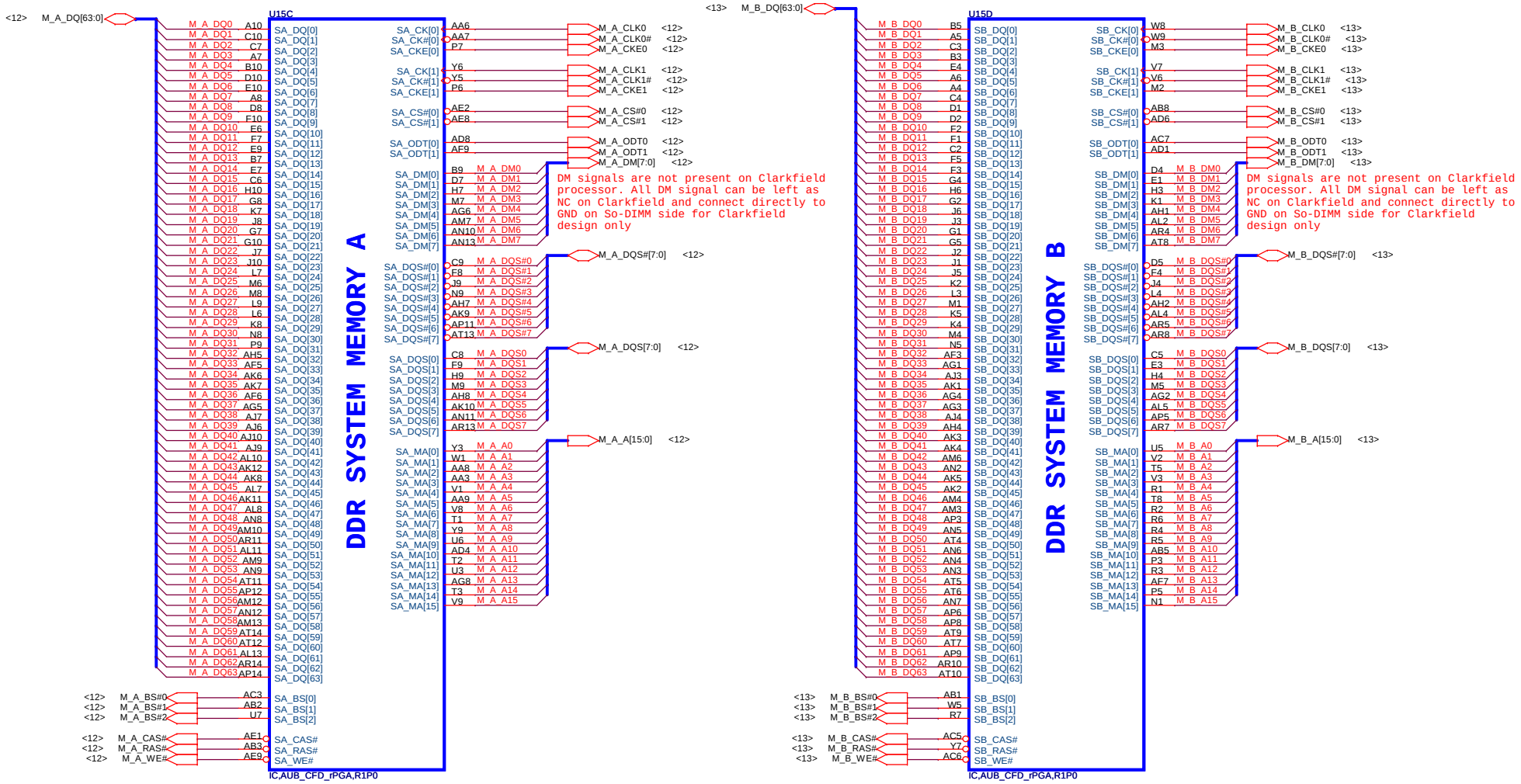
Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	1A
Date: Sunday, September 19, 2010	Sheet 3 of 39	

Text Stamp

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	1A

Date: Tuesday, September 14, 2010 | Sheet 4 of 39

Text Stamp

05

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

	DIS	UMA
Ra	0 ohm	NA

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

UMA only

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

8/25 SI for H/W.

0510 add for WiMAX

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

for S3 power reduction

SI modify

40mile routing

PROJECT : R12
Quanta Computer Inc.

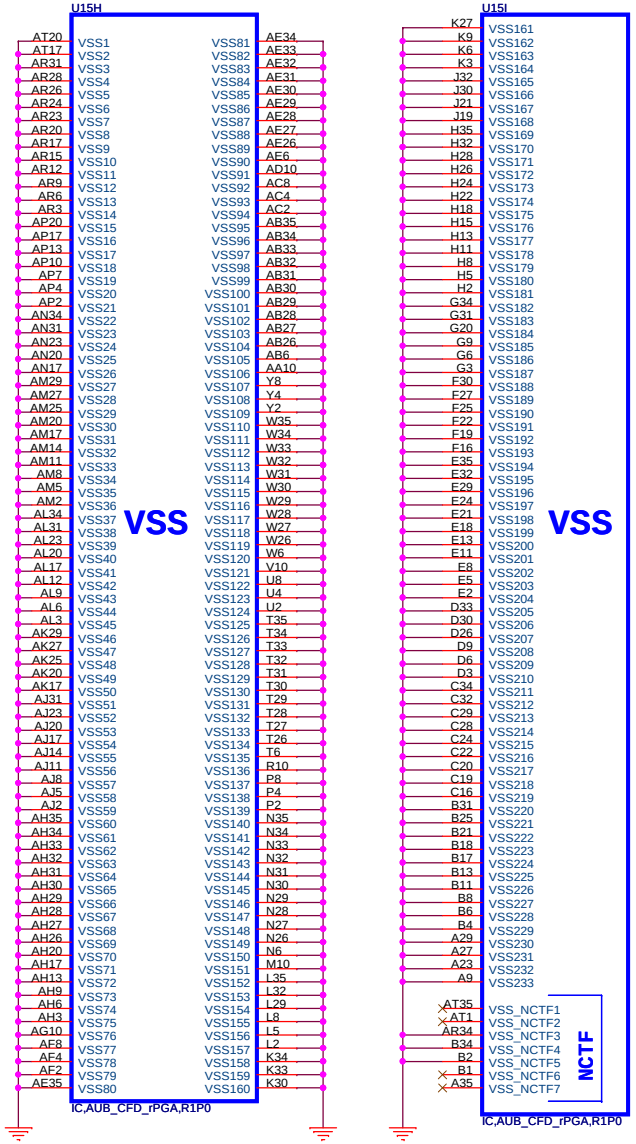
PROCESSER 3/4(POWER)

Size: Custom | Rev: 1A | Date: Sunday, September 19, 2010 | Sheet 5 of 39

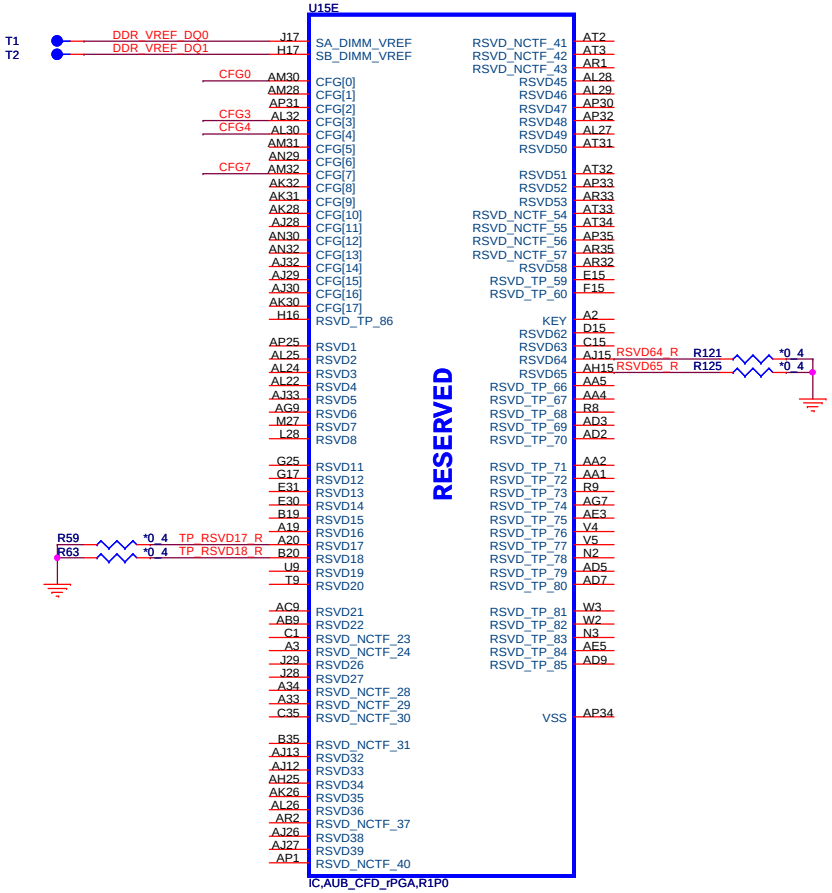
Text Stamp

06

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4 (GND)	1A

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Text Stamp

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U24A

Ibex-M 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN

LPC: FWH0 / LAD0, FWH1 / LAD1, FWH2 / LAD2, FWH3 / LAD3, FWH4 / LFRAME#, LDRQ0#, (+3V) LDRQ1# / GPIO23, SERIRQ

IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN# / GPIO33, HDA_DOCK_RST# / GPIO13

SATA: SATA0RXN/P, SATA0TXN/P, SATA1RXN/P, SATA1TXN/P, SATA2RXN/P, SATA2TXN/P, SATA3RXN/P, SATA3TXN/P, SATA4RXN/P, SATA4TXN/P, SATA5RXN/P, SATA5TXN/P, SATAICOMPO, SATAICOMPI, SATALED#, SATA0GP / GPIO21, SATA1GP / GPIO19

JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#

SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

IbexPeak-M_Rev1_0

C663 18P/50V_4, C665 18P/50V_4, Y4 32.768KHZ, R444 10M_4, RTC_X1, RTC_X2

RTC_RST#, SRTC_RST#, SM_INTRUDER#, +RTC_CELL, R445 330K_6, PCH_INVRMEN

ACZ_BCLK, ACZ_SYNC, ACZ_RST#, <10,25> ACZ_SPKR, <25> ACZ_SDIN0, ACZ_SDOUT

<10,29> GPIO33_E, R249 *0_4, PCH_GPIO33_R

must add test point.

TP12 PCH_JTAG_TCK, TP10 PCH_JTAG_TMS, TP9 PCH_JTAG_TDI, TP8 PCH_JTAG_TDO, TP1 PCH_JTAG_RST#

SPI_CLK_R, SPI_CS0#_R, TP13 SPI_CS1#, SPI_SI_R, SPI_SO

R230 10K_4 +3V SERIRQ <29>

HDD: SATA_RXN0 <23>, SATA_RXP0 <23>, SATA_TXN0 <23>, SATA_TXP0 <23>

ODD: SATA_RXN4 <23>, SATA_RXP4 <23>, SATA_TXN4 <23>, SATA_TXP4 <23>

SATA_COMP R237 37.4/F_4 +1.05V

SATA_LED# <28>

R409 *0_4 ODD_PRSNT# <23>

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

R411 10K_4 SATA_LED#
R223 10K_4 SATA_DET0#
R410 10K_4 SATA_DET1#
R251 *10K_4 GPIO33_E

R433 51_4 PCH_JTAG_TCK

UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)

U24D

Ibex-M 4 OF 10

LVDS--A: L_BKLTEN, L_VDD_EN, L_BKLTCTL, L_DDC_CLK, L_DDC_DATA, L_CTRL_CLK, L_CTRL_DATA, LVD_IBG, LVD_VBG, LVD_VREFH, LVD_VREFL, LVDSA_CLK#, LVDSA_CLK, LVDSA_DATA#0-3, LVDSA_DATA0-3

LVDS--B: LVDSB_CLK#, LVDSB_CLK, LVDSB_DATA#0-3, LVDSB_DATA0-3

CRT: CRT_BLUE, CRT_GREEN, CRT_RED, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC, DAC_IREF, CRT_IRTN

SDVO: SDVO_TVCLKINN/P, SDVO_STALLN/P, SDVO_INTN/P, SDVO_CTRLCLK, SDVO_CTRLDATA

Digital Display Interface

DISPLAY PORT B: DDPB_AUXN/P, DDPB_HPD, DDPB_0N/P, DDPB_1N/P, DDPB_2N/P, DDPB_3N/P

DISPLAY PORT C: DDPC_CTRLCLK, DDPC_CTRLDATA, DDPC_AUXN/P, DDPC_HPD, DDPC_0N/P, DDPC_1N/P, DDPC_2N/P, DDPC_3N/P

DISPLAY PORT D: DDPD_CTRLCLK, DDPD_CTRLDATA, DDPD_AUXN/P, DDPD_HPD, DDPD_0N/P, DDPD_1N/P, DDPD_2N/P, DDPD_3N/P

IbexPeak-M_Rev1_0

<20> LVDS_BLON, <20> DISP_ON, <20> DPST_PWM, <20> EDIDCLK, <20> EDIDDATA

R266 10K_4 L_CTRL_CLK, R269 10K_4 L_CTRL_DATA, +3V, R259 2.37K/F_4 LVDS_IBG, LVDS_VBG, TP7

HDD0 (SATA3 6.0Gb/s)

<20> TXLCLKOUT-/+, <20> TXLOUT0-/1-/2-, <20> TXLOUT0+/1+/2+

<20> TXUCLKOUT-/+, <20> TXUOUT0-/1-/2-/0+/1+/2+

<22> CRT_B, CRT_G, CRT_R, <22> DDCCLK, <22> DDCDATA, <22> HSYNC_COM, <22> VSYNC_COM

R455 150/F_4, R457 150/F_4, R456 150/F_4

R272 1K/F_4 DAC_IREF

TP16, TP15

For ES1 ONLY.NI for ES2.

R415 200_4, R413 200_4, R416 200_4, R192 20K/F_4

PCH_JTAG_RST#, PCH_JTAG_TDO, PCH_JTAG_TDI, PCH_JTAG_TMS

For ES1 ONLY.NI for ES2.

R414 100_4, R412 100_4, R436 100_4, R197 10K_4

UMA HDMI signals

DPB_CTRL_CLK R459 0_4, DPB_CTRL_DATA R458 0_4, DPB_LANE0_N C474 0.1U/10V_4, DPB_LANE0_P C478 0.1U/10V_4, DPB_LANE1_N C471 0.1U/10V_4, DPB_LANE1_P C472 0.1U/10V_4, DPB_LANE2_N C480 0.1U/10V_4, DPB_LANE2_P C482 0.1U/10V_4, DPB_LANE3_N C465 0.1U/10V_4, DPB_LANE3_P C467 0.1U/10V_4

SDVO_CLK <21>, SDVO_DATA <21>, IN_D2# <21>, IN_D2 <21>, IN_D1# <21>, IN_D1 <21>, IN_D0# <21>, IN_D0 <21>, IN_CLK# <21>, IN_CLK <21>

DPB_HPD_Q, Q18 *2N7002K, HDMI_HPD_CON <21>, R287 100K_4, R286 0_4

Part
Part Number
Part Description

For AUDIO

<25> ACZ_RST#_AUDIO, <25> ACZ_SDOUT_AUDIO, <25> ACZ_SYNC_AUDIO, <25> BIT_CLK_AUDIO

R452 33_4 ACZ_RST#, R450 33_4 ACZ_SDOUT, C666 *10P/50V_4
R451 33_4 ACZ_SYNC, C667 *10P/50V_4
R453 33_4 ACZ_BCLK, C464 *10P/50V_4

For MDC

RTC 1mA

+RTC_CELL, +3VPCU, RB500V-40 CR1, +3VRTC_2, RB500V-40 CR2

C438 1U/6.3V_4, R242 20K/F_4 RTC_RST#, C428 1U/6.3V_4

R241 20K/F_4 SRTC_RST#, C429 1U/6.3V_4

R243 1M_4 SM_INTRUDER#

CN24, R254 1K_4 +3VRTC_1, BAT_CONN

8/25 SI for M/E.

DFWF02MS032
50273-0027N-001-2P-L

4M byte SPI ROM

U22

+3V, R422 10K_4, C659 0.1U/10V_4, SPI_HOLD#, SPI_CS0#_R, SPI_CLK_R, SPI_SI_R, SPI_SO, SPI_WP#, R440 10K_4

W25Q32BVSSIG
AKE391P0N00
IC FLASH(8P) W25Q32BVSSIG(SOIC)

<2,8,9,11,39> +1.05V
<2,3,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<20,28,29,31,37> +3VPCU

Vender

Socket DG008000031
EON - EN25F32-100HIP
AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)
WINBOND - W25Q32BVSSIG
AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A

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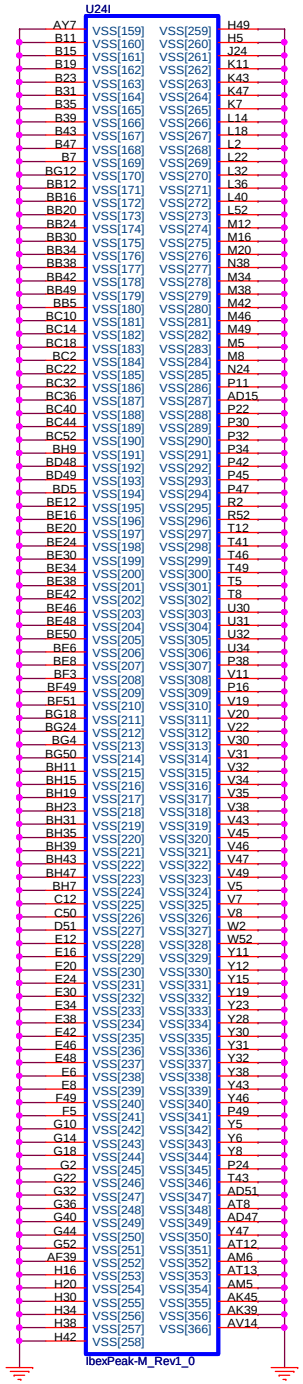
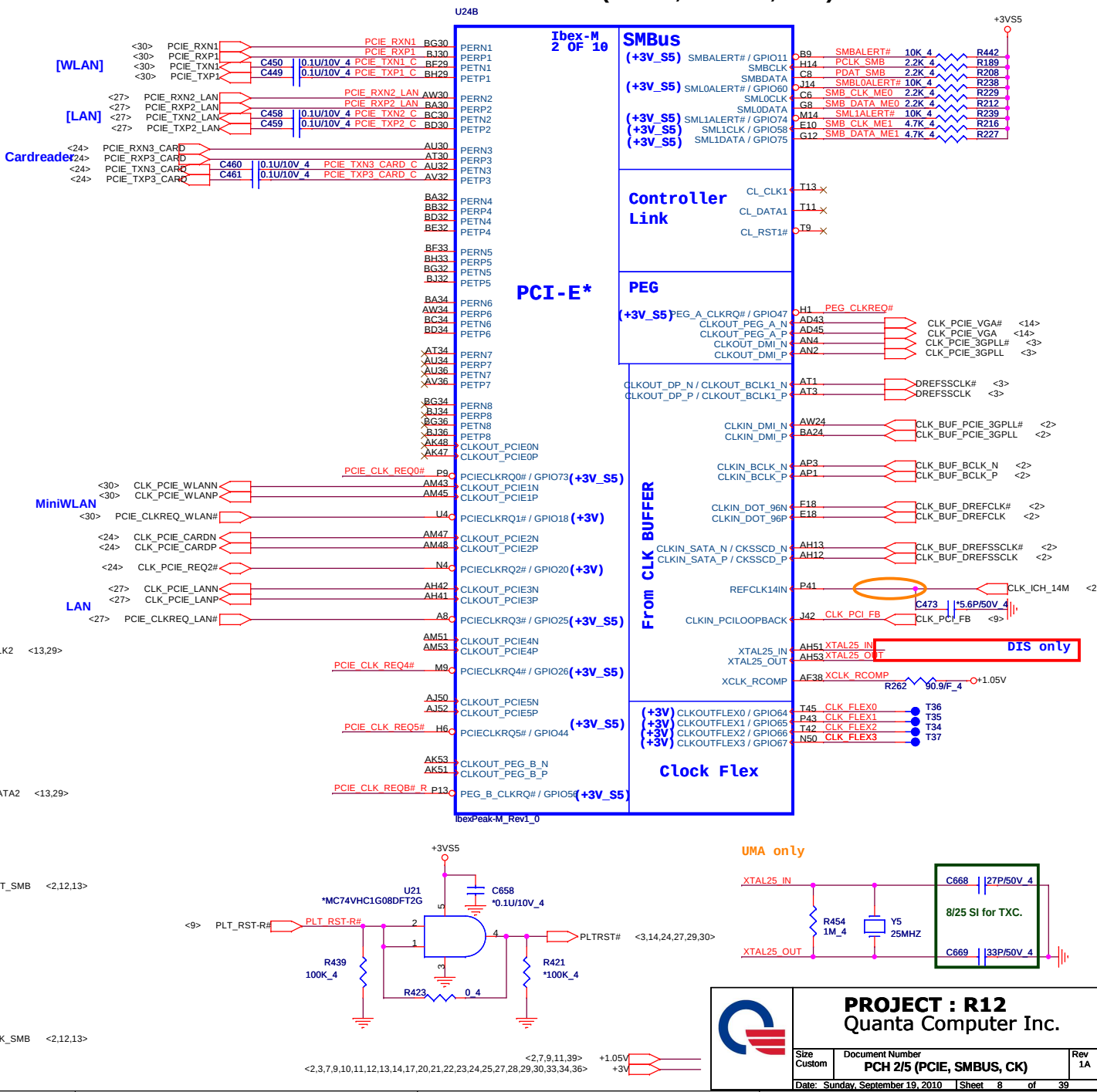
Text Stamp

IBEX PEAK-M (GND)

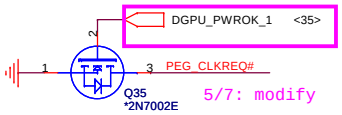


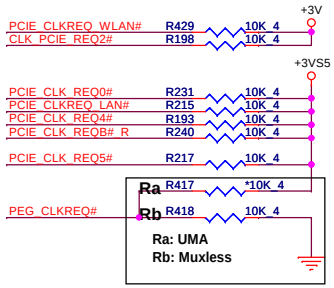
08

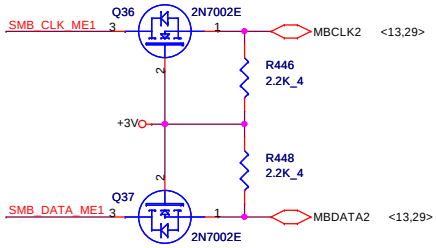
IBEX PEAK-M (PCI-E,SMBUS,CLK)

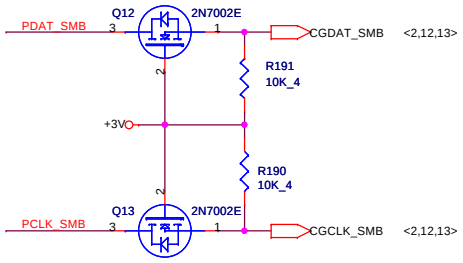


PEG Clock detect (SG only)





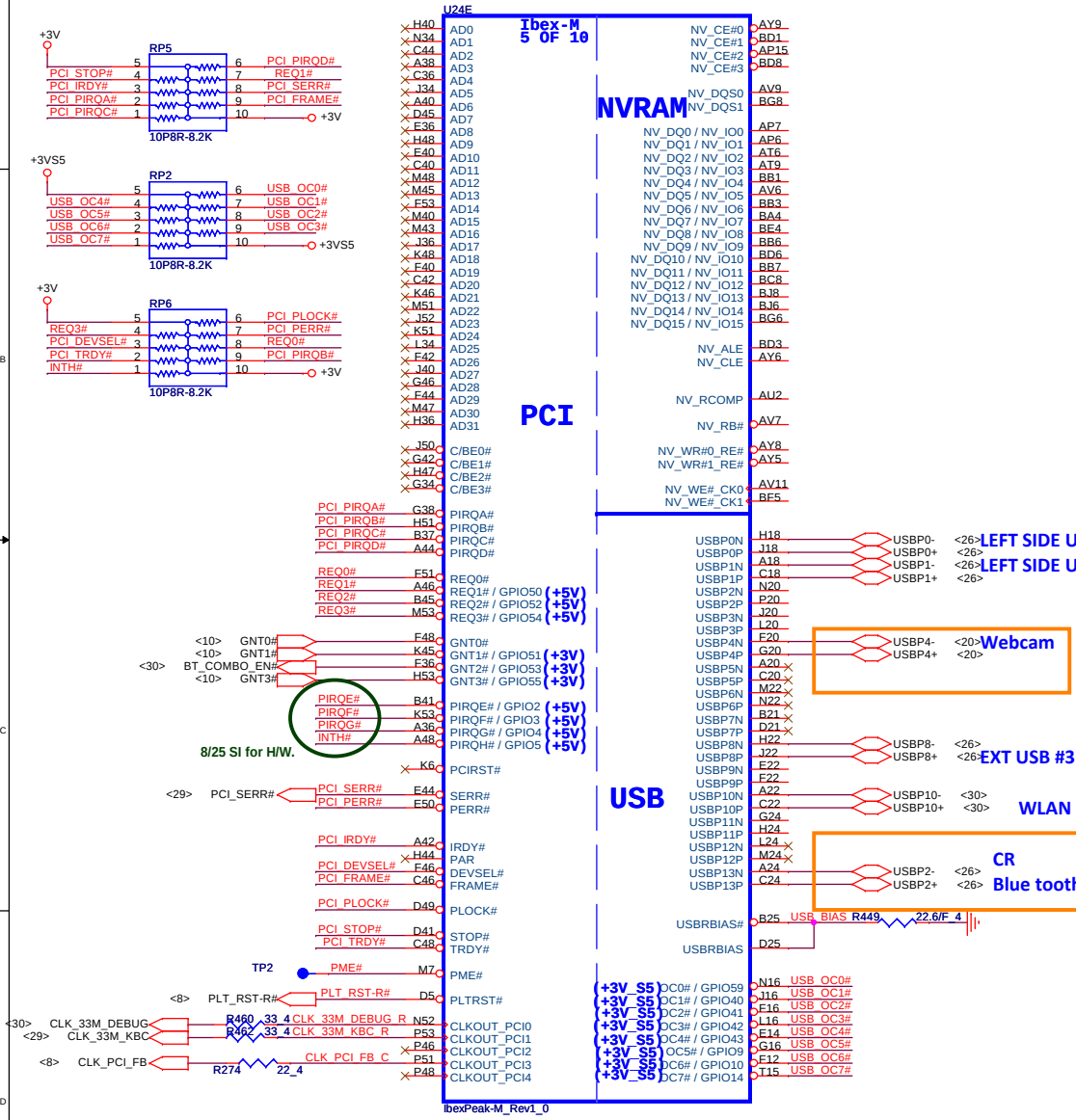




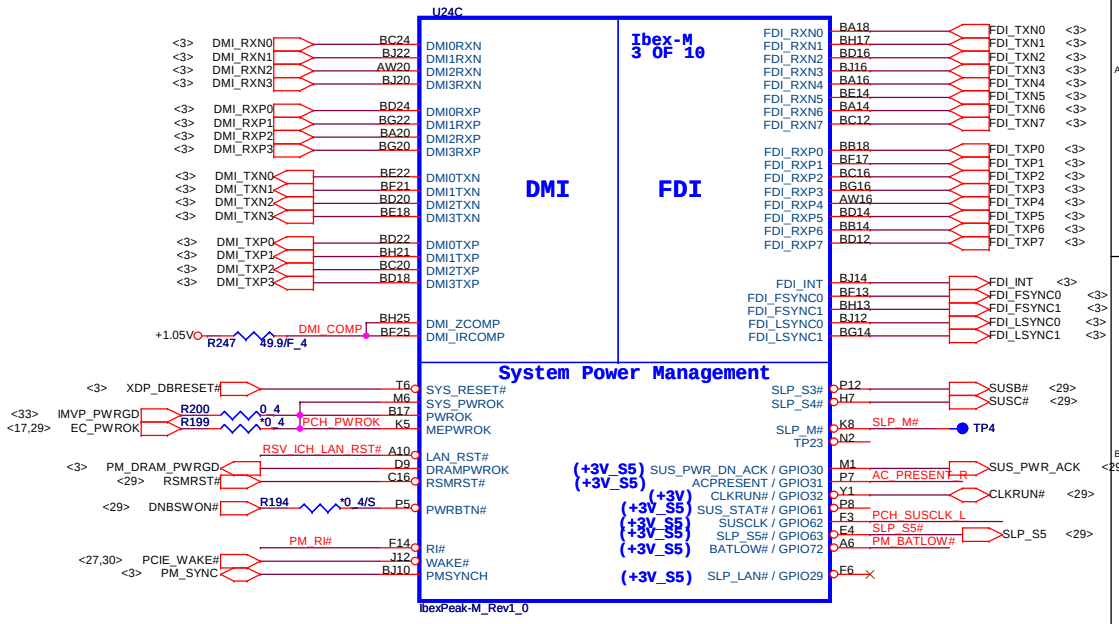
Text Stamp

09

IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)



LEFT SIDE USB #0

LEFT SIDE USB #1

Webcam

EXT USB #3

WLAN

CR

Blue tooth

SI Modify

Change Port2 to Port4

Change Port4 to Port12

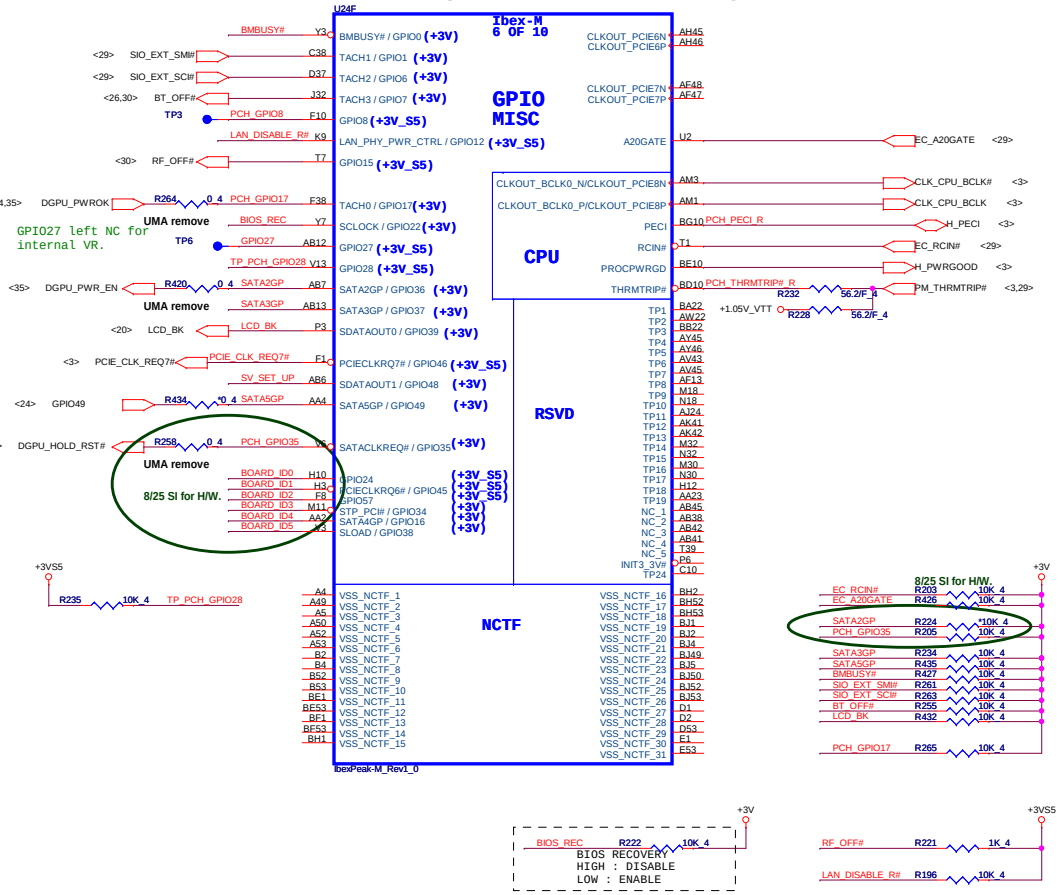
change Port5 to Port13

C673 *5.6P/50V_4

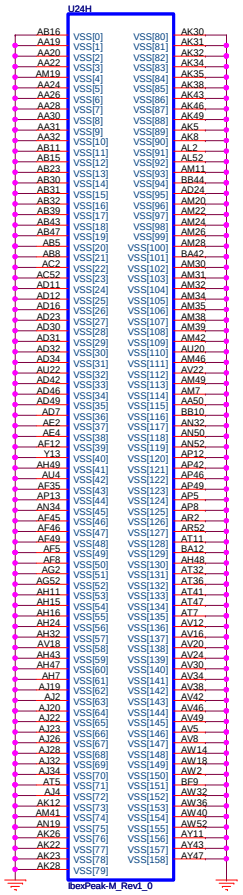
PROJECT : R12 Quanta Computer Inc.		
Size: Custom	Document Number: PCH 3/5 (PCI,ONFI,USB,DMI)	Rev: 1A
Date: Sunday, September 19, 2010	Sheet 9 of 39	

Text Stamp

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



10

<9> GNT3# R464 *10K_4

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R219 10K_4 +3V

SV_SET_UP	1-X High = Strong (Default)

<9> GNT0#
<9> GNT1#
GNT0# R271 *1K_4
GNT1# R463 *1K_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

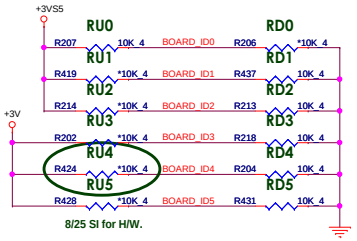
No Reboot Strap

<7,25> ACZ_SPKR *1K_4 R430 +3V
<7,29> GPIO33_E R253 *100K_4

<3,5,11,29,32,33,38> +1.05V_VTT
<5,11,32> +1.8V
<2,3,7,8,9,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<3,7,8,9,11,26,31,32,34,35,36,38> +3VS5

R12 MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
31R12MB0000 (PIM) 31R12MB0010 (PDT)	0 0	0 0	0 0	0 0	0 0	0 0
Seymour XT Hynix 512						
31R12MB0020 (PIM) 31R12MB0030 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Samsung 512						
31R12MB0040 (PIM) 31R12MB0050 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Hynix 1G						
31R12MB0060 (PIM) 31R12MB0070 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Samsung 1G						
31R12MB0080 (PIM) 31R12MB0090 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0

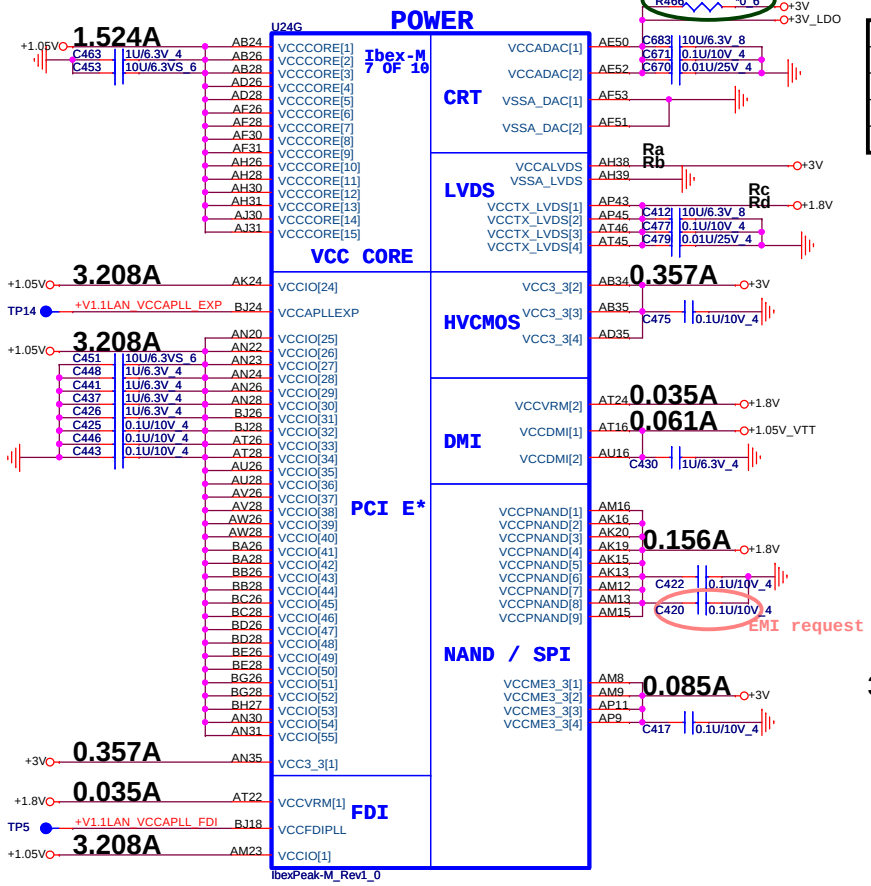
Board ID	ID0 GPIO24	ID1 GPIO45	ID2 GPIO57	ID3 GPIO34	ID4 GPIO35	ID5 GPIO38
UMA/DIS	0=UMA 1=Dis.					
Reserve		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes

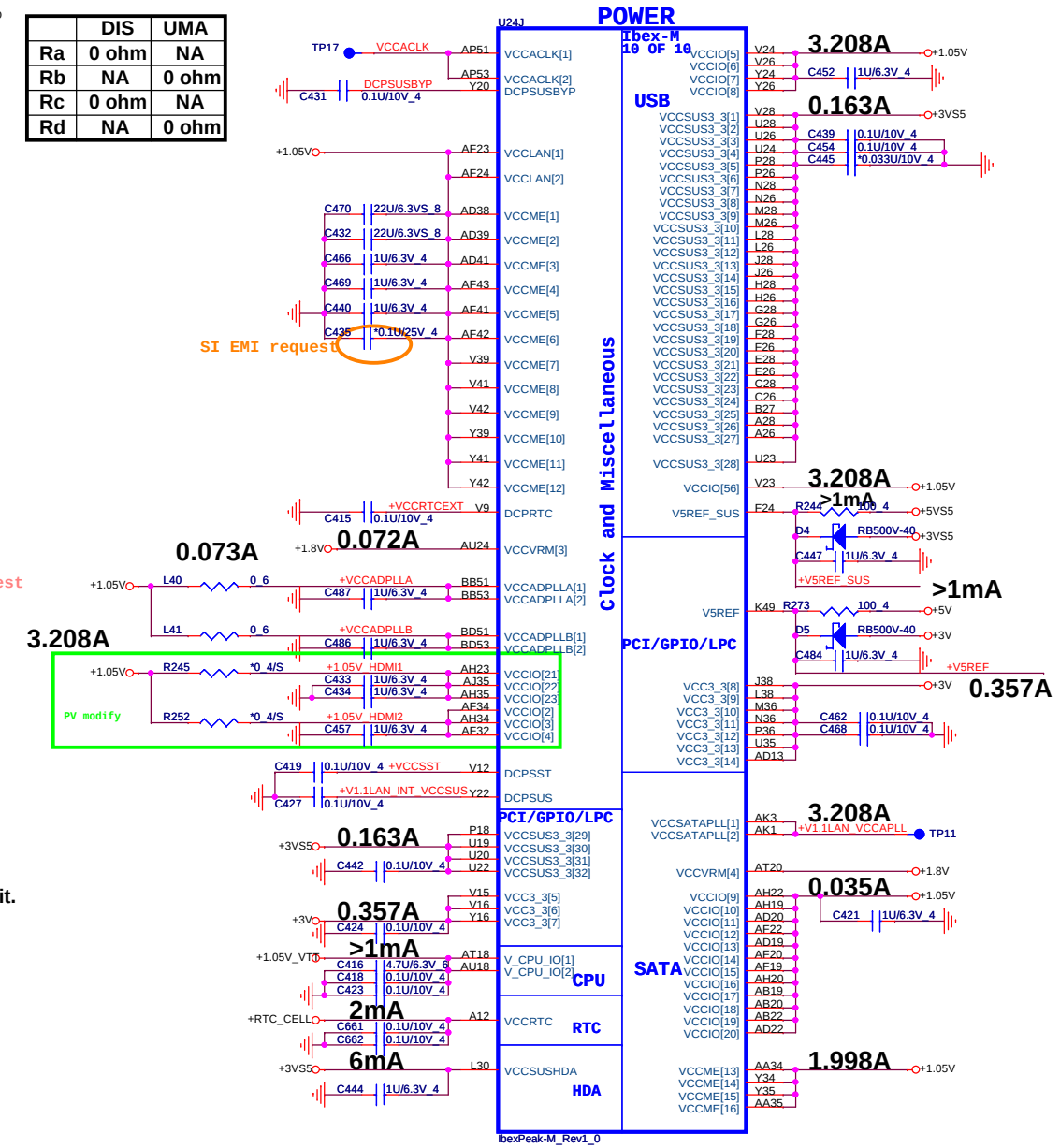


PROJECT : R12
Quanta Computer Inc.
Size: Custom | Document Number: PCH 4/5 (GPIO & Strap) | Rev: 1A
Date: Sunday, September 19, 2010 | Sheet 10 of 39

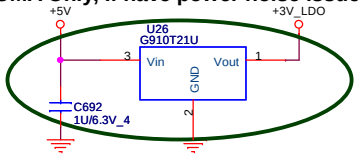
8/25 SI modify
Uninstall on UMA
Install on DIS

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm





UMA Only, If have power noise issue then stuff it.



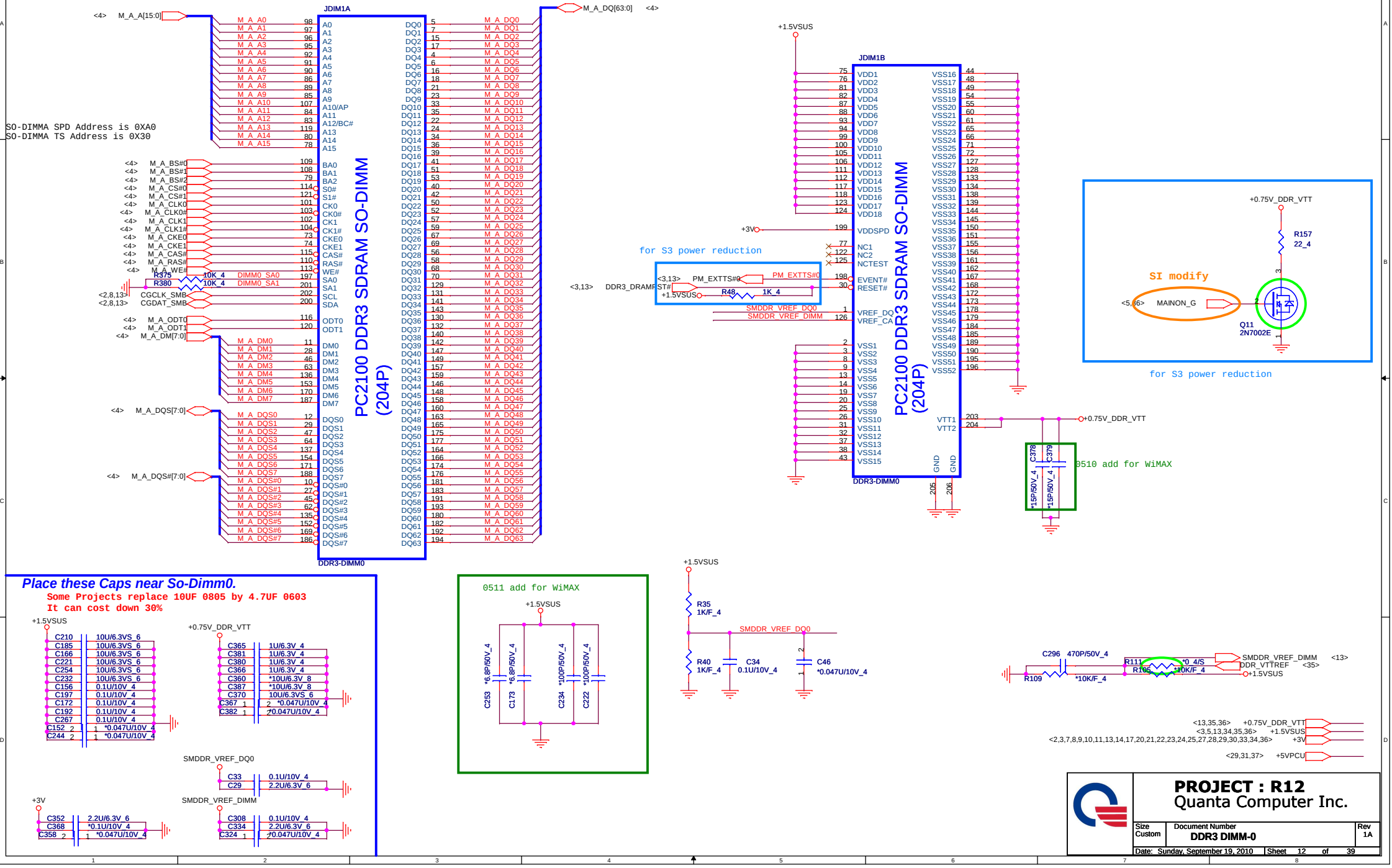
8/25 SI modify
Install LDO when UMA

<2,7,8,9,39> +1.05V
<3,5,10,29,32,33,38> +1.05V_VTT
<5,32> +1.8V
<2,3,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<3,7,8,9,10,26,31,32,34,35,36,38> +3VS5
<17,21,22,23,25,28,30,36> +5V
<20,26,31,32,33,34,35,36,38,39> +5VS5

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	1A

Date: Sunday, September 19, 2010 Sheet 11 of 39


JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0
M_A_A[15:0]
M_A_DQ[63:0]
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30
M_A_BS#0
M_A_BS#1
M_A_BS#2
M_A_CS#0
M_A_CS#1
M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_CKE0
M_A_CKE1
M_A_CAS#
M_A_RAS#
M_A_WE#
R375 10K_4 DIMM0_SA0
R380 10K_4 DIMM0_SA1
CGCLK_SMB
CGDAT_SMB
M_A_ODT0
M_A_ODT1
M_A_DM[7:0]
M_A_DQS[7:0]
M_A_DQS#[7:0]
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0
+1.5VSUS
+3V
for S3 power reduction
PM_EXTTS#0
DDR3_DRAMRST#
R48 1K_4
SMDDR_VREF_DQ0
SMDDR_VREF_DIMM
+0.75V_DDR_VTT
SI modify
MAINON_G
R157 22_4
Q11 2N7002E
for S3 power reduction
C378 *15P/50V_4
C379 *15P/50V_4
0510 add for WiMAX
Place these Caps near So-Dimm0.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
+1.5VSUS
C210 10U/6.3VS_6
C185 10U/6.3VS_6
C166 10U/6.3VS_6
C221 10U/6.3VS_6
C254 10U/6.3VS_6
C232 10U/6.3VS_6
C156 0.1U/10V_4
C197 0.1U/10V_4
C172 0.1U/10V_4
C192 0.1U/10V_4
C267 0.1U/10V_4
C152 *0.047U/10V_4
C244 *0.047U/10V_4
+0.75V_DDR_VTT
C365 1U/6.3V_4
C381 1U/6.3V_4
C380 1U/6.3V_4
C366 1U/6.3V_4
C360 *10U/6.3V_8
C387 *10U/6.3V_8
C370 10U/6.3VS_6
C367 *0.047U/10V_4
C382 *0.047U/10V_4
SMDDR_VREF_DQ0
C33 0.1U/10V_4
C29 2.2U/6.3V_6
+3V
C352 2.2U/6.3V_6
C368 *0.1U/10V_4
C358 *0.047U/10V_4
SMDDR_VREF_DIMM
C308 0.1U/10V_4
C334 2.2U/6.3V_6
C324 *0.047U/10V_4
0511 add for WiMAX
+1.5VSUS
C253 *6.8P/50V_4
C173 *6.8P/50V_4
C234 *100P/50V_4
C222 *100P/50V_4
+1.5VSUS
R35 1K/F_4
SMDDR_VREF_DQ0
R40 1K/F_4
C34 0.1U/10V_4
C46 *0.047U/10V_4
C296 470P/50V_4
R109 *10K/F_4
R111 *0_4/S
R105 *10K/F_4
SMDDR_VREF_DIMM <13>
DDR_VTTREF <35>
+1.5VSUS
<13,35,36> +0.75V_DDR_VTT
<3,5,13,34,35,36> +1.5VSUS
<2,3,7,8,9,10,11,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<29,31,37> +5VPCU
PROJECT : R12
Quanta Computer Inc.
Size Custom
Document Number DDR3 DIMM-0
Rev 1A
Date: Sunday, September 19, 2010
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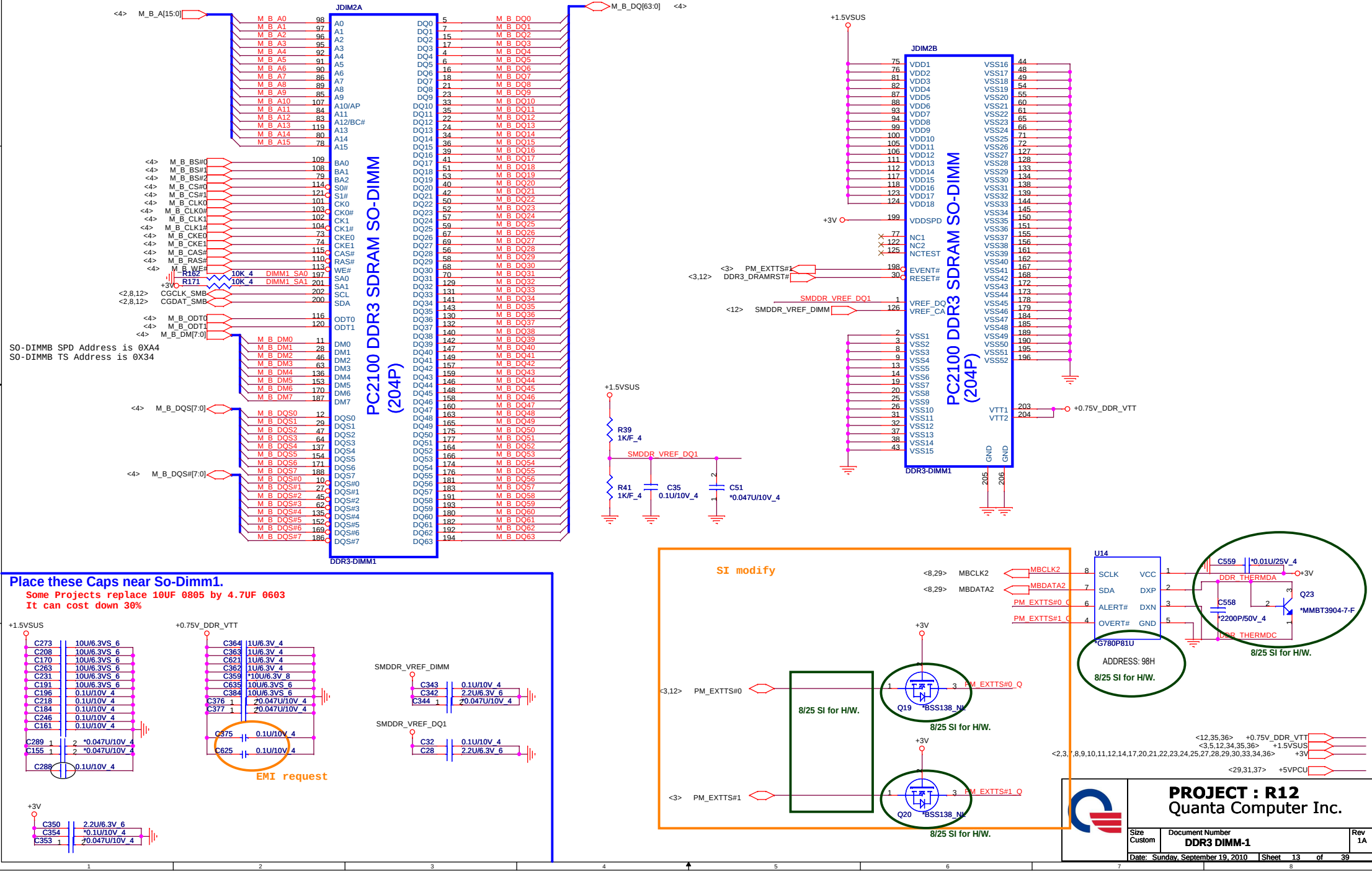
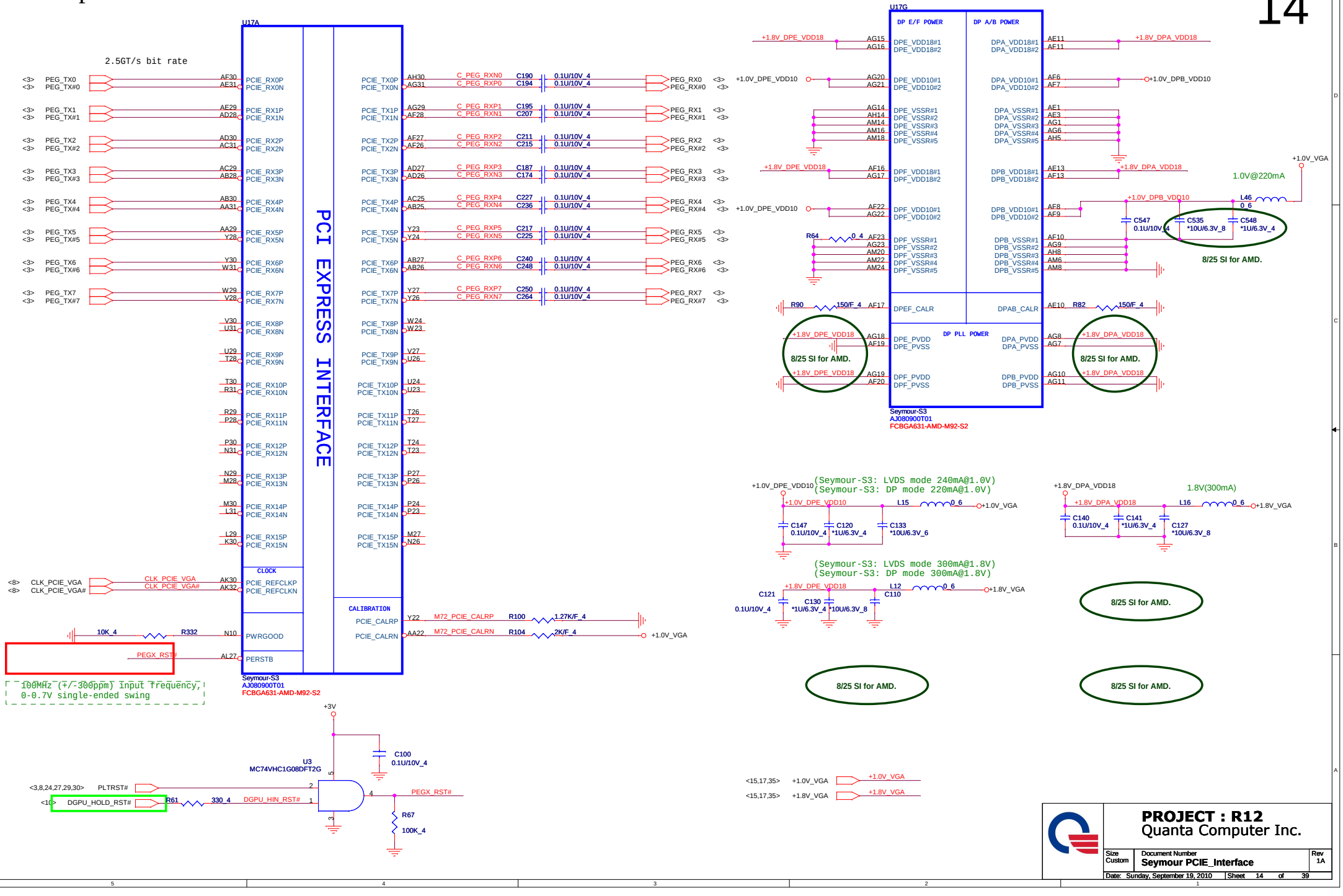
Text Stamp


JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
M_B_A[15:0]
M_B_DQ[63:0]
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
+1.5VSUS
+3V
+0.75V_DDR_VTT
R39 1K/F_4
R41 1K/F_4
C35 0.1U/10V_4
C51 *0.047U/10V_4
SMDDR_VREF_DQ1
SMDDR_VREF_DIMM
PM_EXTTS#1
DDR3_DRAMRST#
CGCLK_SMB
CGDAT_SMB
Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
EMI request
SI modify
U14
*G780P81U
ADDRESS: 98H
8/25 SI for H/W.
Q19 *BSS138_NL
Q20 *BSS138_NL
Q23 *MMBT3904-7-F
PROJECT : R12
Quanta Computer Inc.
DDR3 DIMM-1
Sunday, September 19, 2010

Text Stamp


U17A
PCI EXPRESS INTERFACE
2.5GT/s bit rate
CLOCK
CALIBRATION
PWRGOOD
PERSTB
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2
100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing
U17G
DP E/F POWER
DP A/B POWER
DP PLL POWER
DPEF_CALR
DPAB_CALR
8/25 SI for AMD.
1.0V@220mA
1.8V(300mA)
(Seymour-S3: LVDS mode 240mA@1.0V)
(Seymour-S3: DP mode 220mA@1.0V)
(Seymour-S3: LVDS mode 300mA@1.8V)
(Seymour-S3: DP mode 300mA@1.8V)
U3
MC74VHC1G08DFT2G
PROJECT : R12
Quanta Computer Inc.
Seymour PCIE_Interface
Date: Sunday, September 19, 2010
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MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63BFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-HC12
0100	Micron	128*16-800MHZ	MT41J128M16HA-125:D
0101	Reserved		
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11C
0111	Samsung- E die	64*16-900MHZ	K4W1G1646E-HC11
1000	Samsung- G die	64*16-900MHZ	K4W1G1646G-BC11
1001	Reserved		
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-HC11
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

GPIO15 GPIO20

Seymour	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.12V(Default)
TBD	1	1	NA

Access to SCL and SDA is mandatory on BACO designs for debug purposes

GPIO22(ROMCS#) PD without external VBIOS ROM

If no contact this pin to LVDS need pull low

Seymour uninstall Ra to meet AF24 N/C

DAC2 is NC on Seymour

Reserve for DB debug only

Reserve for DB debug only

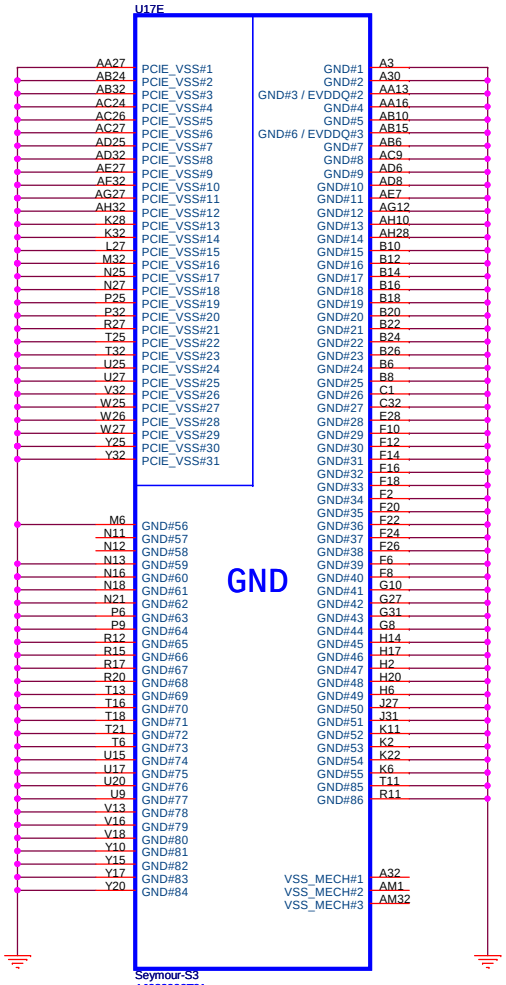
Seymour-S3--NC ROBSON--install

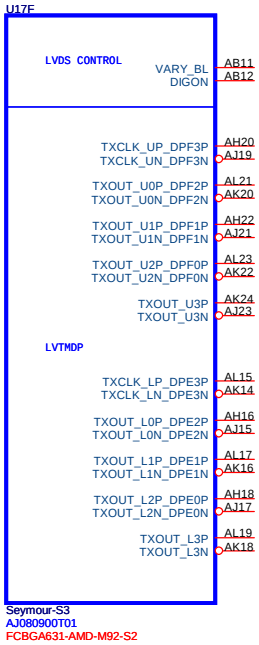
Robson-- Install Seymour- NC BACO mode -- install

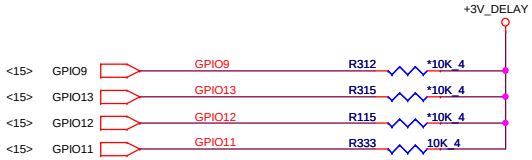
8/25 SI for H/W.

For Int Clk 27Mhz

8/25 SI for H/W.







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

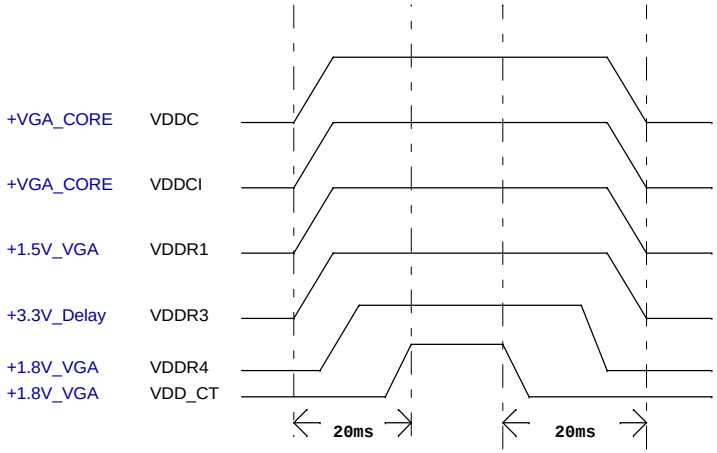
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

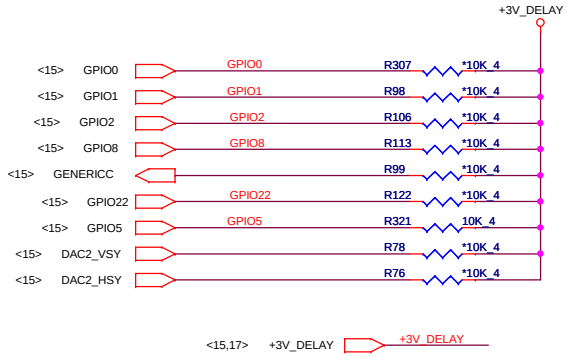
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour GND / LVDS/ Straps	1A
Date: Sunday, September 19, 2010	Sheet 16 of 39	

Text Stamp

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PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

1.5V (DDR3, MVDDQ = 1.5V@2.0A)

1.8V(110mA VDD_CT)

Gated 3.3V 60mA by VDDC

VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

1.8V(170mA VDDR4)

1.8V(75mA MPV18)

1.8V(90mA SPV18)

1.8V(40mA PCIE_PVDD)

8/25 SI for SMT.

1.0V_VGA(100mA SPV10)

1.8V(500mA)

1.0V(2.0A)

VDDC+VDDCI
0.85~1.1V(15A peak)(Ripple < 87.2mV)

0.95V~1.1V(2A VDDCI)

U17D

Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2

Note1.
Ra

Support BACO Mode

not stuff

8/25 SI for AMD.

8/25 SI for AMD.

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

Note1.

1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour_Power_and_NC	1A

Date: Sunday, September 19, 2010 | Sheet 17 of 39

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U17C

MEMORY INTERFACE

VMA_DQ0	K27	DQA_0	MAA_0	K17	VMA_MA0
VMA_DQ1	J29	DQA_1	MAA_1	J20	VMA_MA1
VMA_DQ2	H30	DQA_2	MAA_2	H23	VMA_MA2
VMA_DQ3	H32	DQA_3	MAA_3	G23	VMA_MA3
VMA_DQ4	G29	DQA_4	MAA_4	G24	VMA_MA4
VMA_DQ5	F28	DQA_5	MAA_5	H24	VMA_MA5
VMA_DQ6	F32	DQA_6	MAA_6	J19	VMA_MA6
VMA_DQ7	F30	DQA_7	MAA_7	K19	VMA_MA7
VMA_DQ8	C30	DQA_8	MAA_8	J14	VMA_MA8
VMA_DQ9	F27	DQA_9	MAA_9	K14	VMA_MA9
VMA_DQ10	A28	DQA_10	MAA_10	J11	VMA_MA10
VMA_DQ11	C28	DQA_11	MAA_11	J13	VMA_MA11
VMA_DQ12	E27	DQA_12	MAA_12	H11	VMA_MA12
VMA_DQ13	G26	DQA_13	MAA_13/BA2	G11	VMA_BA2
VMA_DQ14	D26	DQA_14	MAA_14/BA0	J16	VMA_BA0
VMA_DQ15	F25	DQA_15	MAA_15/BA1	L15	VMA_BA1
VMA_DQ16	A25	DQA_16			
VMA_DQ17	C25	DQA_17	DQMA_0	E32	VMA_DM0
VMA_DQ18	E25	DQA_18	DQMA_1	E30	VMA_DM1
VMA_DQ19	D24	DQA_19	DQMA_2	A21	VMA_DM2
VMA_DQ20	E23	DQA_20	DQMA_3	C21	VMA_DM3
VMA_DQ21	F23	DQA_21	DQMA_4	E13	VMA_DM4
VMA_DQ22	D22	DQA_22	DQMA_5	D12	VMA_DM5
VMA_DQ23	F21	DQA_23	DQMA_6	E3	VMA_DM6
VMA_DQ24	E21	DQA_24	DQMA_7	F4	VMA_DM7
VMA_DQ25	D20	DQA_25			
VMA_DQ26	F19	DQA_26	RDQSA_0	H28	VMA_RDQS0
VMA_DQ27	A19	DQA_27	RDQSA_1	C27	VMA_RDQS1
VMA_DQ28	D18	DQA_28	RDQSA_2	A23	VMA_RDQS2
VMA_DQ29	F17	DQA_29	RDQSA_3	E19	VMA_RDQS3
VMA_DQ30	A17	DQA_30	RDQSA_4	E15	VMA_RDQS4
VMA_DQ31	C17	DQA_31	RDQSA_5	D10	VMA_RDQS5
VMA_DQ32	E17	DQA_32	RDQSA_6	D6	VMA_RDQS6
VMA_DQ33	D16	DQA_33	RDQSA_7	G5	VMA_RDQS7
VMA_DQ34	E15	DQA_34			
VMA_DQ35	A15	DQA_35	WDQSA_0	H27	VMA_WDQS0
VMA_DQ36	D14	DQA_36	WDQSA_1	A27	VMA_WDQS1
VMA_DQ37	F13	DQA_37	WDQSA_2	C23	VMA_WDQS2
VMA_DQ38	A13	DQA_38	WDQSA_3	C19	VMA_WDQS3
VMA_DQ39	C13	DQA_39	WDQSA_4	C15	VMA_WDQS4
VMA_DQ40	E11	DQA_40	WDQSA_5	E9	VMA_WDQS5
VMA_DQ41	A11	DQA_41	WDQSA_6	C5	VMA_WDQS6
VMA_DQ42	C11	DQA_42	WDQSA_7	H4	VMA_WDQS7
VMA_DQ43	F11	DQA_43			
VMA_DQ44	A9	DQA_44	ODTA0	L18	VMA_ODT0
VMA_DQ45	C9	DQA_45	ODTA1	K16	VMA_ODT1
VMA_DQ46	E9	DQA_46			
VMA_DQ47	D8	DQA_47	CLKA0	H26	VMA_CLK0
VMA_DQ48	E7	DQA_48	CLKA0B	H25	VMA_CLK0#
VMA_DQ49	A7	DQA_49			
VMA_DQ50	C7	DQA_50	CLKA1	G9	VMA_CLK1
VMA_DQ51	E7	DQA_51	CLKA1B	H9	VMA_CLK1#
VMA_DQ52	A5	DQA_52			
VMA_DQ53	E5	DQA_53	RASA0B	G22	VMA_RAS0#
VMA_DQ54	C3	DQA_54	RASA1B	G17	VMA_RAS1#
VMA_DQ55	E1	DQA_55			
VMA_DQ56	G7	DQA_56	CASA0B	G19	VMA_CAS0#
VMA_DQ57	G6	DQA_57	CASA1B	G16	VMA_CAS1#
VMA_DQ58	G1	DQA_58			
VMA_DQ59	G3	DQA_59	CSA0B_0	H22	VMA_CS0#
VMA_DQ60	J6	DQA_60	CSA0B_1	J22	
VMA_DQ61	J1	DQA_61			
VMA_DQ62	J3	DQA_62	CSA1B_0	G13	VMA_CS1#
VMA_DQ63	J5	DQA_63	CSA1B_1	K13	
	K26	MVREFDA	CKEA0	K20	VMA_CKE0
	J26	MVREFSA	CKEA1	J17	VMA_CKE1
	J25	MEM_CALRN0	WEA0B	G25	VMA_WE0#
	K7	NC/TESTEN#2	WEA1B	H10	VMA_WE1#
	J8	MEM_CALRP1/DPC_CALR	PX_EN	AB16	PX_EN
	K25	MEM_CALRP0	RSVD#2	G14	
			RSVD#3	G20	VMA_MA13
DRAM_RST	L10	DRAM_RST			
CLKTESTA	K8	CLKTESTA			
CLKTESTB	L7	CLKTESTB			

Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2

8/25 SI for SMT.

PX_EN <17>

<19> VMA_ODT0
<19> VMA_ODT1
VMA_ODT0
VMA_ODT1

<19> VMA_RAS0#
<19> VMA_RAS1#
VMA_RAS0#
VMA_RAS1#

<19> VMA_CAS0#
<19> VMA_CAS1#
VMA_CAS0#
VMA_CAS1#

<19> VMA_WE0#
<19> VMA_WE1#
VMA_WE0#
VMA_WE1#

<19> VMA_CS0#
VMA_CS0#

<19> VMA_CS1#
VMA_CS1#

<19> VMA_CKE0
<19> VMA_CKE1
VMA_CKE0
VMA_CKE1

<19> VMA_CLK0
<19> VMA_CLK0#
VMA_CLK0
VMA_CLK0#

<19> VMA_CLK1
<19> VMA_CLK1#
VMA_CLK1
VMA_CLK1#

<19> VMA_WDQS[7..0]
VMA_WDQS[7..0]

<19> VMA_RDQS[7..0]
VMA_RDQS[7..0]

<19> VMA_DM[7..0]
VMA_DM[7..0]

<19> VMA_DQ[63..0]
VMA_DQ[63..0]

<19> VMA_MA[13..0]
VMA_MA[13..0]

<19> VMA_BA0
<19> VMA_BA1
<19> VMA_BA2
VMA_BA0
VMA_BA1
VMA_BA2

support 1Gbit
VRAM (64M X 16)

DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

+1.5V_VGA
R160 40.2/F_4 Ra
MVREFD
C326 0.1U/10V_4
R156 100/F_4 Rb

PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC

+1.5V_VGA
R175 40.2/F_4 Ra
MVREFS
C333 0.1U/10V_4
R167 100/F_4 Rb

+1.5V_VGA
R384 243/F_4
R131 3.1K_4
R127 150/F_4
R385 243/F_4

C316 *0.1U/10V_4
C591 *0.1U/10V_4
R118 *51.1/F_4
R314 *51.1/F_4

route 50ohms
single-ended/100ohms diff
and keep short
Debug only, for clock observation,
if not needed, DNI

<17,19,34> +1.5V_VGA
+1.5V_VGA

DRAM_RST
R129 10_4
R132 51_4
DRAM_RST_M
DRAM_RST_M <19>
R128 5.1K_4
C335 120P/50V_4
8/25 SI for AMD.

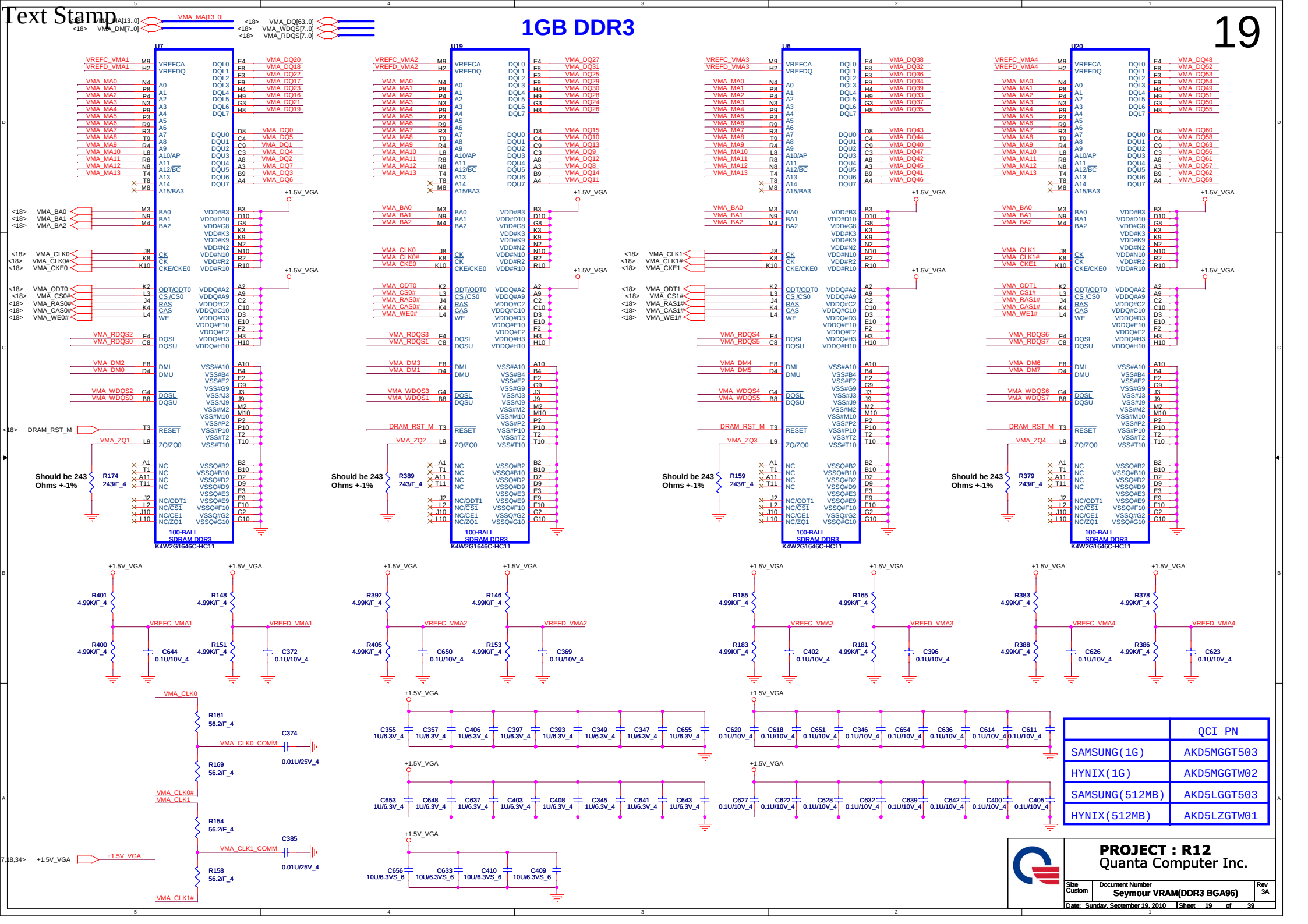
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour/MEM_Interface	1A

Date: Sunday, September 19, 2010 | Sheet 18 of 39

Text Stamp

1GB DDR3



	QCI PN
SAMSUNG(1G)	AKD5MGGT503
HYNIX(1G)	AKD5MGGTW02
SAMSUNG(512MB)	AKD5LGGT503
HYNIX(512MB)	AKD5LZGTW01

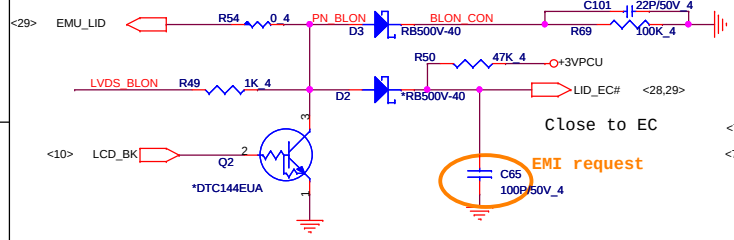
PROJECT : R12
Quanta Computer Inc.

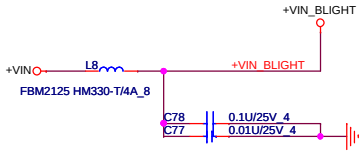
Size	Document Number	Rev
Custom	Seymour VRAM(DDR3 BGA96)	3A

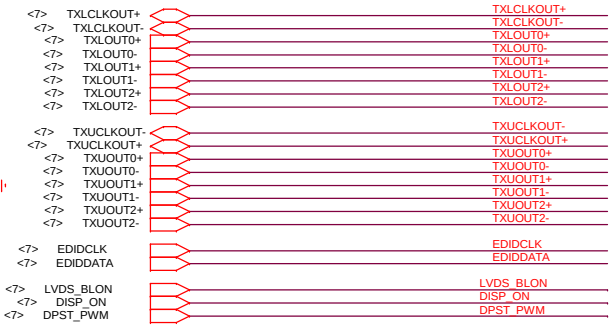
Date: Sunday, September 19, 2010 | Sheet 19 of 39

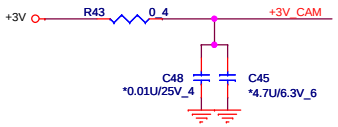
Text Stamp

LID Switch



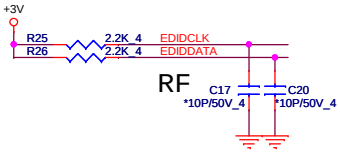


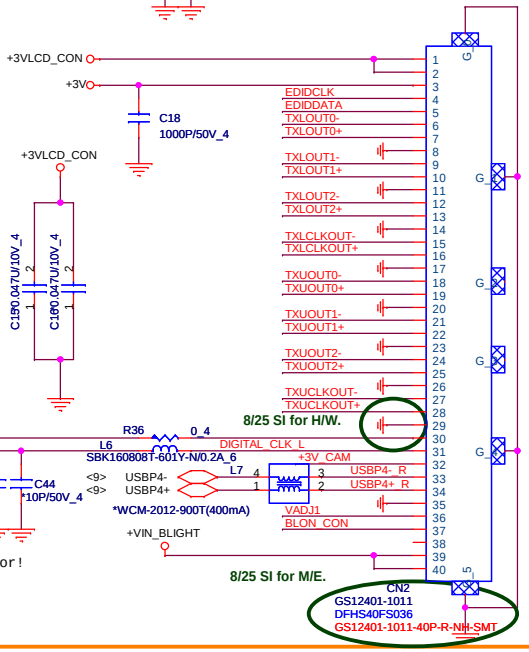




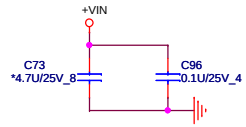
Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

follow L4 location



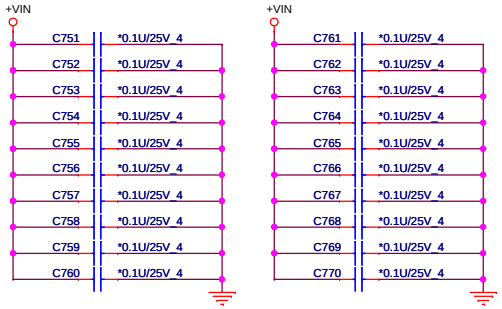


EMI & RF



8/25 SI for H/W.

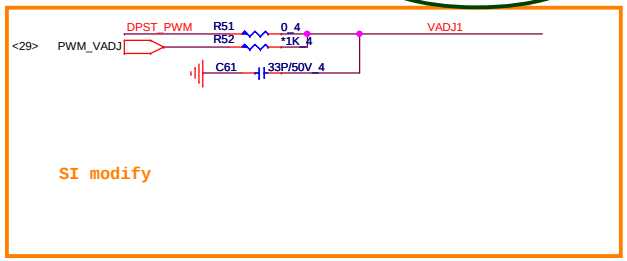
Coupling CAP.



8/25 SI for H/W.

change to +5VS5

1A



<7,28,29,31,37> +3VPCU
<2,3,7,8,9,10,11,12,13,14,17,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<23,34,36,37> +12VALW
<31,32,33,34,35,36,37,38,39> +VIN

PROJECT : R12
Quanta Computer Inc.

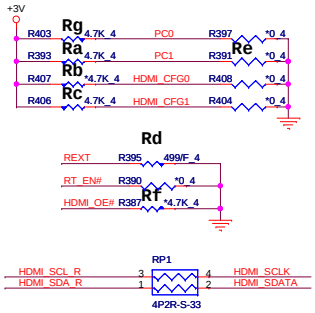
Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

Date: Sunday, September 19, 2010 | Sheet 20 of 39

Text Stamp

For UMA HDMI function

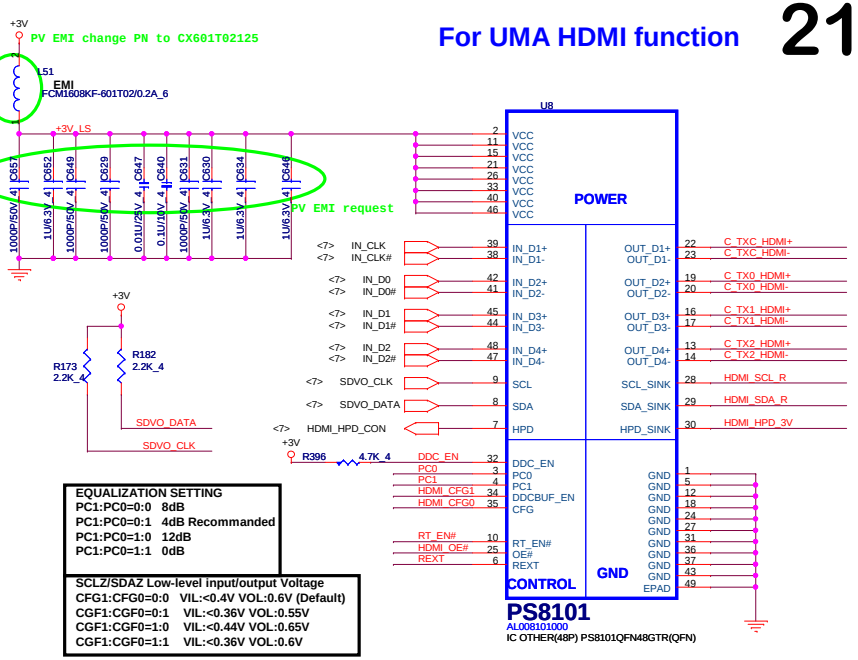
Signals		PDT	PIM	CHR
PC1	Ra	4.7K	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	4.7K	1.2K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	NC	4.7K
PC0	Rg	4.7K	4.7K	4.7K



Vender	Part	Part Number	Part Description
PDT	PS8101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007318002	IC OTHER(48P) CH7318C-BF-TR(QFN)

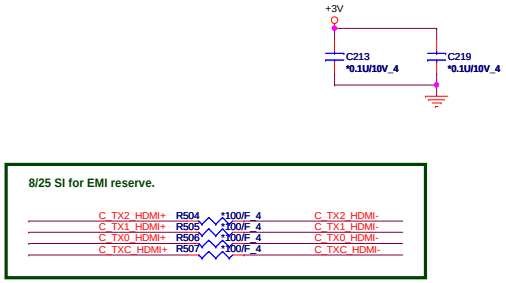
9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

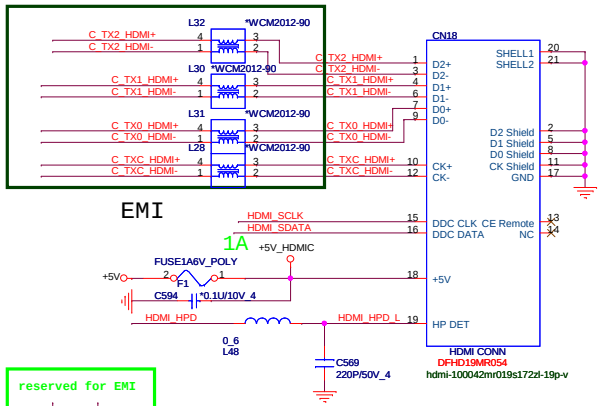
CHR : need Na R1182, add R1027 for capella

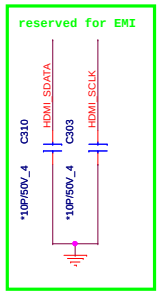


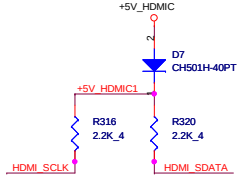
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

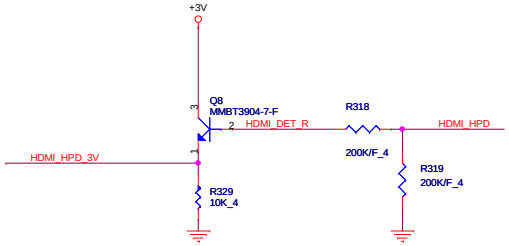
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V











PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A

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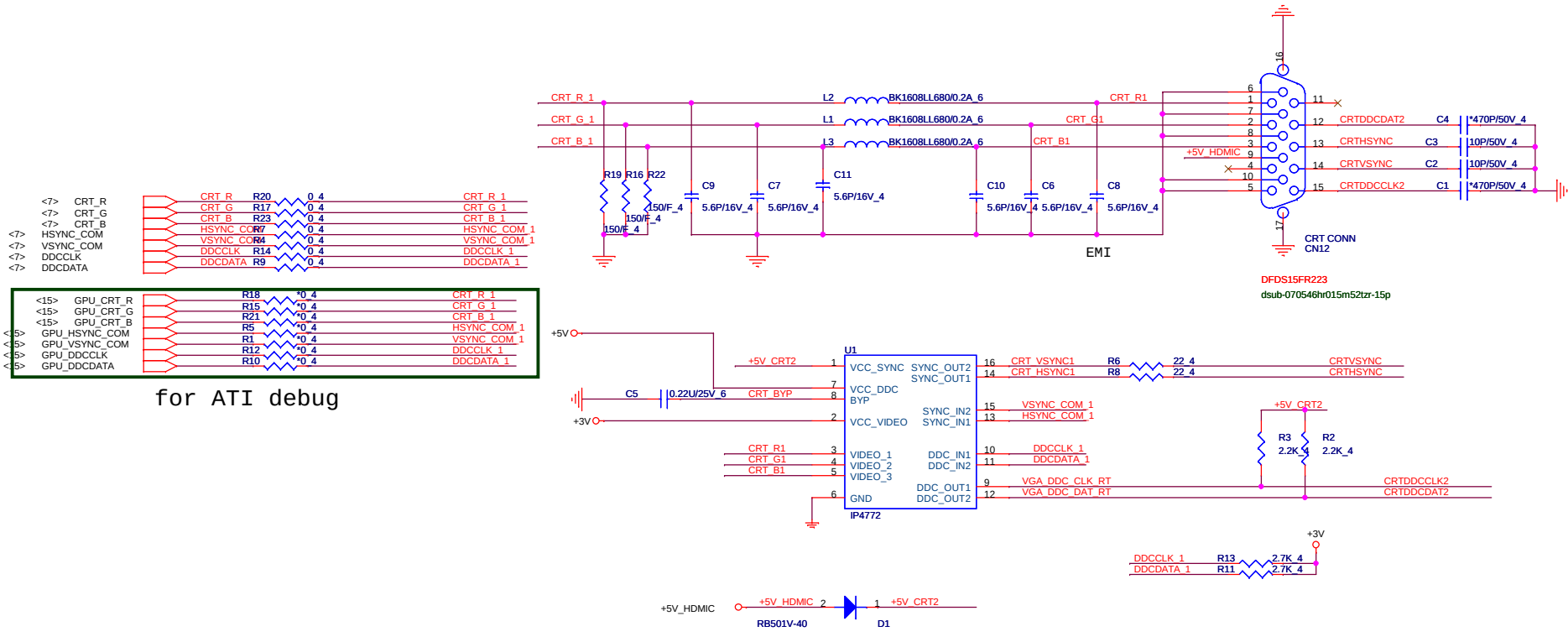
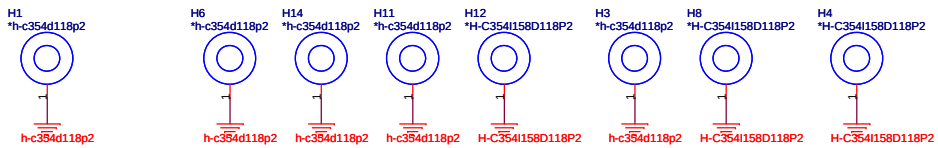
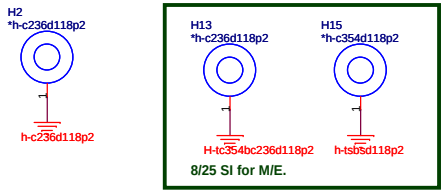
CRT PORT

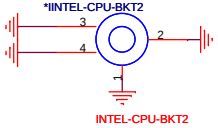


HOLE

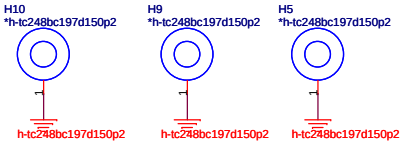




CPU



VGA



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A

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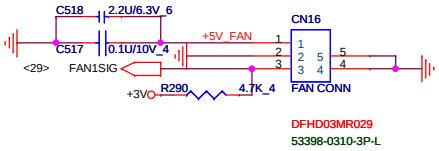
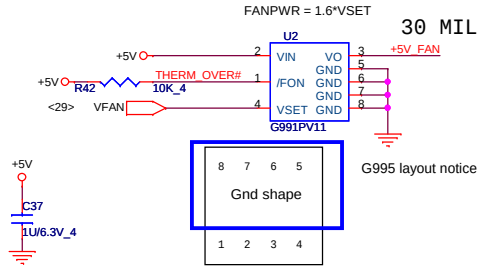
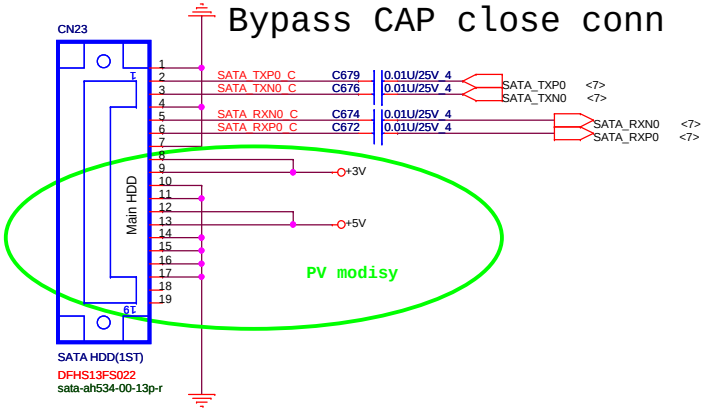
Text Stamp

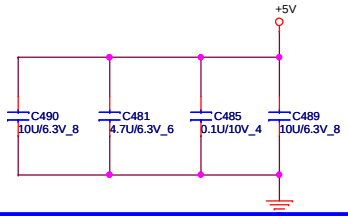
CPU FAN



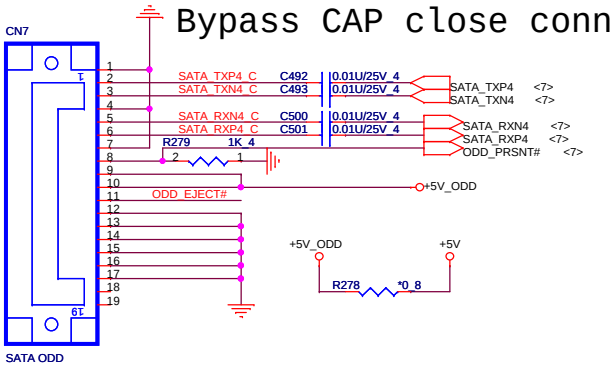


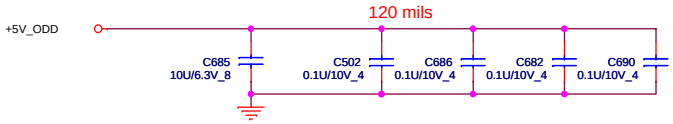
SATA HDD CONNECTOR

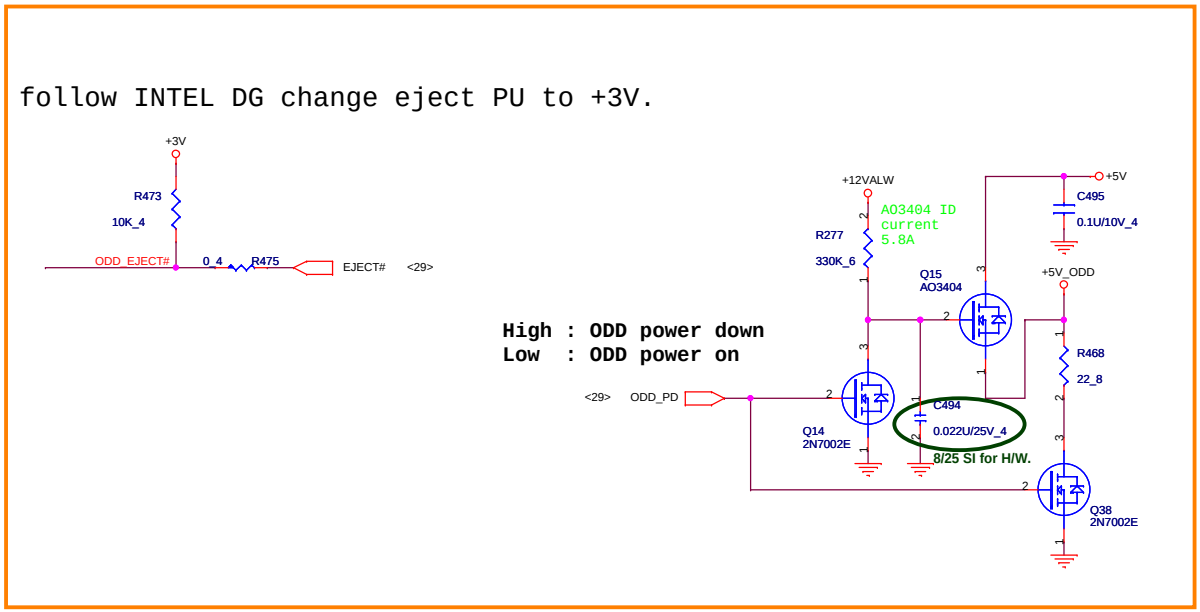




SATA ODD CONNECTOR







PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

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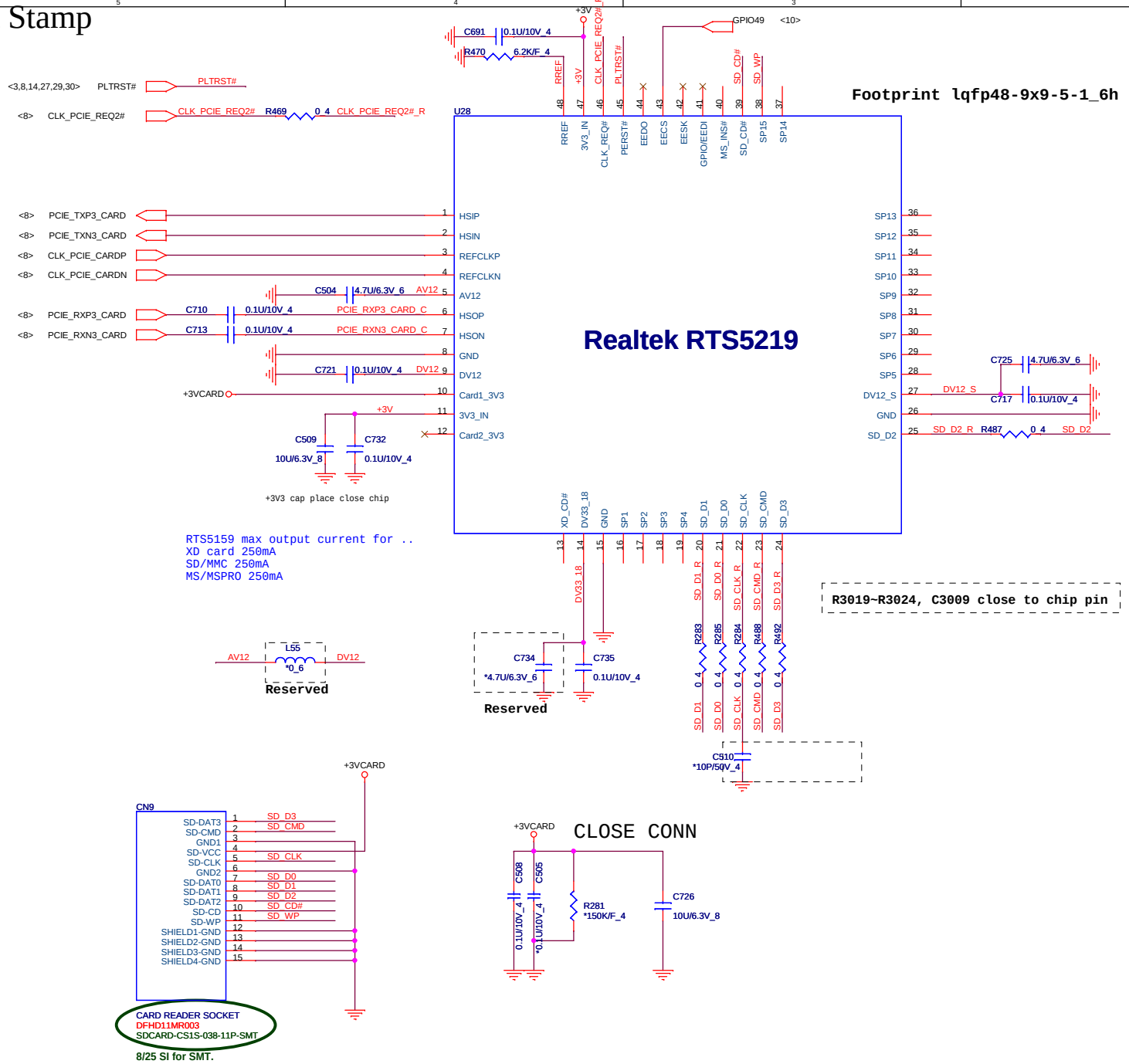

Quanta Computer Inc.	**PROJECT : R12**	
Size: Custom	Document Number: **RTS5219 & CR SOCKET &HOLE**	Rev: 1A
Date: Sunday, September 19, 2010	Sheet 24 of 39	

<2,3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,27,28,29,30,33,34,36> +3V

<11,17,21,22,23,28,30,36> +5V

Close to CODEC

Close to CODEC

>40mils trace

Close to CODEC

>40mils trace

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

HDA Bus

TO Digital MIC

TO Headphone jack

TO Audio Jack MIC

TO Internal Speakers

Check SB side and vendor reply it should reserve only

Check layout mount location

C10625 close C10629, and C10625 close Chip

check value

R10453 close R10454

8/25 SI for IDT recommend.

8/25 SI for IDT recommend.

8/25 SI for IDT recommend.

EMI Request

INT. SPEAKER

FOR EMI

Vset=1.242V

U27

92HD80B1X5NLGXTA48

Digital

Analog

U25

TPS793475

D11 RB500V-40

2N7002E Q40

INT SPEAKER CONN

CN11 DFHD04MR142 3800-X04N-00X-4P-L

Text Stamp

BLUETOOTH

EMI request

BLUELED C496 *1000P/50V_4

300mA

change to +3VS5

+3VS5 +3VS5

R280 4.7K_4

Q16 ME2303T1

24mil 300mA

Q17 DTC144EUA

<10,30> BT_OFF#

C503 *0.01U/25V_4

+3VPCU_BT

C498 0.1U/10V_4 C499 *10U/6.3V_8

CN8

BTCON_P1 T38

USBP2- BLUELED <29,30>

USBP2+ USBP2- <9>

+3VPCU_BT USBP2+ <9>

C497 *1000P/50V_4

BLUE TOOTH CONN

87213-0600-6P-L

DFHD06MR058

LEFT SIDE USBX2

change to AL000547005

2A 2A

change to +5VS5

+5VS5 U23 80 mils (Iout=2A) +5V_USBP0

VIN1 VIN2 EN GND OUT3 OUT2 OUT1 OC

G547E2P81U

<29> USBPW_ON#

C664 1U/6.3V_4

C348 470P/50V_4

C351 0.1U/10V_4

C414 470P/50V_4

C413 0.1U/10V_4

C660 100U/25V

8/25 SI for H/W.

change to ELEC CAP

1A

C356 *0.1U/10V_4

R149 L33 *0_4

+5V_USBP0

USBP0- R

USBP0+ R

WCM2012-90

R152 *0_4

<9> USBP0-

<9> USBP0+

CN19 USB CONN

DFHD04MR133

usb-020173mr004s53qzl-4p-r-v

8/25 SI for EMI.

1A

C411 *0.1U/10V_4

R225 L36 *0_4

+5V_USBP0

USBP1- R

USBP1+ R

WCM2012-90

R226 *0_4

<9> USBP1-

<9> USBP1+

CN20 USB CONN

DFHD04MR133

usb-020173mr004s53qzl-4p-r-v

8/25 SI for EMI.

Right SIDE USBX1

C27 0.1U/10V_4 +5VS5

<29> USBPW_ON#

R502 *0_4

<9> USBP8-

<9> USBP8+

USBP8- R

USBP8+ R

L5 WCM2012-90

R503 *0_4

8/25 SI for EMI.

CN1 USB board

DFFC06MR001

88513-0601-6P-L-SMT

EMI request

USBPW_ON# C19 220P/50V_4

Line out

SENSE_PHONE R465 20K/F_4 SENSE_A SENSE_A <25>

SENSE_MIC R256 10K/F_4 SENSE_A

AGND SHIELD

AGND SHIELD

AGND SHIELD

<25> HPOUT_L HPOUT_L R482 16/F_4 HPOUT_L1 L39 SBK160808T-301Y-N/0.2A_6 HPOUT_L2

<25> HPOUT_R HPOUT_R R480 16/F_4 HPOUT_R1 L42 SBK160808T-301Y-N/0.2A_6 HPOUT_R2

R275 20K/F_4

R270 20K/F_4

C491 1000P/50V_4

C476 1000P/50V_4

AGND

C483 0.1U/10V_4 C488 0.1U/10V_4

AGND

CN22 DFTJ06FR335 audio-311105-2-6p

AEC_311105-2 Normal Open

AGND

SENSE_PHONE

MIC

<25> VREFOUT_C VREFOUT_C C455 1U/6.3V_4 AGND

R248 3.9K/F_4

R246 3.9K/F_4

<25> MIC_L MIC_L C688 2.2U/6.3V_6 MIC_L1 L37 SBK160808T-301Y-N/0.2A_6 MIC_IN_L

<25> MIC_R MIC_R C689 2.2U/6.3V_6 MIC_R1 L38 SBK160808T-301Y-N/0.2A_6 MIC_IN_R

C456 220P/50V_4

C436 220P/50V_4

AGND

CN21 DFTJ06FR335 audio-311105-2-6p

AGND AEC_311105-2 Normal Open AGND

SENSE_MIC

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	1A

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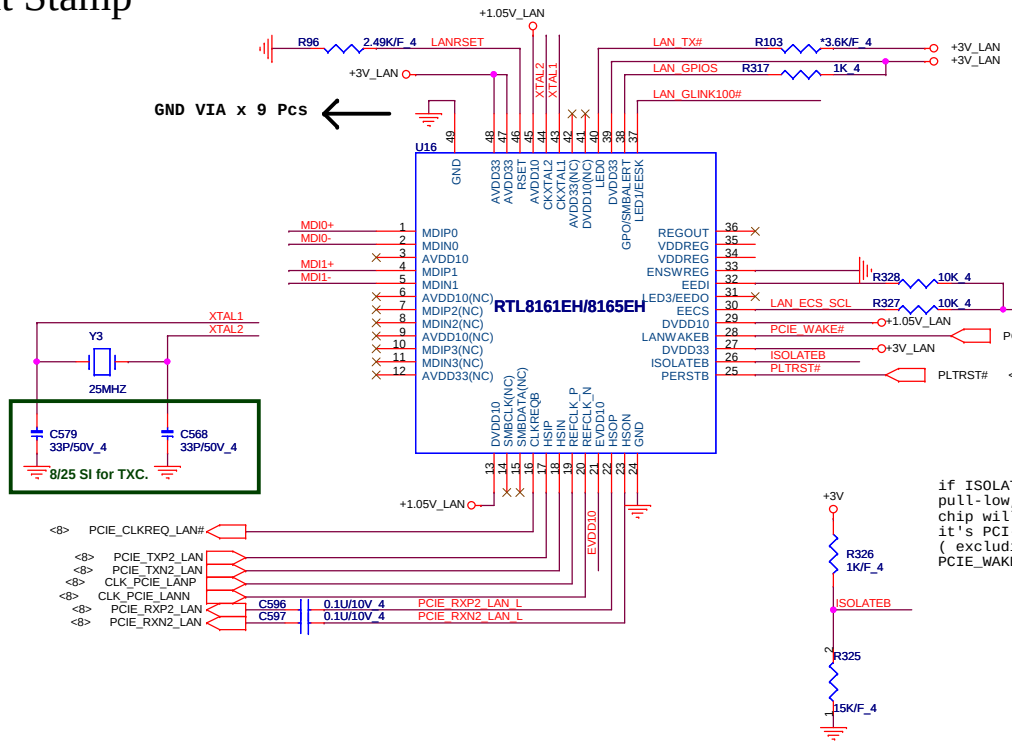
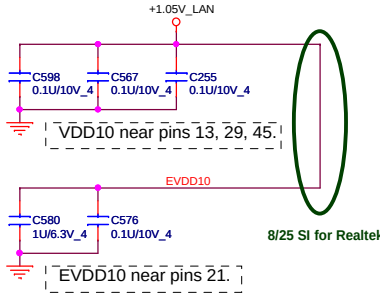
Text Stamp



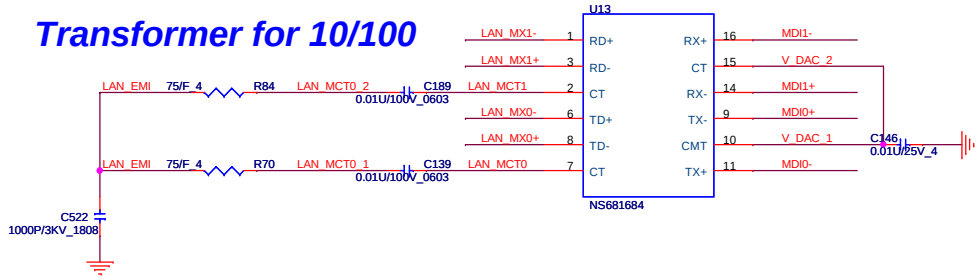
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

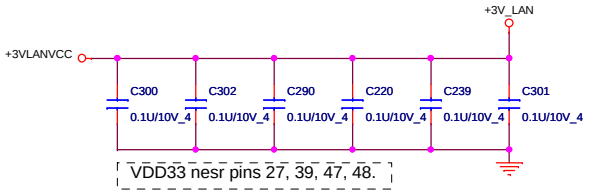
IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

Power trace Layout 寬度> 60mil
>60mil

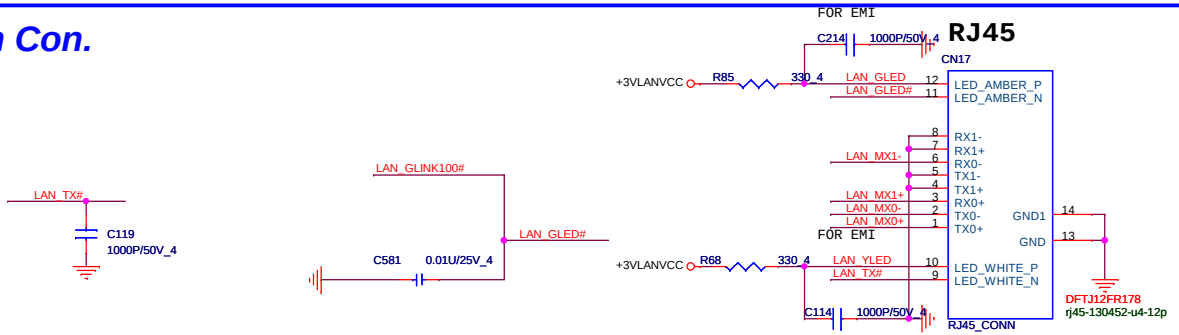


Transformer for 10/100





Lan Con.



<36> +3VLANVCC
<2,3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,28,29,30,33,34,36> +3V

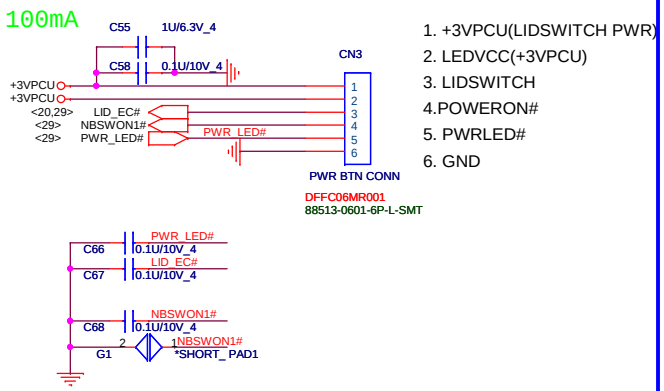
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8165EH	1A
Date: Sunday, September 19, 2010	Sheet 27 of 39	

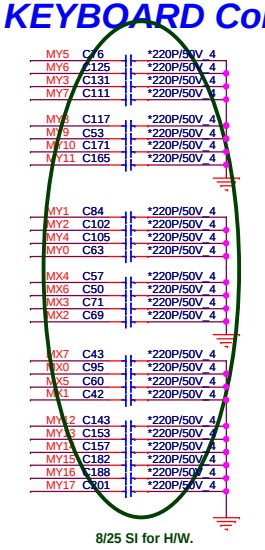
Text Stamp

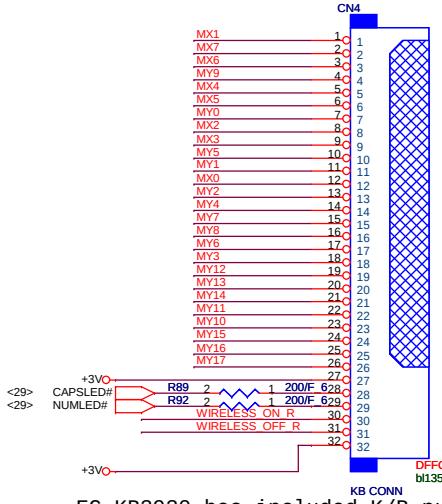
28

POWER BOTTON CONNECT

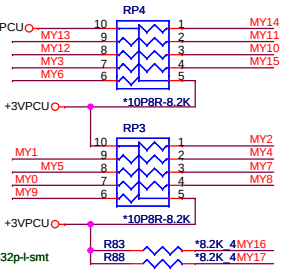


KEYBOARD Con.



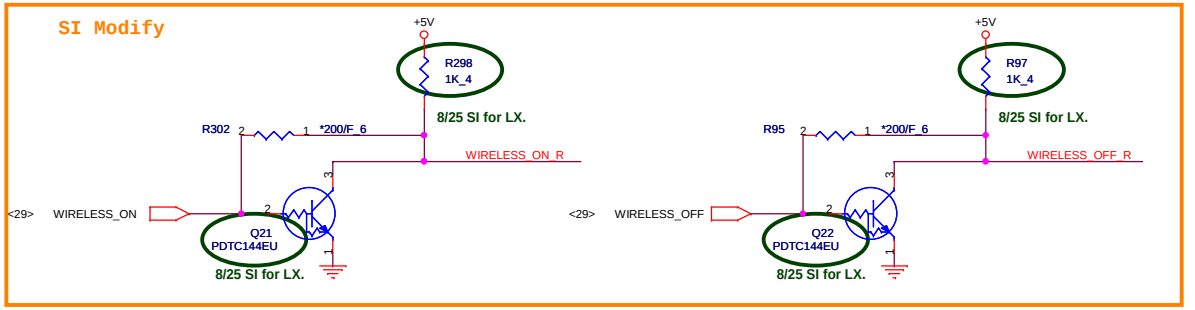


KEYBOARD PULL-UP

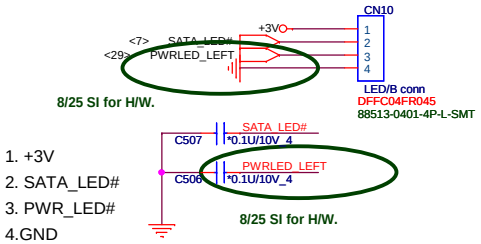


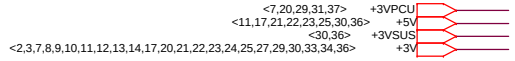
EC KB3930 has included K/B pull-up resistor and function

SI Modify



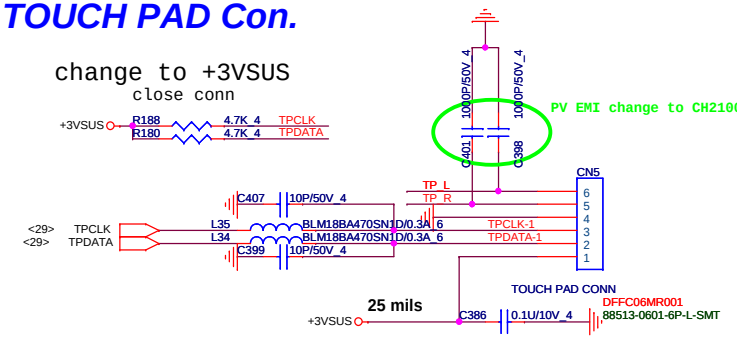
LED Con.



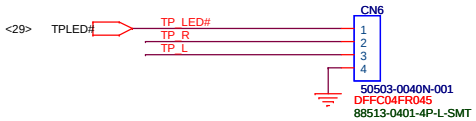


TOUCH PAD Con.

change to +3VSUS
close conn



To TOUCH PAD SW board



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

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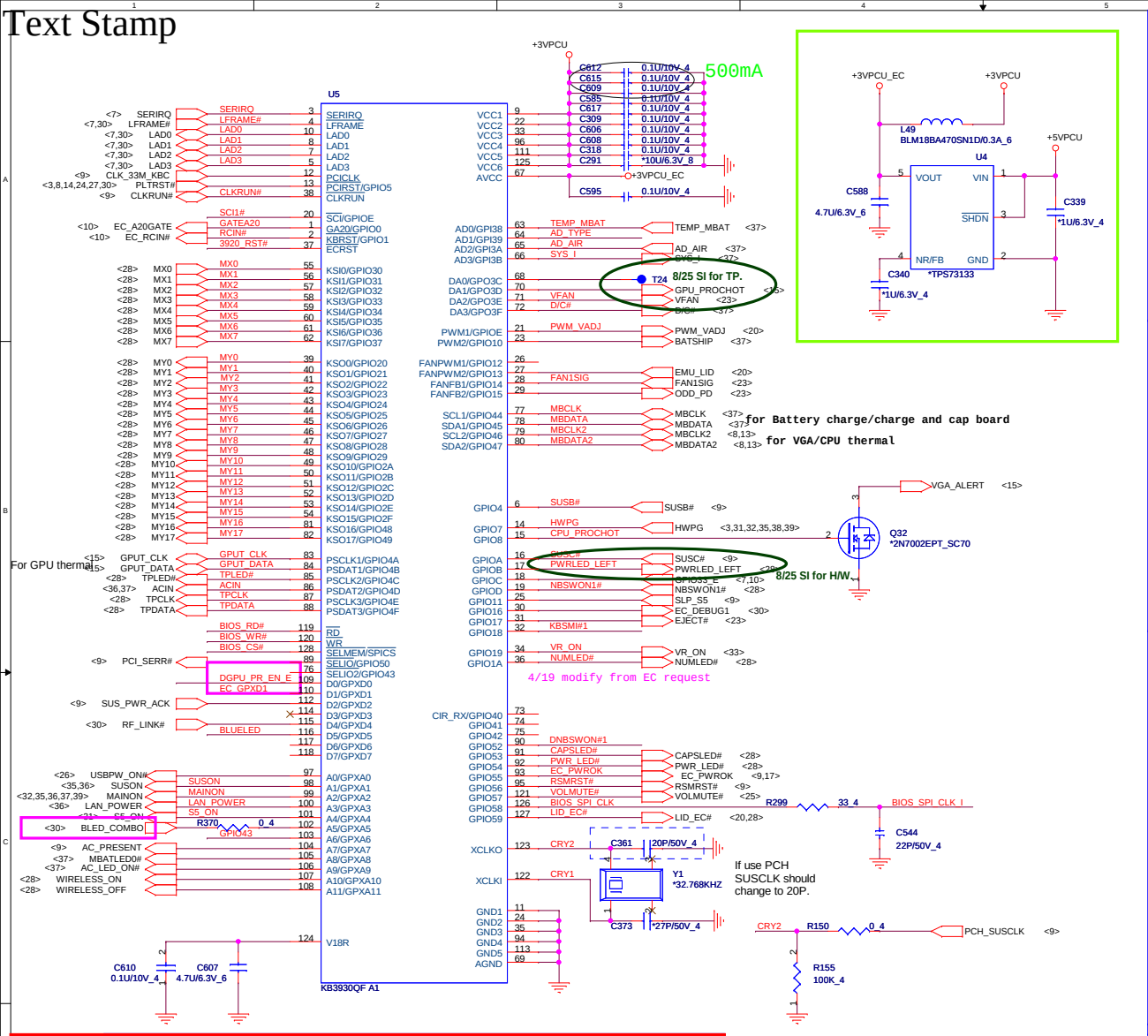
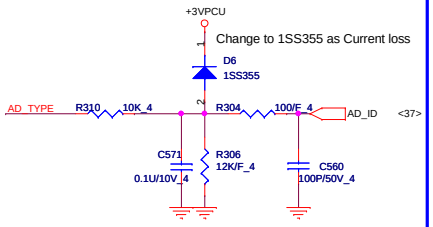
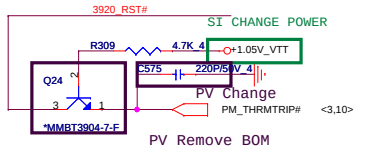
Text Stamp

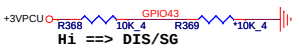


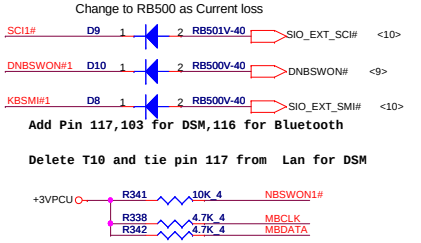
adapter Type check



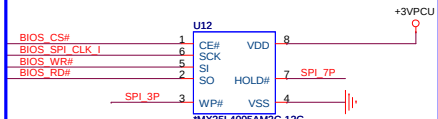


adapter select for EC





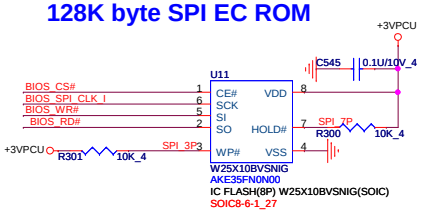
512K byte SPI EC ROM



Vender

Socket DG008000031

128K byte SPI EC ROM



Vender

Socket DG008000031

EON - EN25F10-100GIP

AKE35FN0Q00 IC FLASH(8P) EN25F10-100GIP(SOIC)

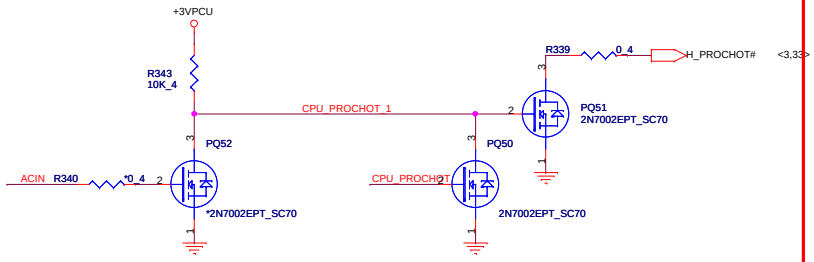
WINBOND - W25X10BVSNIG

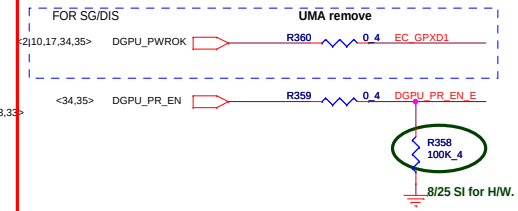
AKE35FN0N00 IC FLASH(8P) W25X10BVSNIG(SOIC)

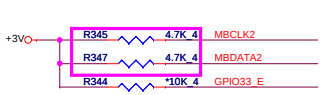
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high

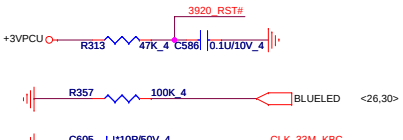
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low

Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high



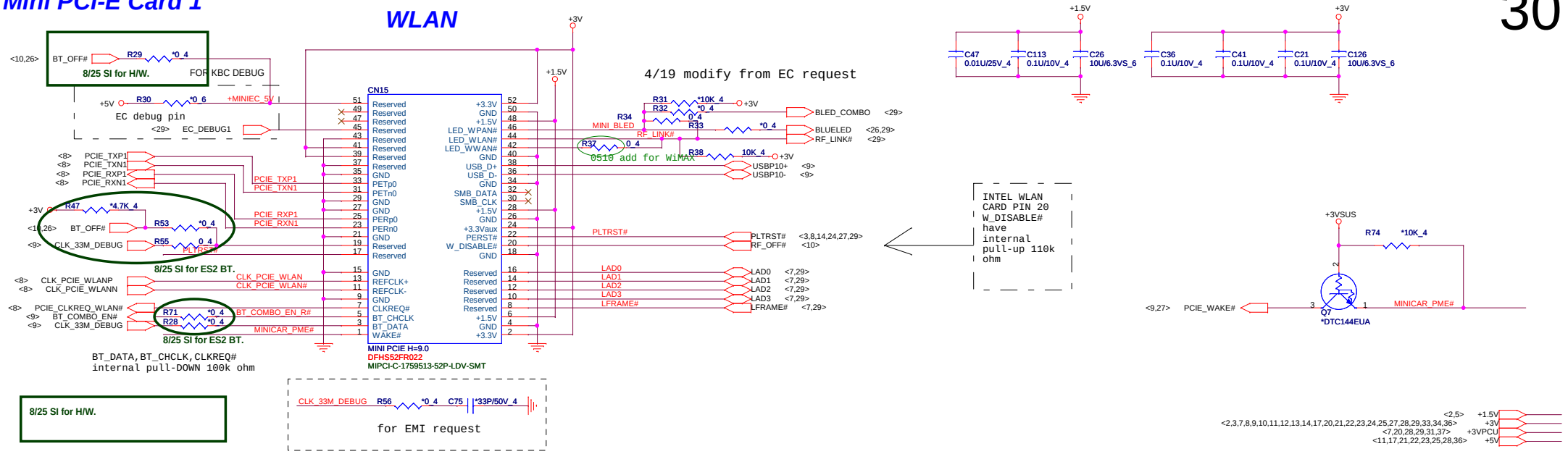






Mini PCI-E Card 1

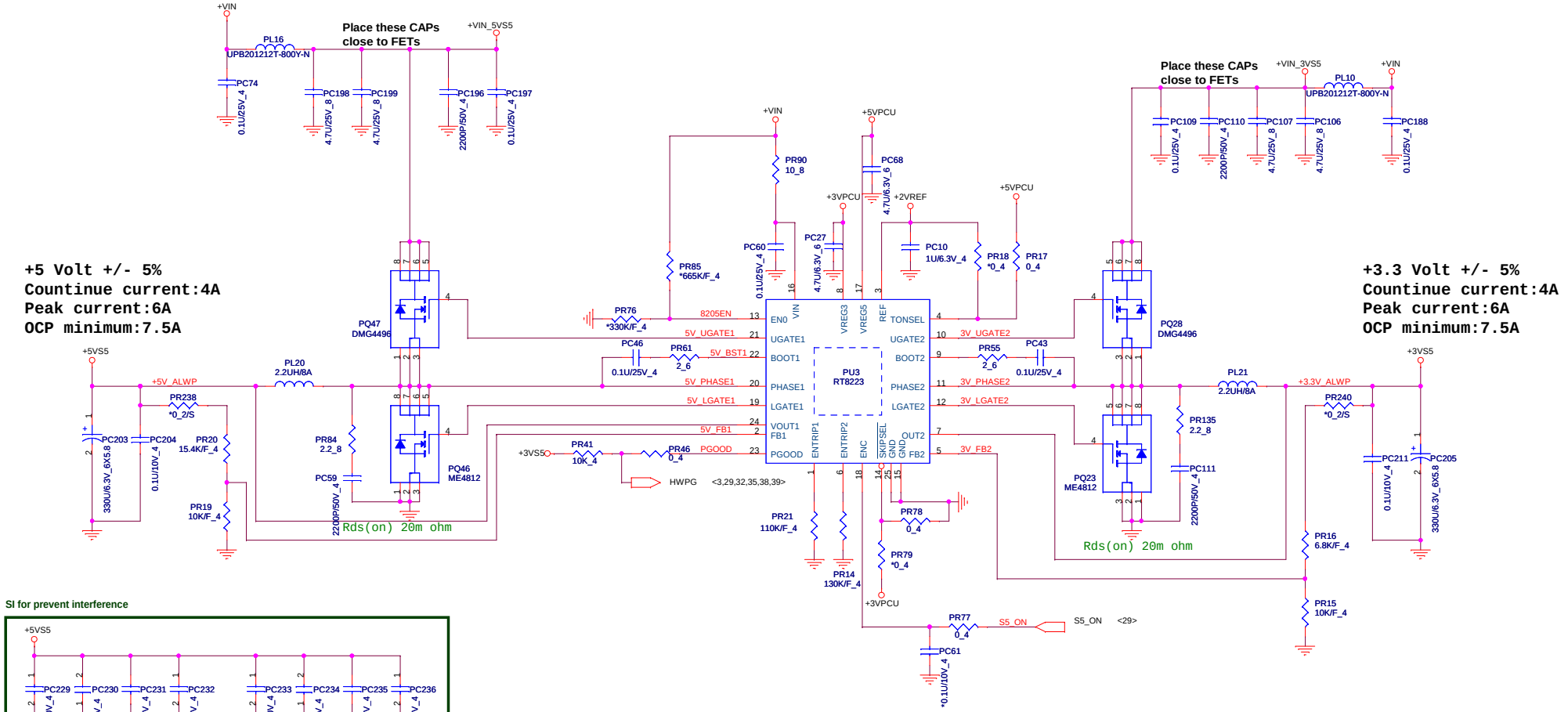
WLAN



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X1	1A

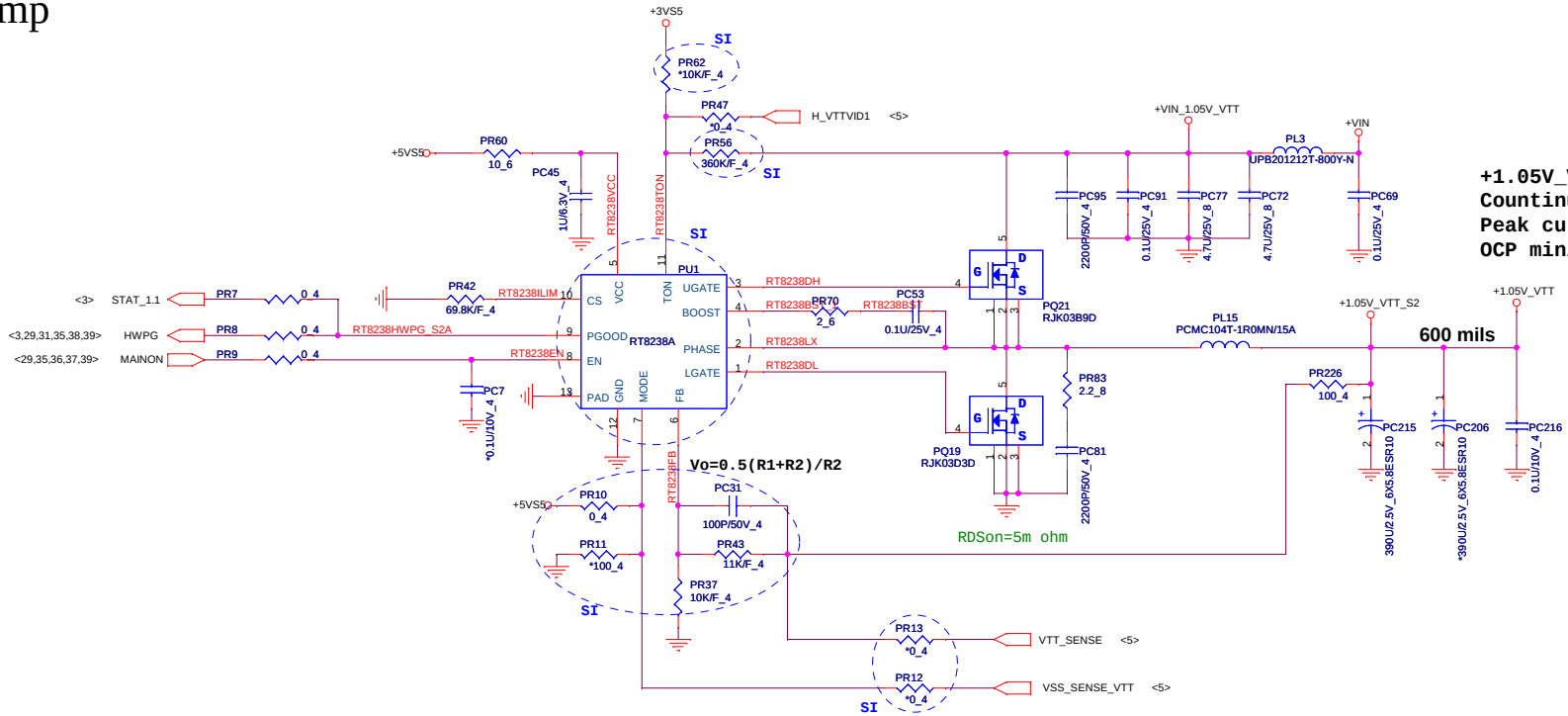
Date: Sunday, September 19, 2010 Sheet 30 of 39



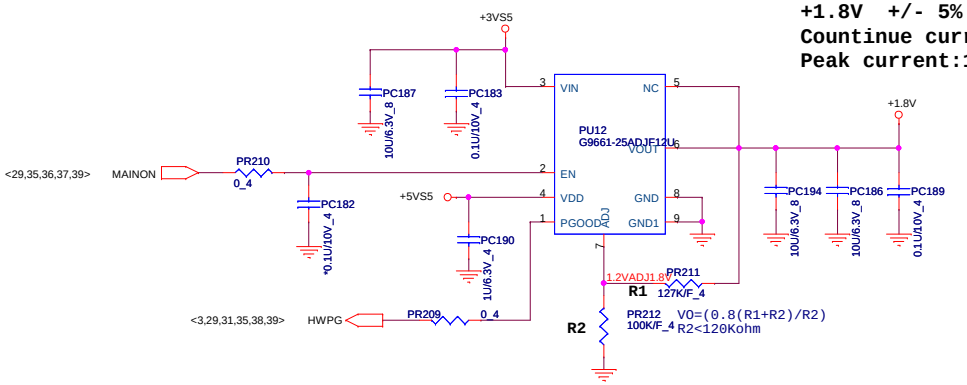
Size: Custom	Document Number: +5V/+3V (RT8206B)		Rev: 1A
Date: Sunday, September 19, 2010	Sheet 31 of 39		

PROJECT : R12
Quanta Computer Inc.

Text Stamp



+1.05V_VTT Volt +/- 5%
Countinue current:10A
Peak current: 16A
OCP minimum: 18A



+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V VTT / PCH	1A

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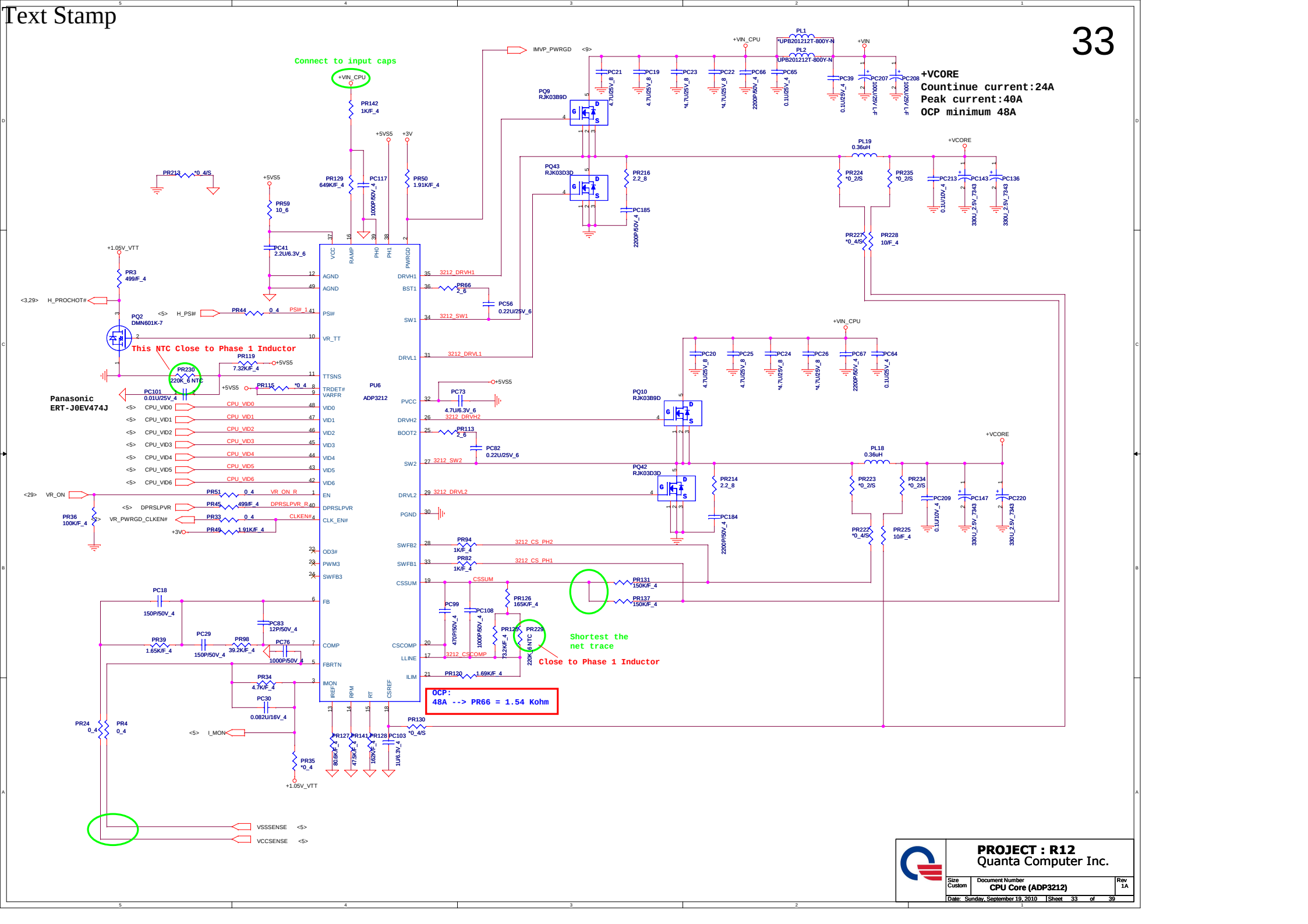
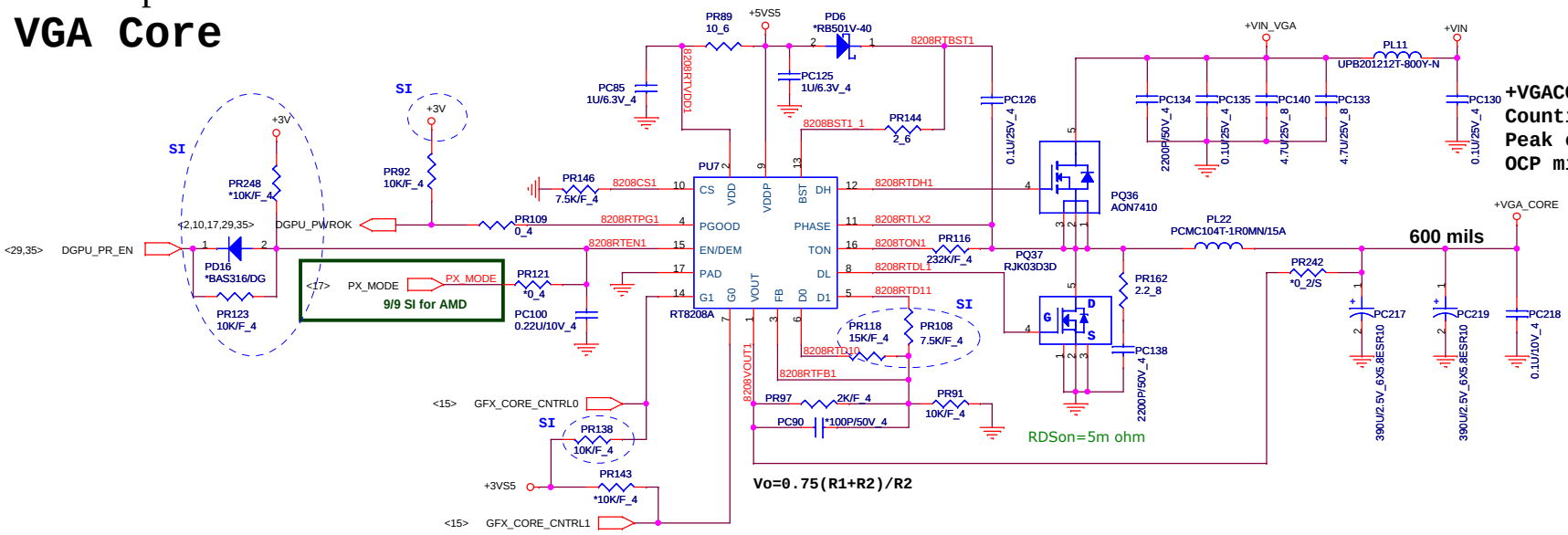
Text Stamp

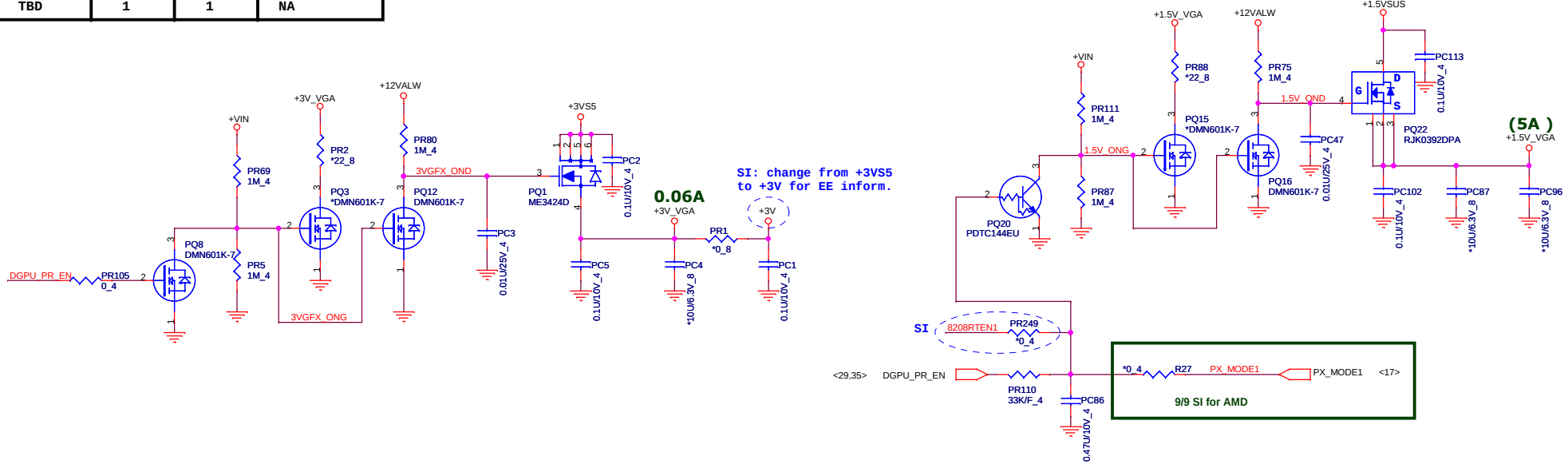

Connect to input caps
+VCORE
Countinue current:24A
Peak current:40A
OCP minimum 48A
This NTC Close to Phase 1 Inductor
Panasonic
ERT-J0EV474J
PU6
ADP3212
Shortest the
net trace
Close to Phase 1 Inductor
OCP:
48A --> PR66 = 1.54 Kohm
PROJECT : R12
Quanta Computer Inc.
CPU Core (ADP3212)
Date: Sunday, September 19, 2010
Sheet 33 of 39

Text Stamp

VGA Core



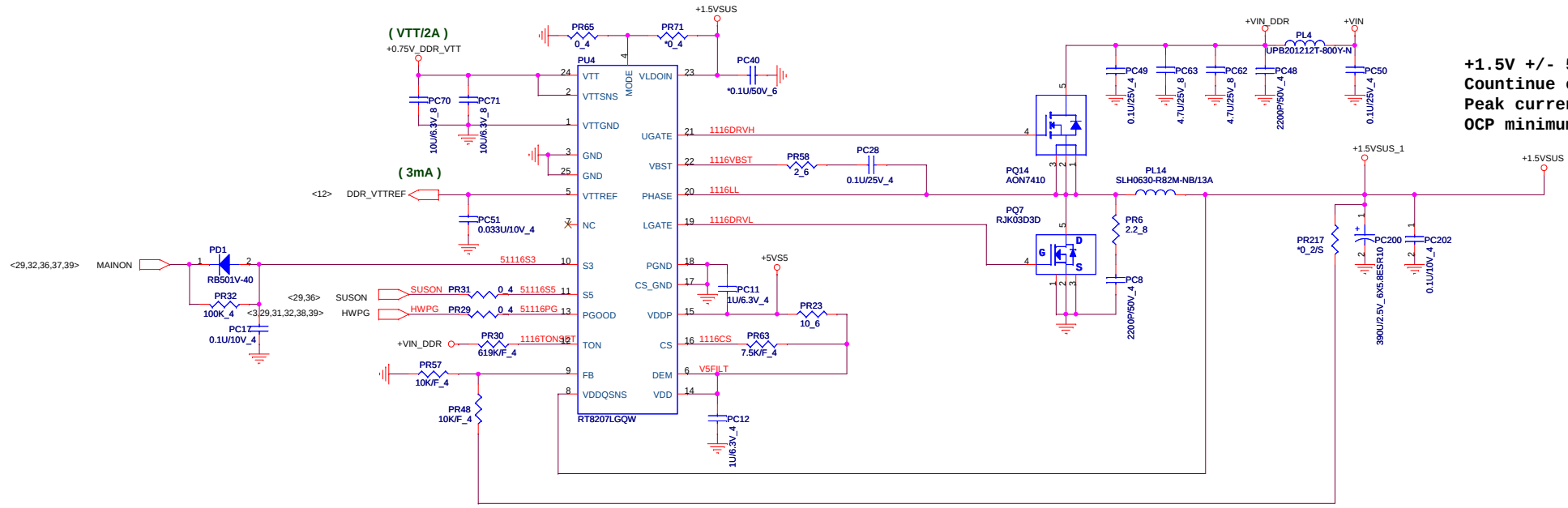
Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA



PROJECT : R12
Quanta Computer Inc.

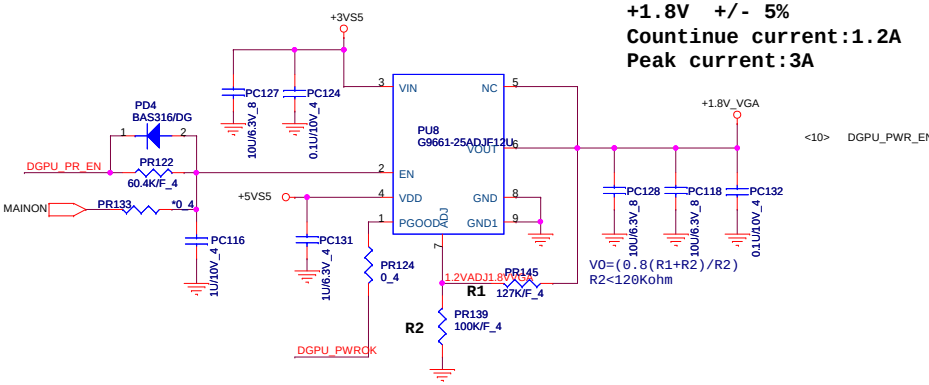
Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

Date: Saturday, September 18, 2010 | Sheet 34 of 39

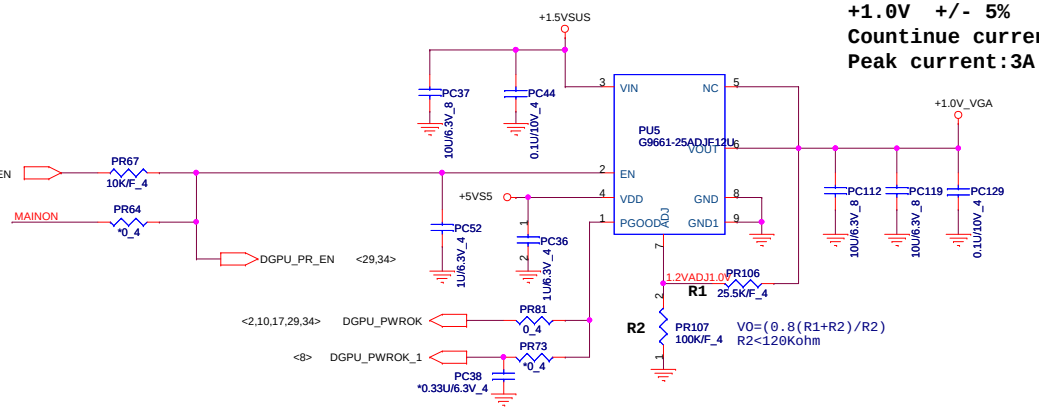


+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

SG & Discrete Only



+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A

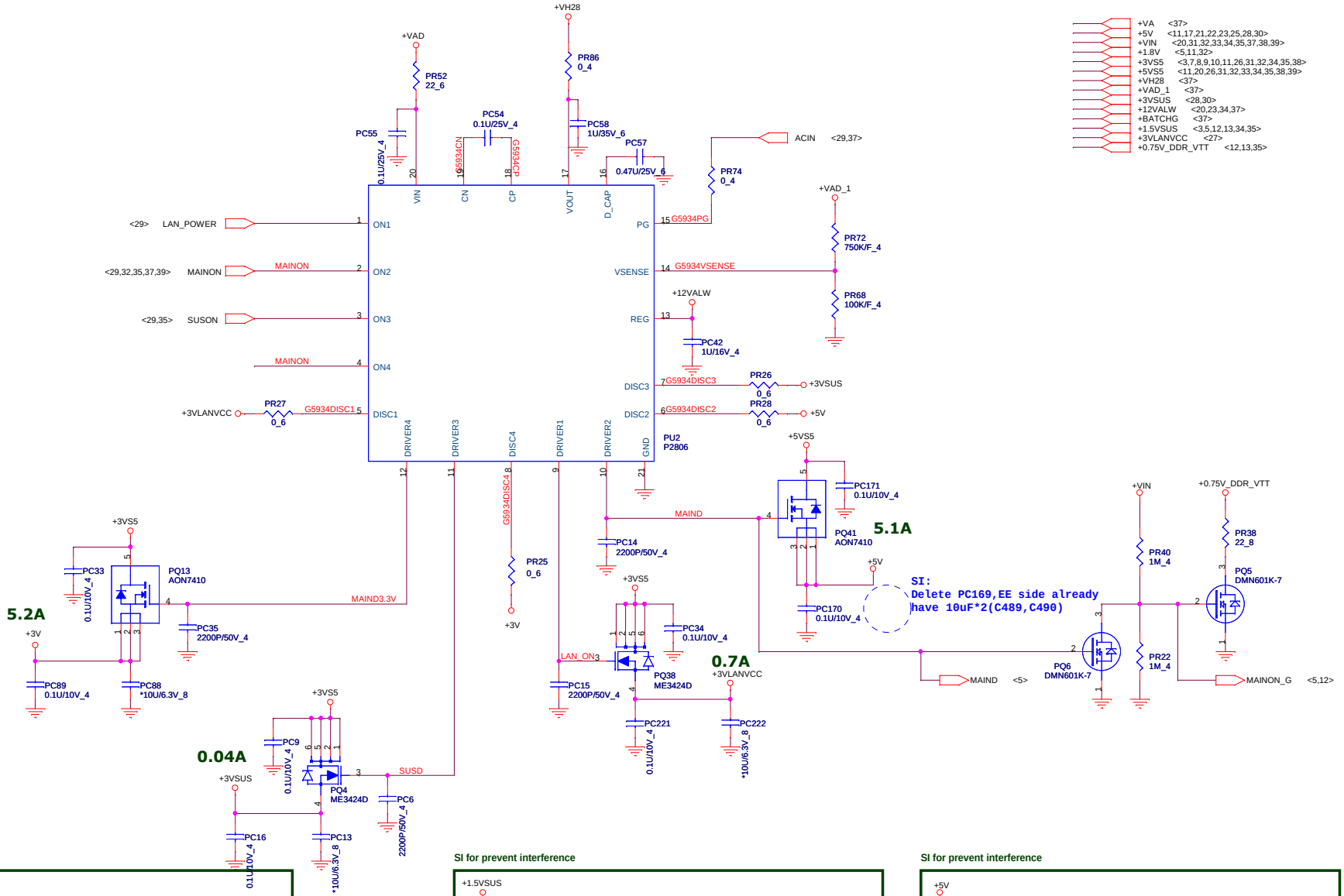


+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A

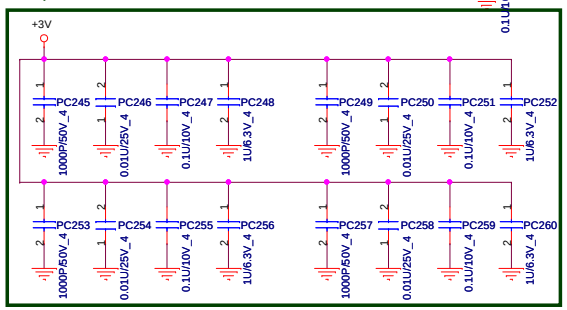
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A
Date: Sunday, September 19, 2010	Sheet 35 of 39	

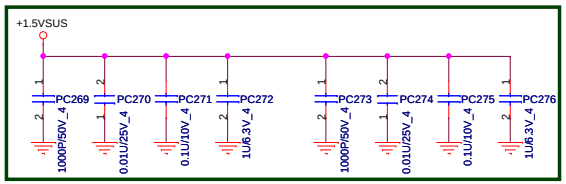
Text Stamp



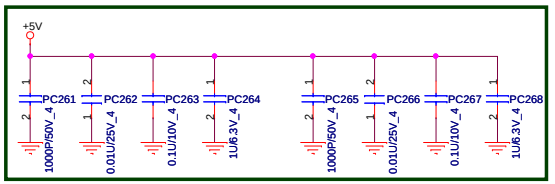
SI for prevent interference



SI for prevent interference



SI for prevent interference



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

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Text Stamp

DC JACK
90W

SI:
M/E modify.

To PWR LED

Do Not add test pad on BATDIS_G signal

Place this ZVS close to
Diode away +VIN

Place this ZVS close to
Far-Far away +VIN

Place this cap
close to EC

Place this cap
close to EC

Place this cap
close to EC

SI:
M/E modify.

PU9
OZ8681

+VA
+VH28 <36>
+VAD_1 <36>
+3VPCU <7,20,28,29,31>
+5VPCU <29,31>
+BATCHG

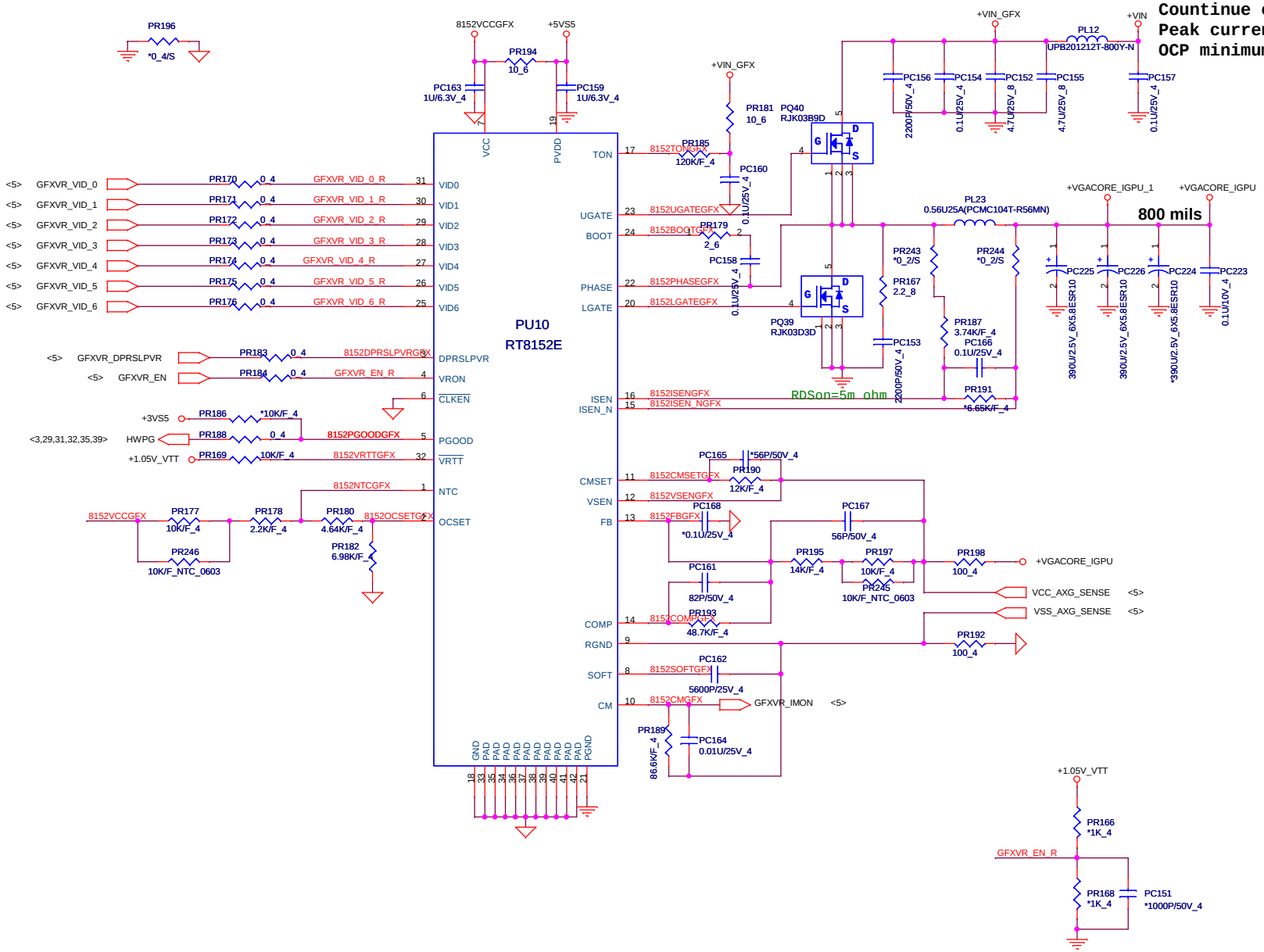
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (OZ8681)	1A

Date: Sunday, September 19, 2010 Sheet 37 of 39

Text Stamp

+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A



Project	
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Size: Custom	Document Number: UMA GPU CORE (RT8152C)
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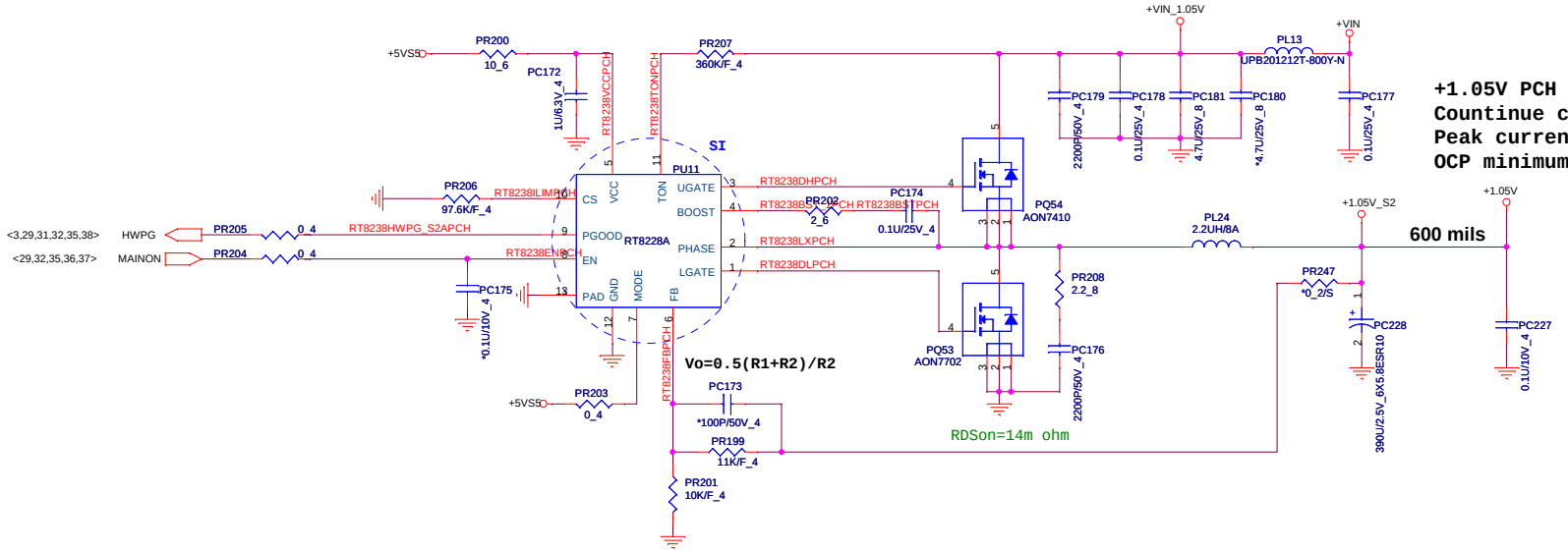

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