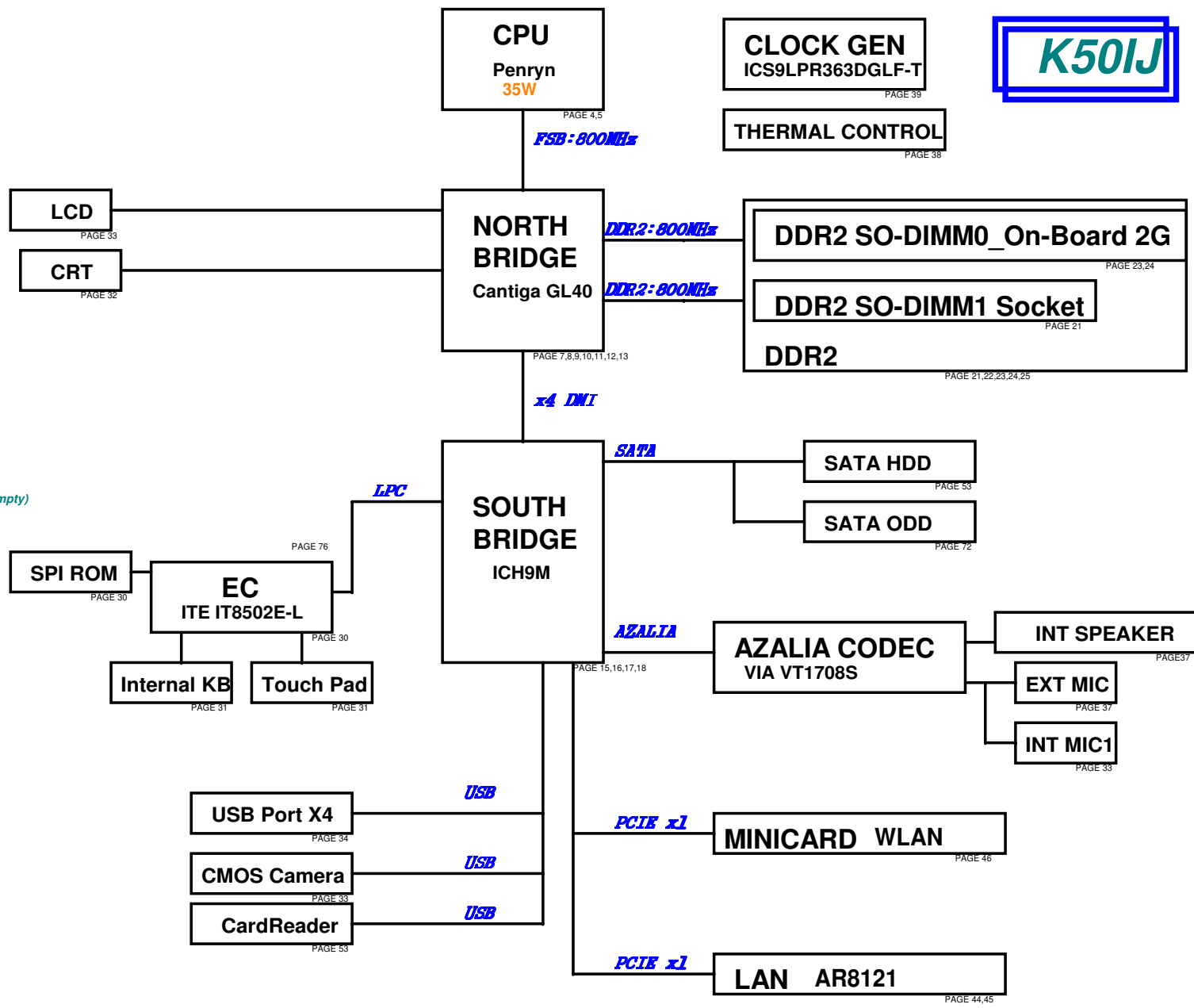
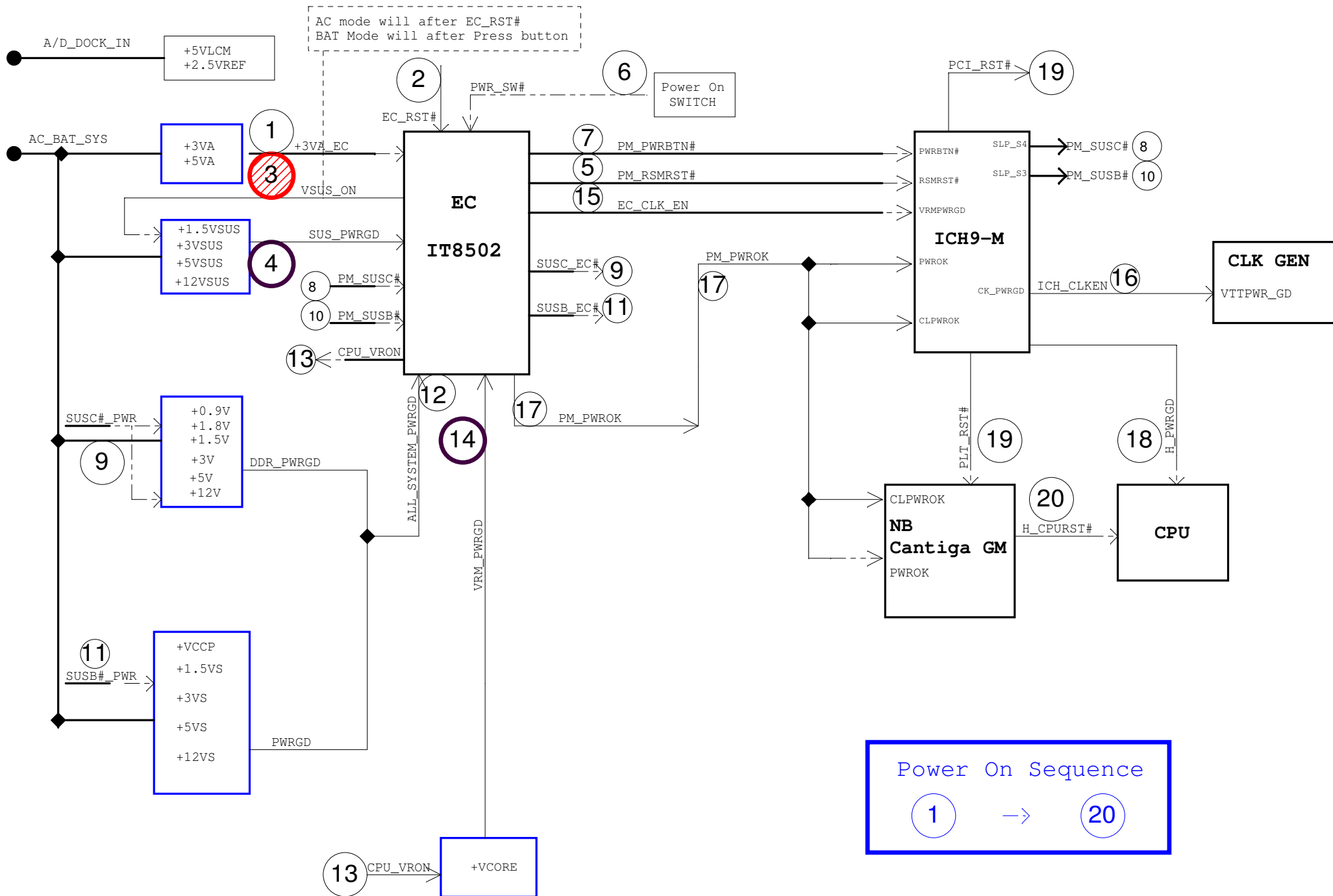


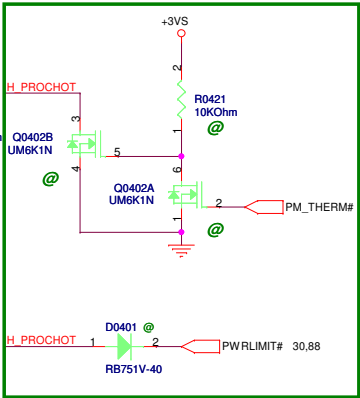
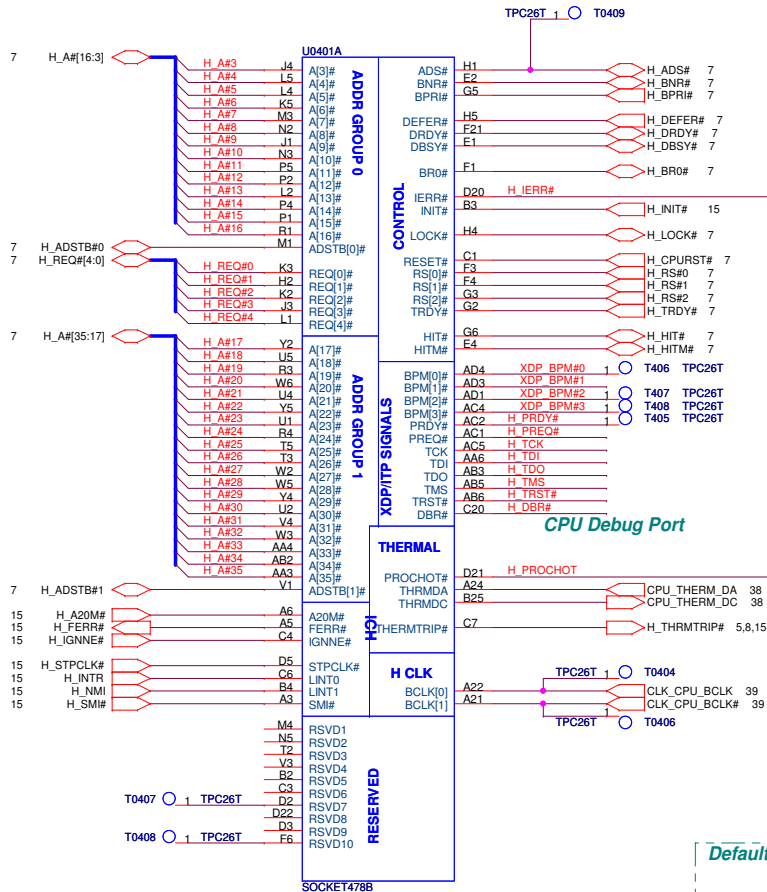
01	Block Diagram	61	*
02	System Setting	62	USB CONN
03	POWER SEQUENCE	63	*
04	CPU-Penryn(HOST)	64	*
05	CPU-Penryn(PWR)	65	*
06	*	66	*
07	Cantiga(HOST)	67	DEBUG CONN
08	Cantiga(DMI & CFG)	68	DC & BAT IN
09	Cantiga(GRAPHIC)	69	*
10	Cantiga(DDR2)	70	*
11	Cantiga(PWR)	71	*
12	Cantiga(PWR2)	72	SATA-HDD & ODD
13	Cantiga(GND)	73	*
14	*	74	HOLE & Spring
15	SB-ICH9M(1)_SATA	75	*
16	SB-ICH9M(2)_PCIE/USB	76	EXPRESS GATE
17	SB-ICH9M(3)_PM/GPIO	77	History
18	SB-ICH9M(PWR)	78	*
19	*	79	*
20	DDR2 SO-DIMM0	80	POWER_VCORE
21	DDR2 SO-DIMM1	81	POWER_SYSTEM
22	DDR2 TERMINATION	82	POWER_I/O_1.5VS & 1.05VS
23	*	83	POWER_I/O_DDR & VTT
24	*	84	POWER_I/O(Empty)
25	*	85	POWER_VGA_CORE&1.1VS(Empty)
26	*	86	POWER_MCH_CORE(Empty)
27	*	87	POWER_CHARGER
28	*	88	POWER_DETECT
29	*	89	POWER_LOAD SWITCH
30	EC_IT8512E-L(1/2)	90	POWER_PROTECT
31	EC_IT8512E-L(2/2)	91	POWER_SIGNAL
32	CRT	92	POWER_FLOWCHART
33	LVDS & INVERTER CONNECTOR	93	POWER_HISTORY
34	BT		
35	*		
36	CONEXANT CX20582		
37	CONEXANT_HP/MIC		
38	THER SENSOR & FAN		
39	CLOCK GEN-ICS9LPR363DGLF-T		
40	*		
41	Switch Button & LED		
42	DISCHARGE		
43	*		
44	PCI-E LAN_RTL8111C		
45	MDC & RJ45+11		
46	Mini card_WLAN+3G		
47	*		
48	*		
49	*		
50	*		
51	*		
52	*		
53	CardReader & SIM CONN & TPM		
54	NEWCARD		
55	*		
56	HDA level shifter		
57	iHDMI		
58	*		
59	*		
60	*		



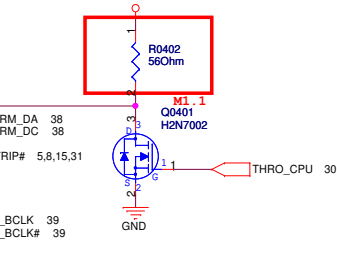


+VCCP +VCCP 5,7,8,9,11,12,15,18,39,42,82

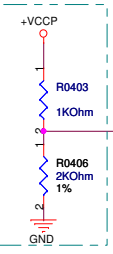
add test point



AGTL+ I/O Voltage Reference



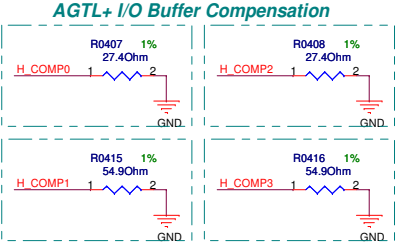
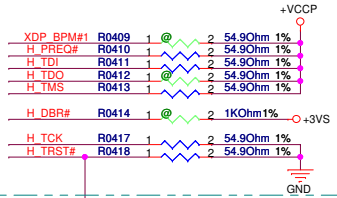
CPU Debug Port



AGTL+ I/O Buffer Compensation

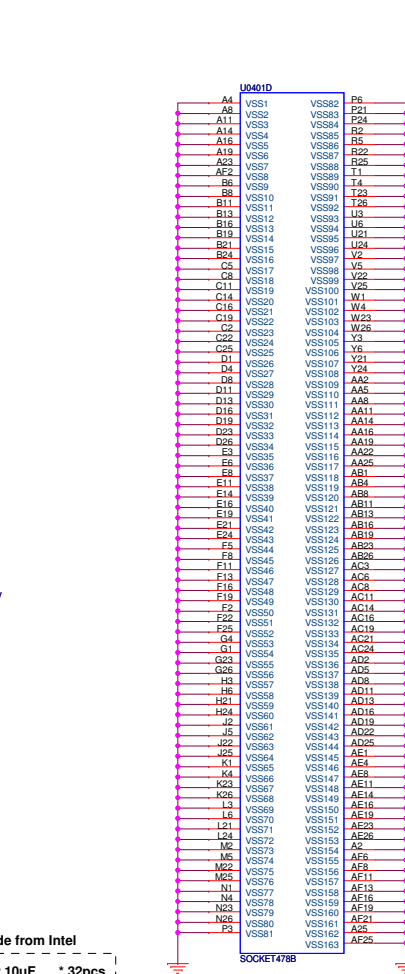
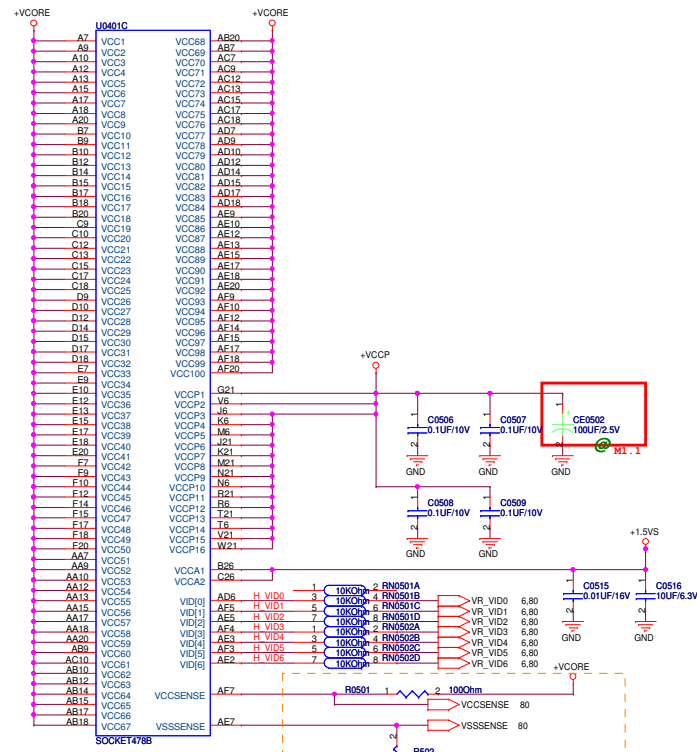
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1066	L	L	L

Default Strapping When Not Used



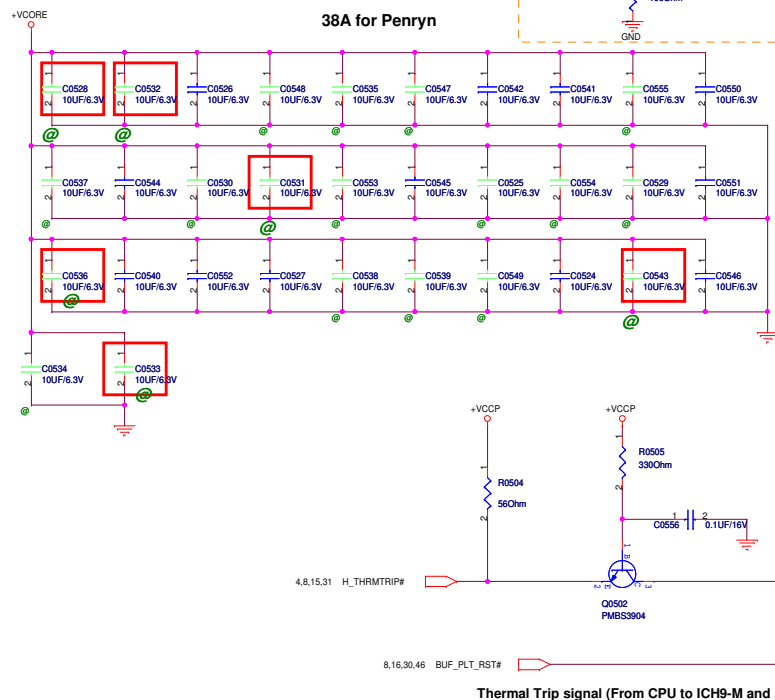
<Variant Name>

ASUS Title : CPU-Penryn(HOST)
 ASUSTek COMPUTER INC. NB1 Engineer: Alex & Bruce
 Size Project Name
 Custom K40IJ/K50IJ Rev 1.1
 Date: Monday, March 09, 2009 Sheet 4 of 96

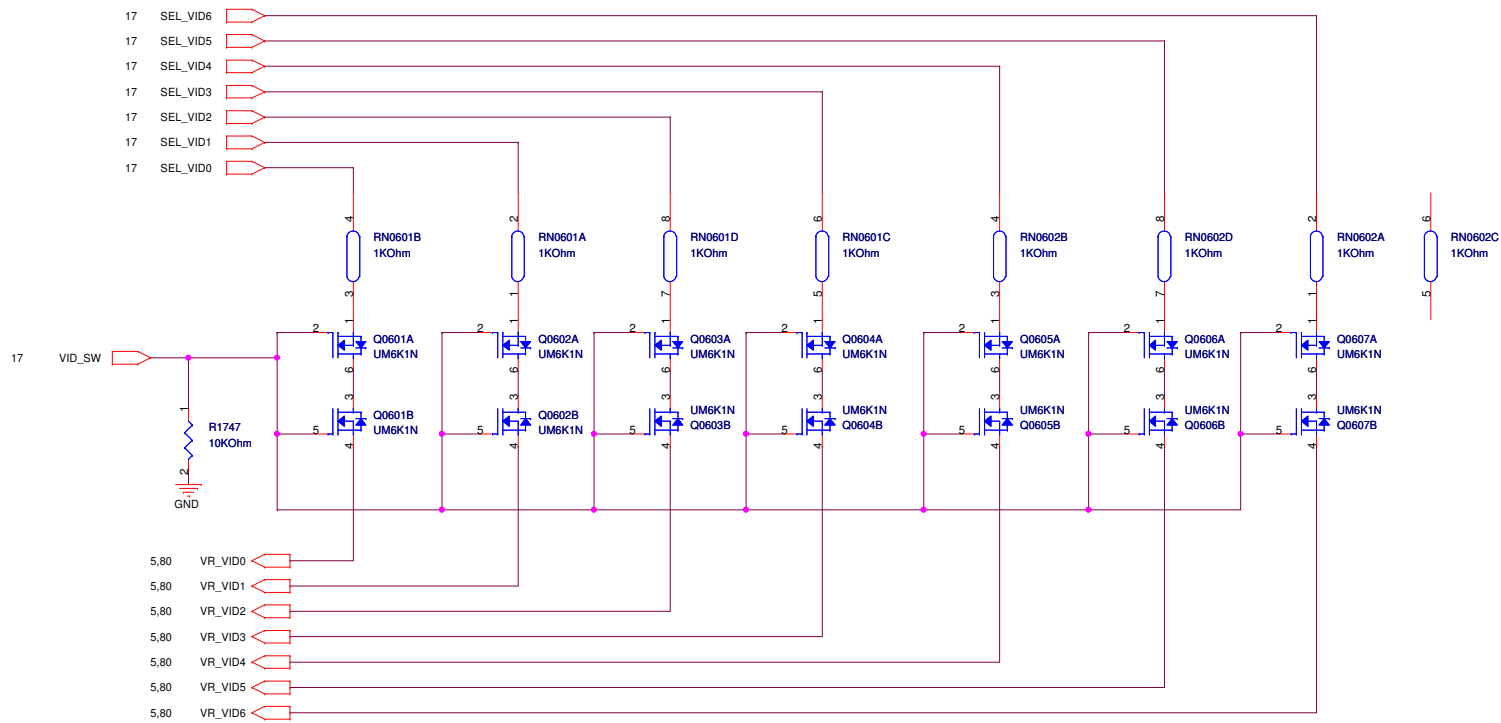


Decoupling guide from Intel

VCCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?



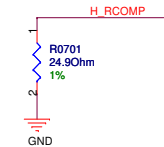
Thermal Trip signal (From CPU to ICH9-M and sequence)



<Variant Name>

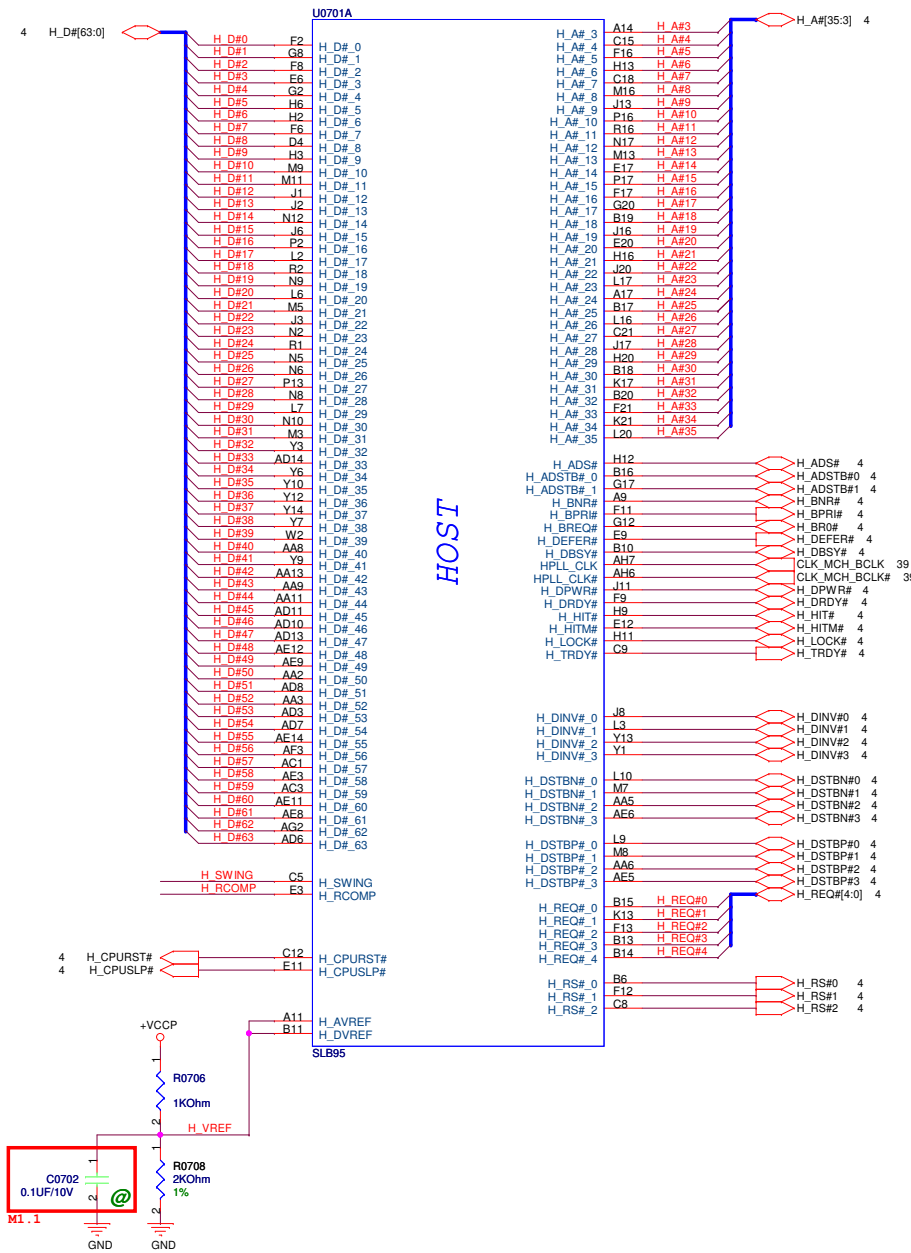
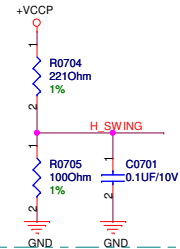
RCOMP

For Calibrating the FSB I/O Buffer

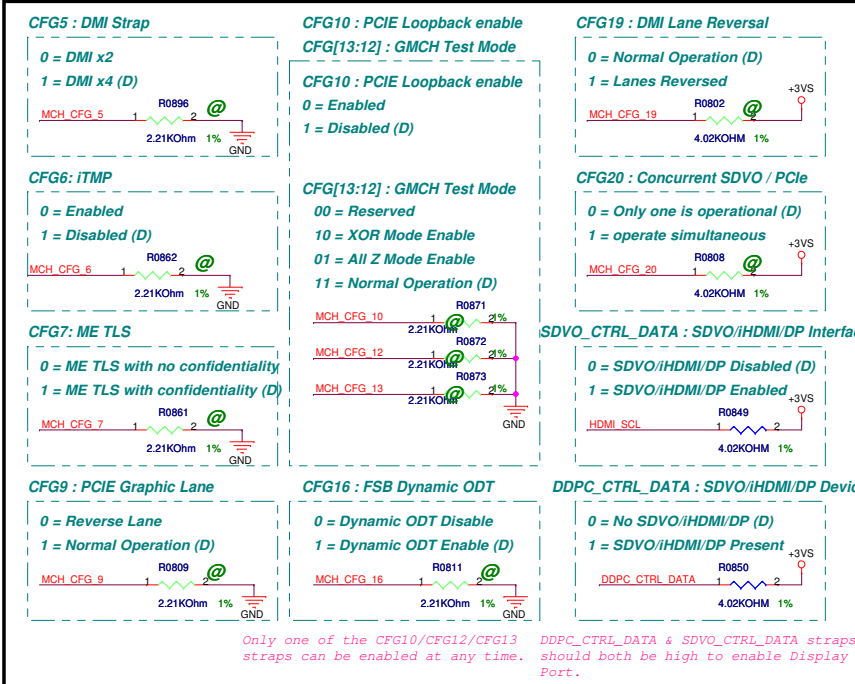


Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



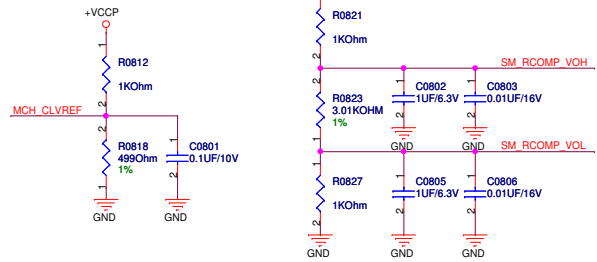
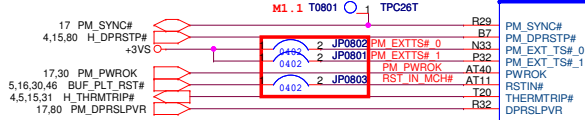
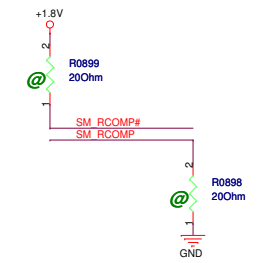
GMCH Strapping



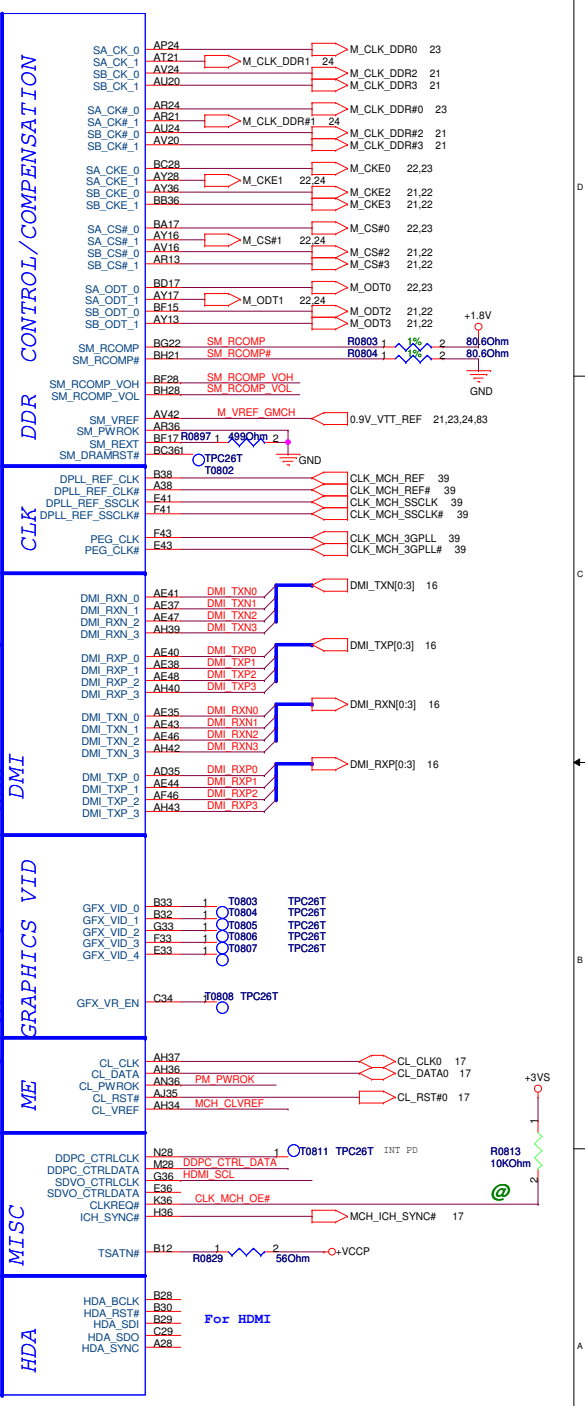
Only one of the CFG10/CFG12/CFG13 DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable Display Port.

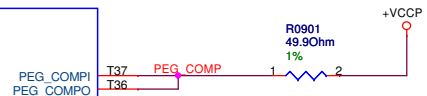
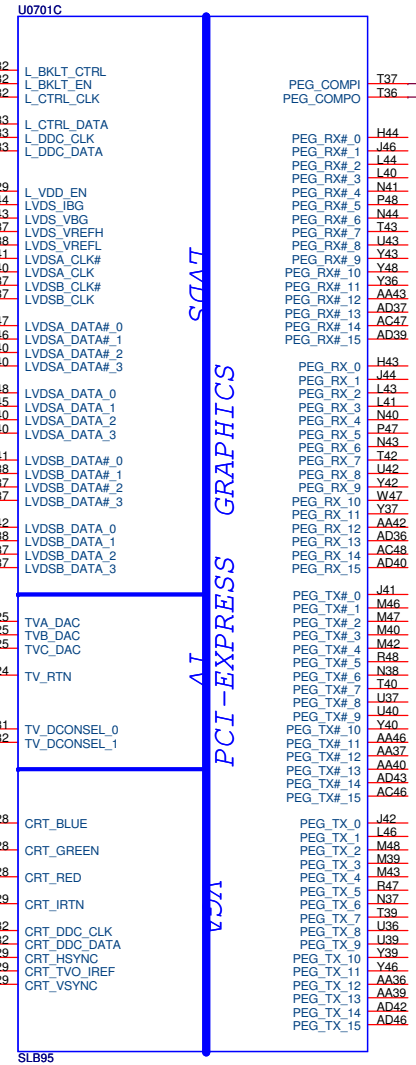
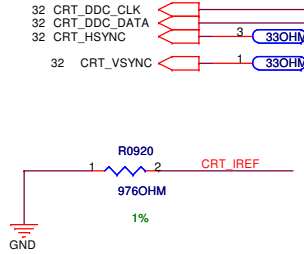
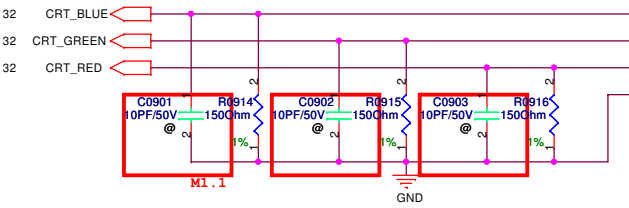
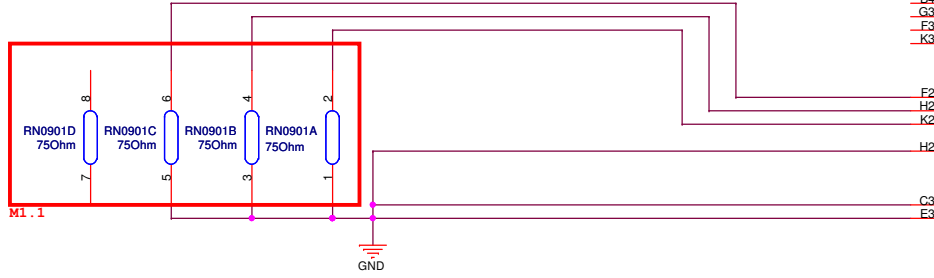
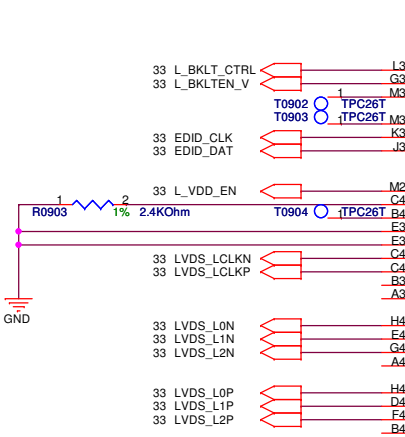
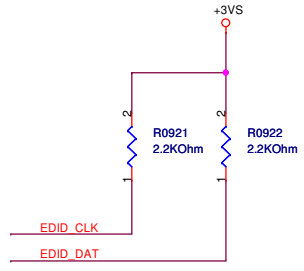
BCLK	FSB	BSEL2	BSEL1	BSEL0
266	1066	L	L	L
166	667	L	H	H
200	800	L	H	L

- MCH_BSEL0
- MCH_BSEL1
- MCH_BSEL2
- MCH_CFG 5
- MCH_CFG 6
- MCH_CFG 7
- MCH_CFG 9
- MCH_CFG 10
- MCH_CFG 12
- MCH_CFG 13
- MCH_CFG 16
- MCH_CFG 19
- MCH_CFG 20



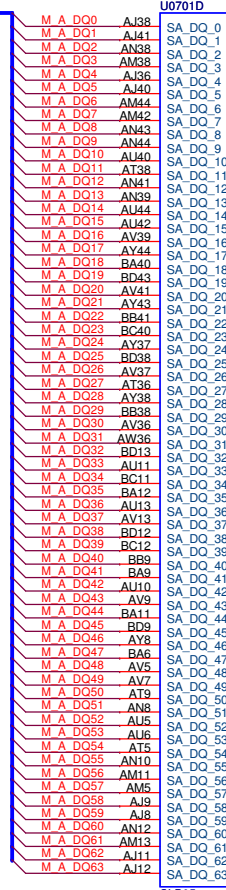
- M36, N36, R333, T33, AH9, AH10, AH12, AH13, K12, AL34, AK34, AN35, AM35, T24
- B31, A16, M1, AY21
- A47, BG23, BF23, BH18, BF18, RSV11, VSS, RSV13, RSV14, RSV16, RSV17, RSV18, RSV19
- NC, BG23, BF23, BH18, BF18
- CFG_0 to CFG_20
- PM_SYNC#, H_DPRSTP#, PM_EXT_TSH_0, PM_EXT_TSH_1, PWROK, RST_IN_MCH#, THERMTRIP#, DPRSLPVR
- NC_1 to NC_25
- HDA_BCLK, HDA_RST#, HDA_SD#, HDA_SDC, HDA_SYNC



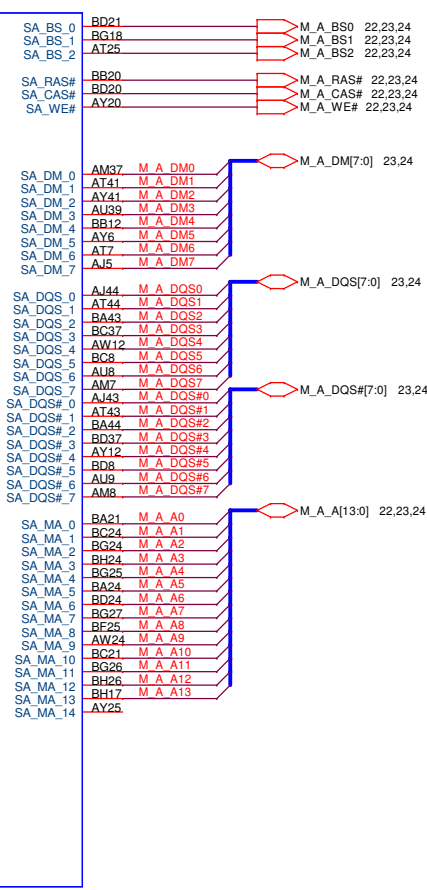


- PEG_COMPI T37
- PEG_COMPO T36
- PEG_RX#_0 H44
- PEG_RX#_1 J46
- PEG_RX#_2 L44
- PEG_RX#_3 L40
- PEG_RX#_4 N41
- PEG_RX#_5 P48
- PEG_RX#_6 N44
- PEG_RX#_7 T43
- PEG_RX#_8 U43
- PEG_RX#_9 Y43
- PEG_RX#_10 Y48
- PEG_RX#_11 Y36
- PEG_RX#_12 AA43
- PEG_RX#_13 AD37
- PEG_RX#_14 AC47
- PEG_RX#_15 AD39
- PEG_RX_0 H43
- PEG_RX_1 J44
- PEG_RX_2 L43
- PEG_RX_3 L41
- PEG_RX_4 N40
- PEG_RX_5 P47
- PEG_RX_6 N43
- PEG_RX_7 T42
- PEG_RX_8 U42
- PEG_RX_9 Y42
- PEG_RX_10 W47
- PEG_RX_11 Y37
- PEG_RX_12 AA42
- PEG_RX_13 AD38
- PEG_RX_14 AC48
- PEG_RX_15 AD40
- PEG_TX#_0 J41
- PEG_TX#_1 M46
- PEG_TX#_2 M47
- PEG_TX#_3 M40
- PEG_TX#_4 M42
- PEG_TX#_5 R48
- PEG_TX#_6 N38
- PEG_TX#_7 T40
- PEG_TX#_8 U37
- PEG_TX#_9 U40
- PEG_TX#_10 Y40
- PEG_TX#_11 AA46
- PEG_TX#_12 AA37
- PEG_TX#_13 AA40
- PEG_TX#_14 AD43
- PEG_TX#_15 AC46
- PEG_TX_0 J42
- PEG_TX_1 L46
- PEG_TX_2 M48
- PEG_TX_3 M39
- PEG_TX_4 M43
- PEG_TX_5 R47
- PEG_TX_6 N37
- PEG_TX_7 U36
- PEG_TX_8 U39
- PEG_TX_9 Y39
- PEG_TX_10 Y46
- PEG_TX_11 AA36
- PEG_TX_12 AA39
- PEG_TX_13 AD42
- PEG_TX_14 AD46
- PEG_TX_15

23,24 M_A_DQ[63:0]

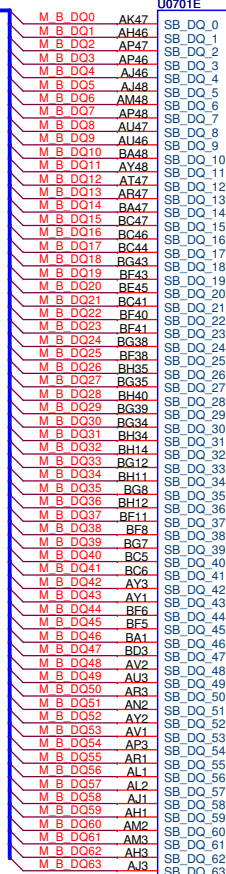


DDR SYSTEM MEMORY A

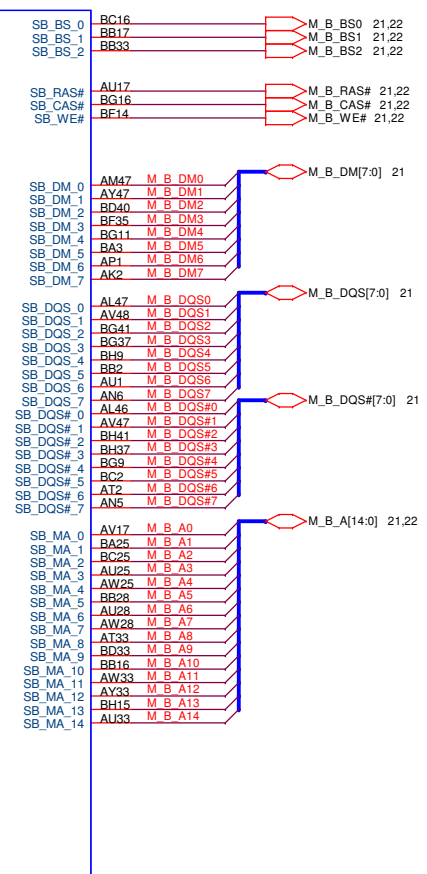


SLB95

21 M_B_DQ[63:0]



DDR SYSTEM MEMORY B



SLB95

<Variant Name>

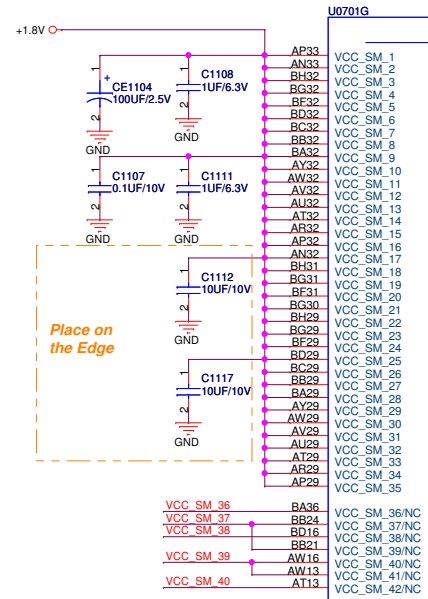
Title : NB-Cantiga(DDR2)

ASUSTeK COMPUTER INC. NB1 Engineer: N/A

Size	Project Name	Rev
Custom	K401J/K501J	1.1

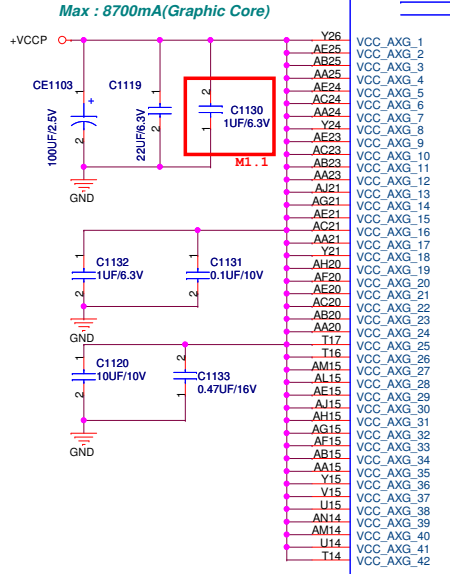
Date: Monday, March 09, 2009 Sheet 10 of 96

Max : 3000mA(DDR2)



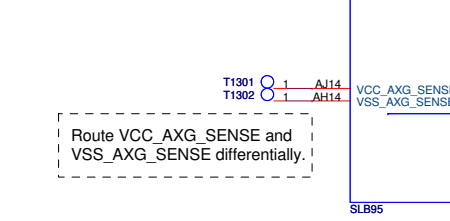
VCC SM POWER

VCC GFX NCTF



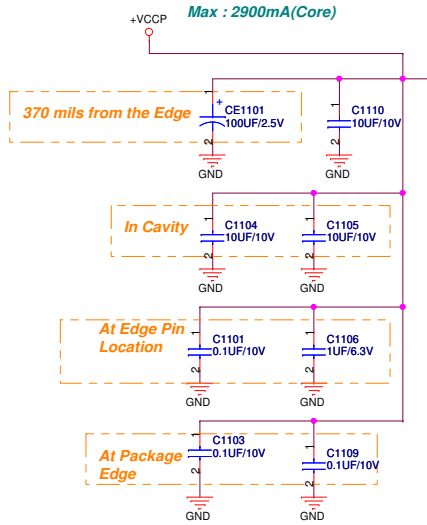
VCC GFX

VCC SM LF



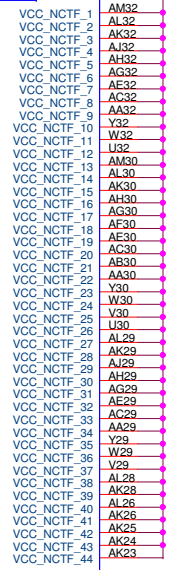
Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.

(Graph Core)

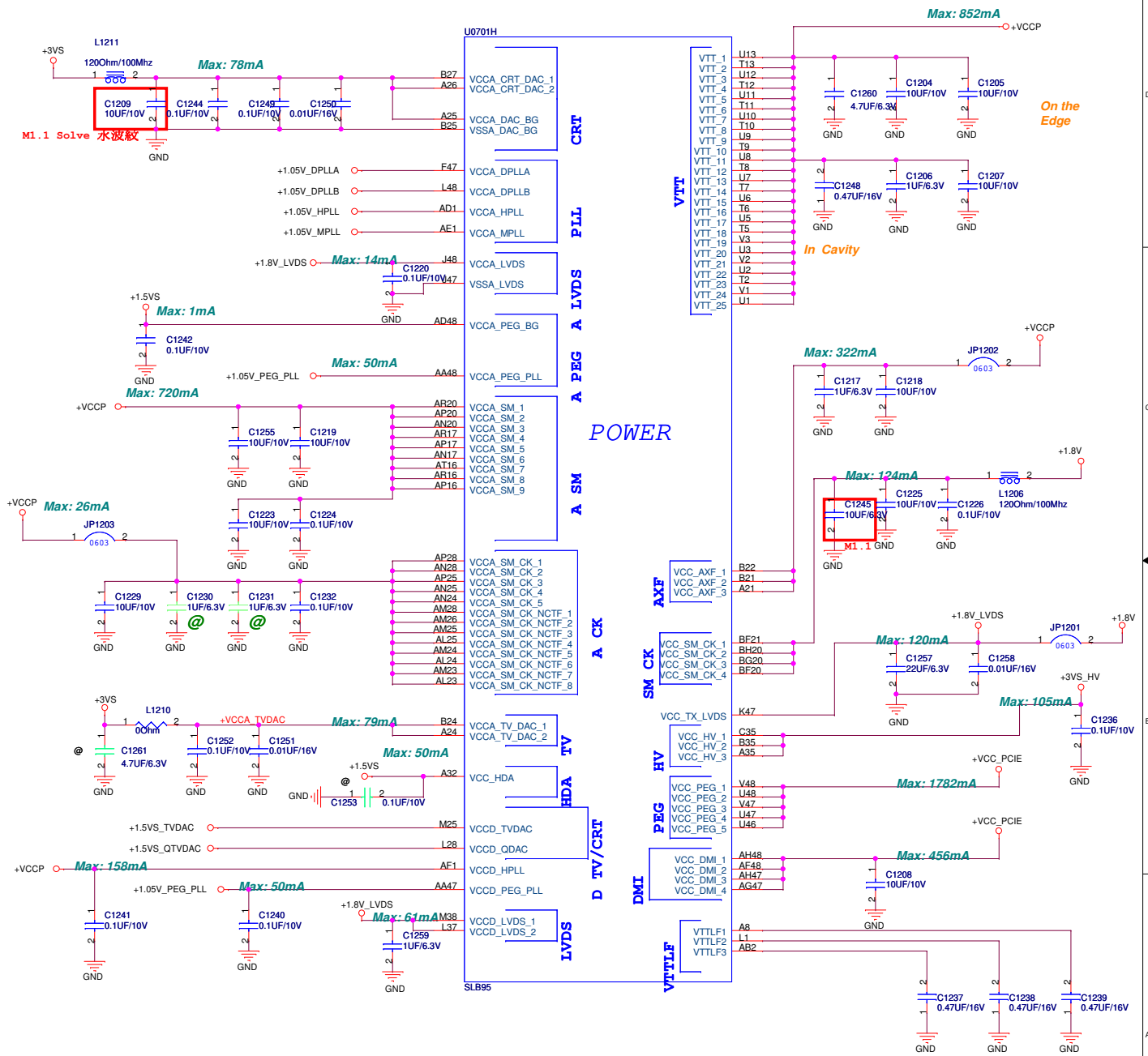
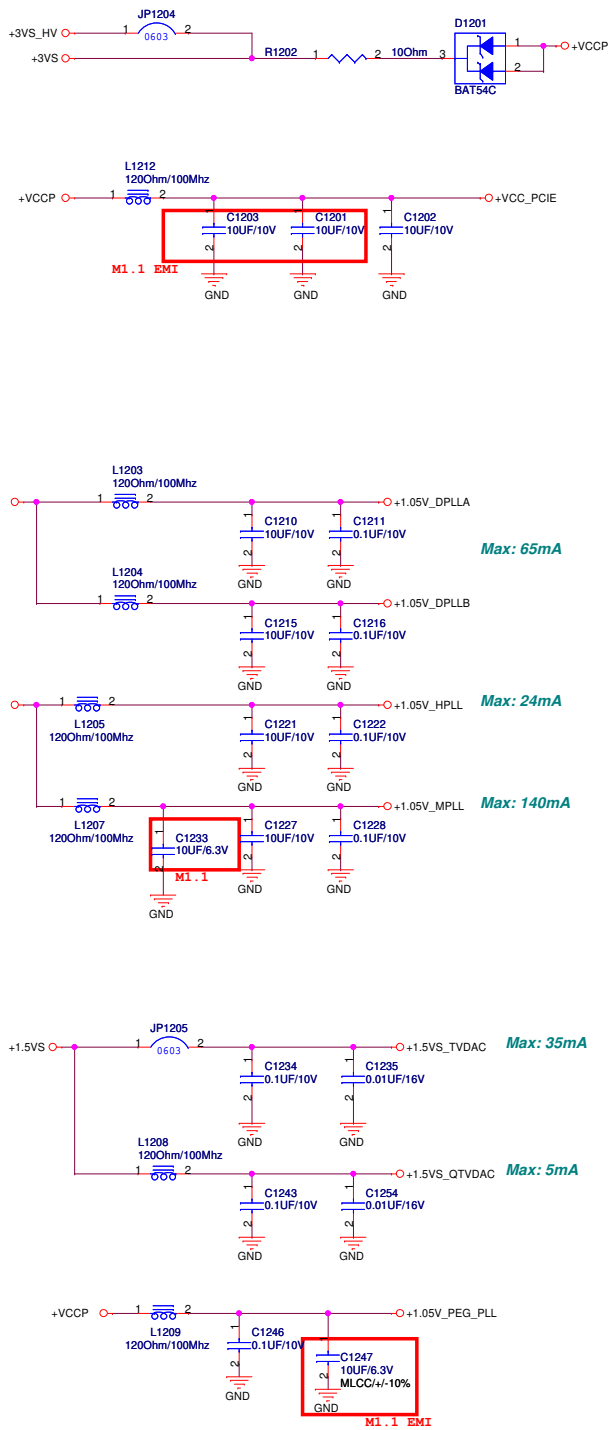


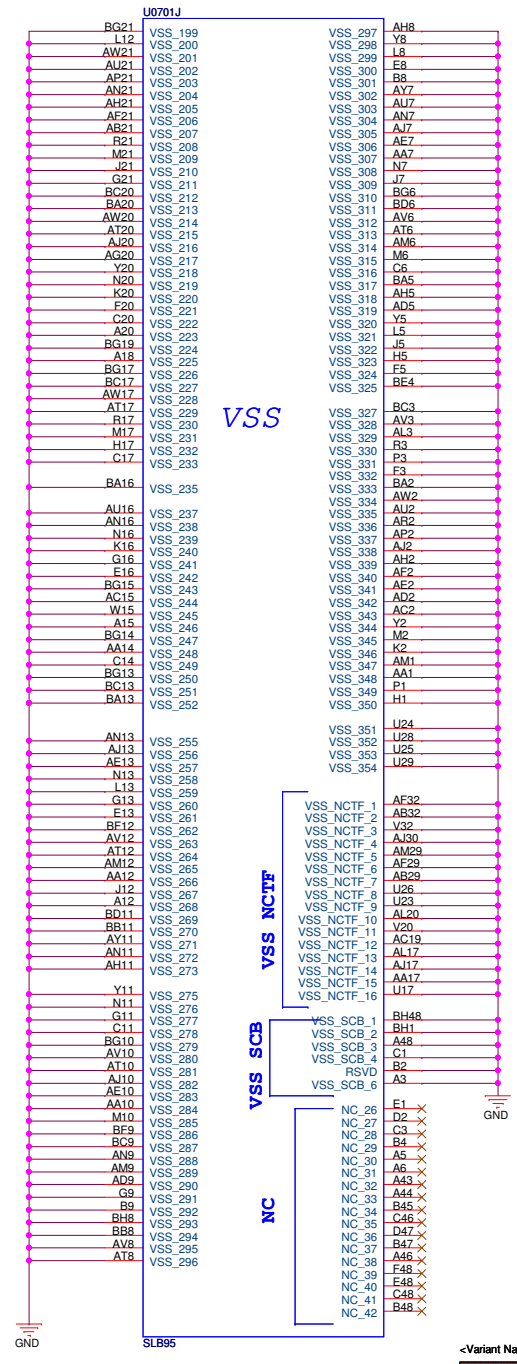
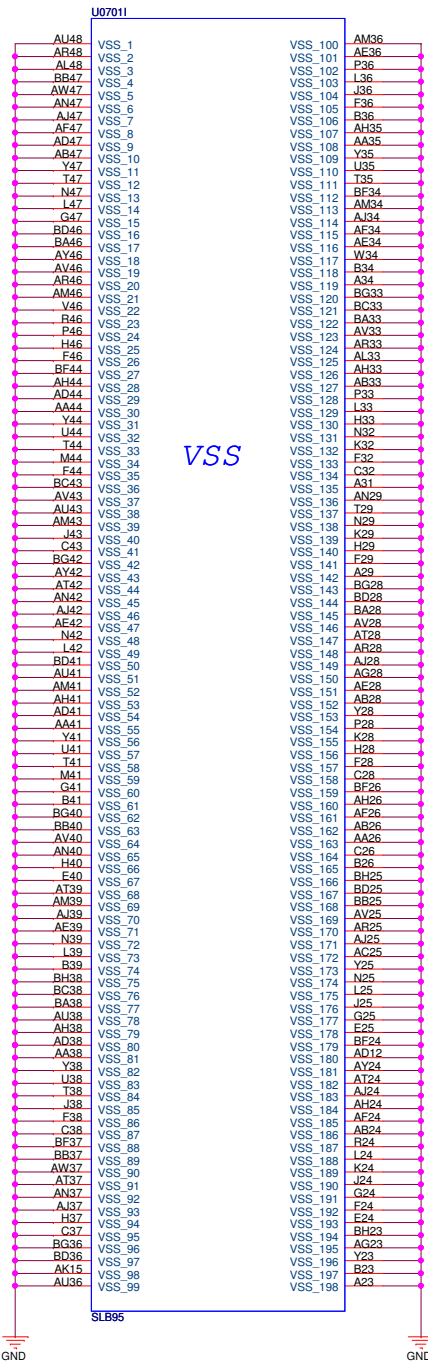
VCC CORE POWER

VCC NCTF



<Variant Name>





5

4

3

2

1

D

D

C

C


B

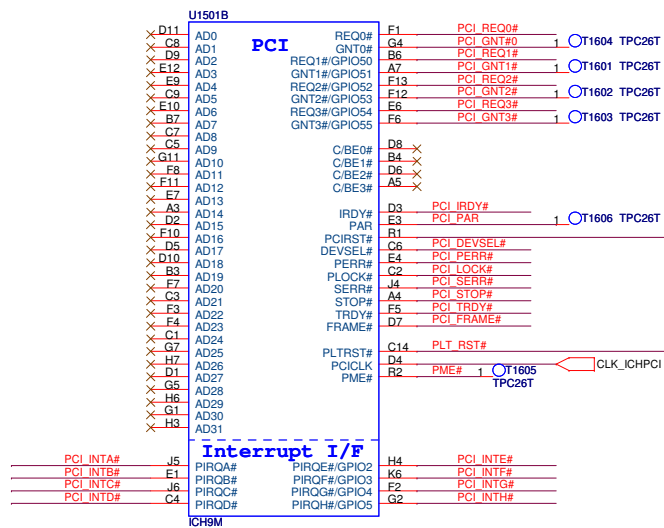
B

A

A

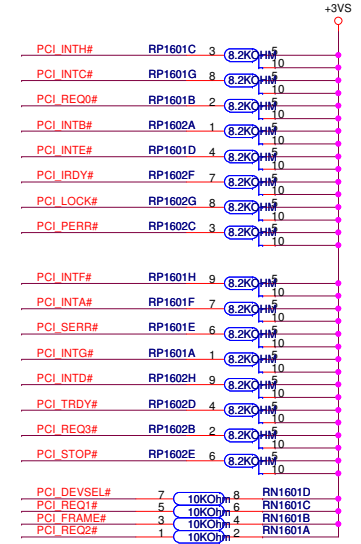
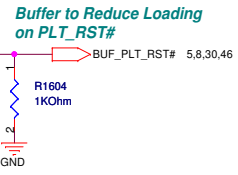
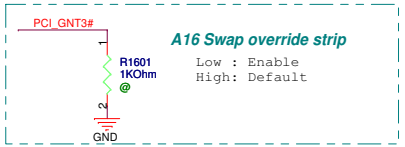
<Variant Name>

		Title : Schematic page name
ASUSTeK COMPUTER INC		Engineer: N/A
Size	Project Name	Rev
C	K40LJ/K50LJ	1.1
Date: Monday, March 09, 2009		Sheet 14 of 95

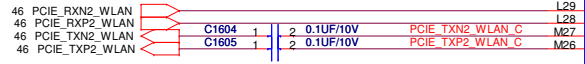


ICH8 Boot BIOS Select

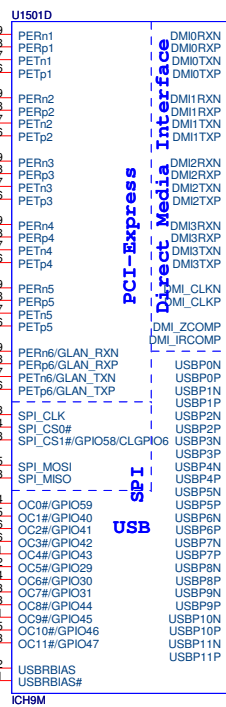
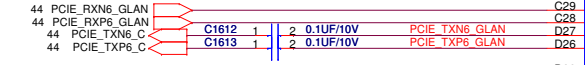
	GNT#0	CS#1
LPC	H	H
PCI	H	L
SPI	L	H



WLAN

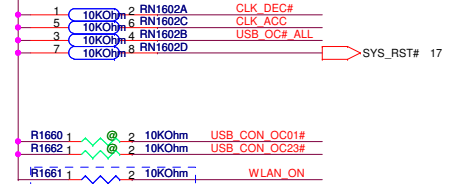


GLAN



USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	USB Conn.(M/B)
USB 3	USB Conn.(M/B)
USB 4	Reverse
USB 5	Reverse
USB 6	Card Reader
USB 7	WLAN
USB 8	CMOS Camera(D/B)
USB 9	Reverse
USB 10	Reverse
USB 11	Reverse

M1.1 For EMI CMOS form Port 4 change to Port 8



When supporting CLK GEN Turbo PIN, un-mount R1661.

ASUS Title : SB-ICH9M(2)

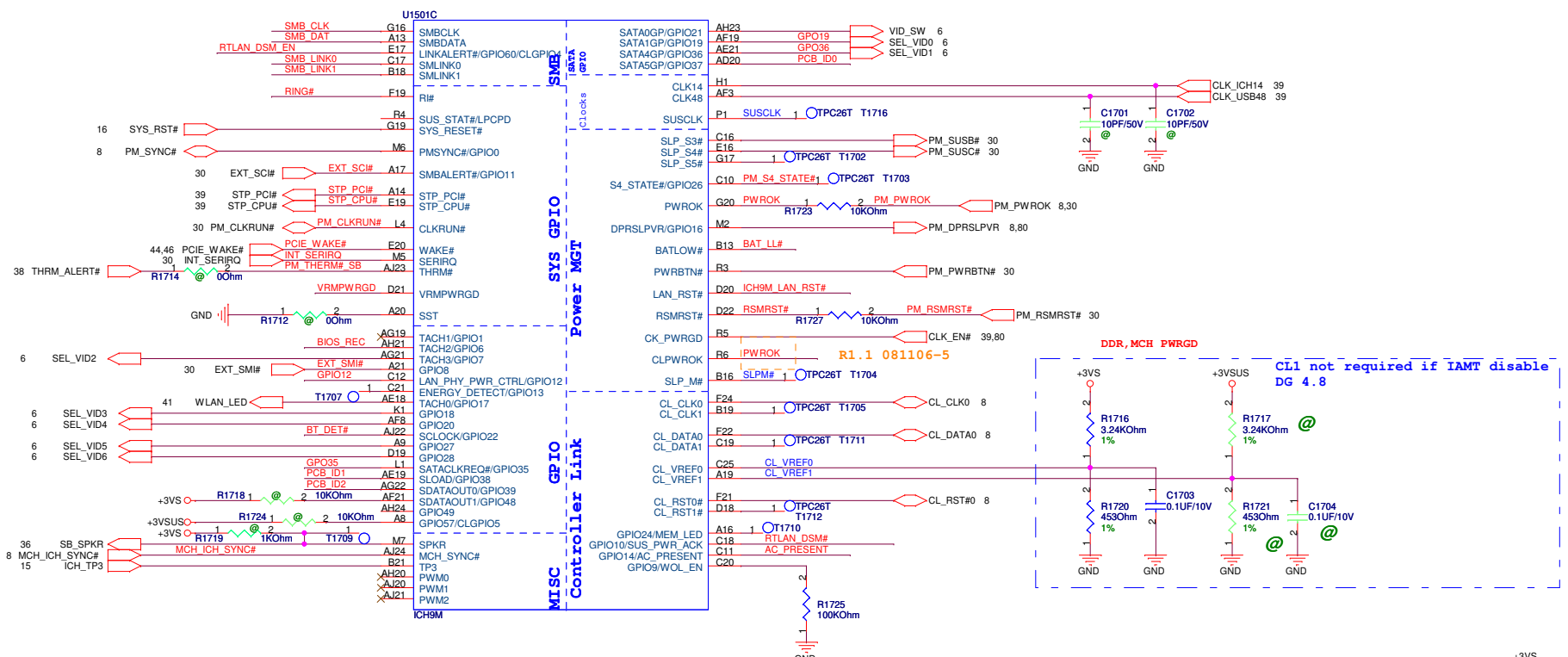
ASUSTek COMPUTER INC. NBI Engineer: N/A

Size Project Name

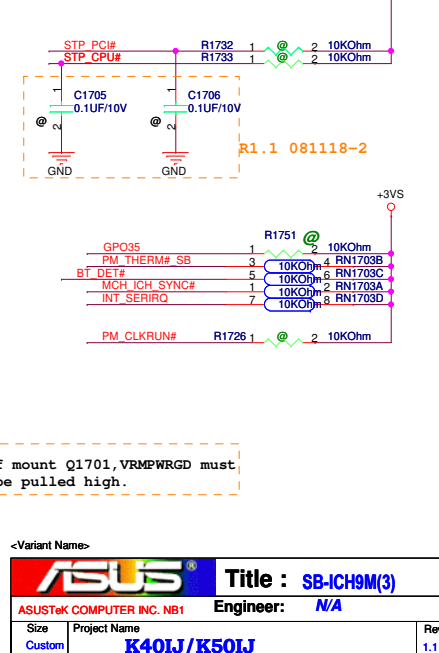
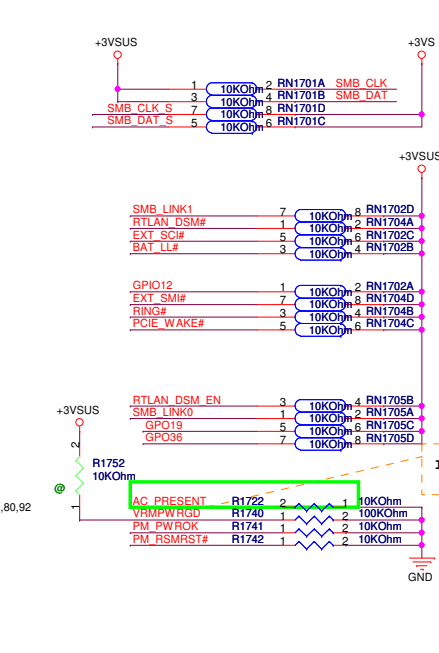
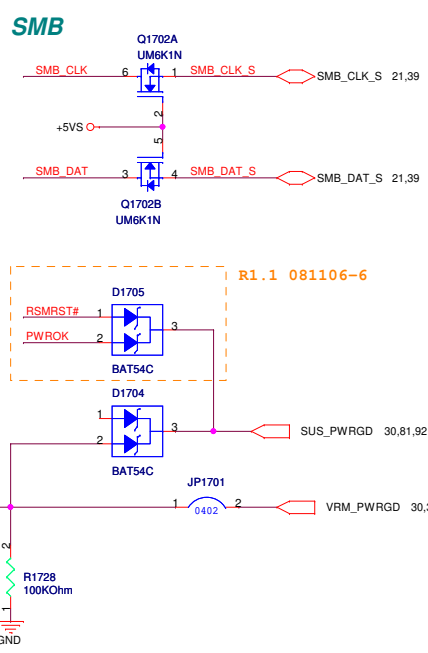
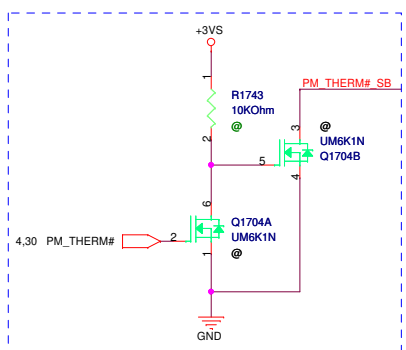
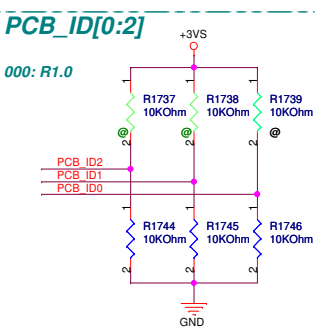
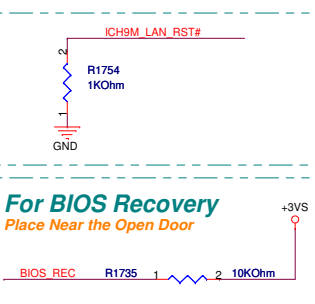
Custom K40J/K50J

Date: Monday, March 09, 2009 Sheet 16 of 96

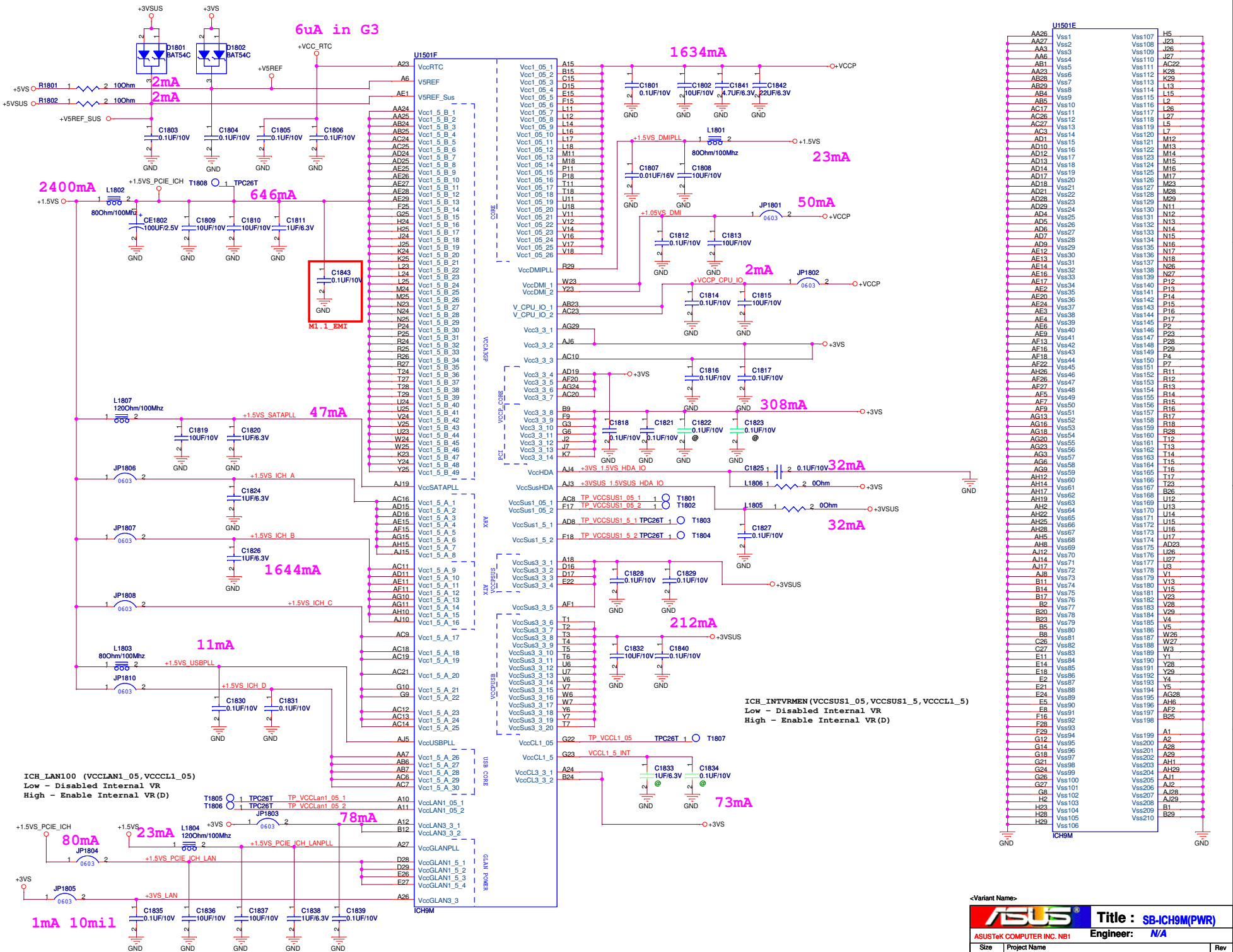
Rev 1.1



No Reboot Strap
 Low = Default
 High = No Reboot



If mount Q1701, VRMPWRGD must be pulled high.



AA26	Vss1	Vss107	H5
AA27	Vss2	Vss108	J6
AA3	Vss3	Vss109	J26
AA6	Vss4	Vss110	J27
AB1	Vss5	Vss111	AC22
AB2	Vss6	Vss112	K29
AB23	Vss7	Vss113	L13
AB29	Vss8	Vss114	L2
AB4	Vss9	Vss115	L15
AB5	Vss10	Vss116	L26
AC17	Vss11	Vss117	L27
AC26	Vss12	Vss118	L5
AC27	Vss13	Vss119	L7
AC3	Vss14	Vss120	M12
AD1	Vss15	Vss121	M13
AD10	Vss16	Vss122	M14
AD12	Vss17	Vss123	M15
AD13	Vss18	Vss124	M16
AD14	Vss19	Vss125	M17
AD17	Vss20	Vss126	M28
AD18	Vss21	Vss127	M23
AD21	Vss22	Vss128	M29
AD22	Vss23	Vss129	N11
AD29	Vss24	Vss130	N11
AD4	Vss25	Vss131	N12
AD5	Vss26	Vss132	N13
AD6	Vss27	Vss133	N14
AD7	Vss28	Vss134	N15
AD9	Vss29	Vss135	N16
AE12	Vss30	Vss136	N17
AE13	Vss31	Vss137	N18
AE14	Vss32	Vss138	N26
AE16	Vss33	Vss139	N27
AE17	Vss34	Vss140	P13
AE20	Vss35	Vss141	P14
AE24	Vss36	Vss142	P15
AE3	Vss37	Vss143	P16
AE4	Vss38	Vss144	P17
AE6	Vss39	Vss145	P2
AE9	Vss40	Vss146	P28
AE11	Vss41	Vss147	P23
AE16	Vss42	Vss148	P29
AE18	Vss43	Vss149	P4
AF18	Vss44	Vss150	P7
AF22	Vss45	Vss151	R11
AH26	Vss46	Vss152	R12
AF26	Vss47	Vss153	R13
AF27	Vss48	Vss154	R14
AE5	Vss49	Vss155	R15
AE7	Vss50	Vss156	R16
AF9	Vss51	Vss157	R17
AG13	Vss52	Vss158	R18
AG16	Vss53	Vss159	R28
AG18	Vss54	Vss160	T12
AG20	Vss55	Vss161	T13
AG23	Vss56	Vss162	T15
AG3	Vss57	Vss163	T14
AG6	Vss58	Vss164	T16
AG9	Vss59	Vss165	T17
AH12	Vss60	Vss166	T23
AH14	Vss61	Vss167	B26
AH17	Vss62	Vss168	L12
AH19	Vss63	Vss169	L13
AH2	Vss64	Vss170	V13
AH22	Vss65	Vss171	L14
AH25	Vss66	Vss172	L15
AH28	Vss67	Vss173	L16
AH5	Vss68	Vss174	L17
AH8	Vss69	Vss175	AD23
AH12	Vss70	Vss176	L27
AH14	Vss71	Vss177	U3
AH17	Vss72	Vss178	V13
AH8	Vss73	Vss179	V15
B11	Vss74	Vss180	V15
B17	Vss75	Vss181	V23
B2	Vss76	Vss182	V28
B2	Vss77	Vss183	V29
B23	Vss78	Vss184	V4
B5	Vss79	Vss185	V5
B5	Vss80	Vss186	W26
B8	Vss81	Vss187	W3
C26	Vss82	Vss188	W27
C27	Vss83	Vss189	W3
E11	Vss84	Vss190	Y1
E18	Vss85	Vss191	Y28
E2	Vss86	Vss192	V4
E21	Vss87	Vss193	Y5
E2	Vss88	Vss194	Y5
E24	Vss89	Vss195	AC28
E5	Vss90	Vss196	AH6
EA	Vss91	Vss197	AF2
F16	Vss92	Vss198	B25
F28	Vss93	Vss199	A1
F29	Vss94	Vss200	A2
G12	Vss95	Vss201	A28
G14	Vss96	Vss202	A29
G21	Vss97	Vss203	AH1
G24	Vss98	Vss204	AH20
G26	Vss99	Vss205	A11
G27	Vss100	Vss206	A12
G3	Vss101	Vss207	A28
H2	Vss102	Vss208	B1
H23	Vss103	Vss209	B1
H28	Vss104	Vss210	B29
H29	Vss105	Vss210	
H29	Vss106	Vss210	

ICH_INTVRMEN (VCCSUS1_05, VCCSUS1_5, VCCCL1_5)
 Low - Disabled Internal VR
 High - Enable Internal VR (D)

<Variant Name>

ASUS		Title : SB-ICH9M(PWR)
ASUSTek COMPUTER INC. NB1		Engineer: N/A
Size	Project Name	Rev
Custom	K40LI/K50IJ	1.1
Date: Monday, March 08, 2009	Sheet	18 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	19 of 96

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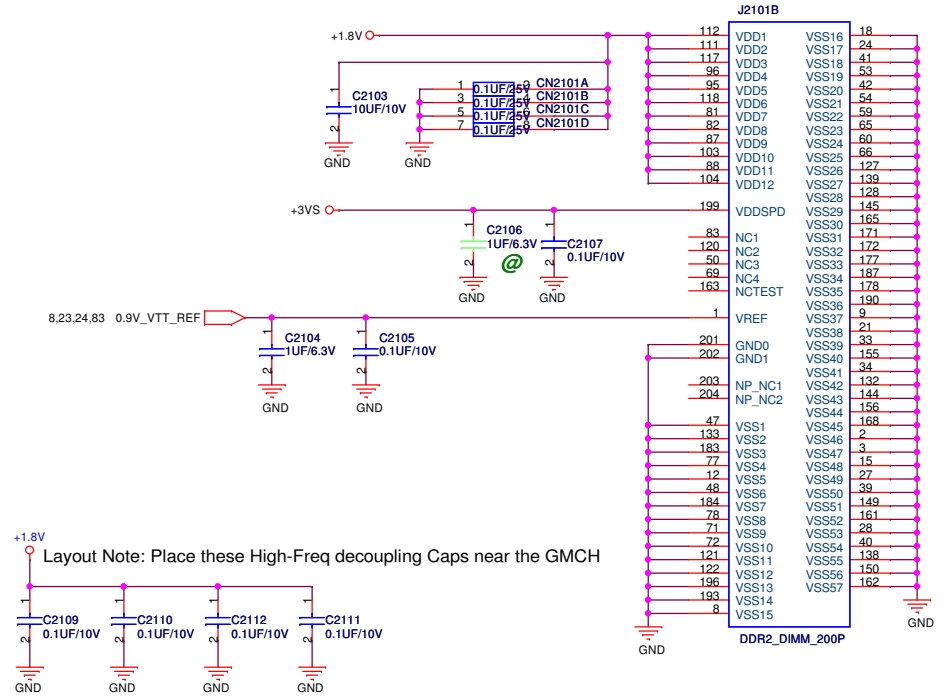
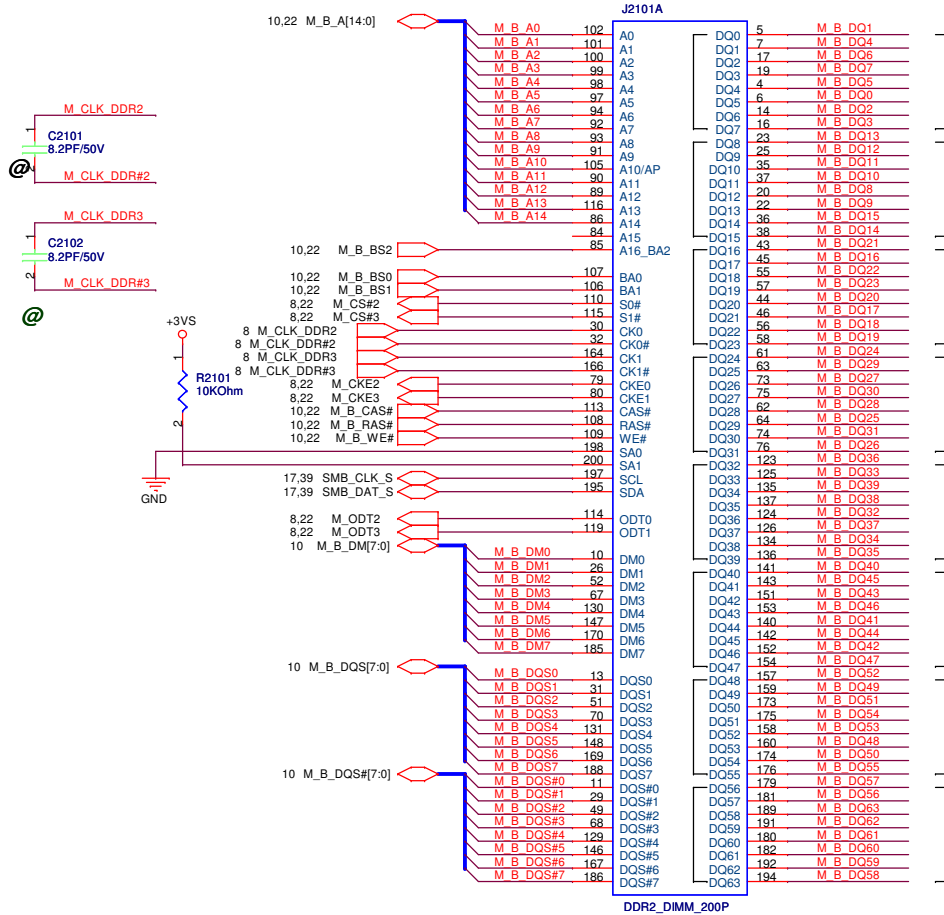


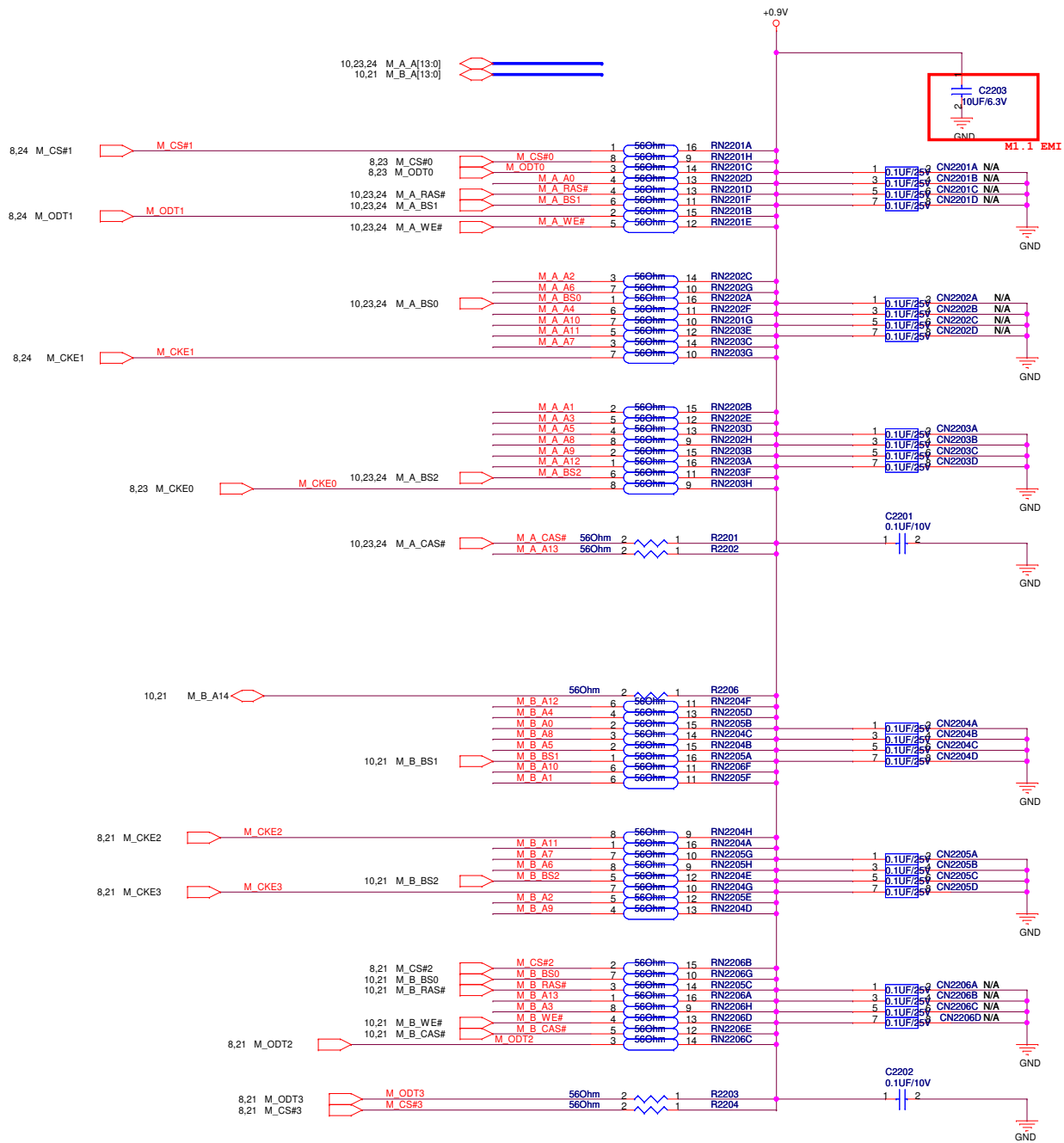
<Variant Name>

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ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size	Project Name	Rev
A3	K40IJ/K50IJ	1.1
Date: Monday, March 09, 2009		Sheet 20 of 96

DDR2 200P H=9.2mm (Reverse Type)

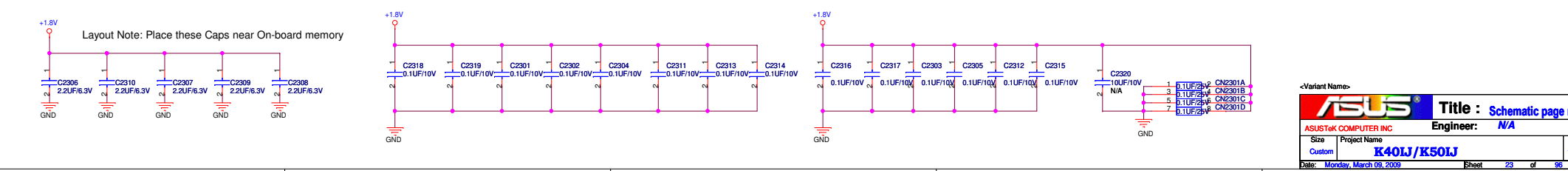
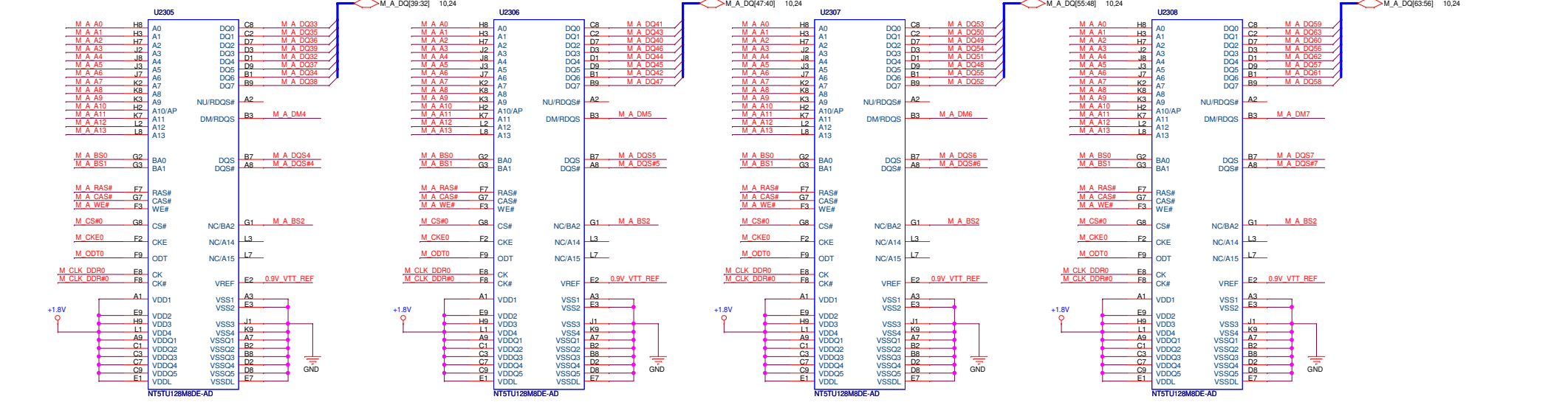
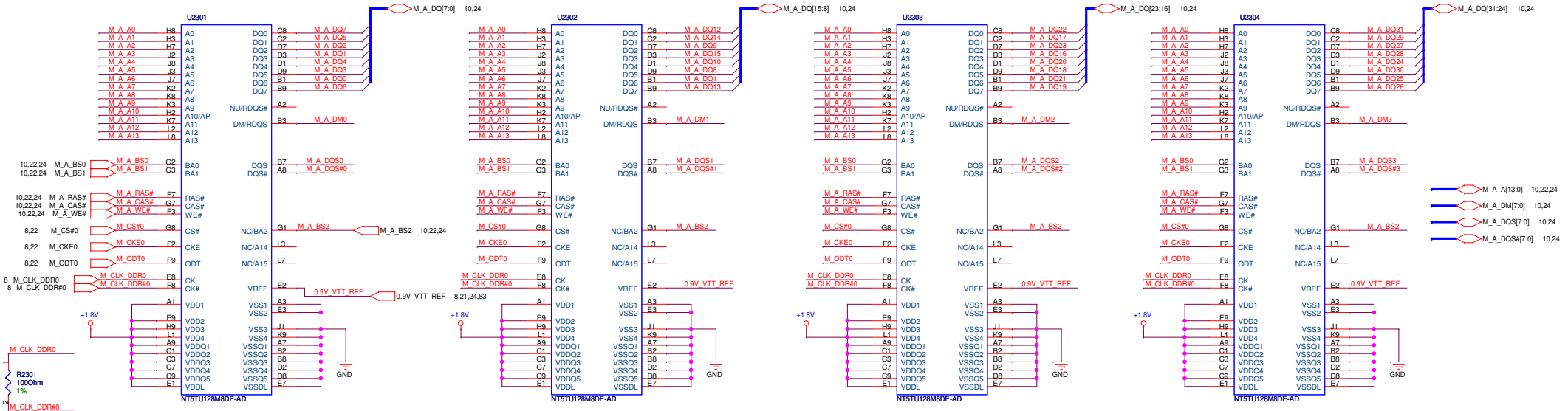
M_B_DQ[63:0] 10



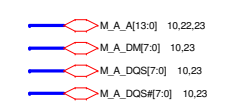
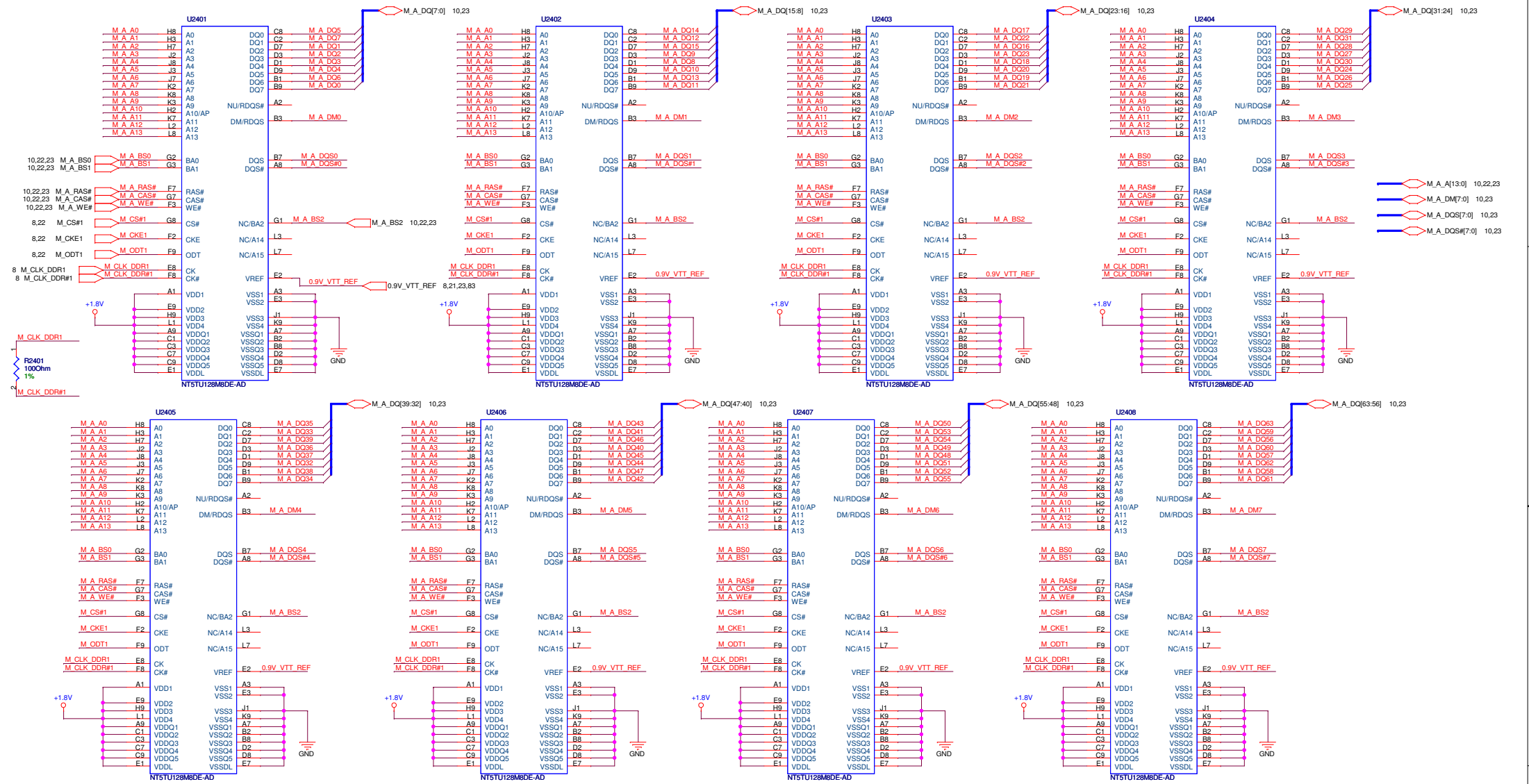


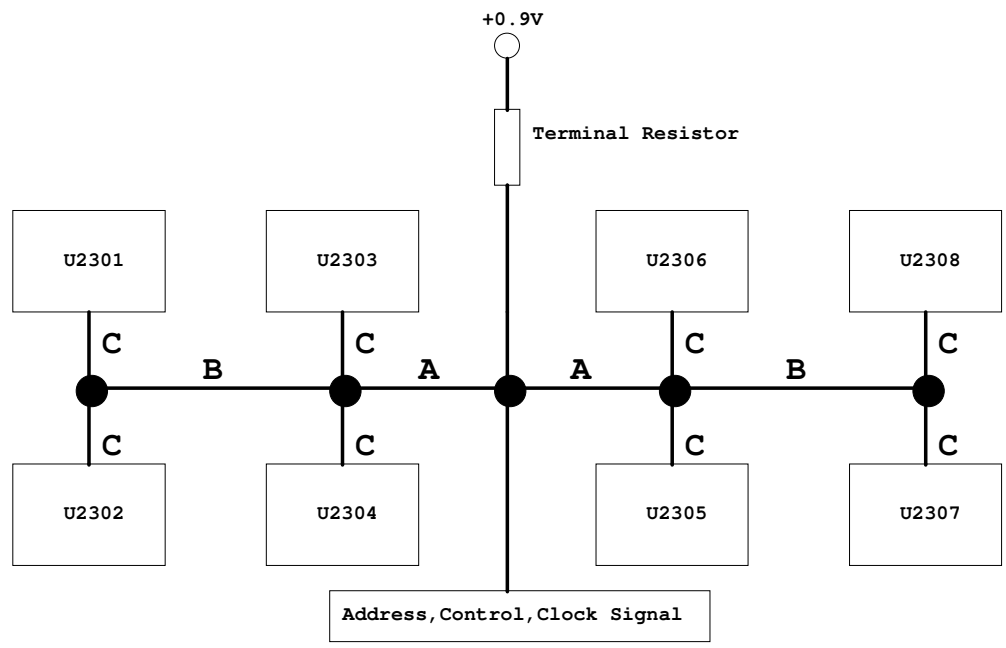
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ASUS		Title : DDR2 TERMINATION	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009	Sheet	22	of 96



ASUS Title : Schematic page name
 ASUSTek COMPUTER INC Engineer: N/A
 Custom Project Name: K40LJ/K50LJ
 Date: Monday, March 09, 2009 Sheet 23 of 96





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<Variant Name>

		Title : Schematic page name	
ASUSTek COMPUTER INC		Engineer: Alex&Bruce	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	26 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	27 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date:	Monday, March 09, 2009	Sheet	28 of 96

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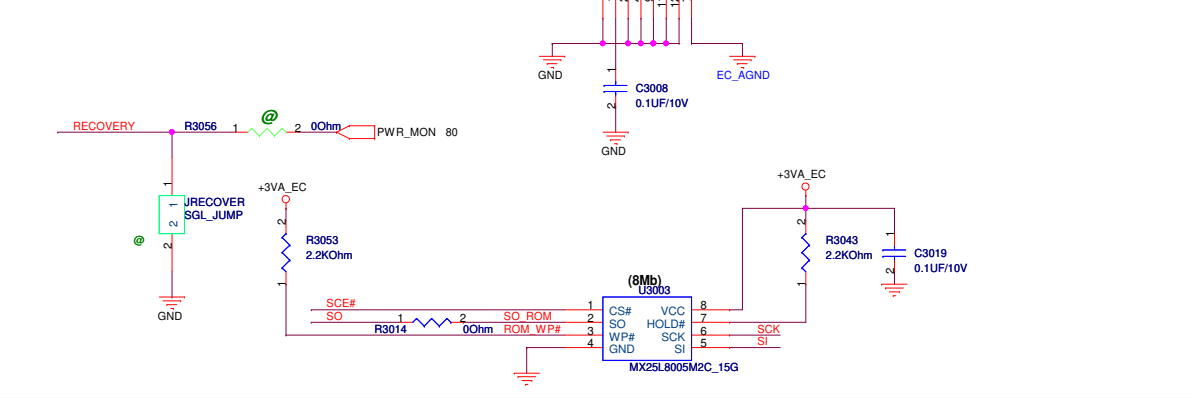
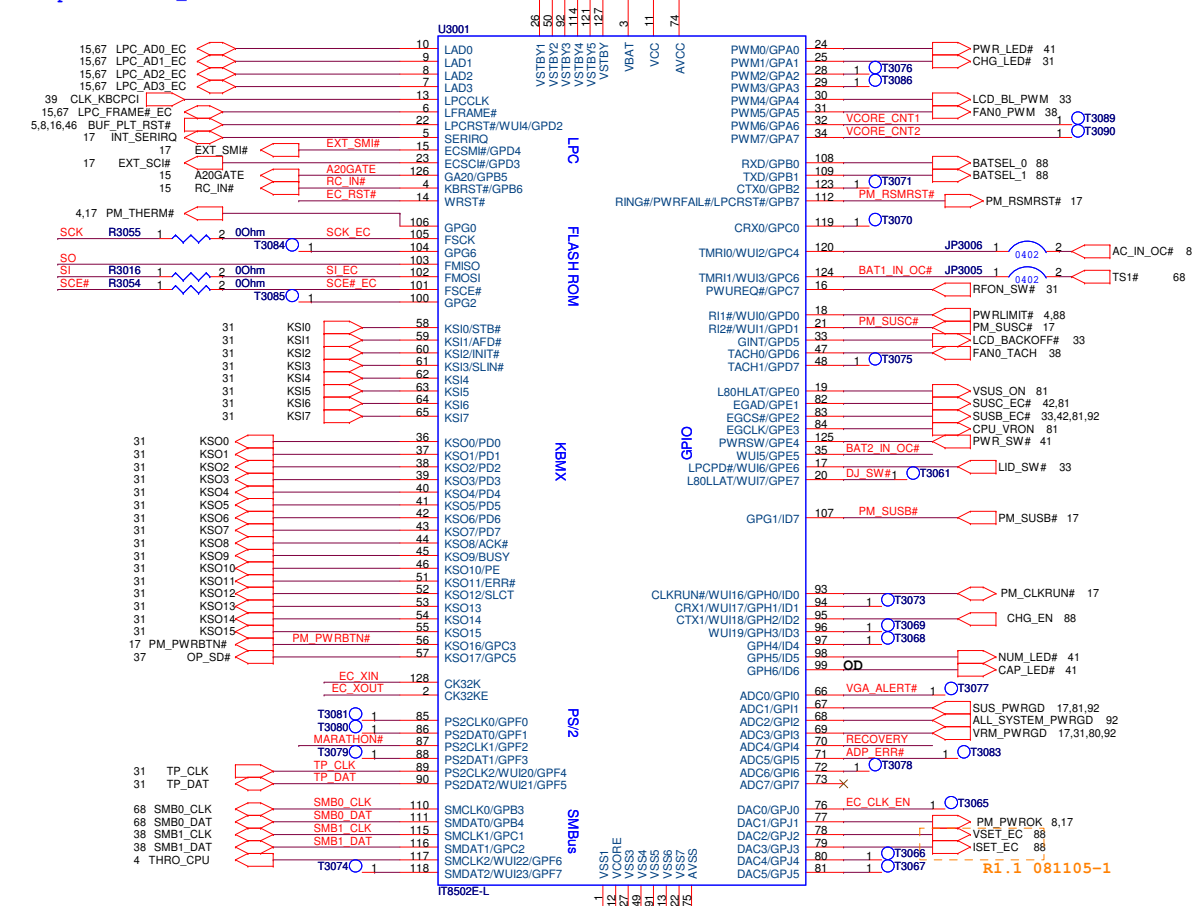
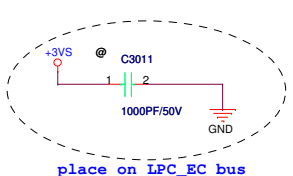
B

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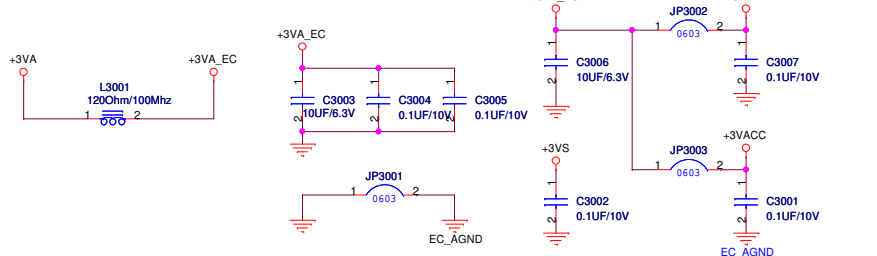
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<Variant Name>

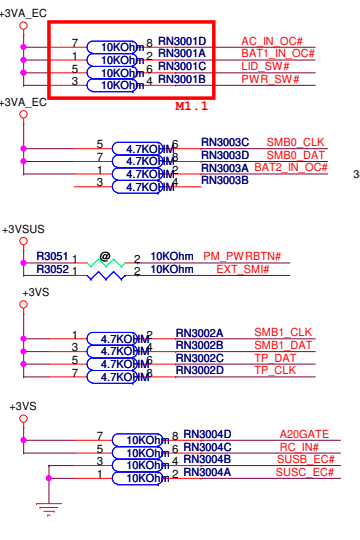
		Title : N/A	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	29 of 96



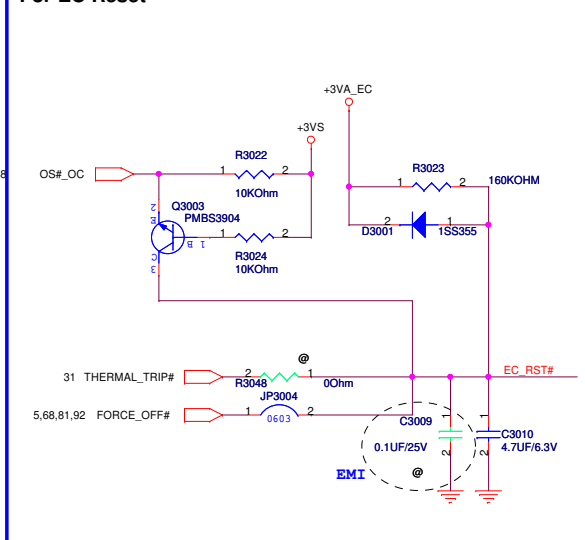
For IT8702 Power



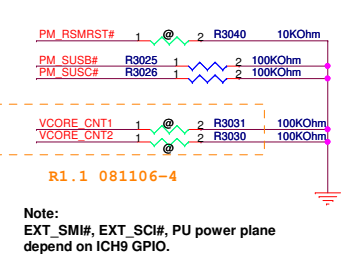
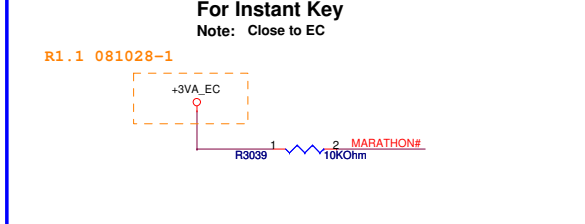
For PU / PD



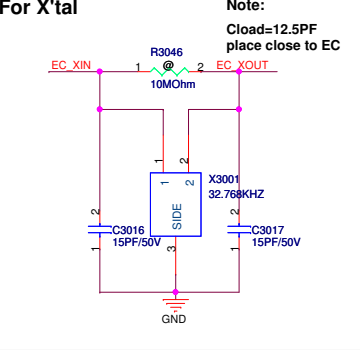
For EC Reset



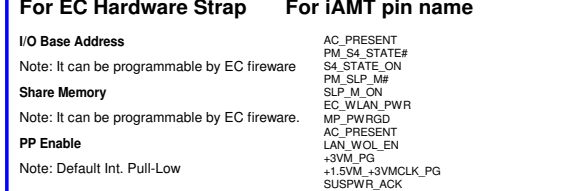
For Instant Key



For X'tal



For EC Hardware Strap



For iAMT pin name

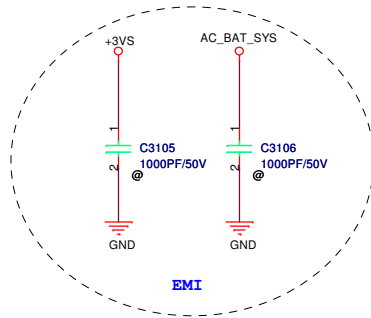
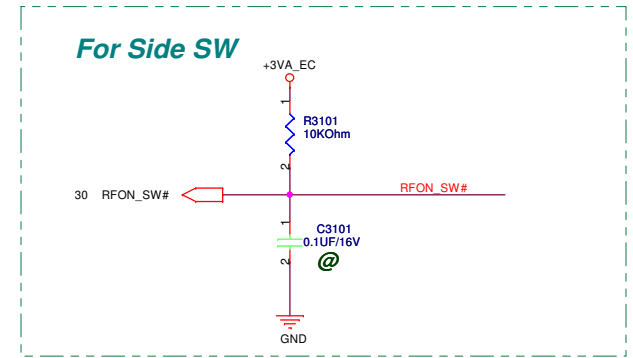
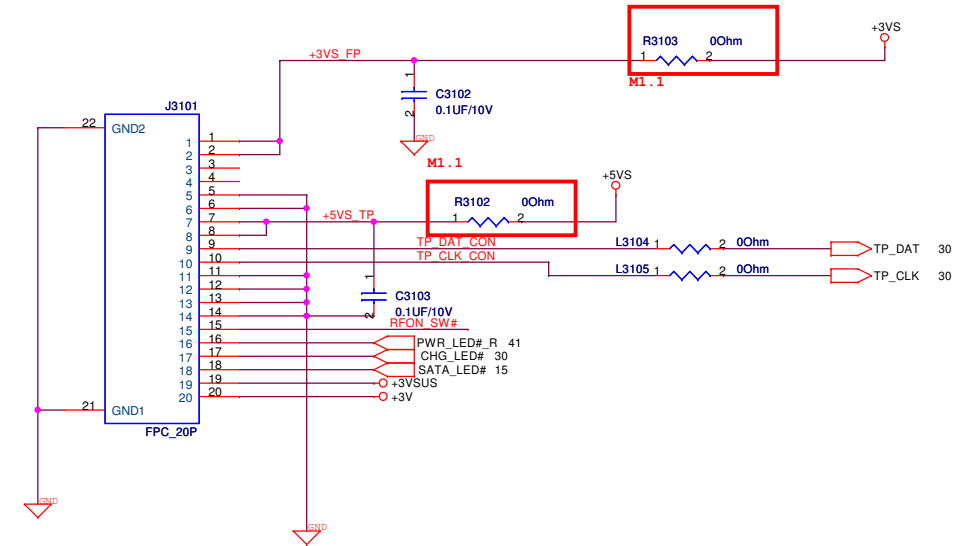
- AC_PRESENT
- PM_S4_STATE#
- S4_STATE_ON
- PM_SLP_M#
- SLP_M_ON
- EC_WLAN_PWR
- MP_PWRGD
- AC_PRESENT
- LAN_WOL_EN
- +3VM_PG
- +1.5VM_+3VMCLK_PG
- SUSPWR_ACK

ASUS® Title : EC_IT8512E-L (1/2)
ASUSTeK COMPUTER INC. NBI Engineer: Wendell Lo

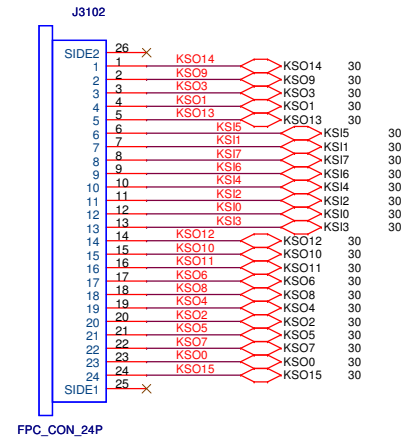
Size	Project Name	Rev
Custom	K40LJ/K50LJ	1.1

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TouchPad & FingerPrint

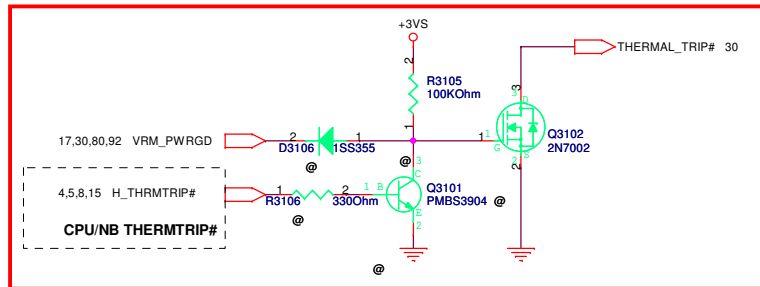


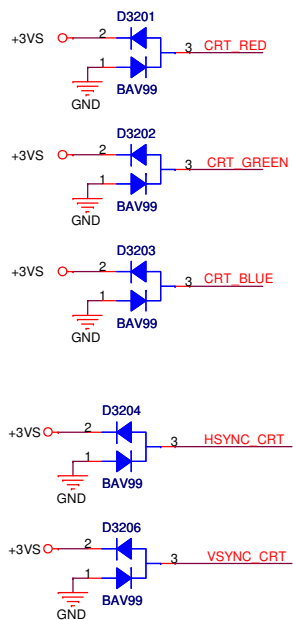
Keyboard Connector



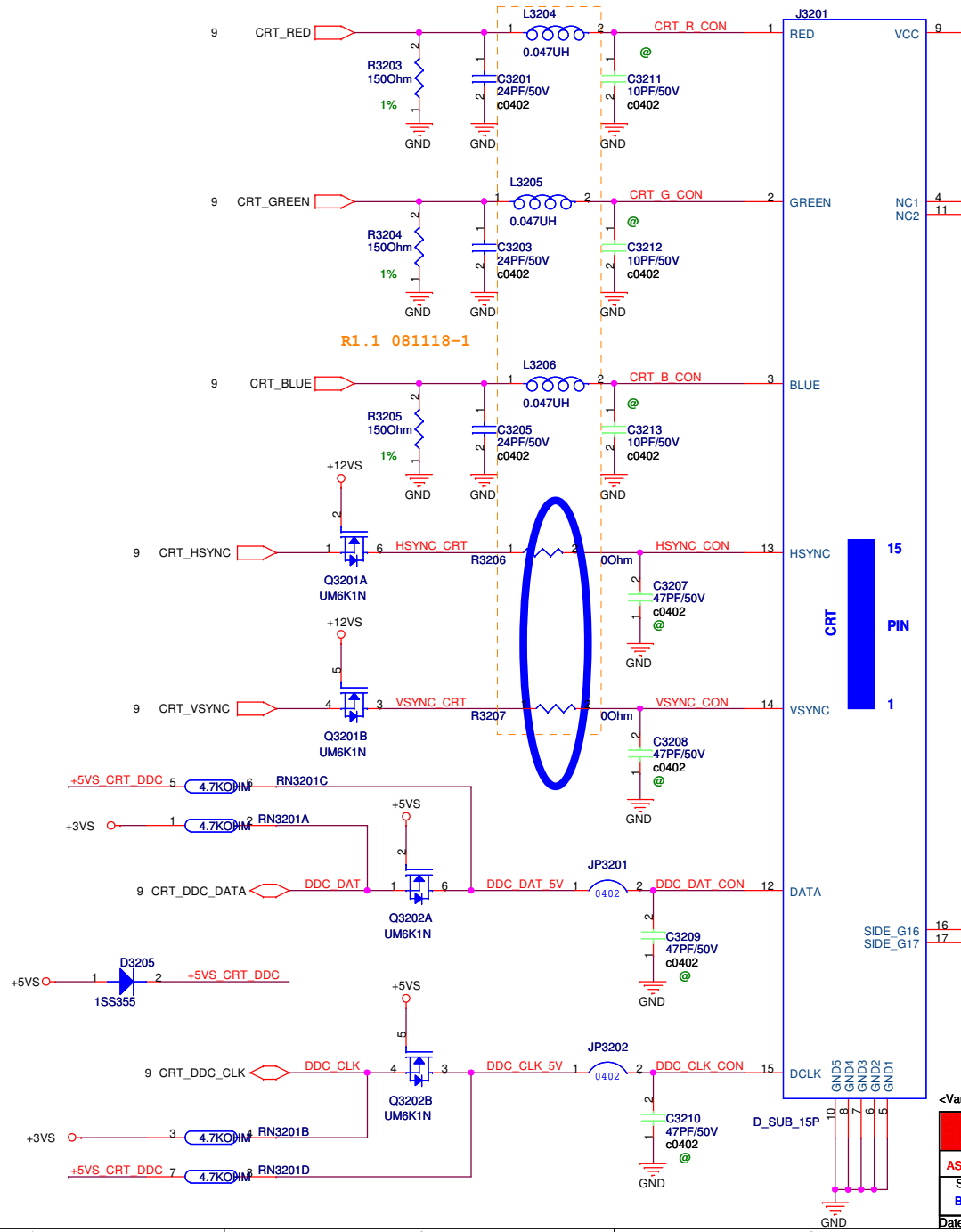
For Thermal Control Method

Remove redundant components





PLACE ESD Diodes near VGA port



<Variant Name>

		Title : CRT
ASUSTeK COMPUTER INC		Engineer: N/A
Size B	Project Name K40IJ/K50IJ	Rev 1.1
Date: Monday, March 09, 2009		Sheet 32 of 96

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For Bluetooth

<Variant Name>

		Title : BT	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	34 of 96

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<Variant Name>  Title : N/A		
ASUSTek COMPUTER INC Engineer: N/A		
Size A	Project Name K40IJ/K50IJ	Rev 1.1
Date: Monday, March 09, 2009		Sheet 35 of 96

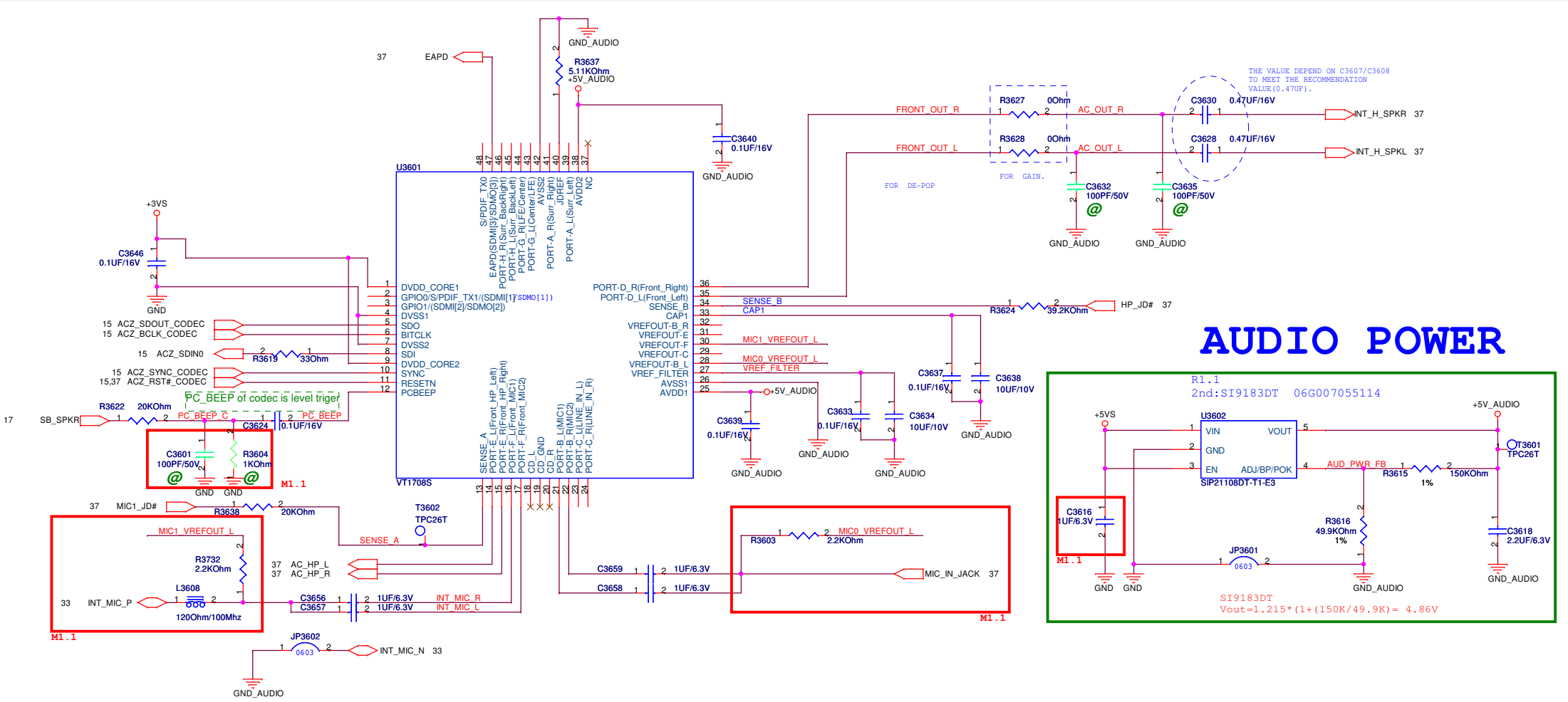
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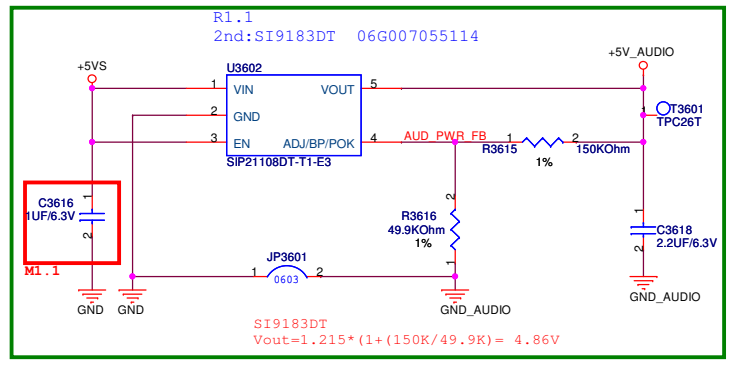
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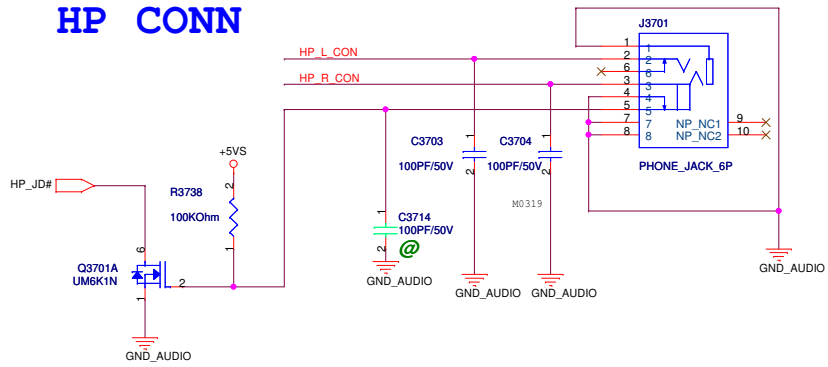
AUDIO POWER



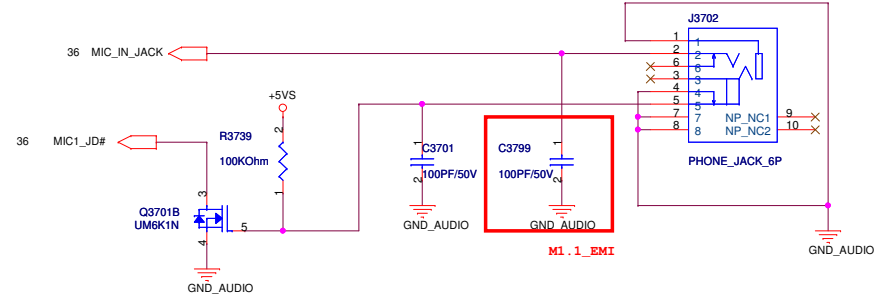
<Variant Name>

ASUS		Title : CONEXANT CX20582	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	K40LJ/K50LJ		1.1
Date: Monday, March 09, 2009		Sheet	36 of 96

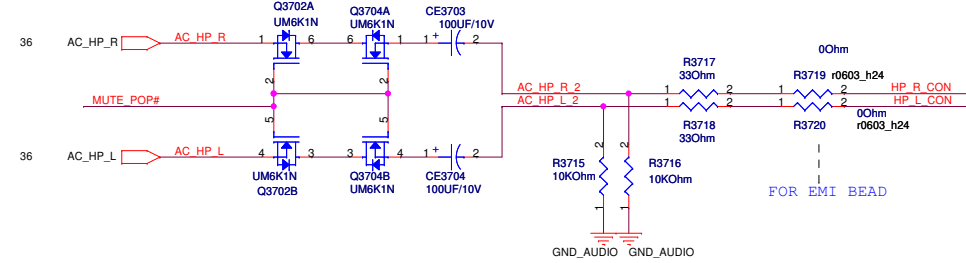
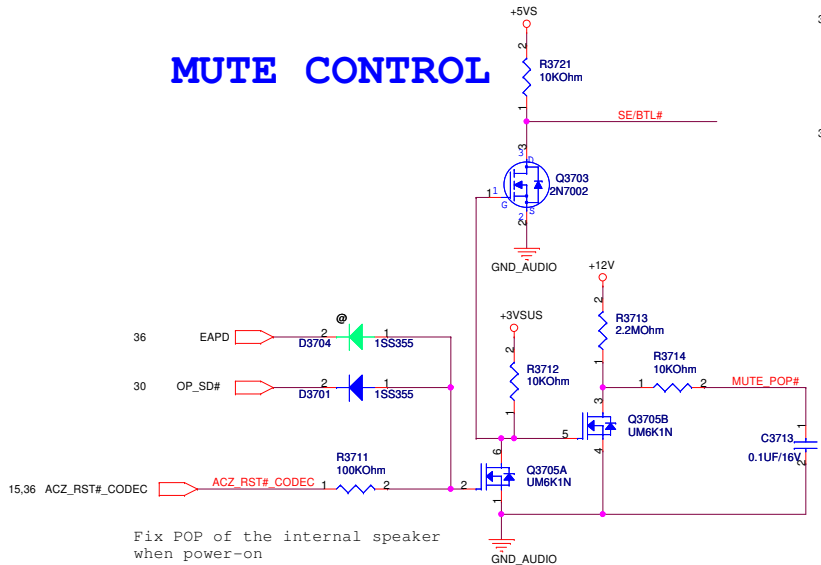
HP CONN



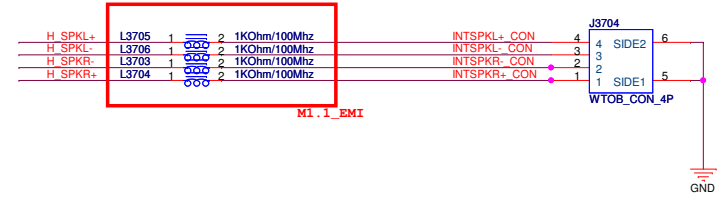
External MIC CONN



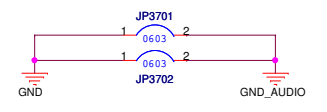
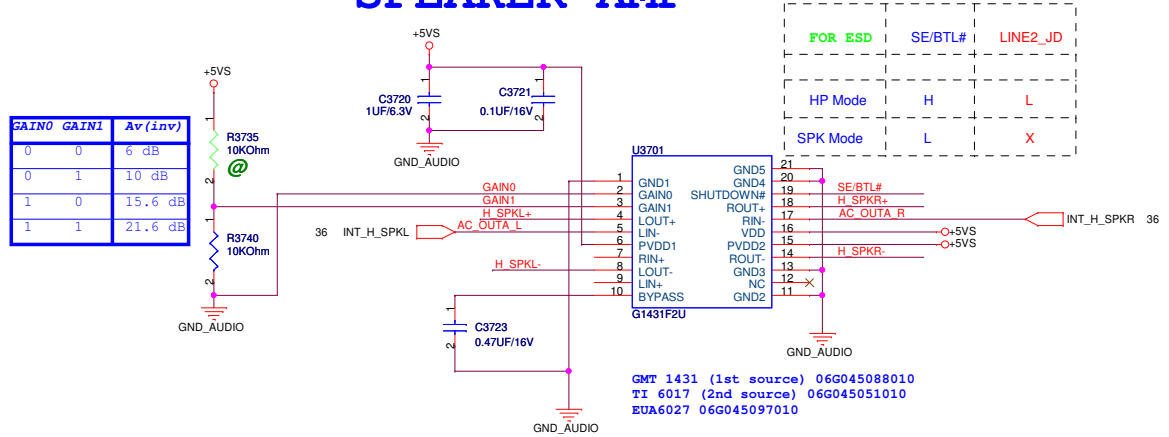
MUTE CONTROL



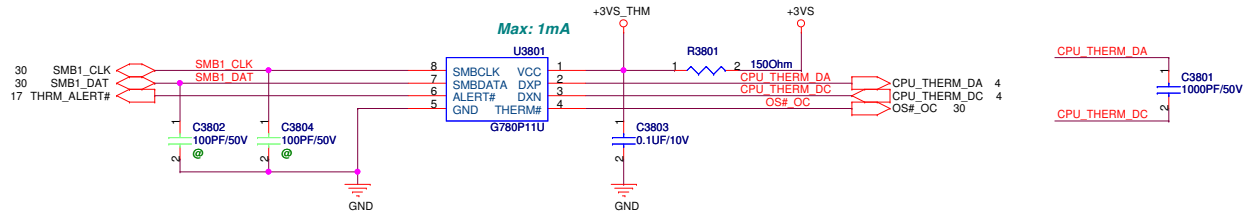
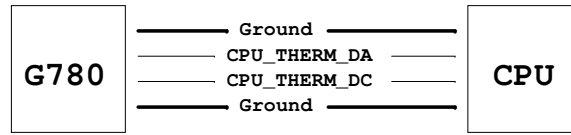
SPEAKER CONNECTOR (2W)



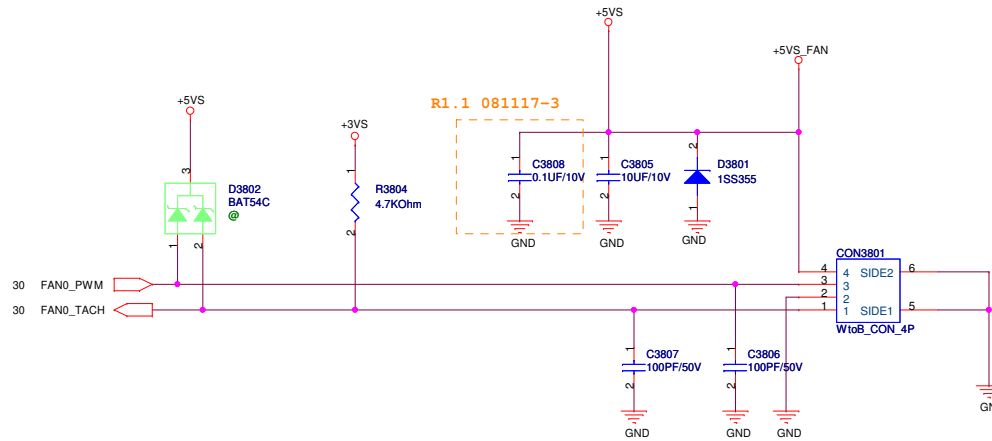
SPEAKER AMP



Thermal Sensor

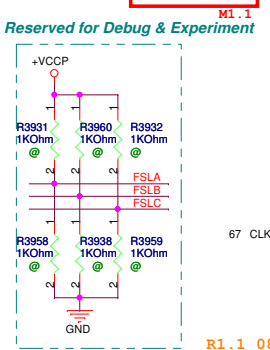
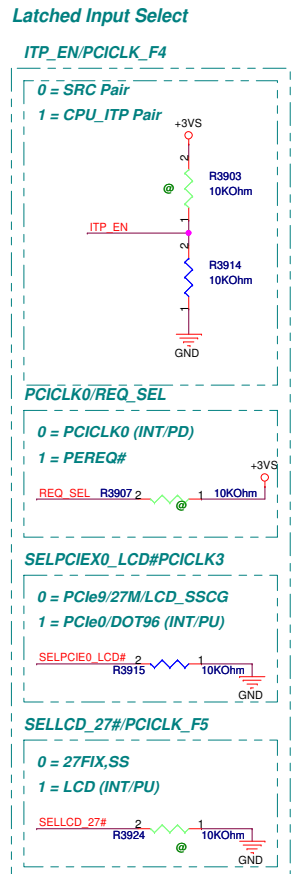
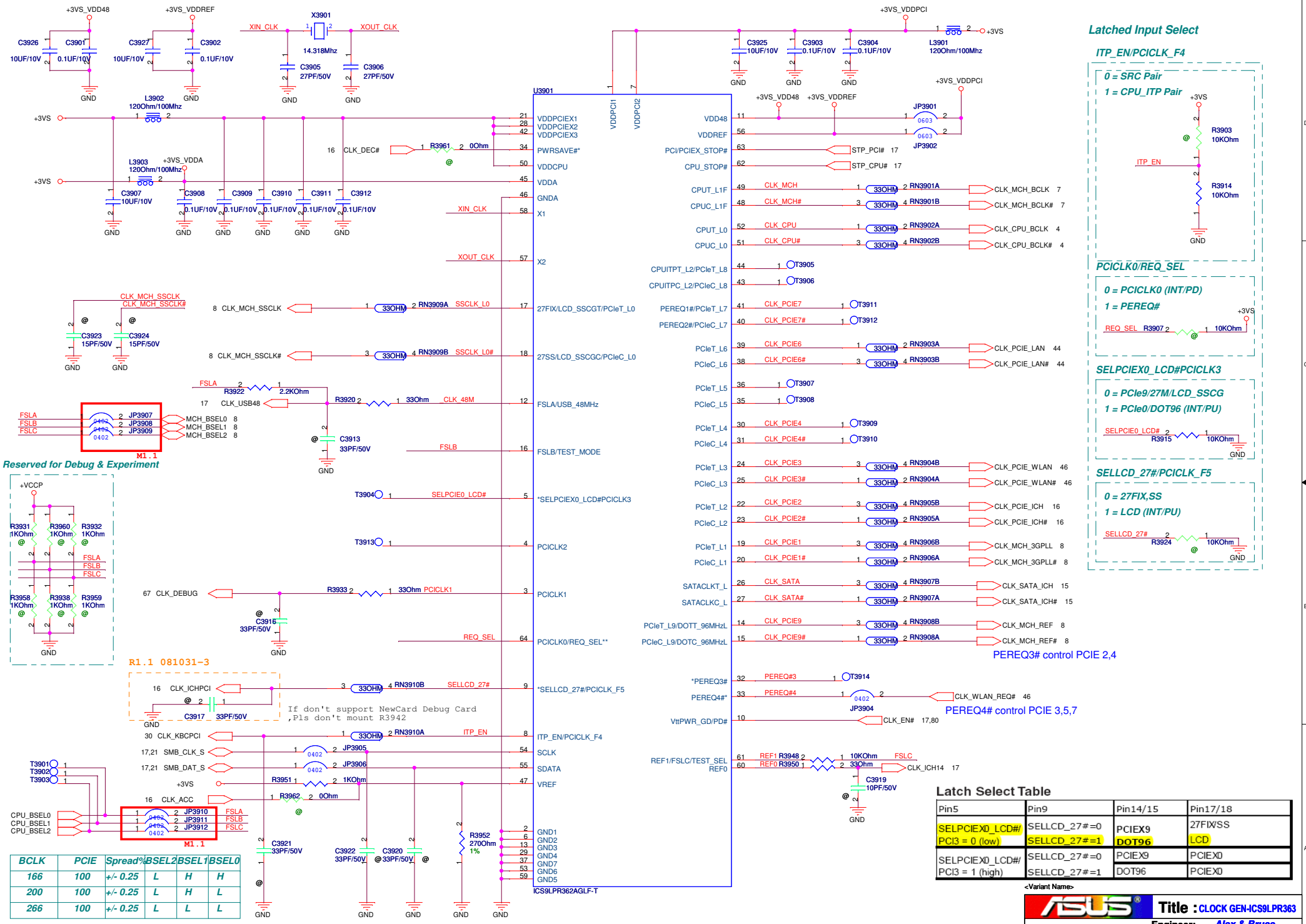


add 2nd source :06G023096010



<Variant Name>

ASUS		Title : THER SENSOR & FAN	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40J/K50J	1.1	
Date: Monday, March 09, 2009		Sheet	38 of 96



BCLK	PCIE	Spread%	BSEL2	BSEL1	BSEL0
166	100	+/- 0.25	L	H	H
200	100	+/- 0.25	L	H	L
266	100	+/- 0.25	L	L	L

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE0_LCD# PCI3 = 0 (low)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	27FIX/SS LCD
SELPCIE0_LCD# PCI3 = 1 (high)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	PCIE0 PCIE0

ASUS Title: **CLOCK GEN-ICS9LPR363**
ASUSTek COMPUTER INC. NB1 Engineer: **Alex & Bruce**
 Size: **Custom** Project Name: **K40IJ/K50IJ** Rev: **1.1**
 Date: **Monday, March 09, 2009** Sheet: **39** of **96**

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	40 of 96

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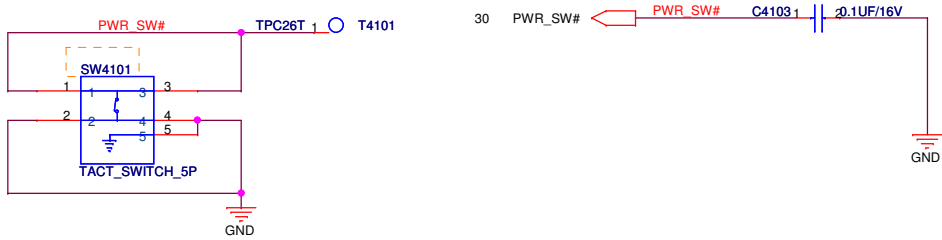
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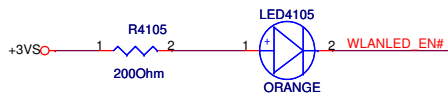
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SWITCH BUTTON

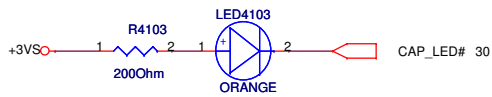


LED

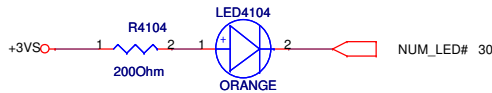
For WireLess LED



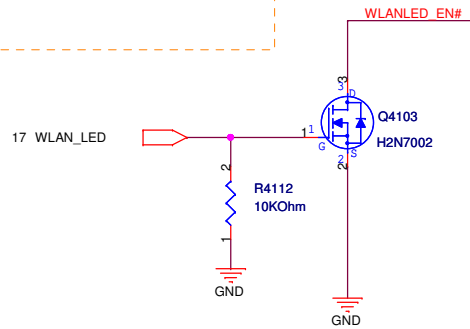
for Cap. Lock



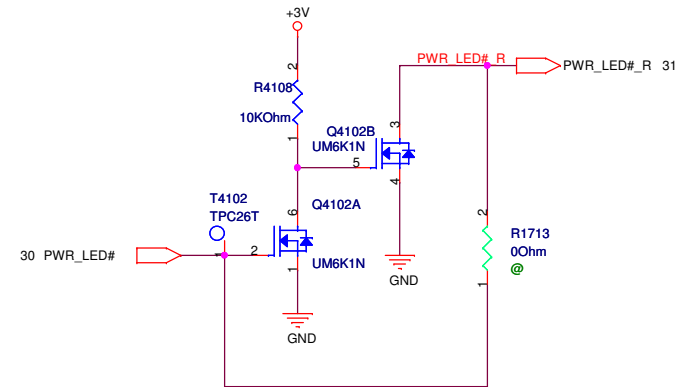
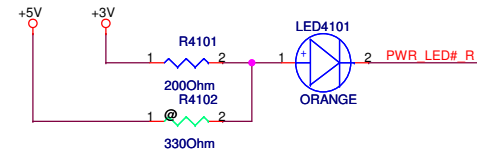
for Num Lock



R1.1 081031-4

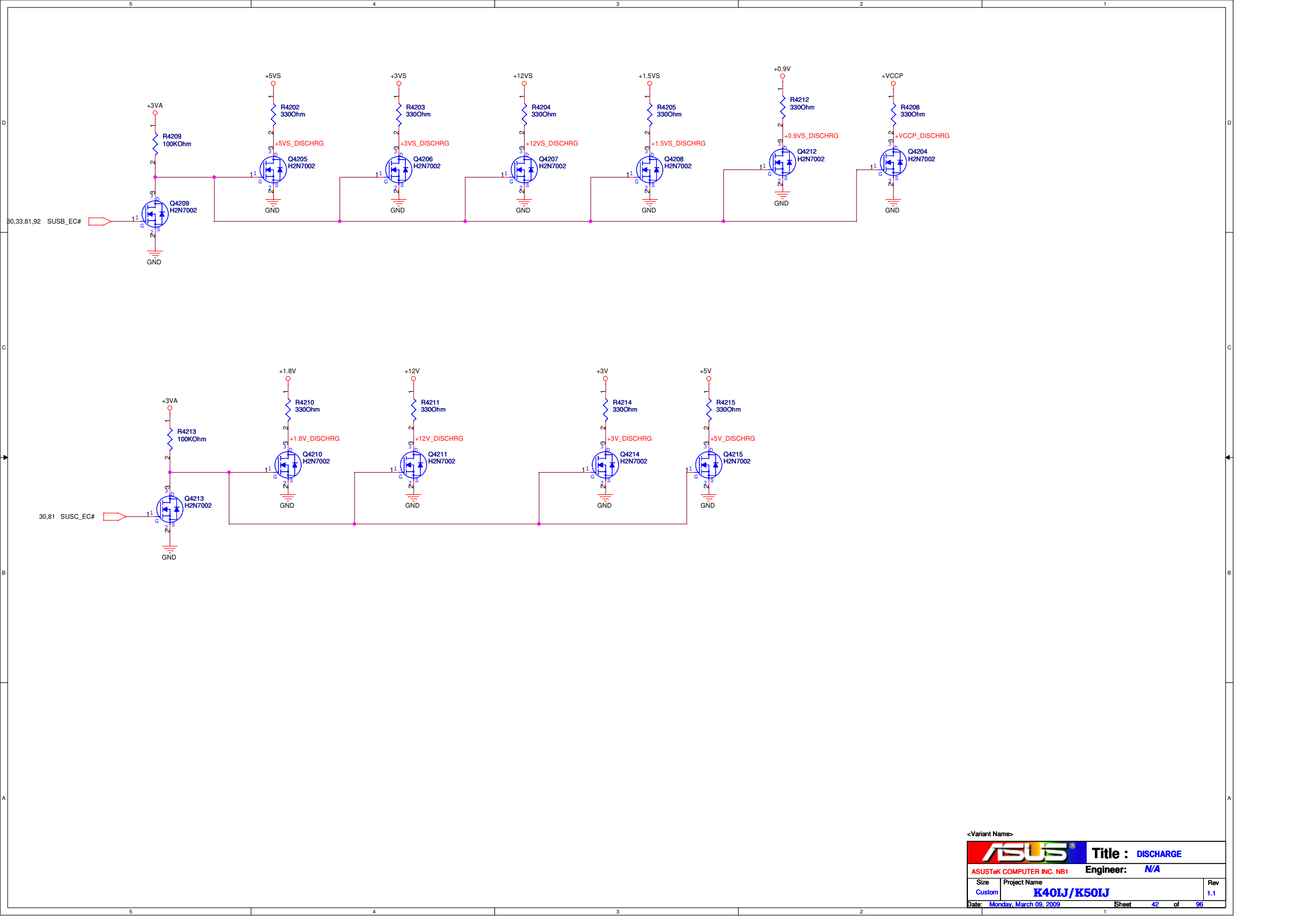


For POWER LED



<Variant Name>

ASUS		Title :Switch Button & LED	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
B	K401J/K501J		1.1
Date: Monday, March 09, 2009		Sheet	41 of 96



<Variant Name>

ASUS		Title : DISCHARGE
ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size	Project Name	Rev
Custom	K40J/K50J	1.1
Date: Monday, March 09, 2009	Sheet	42 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	43 of 96

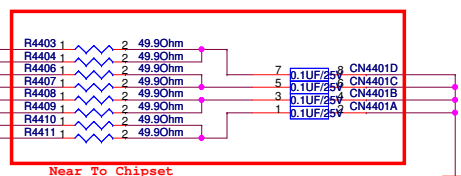
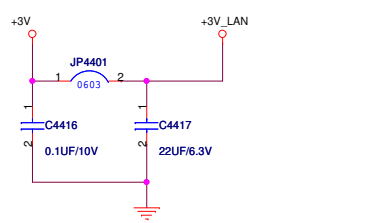
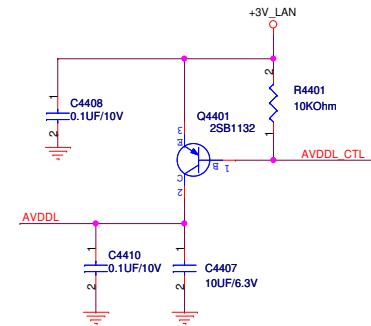
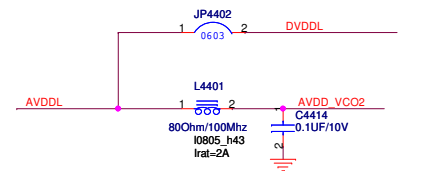
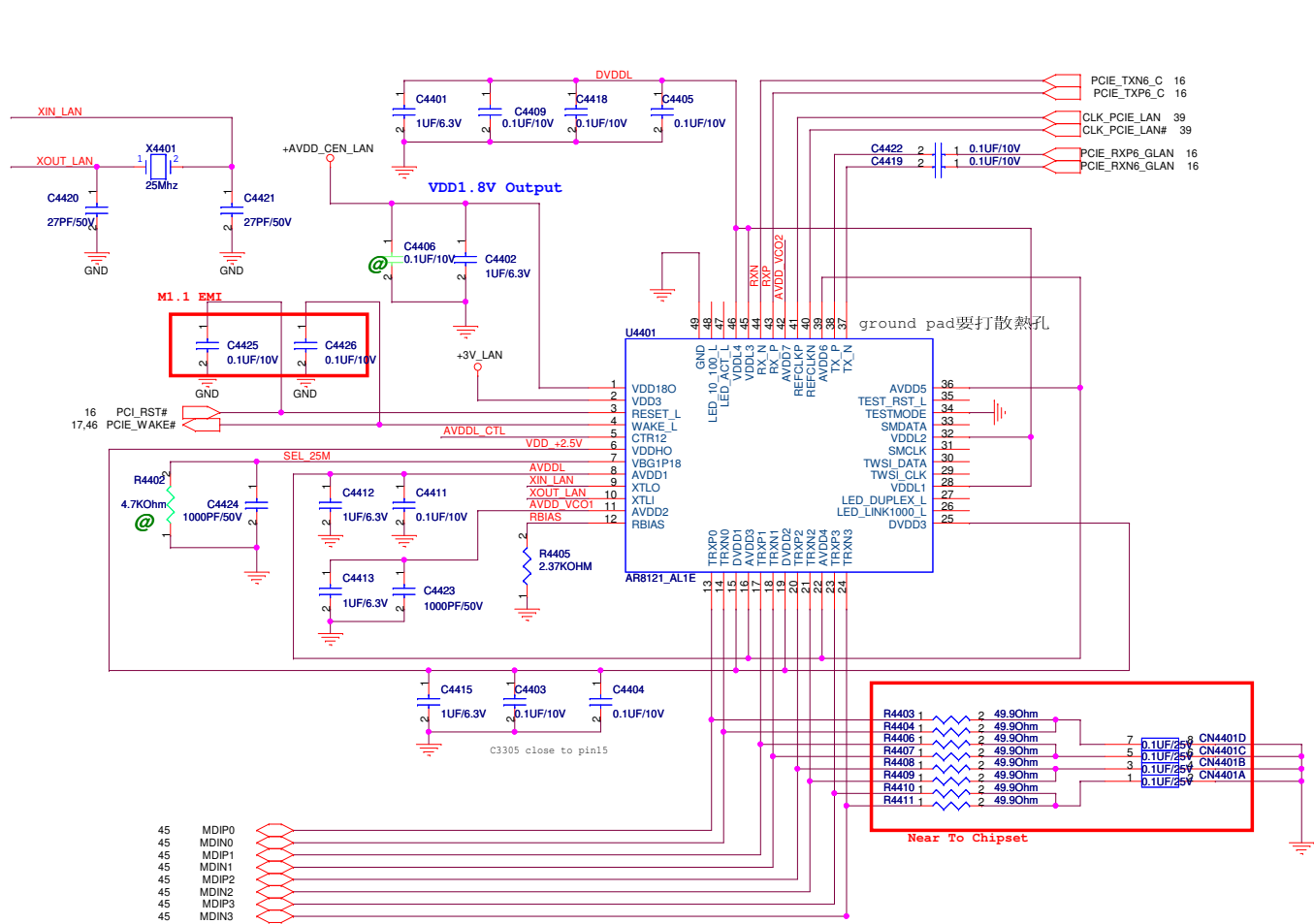
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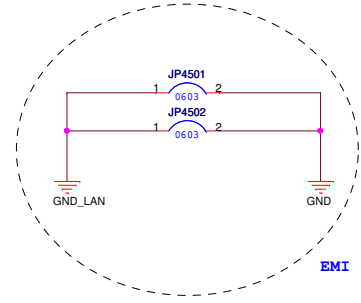
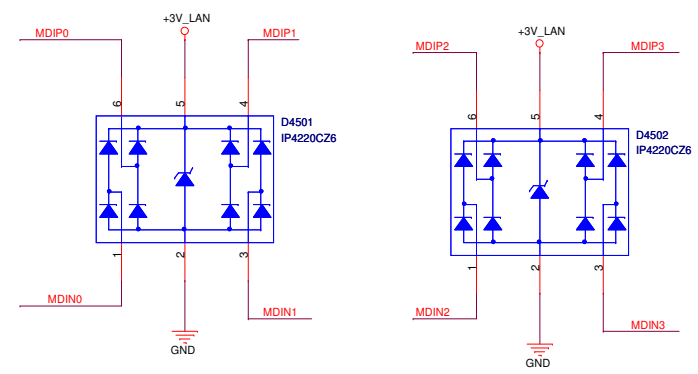
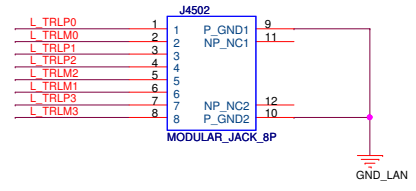
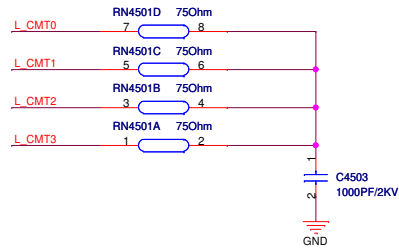
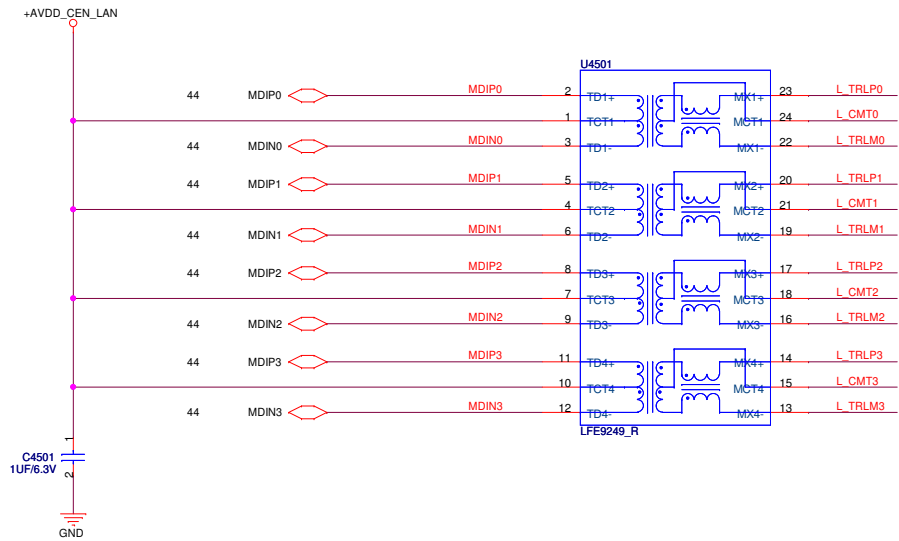
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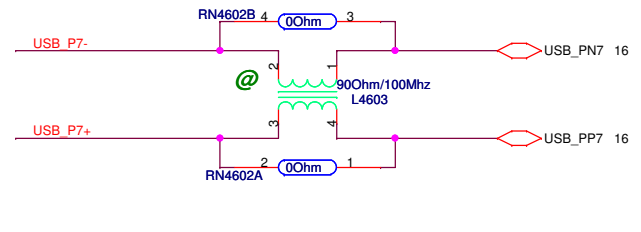
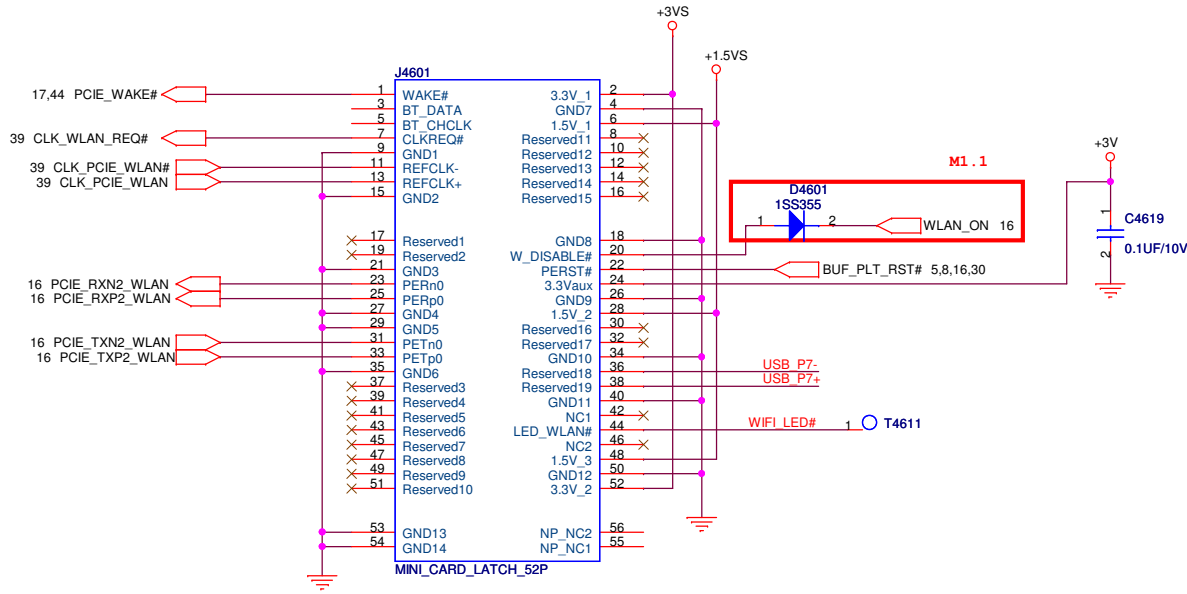
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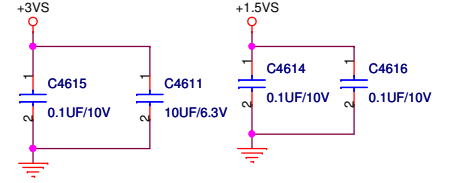


LAN CONN.





WLAN H=7.5mm



<Variant Name>

ASUS		Title :Mini card_WLAN+3G	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	46 of 96

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<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	47 of 96

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<Variant Name>

		Title :Schematic page name	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	48 of 96

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<Variant Name>

		Title : Schematic page name
ASUSTeK COMPUTER INC. NB1		Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009 Sheet 49 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	50 of 96

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<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	51 of 96

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<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	52 of 96

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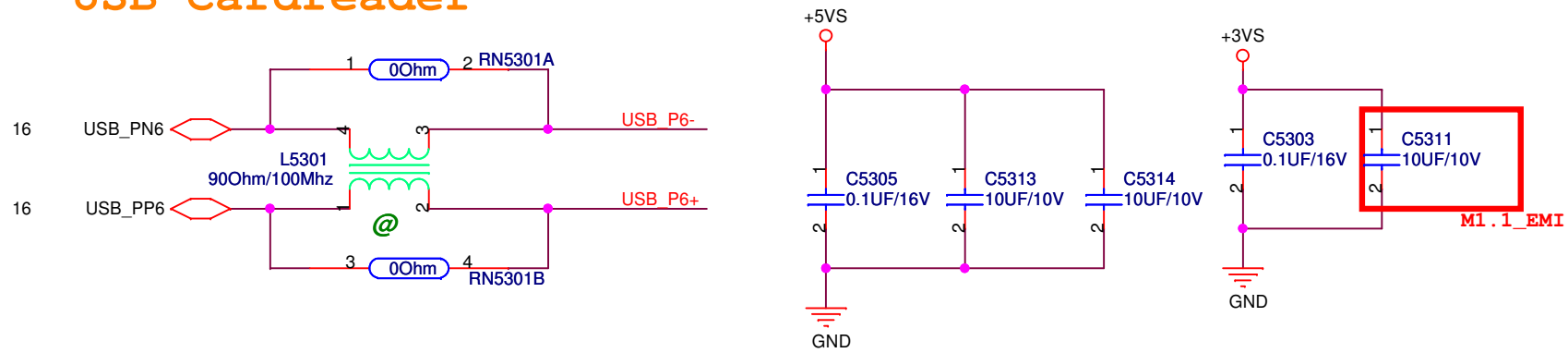
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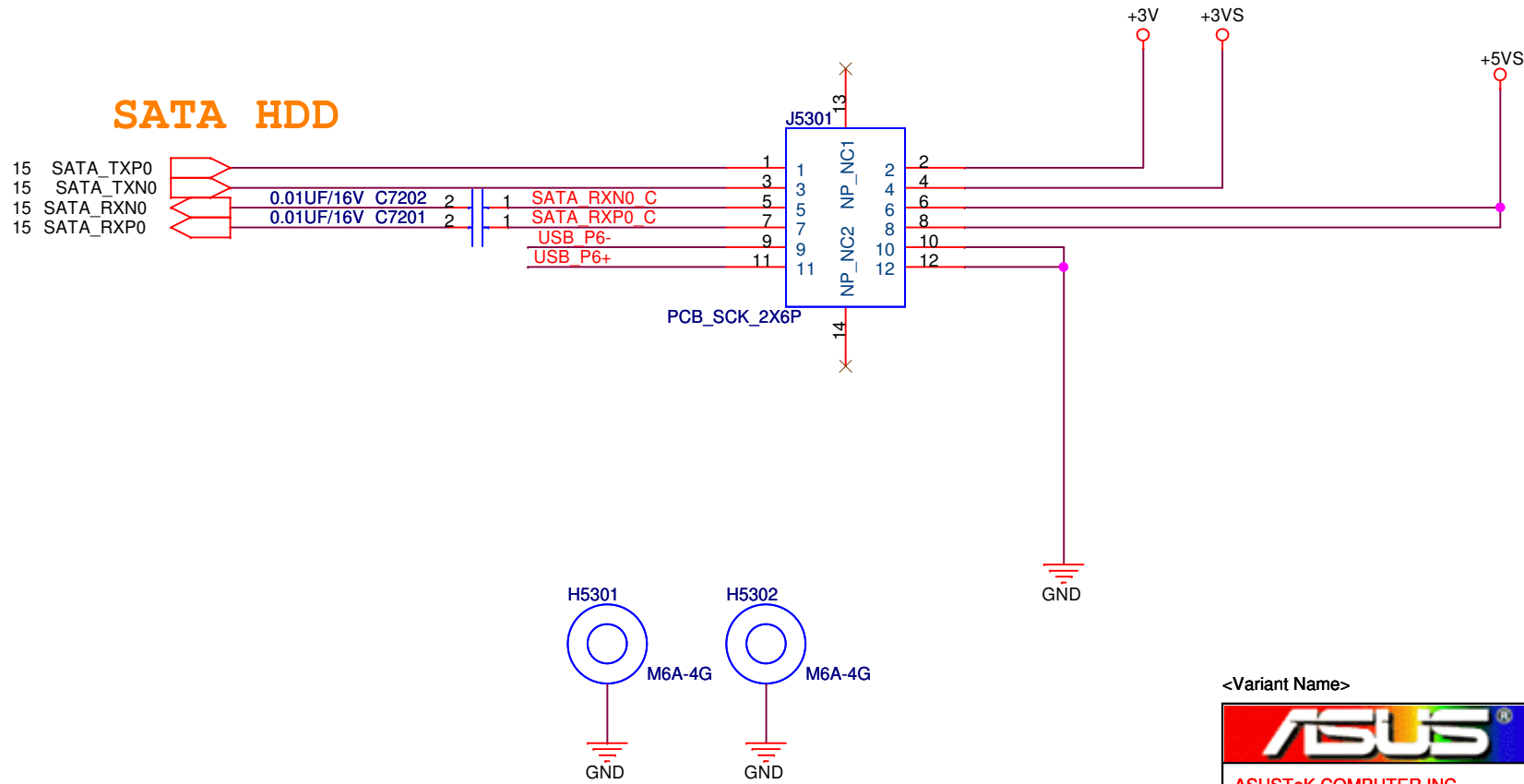
2

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USB Cardreader



SATA HDD



<Variant Name>

		Title :SATA_HDD & Cardreader	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size Custom	Project Name K40IJ/K50IJ		Rev 1.1
Date: Monday, March 09, 2009		Sheet 53 of 96	

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<Variant Name>

		Title : NEWCARD
ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size	Project Name	Rev
B	K40IJ/K50IJ	1.1
Date: Monday, March 09, 2009		Sheet 54 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date:	Monday, March 09, 2009	Sheet	55 of 96

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<Variant Name>

		Title : HDA level shifter	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>N/A</i>	
Size Custom	Project Name K40LJ/K50LJ		Rev 1.1
Date: <i>Monday, March 09, 2009</i>		Sheet <i>56</i> of <i>96</i>	

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HDMI WtoB Connector

HDCP ROM

<Variant Name>

		Title : iHDMI
ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size B	Project Name	Rev 1.1
Date: Monday, March 09, 2009		Sheet 57 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	58 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
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<Variant Name>



Title : Schematic page name

ASUSTeK COMPUTER INC Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	61 of 96

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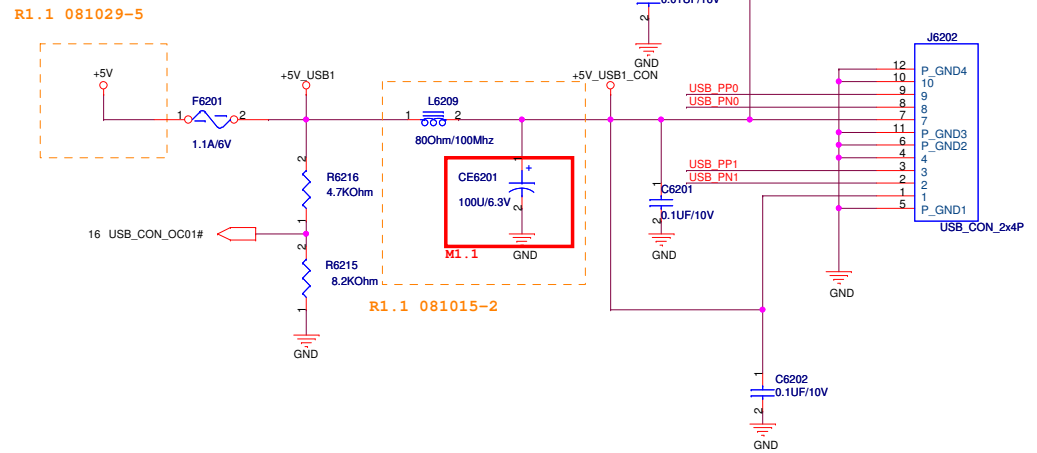
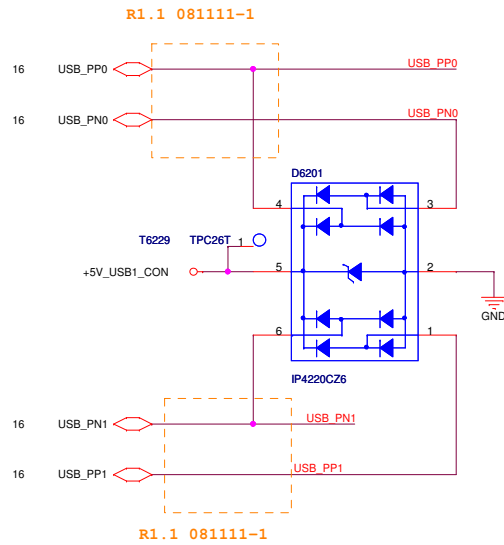
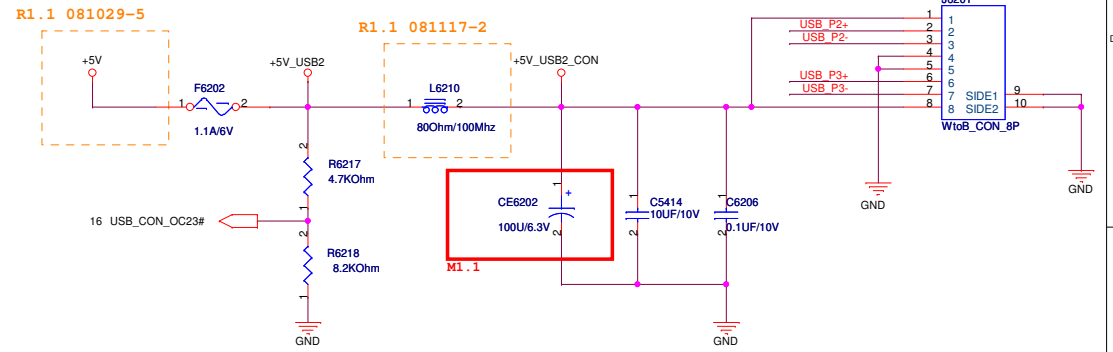
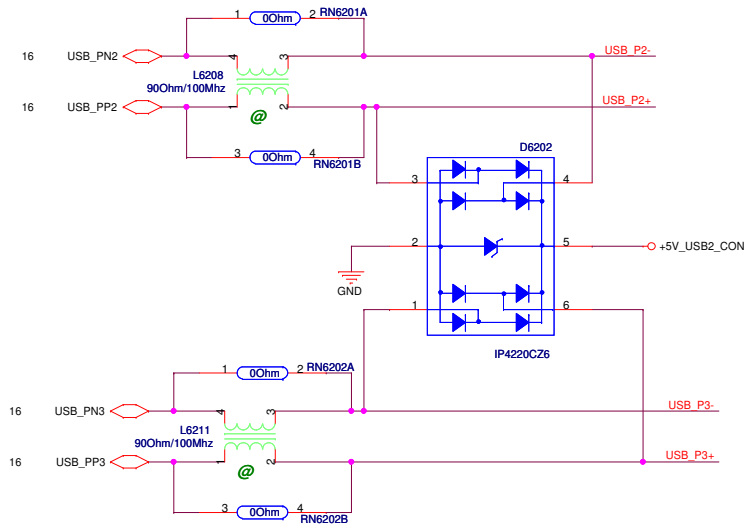
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USB IO Board



<Variant Name>

ASUS		Title : USB CONN	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40J/K50J	1.1	
Date: Monday, March 09, 2009	Sheet	62	of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	63 of 96

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<Variant Name>

		Title :Schematic page name	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009	Sheet 64	of 96	

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<Variant Name>

		Title : SPI ROM	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	65 of 96

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<Variant Name>

		Title : LED	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	66 of 96

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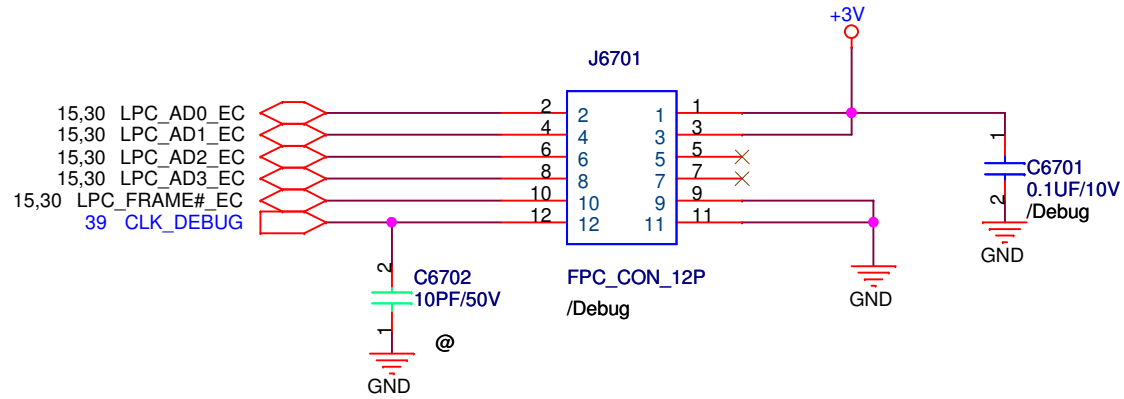
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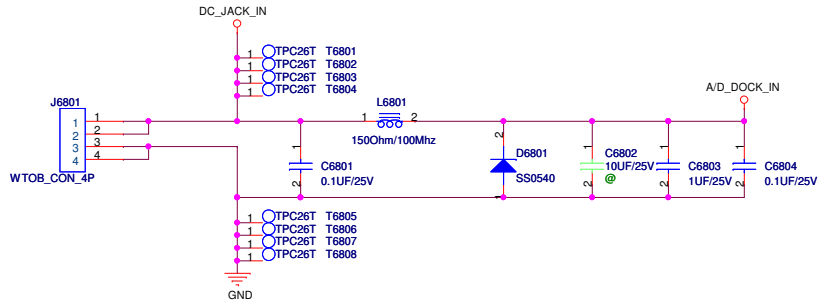
LPC DEBUG PORT



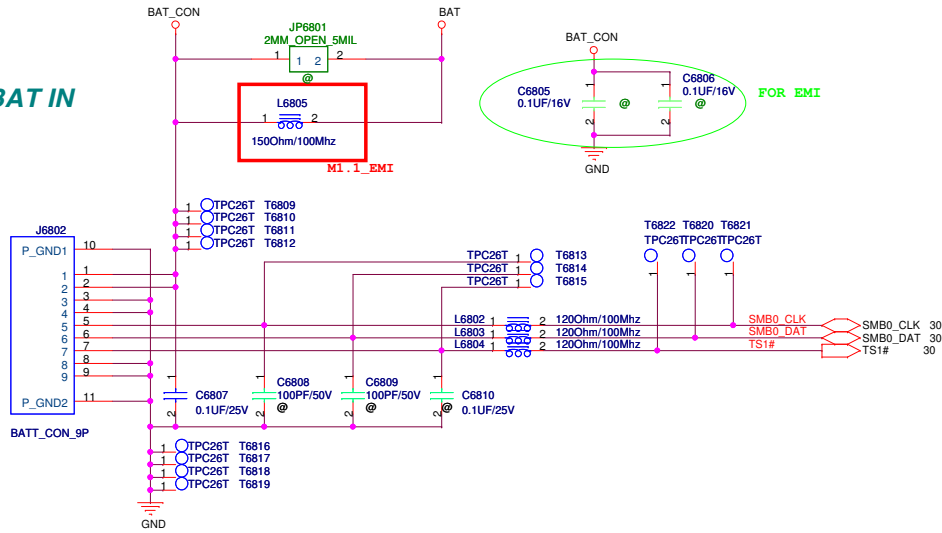
<Variant Name>

ASUS		Title : DEBUG CONN
ASUSTeK COMPUTER INC		Engineer: N/A
Size A	Project Name K40IJ/K50IJ	Rev 1.1
Date: Monday, March 09, 2009		Sheet 67 of 96

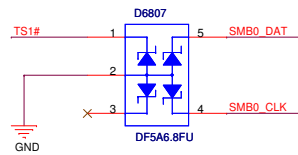
DC IN



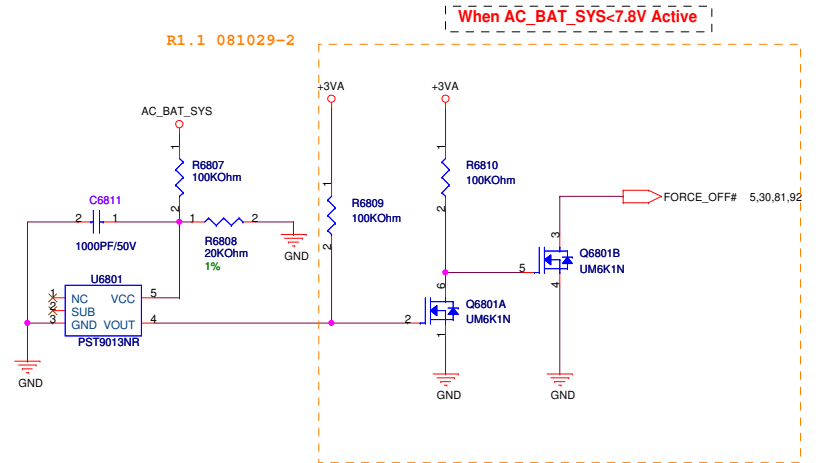
BAT IN



Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.



Without Battery & Pull out Adapter



<Variant Name>

ASUS		Title : DC & BAT IN	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40J/K50J	1.1	
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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
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<Variant Name>

		Title : Debug CONN.
ASUSTeK COMPUTER INC		Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009 Sheet 70 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date:	Monday, March 09, 2009	Sheet	71 of 96

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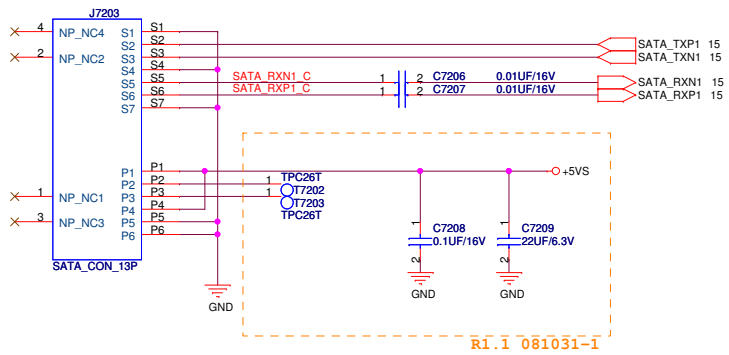
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ODD



<Variant Name>

ASUS		Title : SATA-ODD
ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1
Date: Monday, March 09, 2009	Sheet	72 of 96

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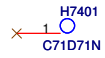
A

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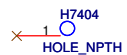
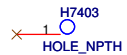
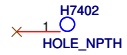
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ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	73 of 96

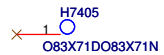
Hole-A



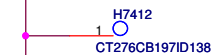
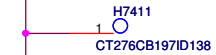
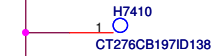
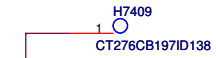
Hole-B



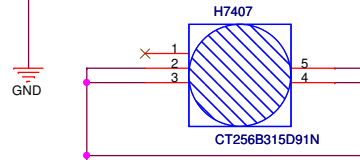
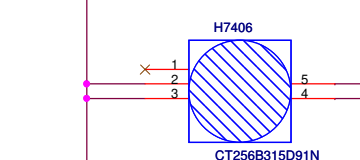
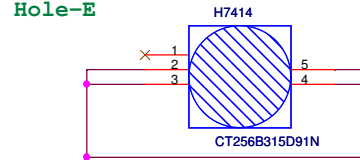
Hole-C



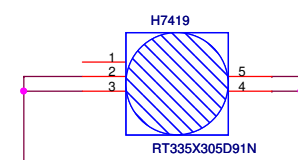
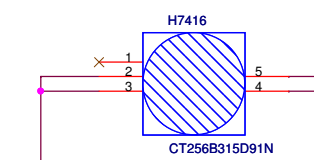
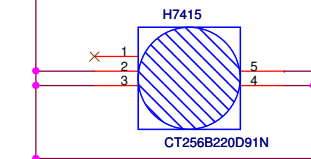
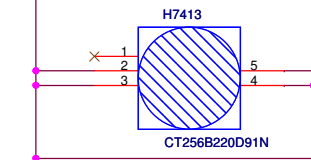
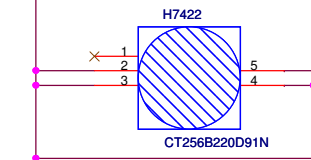
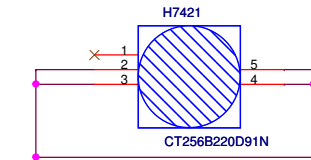
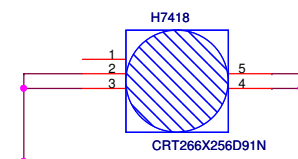
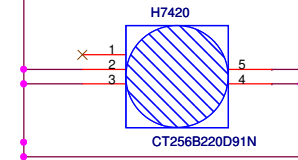
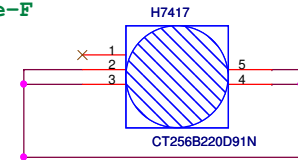
Hole-D



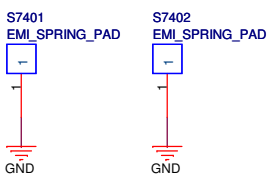
Hole-E



Hole-F



Spring



<Variant Name>

		Title : Hole	
ASUSTeK COMPUTER INC		Engineer: Leon Guo	
Size	Project Name		Rev
B	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	74 of 96

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<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
A	K40IJ/K50IJ	1.1	
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<Variant Name>

	Title :EXPRESS GATE
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ASUSTeK COMPUTER INC	Engineer: N/A
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Size Custom	Project Name K40IJ/K50IJ	Rev 1.1
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R1_1 Modify List
P04_Q0402,R0401 No mount
P36_INT_MIC Change
P37_J2704 speaker_H_SPKL+/H_SPKL-/H_SPKR+/H_SPKR- Signal modify,Del R3732
P05_C80502,C0528,31,32,33,36,43 NO-Stuff
P07_C0702 NO-Stuff
P08_R0813 NO-Stuff,R0815/R0816 10K OHM change to 0 OHM(E/R Check if ok change to J8110 to J8113
R0817 100 OHM Change to Short JP
P12_C1223,C1245 100F/10V(1206) change to 100F/6.3V(0805) for reduce
P24_Add On-board memory to 2G
P30_change "BATSEL_28#" to "BATSEL_0"
change "BATSEL_38#" to "BATSEL_1"
Merge R3020,21,27,29 to array resistor
P36_C3616 Y5V change to X7R for reduce component count
P37_C3720 Y5V change to X7R for reduce component count
P39_Delete RN3901,RN3902
P44_Change LAN Chip from RTL8111DL to AN8121
P09_R0910,11,12 change to RN0901 array package
R3002,03,05,28 change package
P18_Add C1843,C3324,C2203,C4425,C4426 for EMI
Del R3506
Change ReferenceC7213,03,05,11 to C53013,03,05,11
P16_For EMI CMOS form Port 4 change to Port 8
P62_C86202 Change package
P11_C1125,26,30 0.22UF change to 1UF cost down
P3601_Reserve C3601,R3604 for Vendor request
P31_L3102,03 change to R3103,02
Add JP1502 del R3151
Del R0918,R0919 add RN0902
P39_Del R3946 ,add RN3910
P09_C8901,02,03 add for EMI
P04_C0402 add for EMI



P05_Del JP0501
P16_Add R1602
P33_Add R3308,R3309

Power List 1/15
change J8112 to J8112
nostuff C8121
change J8110 to J8110
change J8113 to J8113
change J8114 to J8114
change J8115 to J8115
change J8103 to J8103
change J8106 to J8106
change J8109 to J8109
change J8111 to J8111
change J8105 to J8105
page 82
change JP8203 to J8203
page 83
change JP8303 to J8303
change JP8304 to J8304
page 84
add JP8402
change U8401 to APL5930 from APL5913
page 88
change JP8805 to J8805
1/14
page 80
change Q8001 and Q8003 to 07G005A15011 from 07G005C34010.
change Q8002 and Q8004 to 07G005B71010 from 07G005C33010.
stuff C8003
page 83
change R8304 to 10G212150214030 from 10G212750114010.
1/08
Change all 2MM_SHORT_SMI1 to 2MM_OPEN_SMI1(s00496)
page 81
change "L7020_DLL1" to "8206_DLL1".
page 88
add L8802 between BAT and BAT_CON
change R8823.2 to GND from SGND_CHG.
change "BATSEL_28#" to "BATSEL_0"
change "BATSEL_38#" to "BATSEL_1"
01/07
Delete Empty Page 85,86,87,89,90
Page 80
Change R8010, R8013, R8020, R8035, R8040, R8046 to temp.4759_ch01 from 10G212000004010
Change C8003, C8017 to Unmount
Delete R8050
Page 81
Change R8116, R8119, R8125, R8110, R8107 to temp.4759_ch01 from 10G212000004010
Delete R8102, R8118
Change D8103 to 07G004069020 from 07G001007230
Page 82
Change D8201 to 07G004069020 from 07G001007230
Page 83
Change D8301 to 07G004069020 from 07G001007230
Page 84
Delete R8404
Delete Netname 5913_VCNFL
Page 88
Change D8804 to 07G004069020 from 07G001007230
Page 91
Change R9105, R9108 to 10G252100314030 from 10G212100314030
12/31
page 80
change Q8002, Q8004 to 07G005C35010 from 07G005C33010
change U8001 to 06G008425013 from 06G008692010
change R8026 to 10G212680114010 from 10G212953114010
12/26
page 81
change CE8101, CE8102 to 11G08D21075A from 11G09X222755.
page 82
delete Q8203.
delete C8207.
change CE8202 to 11G08D2227D1 from 11G09X222755.
change U8201.7, U8201.15, R8205.1 to SGND.
page 83
change CE8301 to 11G08D2227D1 from 11G09X222755.
change JP8301 to 2MM.
page 88
change U8801.6 net name to CHG_INE3 from CHG_COMP3.
change C8806, C8809 to 11G233110412030 from 11G23210412360.
change Q8802, Q8803 PCB Footprint to soic_8p_50_197x236.
page 91
change R9107 to 10G212220214030 from 10G213220213010.
page80
add net name "SNB_PH1" between R8020 and C8040
add net name "SNB_PH2" between R8021 and C8041
change C8040 to 11G232115214320 from 11G233115214320.
change C8041 to 11G232115214320 from 11G233115214320.
page 84
change JP8402.1 connection to +1.8V from +1.8V0
add net name "5930_VIN" on U8401.5 and U8401.9
change net name "5913_FB" to "5930_FB" on U8401.2
page 88
add net name "SNB_CHG" between R8804 and C8803
add net name "CHG_BST" between R8810 and C8802
change C8803 to 11G232115214320 from 11G233115214320.

5

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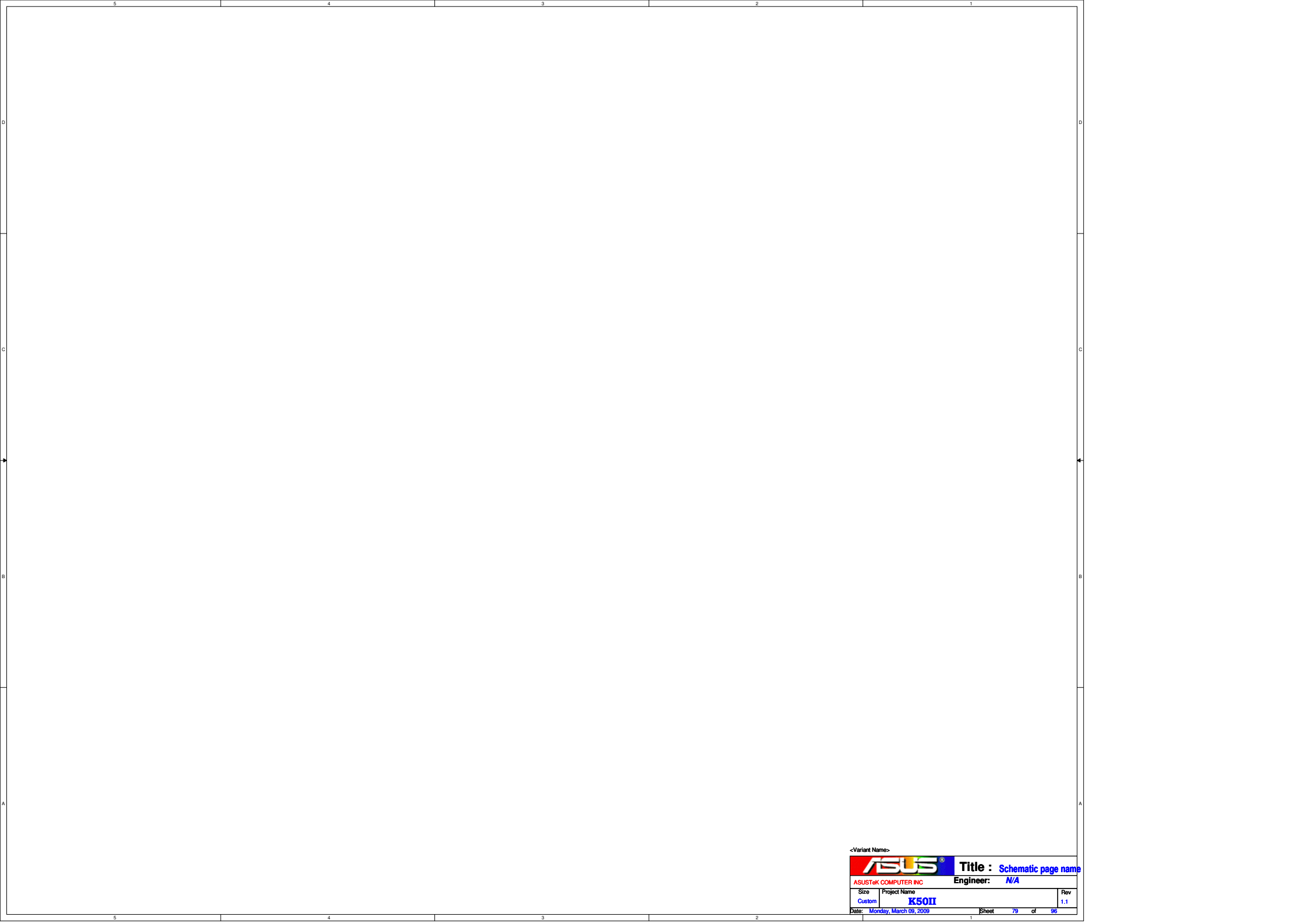
B

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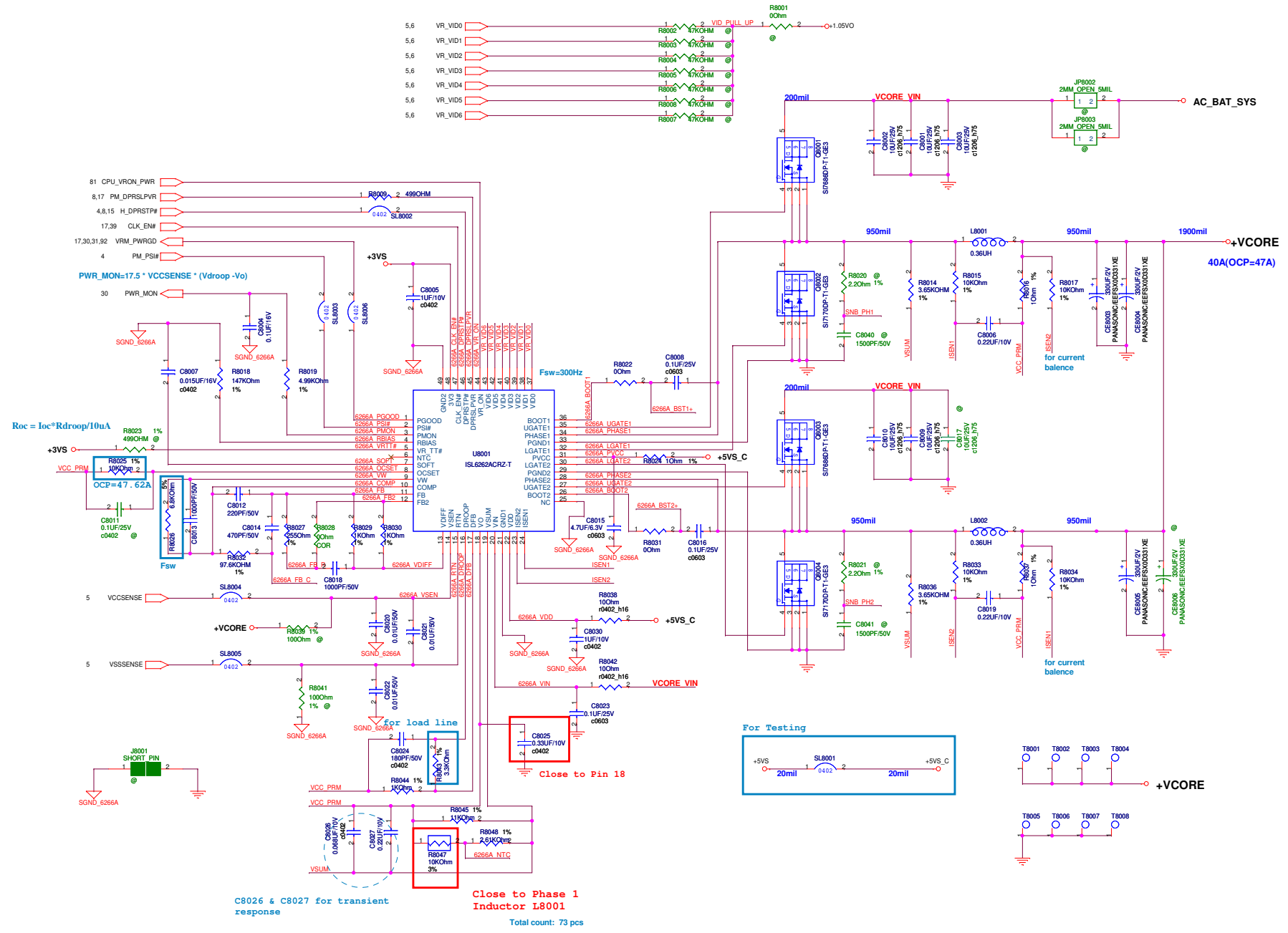
<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	78 of 98



<Variant Name>

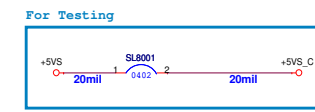
		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K50II	1.1	
Date: Monday, March 09, 2009		Sheet	79 of 96



$Roc = Ioc \cdot Rdroop / 10uA$

$PWR_MON = 17.5 \cdot VCCSENSE \cdot (Vdroop - Vc)$

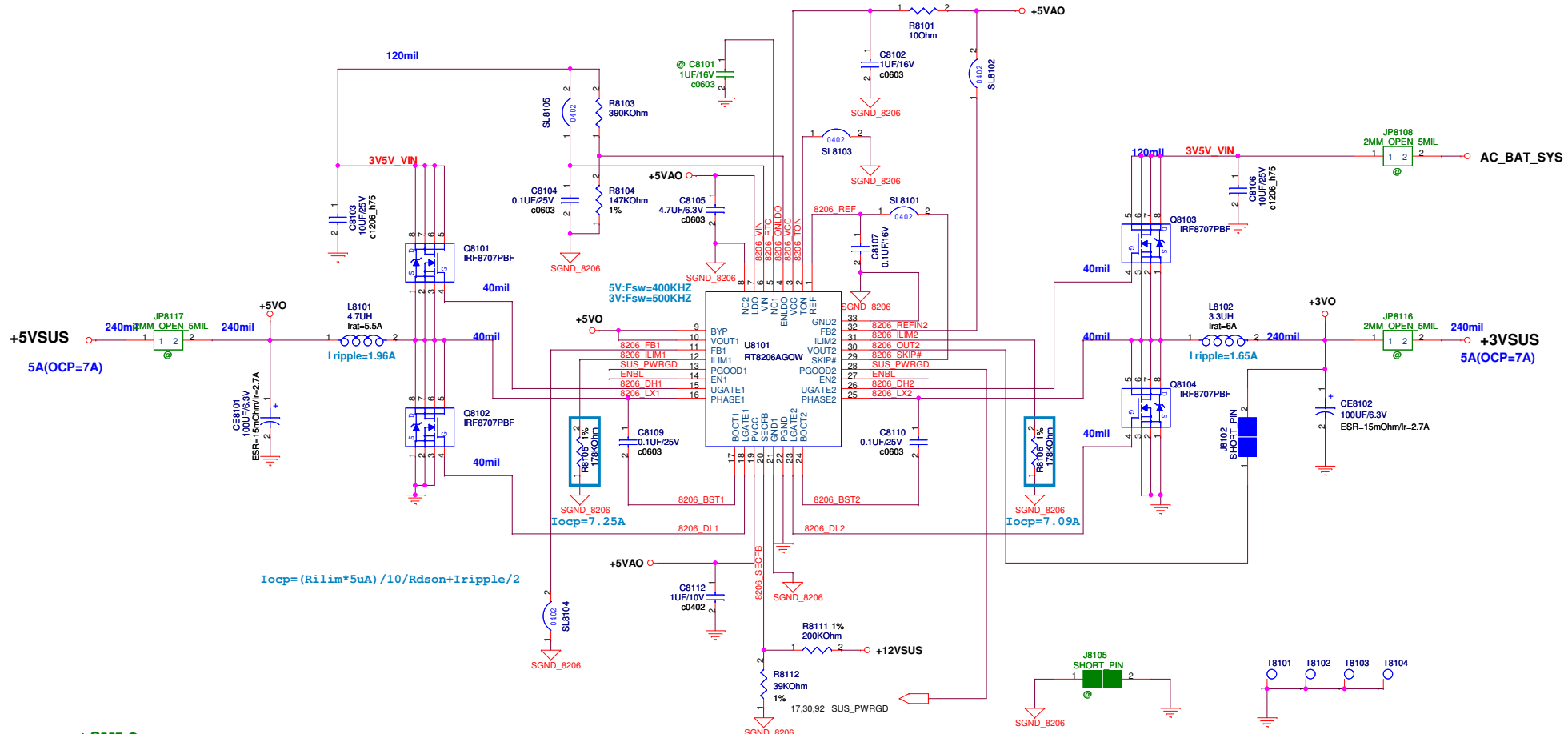
Fsw=300Hz



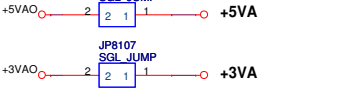
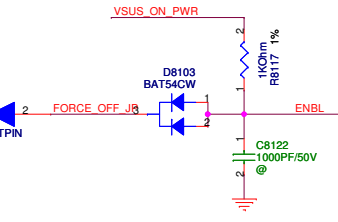
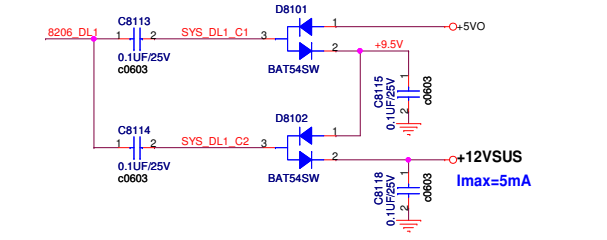
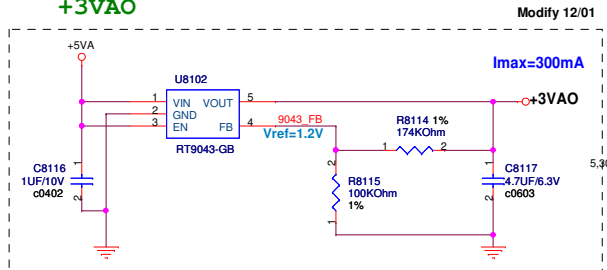
C8026 & C8027 for transient response
Total count: 73 pcs

ASUS		Title : +V CORE	
ASUSTeK COMPUTER INC. NBI		Engineer: Morris	
Size	Project Name	Rev	
Custom	K50	1.0	
Date: Monday, March 03, 2009	Sheet	80	of 96

HS MOS Second source IRF8714
LS MOS Second source IRF8736

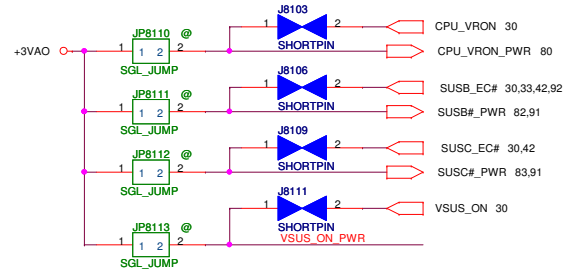


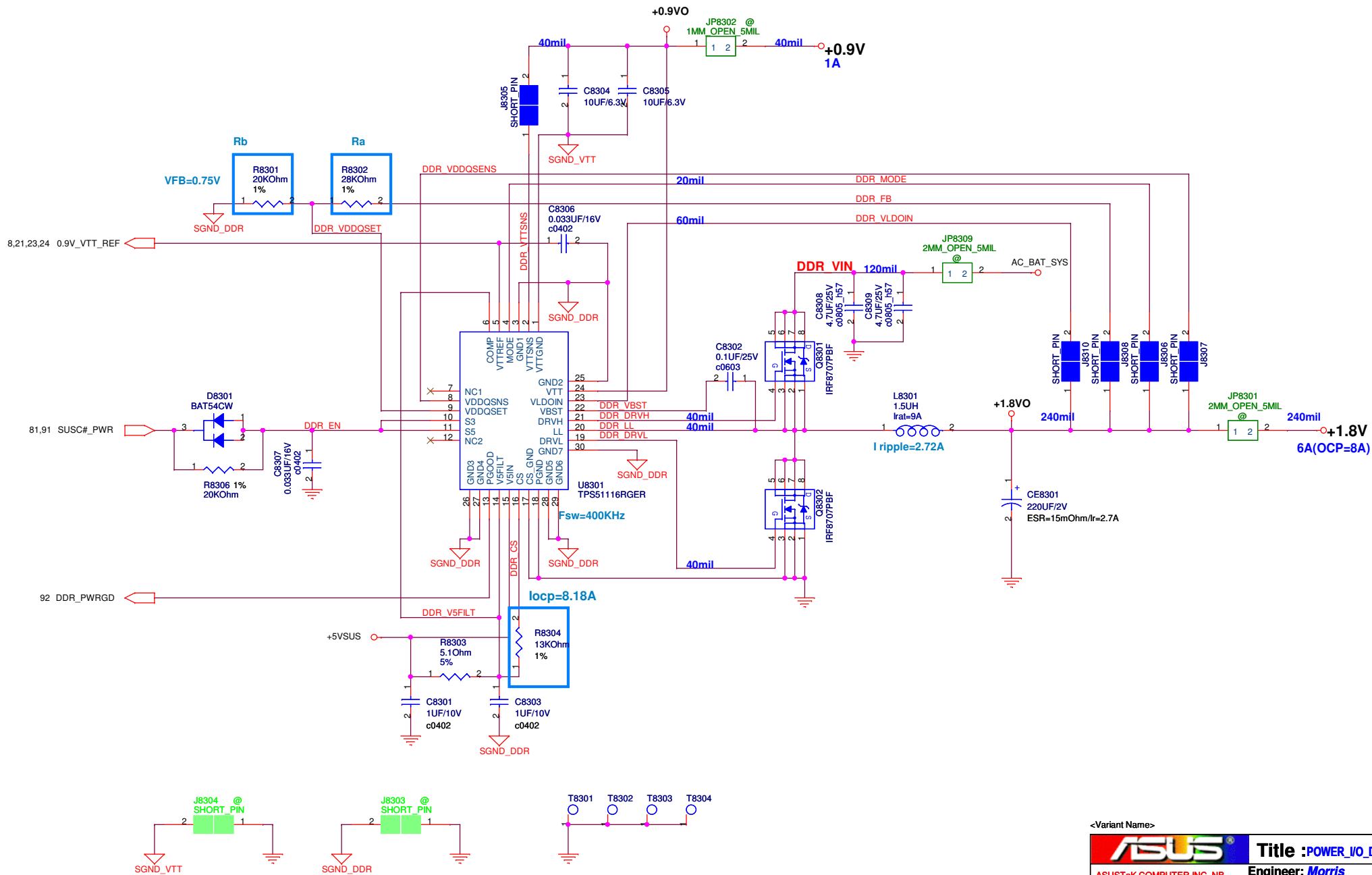
$$I_{ocp} = (R_{ilim} * 5\mu A) / 10 / R_{ds(on)} + I_{ripple} / 2$$



Total count: 44 pcs

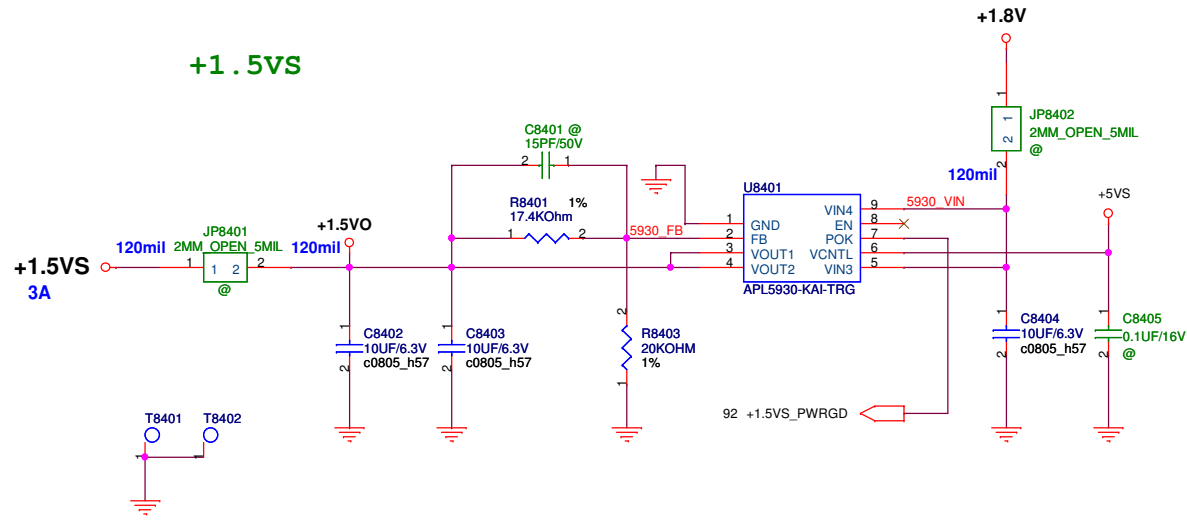
FOR POWER TEST





<Variant Name>

ASUS		Title :POWER_I/O_DDR
ASUSTeK COMPUTER INC. NB		Engineer: Morris
Size B	Project Name K50	Rev 1.0
Date: Monday, March 09, 2009		Sheet 83 of 96



Total count: 7 pcs

<Variant Name>

		Title : POWER_IO_+1.5VS	
ASUSTeK COMPUTER INC. NB		Engineer: Morris	
Size	Project Name		Rev
B	K50		1.0
Date: Monday, March 09, 2009		Sheet	84 of 96

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<Variant Name>



Title :

ASUSTeK COMPUTER INC. NB1

Engineer:

Size	Project Name	Rev
A		1.0

Date: Monday, March 09, 2009

Sheet 85 of 96

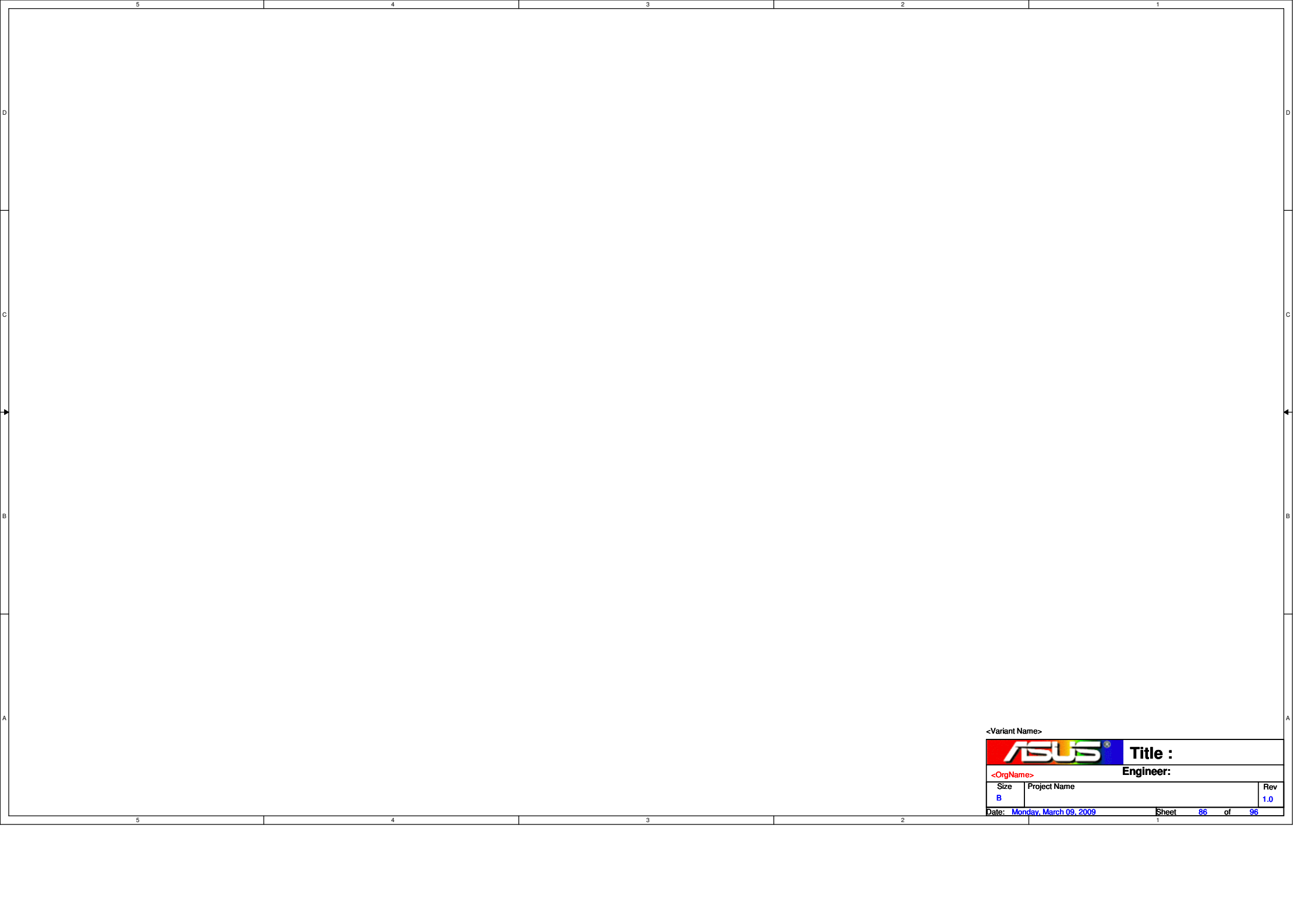
5


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<Variant Name>		
		Title :
<OrgName>		Engineer:
Size	Project Name	Rev
B		1.0
Date: Monday, March 09, 2009		Sheet 86 of 96

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<Variant Name>

		Title :	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Monday, March 09, 2009		Sheet 87 of 96	

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<Variant Name>

		Title :
<OrgName>		Engineer:

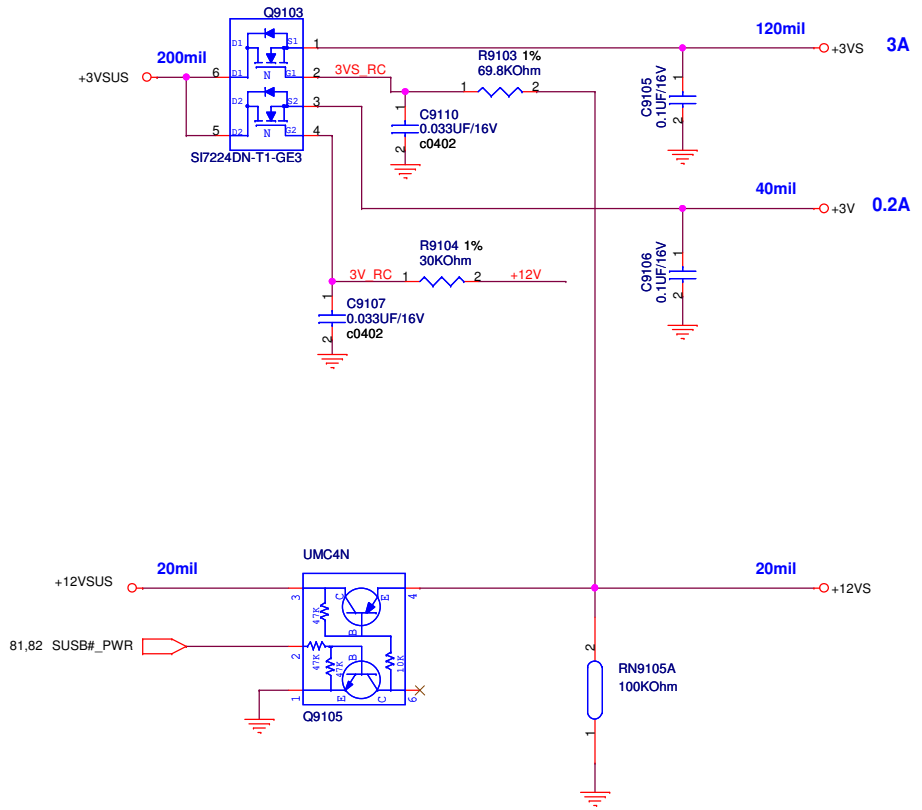
Size	Project Name	Rev
Custom		1.0

BATTERY IN DETECT

<Variant Name>

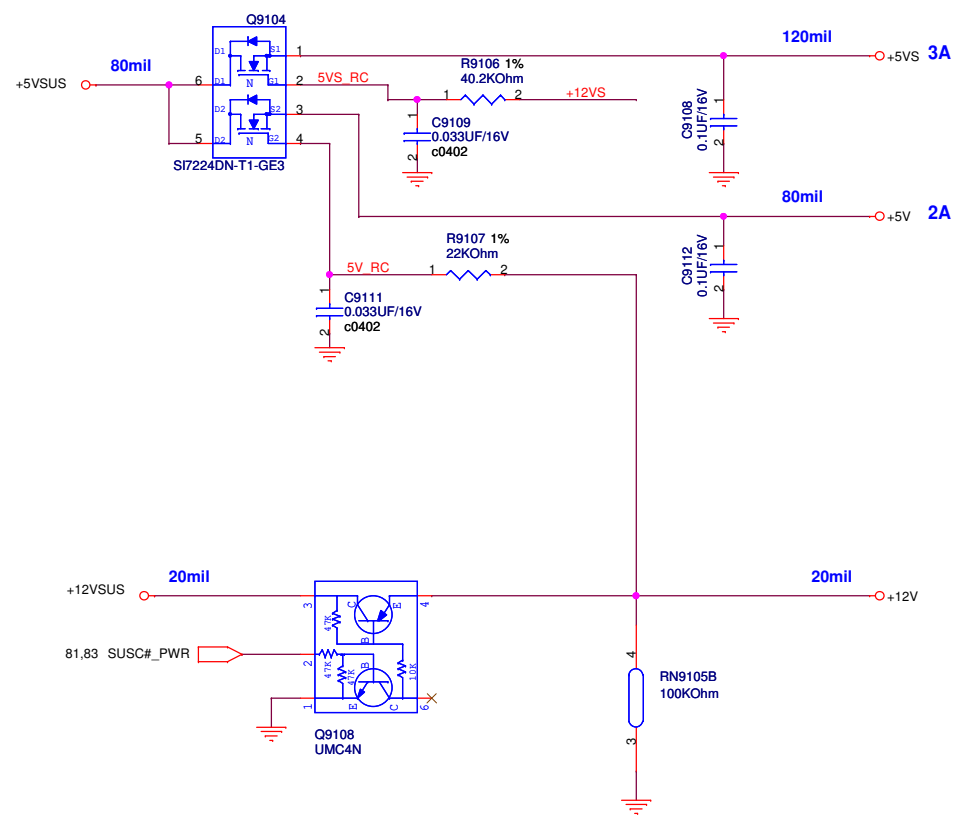
		Title : POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size	Project Name	Rev	
Custom	K50II	1.0	
Date: Monday, March 09, 2009		Sheet	90 of 96

SUSB#_PWR POWER



Total count: 19 pcs

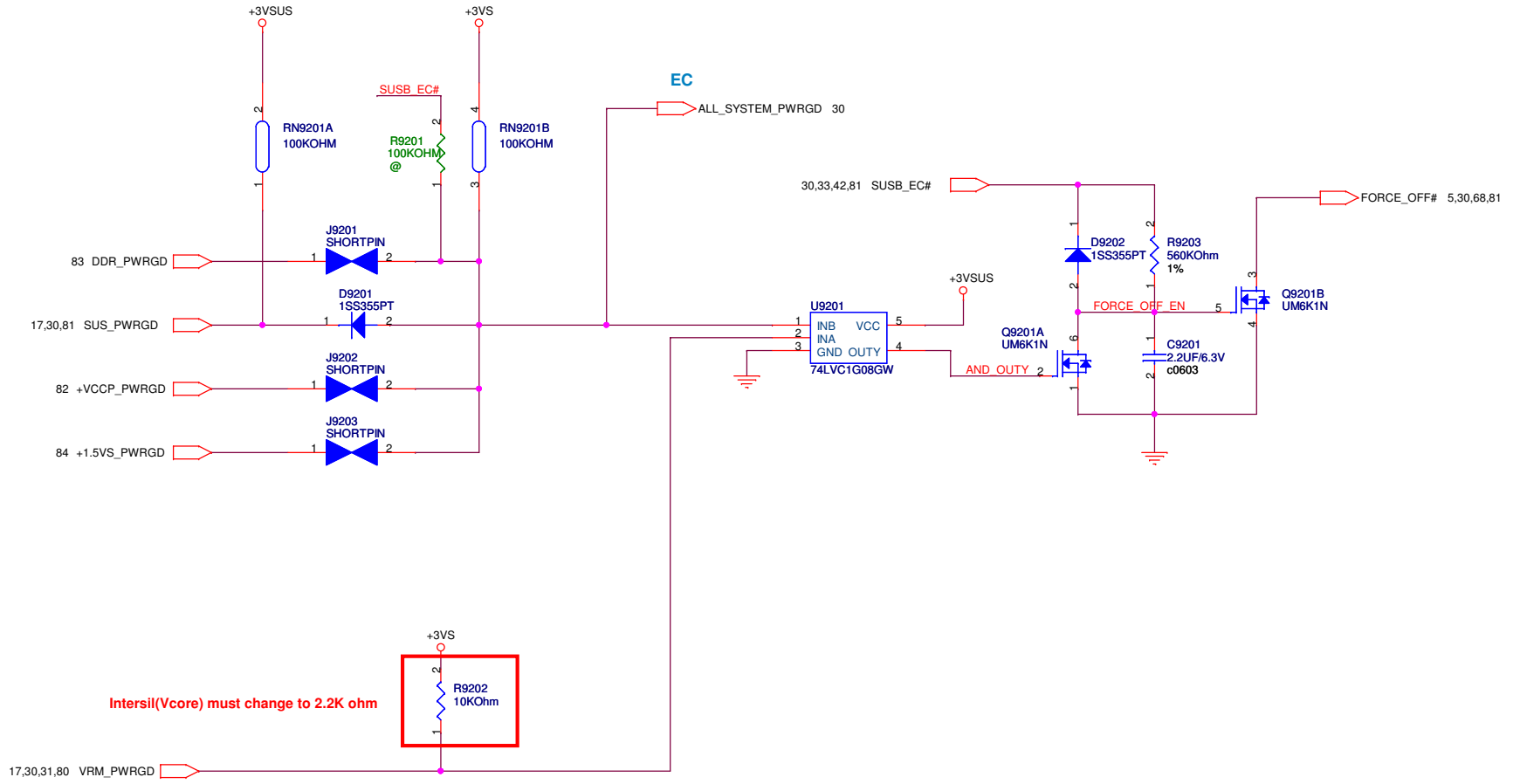
SUSC#_PWR POWER



<Variant Name>

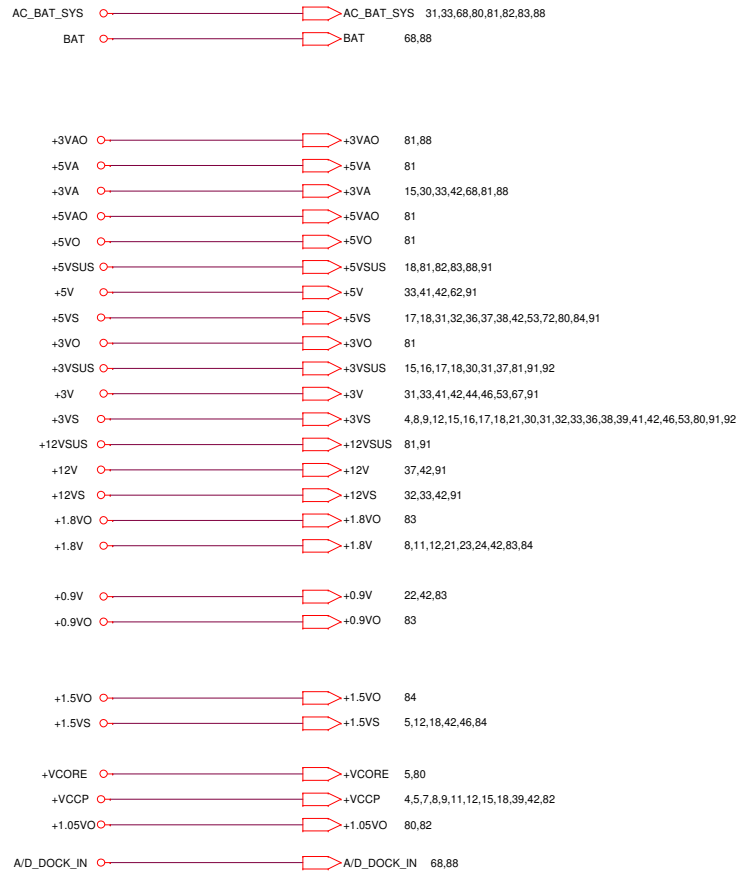
ASUS		Title :POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size	Project Name	Rev	
B	K50	1.0	
Date: Monday, March 09, 2009		Sheet	91 of 96

POWER GOOD DETECTOR




Total count: 8 pcs

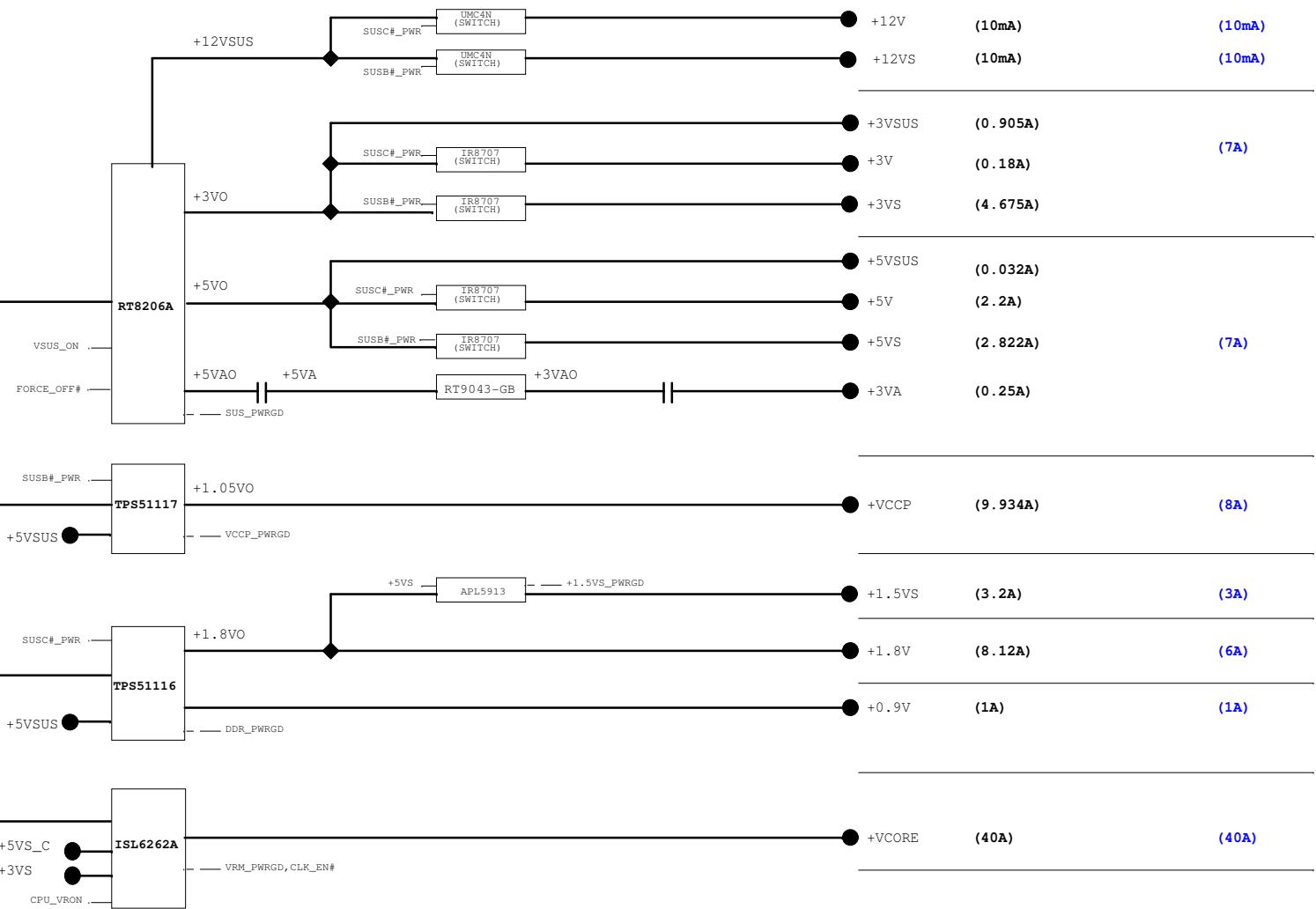
<Variant Name>	
ASUS Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB Engineer: Morris	
Size B	Project Name K50
Date: Monday, March 09, 2009	Rev 1.0
Sheet 92 of 96	



<Variant Name>

		Title : POWER_SIGNAL	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size	Project Name	Rev	
Custom	K50	1.0	
Date: Monday, March 09, 2009		Sheet 93 of 96	

AC_BAT_SYS



K50
Non-IAMT
Design rating

VR_VID0~VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLEPR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON