OSLO

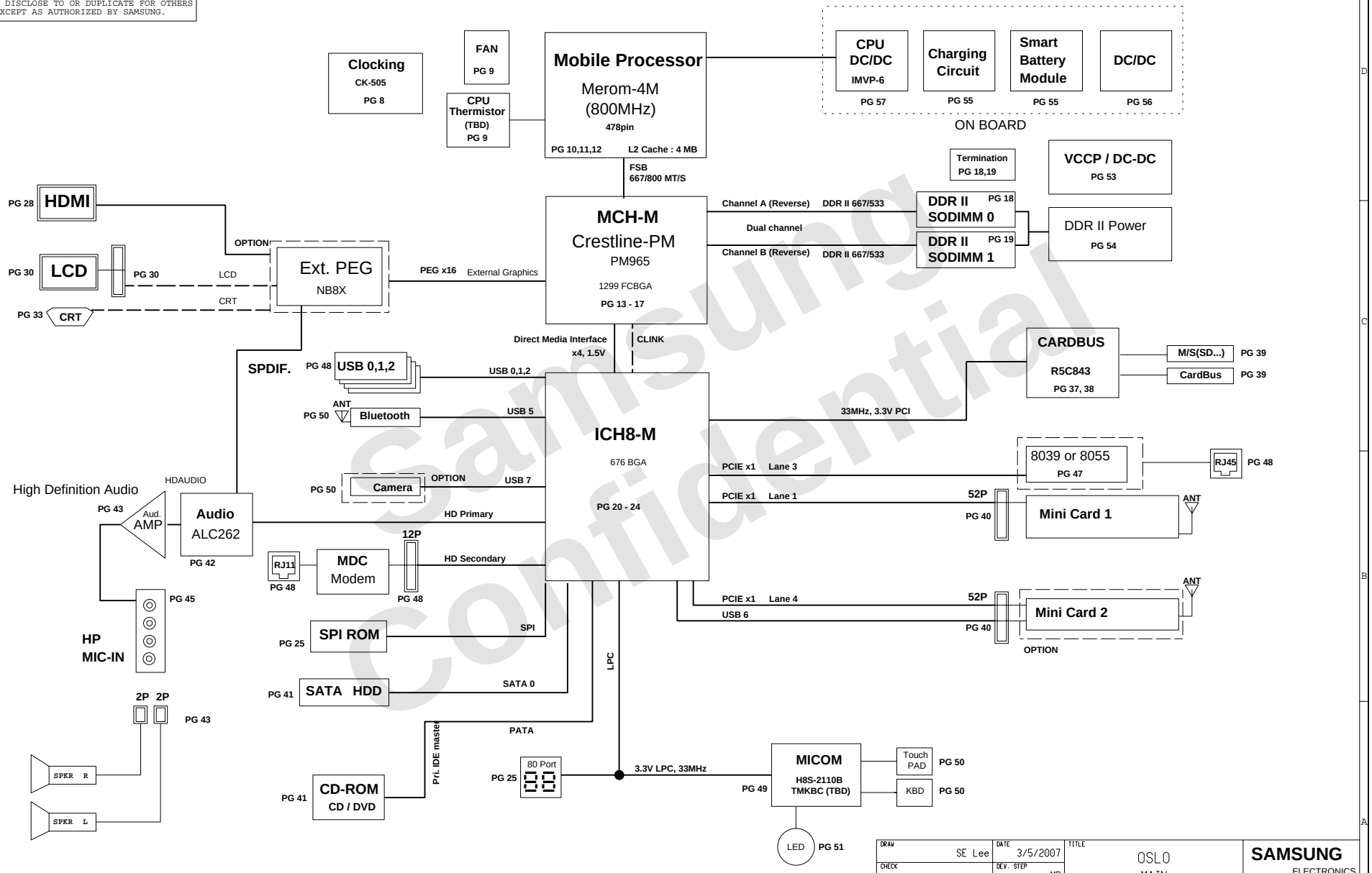
CPU : Intel Merom-4M (800/667 MHz)
Chip Set : Intel Crestline & ICH8-M
Remarks : Mobility Platform

Model Name : SANTA ROSA STD
PBA Name : MAIN
PCB Code : BA41-#####A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2007.03.02

DESIGN	CHECK	APPROVAL

■ ***Owner : SEC Mobile R & D*** ***Signature :*** ***X***

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO MAIN COVER	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		PART NO.: BA41-#####A
APPROVAL	REV: 1.0		
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 1 OF 60	



DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 2 OF 60	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	SYSTEM PORT 2
3	NC
4	NC
5	Bluetooth
6	Mini PCI Express 2
7	Camera
8	NC
9	NC

PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	LOM
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

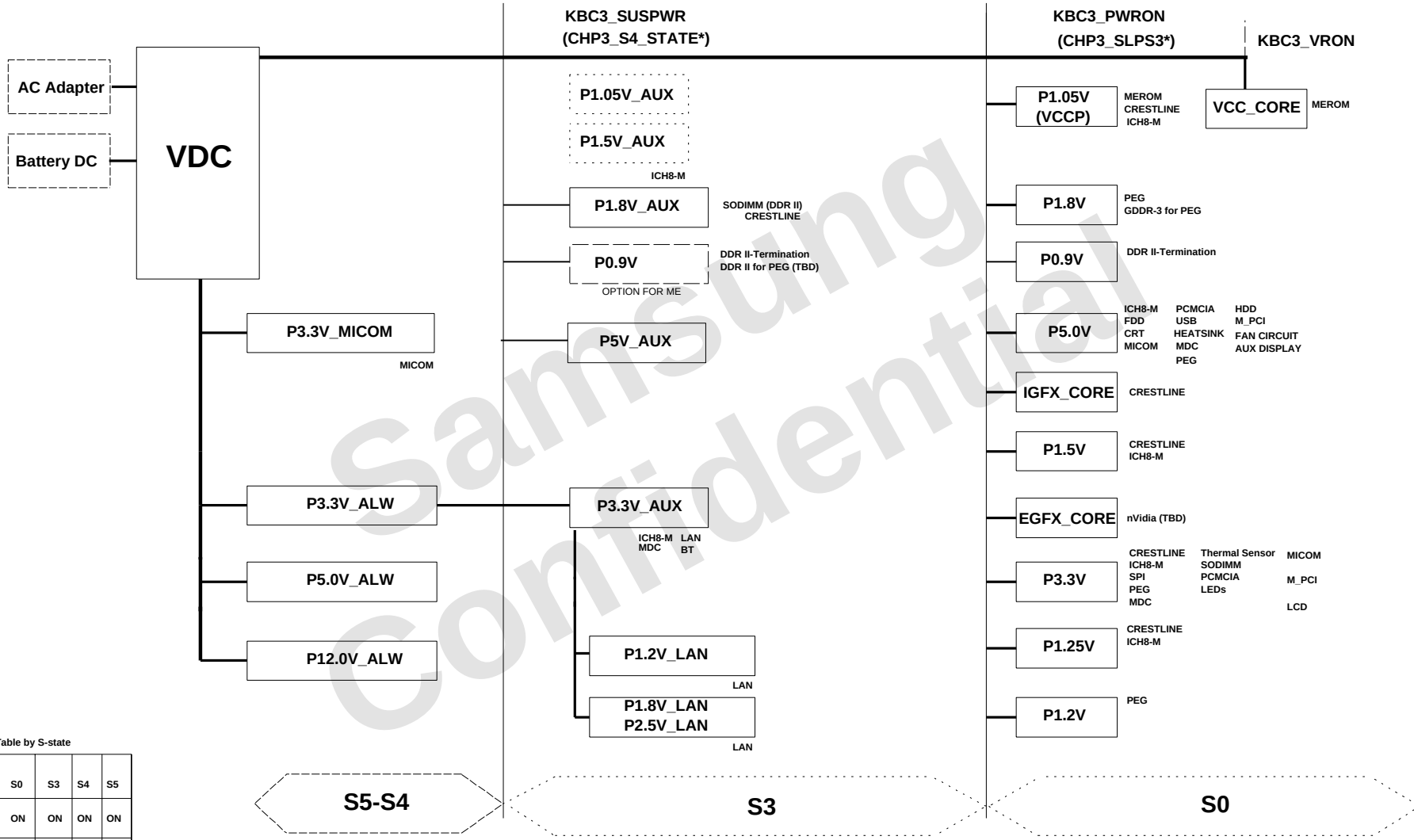
Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

REVISION HISTORY

See rev notes for more information.

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO MAIN BOARD INFO	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 3 OF 60	

POWER DIAGRAM



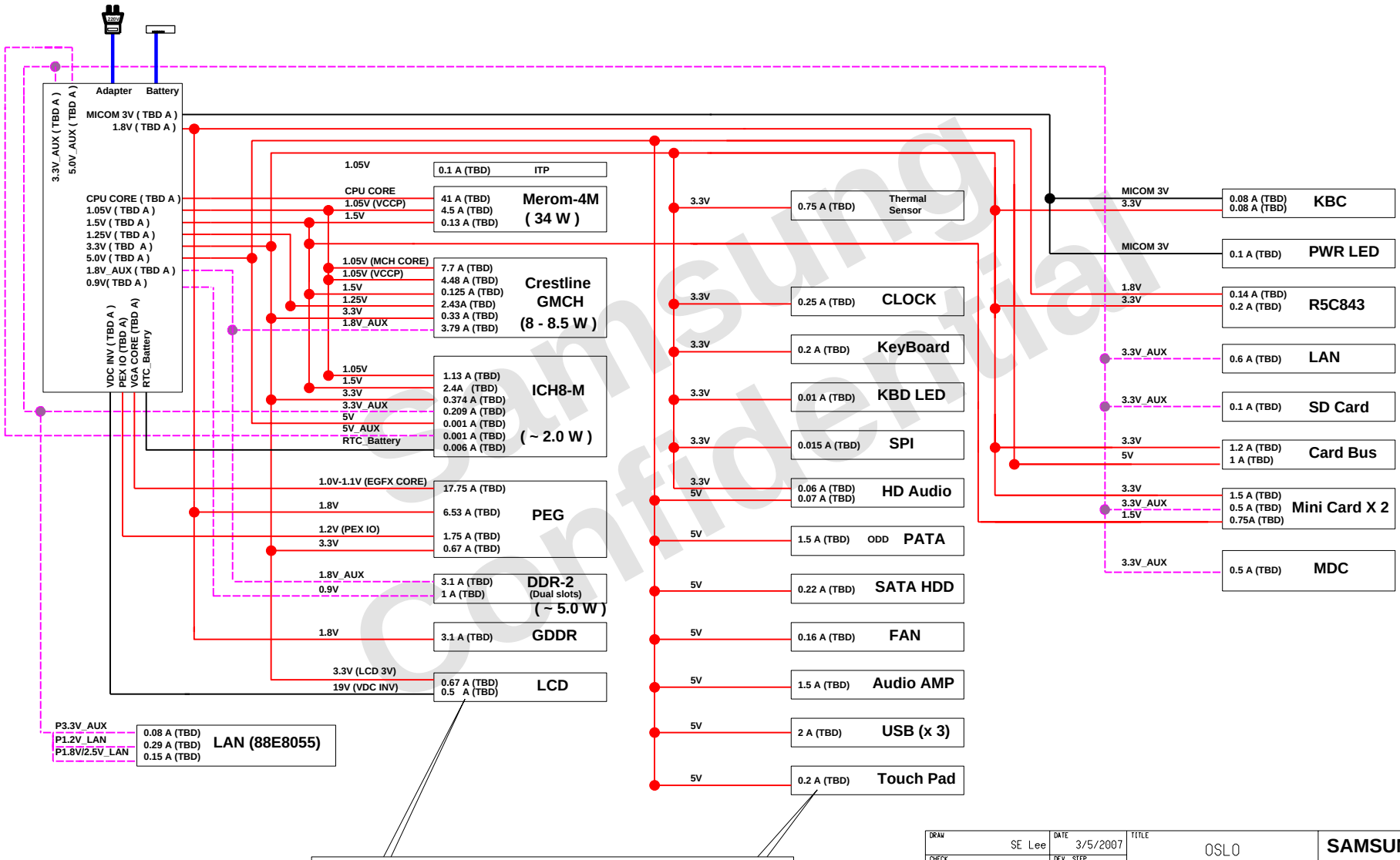
Power On/Off Table by S-state

Rail / State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 4 OF 60	

POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO MAIN POWER RAILS	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 5 OF 60	

POWER SEQUENCE

Rev. 0.7

Host Boot / ME Off
(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot
(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

RTC Battery — PRTC_BAT, CHP3_RTCRST# — 1

POWER S/W — 4) POWER_SW*

KBC — 7
- 110ms Delay — 5
- 8) CHP3_SLPS5#/4#/3#
- 7) KBC3_RSMRST#
- 17) KBC3_PWRGD
- 15)VRM3_CPU_PWRGD
- 5) KBC3_SUSPWR
- 9) KBC3_PWRON
- 13) KBC3_VRON

ICH8-M — Sheet 22-25
- 6) P3.3V_AUX
- PRTC, PRTC — 16
- 10-1) ICH_CORE (P1.05V)
- 7) P1.05V_AUX
- 7) P1.5V_AUX
- LAN100_SLP
- INTVRMEN
- VRMPWRGD
- PWROK
- CL_PWROK
- 16) CLK3_PWRGD
- 17) KBC3_PWRGD
- 17) KBC3_PWRGD
- 15)VRM3_CPU_PWRGD
- 18) CPU1_PWRGDCPU — 18
- 19) PLT3_RST* — 19
- 19) PCI3_RST*

CK-505 — Sheet 8
- 16-1) Clock Running

CPU VRM — DC/DC B'd
- 15) VRM3_CPU_PWRGD — 15
- 11) VCCP3_PWRGD (GM-model)
- 12)GCORE3_PWRGD (PM-model)
- 13) KBC3_VRON (Back-up)
- 14) VCC_CORE — 14

CPU — (Test Option) — Sheet 10-12
- 10-1) P1.5V
- 10-1) P1.05V — 20
- 20) CPU1_CPURST*

GMCH — Sheet 15-19
- 17) KBC3_PWRGD
- 17) KBC3_PWRGD
- PWROK
- CL_PWROK
- 19) PLT3_RST*
- 6) P1.8V_AUX
- 10-1) P3.3V
- 10) P1.05V (IGFX_CORE)

3) P3.3V_MICOM

Adapter / Battery — AC_DC / Battery — MAX 1909
- 2) VDC — 2
- 2-1) P12.0V_ALW

8) KBC3_SUSPWR
9) KBC3_PWRON

SC486 — 10
- 10) P1.5V
- 10) P5.0V

SC4435
- 10) P5.0V
- 9-1

DDR2 POWER — SC486 — Sheet 50 — 6
- 10) P5.0V
- 2) VDC
- 5) KBC3_SUSPWR
- 6) P1.8V_AUX
- 6) MEM1_VREF
- 10-2) 0.9V

9-1) KBC3_PWRON_INV#

MAX 8734 — P3.3V_AUX & P5V_AUX — 3
- P5.0V_ALW
- 6) P5.0V_AUX
- P3.3V_MICOM — 6
- 6) P3.3V_AUX

ISL6227
- 2) VDC
- 9) KBC3_PWRON
- 10) P1.25
- 10) P1.05V (IGFX_CORE)
- 11) VCCP3_PWRGD — 11

PM-model only

ADP3209 — 12
- 11-1) GFX_CORE
- 12)GCORE_PWRGD

9-1
- 6) P3.3V_AUX
- 9-1) KBC3_PWRON_INV#
- 6) P1.8V_AUX
- 10-1) P1.25

FDS6680A — Sheet 40
- 10-1) P3.3V

FDS6680A — Sheet 40
- 10-1) P1.8V

FDC653N — Sheet 40
- 10-1) P1.2V

DDR2 Memory — Sheet 20-21
- 6) P1.8V_AUX
- 10-2) P0.9V

PCIe Devices — 19
- 10-1) P3.3V
- 10-1) P1.8V
- 10) P1.5V

PEG
- 10-1) P1.2V
- 2) VDC
- 10-1) P3.3V

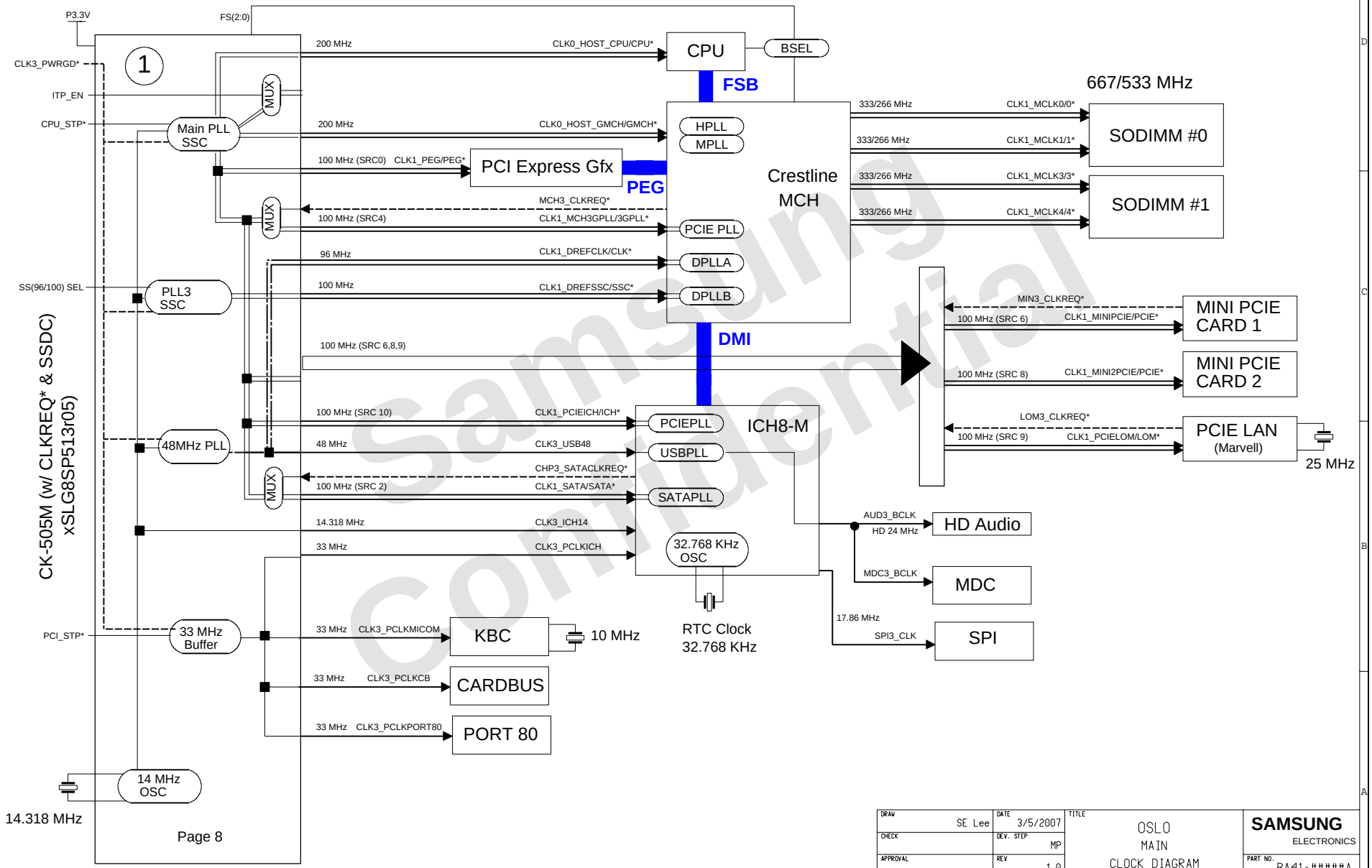
PCI Devices
- 10-1) P3.3V
- 10-1) P1.8V
- 10) P1.5V
- 19) PCI3_RST*

LOM Marvell — Sheet 46-47
- 6-1) P1.2V_LAN
- 6-1) P1.8V/P2.5V_LAN

BCP69 — Sheet 46

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 6 OF 60	

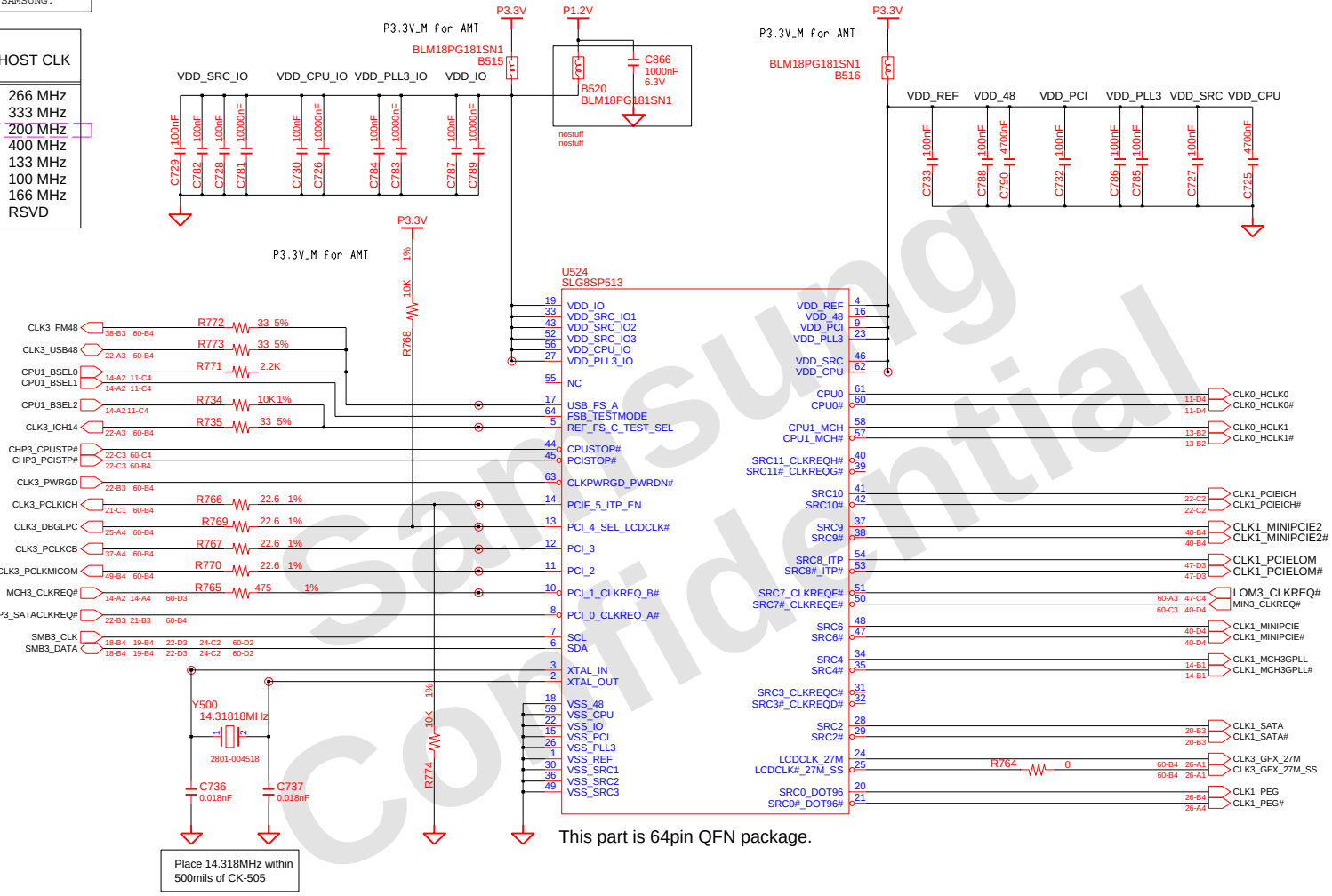
CLOCK DISTRIBUTION Rev. 0.5



Page 8

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO MAIN CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 7 OF 60	

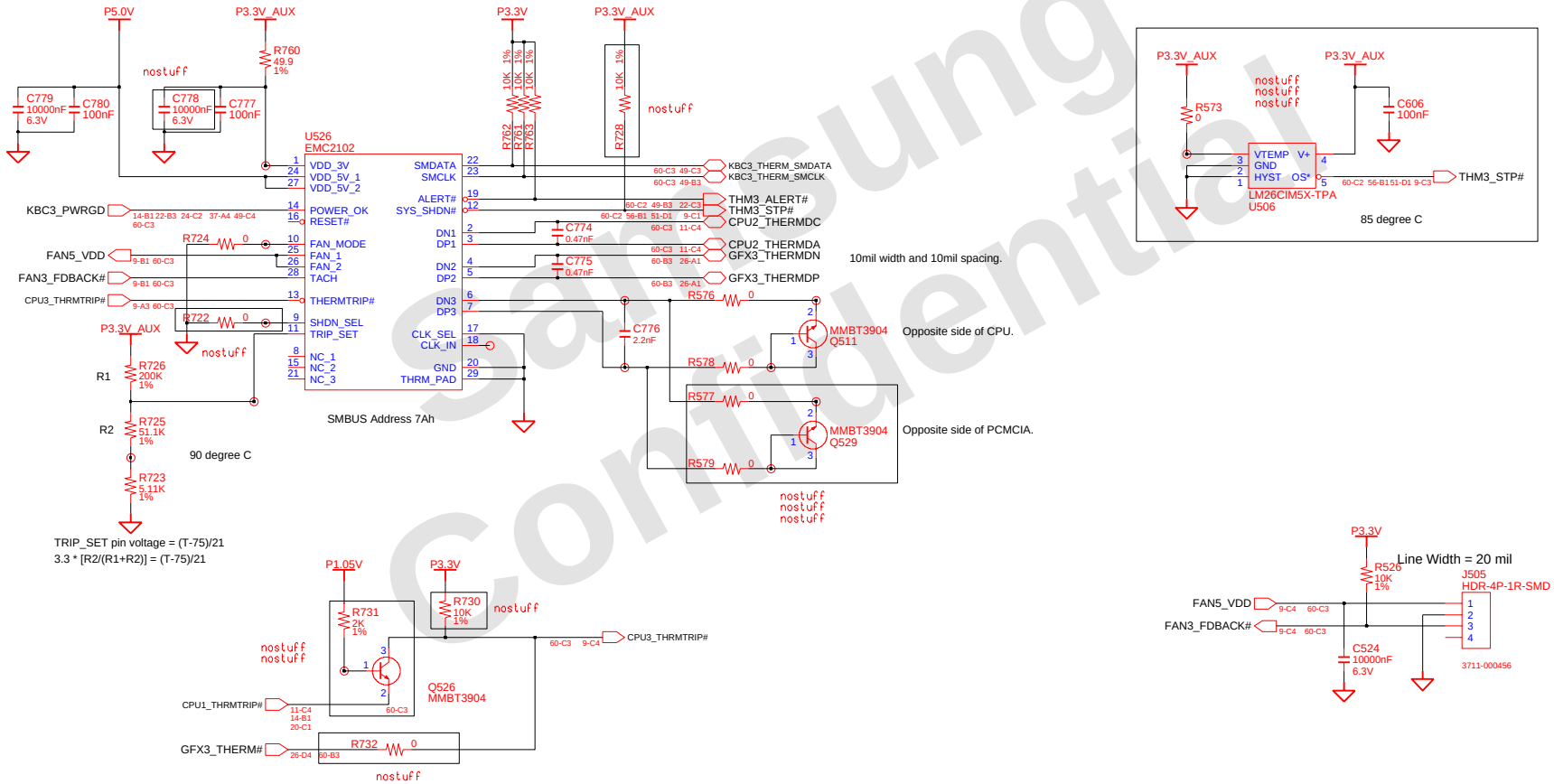
FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



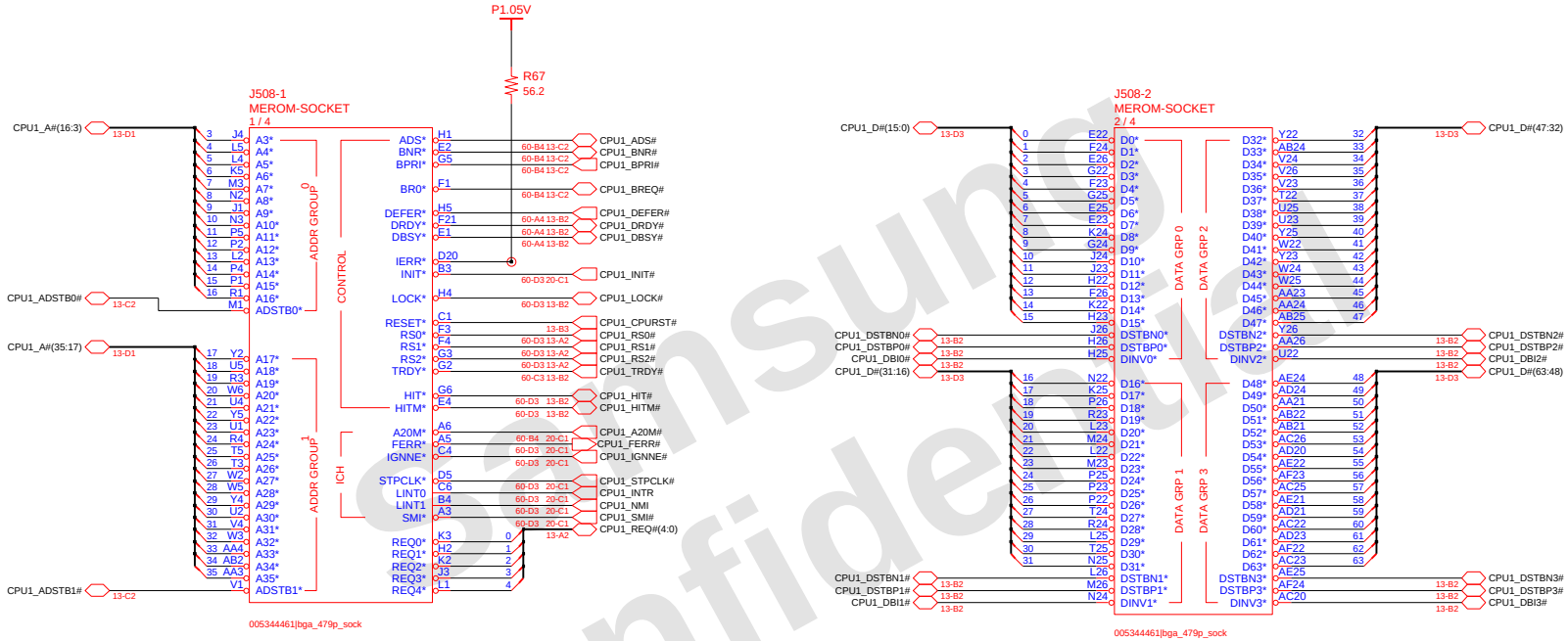
CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	LOM	SRC8

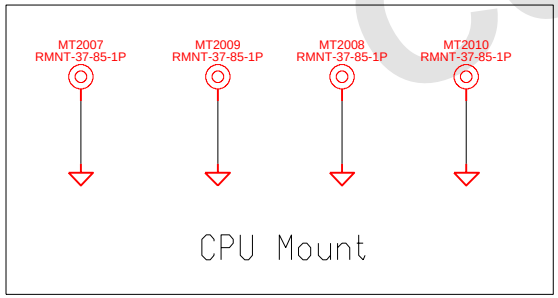
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO CLOCK GENERATOR CK-505	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 8 OF 60	

THERMAL SENSOR & FAN CONTROL

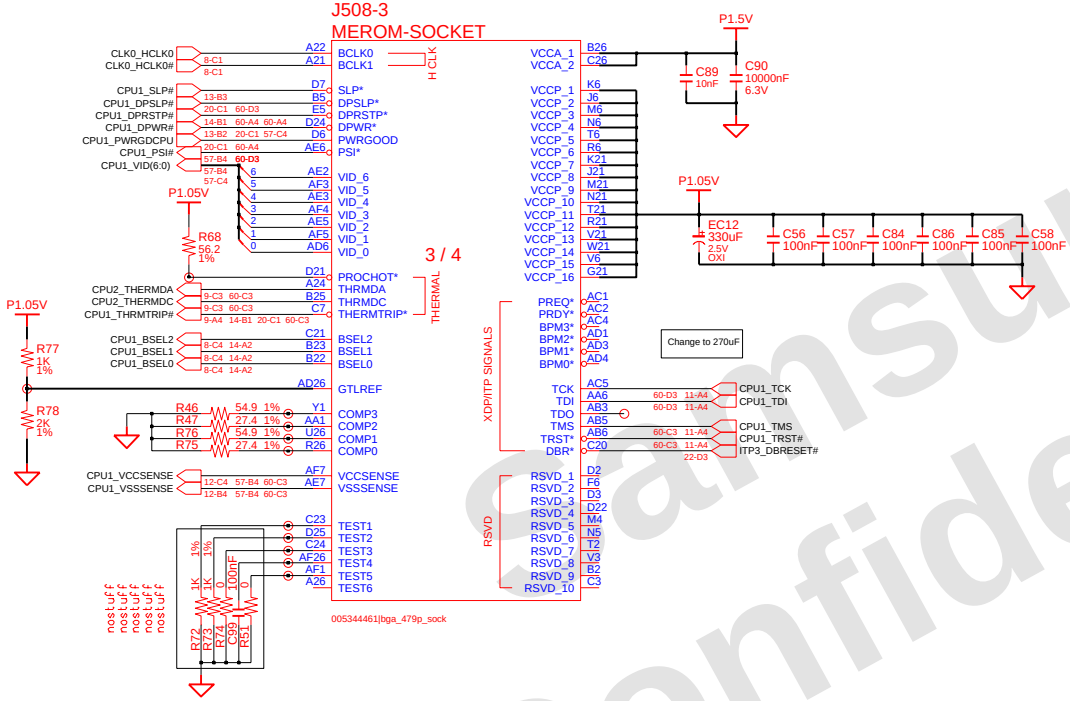


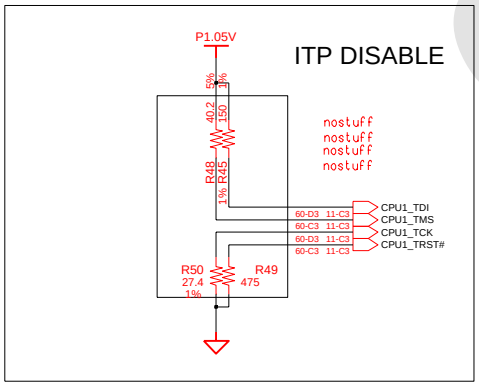
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO THERMAL BLOCK THERMAL & FAN CONTROL	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 9 OF 60	





DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO CPU MEROM (1/3)	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 10 OF 60	





CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active

DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp

DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

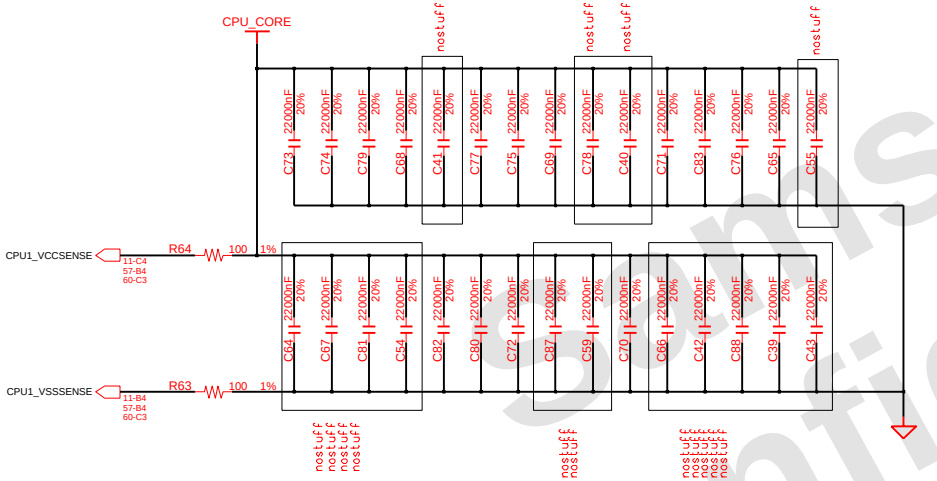
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

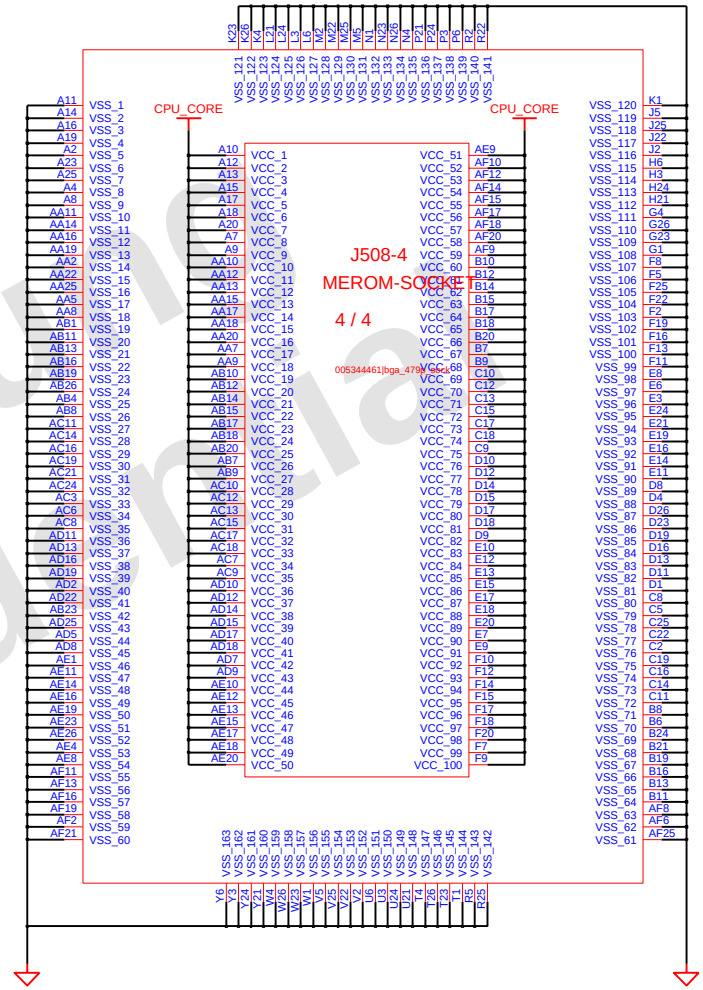
COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

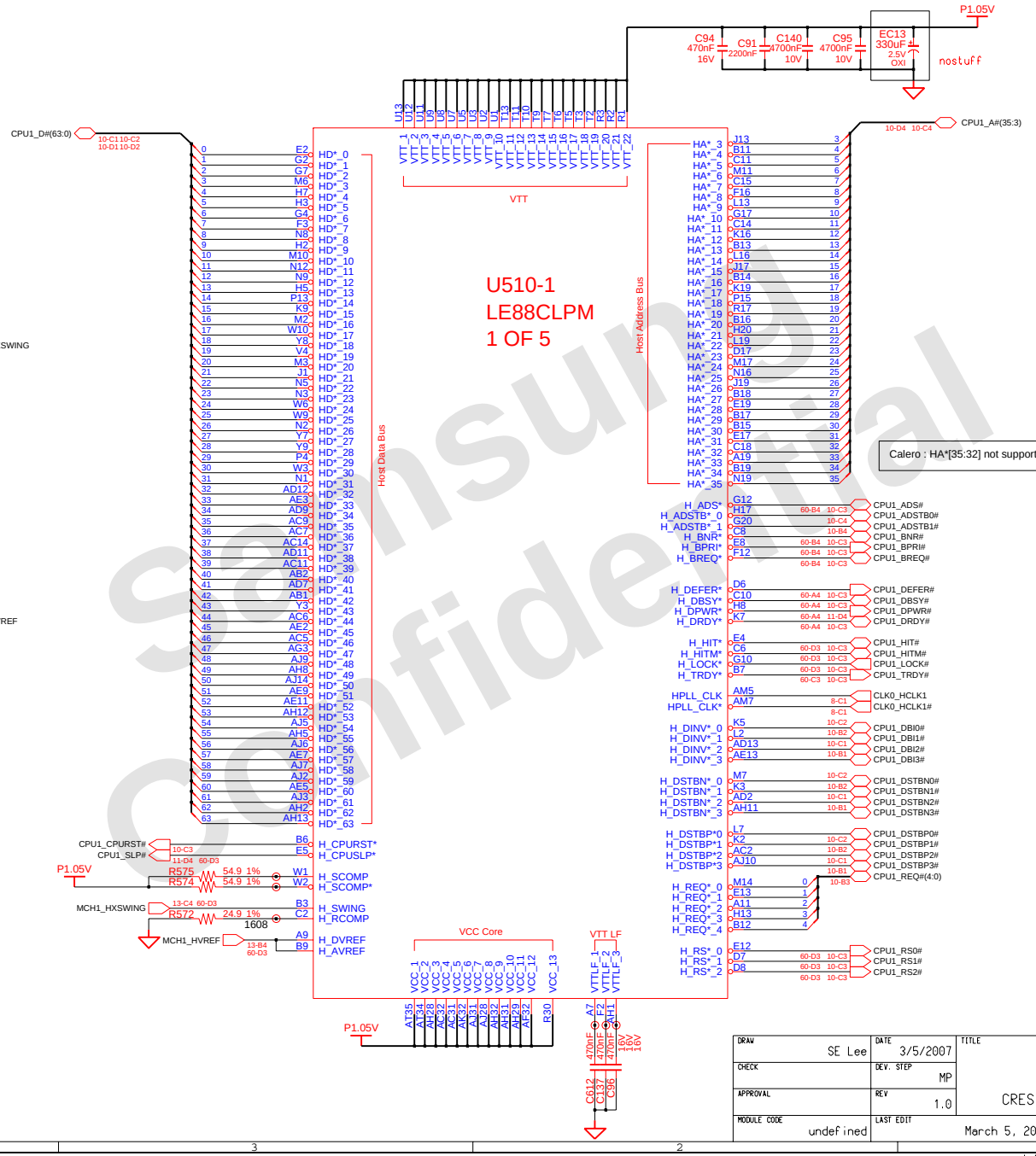
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO CPU MEROM (2/3)	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 11 OF 60	



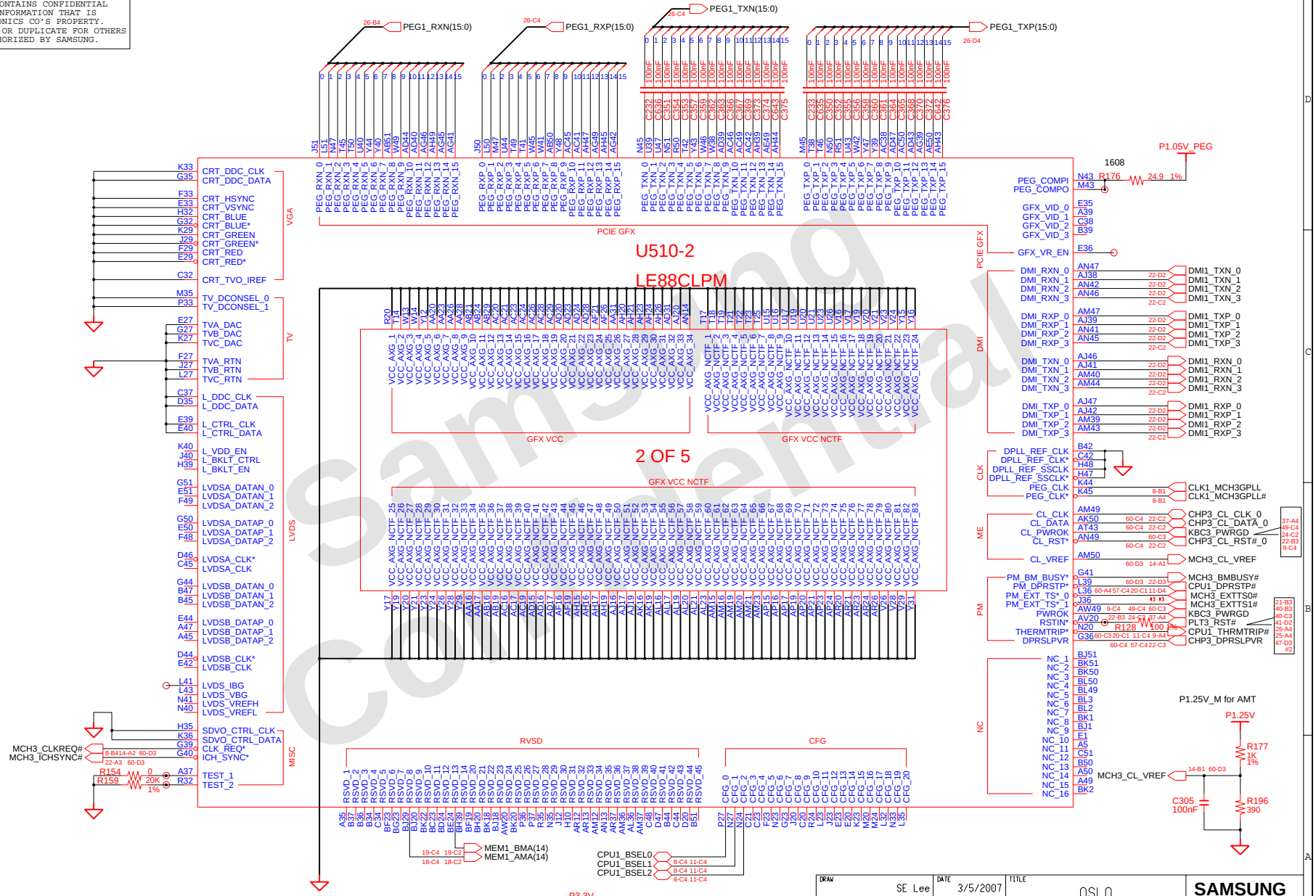
6x 330 uF : CPU VR side



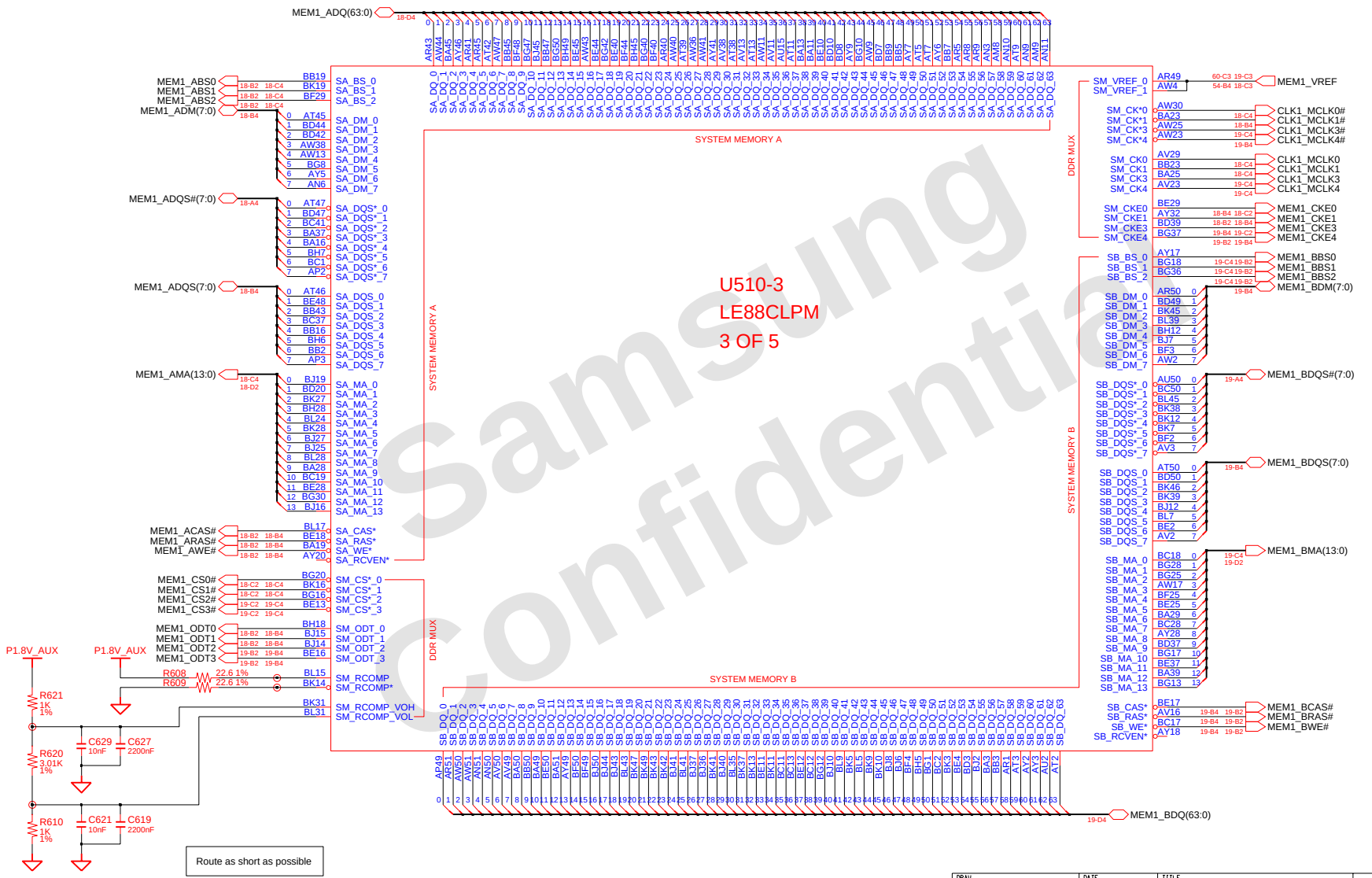
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO CPU MEROM (3/3)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 12 OF 60	



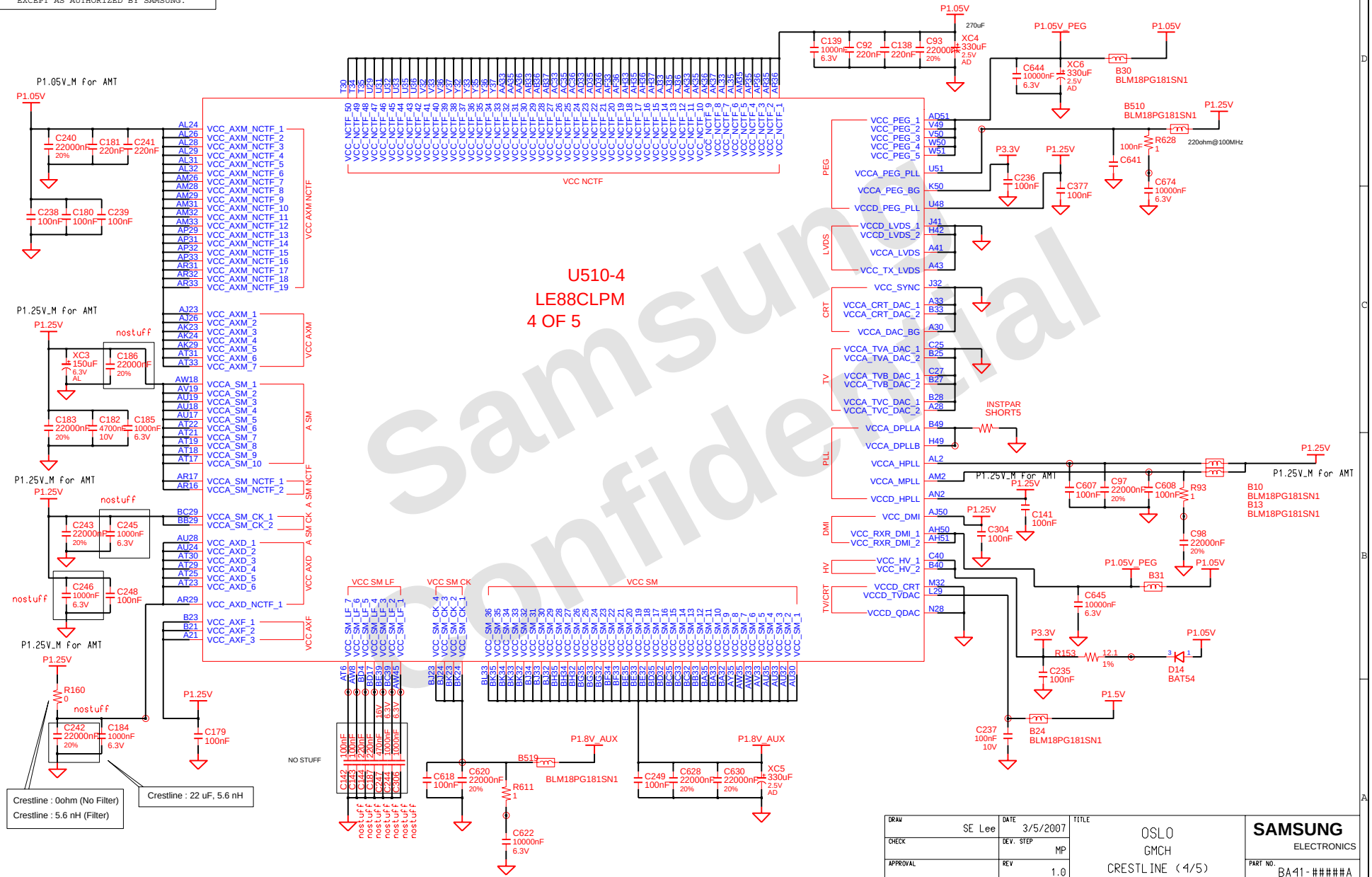
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO GMCH CRESTLINE (1/5)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 13 OF 60	



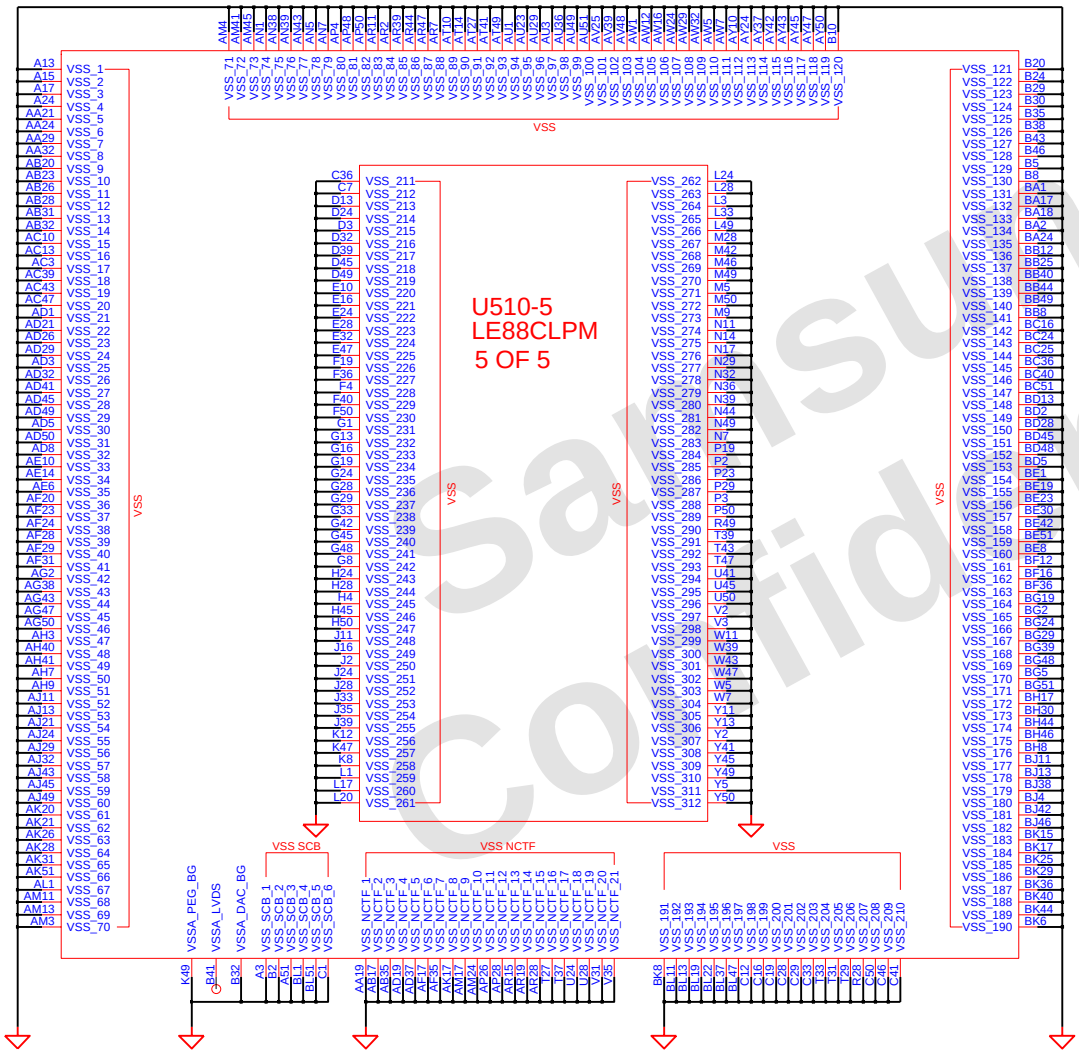
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO GMCH CRESTLINE (2/5)	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		PART NO.: BA41-######A
APPROVAL:	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 14 OF 60	



DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO GMCH CRESTLINE (3/5)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		PART NO.: BA41-#####A
APPROVAL	REV: 1.0		
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 15 OF 60	



DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO GMCH CRESTLINE (4/5)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		PART NO.: BA41-######A
APPROVAL	REV: 1.0		
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 16 OF 60	

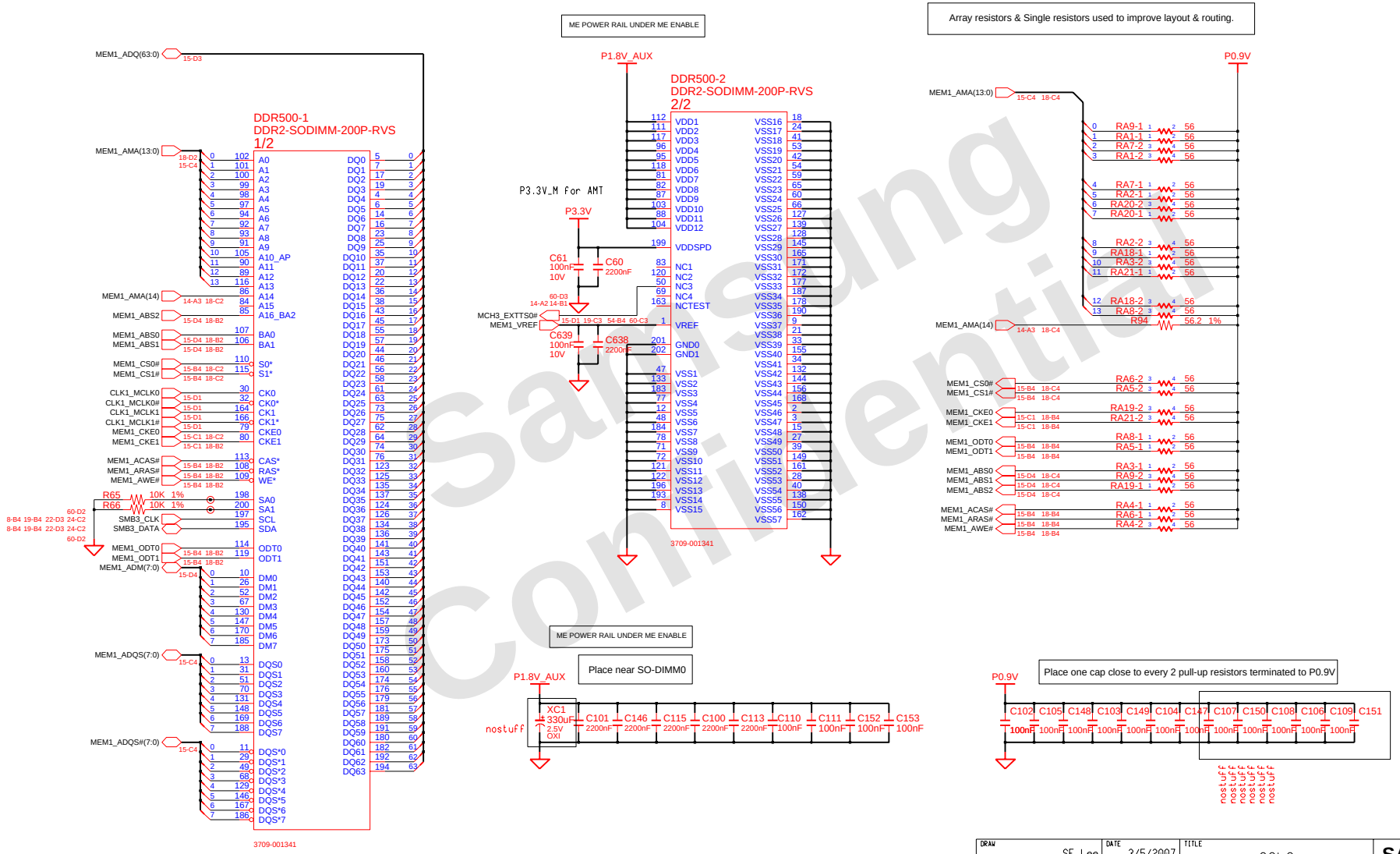


POCAFEB-11 Only (Remove in MP Model)

Current Setting (def. : default Option)		
CFG#	Low	High
CFG(5)	DMIx2	**DMIx4 (def.)**
CFG(6)	Reserved	**DDR-II (def.)**
CFG(7)	DT/Transportable	**Mobile CPU (def.)**
CFG(9)	PEG Reversal	**Normal**
CFG(16)	Dynamic ODT Disabled	**Dynamic ODT Enabled (def.)**
CFG(18)	**VCC 1.05V (def.)**	VCC 1.5V
CFG(19)	**DMI Lane Normal**	DMI Lane Reversal
CFG(20)	**SDVO or PCIE X1 Only(def.)**	SDVO and PCIE X1 Simultaneously

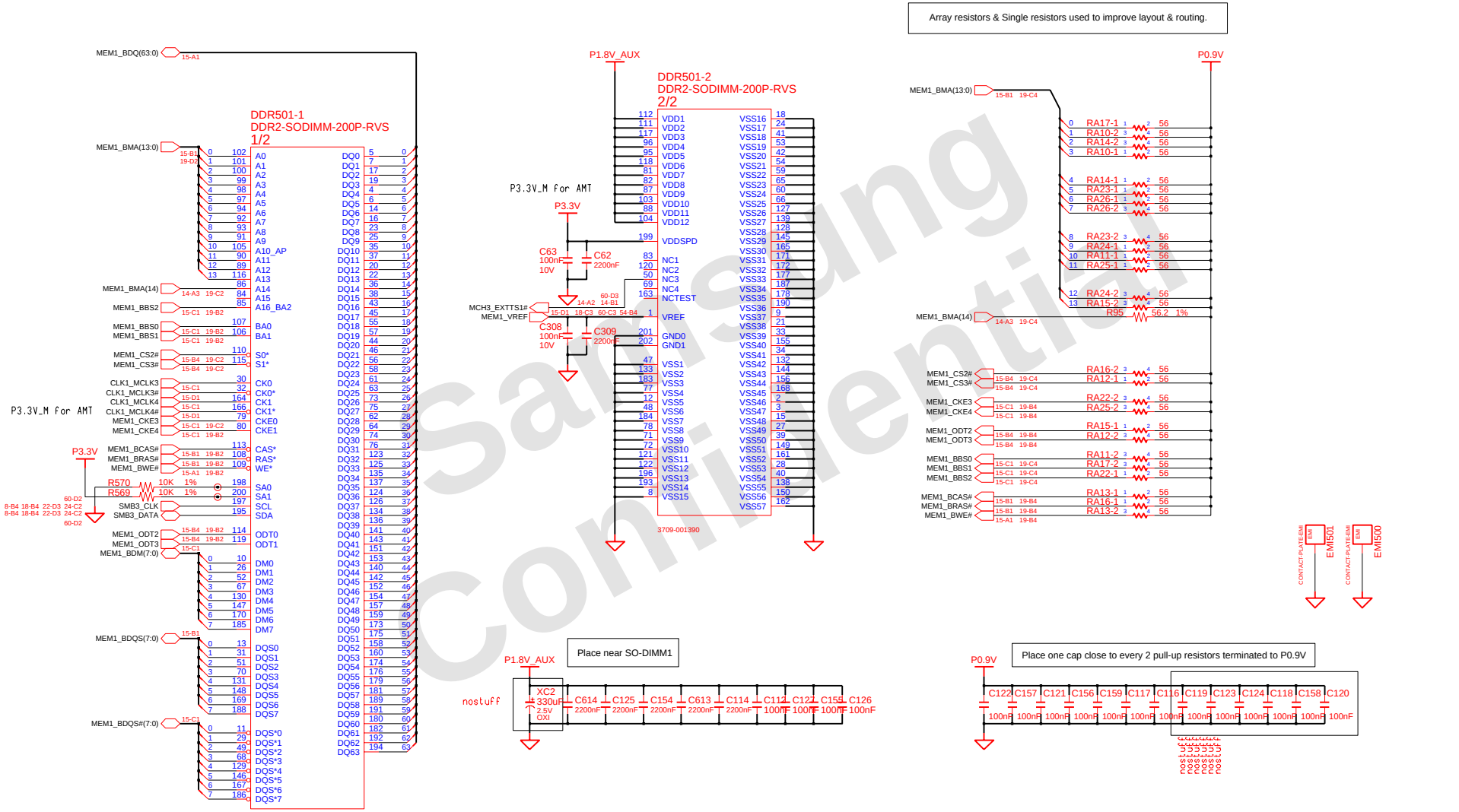
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO GMCH CRESTLINE (5/5)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 17 OF 60	

DDR SO-DIMM #0

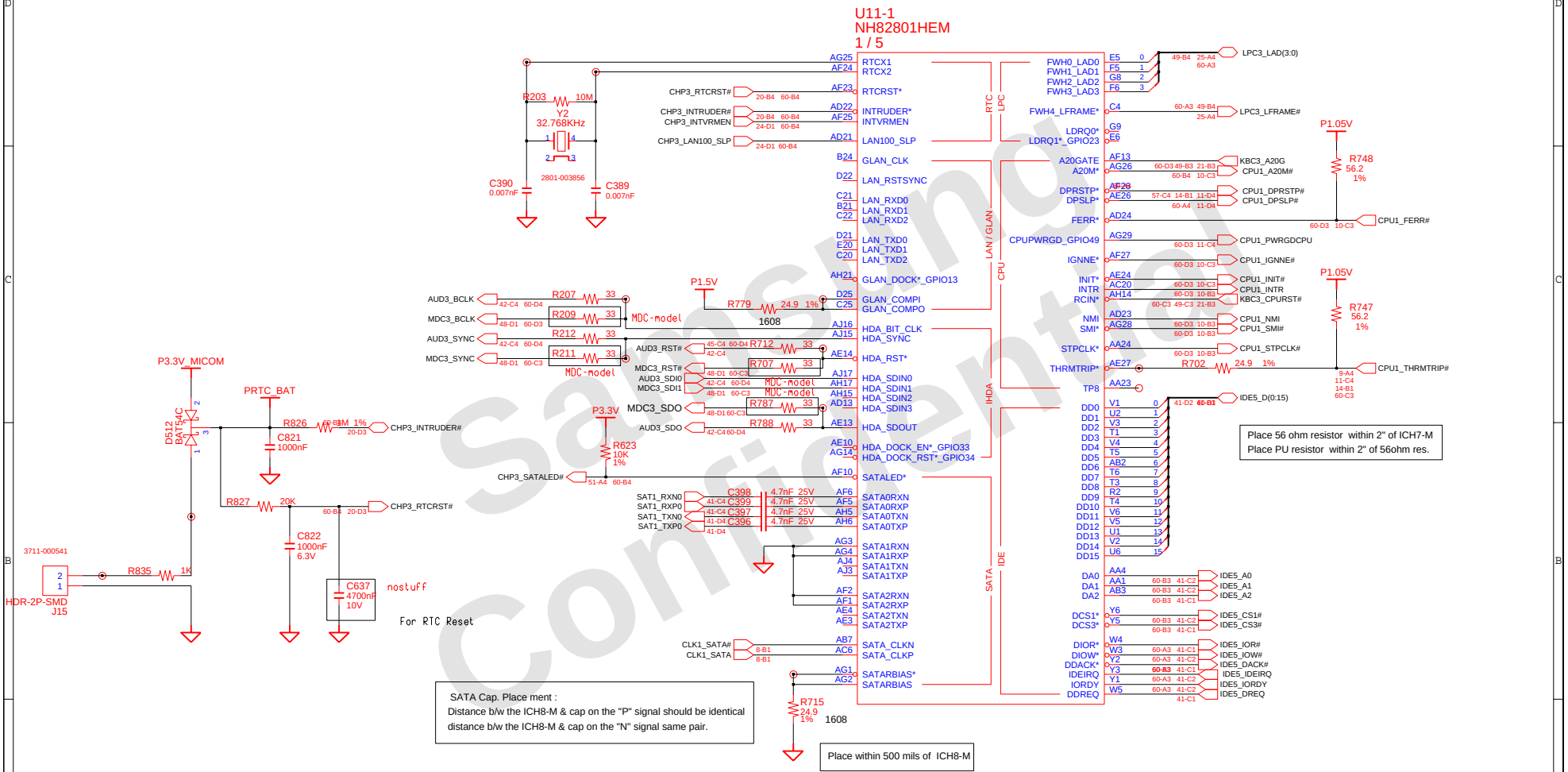


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO SODIMM DDR II CH A	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 18 OF 60	

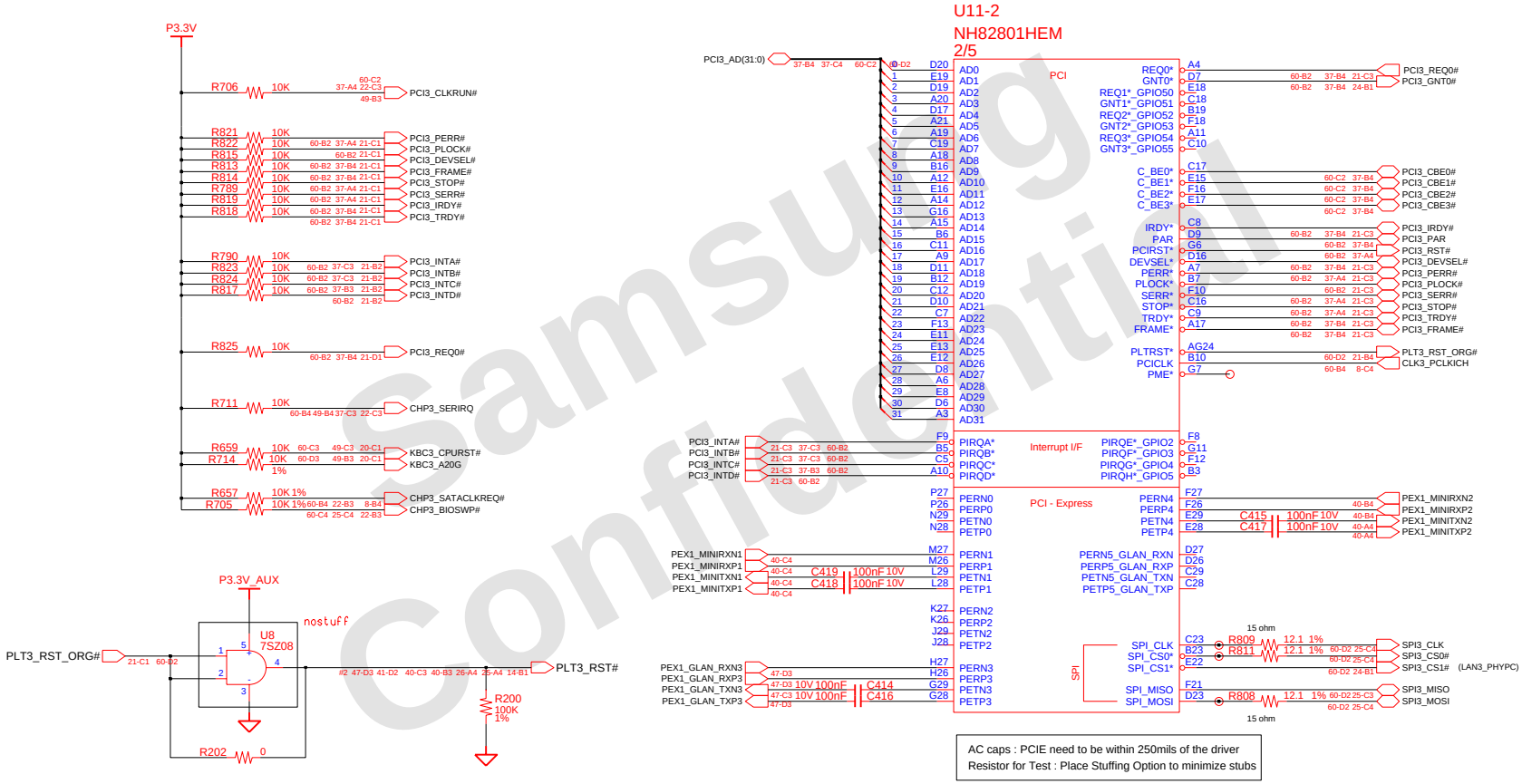
DDR SO-DIMM #1



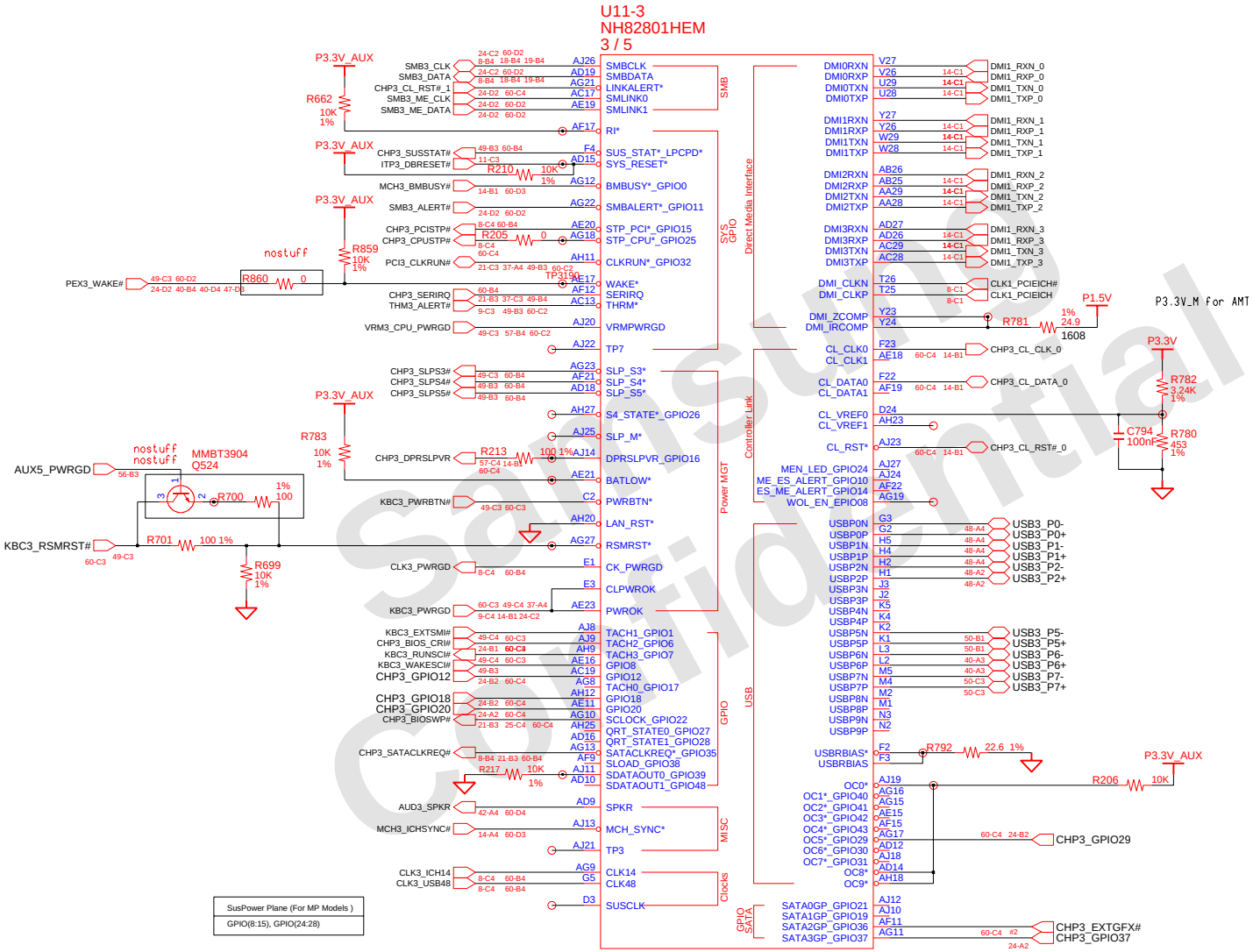
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO SODIMM DDR II CH B	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 19 OF 60	



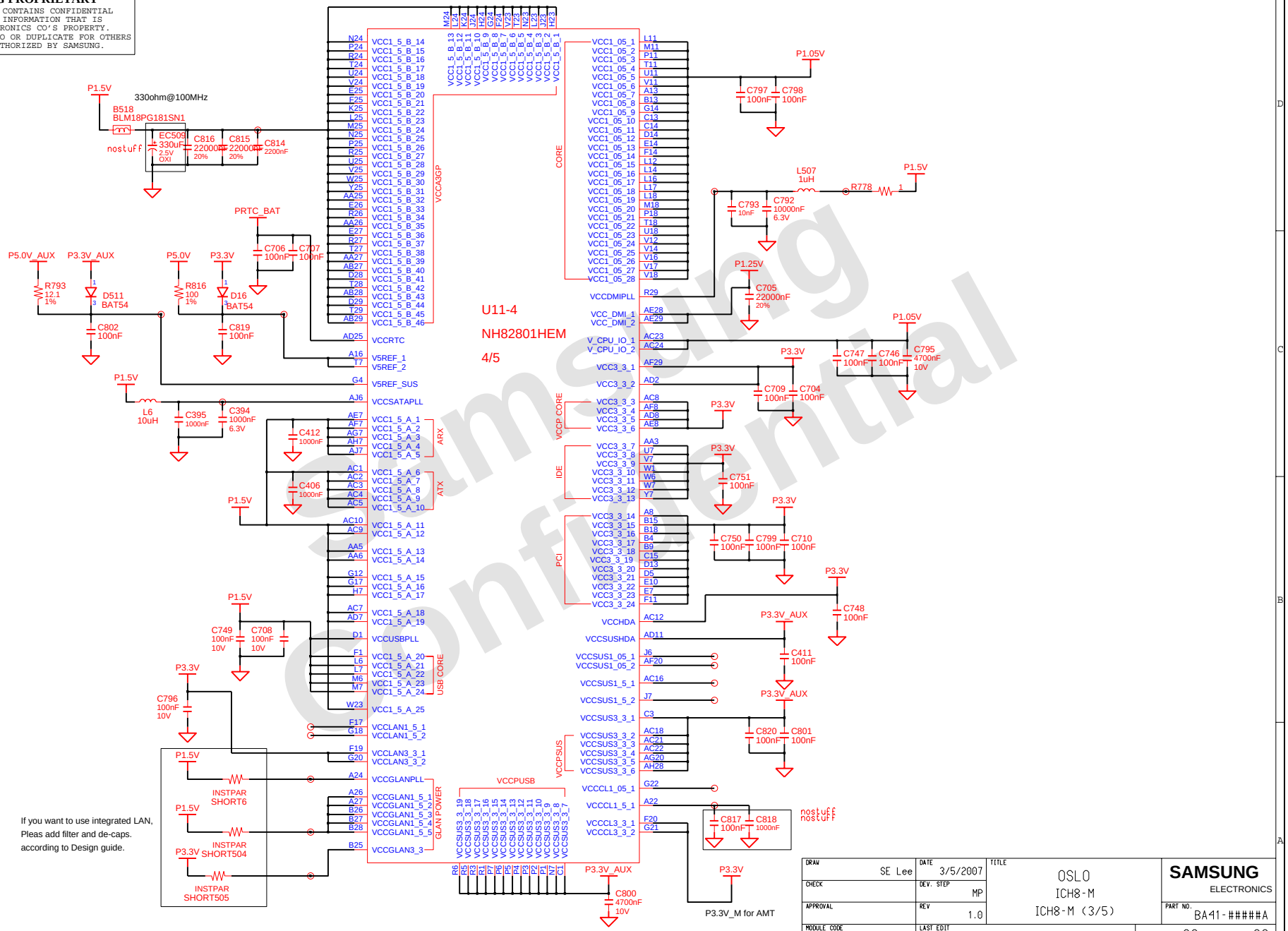
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO ICH8-M ICH8-M (1/5)	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 20 OF 60	



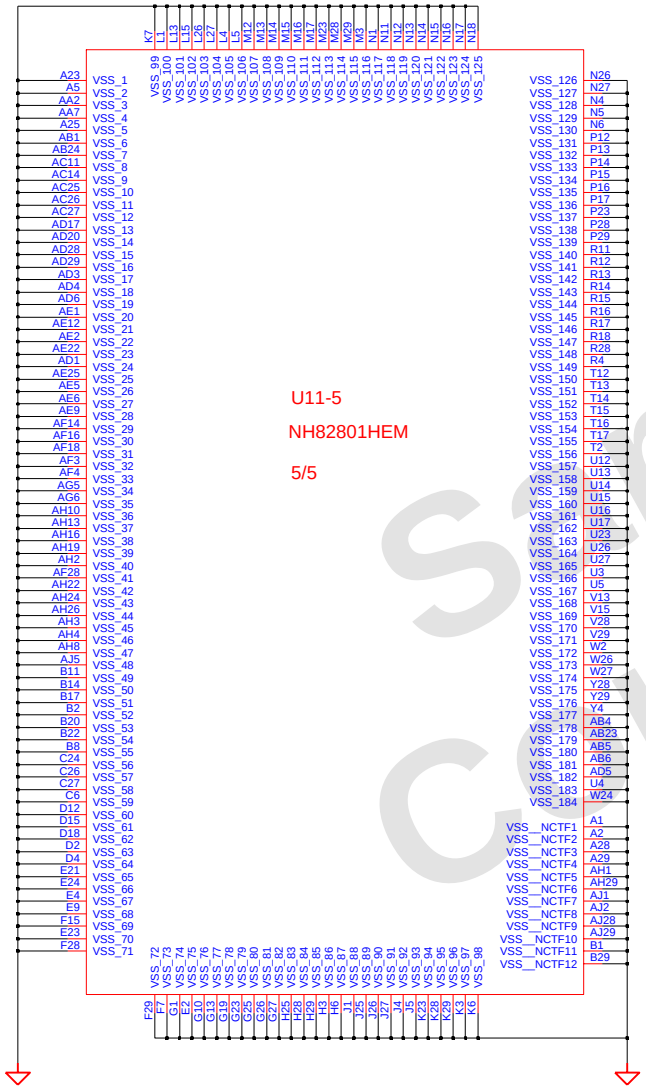
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO ICH8-M ICH8-M(2/5)	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 21 OF 60	

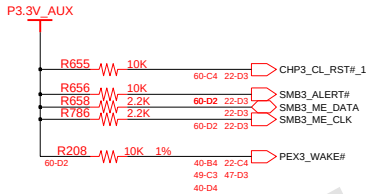


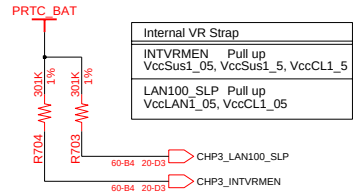
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO ICH8-M ICH8-M (3/5)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 22 OF 60	



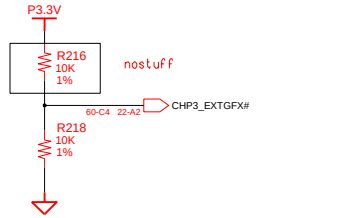
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO ICH8-M ICH8-M (3/5)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 23 OF 60	

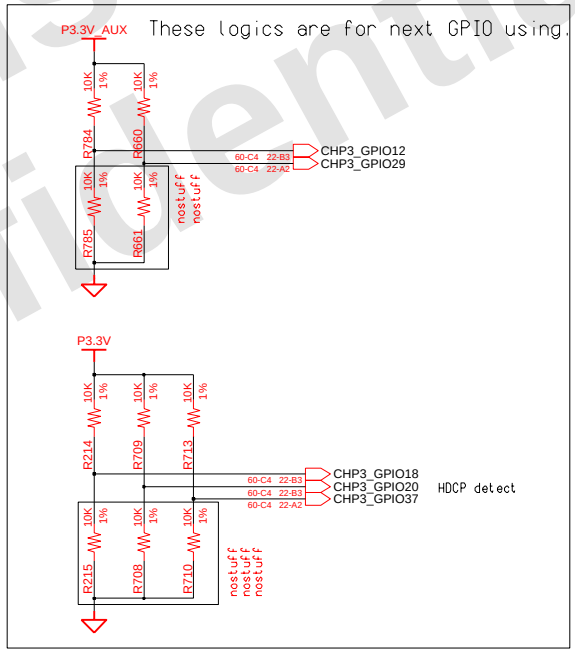






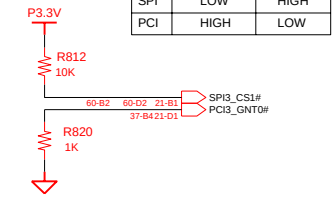
Internal VR Strap
INTVRMEN Pull up VccSus1_05, VccSus1_5, VccCL1_5
LAN100_SLP Pull up VccLAN1_05, VccCL1_05

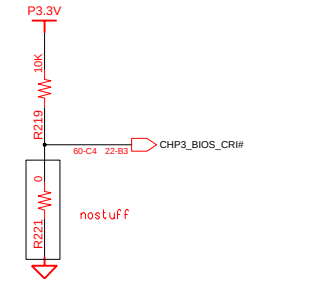




Boot BIOS Select

BIOS	PCI3_GNT0*	SPI3_CS1*
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW





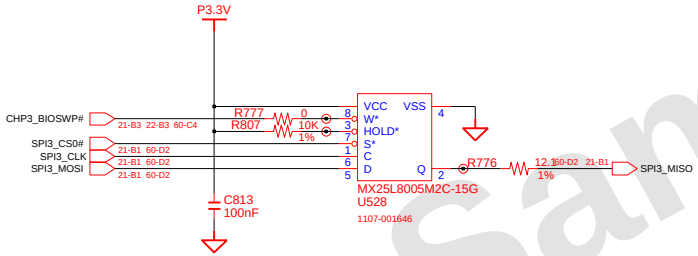
BIOS CRISIS RECOVER STRAP
PLACE NEAR KEYBOARD

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO ICH8-M ICH8-M (5/5)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 24 OF 60	

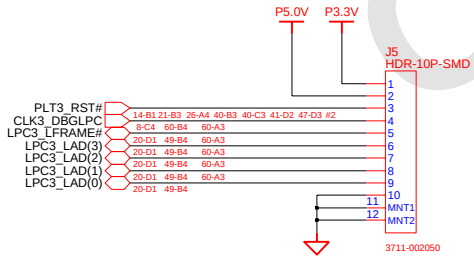
- SPI ROM LIST -

- Macronix - MX25L8005M2C-15G
- STM - M25PE80
- ATMEL - AT26DF081A-SU

SST - 25VF080B-50-4C-S2AF
WINBOND - W25X80-VSSI-G

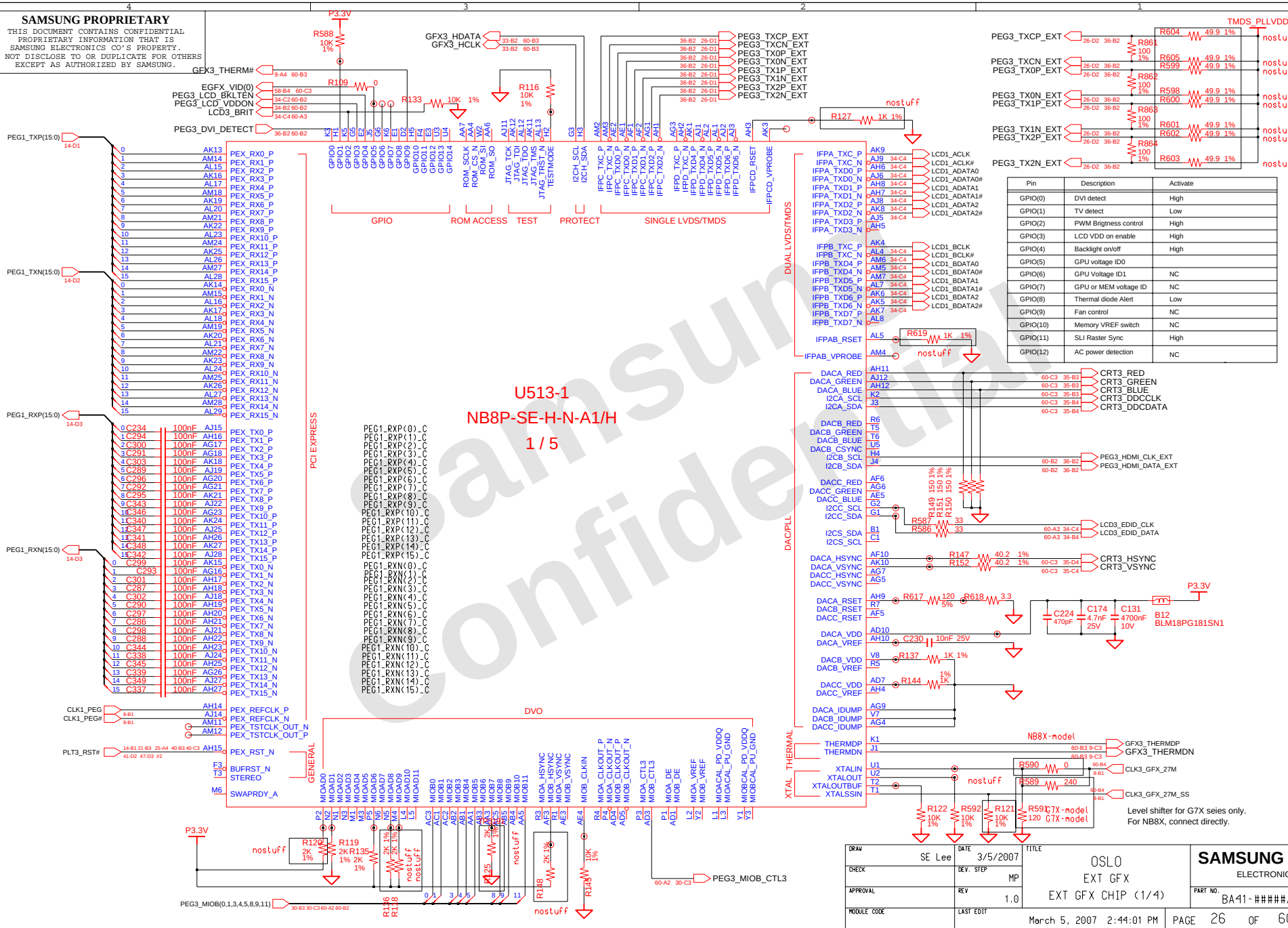


80H DECODER CONNECTOR



02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU.REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
OE INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE	86 RE-INIT. ON-BOARD I/O PORT
14 INIT. KEYBOARD CONTROLLER	88 INIT. BIOS DATA ROM
16 CHECK CHECKSUM	8A INIT.EXTENDED BIOS DATA AREA
18 8254 TIMER INIT.	8C INIT. FDD CONTROLLER
1A 8237 DMA CONTROLLER INIT.	9A SHADOW OPTION ROMS
1C RESET INTERRUP CONTROLLER	9C SETUP POWER MANAGEMENT
20 TEST DRAM REFRESH	9E ENABLE H/W INTERRUPT
22 TEST 8742 KEYBOARD CONTROLLER	A0 SET TIME OF DAY
24 SET ES SEGMENT REG. TO 4GB	A4 INIT. TYPEMATIC RATE
26 ENABLE A20	A8 ERASE F2 PROMPT
28 AUTO SIZING DRAM	AA SCAN FOR F2 KEY STROKE
32 COMPUTE THE CPU SPEED	AC ENTER SETUP
34 TESET CMOS RAM	AE CLEAR IN POST FLAG
38 SHADOW SYSTEM BIOS ROM	B0 CHECK FOR ERRORS
3A AUTO SIZING CACHE	B2 POST DONE-PREPARE TO BOOT O/S
3C CONFIGURE ADVANCED CHIPSET REG.	B4 ONE BEEP
3D LOAD ALTER REG. WITH CMOS VALUE	B6 CHECK PASSWORD (OPTION)
42 INIT. INTERRUPT VECTOR	B7 ACPI INIT
44 INIT. BIOS INTERRUPT	BA DMI INIT
46 CHECK ROM COPYRIGHT NOTICE	BE CLEAR SCREEN
47 INIT. I20 SUPPORT IF INSTALLED	C0 TRY BOOT WITH INT19
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D0 INTERRUPT HANDLER ERROR
49 INIT. PCI BUS AND DEVICE	D2 UNKNOWN INTERRUPT ERROR
4A INIT. ALL VIDEO BIOS ROM	D4 PENDING INTERRUPT ERROR
4C SHADOW VIDEO BIOS ROM	D6 SHUTDOWN 5
50 DISPLAY CPU TYPE AND SPEED	D8 SHUTDOWN ERROR
52 TEST KEYBOARD	DA EXTENDED BLOCK MOVE
54 SET KEYCLICK IF ENABLED	DC SHUTDOWN 10
56 ENABLE KEYBOARD	89 ENABLE NMI
58 TEST FOR UNEXPECTED INTERRUPTS	90 INIT. HDD CONTROLLER
5A DISPLAY " PRESS ..... SETUP"	91 INIT. LOCAL BUS HDD CONTROLLER
5C TEST RAM GETWEEN 512K AND 640K	92 JUMP TO USER PATCH 2
60 TEST EXTENDED MEMORY	94 DISABLE A20 ADDRESS LINE
62 TEST EXTENDED MEMORY ADDRESS LINE	96 CLEAR HUGE ES SEGMENT REG.
64 JUMP TO USER PATCH 1	98 SEARCH FOR OPTION ROMS

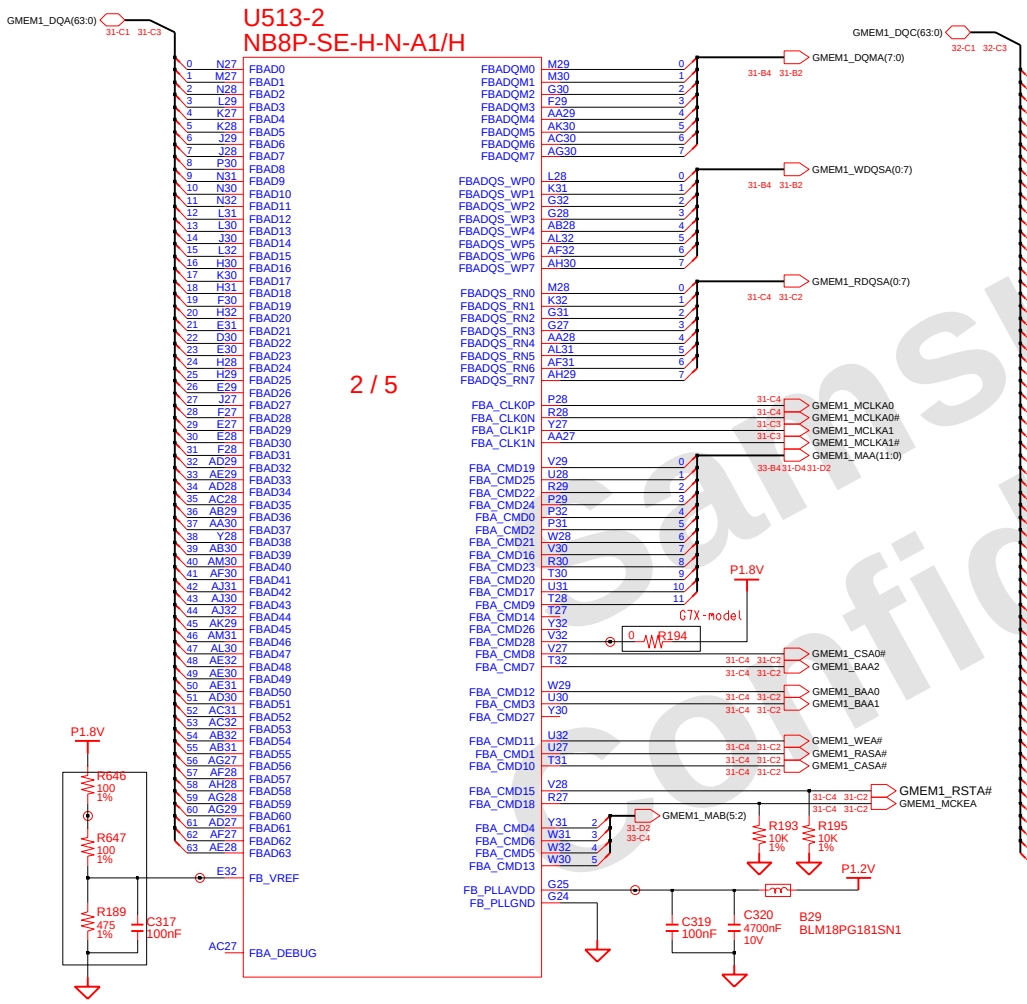
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO SPI ROM SPI ROM	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 25 OF 60	



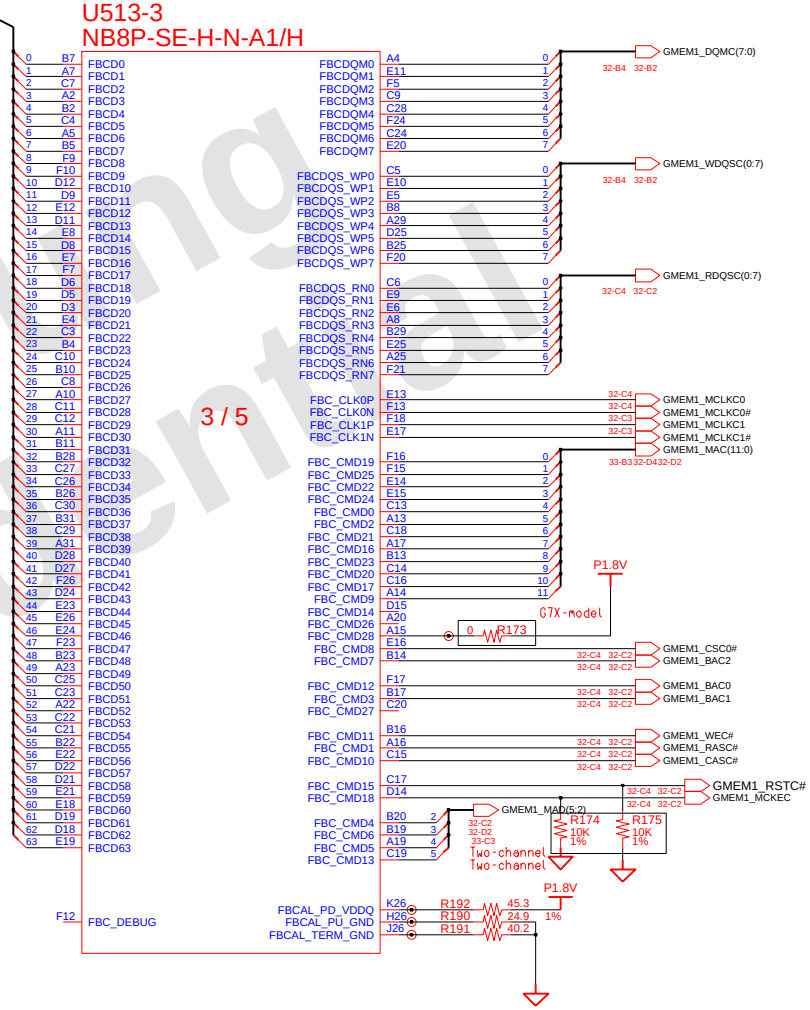
Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brigtness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU voltage ID0	
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU or MEM voltage ID	NC
GPIO(8)	Thermal diode Alert	Low
GPIO(9)	Fan control	NC
GPIO(10)	Memory VREF switch	NC
GPIO(11)	SLI Raster Sync	High
GPIO(12)	AC power detection	NC

DRAW	SE Lee	DATE 3/5/2007	TITLE OSLO EXT GFX EXT GFX CHIP (1/4)
CHECK		DEV. STEP MP	SAMSUNG ELECTRONICS
APPROVAL		REV 1.0	PART NO. BA41-#####A
MODULE CODE		LAST EDIT March 5, 2007 2:44:01 PM	PAGE 26 OF 60

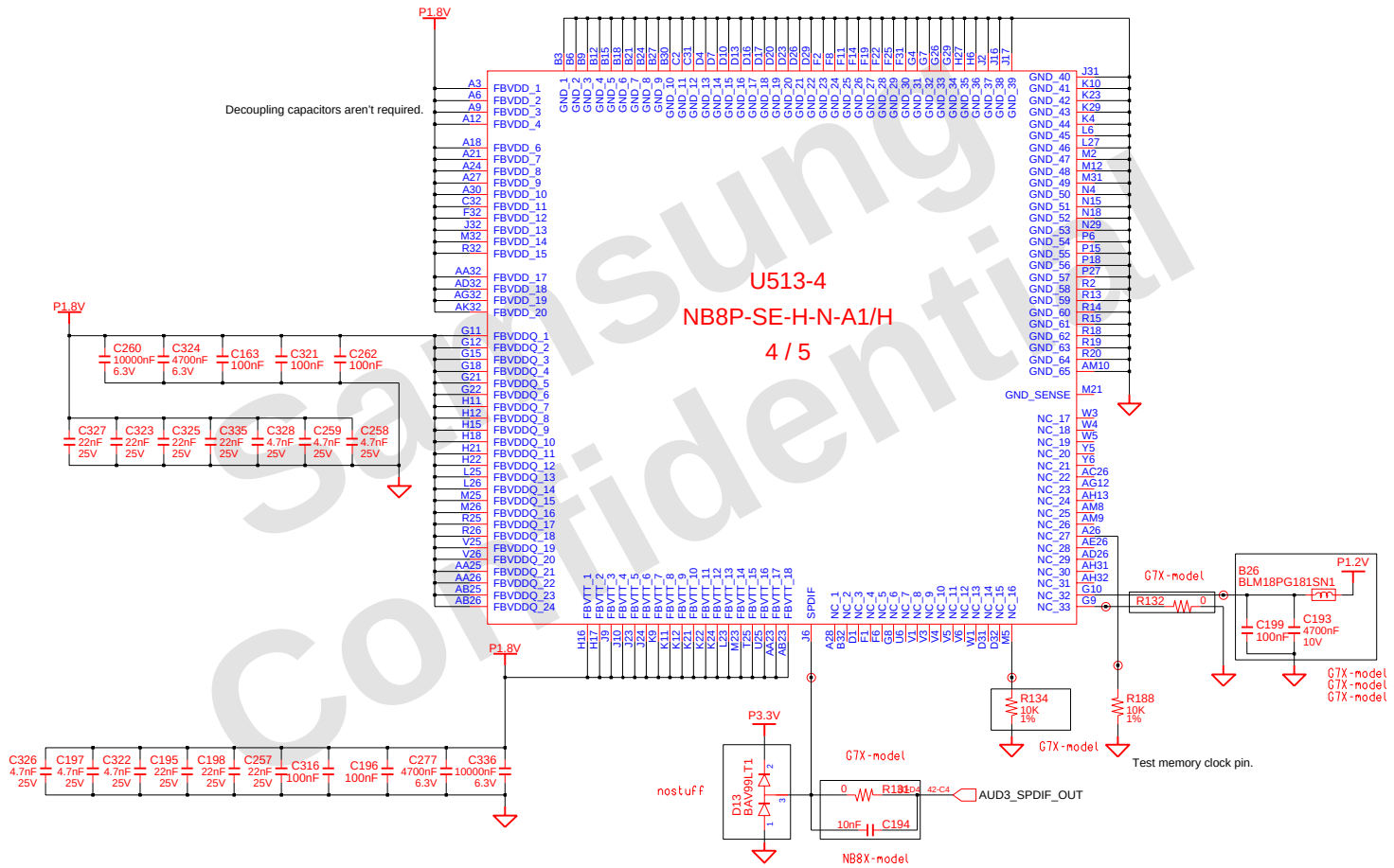
Graphic Memory I/F (Using FBA Channel)



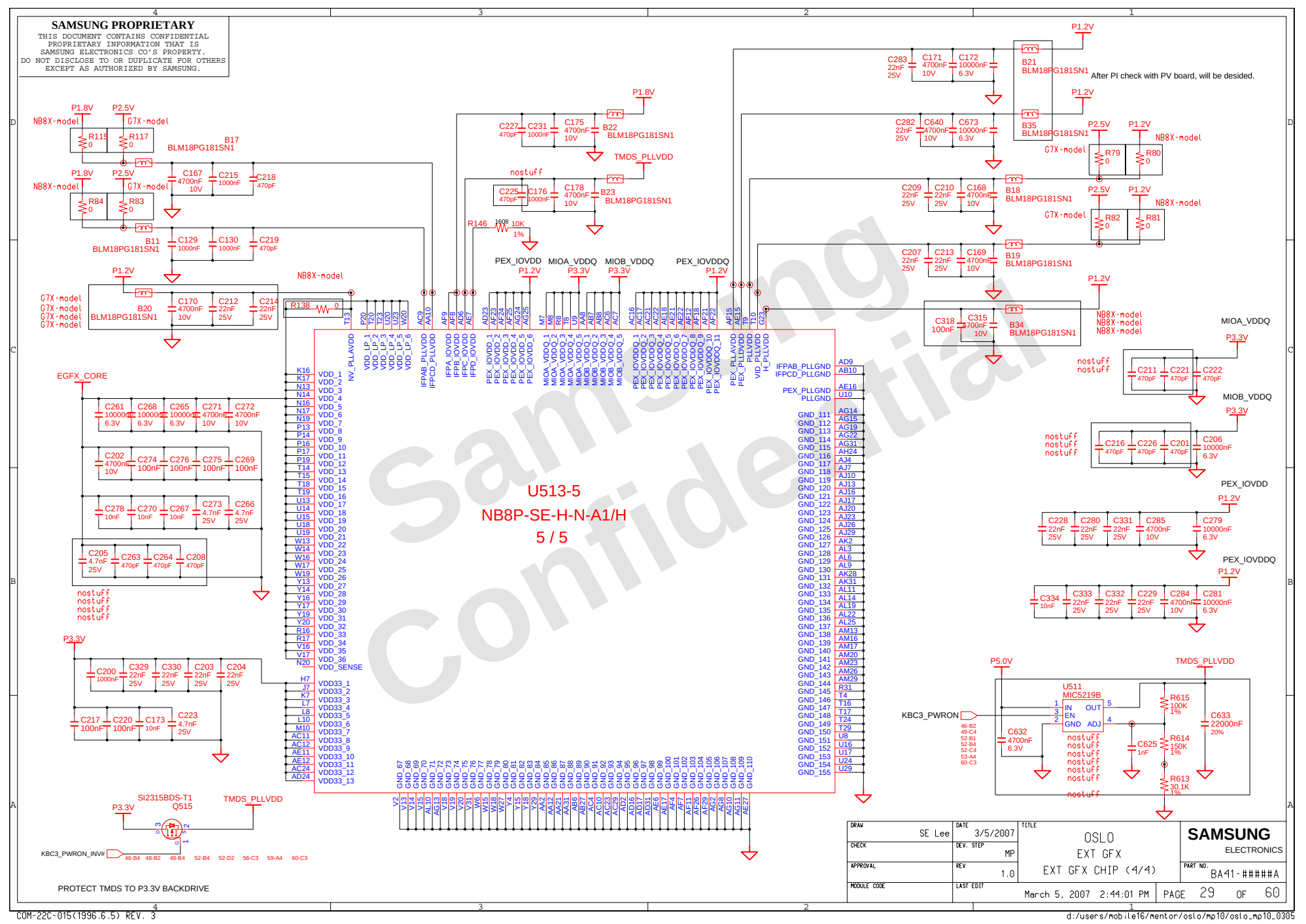
Graphic Memory I/F (Using FBC Channel)



DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO EXT GFX EXT GFX CHIP (2/4)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 27 OF 60	



DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO EXT GFX EXT GFX CHIP (3/4)	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 28 OF 60	



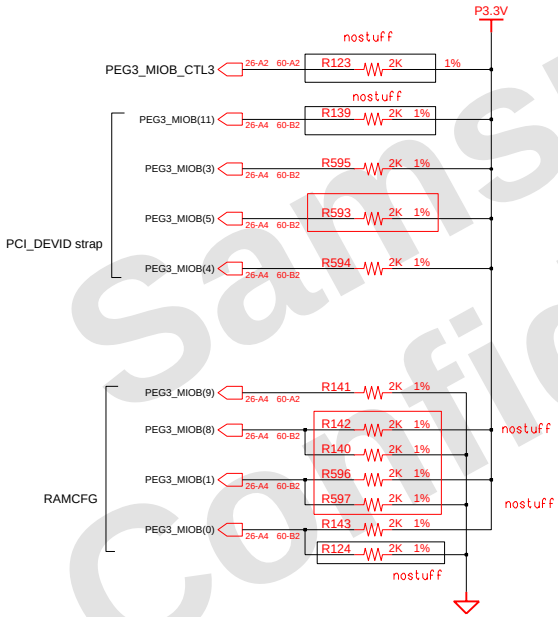
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO EXT GFX EXT GFX CHIP (4/4)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-######A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 29 OF 60	

NB8X

Need to modify

	R677	R80	R78	R79
72M-V	no-stuff	stuff	stuff	stuff
72M	stuff	no-stuff	no-stuff	no-stuff
73M	stuff	no-stuff	no-stuff	no-stuff

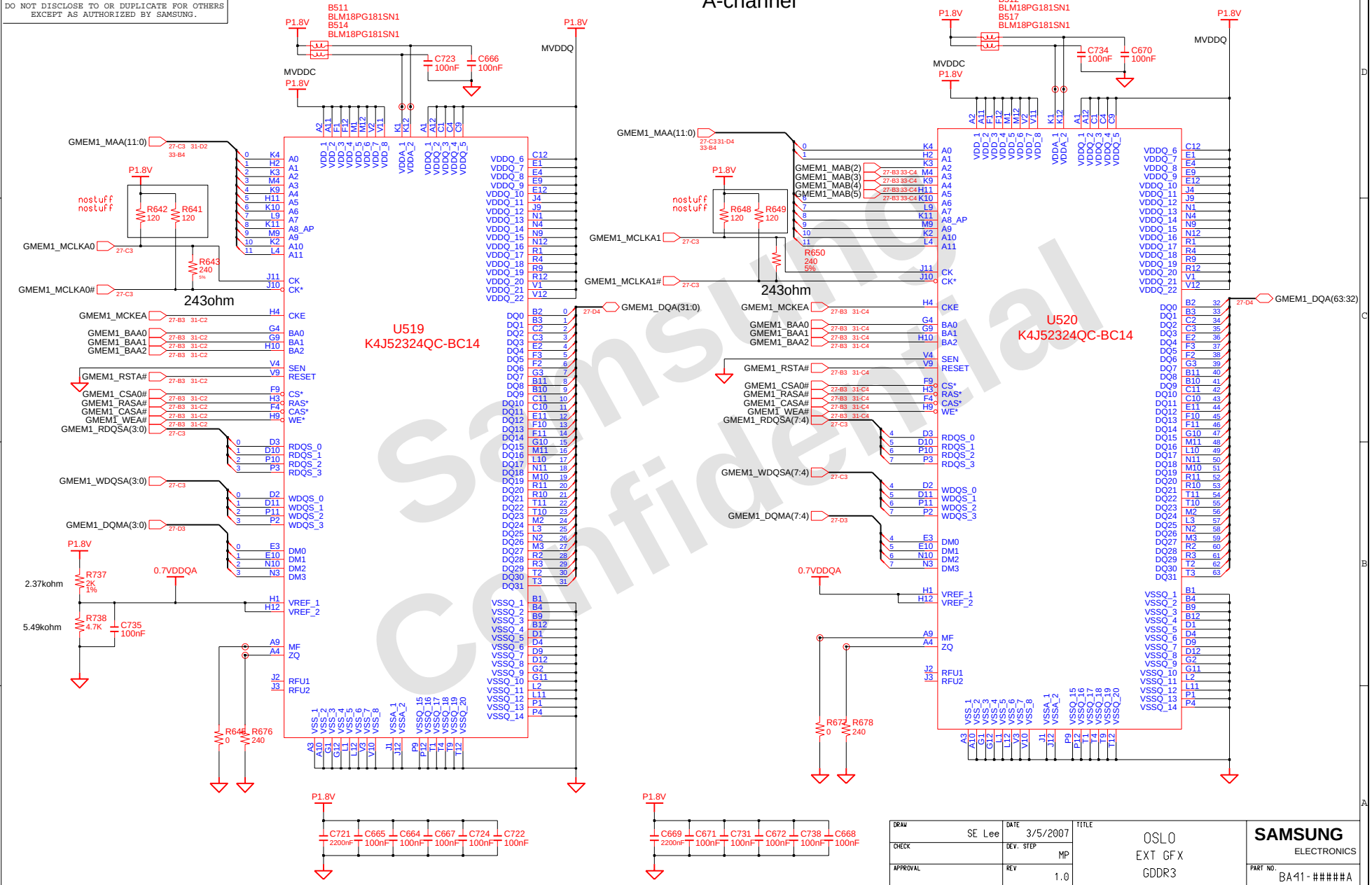
	R680	R78	R81	R82
SS 256Mb	stuff	no-stuff	stuff	no-stuff
INF 256Mb	stuff	no-stuff	no-stuff	stuff
SS 512Mb	no-stuff	stuff	stuff	no-stuff
INF 512Mb	no-stuff	stuff	no-stuff	stuff



Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS(Default)
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : samsung GDDR3 256Mbit 0101 : infineon GDDR3 256Mbit 0011 : samsung GDDR3 512Mbit 0001 : infineon GDDR3 512Mbit
CRYSTAL	MIOB(2)	0 : 27 MHz (Default) 1 : Reserved
TV_MODE(2:0)	MIOB(6) MIOAD(10) MIOAD(7)	000 : NTSC M 001 : NTSC J (default) 010 : PAL M 011 : PAL N 100 : PAL CN 101 : PAL BDGHI 110 : Reserved 111 : Reserved
PCI_DEVID(4:0) [CTL3, 11,3,5,4]	CTL 3 MIOB(11) MIOB(3) MIOB(5) MIOB(4)	NB8P-GS : 0x407 (0111) NB8P-SE : 0x425 (0101) NB8M-GS : 0x427 (0111) 73M : 0X0398
ROM_TYPE(1:0)	MIOBVSYNC MIOB(10)	No ROM (NC)
USER STRAP	MIOAD(5:2)	EDID

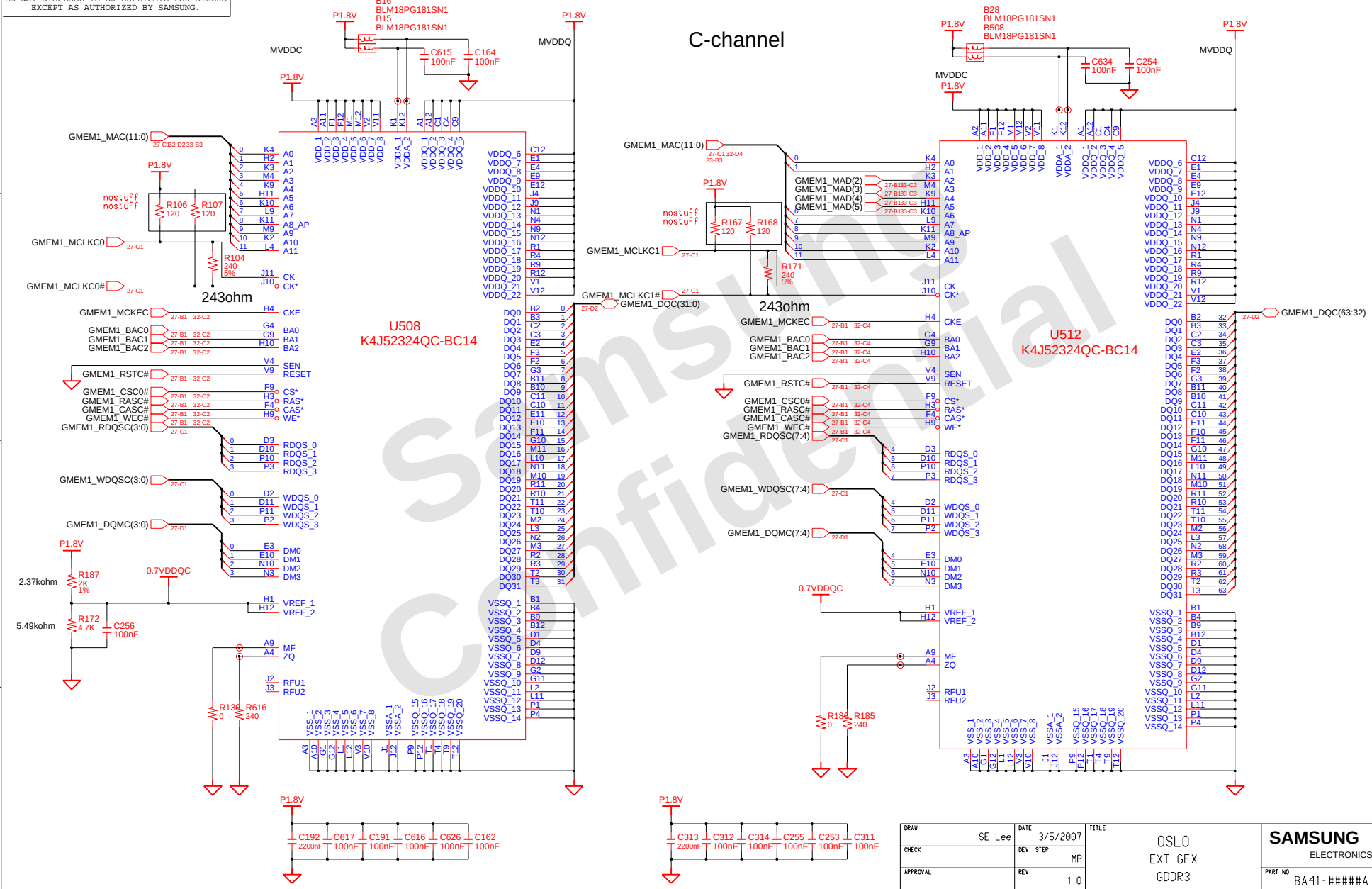
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO EXT GFX STRAP	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 30 OF 60	

A-channel

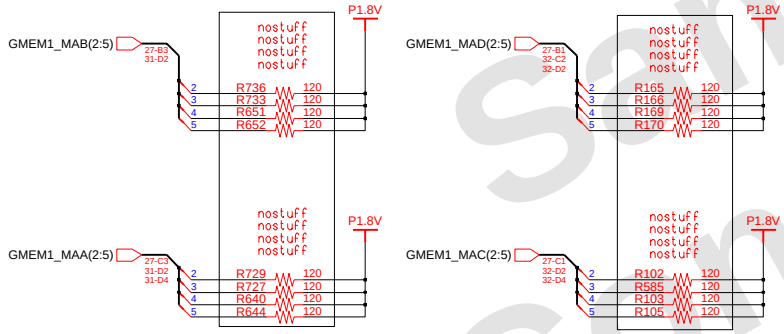


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO EXT GFX GDDR3	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-######A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 31 OF 60	

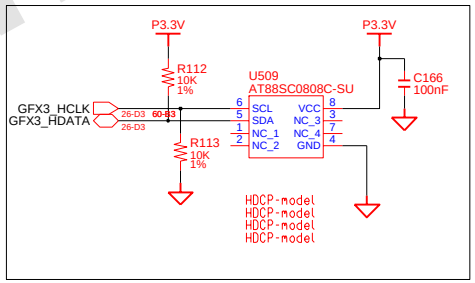
This page is for "2channel-model".



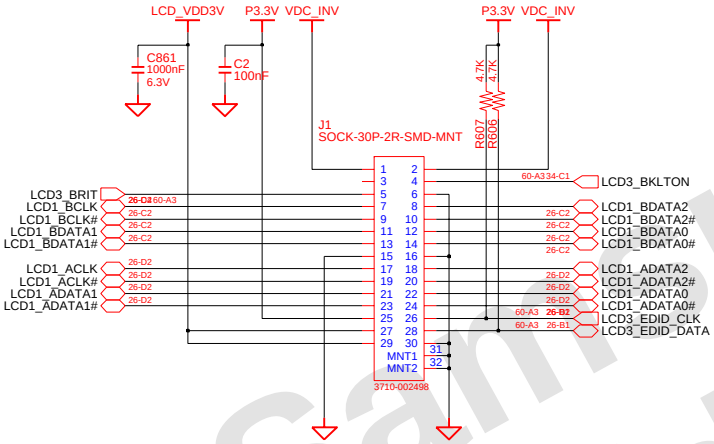
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO EXT GFX GDDR3	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-######A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 32 OF 60	

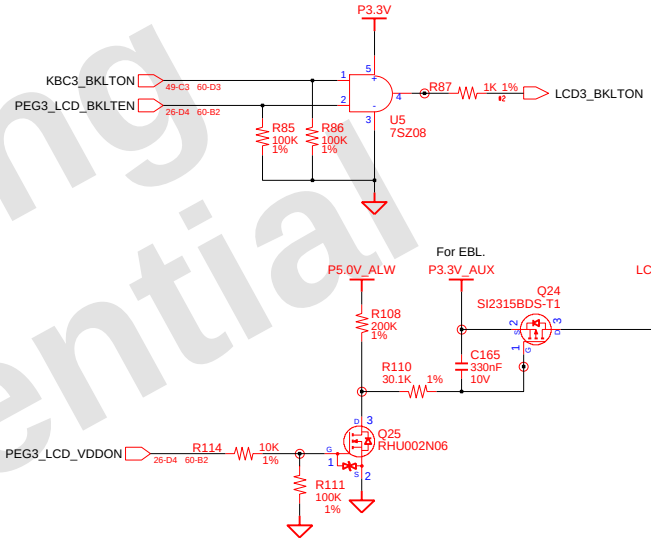


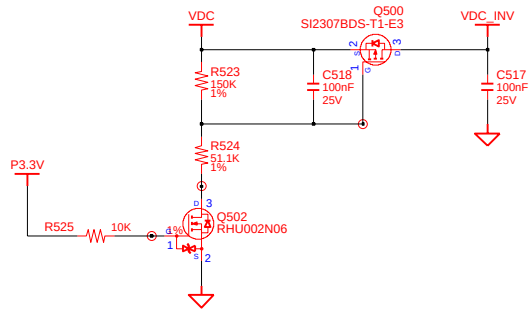
HDCP ROM



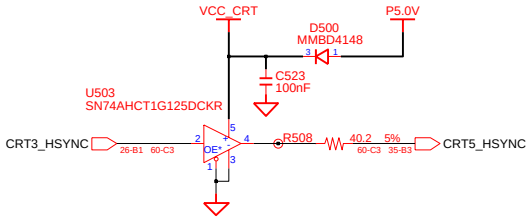
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO EXT GFX HDCP ROM	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 33 OF 60	

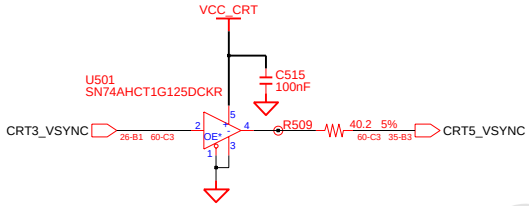


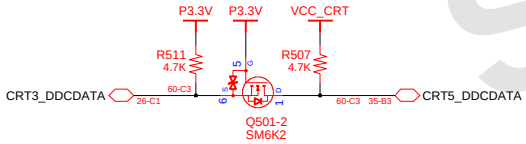


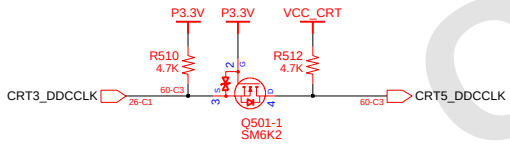


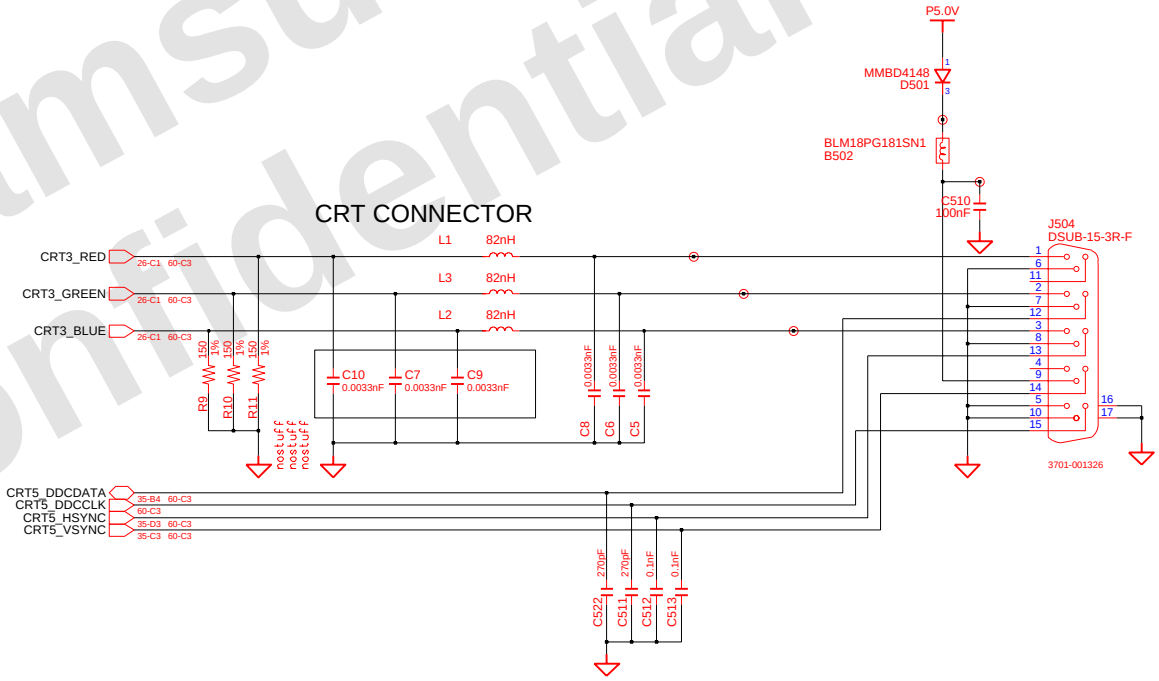
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO LCD LCD OPTION & LCD VDDEN	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 34 OF 60	



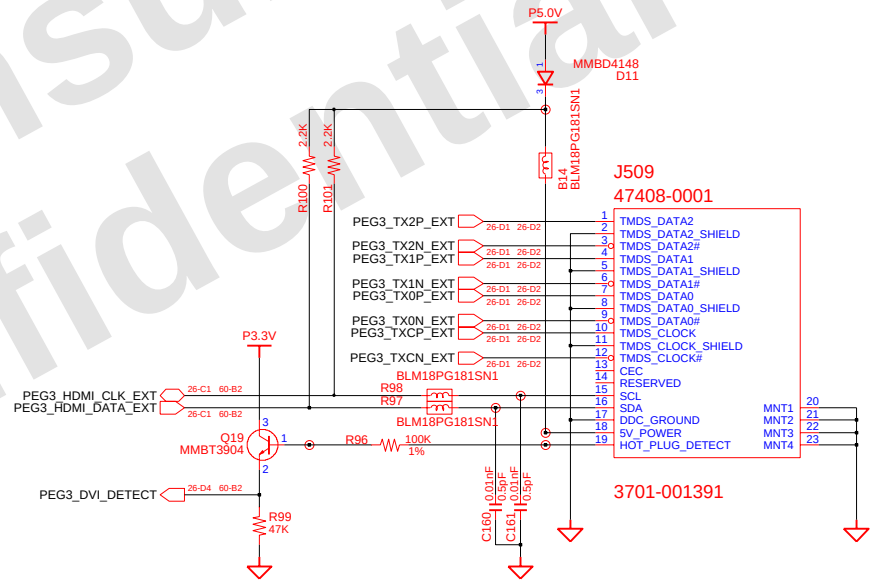




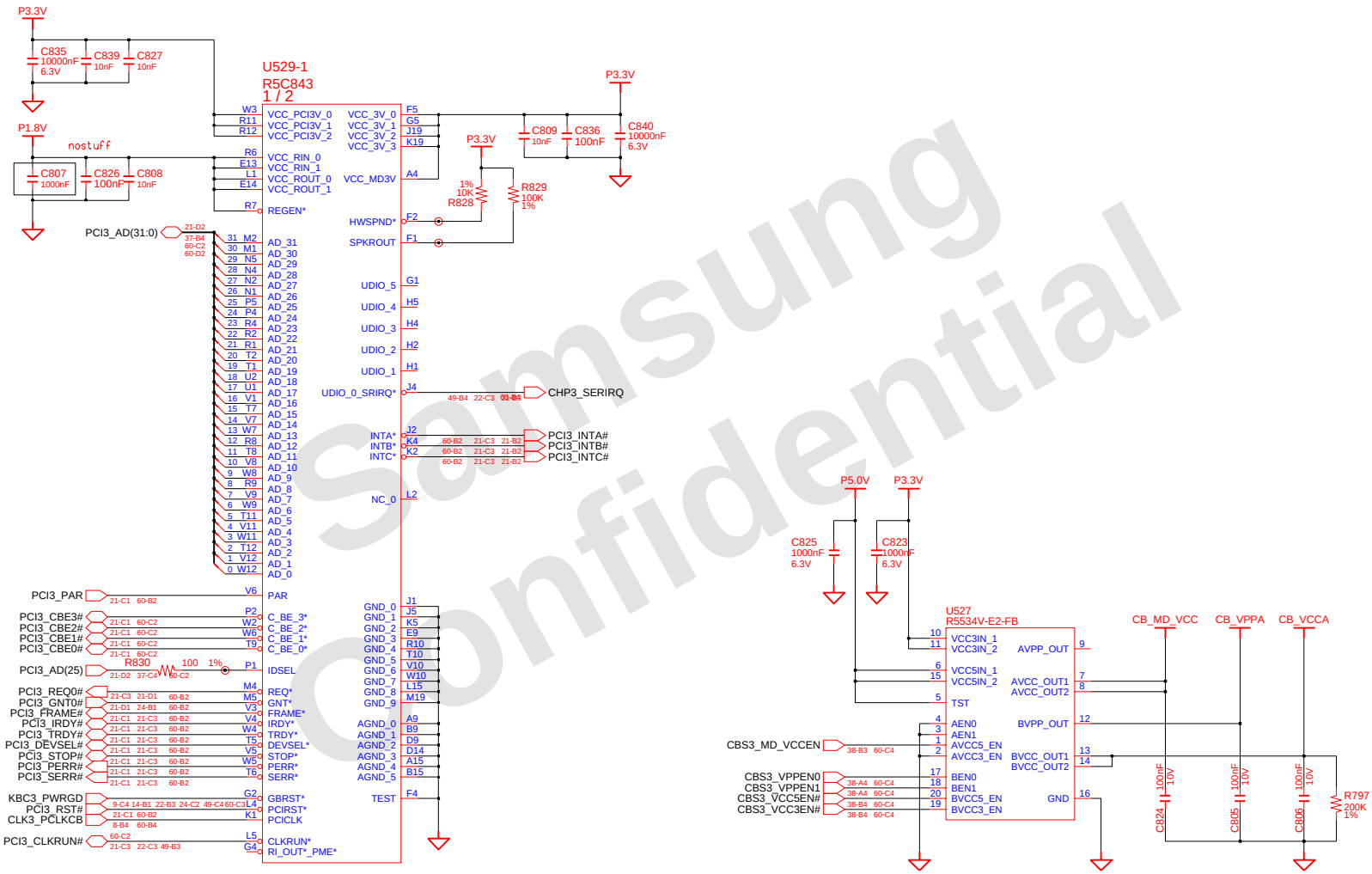




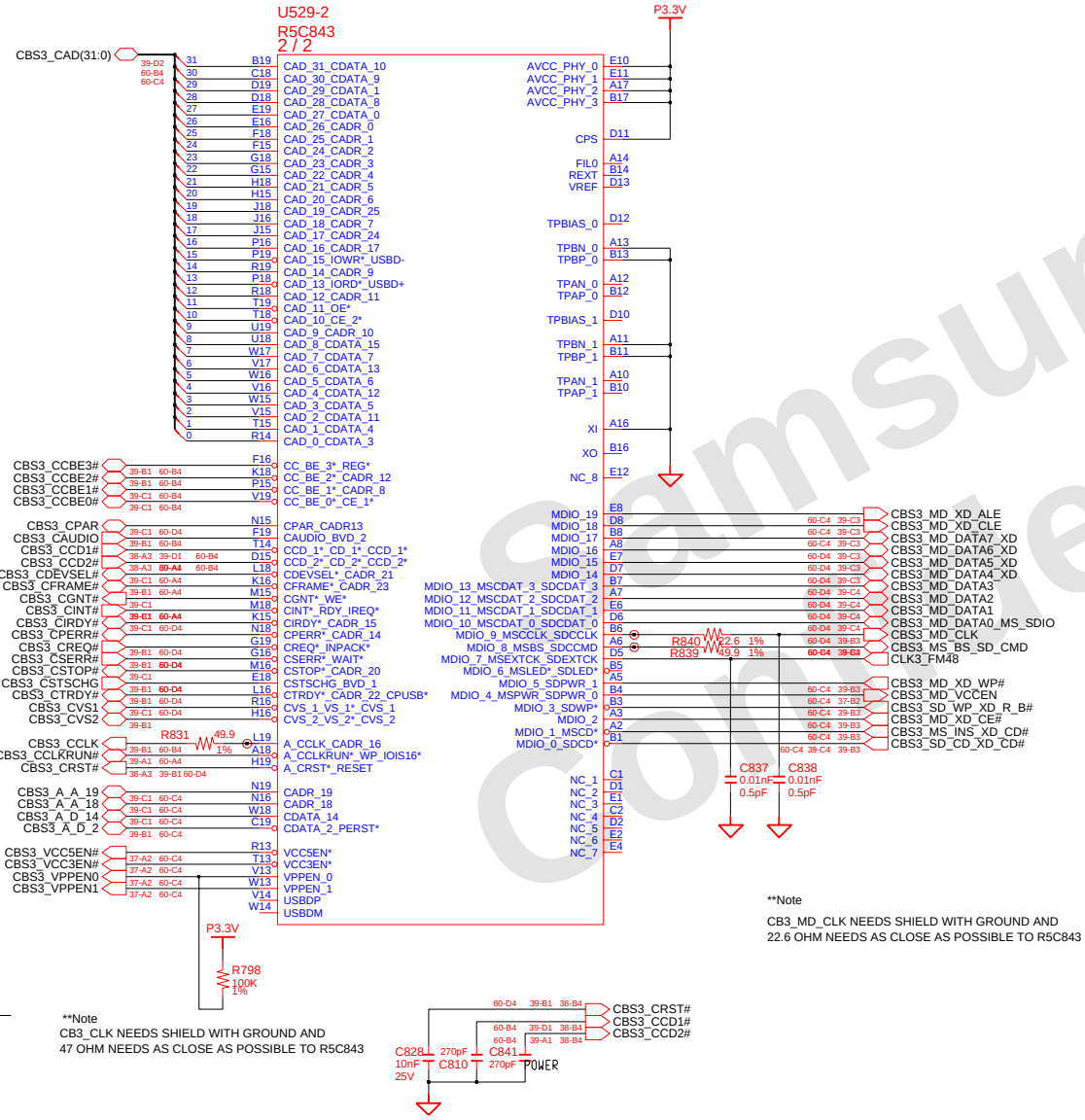
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO VIDEO CRT & option	SAMSUNG ELECTRONICS
CHECK: CHO, KS	DEV. STEP: MP		
APPROVAL: KOO, JG	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 35 OF 60	



DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO VIDEO HDMI	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 36 OF 60	



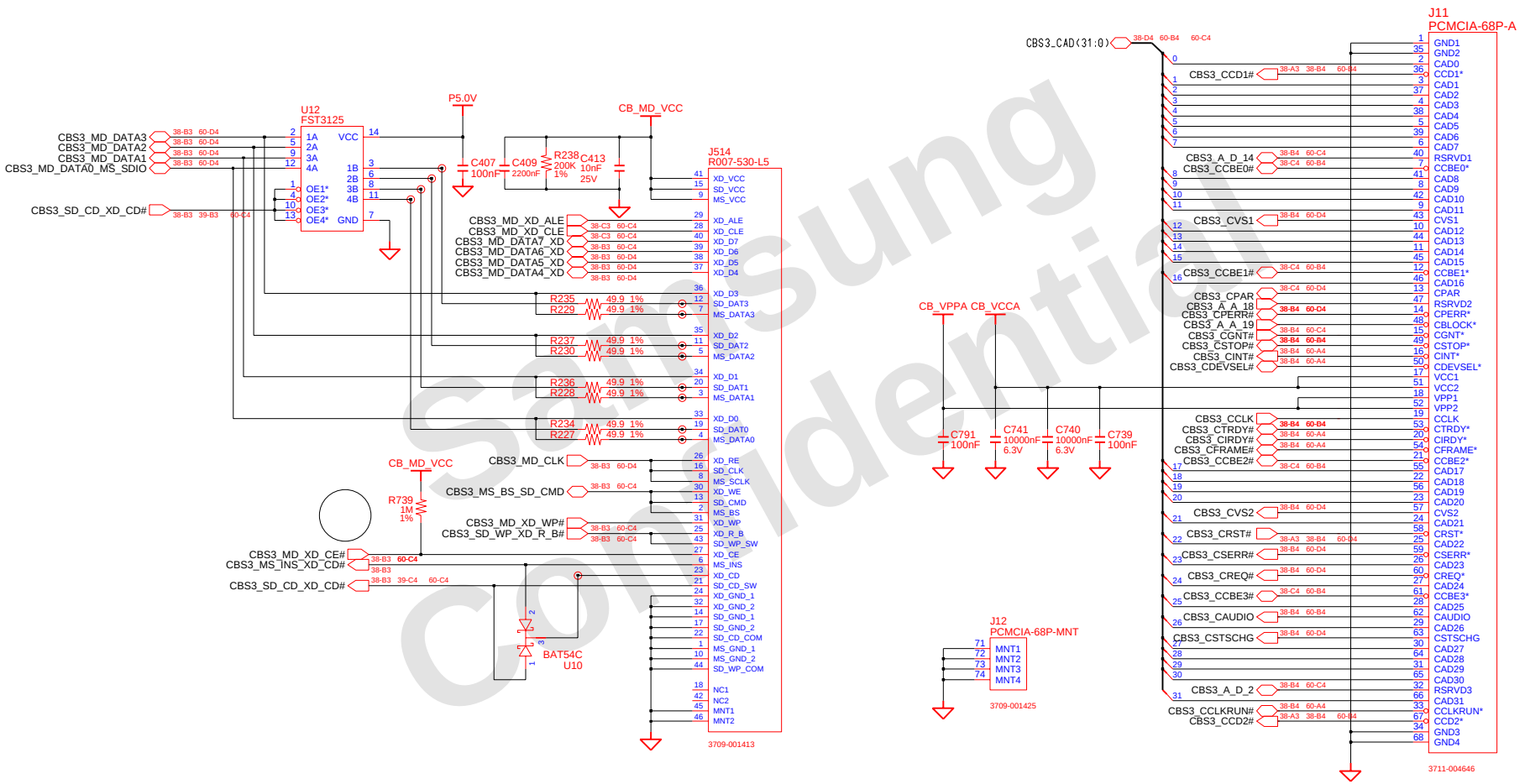
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO CARD BUS CONTROLLER R5C843(1/2)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 37 OF 60	



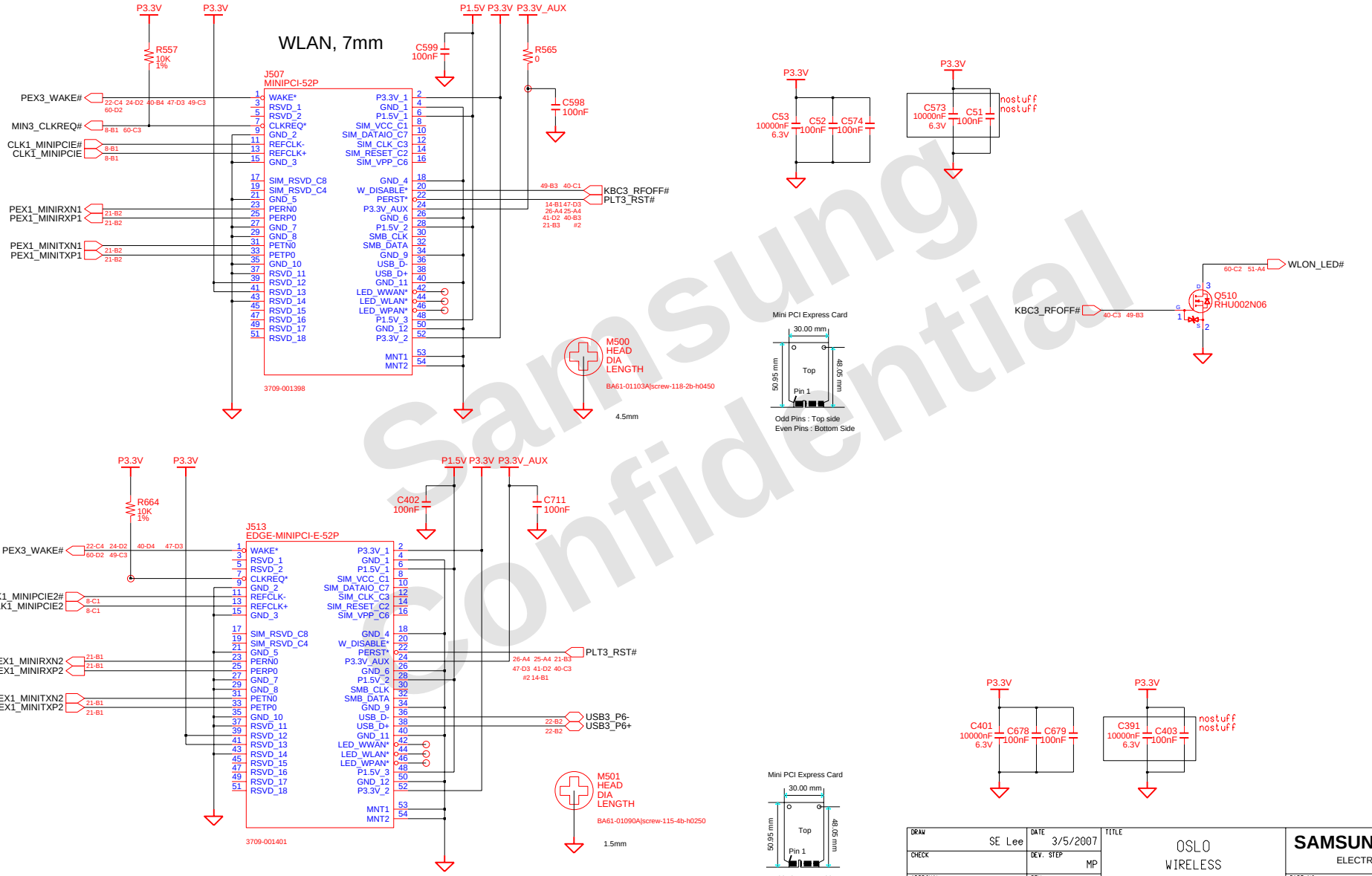
**Note
CB3_CLK NEEDS SHIELD WITH GROUND AND
47 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

**Note
CB3_MD_CLK NEEDS SHIELD WITH GROUND AND
22.6 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO CARD BUS CONTROLLER R5C843(2/2)	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 38 OF 60	

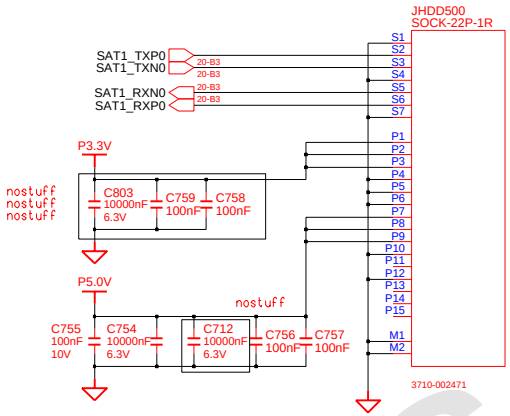


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO CARD BUS CONTROLLER 4-I ONE CONNECTOR	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 39 OF 60	

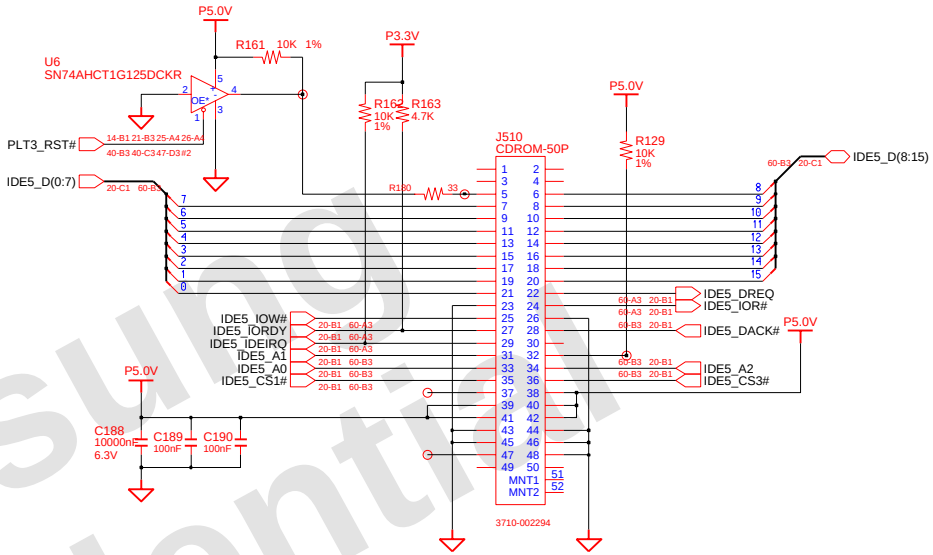


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO WIRELESS MINI CARD	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 40 OF 60	

Main to HDD

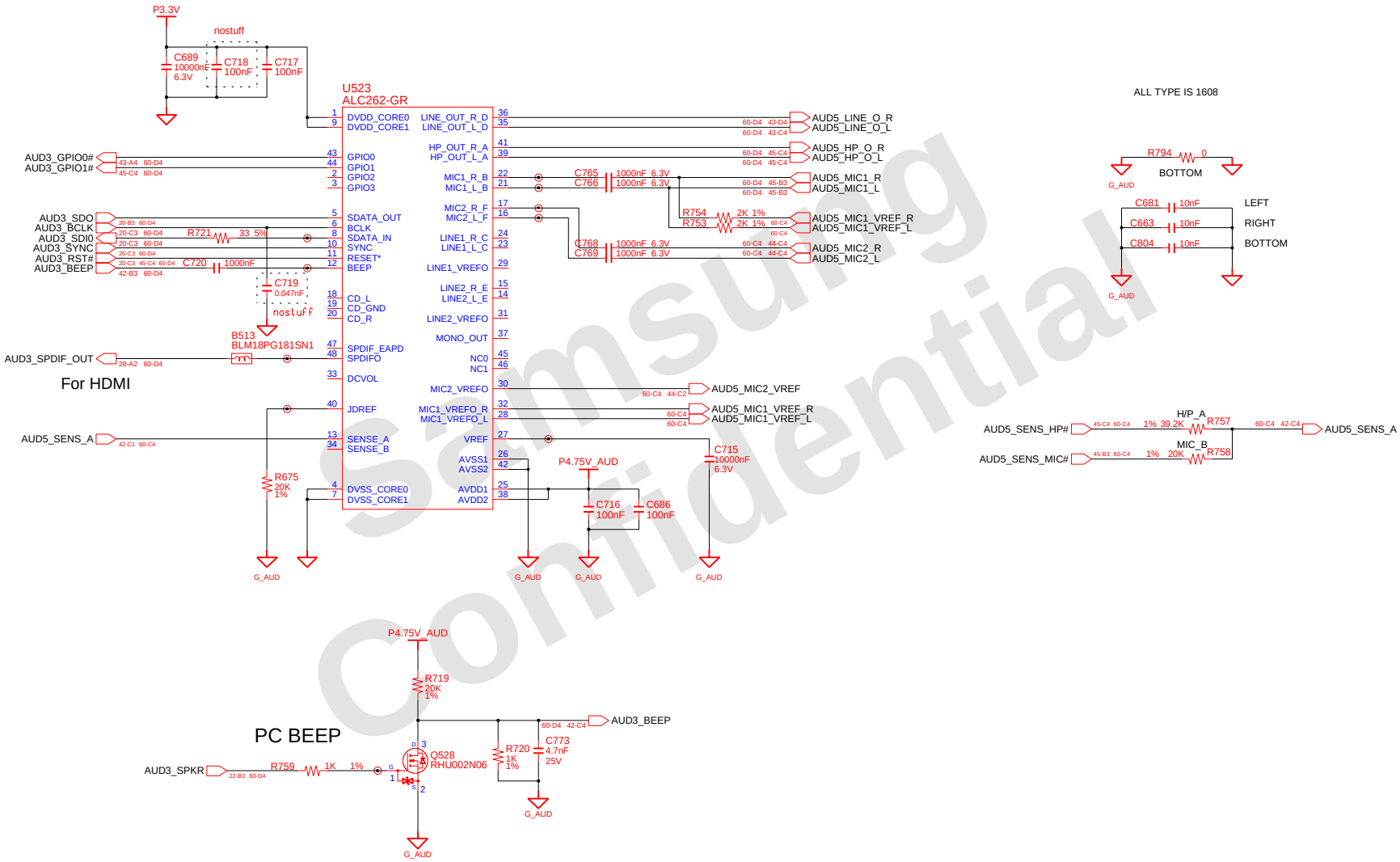


Main to Swap B'd

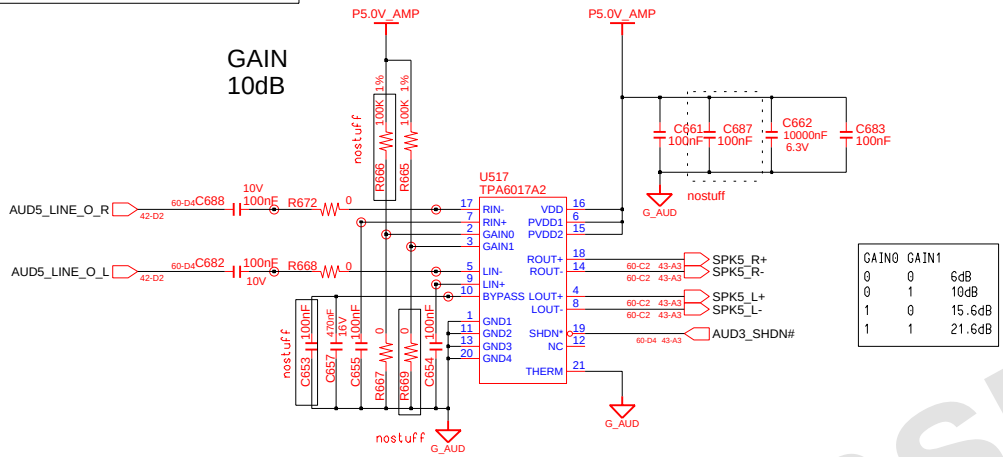


	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)

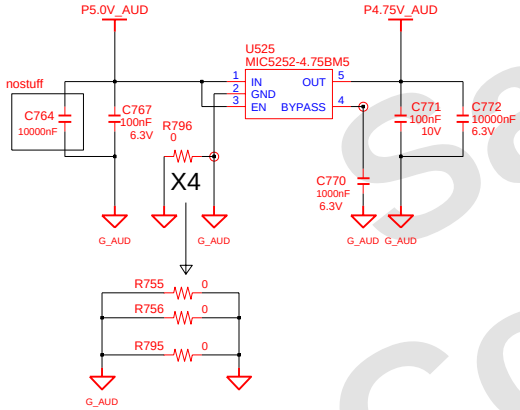
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO HDD & ODD HDD& ODD	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		PART NO.: BA41-#####A
APPROVAL:	REV: 1.0		
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 41 OF 60	

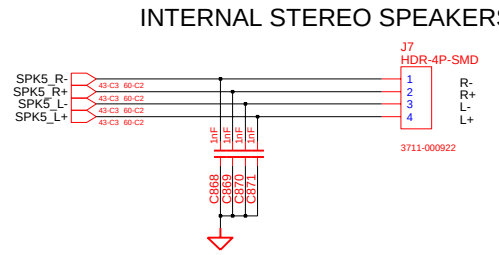


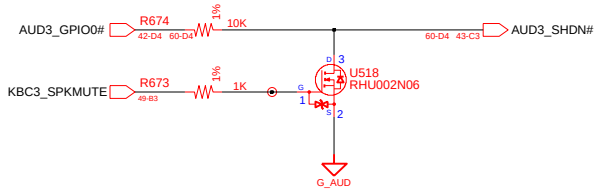
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO HD AUDIO ALC262	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 42 OF 60	



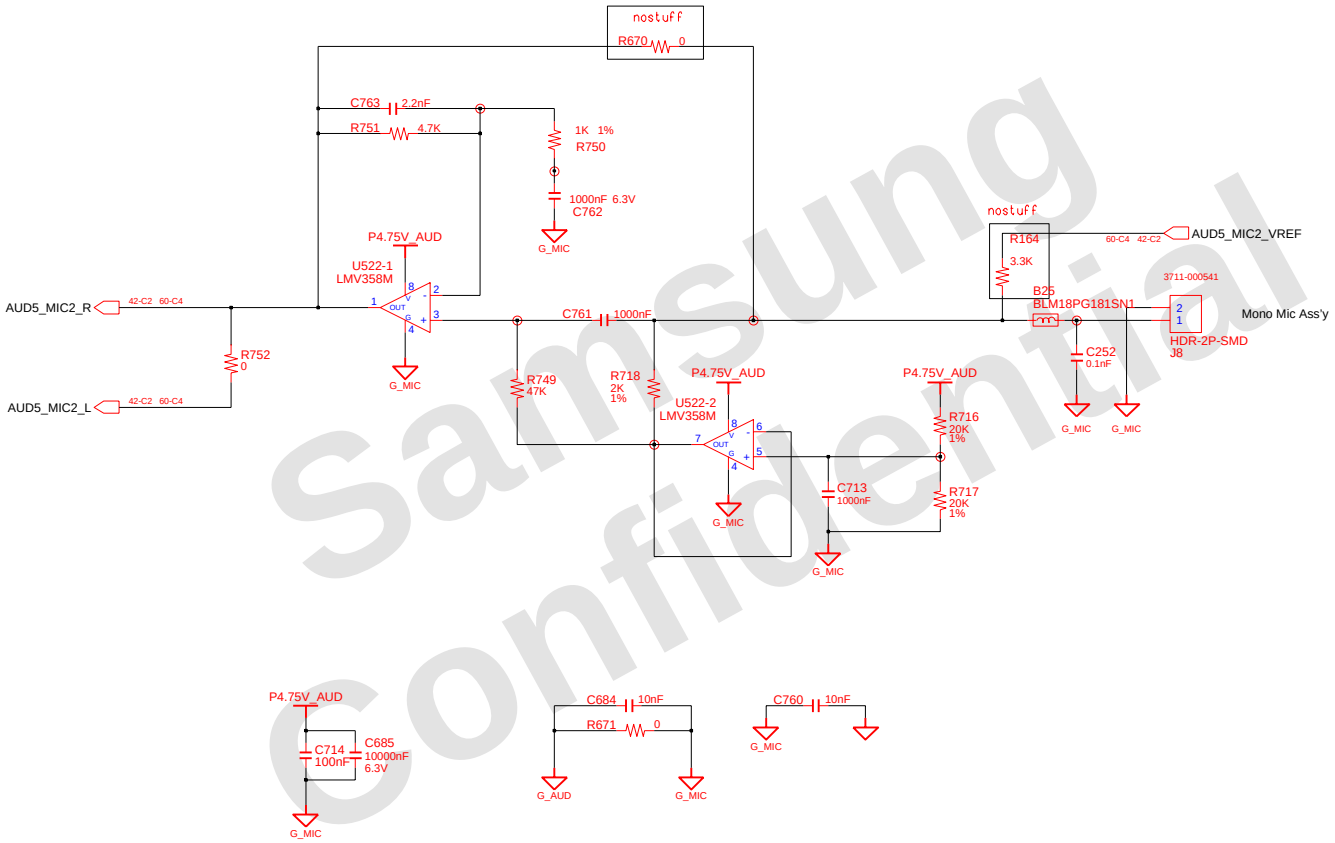
GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



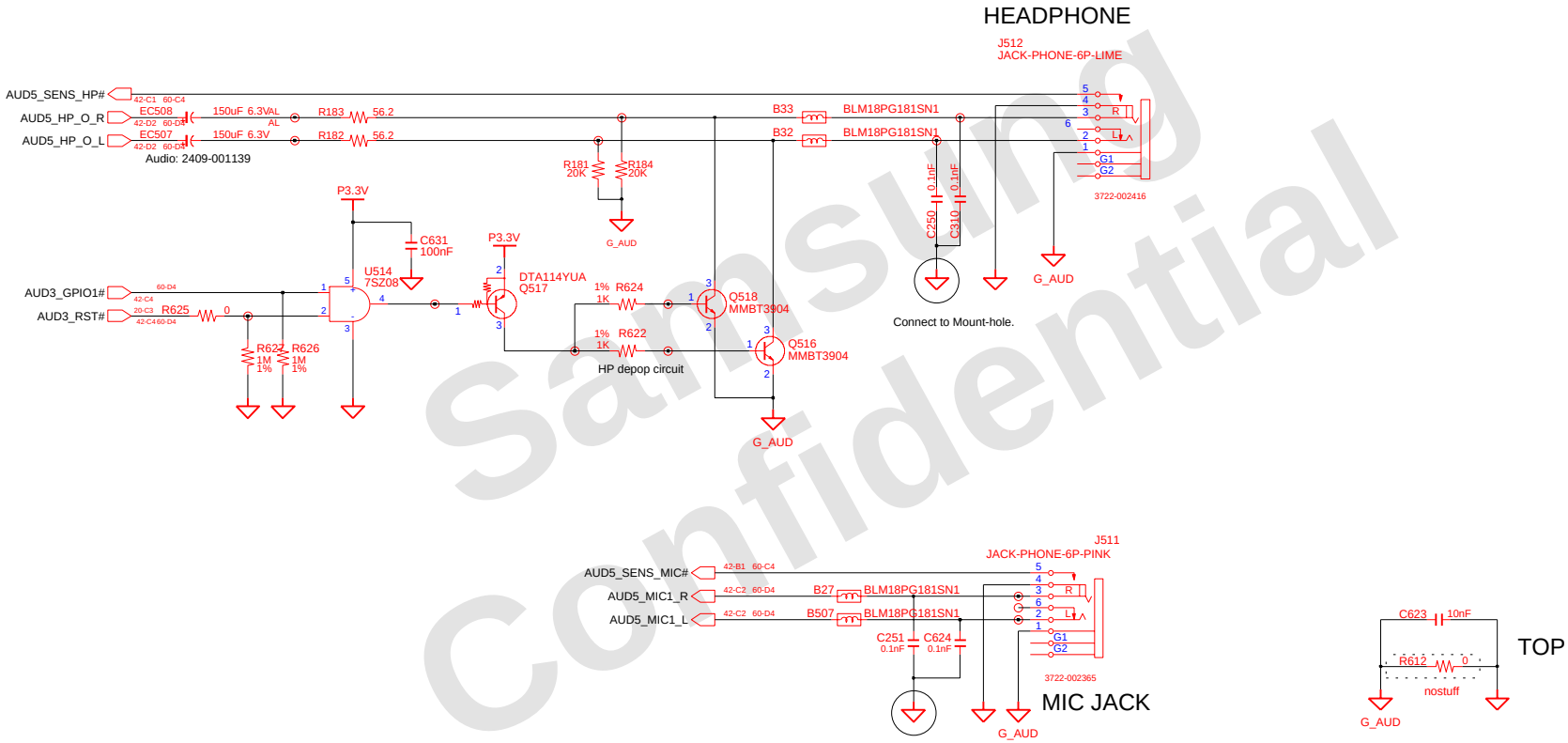




DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO HD AUDIO AUDIO POWER & SPEAKER	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 43 OF 60	



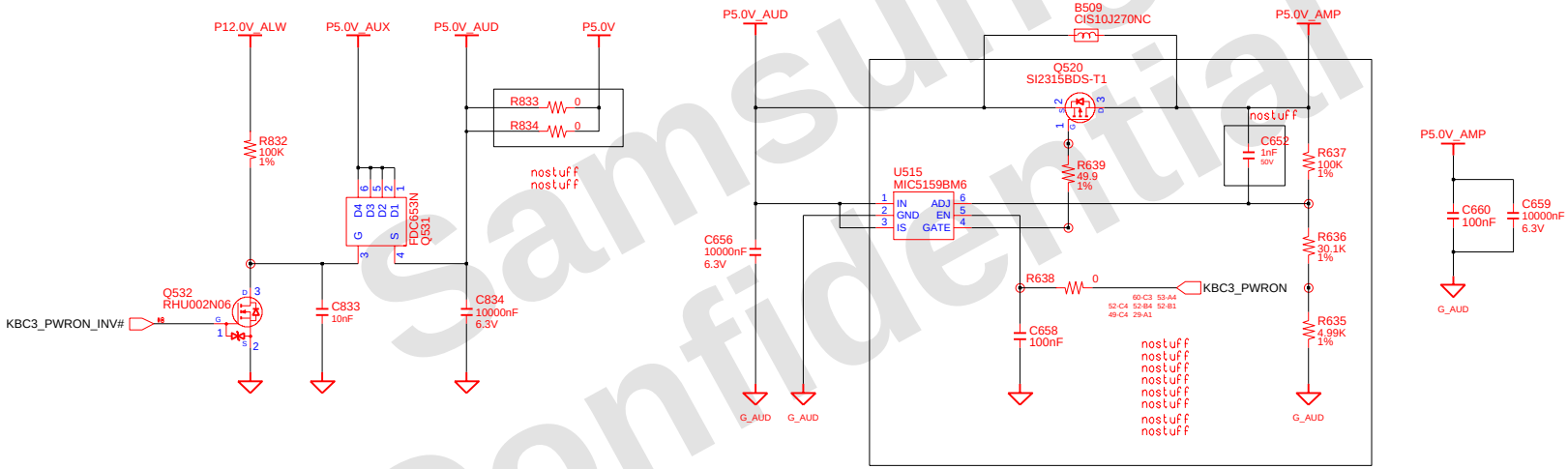
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO HD AUDIO MONO MIC	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 44 OF 60	



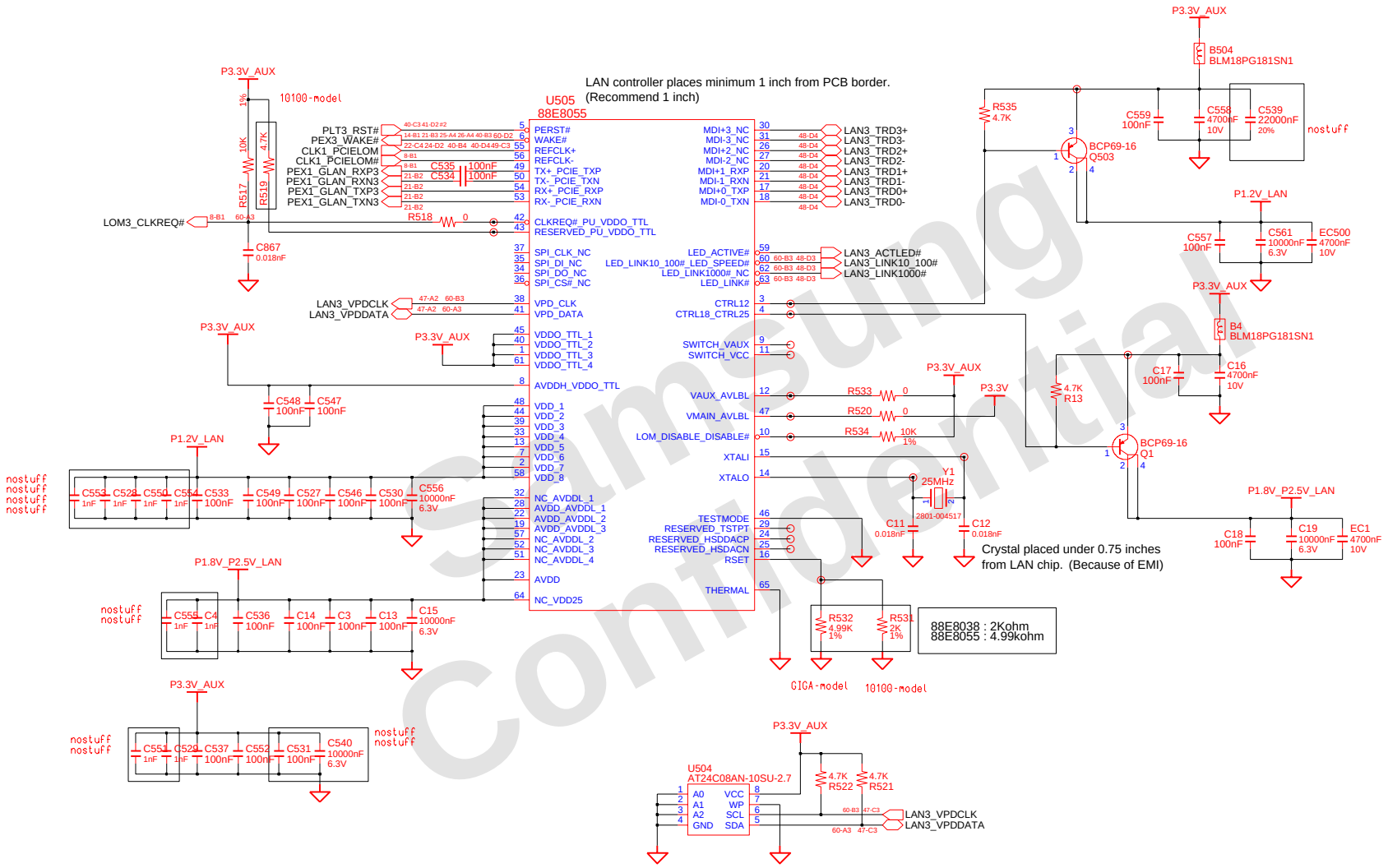
The traces led to Audio Jacks have the width over 10mil

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO HD AUDIO HEAD PHON & MIC JACK	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 45 OF 60	

AUDIO POWER

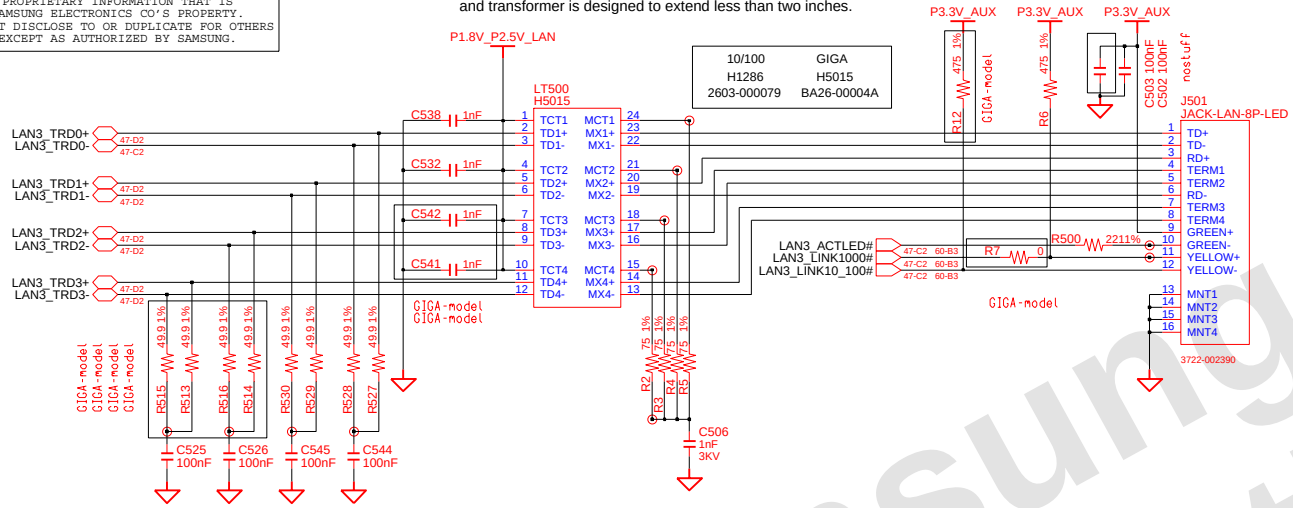


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO HD AUDIO AUDIO AMP POWER	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 46 OF 60	

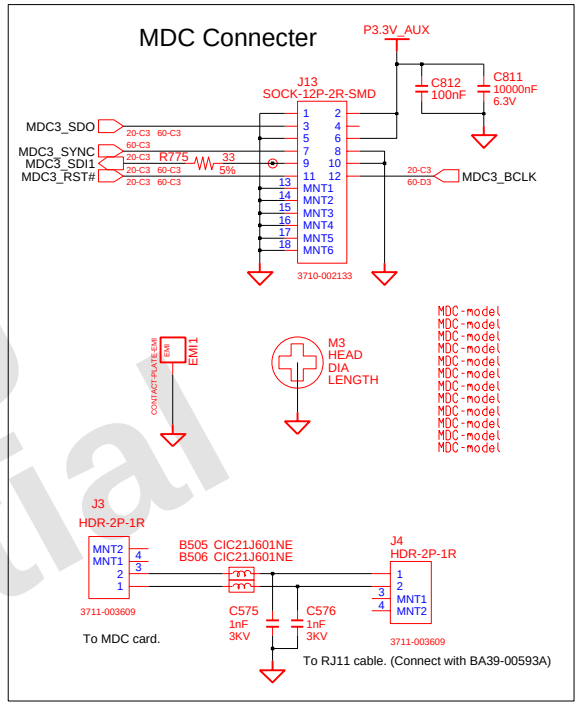


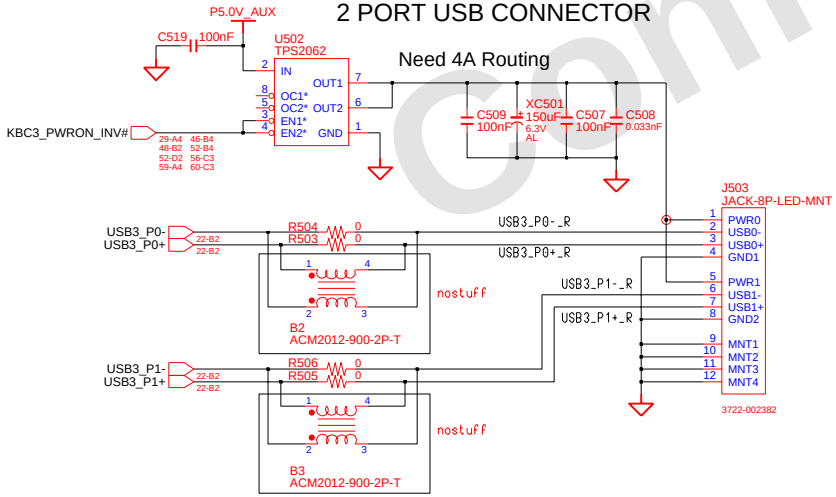
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO WIRE LAN 82566/NINEVEH	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 47 OF 60	

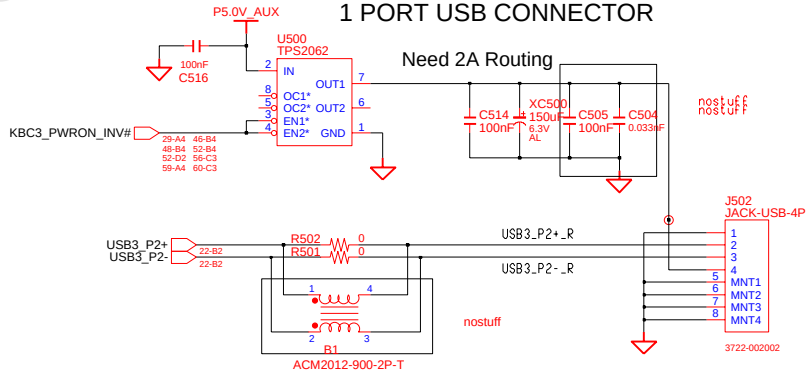
The distance between LAN controller and transformer is designed to extend less than two inches.



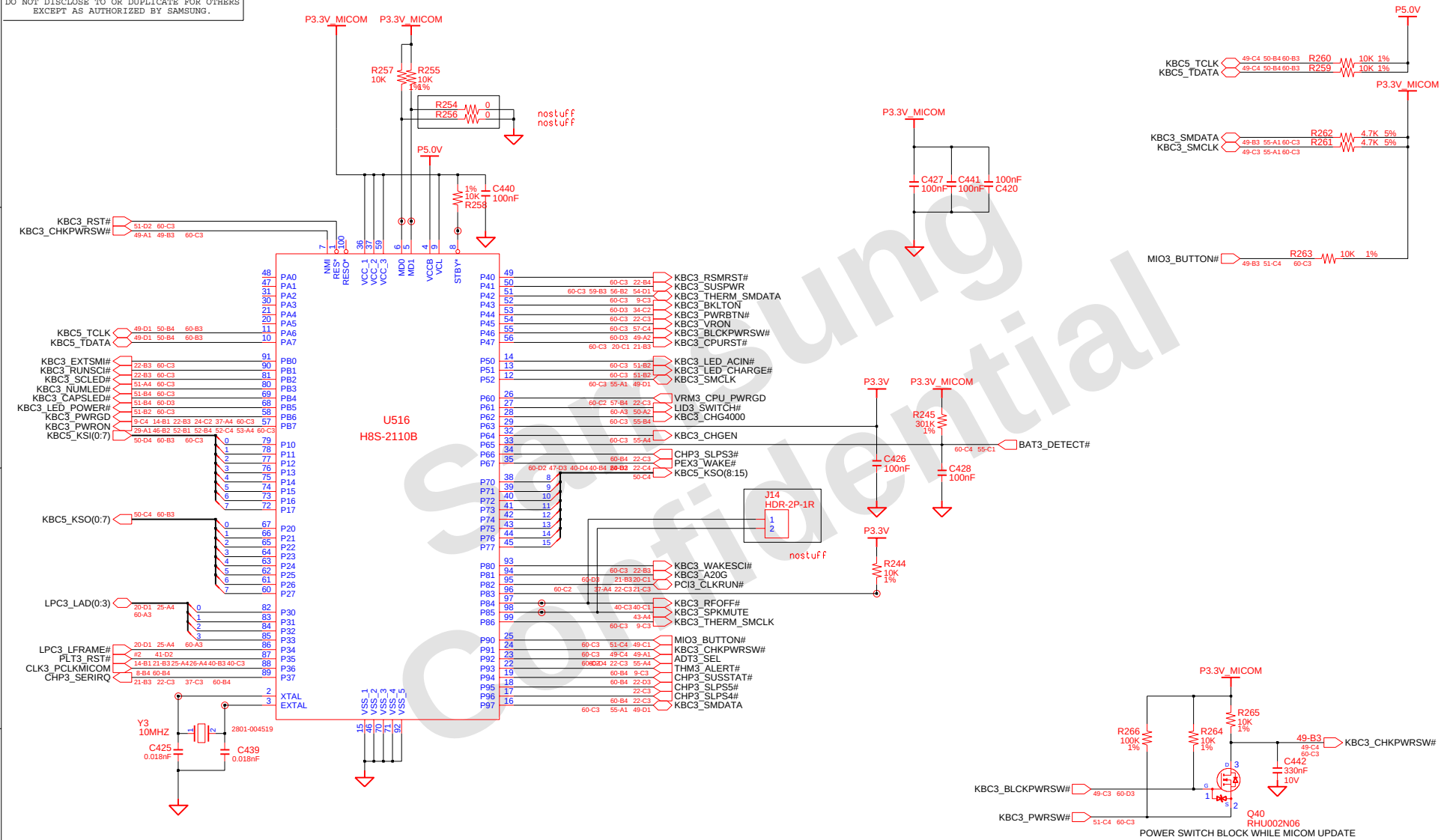
Place near to the Marvell chip.





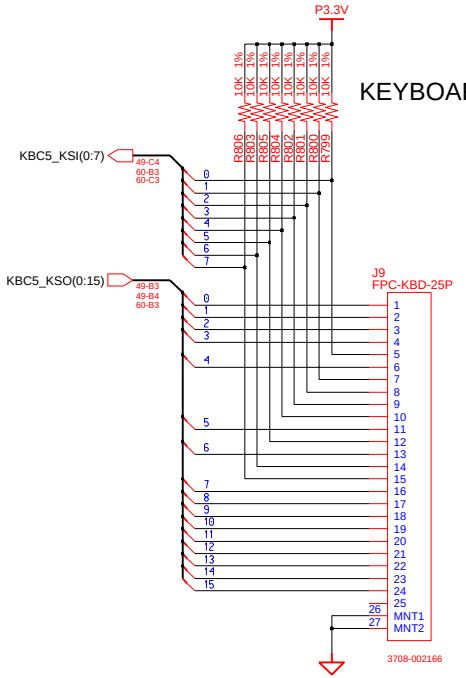


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO WIRED LAN RJ45 USB & MODEM	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 48 OF 60	

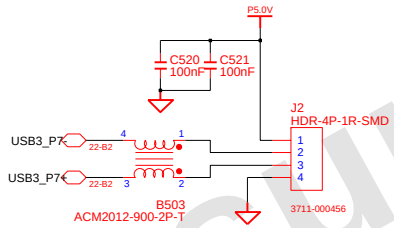


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO MICOM H8S-2110B	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 49 OF 60	

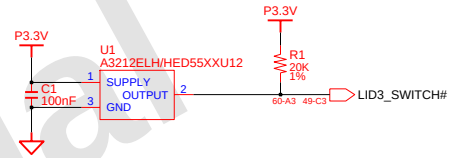
KEYBOARD



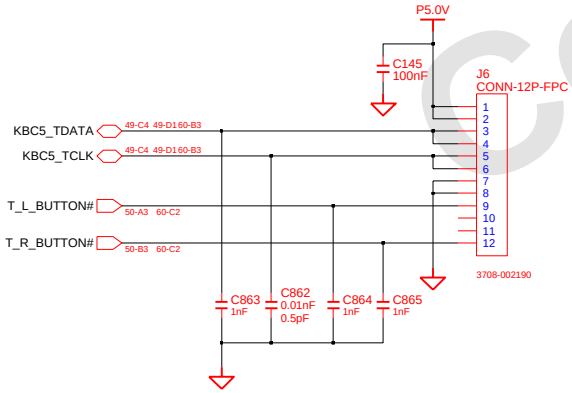
CAMERA

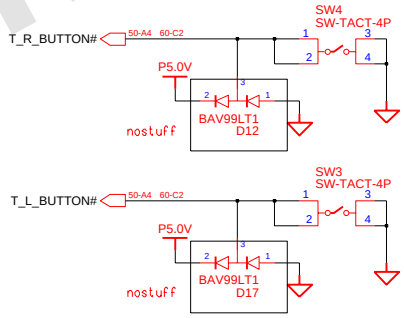


LID_SWITCH

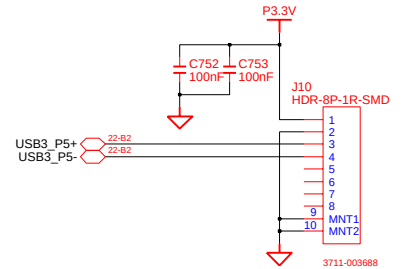


TOUCHPAD





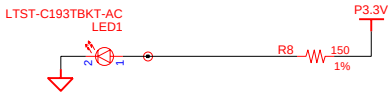
Bluetooth Interface

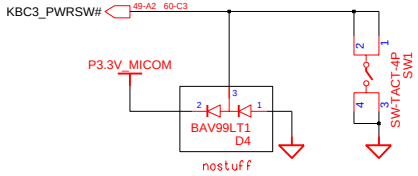


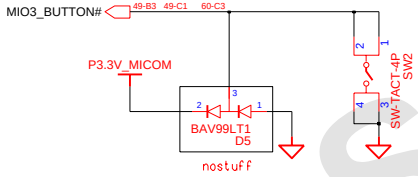
Need to check

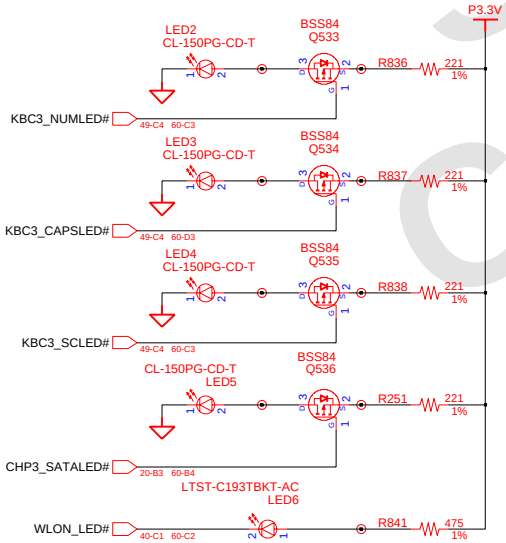
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO KEYBOSARD CONNECTORS	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 50 OF 60	

Power LED, Blue color

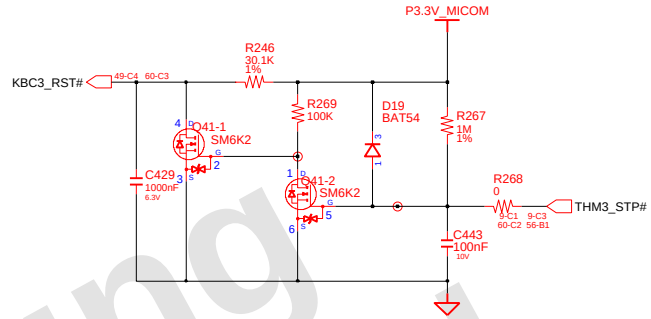




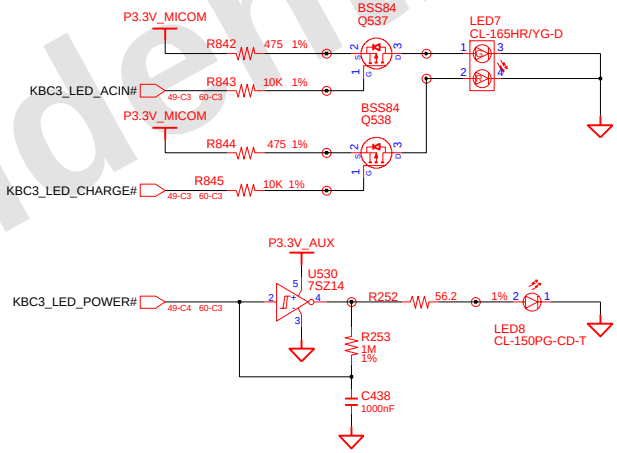




MICOM RESET

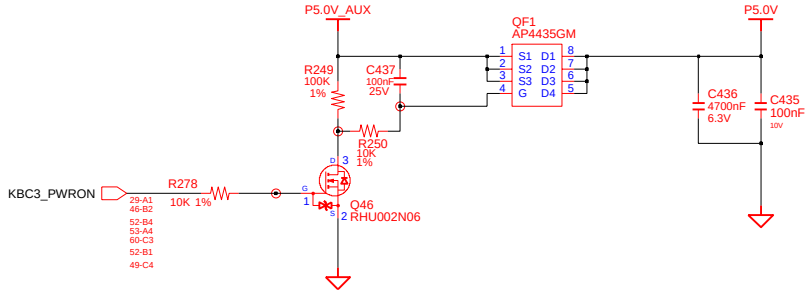


ADAPTERIN/CHARGING LED

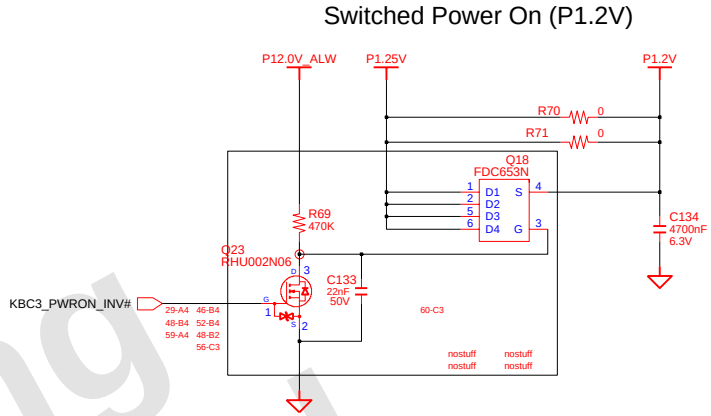


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO LED LOGICS LED LOGICS	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 51 OF 60	

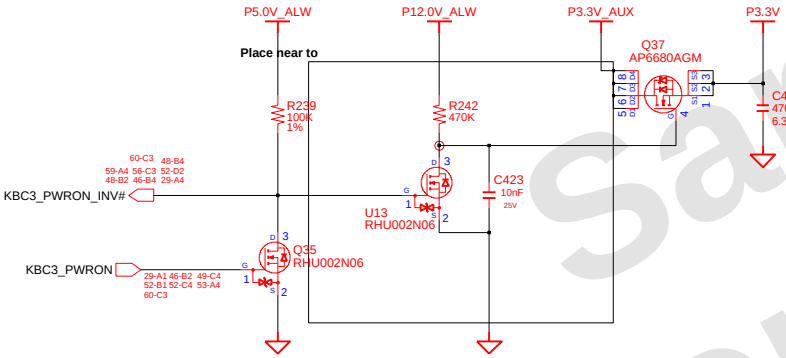
Switched Power On (P5.0V)



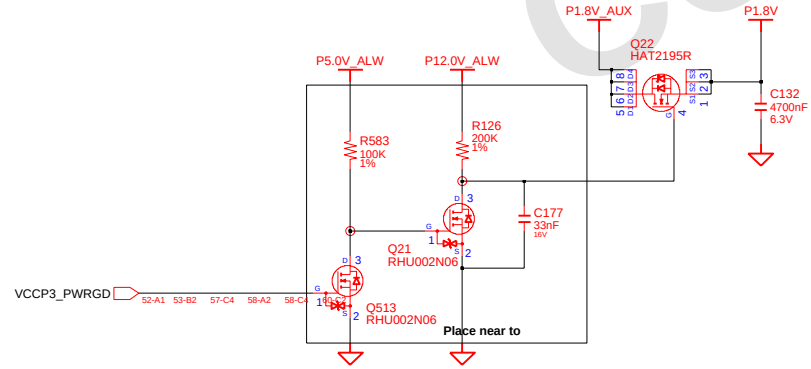
Switched Power On (P1.2V)

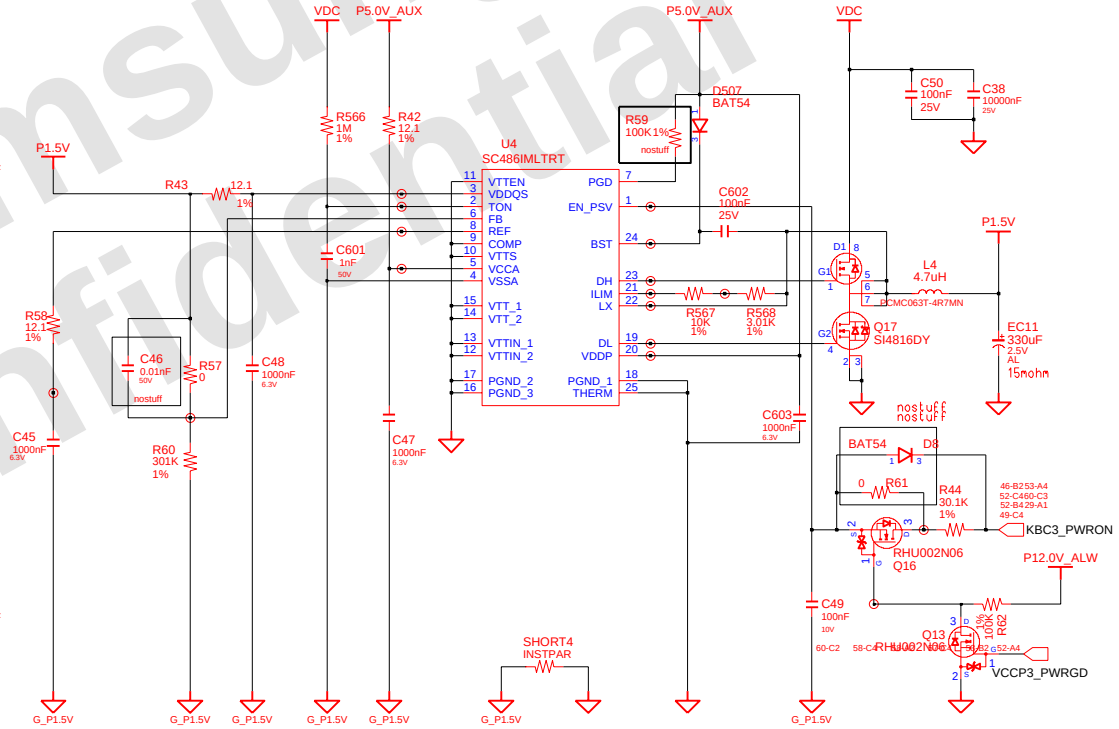


Switched Power On (P3.3V)

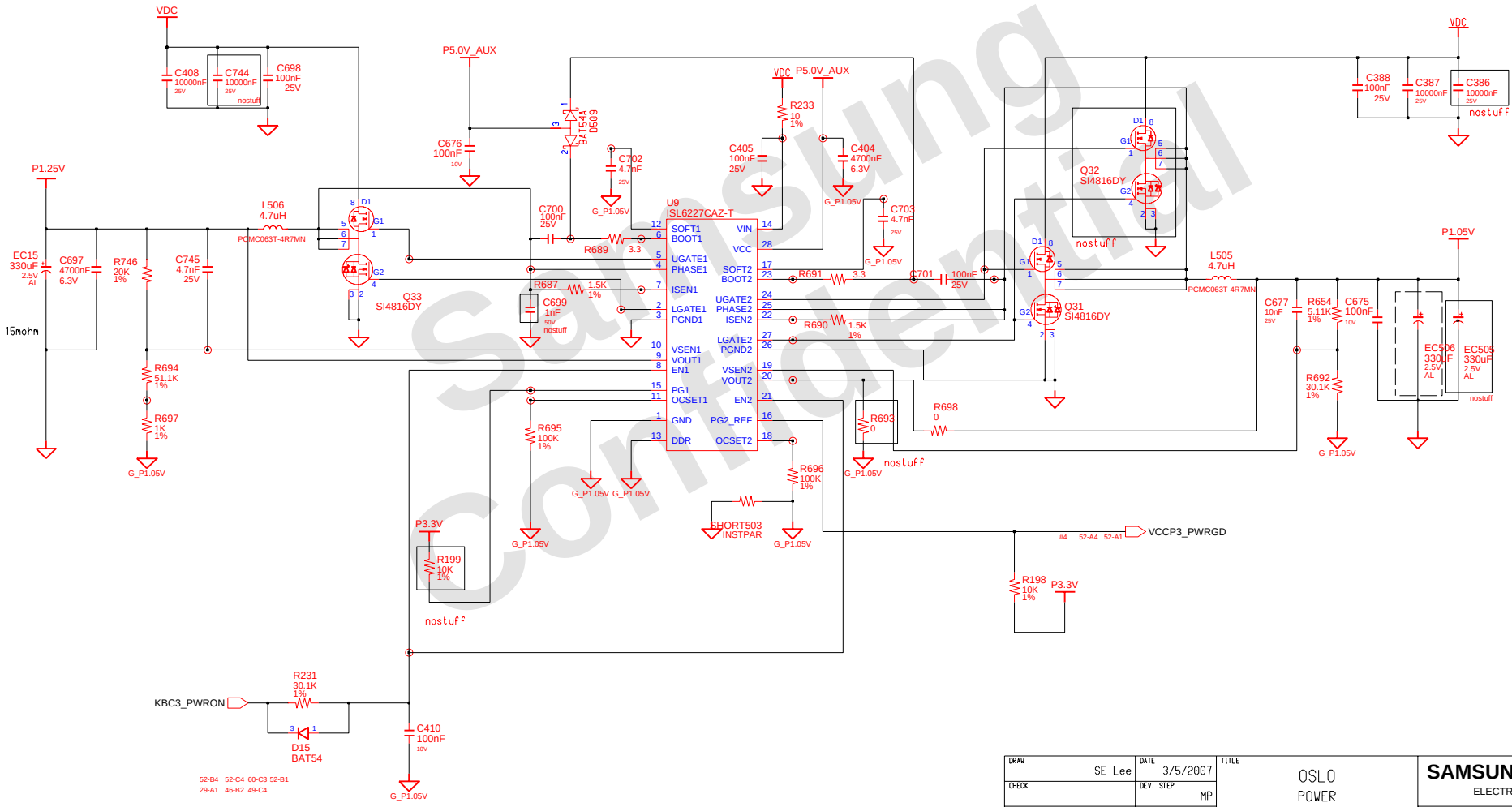


Switched Power On (P1.8V)



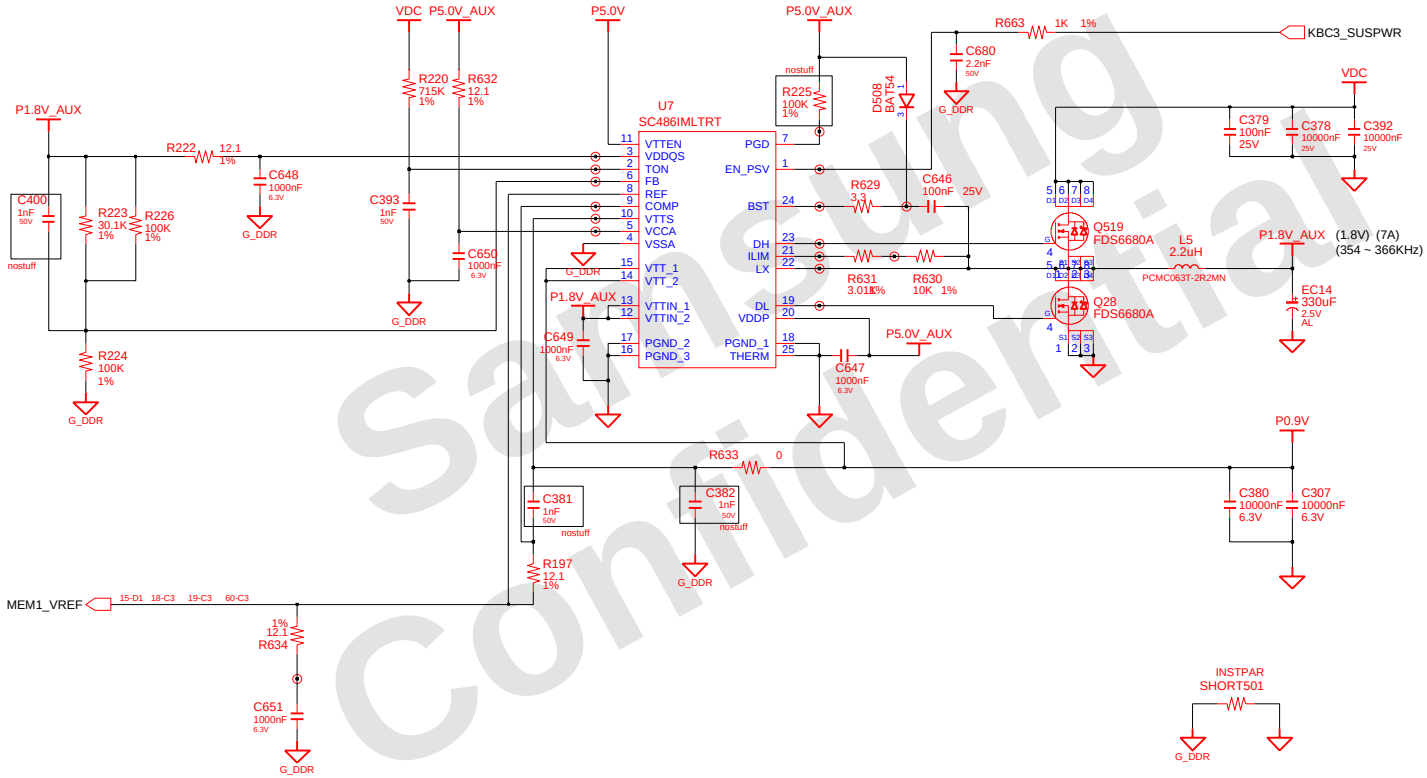


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO POWER SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		PART NO.: BA41-#####A
APPROVAL	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 52 OF 60	



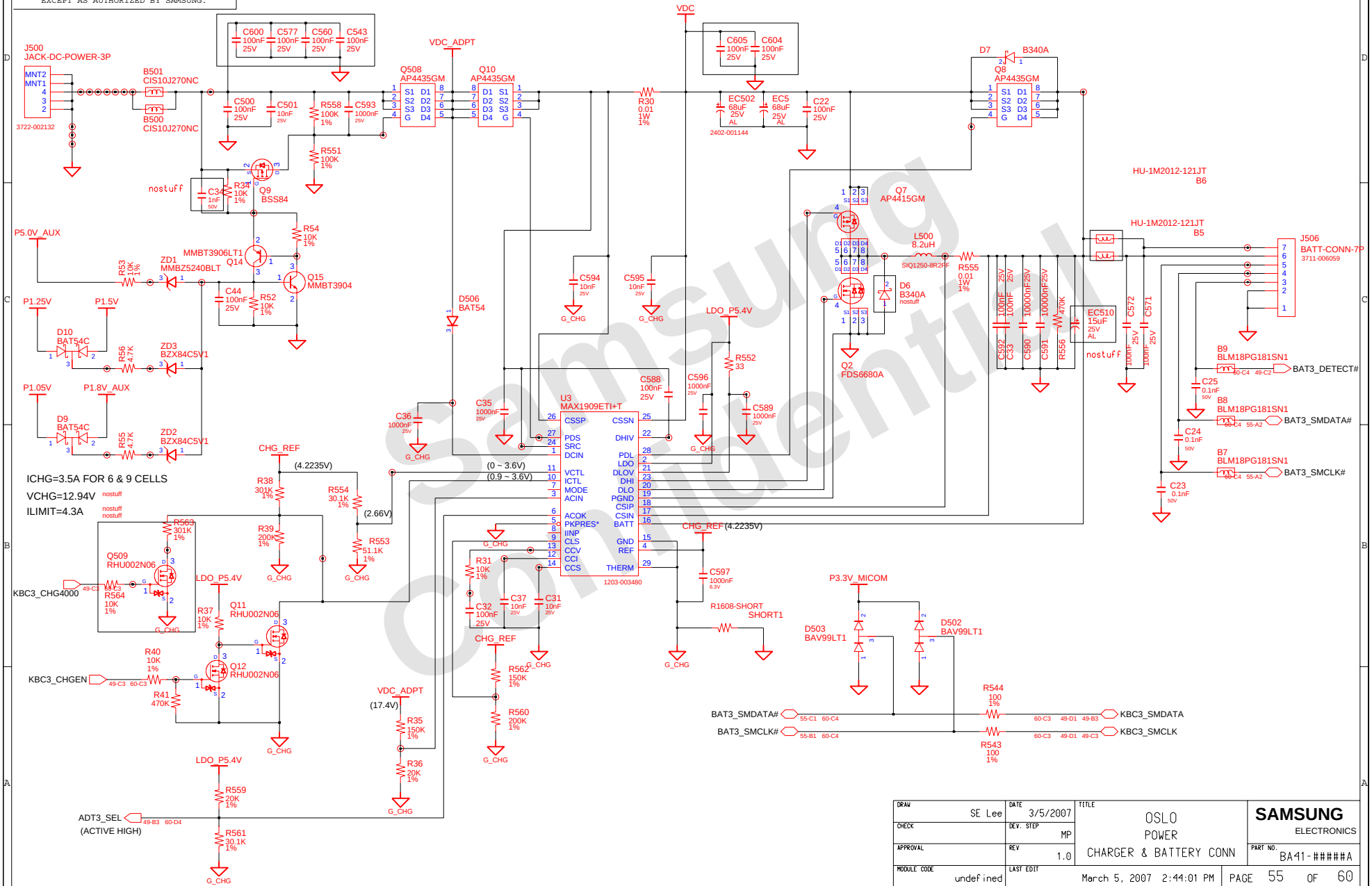
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO POWER ISL6227	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 53 OF 60	

DDR2 Power



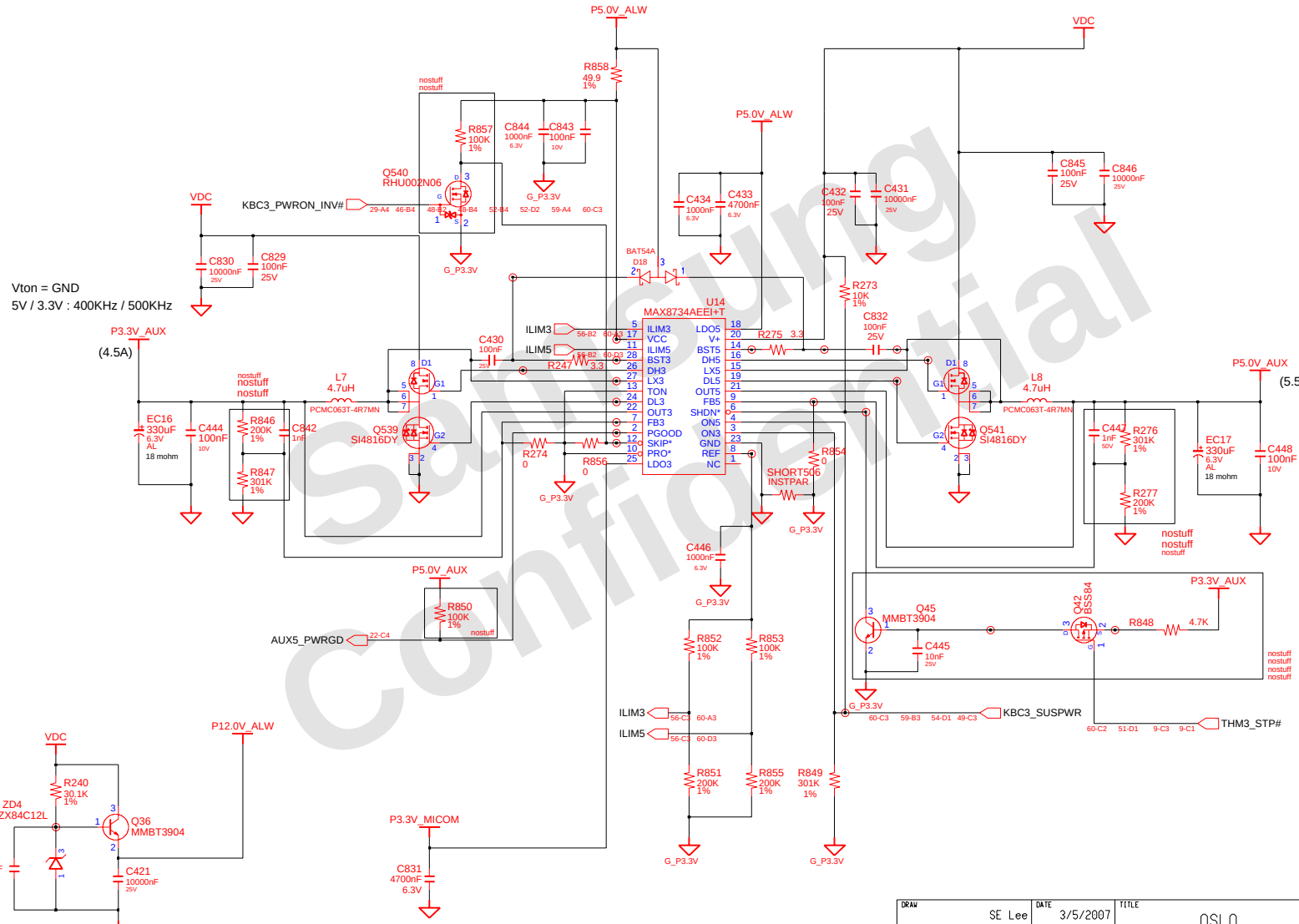
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO POWER DDR2 POWER	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		PART NO.: BA41-#####A
APPROVAL:	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 54 OF 60	

CHARGER & POWER MANAGEMENT



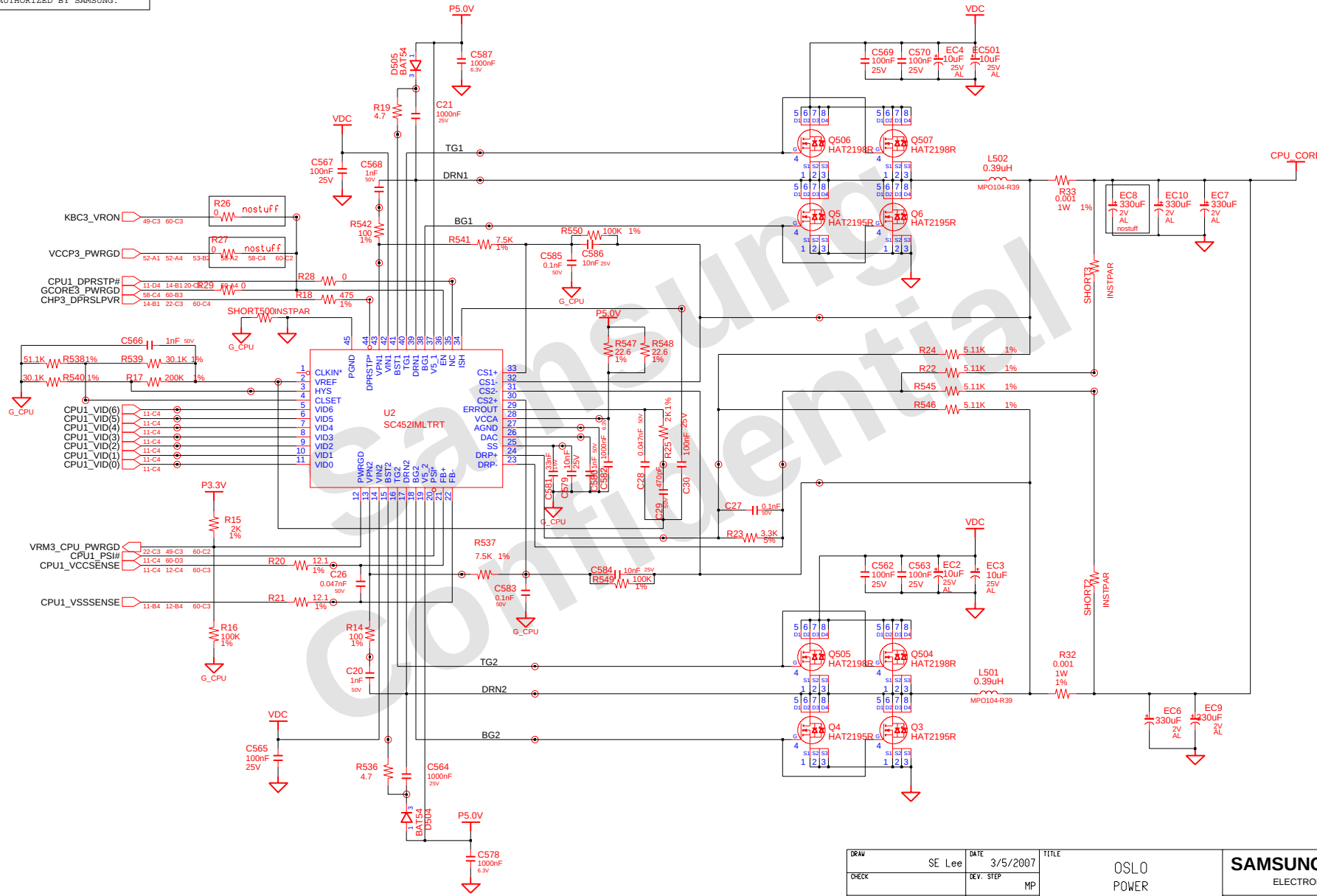
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO POWER CHARGER & BATTERY CONN	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-######A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 55 OF 60	

P3.3V_AUX & P5.0V_AUX



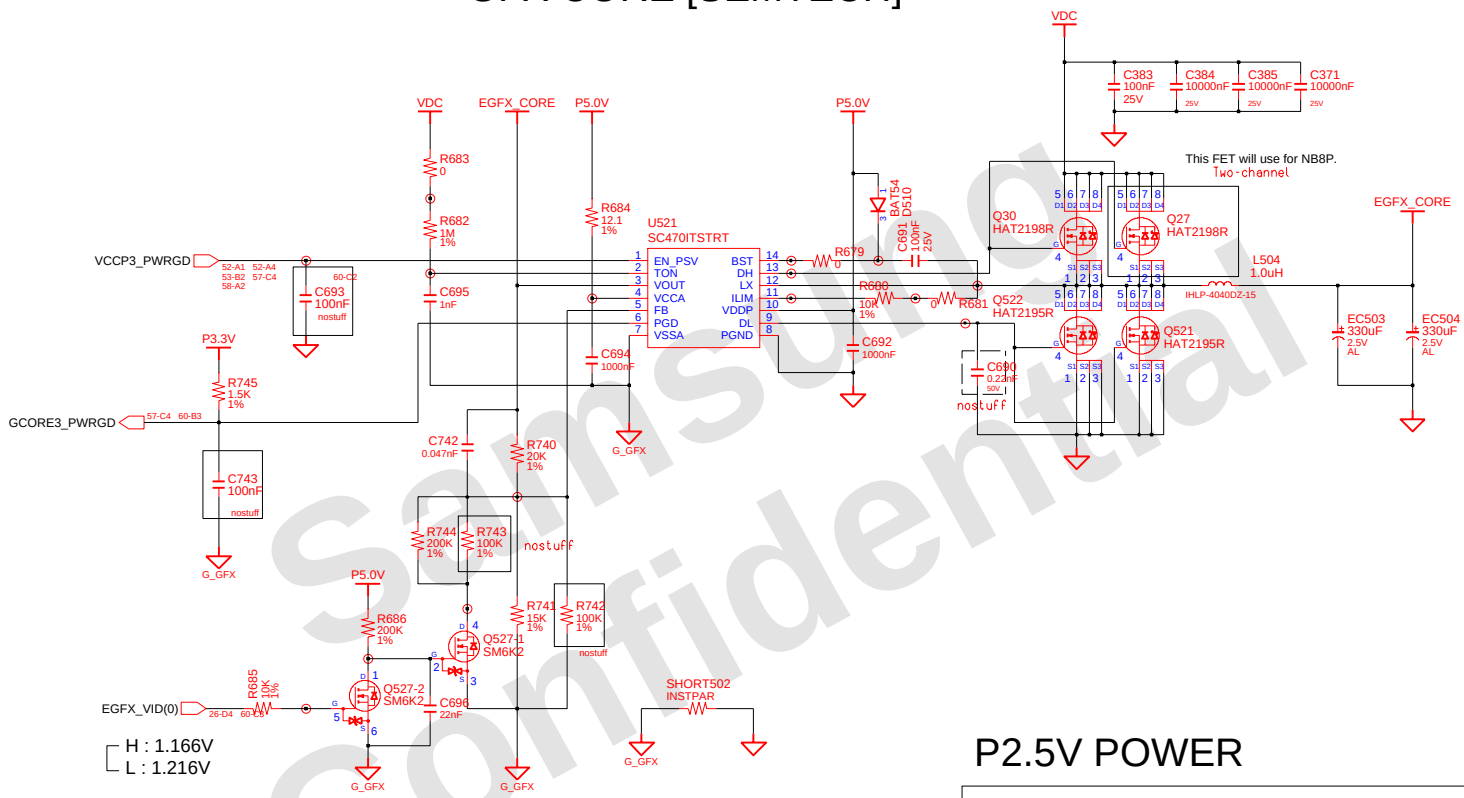
DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO POWER ALWS/AUX POWER	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 56 OF 60	

CPU VRM [SEMTECH]

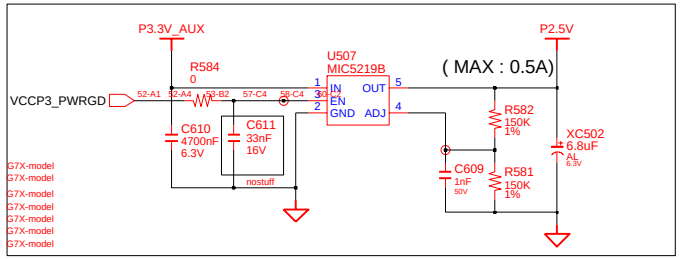


DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO POWER CPUI VRM (IMVP6+)	SAMSUNG ELECTRONICS
CHECK	DEV. STEP: MP		
APPROVAL	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 57 OF 60	

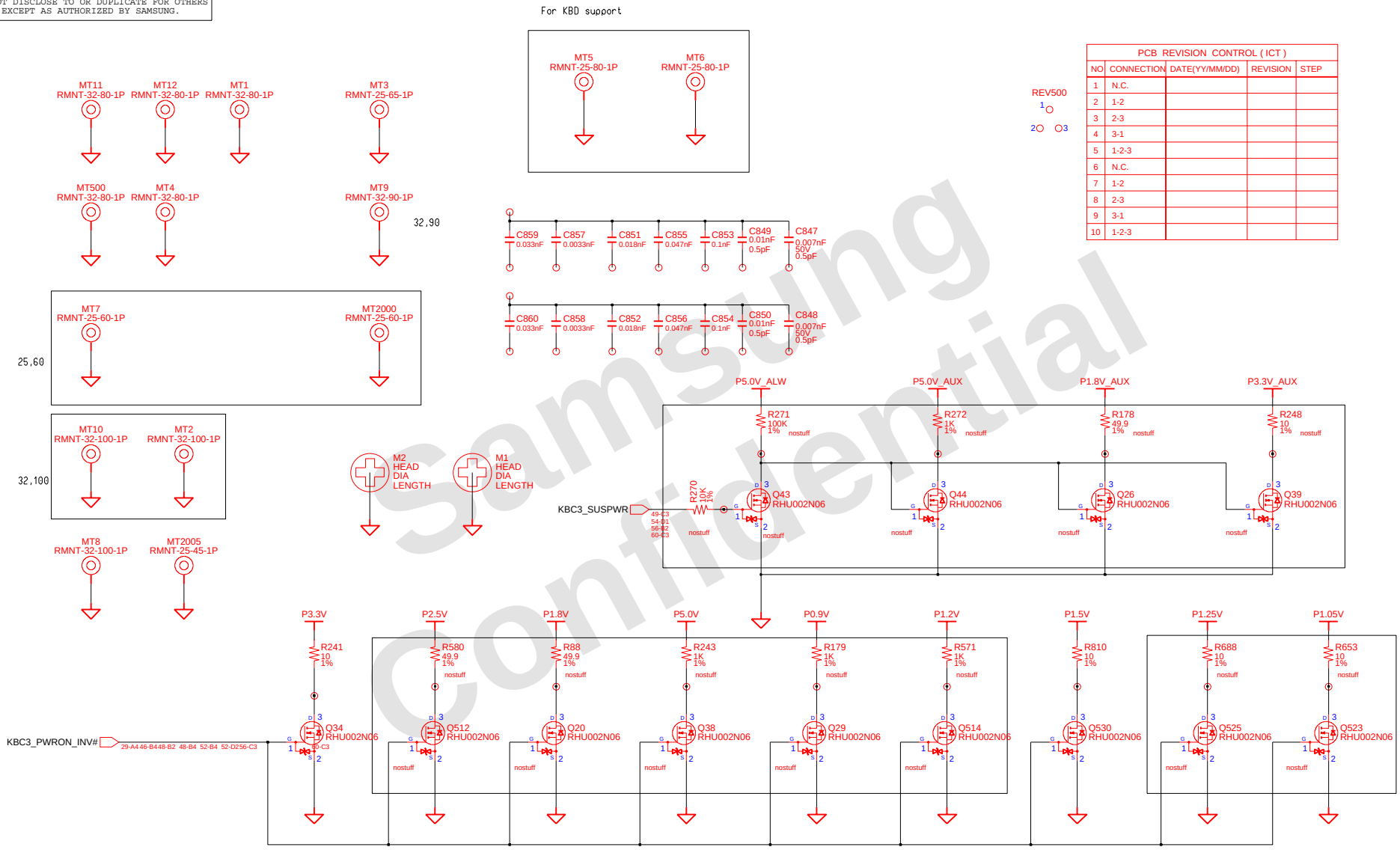
GFX CORE [SEMTECH]



P2.5V POWER



DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO POWER GFX CORE VRM	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 58 OF 60	



PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO ETC DISCHARGING LOGIC	SAMSUNG ELECTRONICS
CHECK:	DEV. STEP: MP		
APPROVAL:	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE: undefined	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 59 OF 60	

- ADT3_SEL
- AUD3_BCLK
- AUD3_BEEP
- AUD3_GPIO0#
- AUD3_GPIO1#
- AUD3_RST#
- AUD3_SDI0
- AUD3_SDO
- AUD3_SHDN#
- AUD3_SPDIF_OUT
- AUD3_SPKR
- AUD3_SYNC
- AUD5_HP_O_L
- AUD5_HP_O_R
- AUD5_LINE_O_L
- AUD5_LINE_O_R
- AUD5_MIC1_L
- AUD5_MIC1_R
- AUD5_MIC1_VREF_L
- AUD5_MIC1_VREF_R
- AUD5_MIC2_L
- AUD5_MIC2_R
- AUD5_MIC2_VREF
- AUD5_SENS_A
- AUD5_SENS_HP#
- AUD5_SENS_MIC#

- BAT3_DETECT#
- BAT3_SMCLK#
- BAT3_SMDATA#
- CBS3_A_A_18
- CBS3_A_A_19
- CBS3_A_D_14
- CBS3_A_D_2
- CBS3_CAD(0)
- CBS3_CAD(1)
- CBS3_CAD(10)
- CBS3_CAD(11)
- CBS3_CAD(12)
- CBS3_CAD(13)
- CBS3_CAD(14)
- CBS3_CAD(15)
- CBS3_CAD(16)
- CBS3_CAD(17)
- CBS3_CAD(18)
- CBS3_CAD(19)
- CBS3_CAD(2)
- CBS3_CAD(20)
- CBS3_CAD(21)
- CBS3_CAD(22)
- CBS3_CAD(23)
- CBS3_CAD(24)
- CBS3_CAD(25)
- CBS3_CAD(26)
- CBS3_CAD(27)
- CBS3_CAD(28)
- CBS3_CAD(29)
- CBS3_CAD(3)
- CBS3_CAD(30)
- CBS3_CAD(31)
- CBS3_CAD(4)
- CBS3_CAD(5)
- CBS3_CAD(6)
- CBS3_CAD(7)
- CBS3_CAD(8)
- CBS3_CAD(9)
- CBS3_CAUDIO
- CBS3_CCBE0#
- CBS3_CCBE1#
- CBS3_CCBE2#
- CBS3_CCBE3#
- CBS3_CCD1#
- CBS3_CCD2#
- CBS3_CCLK
- CBS3_CCLKRUN#
- CBS3_CDEVSEL#
- CBS3_CFRAME#
- CBS3_CGNT#
- CBS3_CINT#
- CBS3_CIRDY#
- CBS3_CPAR
- CBS3_CPERR#
- CBS3_CREQ#
- CBS3_CRST#
- CBS3_CSERR#
- CBS3_CSTOP#
- CBS3_CSTSCHG
- CBS3_CTRDY#
- CBS3_CVS1
- CBS3_CVS2
- CBS3_MD_CLK
- CBS3_MD_DATA0_MS_SDIO
- CBS3_MD_DATA1
- CBS3_MD_DATA2
- CBS3_MD_DATA3
- CBS3_MD_DATA4_XD
- CBS3_MD_DATA5_XD
- CBS3_MD_DATA6_XD
- CBS3_MD_DATA7_XD
- CBS3_MD_VCCEN
- CBS3_MD_XD_ALE
- CBS3_MD_XD_CE#
- CBS3_MD_XD_CLE
- CBS3_MD_XD_WP#
- CBS3_MS_BS_SD_CMD
- CBS3_MS_INS_XD_CD#
- CBS3_SD_CD_XD_CD#
- CBS3_SD_WP_XD_R_B#
- CBS3_VCC3EN#
- CBS3_VCC5EN#
- CBS3_VPPEN0
- CBS3_VPPEN1
- CHP3_BIOSWP#
- CHP3_BIOS_CRI#
- CHP3_CL_CLK_0
- CHP3_CL_DATA_0
- CHP3_CL_RST#_0
- CHP3_CL_RST#_1
- CHP3_CPUSTP#
- CHP3_DPRSLPVR
- CHP3_EXTGFX#
- CHP3_GPIO12
- CHP3_GPIO18
- CHP3_GPIO20
- CHP3_GPIO29
- CHP3_GPIO37
- CHP3_INTRUDER#
- CHP3_INTVRMEN
- CHP3_LAN100_SLP
- CHP3_PCISTP#
- CHP3_RTCRST#
- CHP3_SATACLKREQ#
- CHP3_SATALED#
- CHP3_SERIRQ
- CHP3_SLPS3#
- CHP3_SLPS4#
- CHP3_SLPS5#
- CHP3_SUSSTAT#
- CLK1_DREFSSCLK#_R
- CLK3_DBGLPC
- CLK3_FM48
- CLK3_GFX_27M
- CLK3_GFX_27M_SS
- CLK3_ICH14
- CLK3_PCLKCB
- CLK3_PCLKICH
- CLK3_PCLKMICOM
- CLK3_PWRGD
- CLK3_USB48
- CPU1_A20M#
- CPU1_ADS#
- CPU1_BNR#
- CPU1_BPRI#
- CPU1_BREQ#
- CPU1_DBSY#
- CPU1_DEFER#
- CPU1_DPRSTP#
- CPU1_DPSLP#
- CPU1_DPWR#
- CPU1_DRDY#
- CPU1_FERR#
- CPU1_HIT#
- CPU1_HITM#
- CPU1_IGNNE#
- CPU1_INIT#
- CPU1_INTR
- CPU1_LOCK#
- CPU1_NMI
- CPU1_PSI#
- CPU1_PWRGDCPU
- CPU1_RS0#
- CPU1_RS1#
- CPU1_RS2#
- CPU1_SLP#
- CPU1_SMI#
- CPU1_STPCLK#
- CPU1_TCK
- CPU1_TDI
- CPU1_THRMTRIP#
- CPU1_TMS
- CPU1_TRDY#
- CPU1_TRST#
- CPU1_VCCSENSE
- CPU1_VSSSENSE
- CPU2_THERMDA
- CPU2_THERMDC
- CPU3_THRMTRIP#
- CPU_CORE_HG1
- CPU_CORE_LG1
- CPU_CORE_PHASE_1
- CR13_BLUE
- CR13_DDCCLK
- CR13_DDCDATA
- CR13_GREEN
- CR13_HSYNC
- CR13_RED
- CR13_VSYNC
- CR15_DDCCLK
- CR15_DDCDATA
- CR15_HSYNC
- CR15_VSYNC
- EGFX_VID(0)

- FAN3_FDBACK#
- FAN5_VDD
- GCORE3_PWRGD
- GFX3_HCLK
- GFX3_HDATA
- GFX3_THERM#
- GFX3_THERMDN
- GFX3_THERMDP
- IDE5_A0
- IDE5_A1
- IDE5_A2
- IDE5_CS1#
- IDE5_CS3#
- IDE5_D(0)
- IDE5_D(1)
- IDE5_D(10)
- IDE5_D(11)
- IDE5_D(12)
- IDE5_D(13)
- IDE5_D(14)
- IDE5_D(15)
- IDE5_D(2)
- IDE5_D(3)
- IDE5_D(4)
- IDE5_D(5)
- IDE5_D(6)
- IDE5_D(7)
- IDE5_D(8)
- IDE5_D(9)
- IDE5_DACK#
- IDE5_DREQ
- IDE5_IDEIRQ
- IDE5_IOR#
- IDE5_IORDY
- IDE5_IOW#
- ILIM3
- ILIM5
- KBC3_A20G
- KBC3_BKLTON
- KBC3_BLCKPWRSW#
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND

- KBC3_CAPSLED#
- KBC3_CHG4000
- KBC3_CHGEN
- KBC3_CHKPWRSW#
- KBC3_CPURST#
- KBC3_EXTSMI#
- KBC3_LED_ACIN#
- KBC3_LED_CHARGE#
- KBC3_LED_POWER#
- KBC3_NUMLED#
- KBC3_PWRBTN#
- KBC3_PWRGD
- KBC3_PWRON
- KBC3_PWRON_INV#
- KBC3_PWRSW#
- KBC3_RSMRST#
- KBC3_RST#
- KBC3_RST#_ONRC
- KBC3_RUNSCI#
- KBC3_SCLED#
- KBC3_SMCLK
- KBC3_SMDATA
- KBC3_SUSPWR
- KBC3_THERM_SMCLK
- KBC3_THERM_SMDATA
- KBC3_VPON
- KBC3_WAKESCI#
- KBC5_KSI(0)
- KBC5_KSI(1)
- KBC5_KSI(2)
- KBC5_KSI(3)
- KBC5_KSI(4)
- KBC5_KSI(5)
- KBC5_KSI(6)
- KBC5_KSI(7)
- KBC5_KSO(0)
- KBC5_KSO(1)
- KBC5_KSO(10)
- KBC5_KSO(11)
- KBC5_KSO(12)
- KBC5_KSO(13)
- KBC5_KSO(14)
- KBC5_KSO(15)
- KBC5_KSO(2)
- KBC5_KSO(3)
- KBC5_KSO(4)
- KBC5_KSO(5)
- KBC5_KSO(6)
- KBC5_KSO(7)
- KBC5_KSO(8)
- KBC5_KSO(9)
- KBC5_TCLK
- KBC5_TDATA
- LAN3_ACTLED#
- LAN3_LINK1000#
- LAN3_LINK10_100#
- LAN3_VPDCLK
- LAN3_VPDDATA
- LCD3_BKLTON
- LCD3_BRIT
- LCD3_EDID_CLK
- LCD3_EDID_DATA
- LID3_SWITCH#
- LOM3_CLKREQ#
- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)
- LPC3_LFRAME#

- MAX8734_FB3
- MAX8734_FB5

- MCH1_HVREF
- MCH1_HXSWING
- MCH3_BMBUSY#
- MCH3_CLKREQ#
- MCH3_CL_VREF
- MCH3_EXTTS0#
- MCH3_EXITS1#
- MCH3_ICHSYNC#
- MDC3_BCLK
- MDC3_RST#
- MDC3_SDI1
- MDC3_SDO
- MDC3_SYNC
- MEM1_VREF
- MIN3_CLKREQ#
- MIO3_BUTTON#

- P1.5V_PWRGD
- P3.3V_ALW_BST

- P3.3V_ALW_PHASE
- P5.0V_AUX_HG
- P5.0V_AUX_LG
- P5.0V_AUX_PHASE
- PCI3_AD(0)
- PCI3_AD(1)
- PCI3_AD(10)
- PCI3_AD(11)
- PCI3_AD(12)
- PCI3_AD(13)
- PCI3_AD(14)
- PCI3_AD(15)
- PCI3_AD(16)
- PCI3_AD(17)
- PCI3_AD(18)
- PCI3_AD(19)
- PCI3_AD(2)
- PCI3_AD(20)
- PCI3_AD(21)
- PCI3_AD(22)
- PCI3_AD(23)
- PCI3_AD(24)
- PCI3_AD(25)
- PCI3_AD(26)
- PCI3_AD(27)
- PCI3_AD(28)
- PCI3_AD(29)
- PCI3_AD(3)
- PCI3_AD(30)
- PCI3_AD(31)
- PCI3_AD(4)
- PCI3_AD(5)
- PCI3_AD(6)
- PCI3_AD(7)
- PCI3_AD(8)
- PCI3_AD(9)
- PCI3_CBE0#
- PCI3_CBE1#
- PCI3_CBE2#
- PCI3_CBE3#
- PCI3_CLKRUN#
- PCI3_DEVSEL#
- PCI3_FRAME#
- PCI3_GNT0#
- PCI3_INTA#
- PCI3_INTB#
- PCI3_INTC#
- PCI3_INTD#
- PCI3_IRDY#
- PCI3_PAR
- PCI3_PERR#
- PCI3_PLOCK#
- PCI3_REQ0#
- PCI3_RST#
- PCI3_SERR#
- PCI3_STOP#
- PCI3_TRDY#
- PEG3_DVI_DETECT
- PEG3_HDMI_CLK_EXT
- PEG3_HDMI_DATA_EXT
- PEG3_LCD_BKLTEN
- PEG3_LCD_VDDON
- PEG3_M10B(0)
- PEG3_M10B(1)
- PEG3_M10B(11)
- PEG3_M10B(3)
- PEG3_M10B(4)
- PEG3_M10B(5)
- PEG3_M10B(8)
- PEG3_M10B(9)
- PEG3_M10B_CTL3

- PEX3_WAKE#
- PLT3_RST#
- PLT3_RST_ORG#

- SC452_CS1*
- SC452_ERROUT

- SMB3_ALERT#
- SMB3_CLK
- SMB3_DATA
- SMB3_ME_CLK
- SMB3_ME_DATA
- SPI3_CLK
- SPI3_CS0#
- SPI3_CS1#
- SPI3_MISO
- SPI3_MOSI
- SPK5_L+
- SPK5_L-
- SPK5_R+
- SPK5_R-
- THM3_ALERT#
- THM3_STP#
- T_L_BUTTON#
- T_R_BUTTON#
- VCCP3_PWRGD
- VRM3_CPU_PWRGD
- WLON_LED#
- 0.7VDDQA
- VDC_ADPT
- VDC_ADPT
- VDC_ADPT
- VDC_INV
- VDC_INV
- VDC_INV

- 0.7VDDQA
- 0.7VDDQA
- 0.7VDDQA
- 0.7VDDQC
- 0.7VDDQC
- 0.7VDDQC
- 0.7VDDQC
- CB_MD_VCC
- CB_MD_VCC
- CB_MD_VCC
- CB_MD_VCC
- CB_VCCA
- CB_VCCA
- CB_VCCA
- CB_VCCA
- CB_VPPA
- CB_VPPA
- CB_VPPA
- CB_VPPA

- CHG_REF

- CPU_CORE
- CPU_CORE
- CPU_CORE
- CPU_CORE
- CPU_CORE
- EGFX_CORE
- EGFX_CORE
- EGFX_CORE
- EGFX_CORE

- G_CHG
- G_CHG
- G_CHG
- G_CHG
- G_DDR
- G_DDR
- G_DDR
- G_DDR
- G_DDR
- G_GFX
- G_GFX
- G_GFX
- G_GFX
- G_MIC
- G_MIC
- G_MIC
- G_MIC
- G_P1.05V
- G_P1.05V
- G_P1.05V
- G_P1.05V

- G_P1.5V
- G_P1.5V
- G_P3.3V
- G_P3.3V
- G_P3.3V
- G_P3.3V
- LCD_VDD3V
- LCD_VDD3V
- LCD_VDD3V
- LCD_VDD3V

- LDO_P5.4V
- LDO_P5.4V

- P0.9V
- P0.9V
- P0.9V
- P0.9V
- P1.05V
- P1.05V
- P1.05V
- P1.05V
- P1.05V_PEG
- P1.05V_PEG
- P1.05V_PEG
- P1.05V_PEG
- P1.25V

- P1.25V
- P1.25V
- P1.25V
- P1.2V
- P1.2V
- P1.2V
- P1.2V
- P1.2V_LAN
- P1.2V_LAN
- P1.2V_LAN
- P1.2V_LAN
- P1.5V
- P1.5V
- P1.5V
- P1.5V
- P1.5V
- P1.8V
- P1.8V
- P1.8V
- P1.8V_AUX
- P1.8V_AUX
- P1.8V_AUX
- P1.8V_AUX
- P1.8V_P2.5V_LAN
- P1.8V_P2.5V_LAN
- P1.8V_P2.5V_LAN
- P1.8V_P2.5V_LAN
- P12.0V_ALW
- P12.0V_ALW
- P12.0V_ALW
- P12.0V_ALW
- P2.5V
- P2.5V
- P2.5V
- P2.5V
- P3.3V
- P3.3V
- P3.3V
- P3.3V
- P3.3V_MICOM
- P3.3V_MICOM
- P3.3V_MICOM
- P3.3V_MICOM
- P4.75V_AUD
- P4.75V_AUD
- P4.75V_AUD
- P4.75V_AUD
- P5.0V
- P5.0V
- P5.0V
- P5.0V
- P5.0V_ALW
- P5.0V_ALW
- P5.0V_ALW
- P5.0V_ALW
- P5.0V_AMP
- P5.0V_AMP
- P5.0V_AMP
- P5.0V_AMP
- P5.0V_AUD
- P5.0V_AUD
- P5.0V_AUD
- P5.0V_AUD
- PRTC_BAT
- PRTC_BAT
- PRTC_BAT
- PRTC_BAT
- TMDS_PLLVDD
- TMDS_PLLVDD
- TMDS_PLLVDD
- TMDS_PLLVDD
- VCC_CRT
- VCC_CRT
- VCC_CRT
- VCC_CRT
- VDC
- VDC
- VDC
- VDC
- VDC_ADPT

DRAW: SE Lee	DATE: 3/5/2007	TITLE: OSLO TP TP	SAMSUNG ELECTRONICS
CHECK: ,	DEV. STEP: MP		
APPROVAL: ,	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: March 5, 2007 2:44:01 PM	PAGE 60 OF 60	