Three-Channel Voltage Console with I2C Programmable Current DAC in SOT23-8

General Description

The uP6262 is a high precision voltage console consisting of three sets I2C programmable current DACs. Each current DAC is capable of sinking 64-step and sourcing 16-step output current that are programmed by the I2C interface. The sinking and sourcing current of OUT1 and OUT2 are programmable for 20x boost respectively.

The uP6262 features soft-jump, easily interfacing with standard DC/DC converter for voltage console. The uP6262 is available in space-saving SOT23-8 package.

Ordering Information

Order Number	Package	Remark
uP6262M8	SOT23-8	

Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

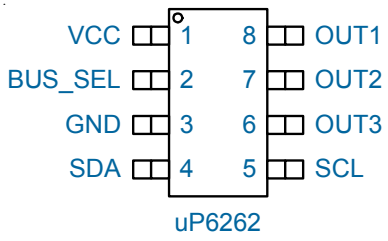
Features

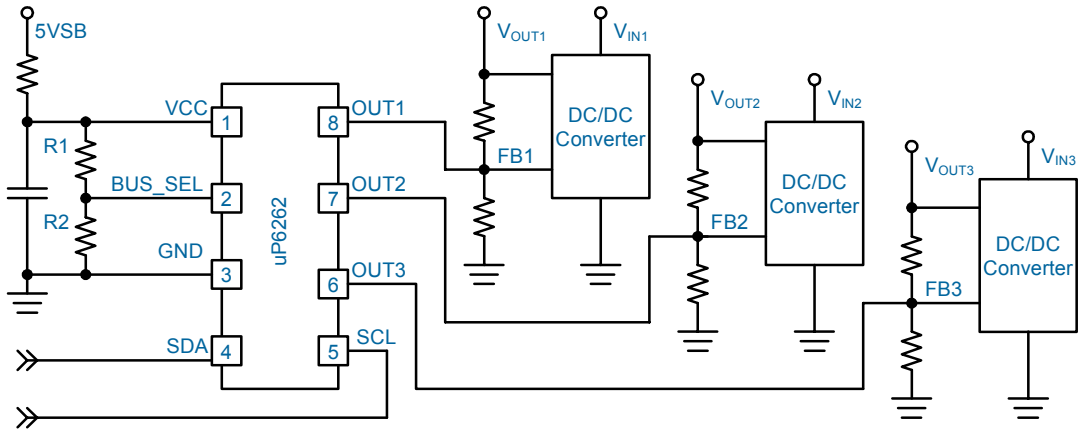
- Provide 3 Sets Current DACs
  - 6% Initial Accuracy
  - I2C Programmable 16-Step Sourcing Current
  - I2C Programmable 64-Step Sinking Current
  - Programmable Full Scale Current
- Internal Soft-Jump Function
- RoHS Compliant and 100% Lead (Pb)- Free
- Low External Component Count
- Low Cost and Easy to Use
- Small Footprint SOT23-8 Package
- Patent Pending

Applications

- Power Supply Adjustment for M/B and VGA
- Power Supply Margining
- Adjustable Current Sink and Source

Pin Configuration & Typical Application Circuit

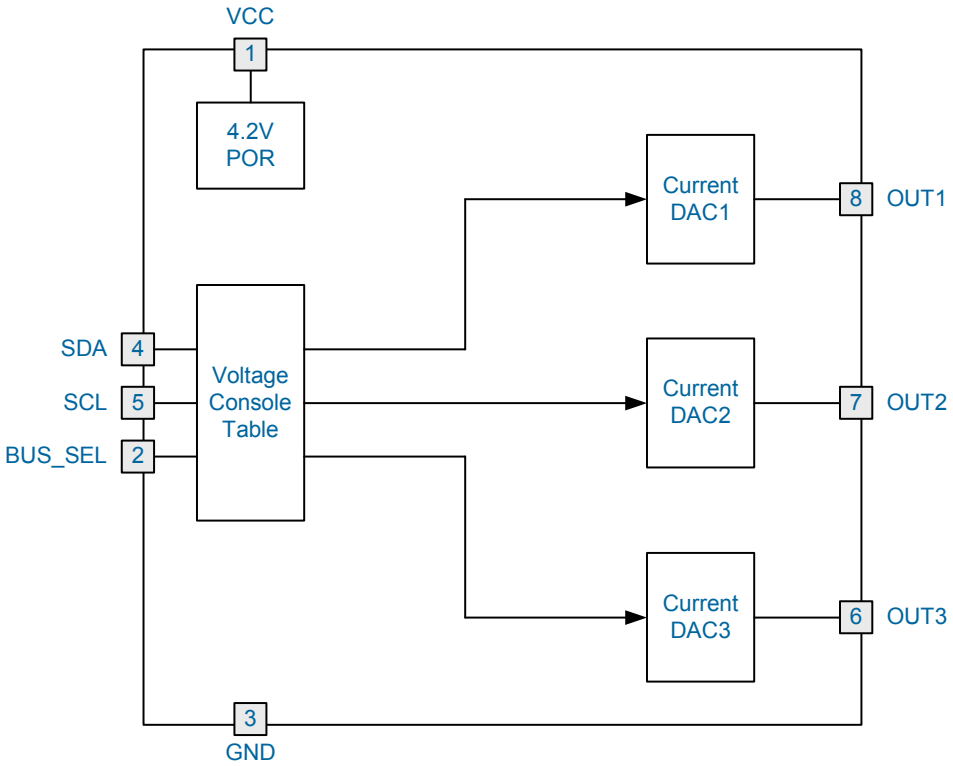




Functional Pin Description

Pin No.	Name	Pin Function
1	VCC	**Supply Voltage Input**. This pin is power input of uP6261. This pin is continuously monitored for POR. The POR threshold level is 4.2V with 0.4V hysteresis. Connected this pin to 5VSB with a ceramic decoupling capacitor directly to GND pin.
2	BUS_SEL	**Bus Address Selection.** Connect a voltage divider to program the bus address of the uP6262.
3	GND	**Ground.**
4	SDA	**Serial Data Input.** This pin is input or output of serial bus data signal.
5	SCL	**Serial Clock Input.** This pin receives serial bus clock signal.
6	OUT3	**Current Output 3.**
7	OUT2	**Current Output 2.**
8	OUT1	**Current Output 1.**

Functional Block Diagram



Functional Description

The uP6262 is a high precision voltage console consisting of three sets I2C programmable current DACs. Each current DAC is capable of sinking 64-step and sourcing 16-step output current that are programmed by the I2C interface. The sinking and sourcing current of OUT1 and OUT2 are programmable for 20x boost respectively.

The uP6262 features soft-jump, easily interfacing with standard DC/DC converter for voltage console. The uP6262 is available in space-saving SOT23-8 package.

Power On Reset

The uP6262 continuously monitors supply voltage at VCC pin for power on reset circuit POR. The POR threshold at V_{CC} rising is typically 4.2V. All three reference voltage outputs are disabled if the supply voltage is lower than the POR threshold level.

I2C Address Programming

The uP6262 features user programmable address by a voltage divider from VCC-to-BUS_SEL-to-GND as shown in the *Typical Application Circuit*. BUS_SEL pin voltage is compared with internal reference voltage for address programming. There are total 6 addresses available. Table 1 illustrates recommended external voltage divider for address programming.

Table 1. Recommended Address Programming

Address	0x6A	0x68	0x66	0x64	0x62	0x60
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.3	3	3.9	open
BUS_SEL Voltage (% of VCC)	0	25	40	60	75	100

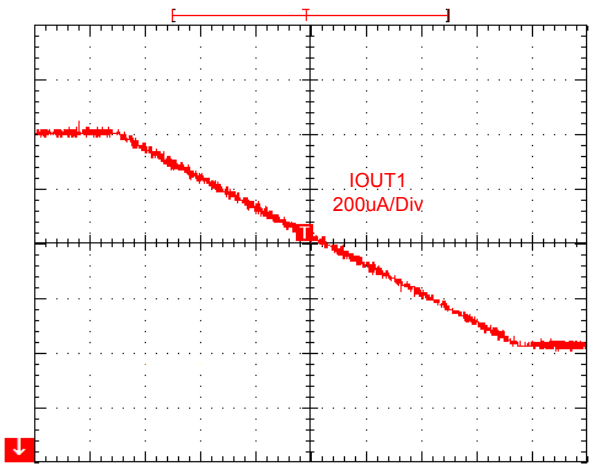
I2C Programming Interface

The uP6262 integrates 3-channel current DAC OUT1, OUT2 and OUT3 that are programmed by Reg0x01, Reg0x02 and Reg0x03 respectively. Each output can sink 64-step current (0~630uA) and source 16 step current (0~800uA) as shown in Table 2. When bit 7 of Reg0x01 or Reg0x02 is set to 1, the corresponding output current is boost to 20 times.

When the undefined value for Reg0x01~03 is selected, the output current will keep the last value.

Soft Jump

The uP6262 features soft jump function that changes output current gradually to its final value. Each step takes about 30us. This makes the output voltage of companied DC/DC converter smooth transition to it final value, resulting in minimum inrush current form it supply input and avoiding false trigger of overcurrent protection. Figure 1 shows the output current transition of soft jump.



Time: 250uA/Div

Figure 1. Output Current Transition

Bit 7 Transition

The uP6262 current DAC does not support bit 7 direct transition (from 0 to 1 or 1 to 0). This will disable the soft-jump function and causes inrush current at companied DC/DC converter. If bit 7 transition is required, the DAC output must be turned off first. For example, Reg0x01 from 0x8F to 0x0F transition must be executed as Reg0x01 = 0x80; Reg0x01 = 00; Reg0x01 = 0x0F in sequence.

0x04 Watching Timer Delay; Default 0x00

Bit 7: Enable Watching Dog Timer

1: Start watching dog counter and reset all registers to default after time-out.

0: Stop watching dog counter and reset watching dog timer.

Bit 6: Watching Dog Timer Status; Read Only

This bit is set 1 when watching dog time-out happens.

This bit is clear to 0 once this register is read out.

Bits 5~4: Watching Dog Timer. Accuracy 50%

11: 11000ms

10: 5500ms

01: 2800ms

00: 1400ms

Bit 3~0: Version Identification.

Functional Description

Table 2. Current DAC Table with Bit7 = 0

Step	Bits 7~0	OUT1 (uA)	OUT2 (uA)	OUT3 (uA)
0	0000,0000	0	0	0
1	0000,0001	-10	-10	-10
2	0000,0010	-20	-20	-20
3	0000,0011	-30	-30	-30
4	0000,0100	-40	-40	-40
5	0000,0101	-50	-50	-50
6	0000,0110	-60	-60	-60
7	0000,0111	-70	-70	-70
8	0000,1000	-80	-80	-80
9	0000,1001	-90	-90	-90
10	0000,1010	-100	-100	-100
11	0000,1011	-110	-110	-110
12	0000,1100	-120	-120	-120
13	0000,1101	-130	-130	-130
14	0000,1110	-140	-140	-140
15	0000,1111	-150	-150	-150
16	0001,0000	-160	-160	-160
17	0001,0001	-170	-170	-170
18	0001,0010	-180	-180	-180
19	0001,0011	-190	-190	-190
20	0001,0100	-200	-200	-200
21	0001,0101	-210	-210	-210
22	0001,0110	-220	-220	-220
23	0001,0111	-230	-230	-230
24	0001,1000	-240	-240	-240
25	0001,1001	-250	-250	-250
26	0001,1010	-260	-260	-260
27	0001,1011	-270	-270	-270
28	0001,1100	-280	-280	-280
29	0001,1101	-290	-290	-290
30	0001,1110	-300	-300	-300
31	0001,1111	-310	-310	-310

Table 2 (Cont). Current DAC Table with Bit7 = 0

Step	Bits 7~0	OUT1 (uA)	OUT2 (uA)	OUT3 (uA)
32	0010,0000	-320	-320	-320
33	0010,0001	-330	-330	-330
34	0010,0010	-340	-340	-340
35	0010,0011	-350	-350	-350
36	0010,0100	-360	-360	-360
37	0010,0101	-370	-370	-370
38	0010,0110	-380	-380	-380
39	0010,0111	-390	-390	-390
40	0010,1000	-400	-400	-400
41	0010,1001	-410	-410	-410
42	0010,1010	-420	-420	-420
43	0010,1011	-430	-430	-430
44	0010,1100	-440	-440	-440
45	0010,1101	-450	-450	-450
46	0010,1110	-460	-460	-460
47	0010,1111	-470	-470	-470
48	0011,0000	-480	-480	-480
49	0011,0001	-490	-490	-490
50	0011,0010	-500	-500	-500
51	0011,0011	-510	-510	-510
52	0011,0100	-520	-520	-520
53	0011,0101	-530	-530	-530
54	0011,0110	-540	-540	-540
55	0011,0111	-550	-550	-550
56	0011,1000	-560	-560	-560
57	0011,1001	-570	-570	-570
58	0011,1010	-580	-580	-580
59	0011,1011	-590	-590	-590
60	0011,1100	-600	-600	-600
61	0011,1101	-610	-610	-610
62	0011,1110	-620	-620	-620
63	0011,1111	-630	-630	-630

Table 2 (Cont). Current DAC Table with Bit7 = 0

Step	Bits 7~0	OUT1 (uA)	OUT2 (uA)	OUT3 (uA)
64	0100,0000	0	0	0
65	0100,0001	50	50	50
66	0100,0010	100	100	100
67	0100,0011	150	150	150
68	0100,0100	200	200	200
69	0100,0101	250	250	250
70	0100,0110	300	300	300
71	0100,0111	350	350	350
72	0100,1000	400	400	400
73	0100,1001	450	450	450
74	0100,1010	500	500	500
75	0100,1011	550	550	550
76	0100,1100	600	600	600
77	0100,1101	650	650	650
78	0100,1110	700	700	700
79	0100,1111	750	750	750
80	0101,0000	800	800	800
81 ~ 127	01##,####	Reserved	Reserved	Reserved

Table 3. Current DAC Table with Bit7 = 1

Step	Bits 7~0	OUT1 (uA)	OUT2 (uA)	OUT3 (uA)
0	1000,0000	0	0	Reserved
1	1000,0001	-200	-200	
2	1000,0010	-400	-400	
3	1000,0011	-600	-600	
4	1000,0100	-800	-800	
5	1000,0101	-1000	-1000	
6	1000,0110	-1200	-1200	
7	1000,0111	-1400	-1400	
8	1000,1000	-1600	-1600	
9	1000,1001	-1800	-1800	
10	1000,1010	-2000	-2000	
11	1000,1011	-2200	-2200	
12	1000,1100	-2400	-2400	
13	1000,1101	-2600	-2600	
14	1000,1110	-2800	-2800	
15	1000,1111	-3000	-3000	
16	1001,0000	-3200	-3200	
17	1001,0001	-3400	-3400	
18	1001,0010	-3600	-3600	
19	1001,0011	-3800	-3800	
20	1001,0100	-4000	-4000	
21	1001,0101	-4200	-4200	
22	1001,0110	-4400	-4400	
23	1001,0111	-4600	-4600	
24	1001,1000	-4800	-4800	
25	1001,1001	-5000	-5000	
26	1001,1010	-5200	-5200	
27	1001,1011	-5400	-5400	
28	1001,1100	-5600	-5600	
29	1001,1101	-5800	-5800	
30	1001,1110	-6000	-6000	
31	1001,1111	-6200	-6200	

Table 3 (Cont). Current DAC Table with Bit7 = 1

Step	Bits 7~0	OUT1 (uA)	OUT2 (uA)	OUT3 (uA)
32	1010,0000	-6400	-6400	Reserved
33	1010,0001	-6600	-6600	
34	1010,0010	-6800	-6800	
35	1010,0011	-7000	-7000	
36	1010,0100	-7200	-7200	
37	1010,0101	-7400	-7400	
38	1010,0110	-7600	-7600	
39	1010,0111	-7800	-7800	
40	1010,1000	-8000	-8000	
41	1010,1001	-8200	-8200	
42	1010,1010	-8400	-8400	
43	1010,1011	-8600	-8600	
44	1010,1100	-8800	-8800	
45	1010,1101	-9000	-9000	
46	1010,1110	-9200	-9200	
47	1010,1111	-9400	-9400	
48	1011,0000	-9600	-9600	
49	1011,0001	-9800	-9800	
50	1011,0010	-10000	-10000	
51	1011,0011	-10200	-10200	
52	1011,0100	-10400	-10400	
53	1011,0101	-10600	-10600	
54	1011,0110	-10800	-10800	
55	1011,0111	-11000	-11000	
56	1011,1000	-11200	-11200	
57	1011,1001	-11400	-11400	
58	1011,1010	-11600	-11600	
59	1011,1011	-11800	-11800	
60	1011,1100	-12000	-12000	
61	1011,1101	-12200	-12200	
62	1011,1110	-12400	-12400	
63	1011,1111	-12600	-12600	

Table 3 (Cont). Current DAC Table with Bit7 = 1

Step	Bits 7~0	OUT1 (uA)	OUT2 (uA)	OUT3 (uA)
64	1100,0000	0	0	Reserved
65	1100,0001	400	400	
66	1100,0010	800	800	
67	1100,0011	1200	1200	
68	1100,0100	1600	1600	
69	1100,0101	2000	2000	
70	1100,0110	2400	2400	
71	1100,0111	2800	2800	
72	1100,1000	3200	3200	
73	1100,1001	3600	3600	
74	1100,1010	4000	4000	
75	1100,1011	4400	4400	
76	1100,1100	4800	4800	
77	1100,1101	5200	5200	
78	1100,1110	5600	5600	
79	1100,1111	6000	6000	
80	1101,0000	6400	6400	
81 ~ 127	11##,####	Reserved	Reserved	Reserved

Absolute Maximum Rating

Supply Input Voltage V_{CC} (Note 1) ---------- -0.3V to +6V
Other Pins ---------- -0.3V to (V_{CC} +0.3V)
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
SOT23-8 θ_{JA} ---------- 250°C/W
Power Dissipation, P_D @ T_A = 25°C
SOT23-8 ---------- 0.25W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- +4.5V to +5.5V

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input Voltage						
Supply Input Voltage	V_{CC}		4.5	--	5.5	V
POR Threshold	V_{CC_RTH}		4.0	4.2	4.5	V
POR Hysteresis	V_{CC_HYS}		--	0.4	--	V
Supply Input Current	I_{CC}	I_{OUT1} = I_{OUT2} = I_{OUT3} = 0uA	0.5	--	1.5	mA
Current DAC Output						
Output Offset Current	I_{OUT_OFST}	I_{OUT} programmed as 0uA, V_{OUT} = 0V ~ 5.5V.	-1	--	1	uA
Output Current Accuracy		I_{OUT} programmed as 100uA ~ 12800uA, V_{OUT} = 0.8V	-6	--	6	%
		I_{OUT} programmed as 0uA ~ 100uA, V_{OUT} = 0.8V	-6	--	6	uA
Output Current Line Regulation		I_{OUT} sinking, V_{OUT} = 0.5V ~ V_{CC}	-1	--	1	%/V
		I_{OUT} sourcing, V_{OUT} = 0V ~ V_{CC} - 1V	-1	--	1	%/V
Soft Jump Speed		Time interval per current step	--	30	--	us
Output Current Differential Linearity			--	--	0.5	LSB
Output Current Integral Linearity			--	--	1	LSB

Electrical Characteristics

Prameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Address Selection						
Adress 1 Voltage Range		Address = 0x6A	--	--	15	$\%V_{CC}$
Adress 2 Voltage Range		Address = 0x68	20	25	30	$\%V_{CC}$
Adress 3 Voltage Range		Address = 0x66	37	42	47	$\%V_{CC}$
Adress 4 Voltage Range		Address = 0x64	53	58	62	$\%V_{CC}$
Adress 5 Voltage Range		Address = 0x62	70	75	80	$\%V_{CC}$
Adress 6 Voltage Range		Address = 0x60	85	--	--	$\%V_{CC}$

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

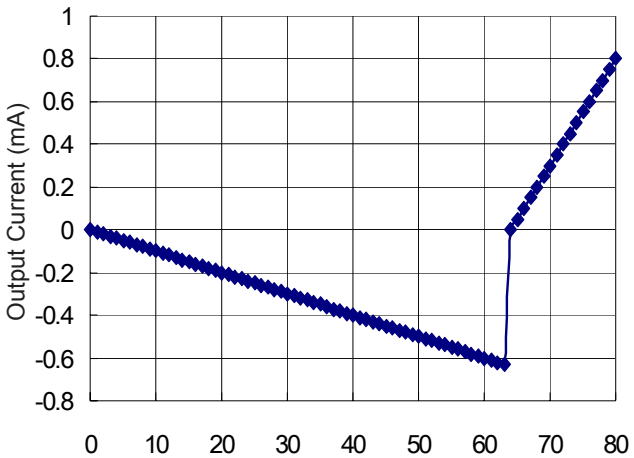
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Differential linearity is defined as the difference between the expected incremental current increase with respect to position and the actual increase.

Note 6. Integral linearity is defined as the difference between the expected value as a function of the setting and the actual value. The expected value is a straight line between the zero and the full-scale values proportional to the setting.

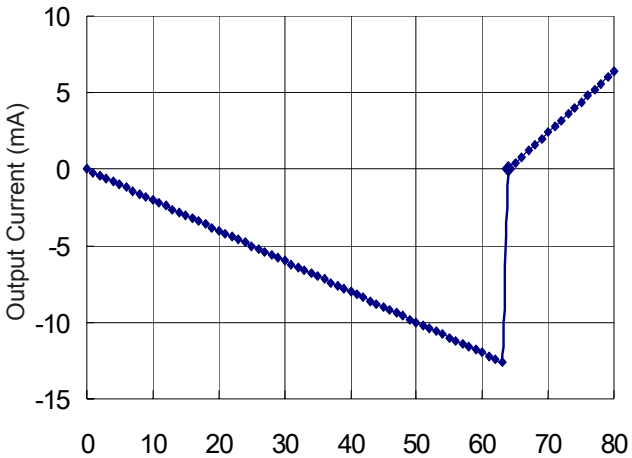
Typical Operation Characteristics

Output Current with Bit 7 = 0



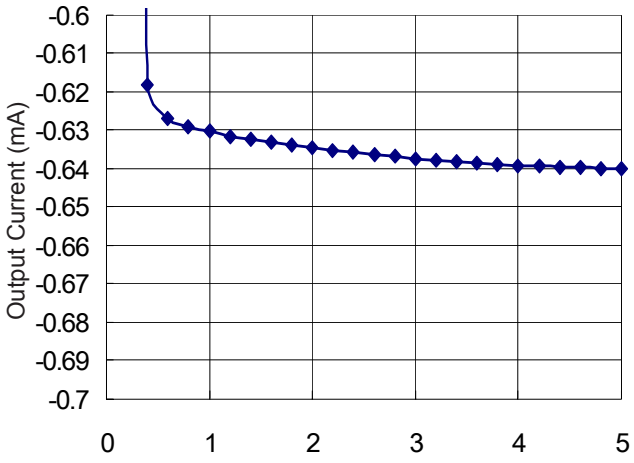
Output Voltage = 0.8V

Output Current with Bit 7 = 1



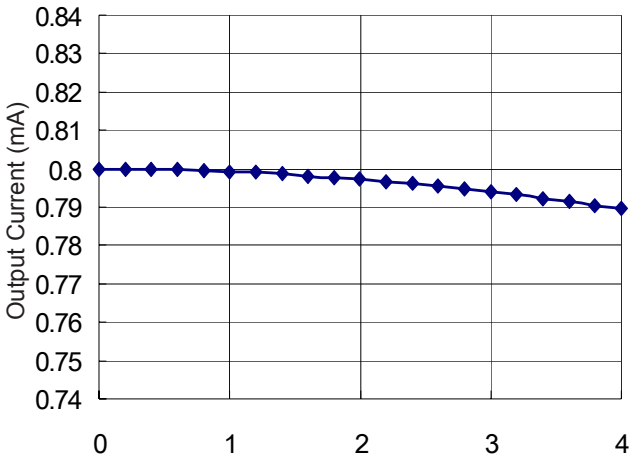
Output Voltage = 0.8V

Output Current vs. Output Voltage



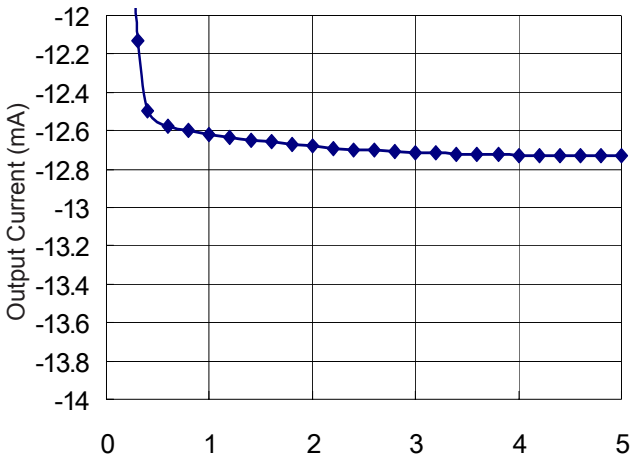
Reg0x01 ~ 0x03 = 0x3F (630uA Sinking)

Output Current vs. Output Voltage



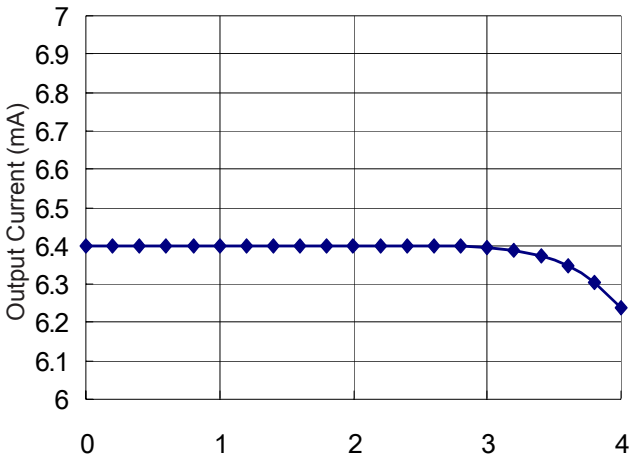
Reg0x01 ~ 0x03 = 0x50 (800uA Sourcing)

Output Current vs. Output Voltage



Reg0x01 ~ 0x02 = 0xBF (12600uA Sinking)

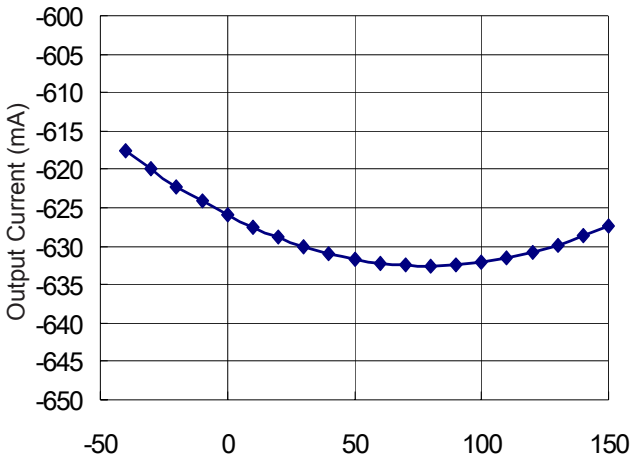
Output Current vs. Output Voltage



Reg0x01 ~ 0x02 = 0xD0 (6400uA Sourcing)

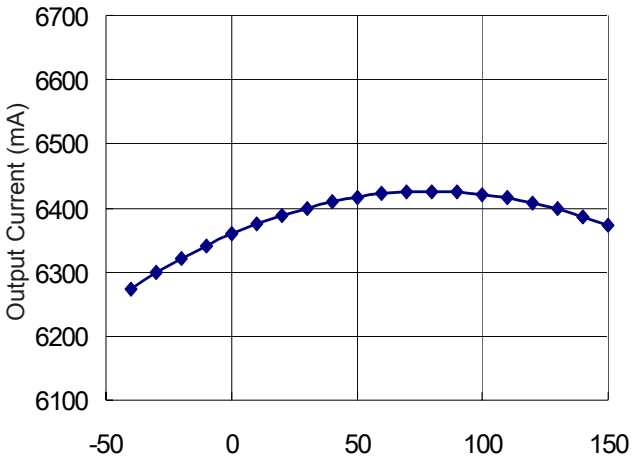
Typical Operation Characteristics

Output Current vs. Temperature



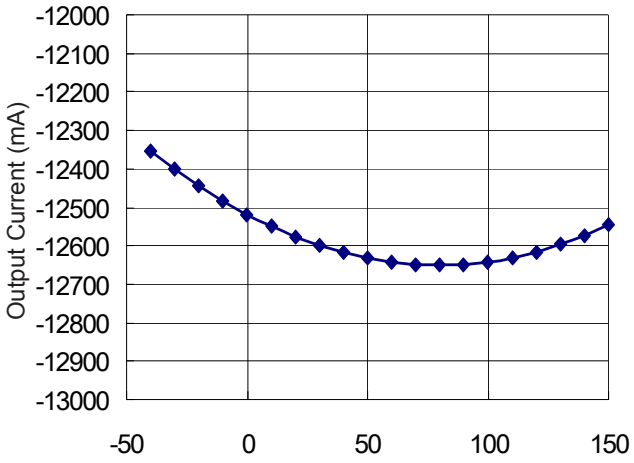
Reg0x01 ~ 0x03 = 0x3F (630uA Sinking)

Output Current vs. Temperature



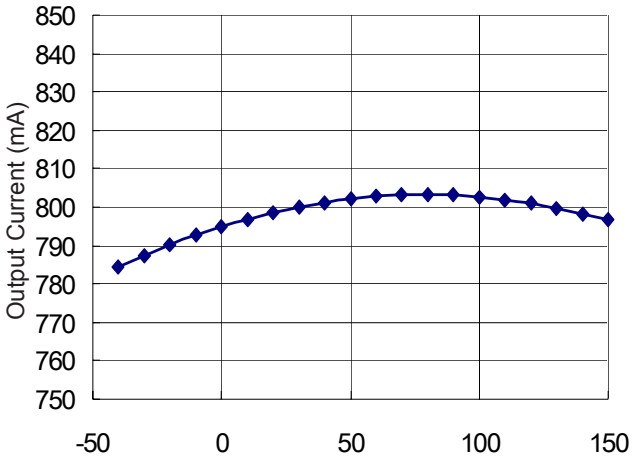
Reg0x01 ~ 0x03 = 0x50 (800uA Sourcing)

Output Current vs. Temperature



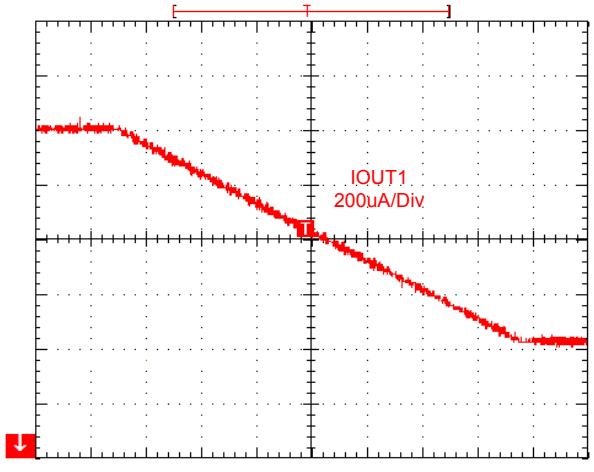
Reg0x01 ~ 0x02 = 0xBF (12600uA Sinking)

Output Current vs. Temperature



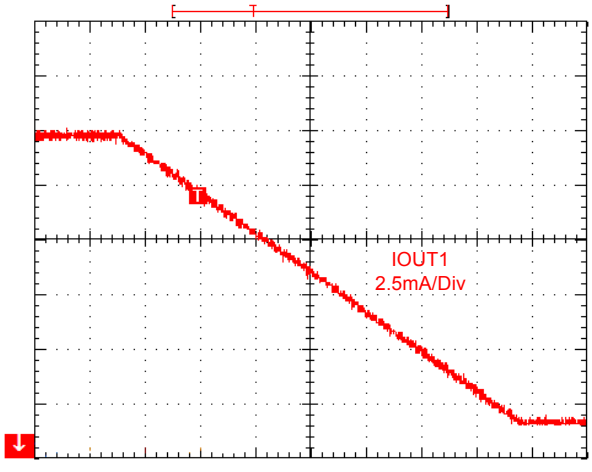
Reg0x01 ~ 0x02 = 0xD0 (6400uA Sourcing)

Output Current Transition



Time (250us/Div)
Reg0x01 = 0x00 to 0x3F

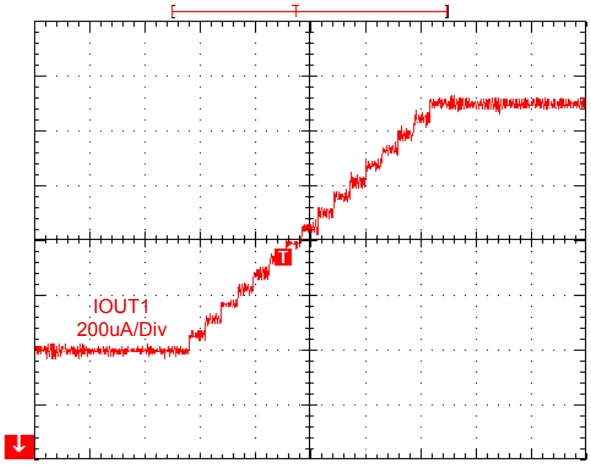
Output Current Transition



Time (250us/Div)
Reg0x01 = 0x80 To 0xBF

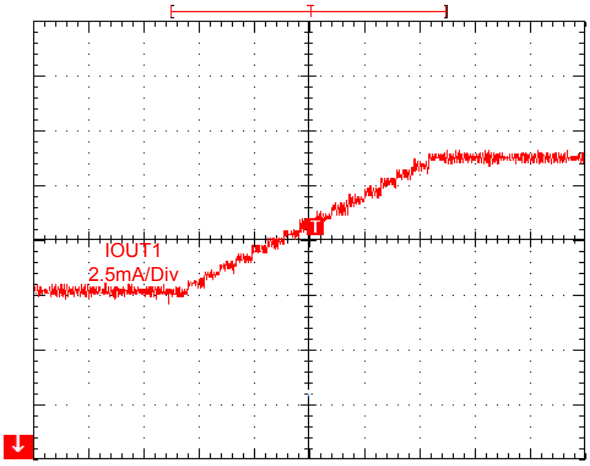
Typical Operation Characteristics

Output Current Transition



Time (100us/Div)
Reg0x01 = 0x40 to 0x50

Output Current Transition



Time (100us/Div)
Reg0x01 = 0xC0 To 0xD0

Application Information

The uP6262 is a high precision voltage console consisting of three sets I2C programmable current DACs. Each current DAC is capable of sinking 64-step and sourcing 16-step output current that are programmed by the I2C interface. The sinking and sourcing current of OUT1 and OUT2 are programmable for 20x boost respectively.

The uP6262 features soft-jump, easily interfacing with standard DC/DC converter for voltage console. The uP6262 is available in space-saving SOT23-8 package.

Output Voltage Programming of DC/DC Converter

Figure 1 shows a typical interface between uP6262 and a general-purposed DC/DC converter. It is convenient to program the output voltage V_{OUT} by selecting appropriate output current I_{OUT} of uP6262.

The output voltage difference when I_{OUT} is applied is calculated as:

$$\Delta V_{OUT} = V_{OUT} - V_{OUT\_NORM} = -I_{OUT} \times R1$$

For example, if I_{OUT} = -630uA (sinking) is selected and R1 =1kΩ, the output voltage will increase by amount as:

$$\Delta V_{OUT} = 630uA \times 1k\Omega = 0.63V$$

It is noted the above calculation is independent of R2. Users can select R2 according to required nominal output voltage.

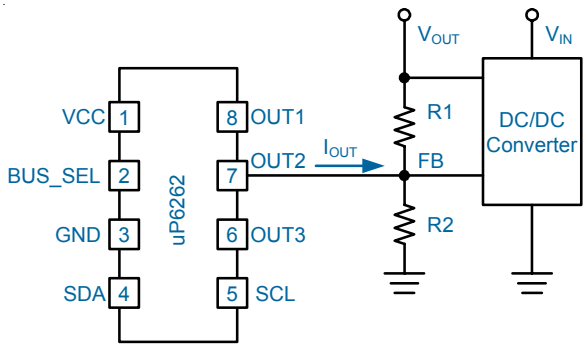


Figure 1. Interfacing the uP6262 and DC/DC Converter

Extra Current for Charging/Discharging Output Capacitor

Extra current besides normal loading is required to charge/discharge the output capacitors to its new level when the output voltage is making transition due to I_{OUT} change of uP6262. For example, I_{OUT} changes from 0uA to -630uA in 63 steps and ΔV_{OUT} changes from 0V to 0.63V accordingly. It takes about 1890us for I_{OUT} to change from 0uA to -630uA. The extra current to charge the output capacitor C_{OUT} = 2000uF is calculated as:

$$I_{EXTRA} = \frac{C_{OUT} \times \Delta V_{OUT}}{\Delta T} = \frac{2000uF \times 0.63V}{1890us} = 0.67A$$

Make sure the DC/DC converter can afford the extra current without false triggering any protection functions.

Layout Consideration

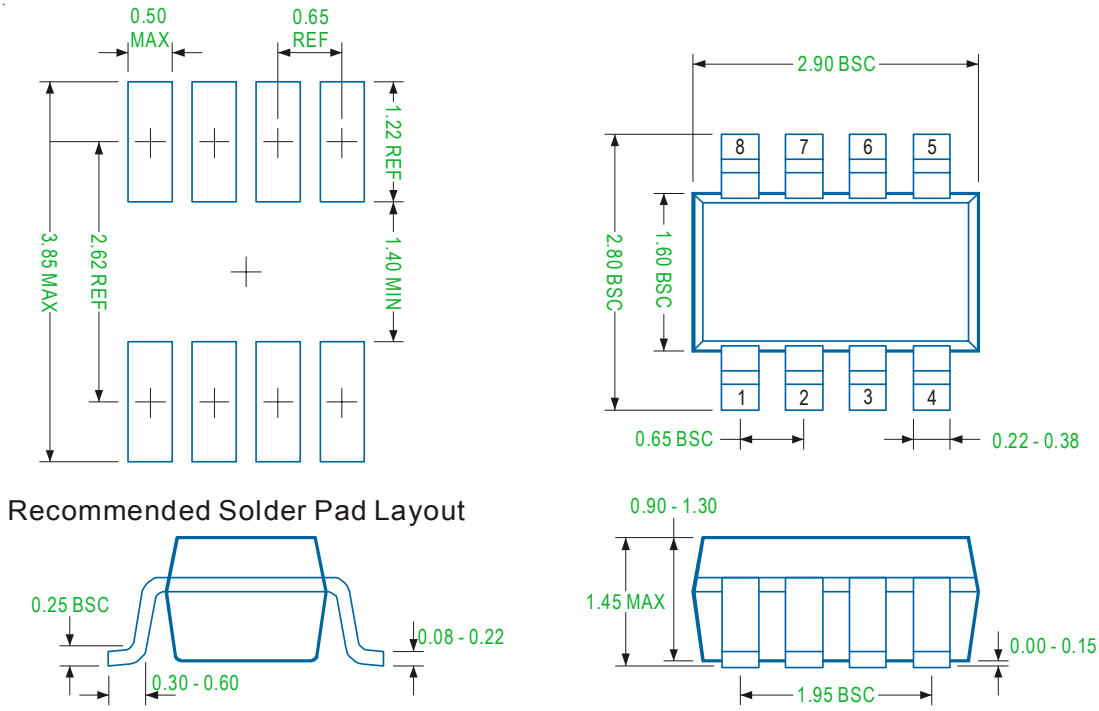
PCB layout is an important part of design for uP6262. The FB pin of the DC/DC converter is a noise sensitive pin. Great care should be taken when placing the parts and routing the FB trace.

Place the uP6262 physically near the FB pin of the DC/DC converter. Keep the FB traces short and away from noisy nodes to avoid noise pick-up.

Check Transient Response and Stability

Even though the output impedance of uP6262 is quite high over a wide frequency range, the insertion of uP6262 does affect voltage control loop design of the DC/DC converter. It is highly recommended to check the transient response and stability of the converter when uP6262 is applied.

Package Information



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.