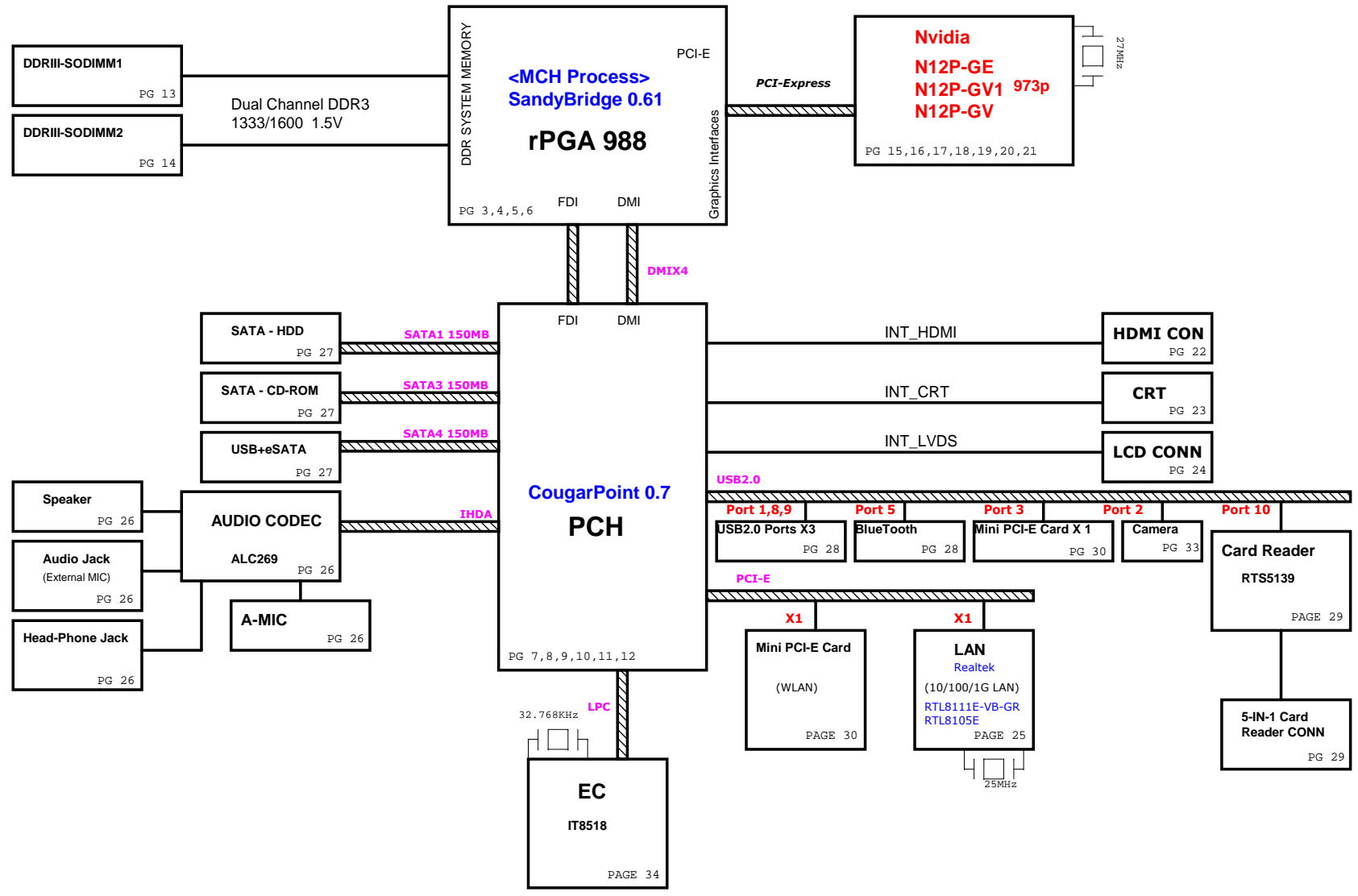


FAN / THERMAL  
EMC2103-2



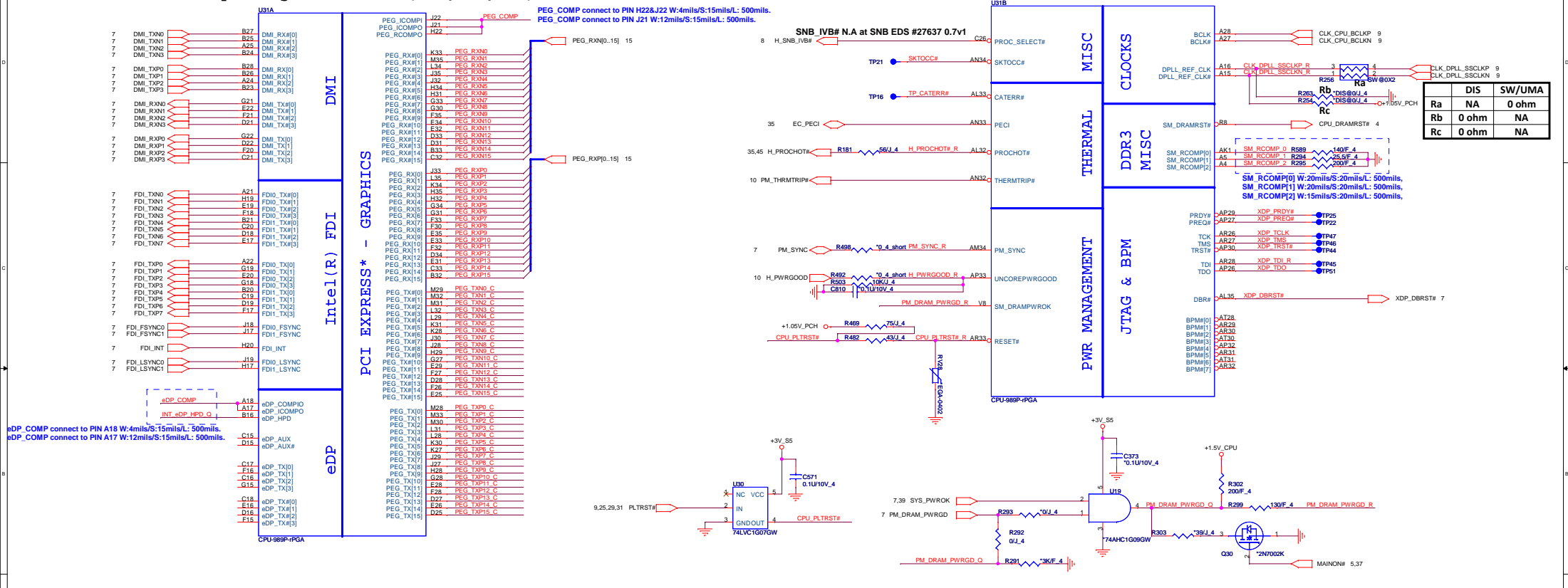
- REGULATOR (DDR3)**  
1.5VSUS, 0.75VSMDDR\_VTERM, 1.5V  
1.5V\_GPU, 1.5V\_CPU
- REGULATOR**  
+1.05V\_VTT, +1.8V
- DC/DC**  
3VPCU, 5VPCU, +15V  
PG 42
- CPU Core**  
PG 43
- VGA Core Discrete**  
PG 44

Table of Contents	
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3	CLOCK GENERATOR
4-7	PineView CPU
8-13	TigerPoint
14	DDRII SO-DIMM
15	LCD Conn
16	CRT Conn.
17	Audio Codec CX20582
18	LAN(RTL8103EL/8111DL)
19	SATA HDD
20	USB x 3
21	CardReader AU6433
22	MINI-Card (WLAN)
23	MINI-Card ( WWAN)
24	BLUETOOTH
25	KB/TP
26	SW/LED/Other
27	FAN & Thermal
28	KBC IT8502E
29	HOLD & SKEW
30	Discharge
31	Charger
32	DDR 1.8V (TPS51116)
33	VCCP (OZ8116LN)
34	3V/5V (ISL6237)
35	VCore (ISL6261A)
36	VCC1.5V/ GFX CORE
37	Power Block Dianram
38	
39	
40	

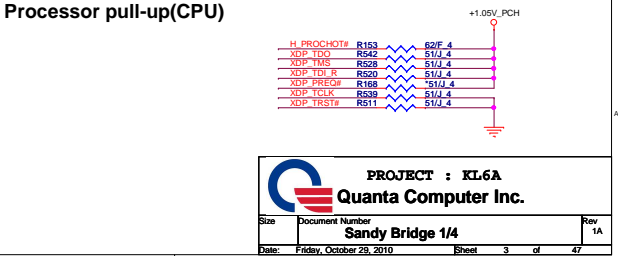
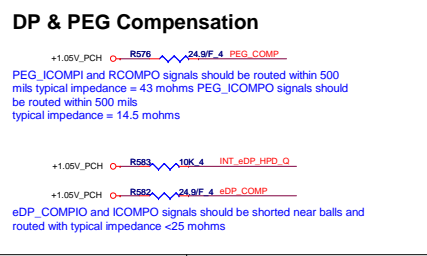
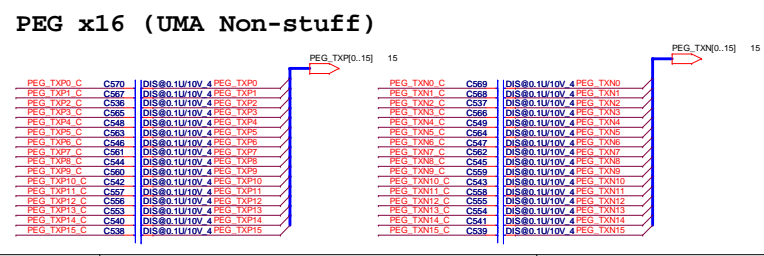
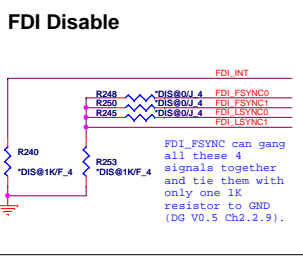
## Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	15,30,31,32,33,34,35	MAIN POWER		S0-S5
+3VRTC	+3.0V~+3.3V	11,12,38	RTC		S0-S5
3VPCU	+3.3V	11,15,18,25,26,28,30,31,34,36	ITE8052 POWER	3V5V_EN	S0-S5
5VPCU	+5V	11,30,31,32,33,34,36	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
+15V	+15V	15,30,32,34	LARGE POWER	3V5V_EN	S0-S5
LANVCC	+3.3V	18,30	LAN POWER	LAN_ON	
5V_S5	+5V	12,20,30	PCH SUS POWER	S5_ON	S0-S3
3V_S5	+3.3V	8,11,12,21,22,30	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WIMAX POWER	S5_ON	S0-S3
5VSUS	+5V	15,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0-S3
3VSUS	+3.3V	26,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0-S3
+VCC_GFX_CORE	+0.9V~+1.2V	6,36	VGA CORE POWER	MAIN_ON	S0
0.9VSMDDR_VTERM	+0.75V	5,14,32	DDR2 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,15,16,17,19,25,27,28,30	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,6,9,10,11,12,14,15,16,17,18,19,21,22,23,24,26,28,30,32,33,34,35	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,21,32	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	6,8,12,17,22,23,36	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V	+1.05V	3,4,6,9,12,30,33	PCH CORE POWER	MAIN_ON	S0
VCC_CORE		6,30,35	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	15	LCD Power	L_VDD_EN	S0
BAT-V	+10V~+17V	31	MAIN BATTERY	CHG_PBATT	S0-S5

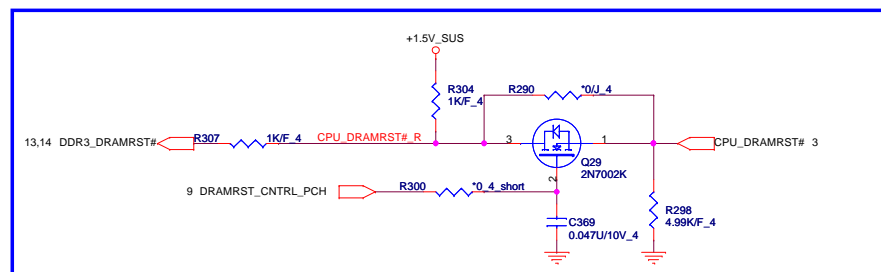
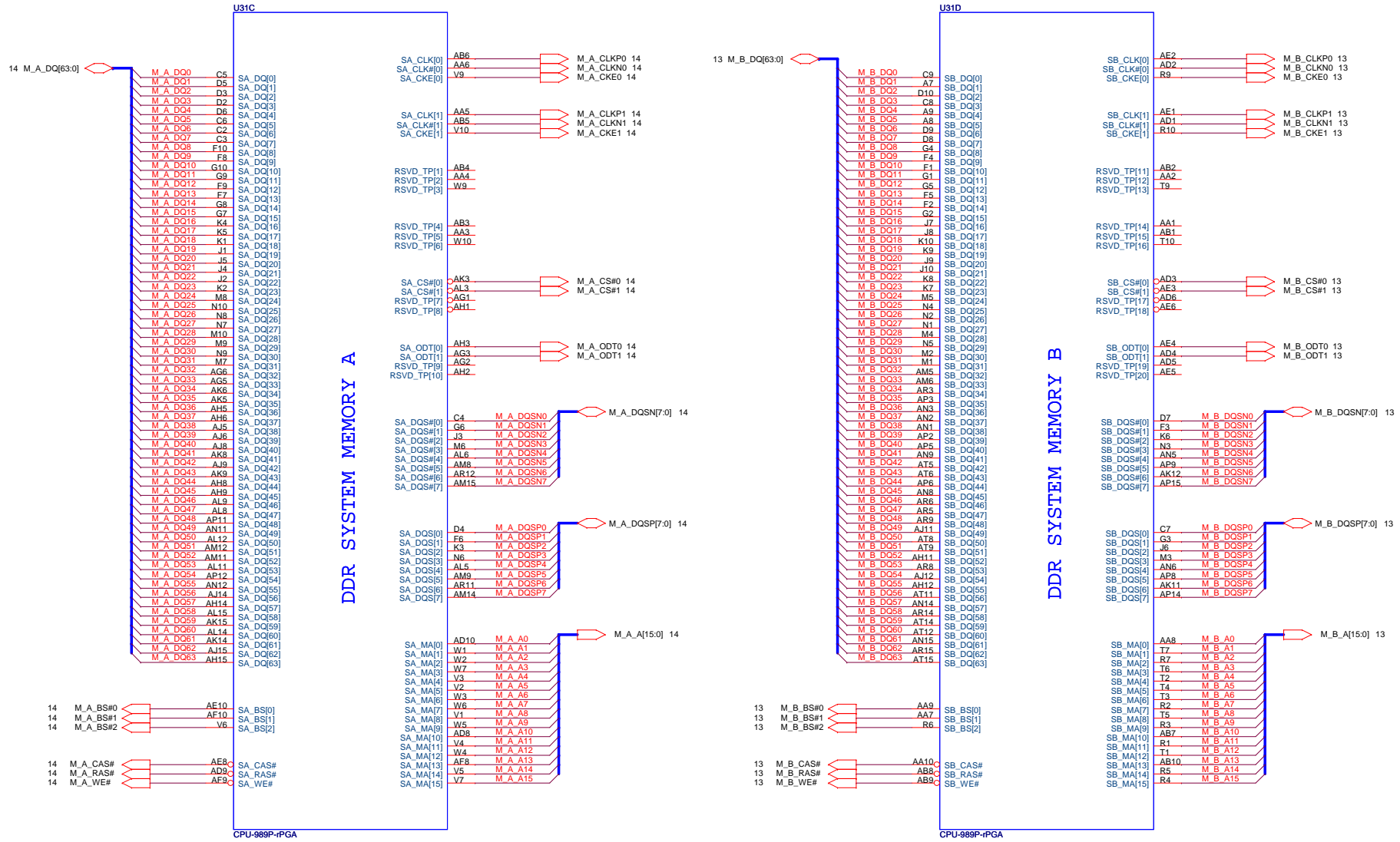
Sandy Bridge Processor (DMI,PEG,FDI)



Ra	DIS	SW/UMA
Rb	0 ohm	NA
Rc	0 ohm	NA



# Sandy Bridge Processor (DDR3)



**PROJECT : KL6A**  
**Quanta Computer Inc.**

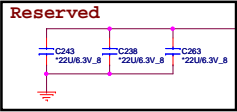
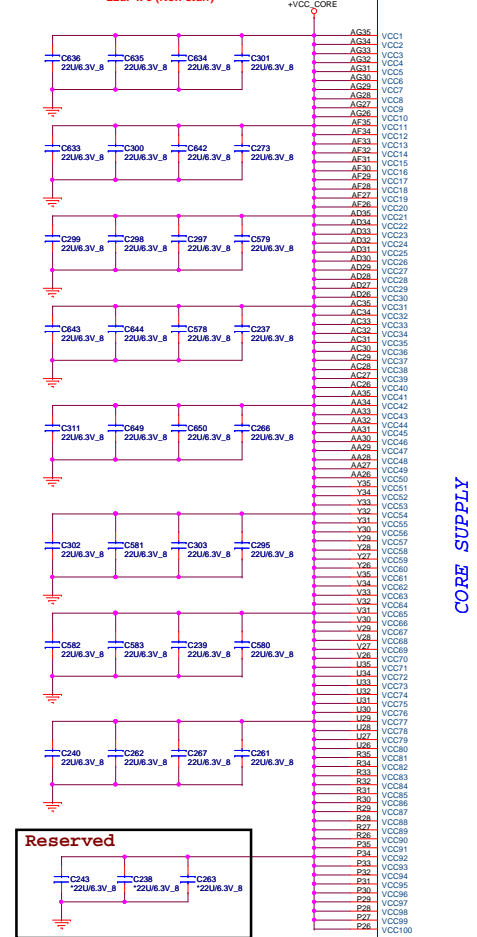
Size	Document Number	Rev
	<b>Sandy Bridge 2/4</b>	1A
Date:	Friday, October 29, 2010	Sheet 4 of 47

Sandy Bridge Processor (POWER)

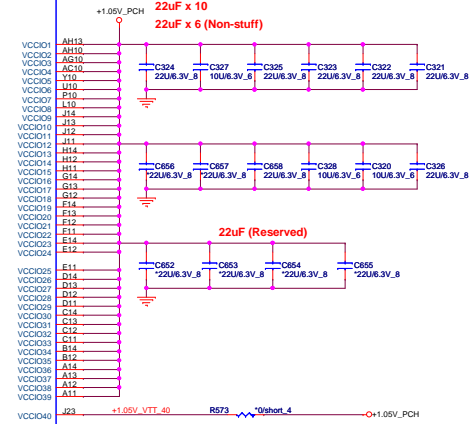
Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power  
SNB 45W:55A  
22uF x 32  
22uF x 3 (Non-stuff)

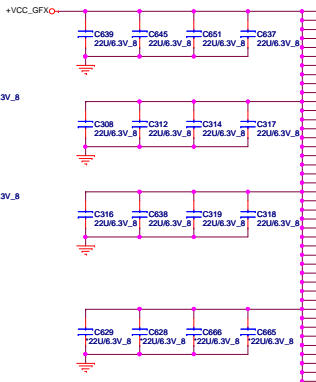
POWER



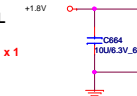
CPU VTT  
SNB 45W:8.5A  
22uF x 10  
22uF x 6 (Non-stuff)



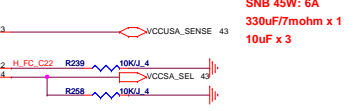
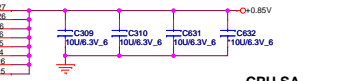
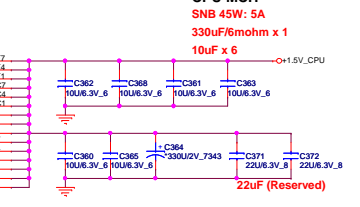
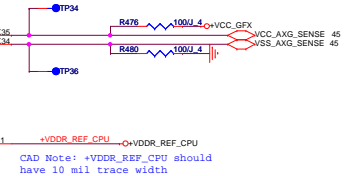
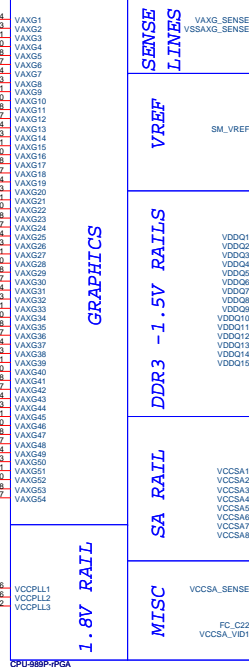
CPU VGT  
SNB 45W:22A  
22uF x 12  
22uF x 4 (Reserved)



CPU VCCPL  
SNB 45W:3A  
330uF/7mohm x 1  
10uF x 1  
1uF x 2

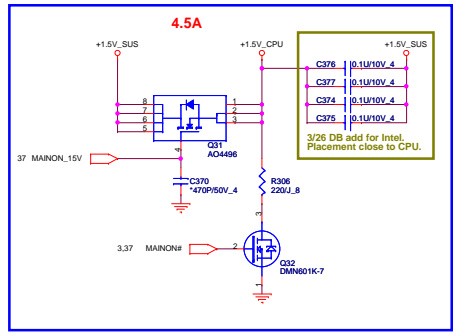
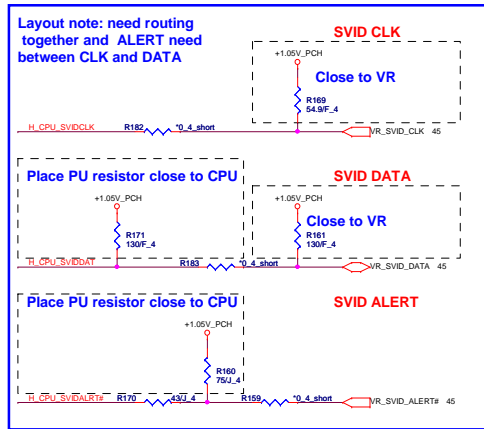
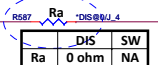


POWER



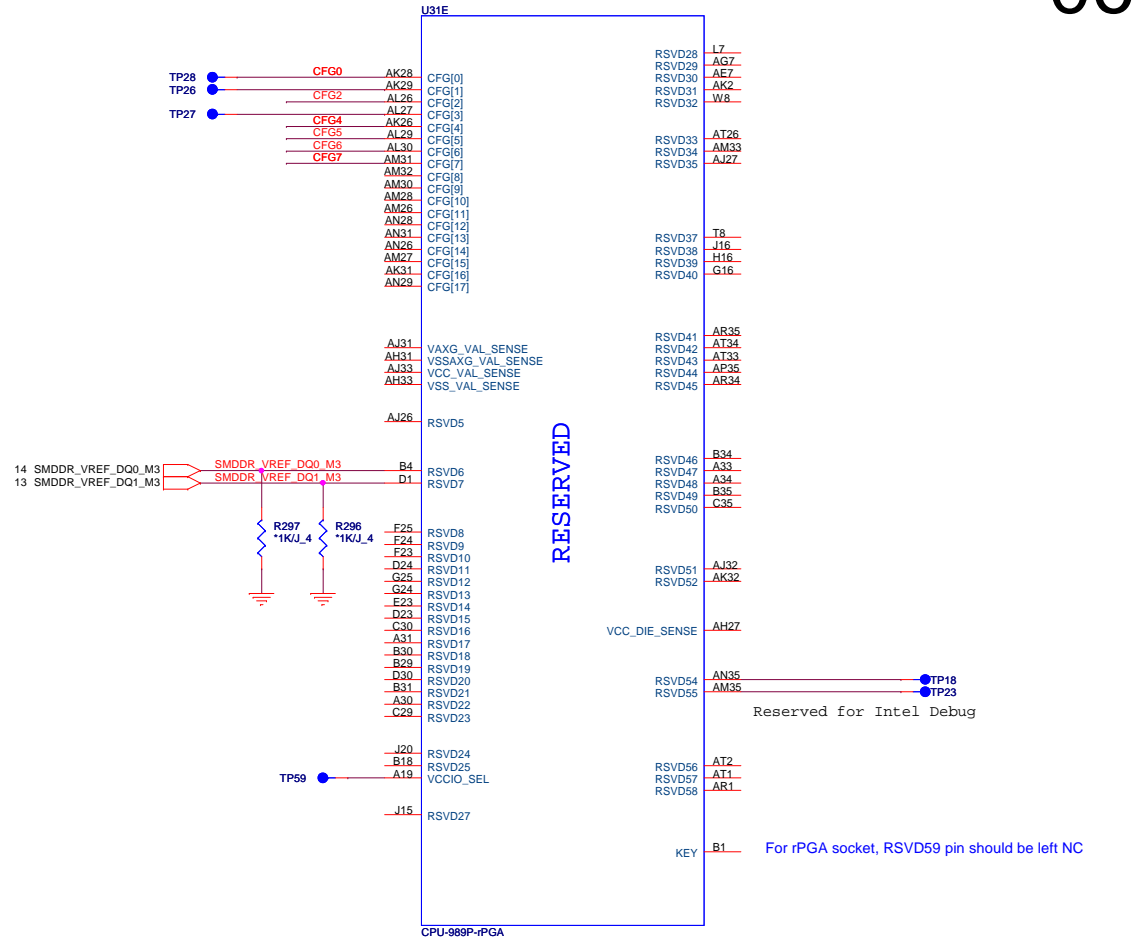
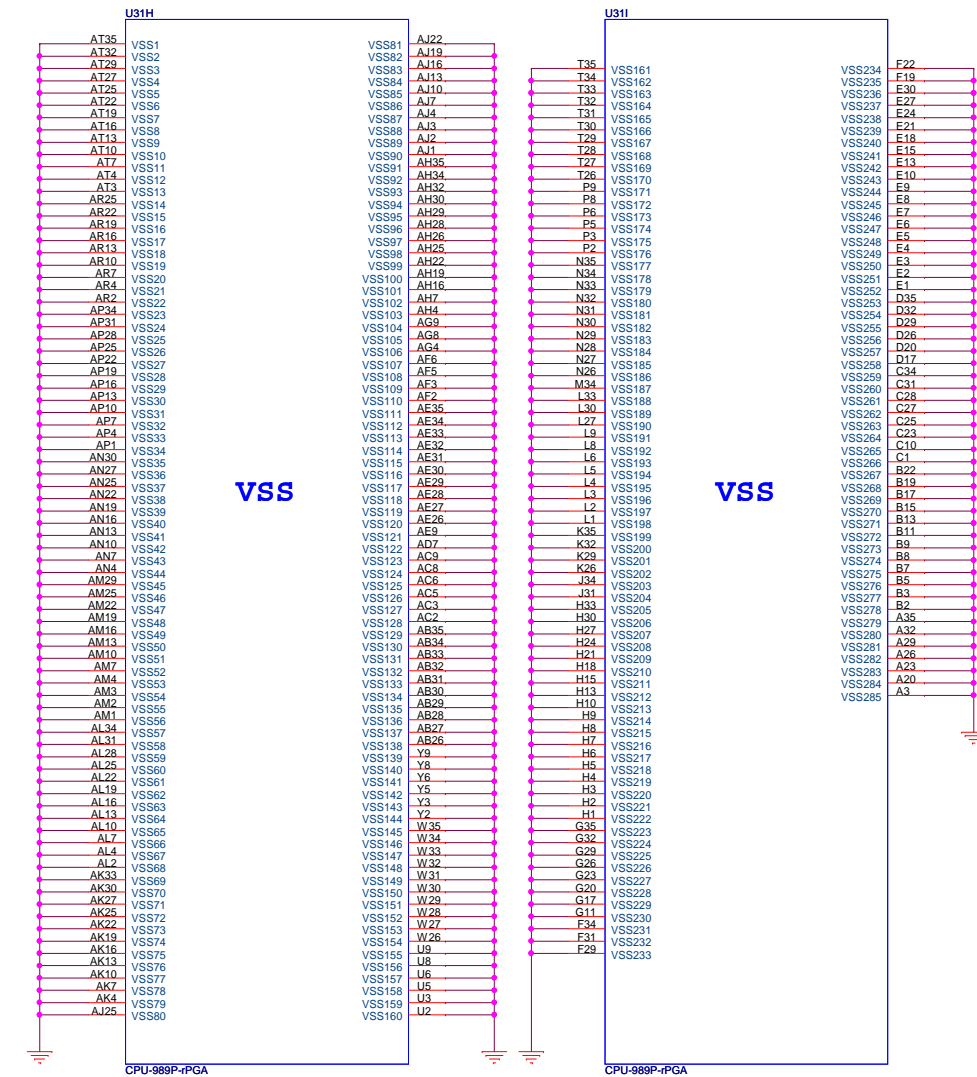
CPU MCH  
SNB 45W: 5A  
330uF/6mohm x 1  
10uF x 6

CPU SA  
SNB 45W: 6A  
330uF/7mohm x 1  
10uF x 3



# Sandy Bridge Processor (GND)

# Sandy Bridge Processor (RESERVED, CFG)



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)  
 11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

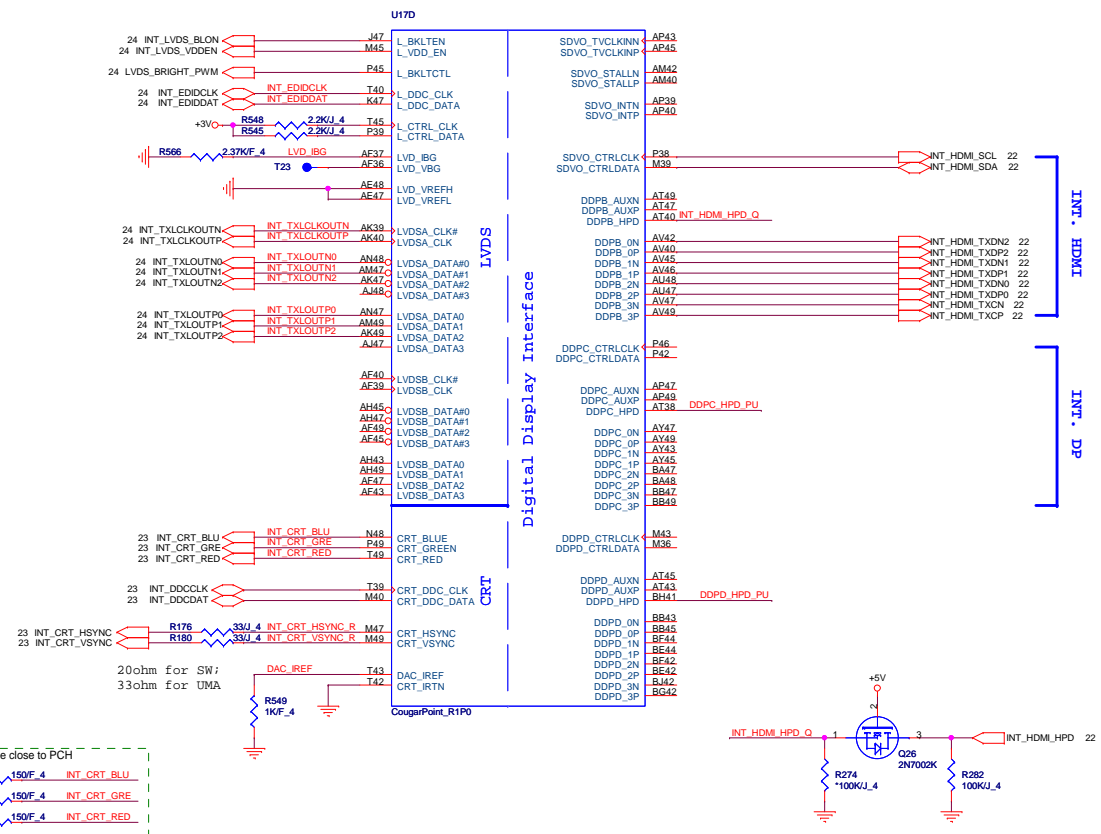
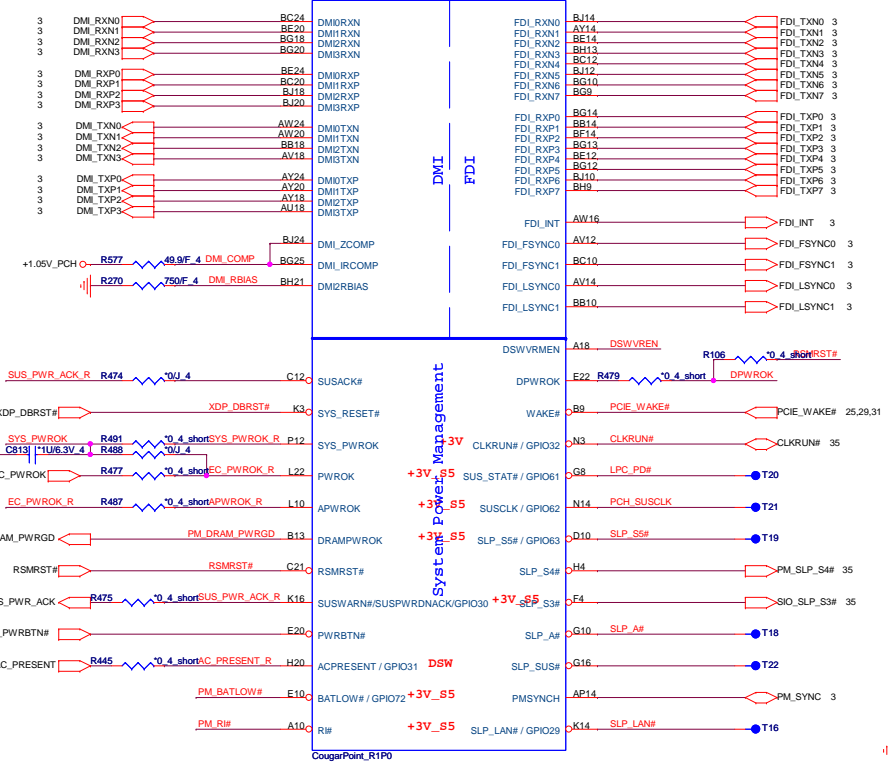
**PROJECT : KL6A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>Sandy Bridge 4/4</b>	1A
Date:	Friday, October 29, 2010	Sheet 6 of 47

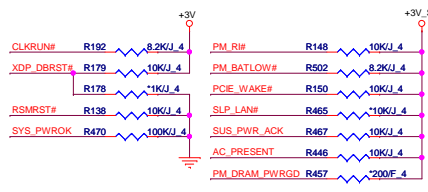
Cougar Point (LVDS,DDI)

Cougar Point (DMI,FDI,PM)

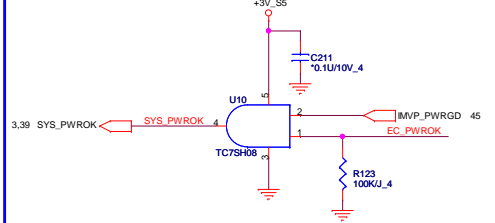
U17C



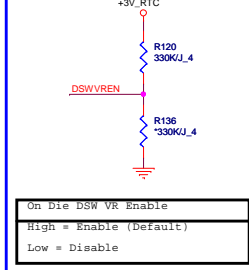
PCH Pull-high/low(CLG)



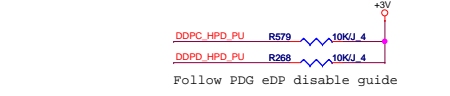
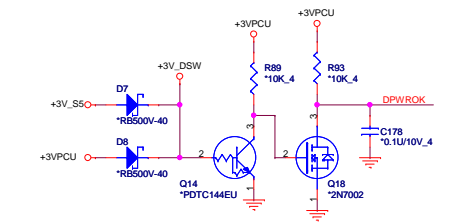
System PWR\_OK(CLG)



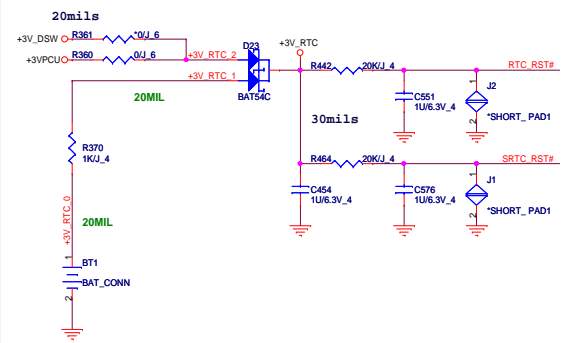
DPWROK FOR DSW



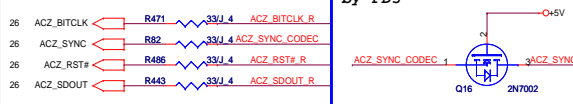
DPWROK FOR DSW



RTC Circuitry(RTC)

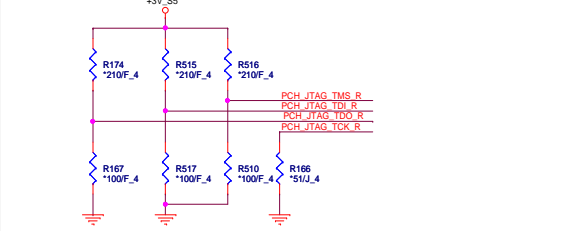


HDA Bus(CLG)

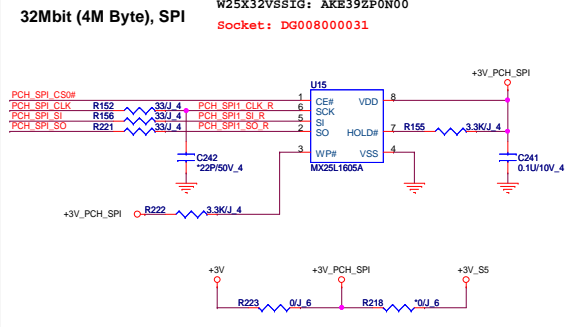


To Separate Codec Sync by PD3

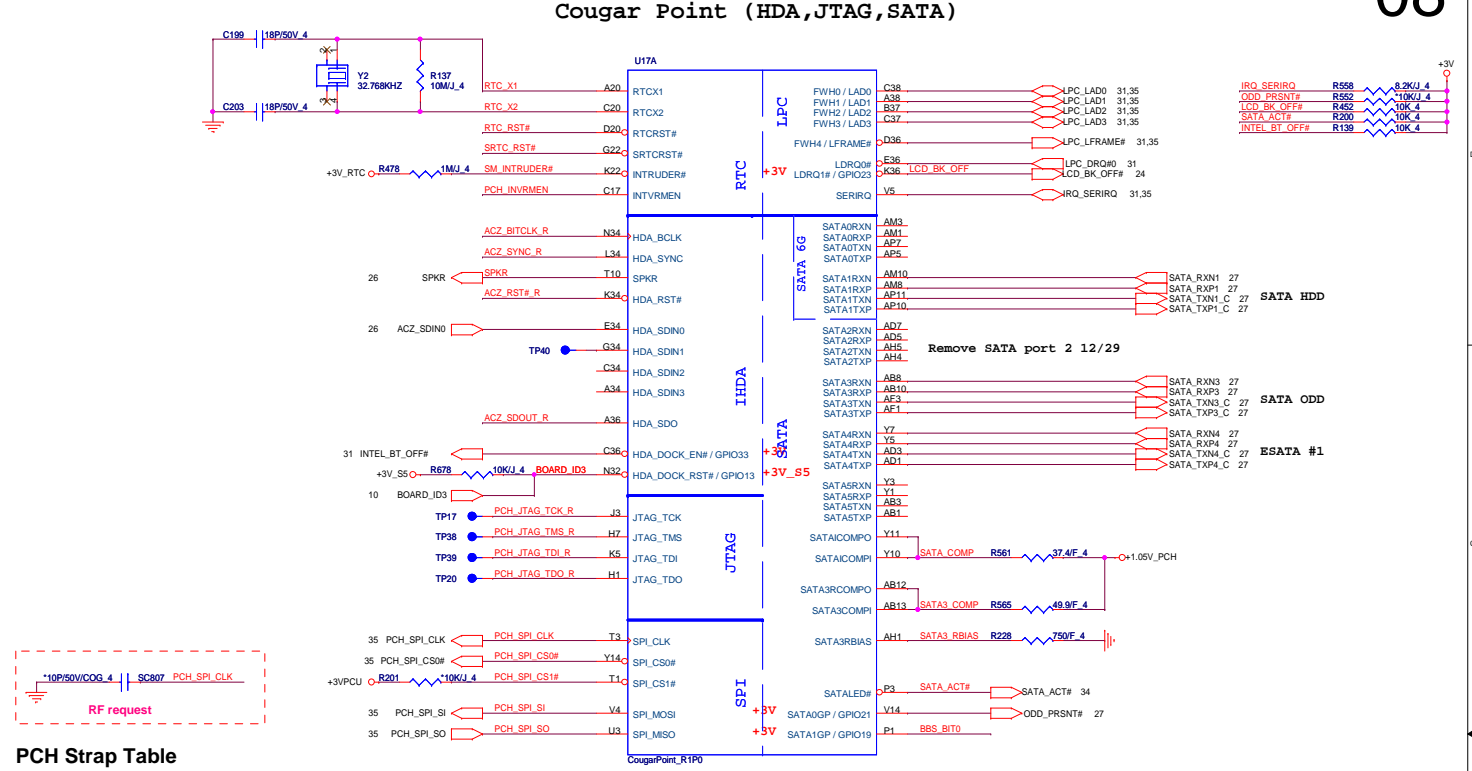
PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)



PCH2 ( CLG)

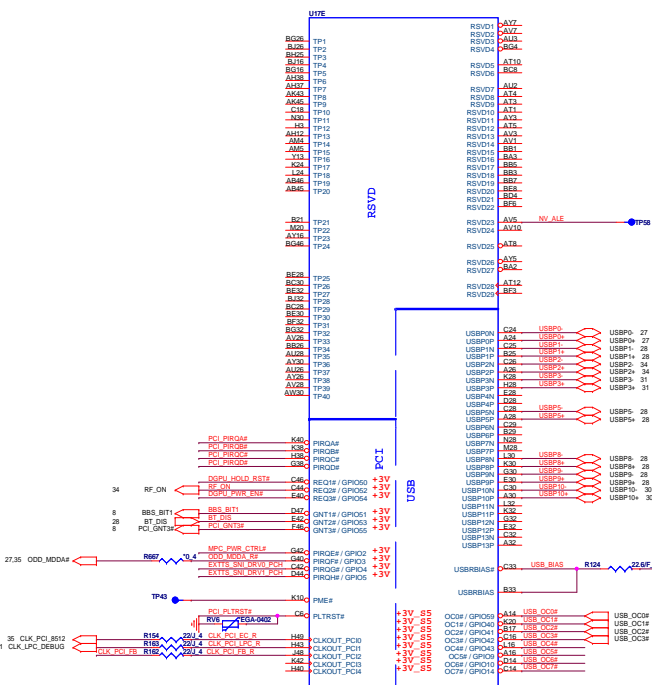


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V<sub>O</sub> R567 1KJ 4 SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R521 1KJ 4 PCI_GNT3# 9									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC<sub>O</sub> R121 330KJ 4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	<b>Default weak pull-up on GNT0/1#</b> <b>[Need external pull-down for LPC BIOS]</b> R504 1KJ 4 BBS_BIT1 9 R193 1KJ 4 BBS_BIT0
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5<sub>O</sub> R463 1KJ 4 ACZ_SDOUT_R									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R265 2.2KJ 4 DF_TVS 10 R266 3.7KJ 4 H_SNB_IVB# 3									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R522 1KJ 4 PLL_OVDR_EN 10									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5<sub>O</sub> R81 1KJ 4 ACZ_SYNC_R									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V<sub>O</sub> R146 1KJ 4 PCH_SPI_SI									
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)										

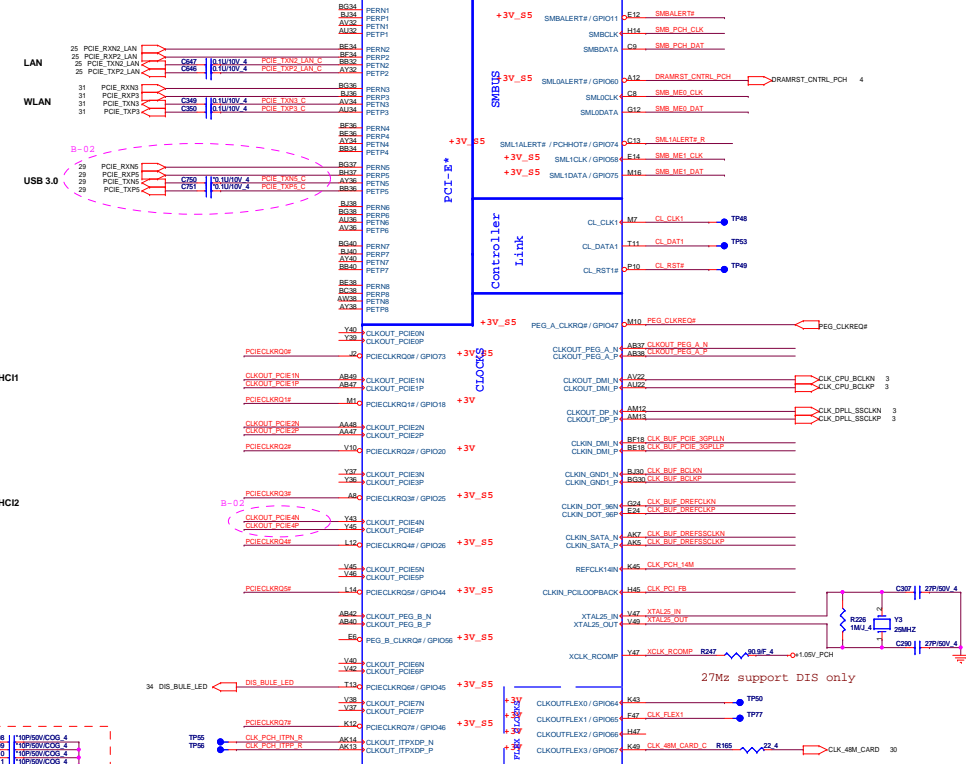


Cougar Point-M (PCI,USB,NVRAM)



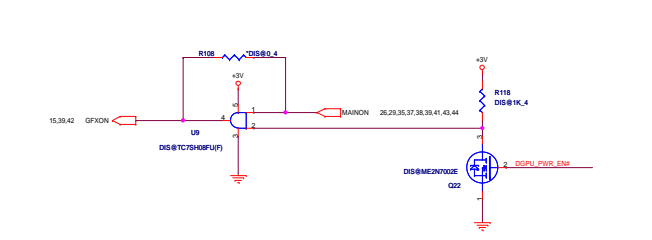
USB/eSATA Combo #1(Phoenix debug)
USB#0 - L port(BIOS debug)
CCD
WLAN
WAN(too common design reserved)
BlueTooth
USB#2 - R port(Right side)
USB #1 - R port(DB&BIOS debug)
Card Reader
USB port 6,7:disable for HM65.

Cougar Point-M (PCI-E, SMBUS, CLK)

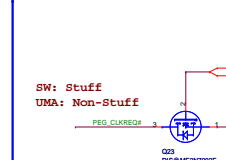


USB/eSATA Combo #1(Phoenix debug)
USB#0 - L port(BIOS debug)
CCD
WLAN
WAN(too common design reserved)
BlueTooth
USB#2 - R port(Right side)
USB #1 - R port(DB&BIOS debug)
Card Reader
USB port 6,7:disable for HM65.

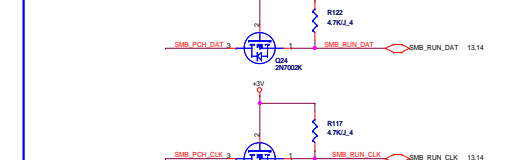
DGPU Power ON



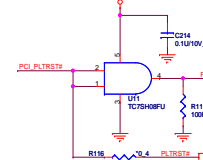
PEG CLK detect



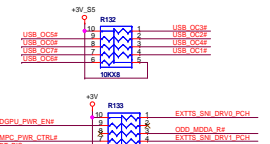
SMBus(CLK)



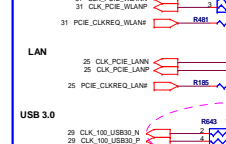
PLTRST#(CLG)



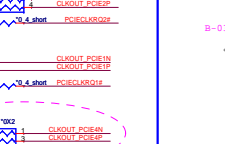
PCI/USB0C# Pull-up(CLG)



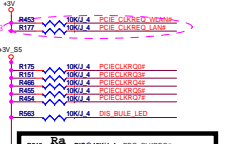
WLAN



LAN



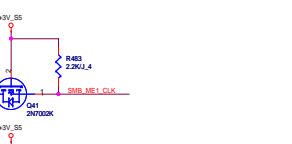
USB 3.0



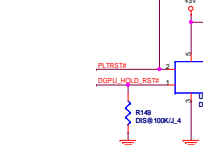
CLK\_REQ/Strap Pin(CLG)



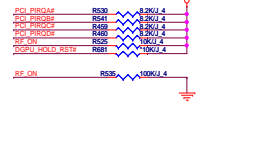
SMBus/Pull-up(CLG)



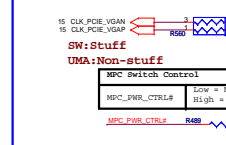
GPU RST#(CLG)



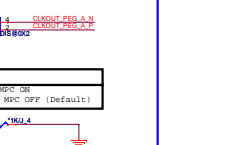
PCI/USB0C# Pull-up(CLG)



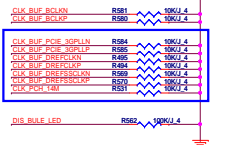
WLAN



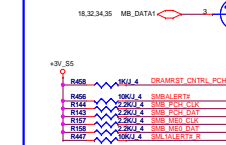
LAN



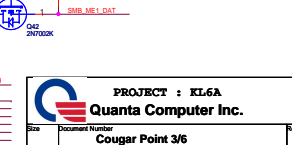
USB 3.0



CLK\_REQ/Strap Pin(CLG)

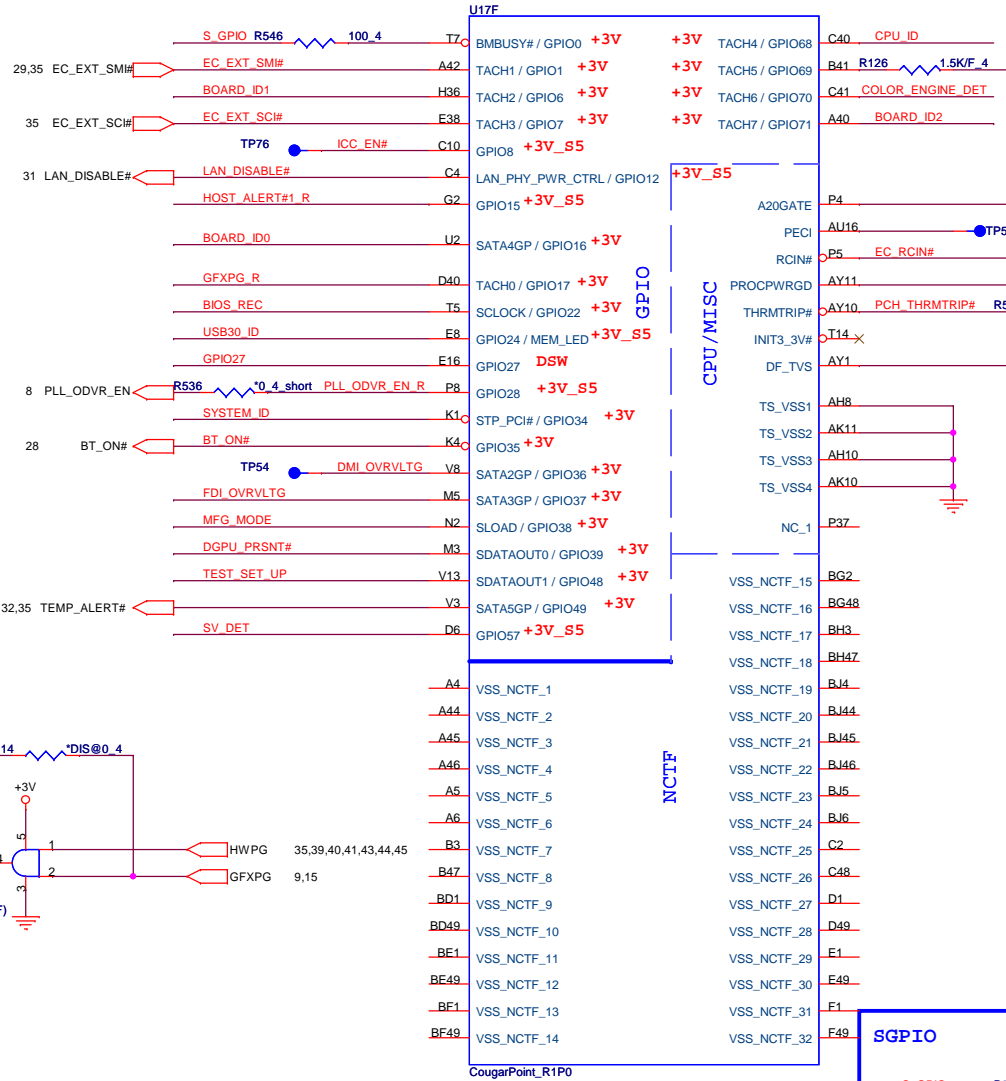


SMBus/Pull-up(CLG)

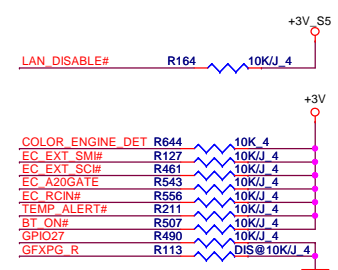


PROJECT : XL6A
Quanta Computer Inc.
Cougur Point 3/6
Date: Friday, October 28, 2011

## Cougar Point (GPIO,VSS\_NCTF,RSVD)



### GPIO Pull-up/Pull-down(CLG)

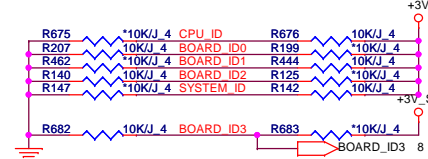


Board ID For Function	SYSTEM_ID GPIO34	ID2 GPIO71	ID3 GPIO13	ID1 GPIO6	ID0 GPIO16	CPU_ID GPIO68	Board ID
SDV	1	1	0	0	0	1	B-04
SIV	1	1	0	0	1	1	Board ID use below GPIO: BOARD_ID0 BOARD_ID1 BOARD_ID3
SIT	1	1	0	1	0	1	
SVT	1	1	0	1	1	1	
SOVP	1	1	1	0	0	1	

**ID2: 0-->6 layer  
1-->8 layer**

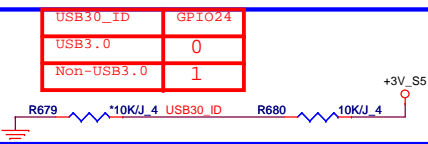
**System ID: 0-->KL5  
1-->KL6**

**CPU\_ID: 0-->35W  
1-->45W**



**SV\_SET\_UP**

High = Strong (Default)



**TEST\_SET\_UP**

R559 10K/J 4 R555 10K/J 4

**HOST\_ALERT#1 R R508 1K/J 4**

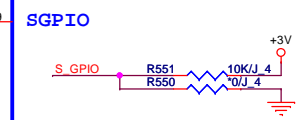
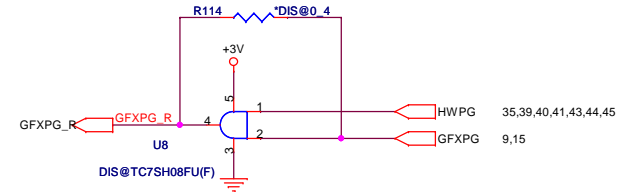
Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

	SWITCHABLE	UMA
Stuff	R532	R533
No Stuff	R533	R532

R533 \*10K/J 4 DGPU\_PRSN# R532 DIS@100K/J 4



**FDI TERMINATION VOLTAGE OVERRIDE**

LOW - Tx, Rx terminated to same voltage

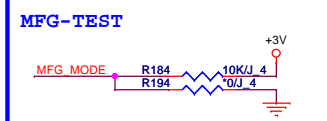
**DMI TERMINATION VOLTAGE OVERRIDE**

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

**BIOS RECOVERY**

High = Disable (Default)

Low = Enable



**PROJECT : KL6A**

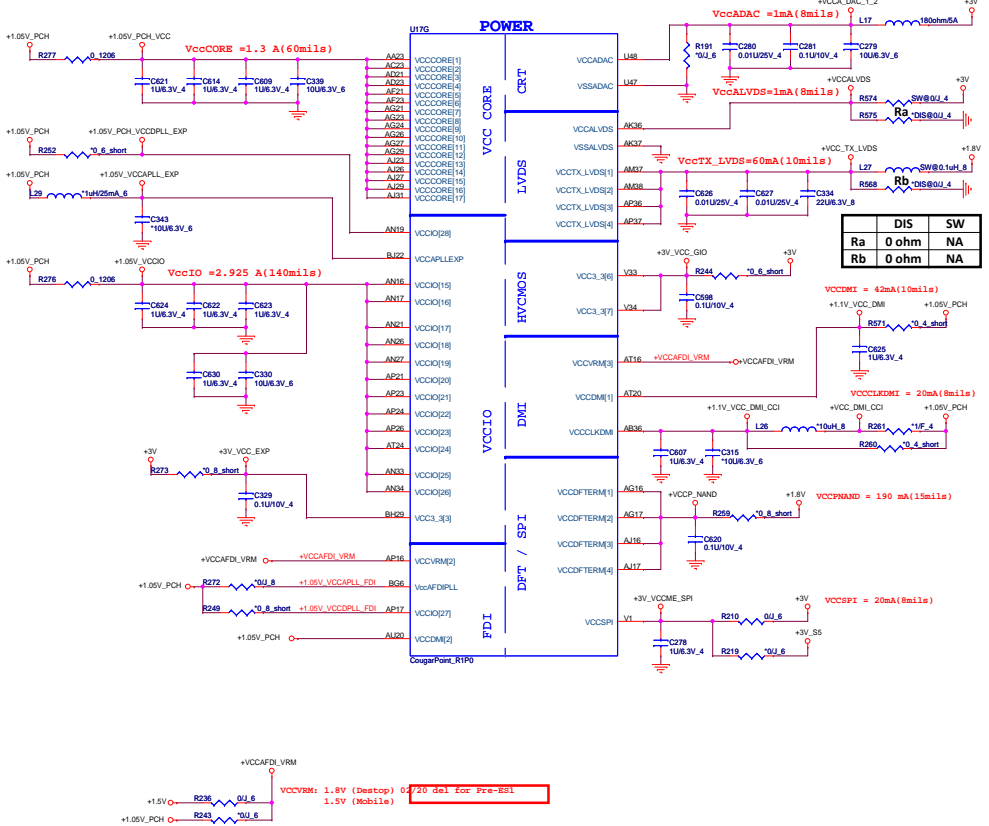
**Quanta Computer Inc.**

Size Document Number

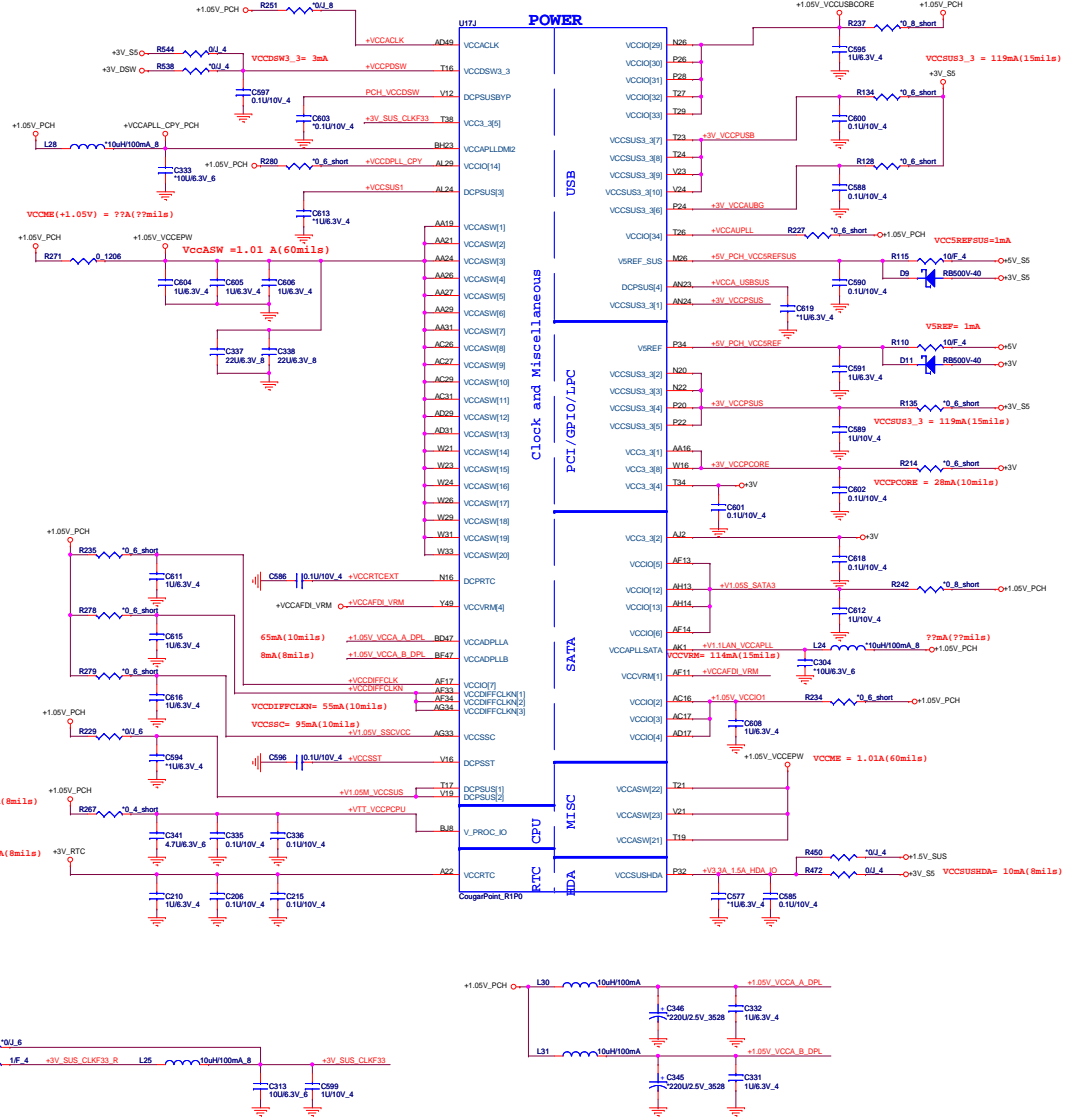
**Cougar Point 4/6**

Date: Friday, October 29, 2010 Sheet 10 of 47 Rev 1A

COUGAR POINT (POWER)

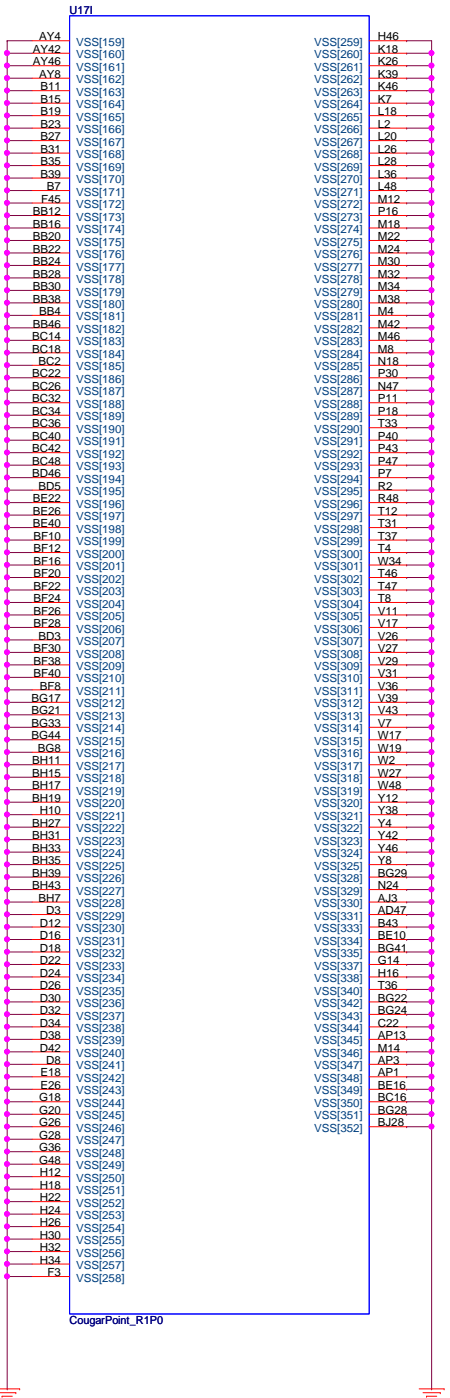
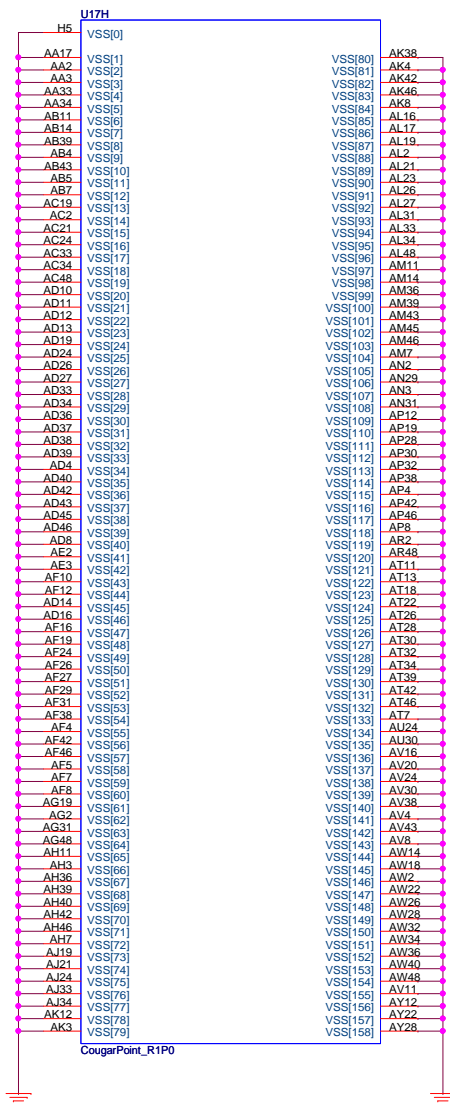


Cougar Point-M (POWER)



VCCVRM: 1.8V (Desktop) 1.5V (Mobile) 20 dsl for Pre-ES1

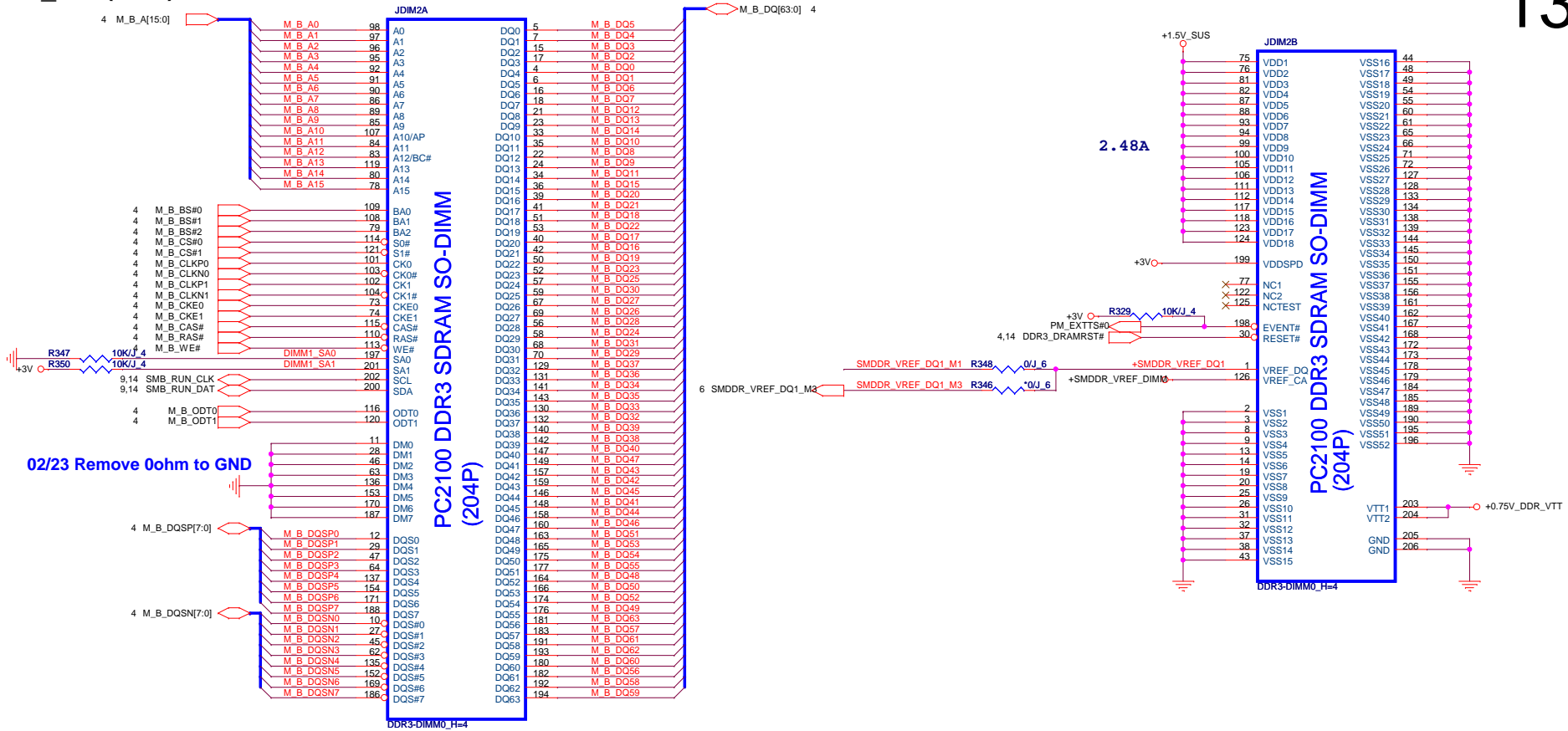
IBEX PEAK-M (GND)



**PROJECT : KL6A**  
**Quanta Computer Inc.**

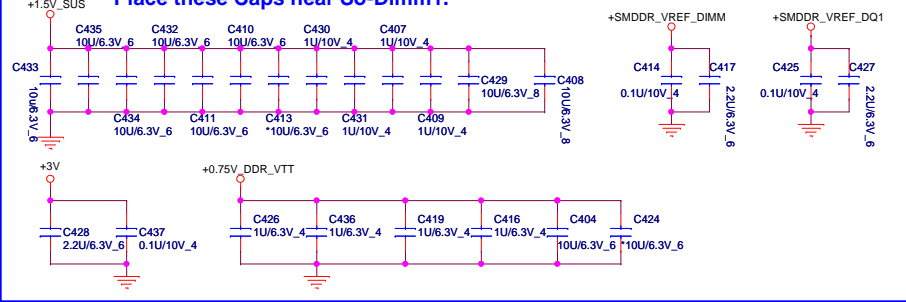
Size Document Number Rev 1A  
**Cougar Point 6/6**

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02/23 Remove 0ohm to GND

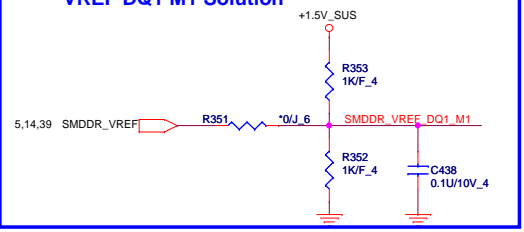
Place these Caps near So-Dimm1.



VREF DQ1 M2 Solution



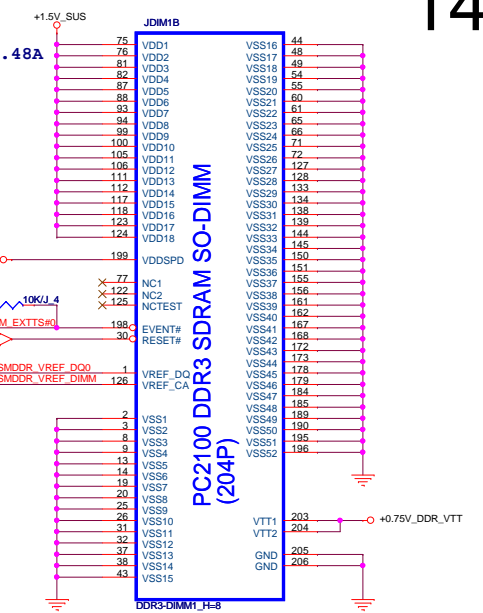
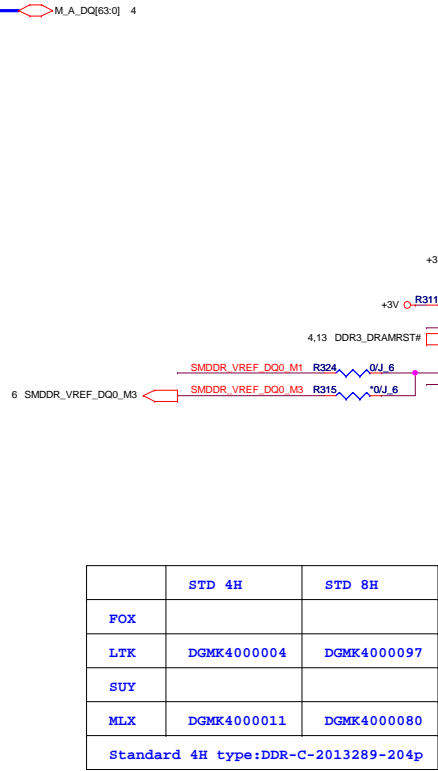
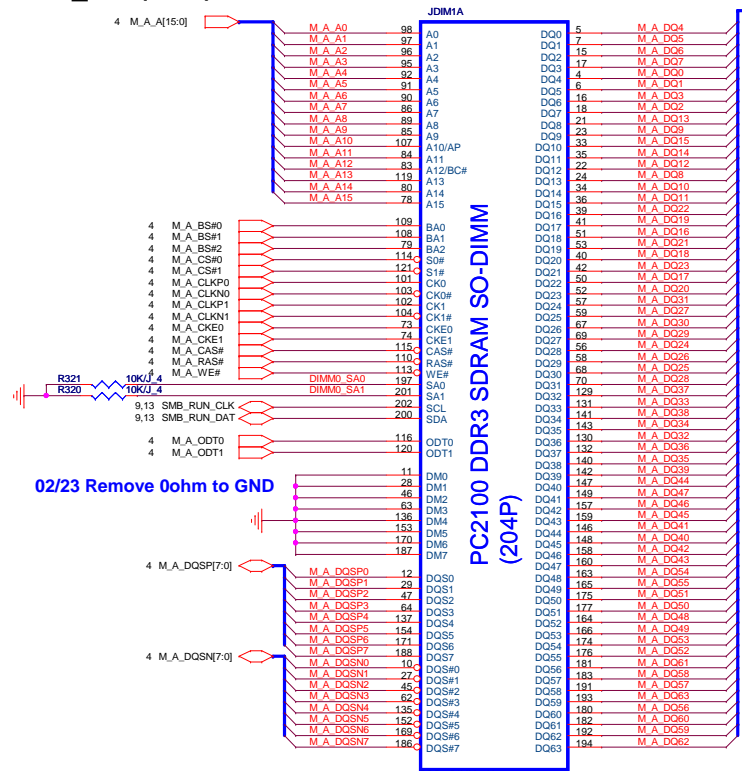
VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

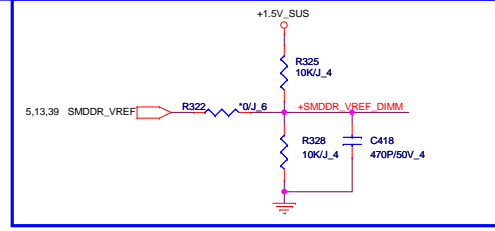
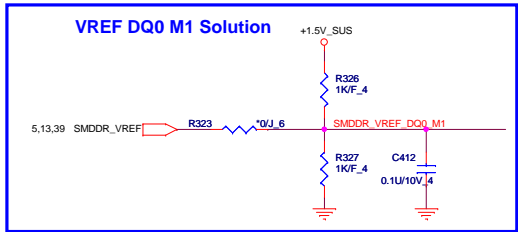
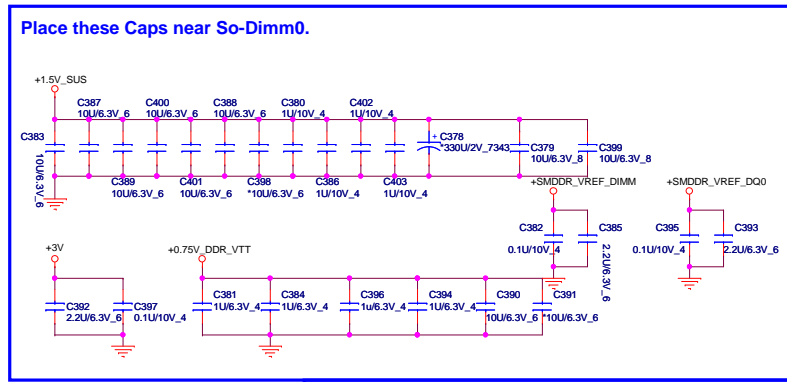
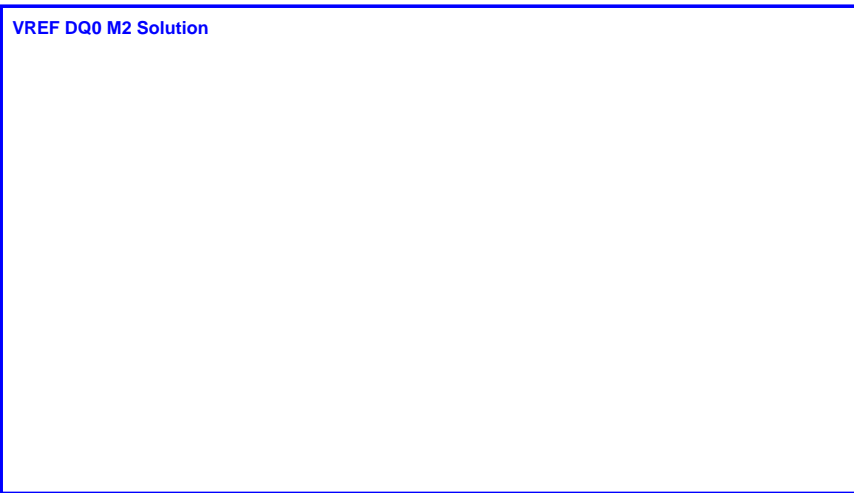
**PROJECT : KL6A**  
**Quanta Computer Inc.**

Size: Document Number: **DDR3 SO-DIMM-0** Rev: 1A  
 Date: Friday, October 29, 2010 Sheet: 13 of 47

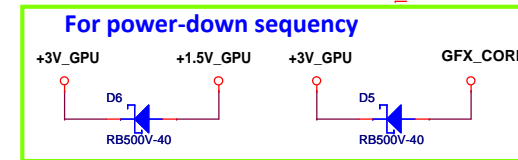
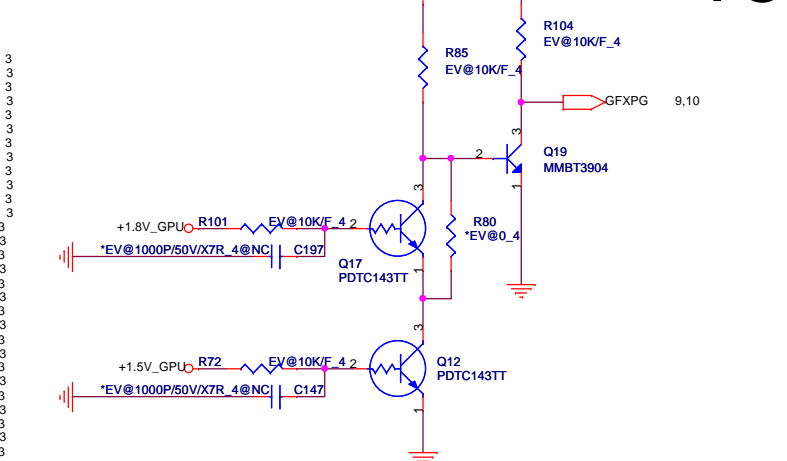
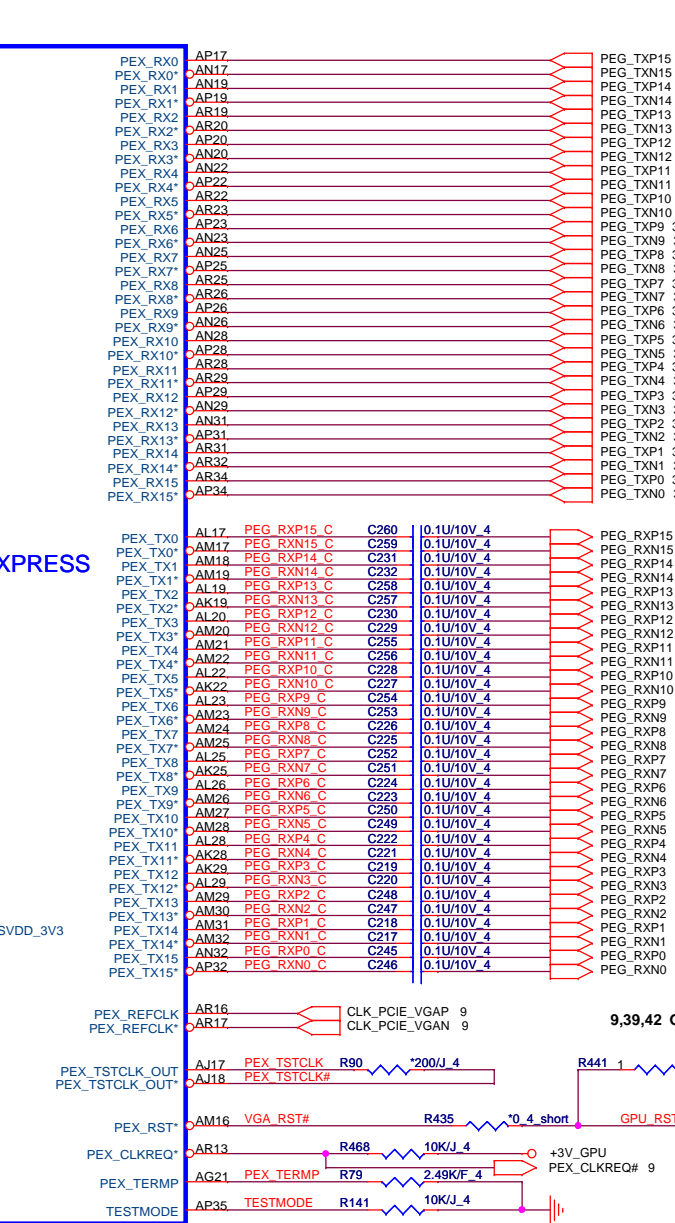
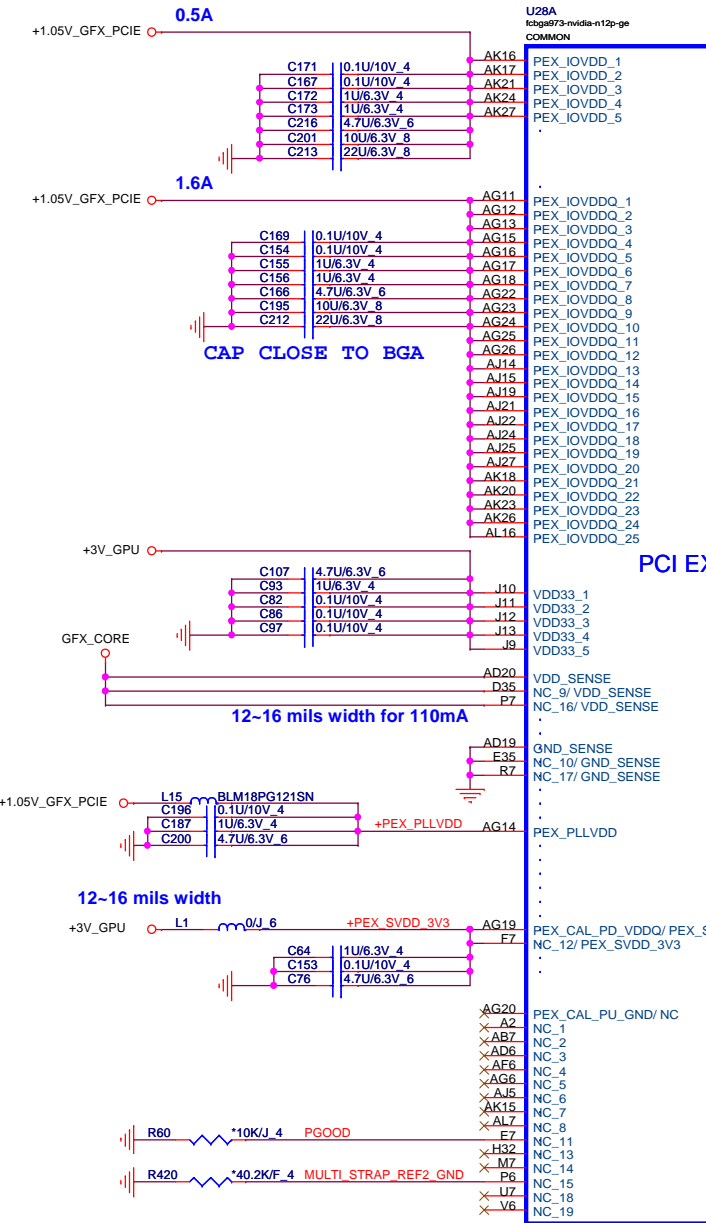


	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 4H type:DDR-C-2013289-204p

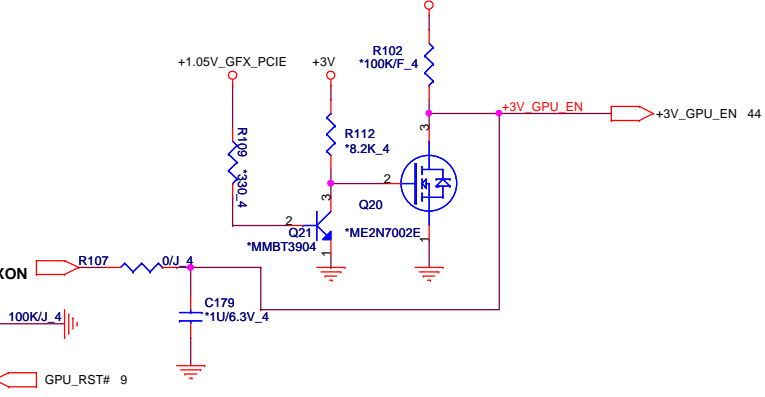


PEX\_IOVDD+PEX\_IOVDDQ+PEX\_PLLVDD > 2.2A



The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

- ▶ NVVDD <= VDD33+0.5 V
- ▶ FBVDDQ <= VDD33+0.5 V



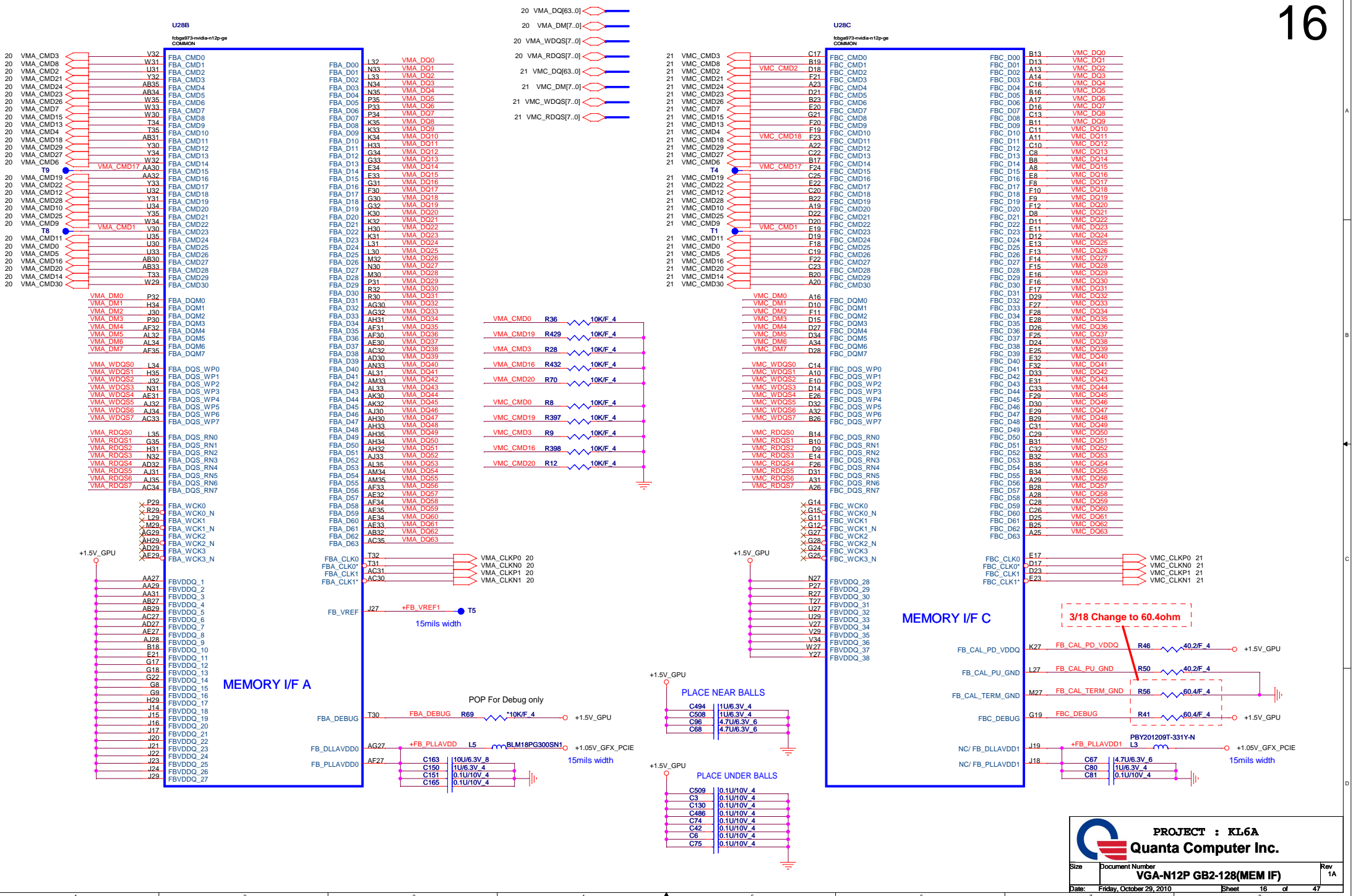
**PROJECT : KL6A**

**Quanta Computer Inc.**

Size Document Number Rev 1A

**VGA-N12P GB2-128(PCle)**

Date: Friday, October 29, 2010 Sheet 15 of 47

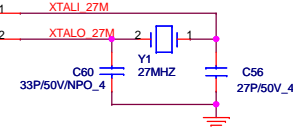
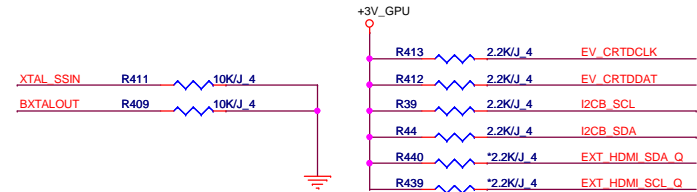
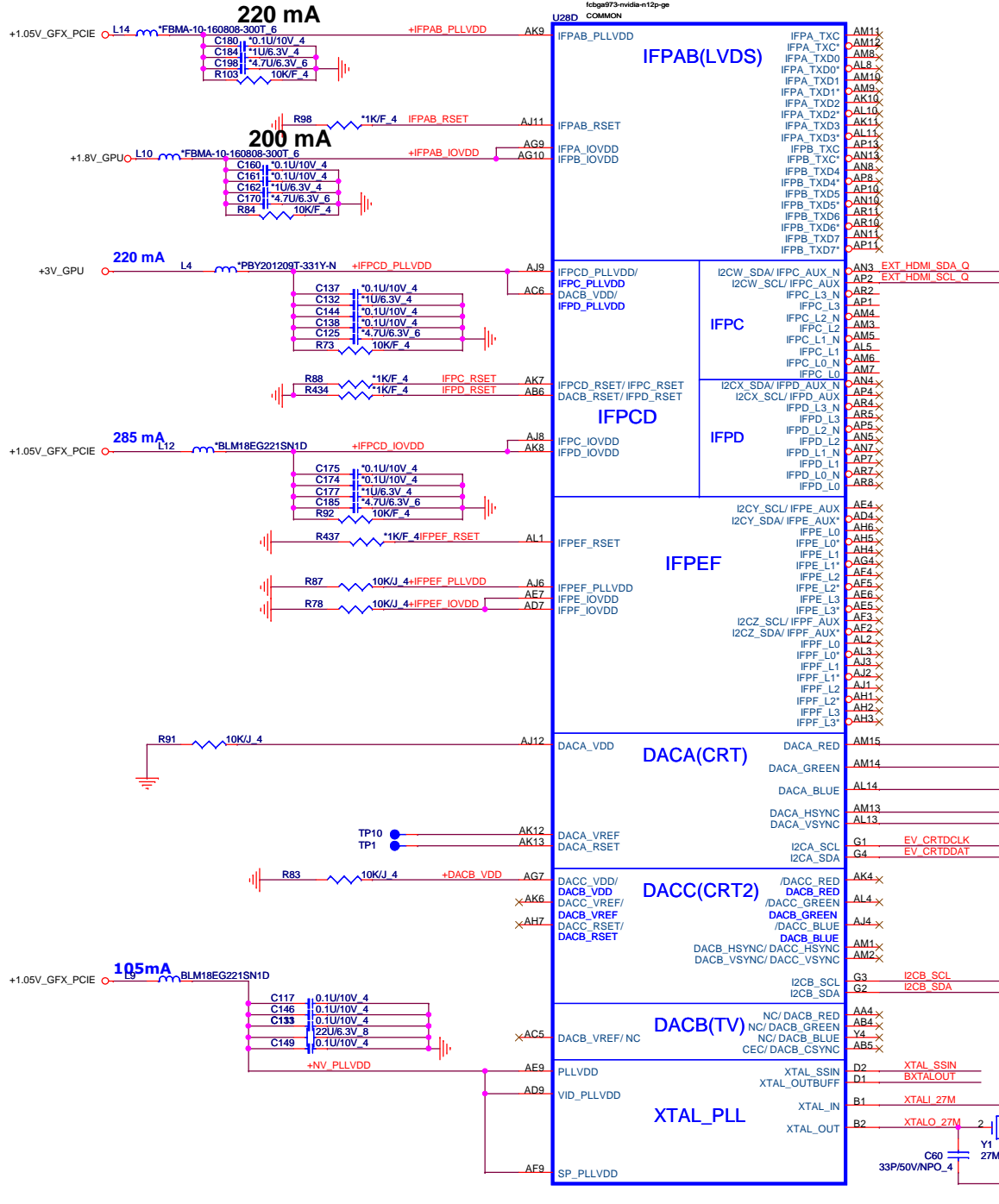


**PROJECT : KL6A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>VGA-N12P GB2-128(MEM IF)</b>	<b>1A</b>
Date:	Friday, October 29, 2010	Sheet 16 of 47



4/28 Enable LVDS For 3DV



**PROJECT : KL6A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>VGA-N12P GB2-128(Display)</b>	<b>1A</b>
Date:	Friday, October 29, 2010	Sheet 18 of 47

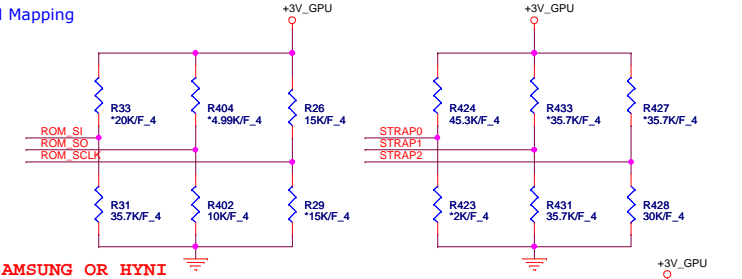
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK		PCI_DEVICE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0101
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGH7500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW01	AKD5LZWTW00	H5TQ1G63BFR-11C
0x6(0110)	800MHz 2GB(128M*16) Hynix	AKD5MGWTW01	AKD5MGWTW06	H5TQ2G63BFR-12C
0x7(0111)	800MHz 2GB(128M*16) Samsung	AKD5MGGT501	AKD5MGGT507	K4W2G1646B-HC12
0x6(0110)	900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

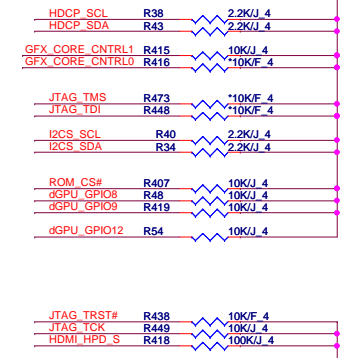
ROM\_SI Strap Bit for RAM Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



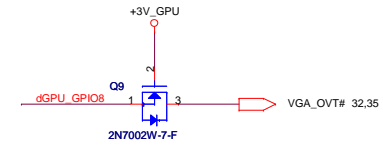
SAMSUNG OR HYNIX

- N12P-GE ROM\_SO 10K pull low  
Strap2 30K pull low
- N12P-GV1 ROM\_SO 10K pull low  
Strap2 45K pull low
- N12P-GV ROM\_SO 10K pull high  
Strap2 45K pull high  
Strap3 5K pull low  
Strap4 20K pull low

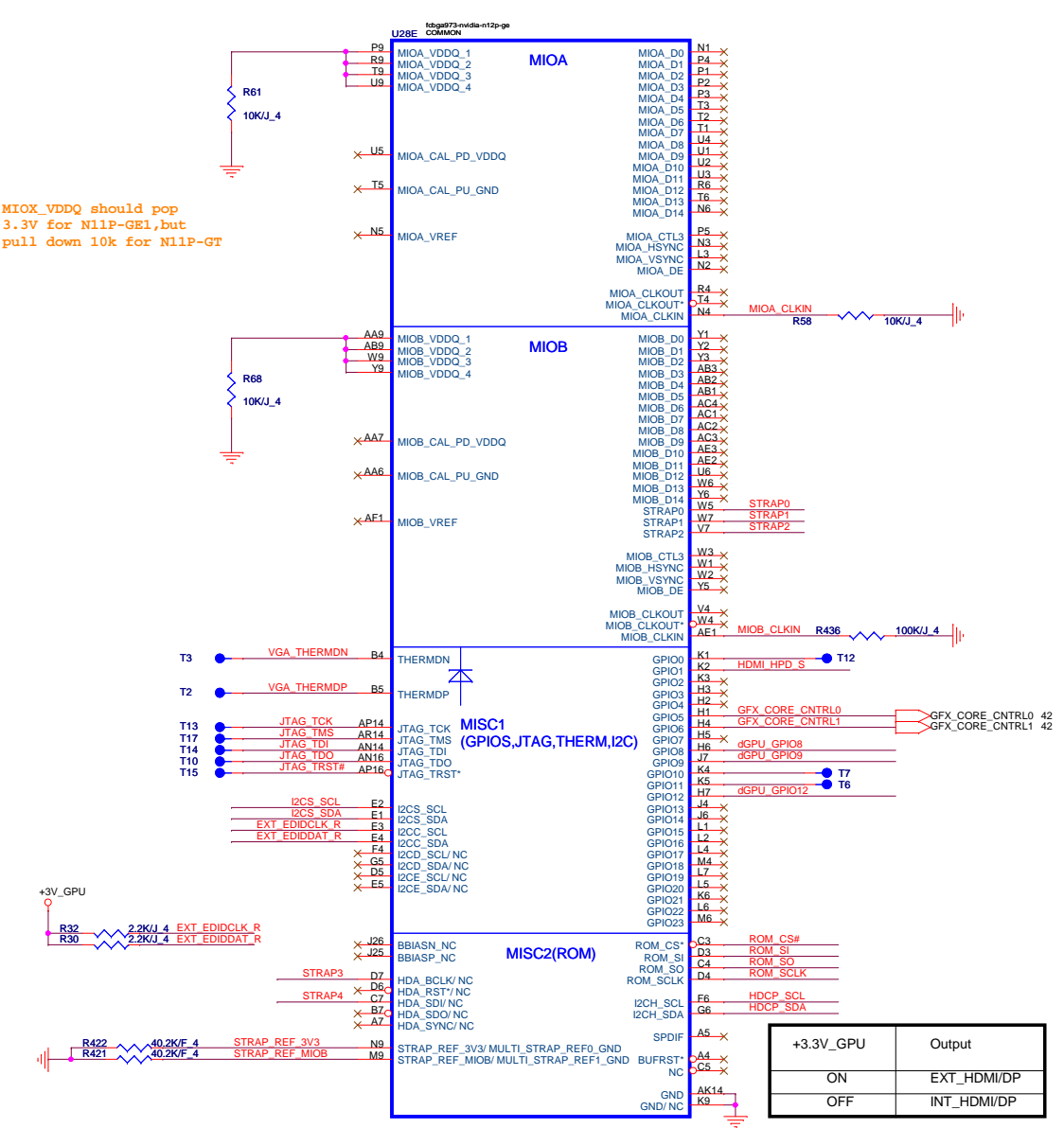


### GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	N/A	
3	OUT	N/A	
4	OUT	N/A	
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

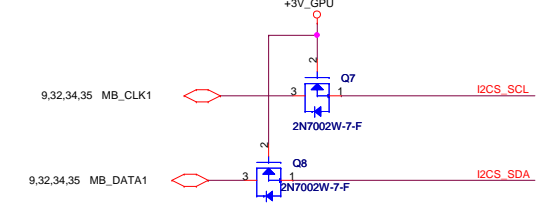


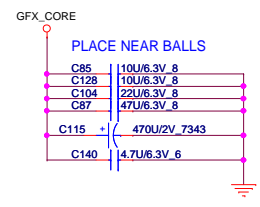
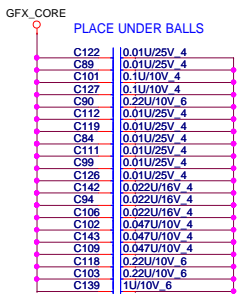
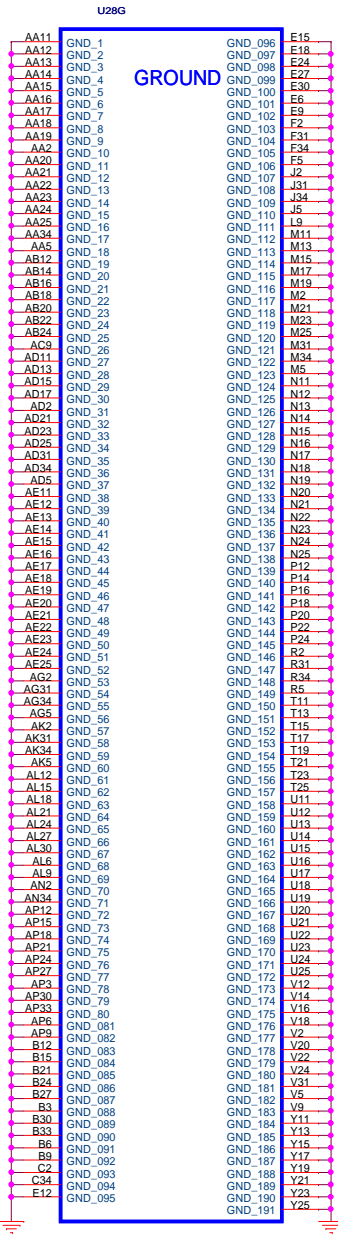
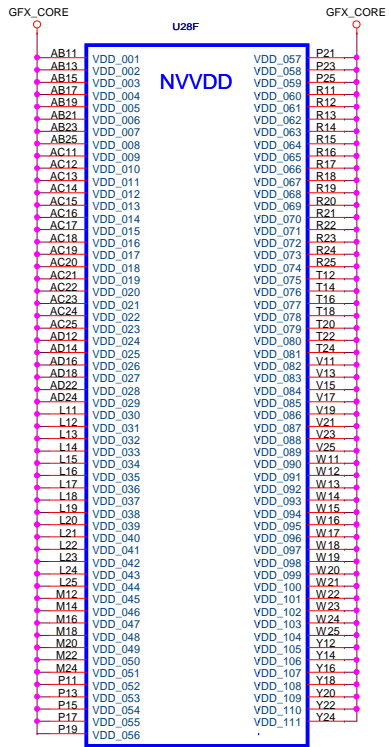
MIOX\_VDDQ should pop 3.3V for N11P-GE1, but pull down 10k for N11P-GT



+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP

Using internal thermal sensor





**PROJECT : KL6A**

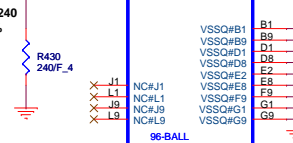
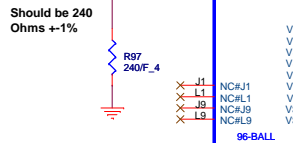
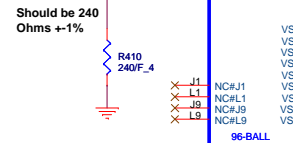
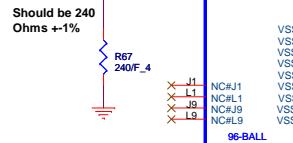
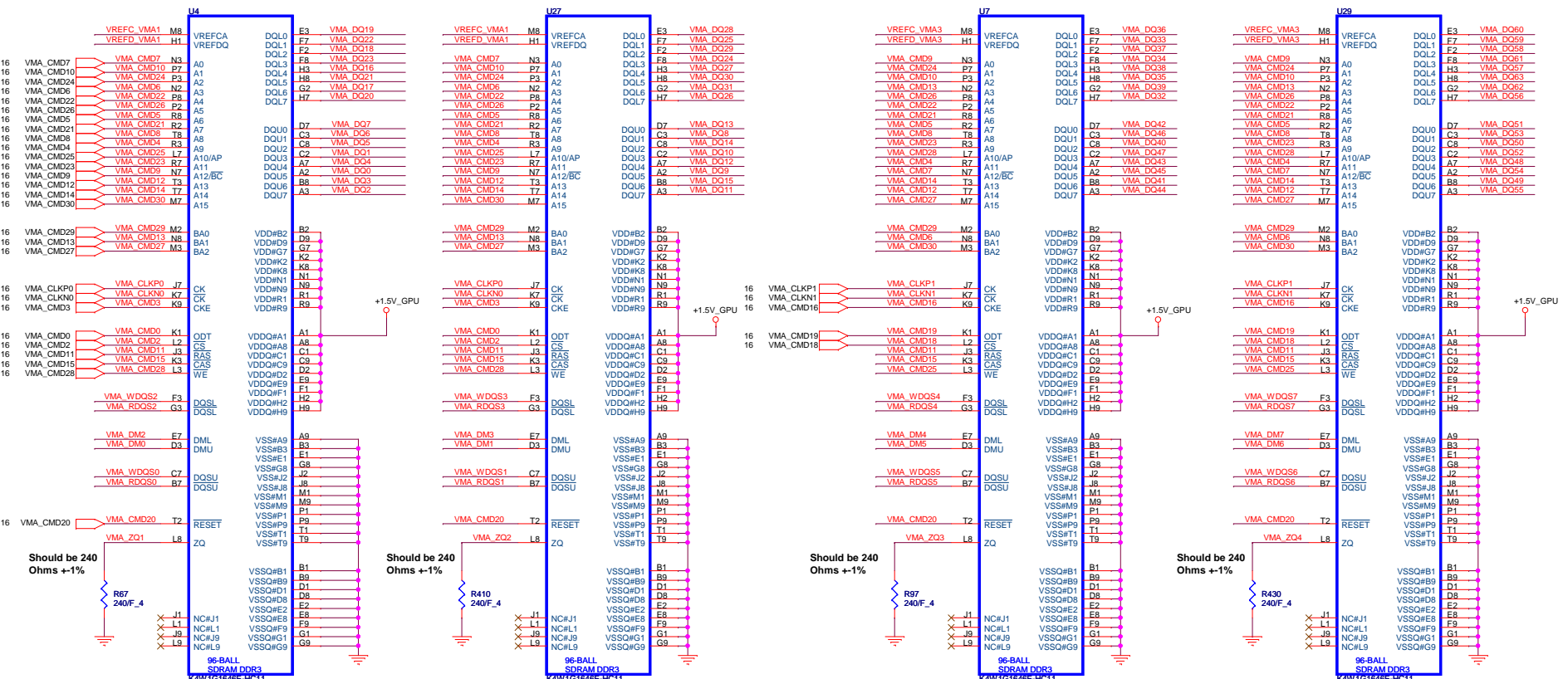
**Quanta Computer Inc.**

Size Document Number Rev 1A

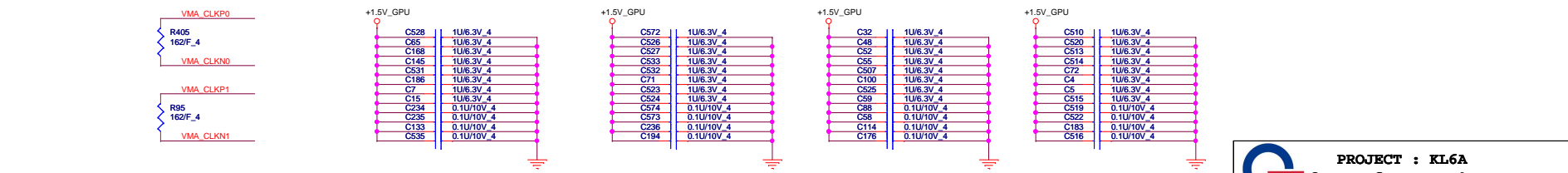
**VGA-N12P GB2-128(POWER)**

Date: Friday, October 29, 2010 Sheet 19 of 47

## CHANNEL A: 512MB/1024MB DDR3



Placement has to be close to VRAM

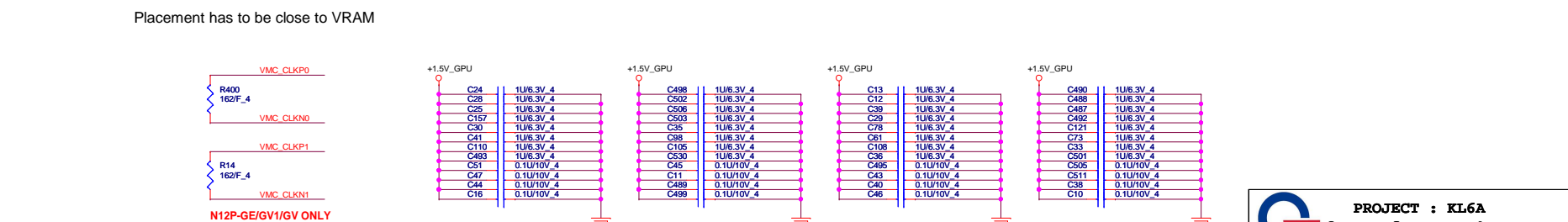
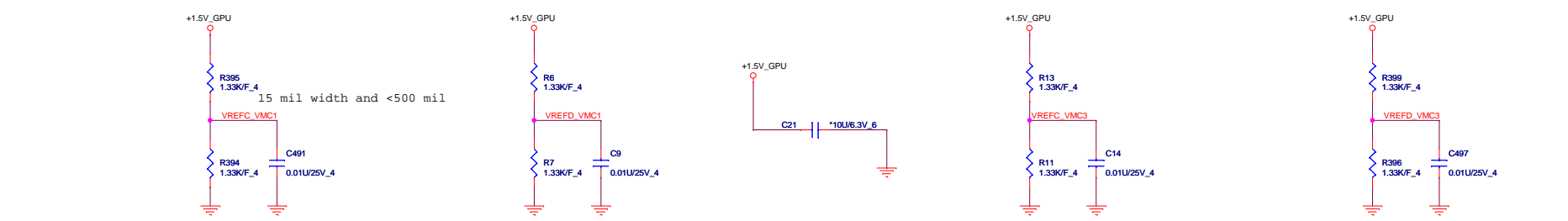
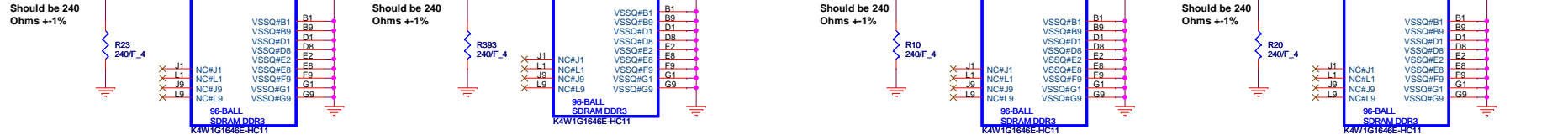
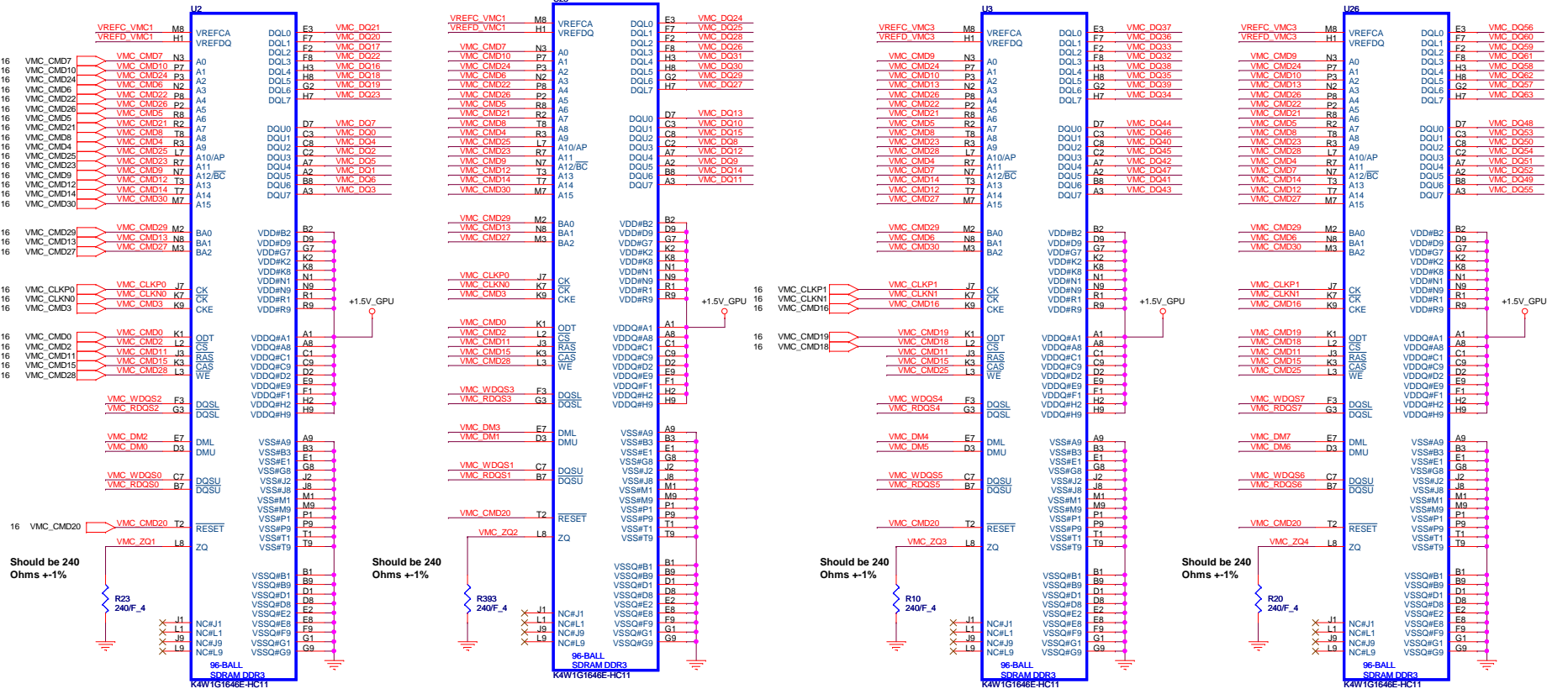


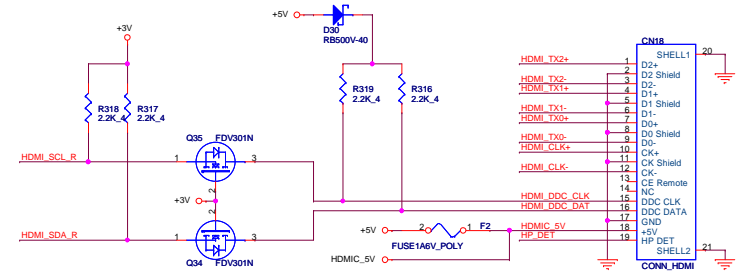
**PROJECT : KL6A**  
**Quanta Computer Inc.**

Size: \_\_\_\_\_ Document Number: **VGA-N12P GB2-128(VRAM-1)** Rev: 1A

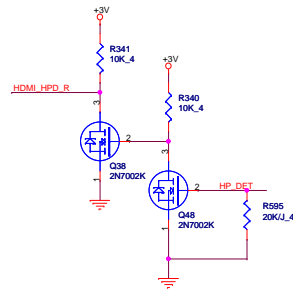
Date: Friday, October 28, 2010 Sheet: 20 of 47

CHANNEL B: 512MB/1024MB DDR3

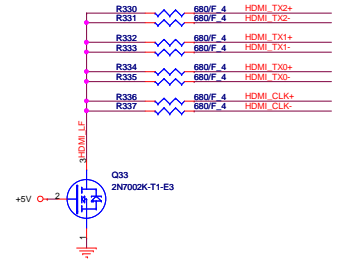




HDMI Hot-PLUG to EC and GPU



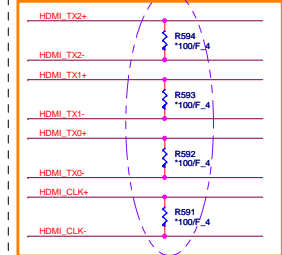
7_INT_HDMI_TXDP2	C688	0.1U/10V/X5R_4	HDMI_TX2+
7_INT_HDMI_TXDN2	C687	0.1U/10V/X5R_4	HDMI_TX2-
7_INT_HDMI_TXDP1	C686	0.1U/10V/X5R_4	HDMI_TX1+
7_INT_HDMI_TXDN1	C685	0.1U/10V/X5R_4	HDMI_TX1-
7_INT_HDMI_TXDP0	C684	0.1U/10V/X5R_4	HDMI_TX0+
7_INT_HDMI_TXDN0	C683	0.1U/10V/X5R_4	HDMI_TX0-
7_INT_HDMI_TXCP	C682	0.1U/10V/X5R_4	HDMI_CLK+
7_INT_HDMI_TXCN	C681	0.1U/10V/X5R_4	HDMI_CLK-



RClamp0514M_AG USB		RClamp0514M_AG USB		
HDMI_TX2+	1	10	HDMI_TX2+	
HDMI_TX2-	2	10	HDMI_TX2-	
HDMI_TX1+	4	VCC	7	HDMI_TX1+
HDMI_TX1-	5	GND	8	HDMI_TX1-
HDMI_TX0+	1	10	HDMI_TX0+	
HDMI_TX0-	2	10	HDMI_TX0-	
HDMI_CLK+	4	VCC	7	HDMI_CLK+
HDMI_CLK-	5	GND	8	HDMI_CLK-
HDMI_DDC_DAT	1	10	HDMI_DDC_DAT	
HDMI_DDC_CLK	2	10	HDMI_DDC_CLK	
HDMIC_SV	4	VCC	7	HDMIC_SV
HP_DET	5	GND	8	HP_DET

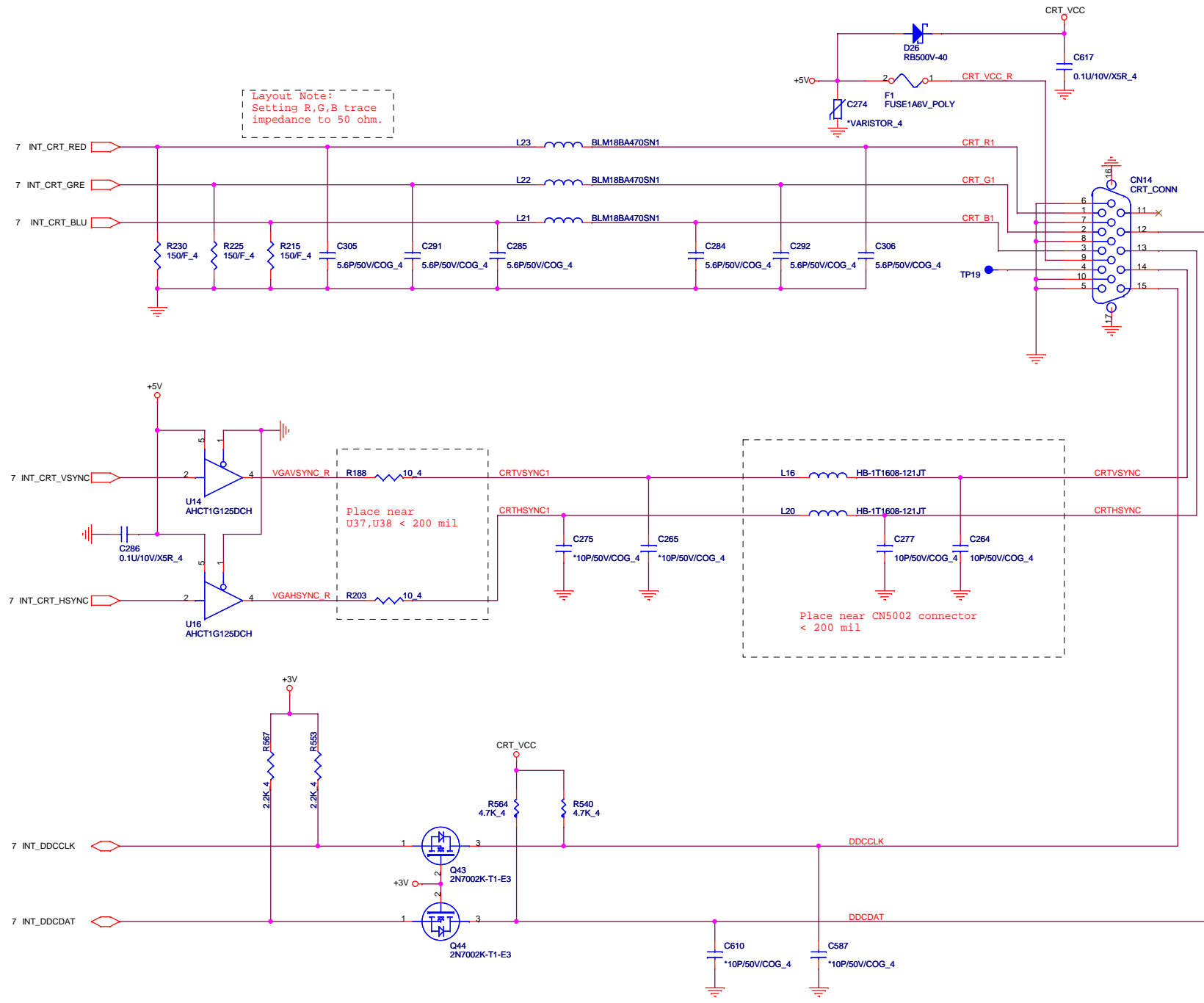
For ESD Layout note: Place close to HDMI Conn

EMI reserve for HDMI



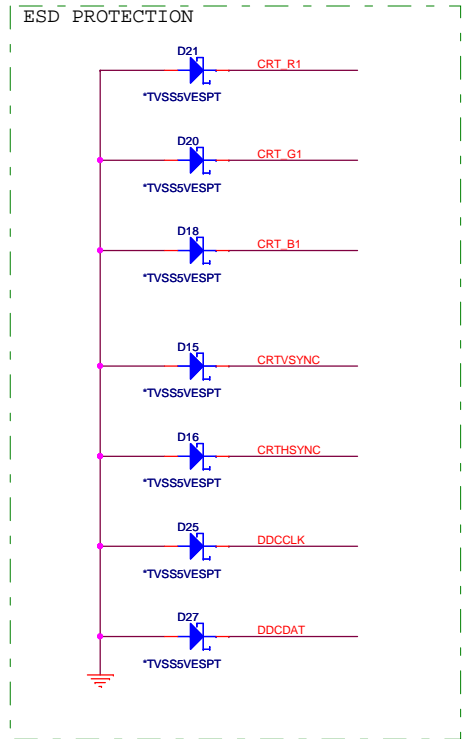


Layout Note:  
Setting R,G,B trace  
impedance to 50 ohm.

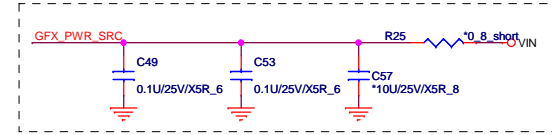
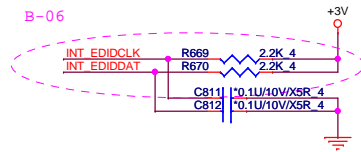
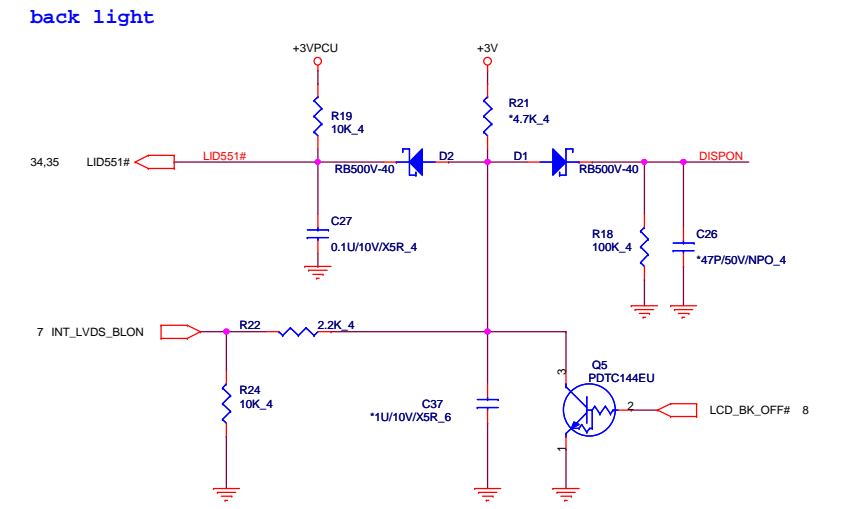
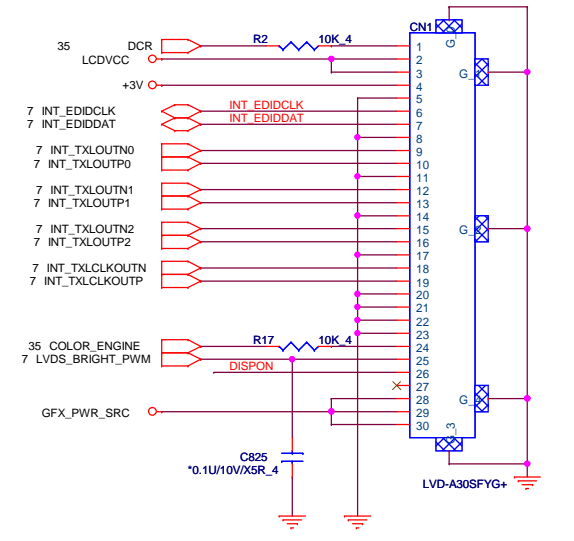
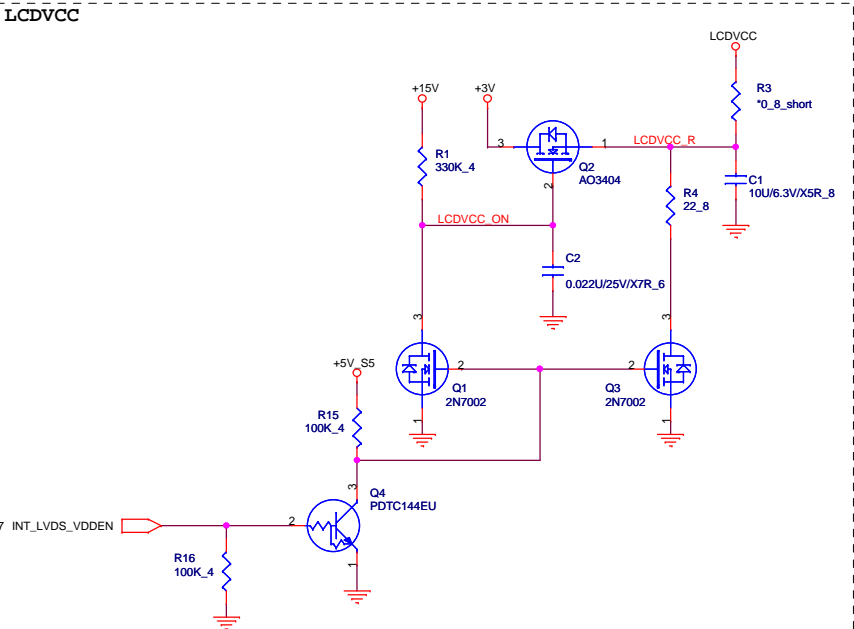
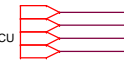


Place near  
U37, U38 < 200 mil

Place near  
CN5002 connector  
< 200 mil

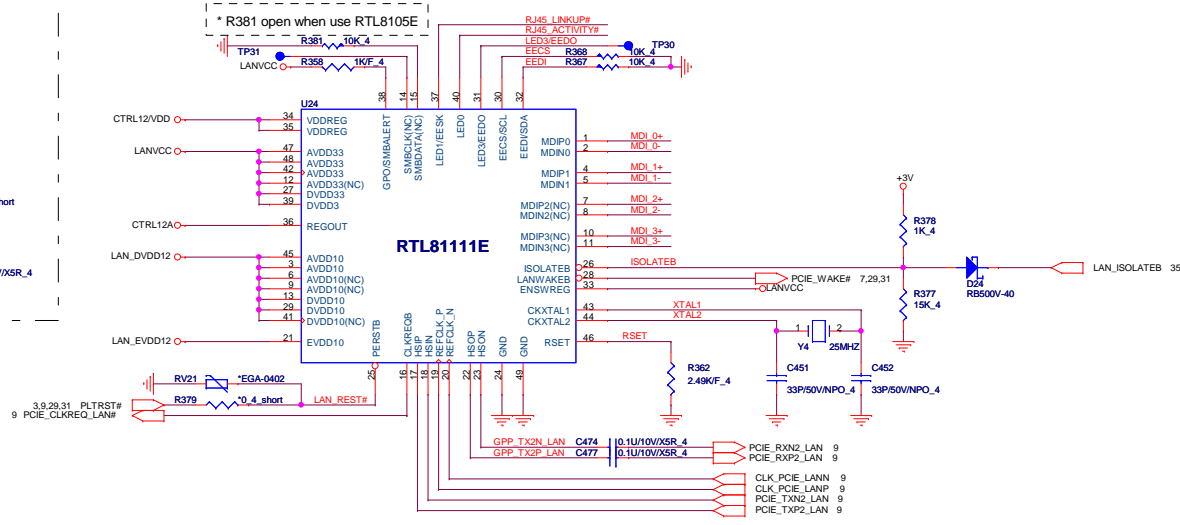
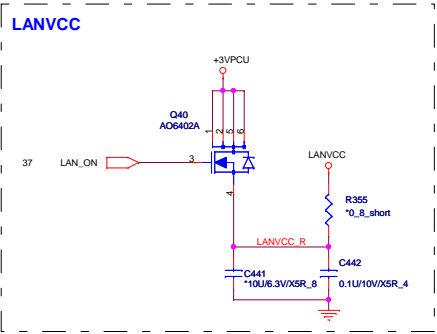


7,8,9,10,11,13,14,15,22,23,25,26,27,28,29,30,31,32,34,35,36,37,38,42,43,44,45 +3V  
 27,28,29,37,39,40,41,44 +15V  
 7,8,25,27,33,34,35,37,38,40,41 +3VPCU  
 36,38,39,40,42,43,44,45 VIN

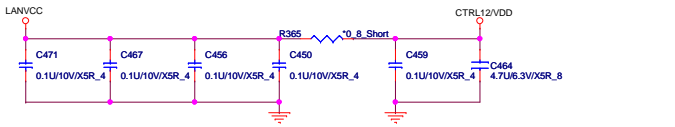


		<b>PROJECT : KL6A</b>	
		<b>Quanta Computer Inc.</b>	
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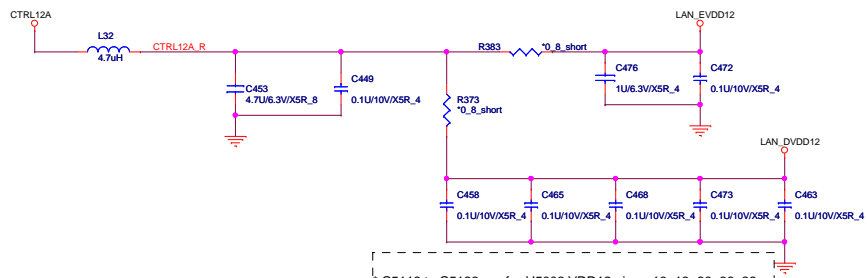




\* C476 and C472 are for U24 LAN\_EVDD12 pin 21.

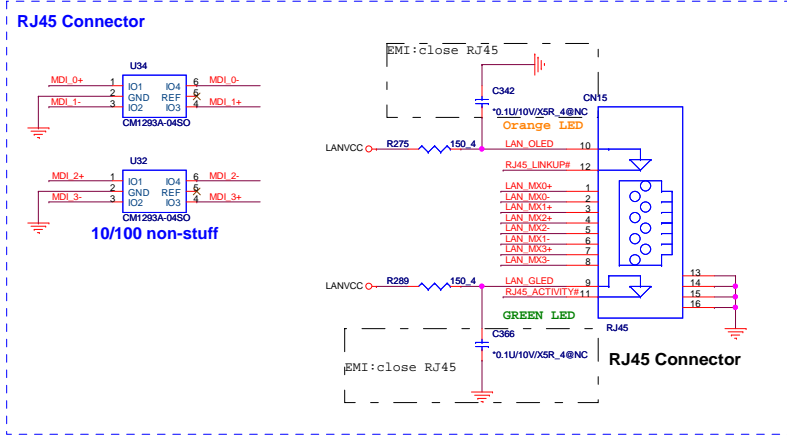
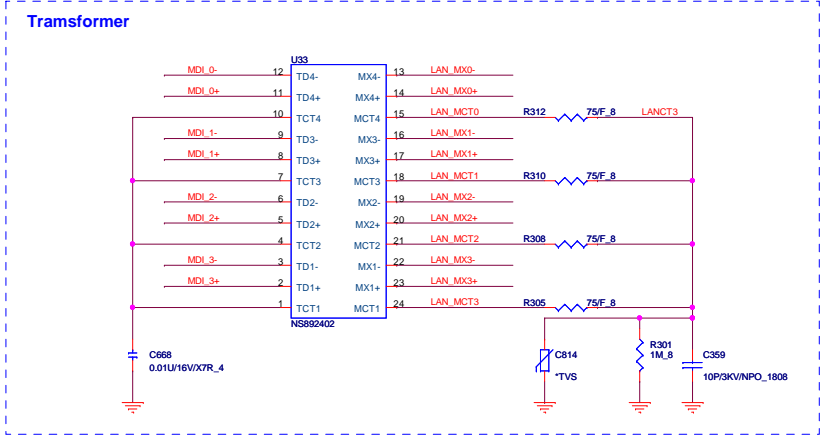


\* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40. Place C5113, C5094 closed to U5006 pins 44, 45, and 40.



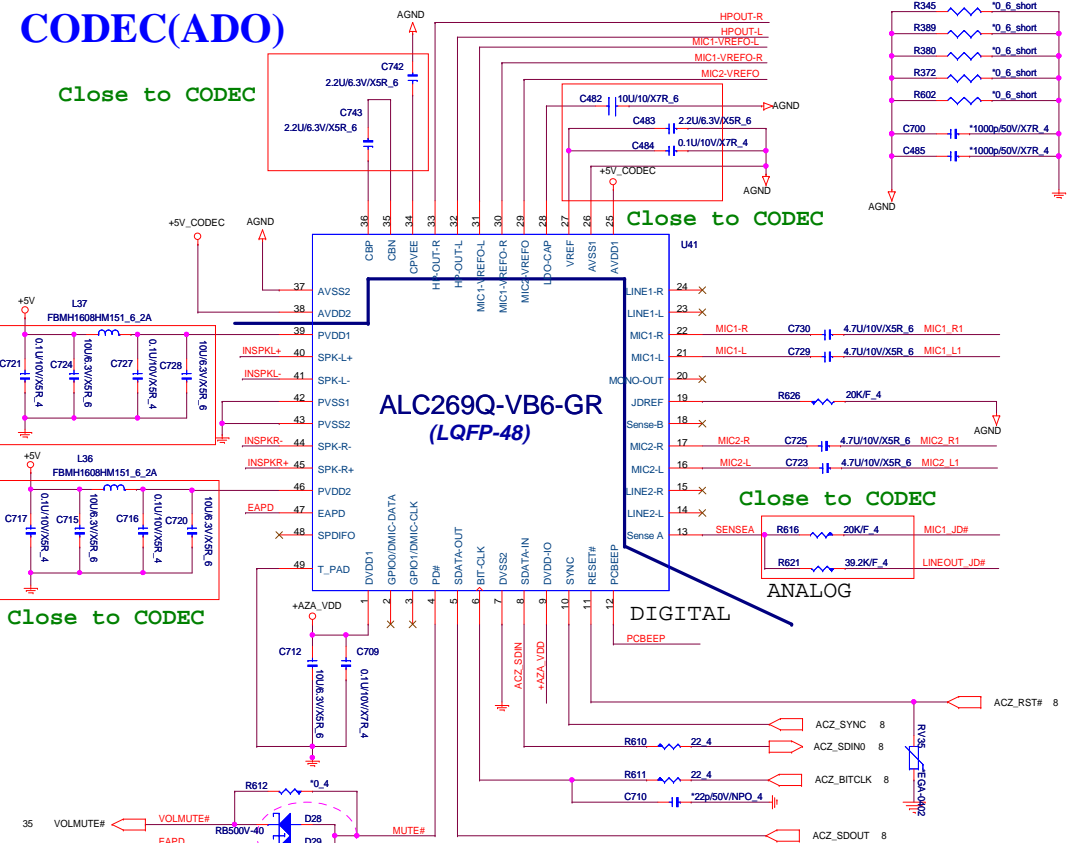
\* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Layout: All termination signal should have 20 mil trace



# CODEC(ADO)

Close to CODEC



Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

Close to CODEC

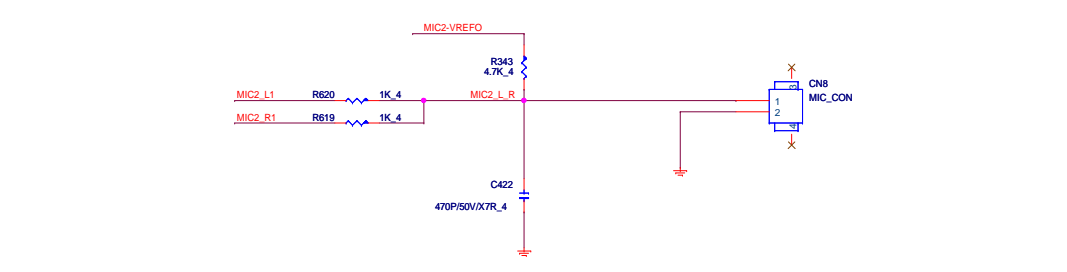
Close to CODEC

Close to CODEC

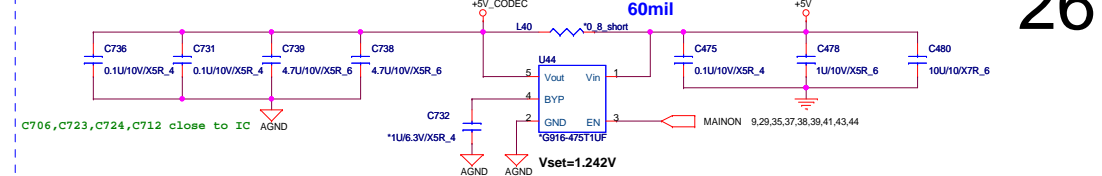
Close to CODEC

Close to CODEC

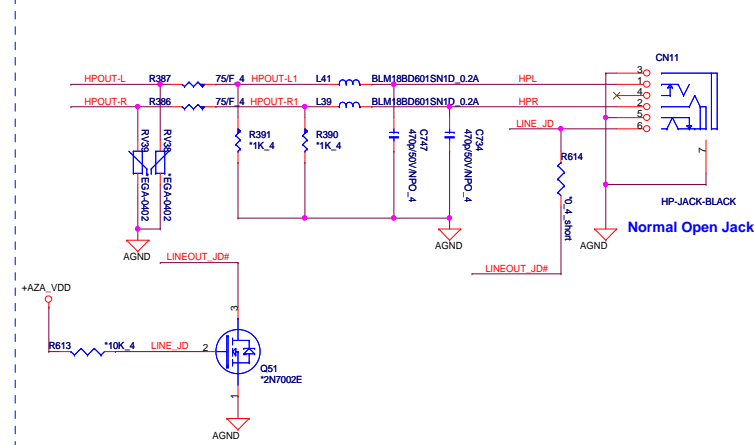
## INTERNAL MIC



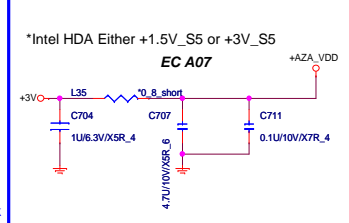
## Codec Power(ADO)



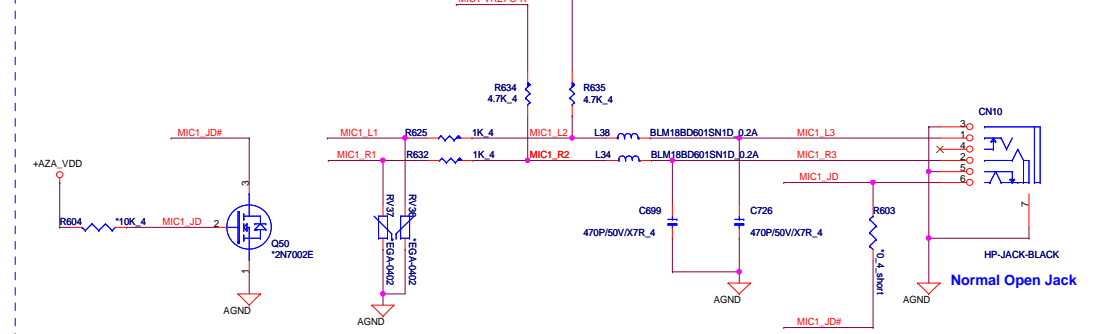
## Earphone(AMP)



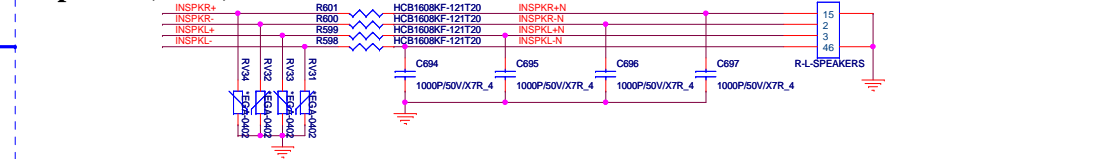
## HDA Power(ADO)



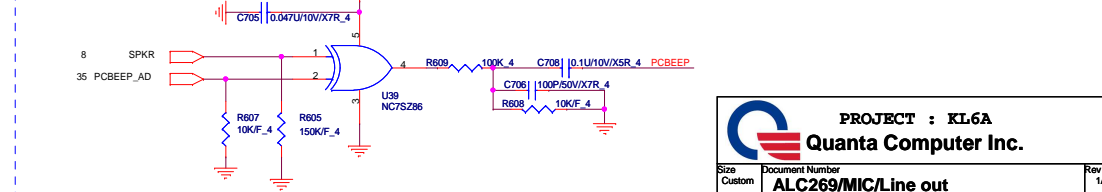
## System MIC(AMP)



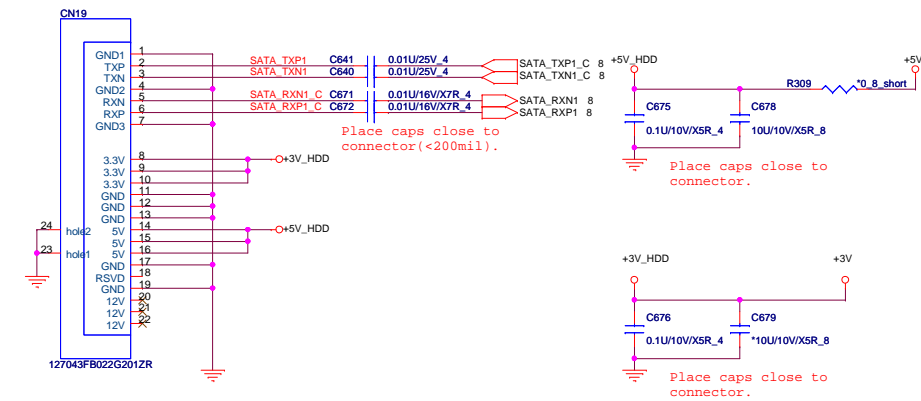
## Speaker(AMP)



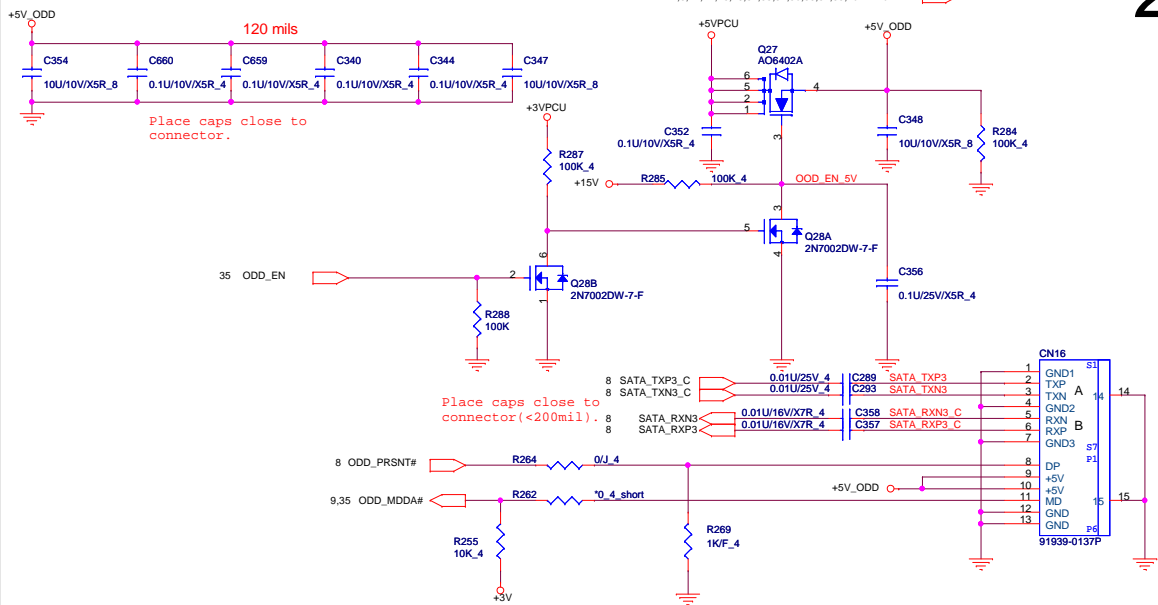
## PC BEEP



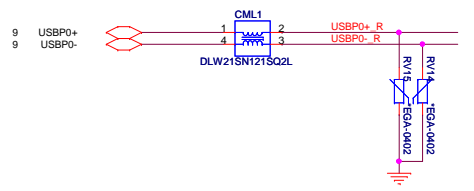
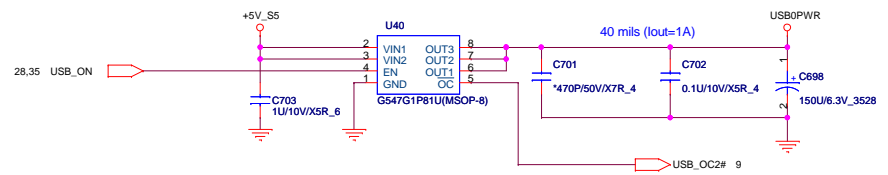
SATA HDD Connector.



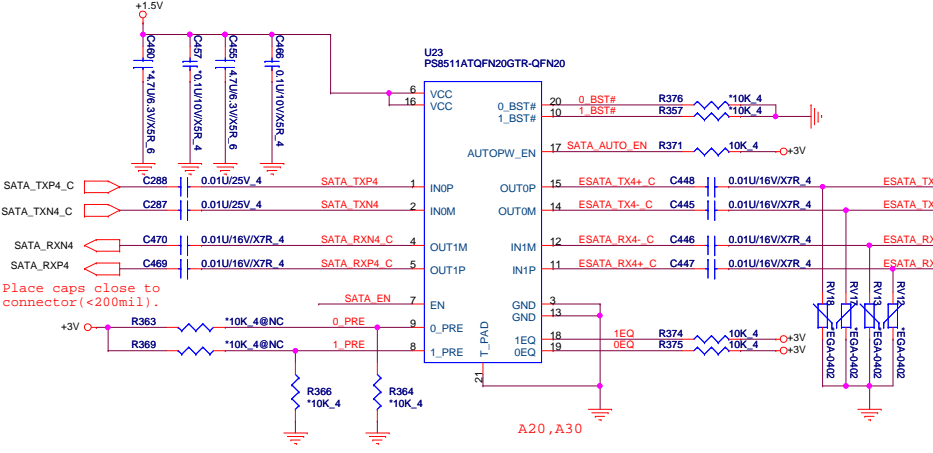
SATA ODD Connector.



USB + E-SATA



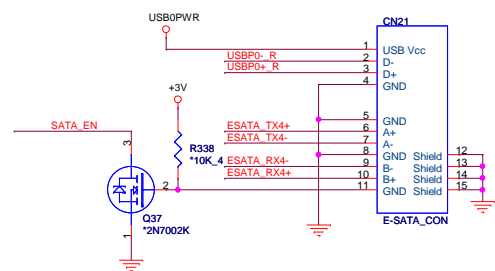
E-SATA RE-DRIVER



All straps of PS8511A have int. PL 150Kohm.

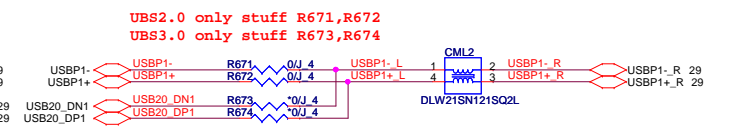
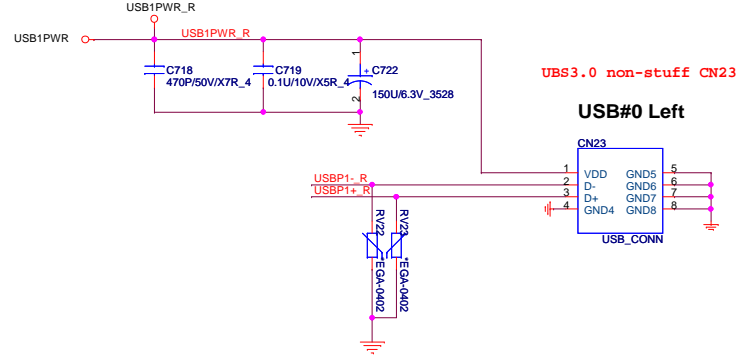
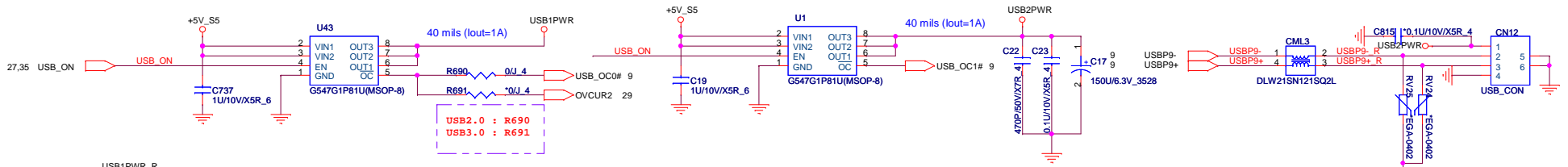
EN	AUTO_EN	0/1EQ	0/1EQ	0/1_BST#	0/1_BST#	0/1_PRE	0/1_PRE	Function
0	X	X	X	X	X	X	X	Standby
1	0	X	X	X	X	X	X	disable auto power saving
1	1	X	X	X	X	X	X	enable auto power saving
1	X	0	X	X	X	X	X	Short and medium length
1	X	X	1	X	X	X	X	Long length
1	X	X	X	0	X	X	X	Output :800~1200 mVpp
1	X	X	X	X	1	X	X	Output :400~700 mVpp
1	X	X	X	X	X	0	X	Pre-emphasis disabled
1	X	X	X	X	X	X	1	Pre-emphasis enabled

USB 0



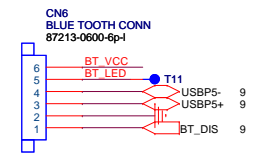
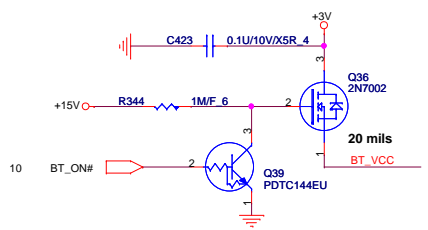
USB2.0\*3

USB#1 Daughter board

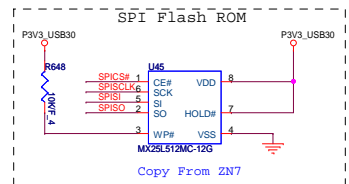
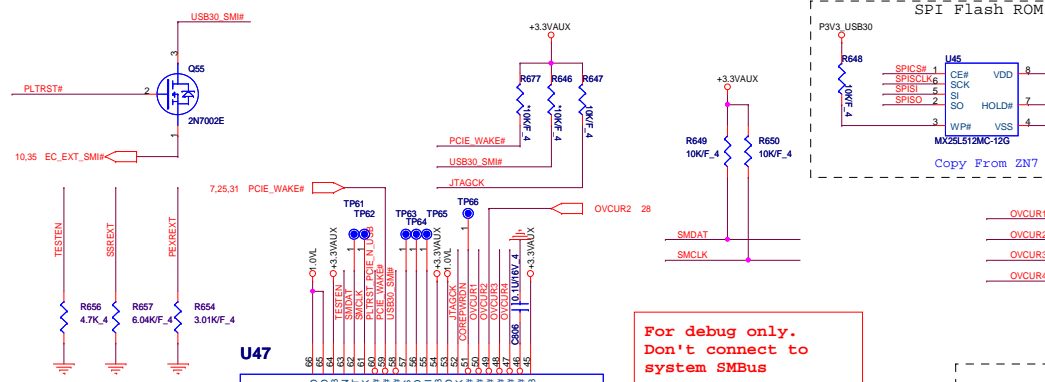


USB2.0 only stuff R671,R672  
 USB3.0 only stuff R673,R674

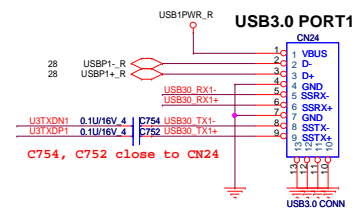
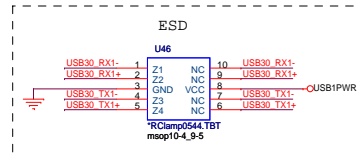
BLUETOOTH



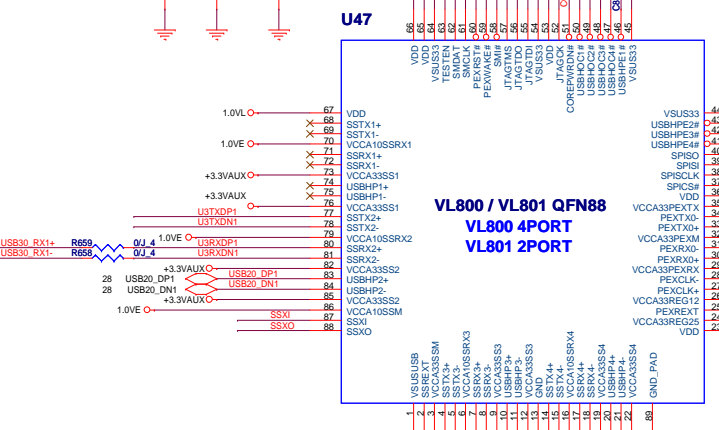
REAR USB PORT X1



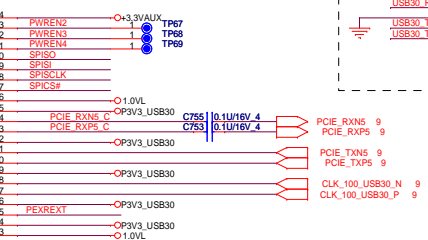
For debug only.  
Don't connect to  
system SMBus



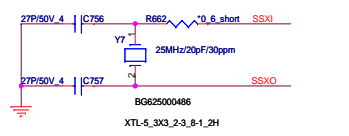
SUY USB3.0: DFHS09FR063



Near PCIe Slot

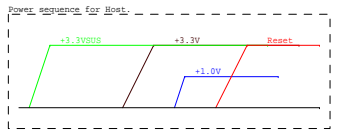
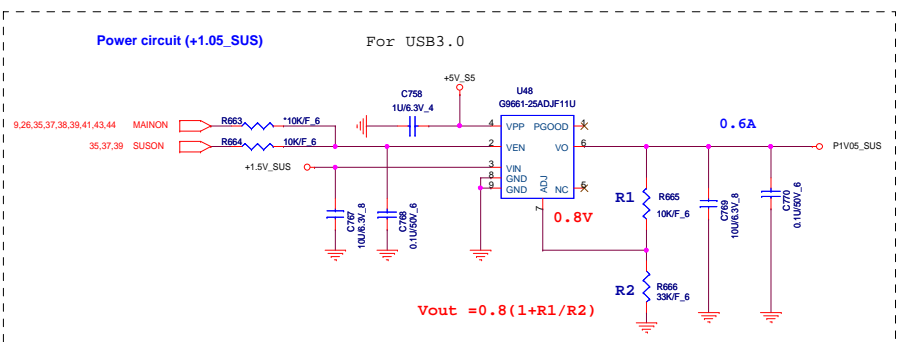
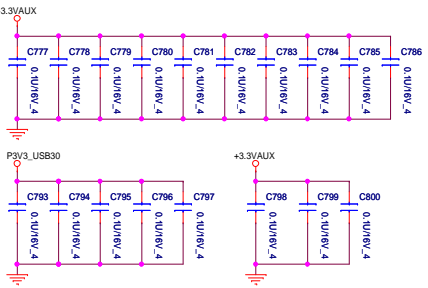
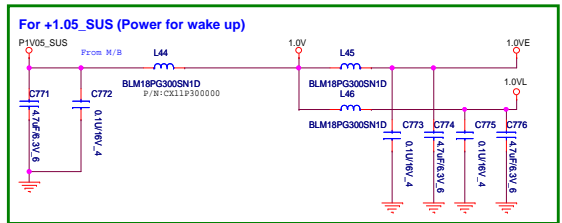
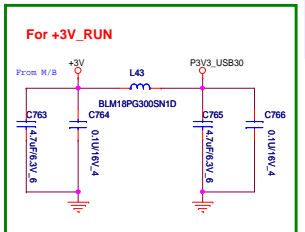
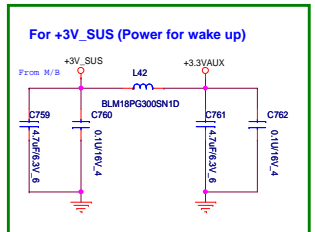
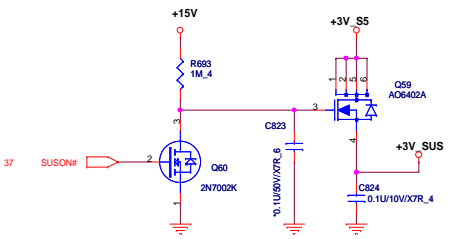
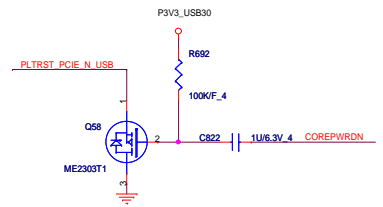


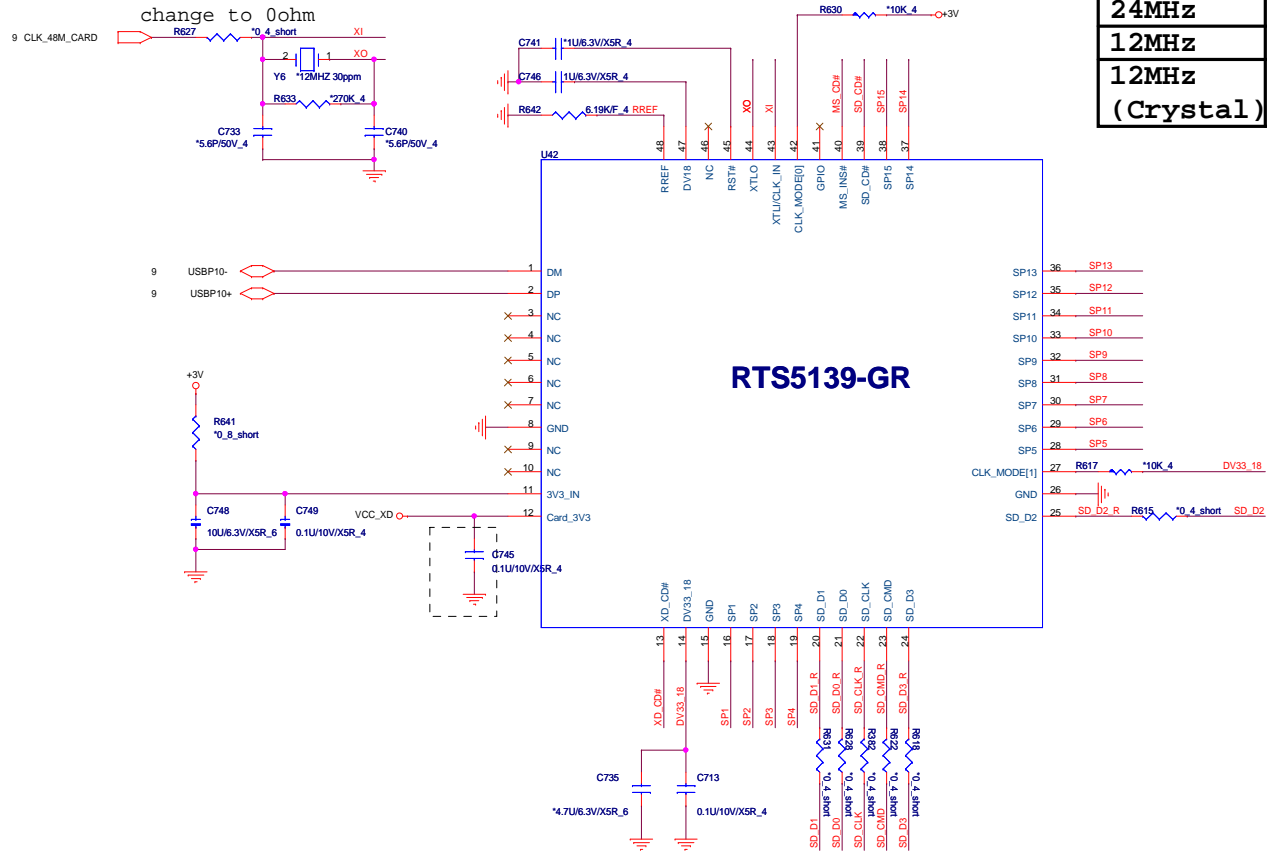
X'tal 25MHz



Crystal foot print must be reserved  
in case 25MHz clock from clock  
generator is not stable enough.

For USB3.0  
Remove SUSD turn on switch (From PCU to SUS)  
(Used +3V\_S5 power plane)



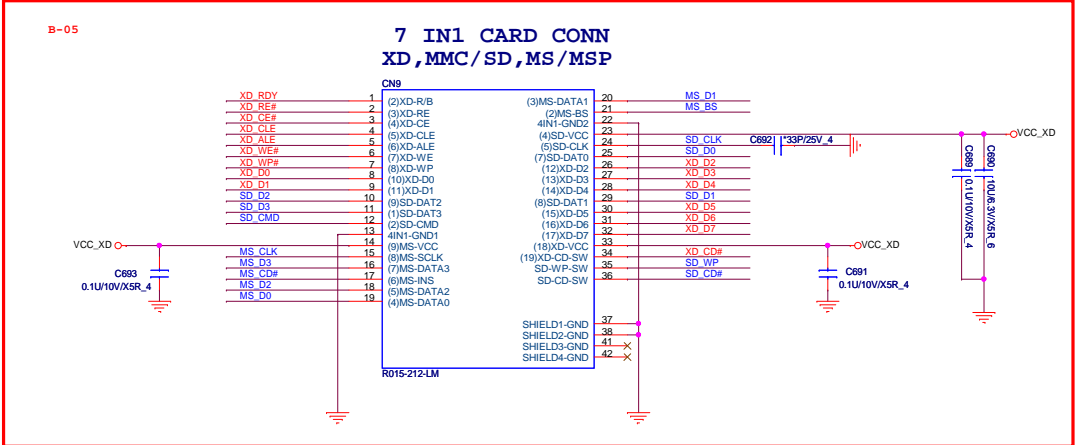


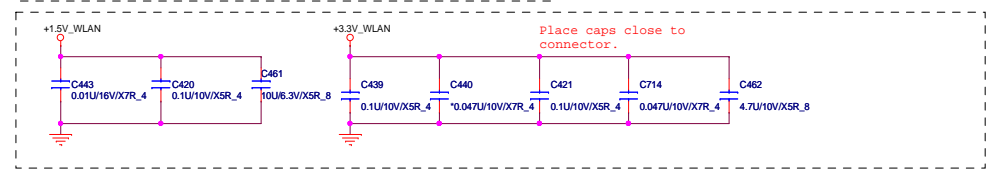
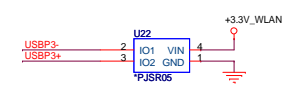
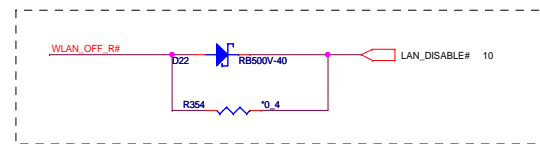
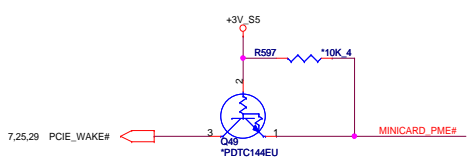
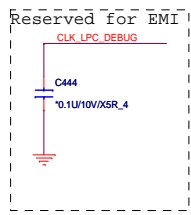
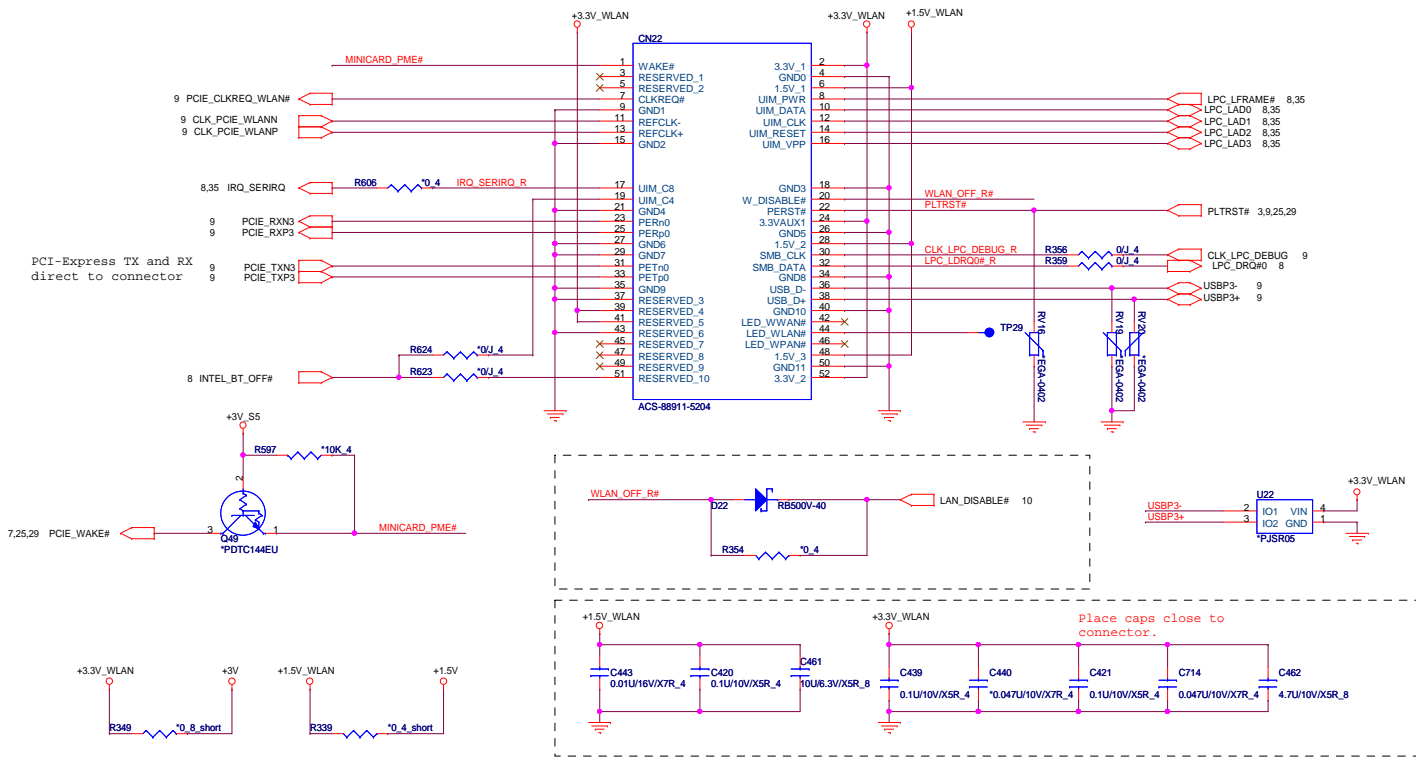
Clock Mode strap	R9287	R9307
48MHz	X	X
24MHz	X	O
12MHz	O	X
12MHz (Crystal)	O	O

**Note:**

SD/MMC	MS	XD
SP1	SD D7	XD RDY
SP2	SD D6	XD KE#
SP3	SD D5	XD CE#
SP4	SD D4	XD WE#
SP5	MS BS	XD CLE
SP6	MS D5	XD ALE
SP7	MS D1	XD WP#
SP8	MS D4	XD D0
SP9	MS D0	XD D1
SP10	MS D2	XD D2
SP11	MS D6	XD D3
SP12	MS D3	XD D4
SP13	MS D7	XD D5
SP14	MS CLK	XD D6
SP15	SD_WP	XD D7

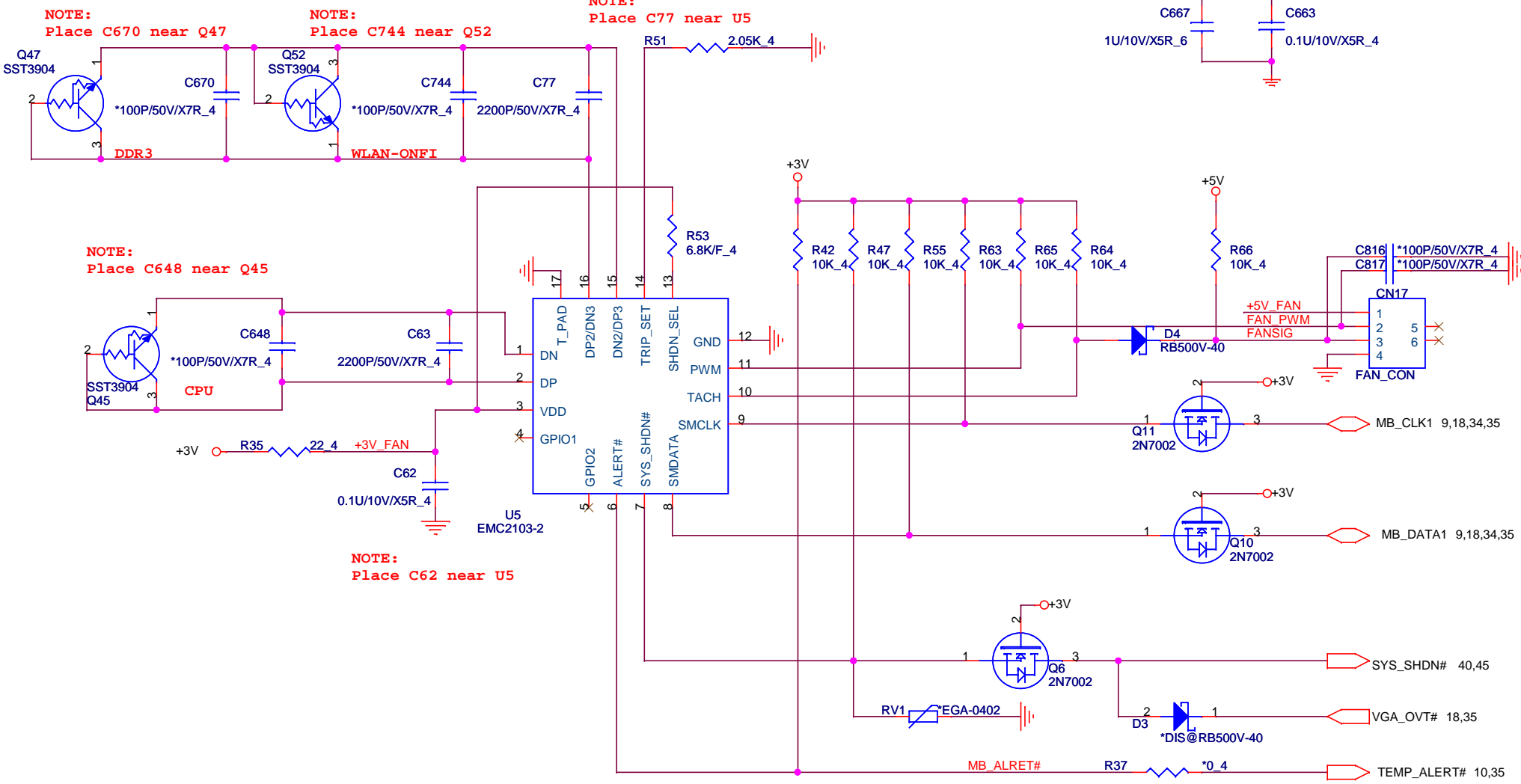
For RTS5139  
SD,MS 4bit only





# FAN CONTROL

7,8,9,10,11,13,14,15,22,23,24,25,26,27,28,29,30,31,34,35,36,37,38,42,43,44,45  
 +3V  
 7,8,11,22,23,26,27,33,34,35,36,37,38,45  
 +5V

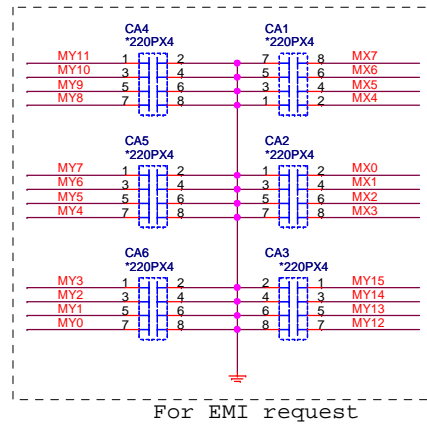
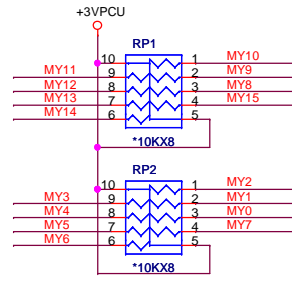
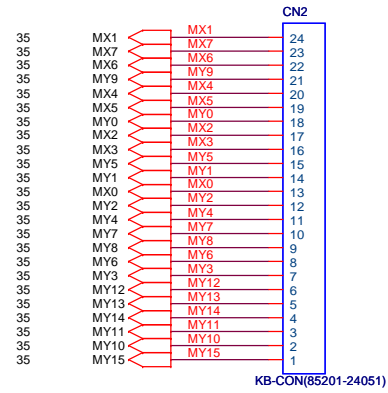


		<b>PROJECT : KL6A</b>	
		<b>Quanta Computer Inc.</b>	
Size Custom	Document Number <b>FAN /THERMAL</b>	Rev 1A	
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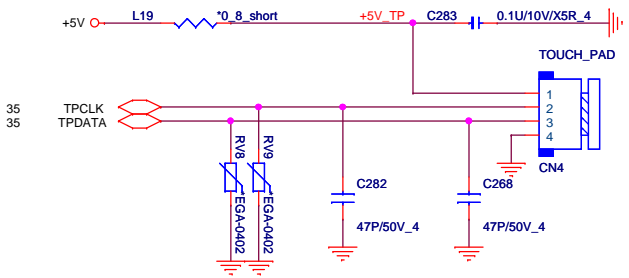


# KEYBOARD

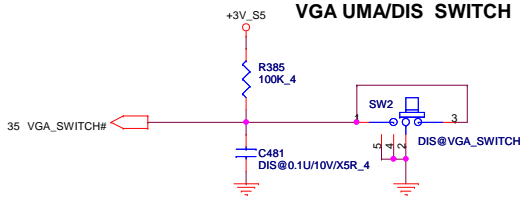
7,8,11,22,23,26,27,32,34,35,36,37,38,45 +5V  
7,8,24,25,27,34,35,37,38,40,41 +3VPCU



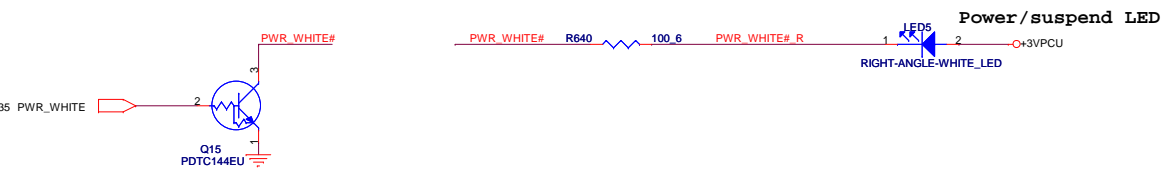
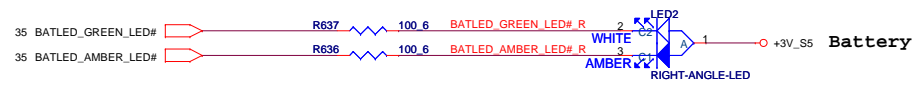
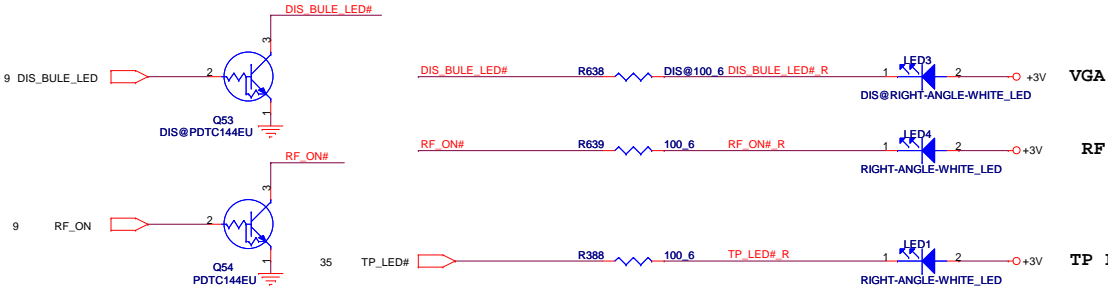
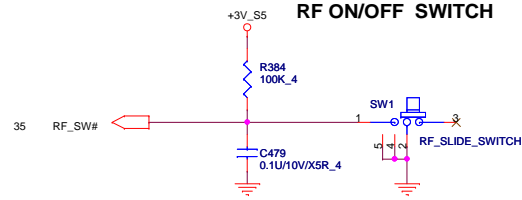
# Touch pad



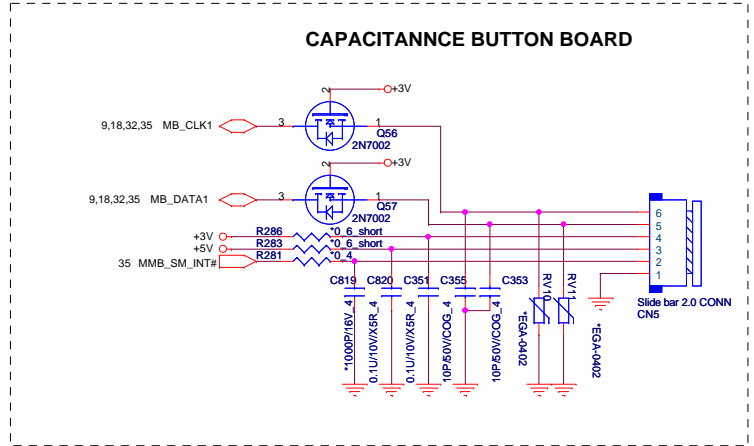
VGA UMA/DIS SWITCH



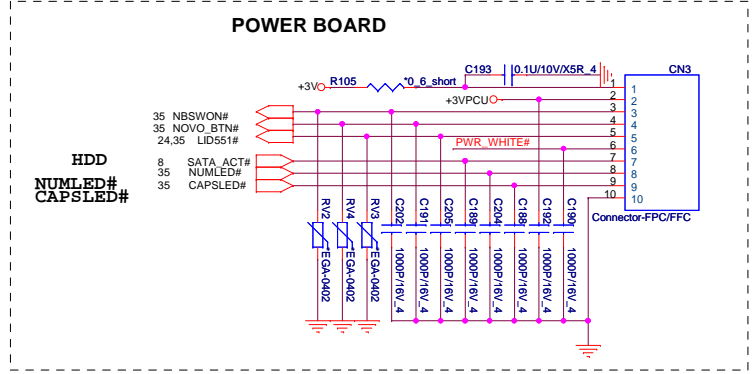
RF ON/OFF SWITCH



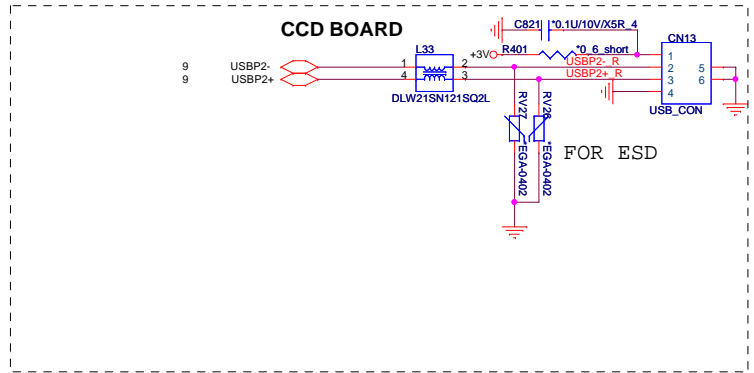
CAPACITANCE BUTTON BOARD

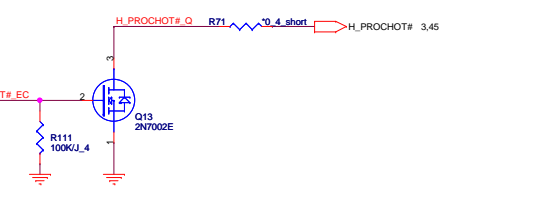
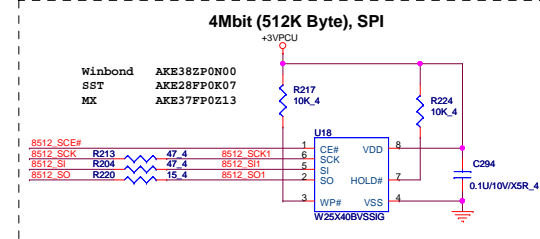
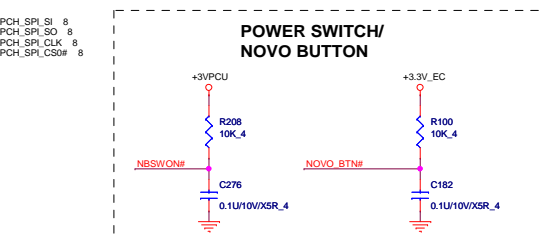
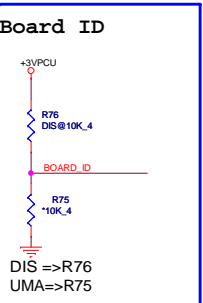
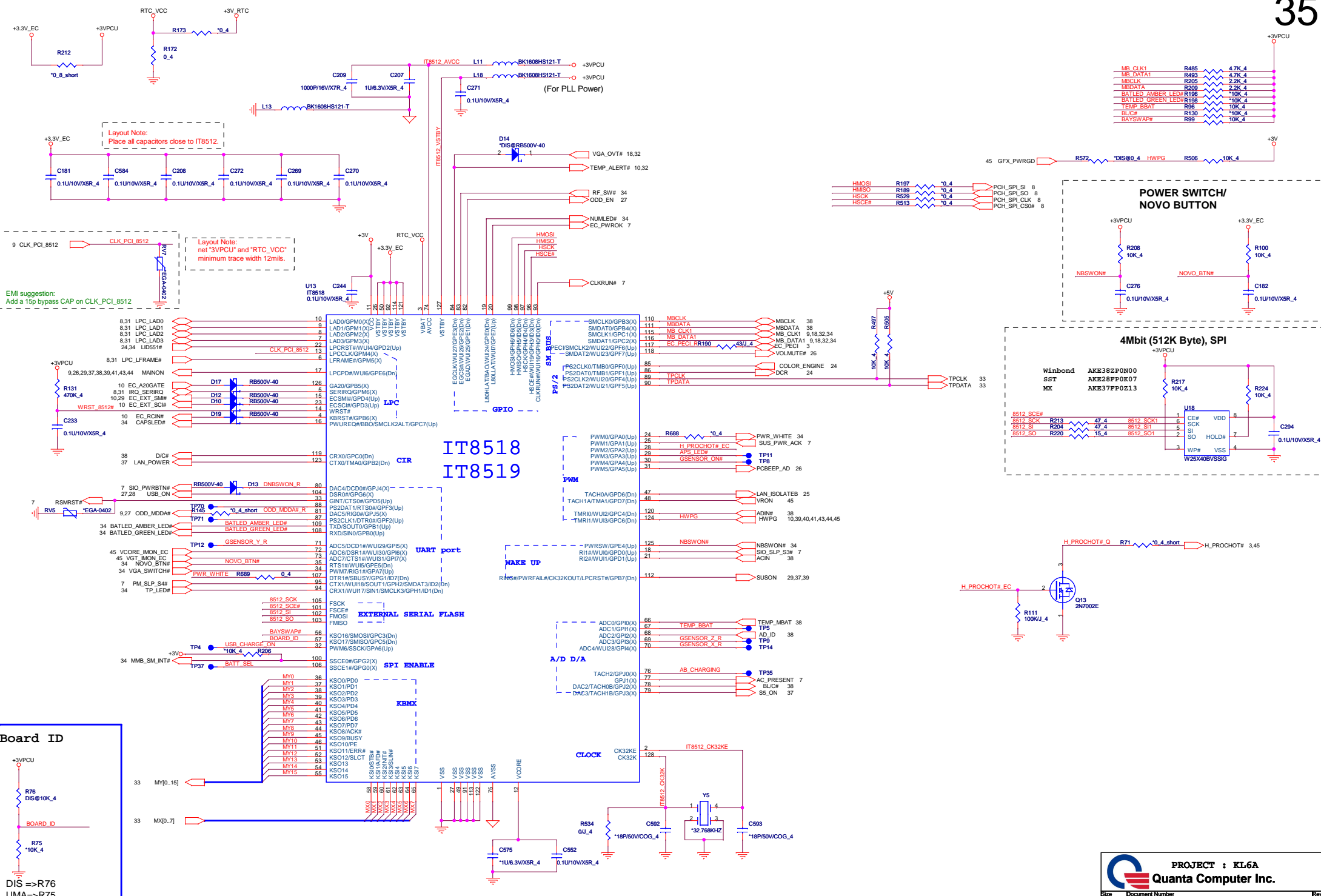


POWER BOARD



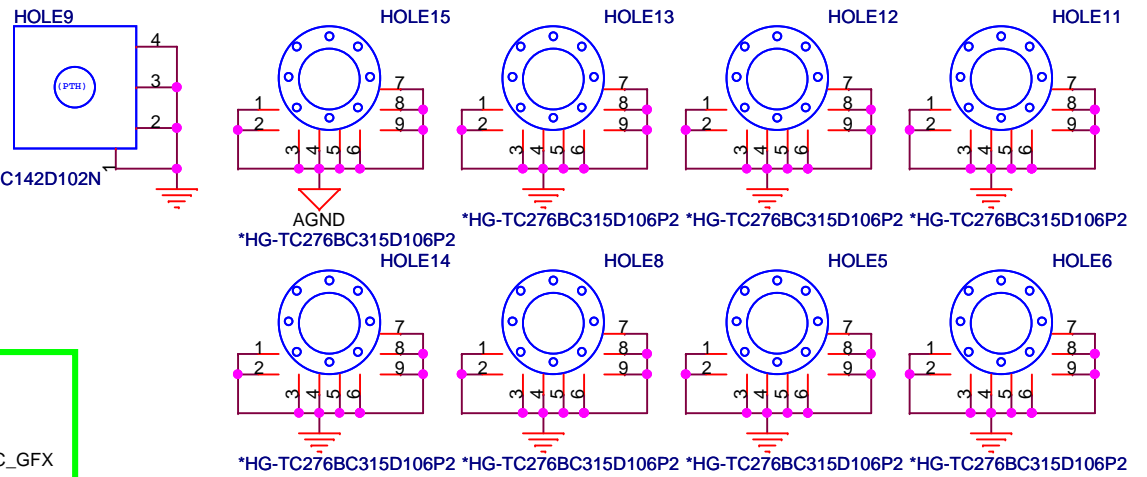
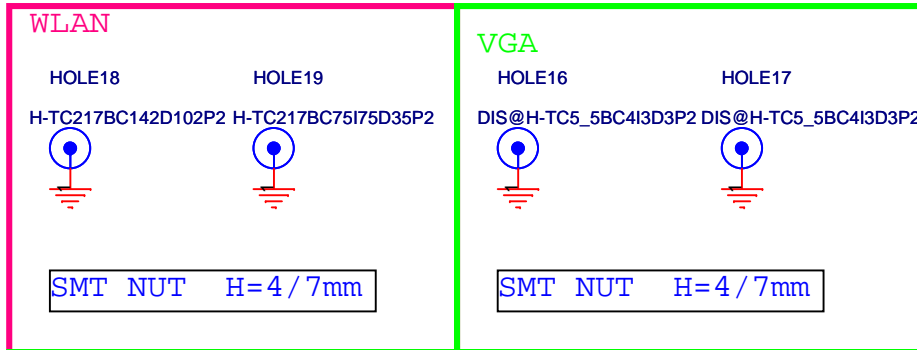
CCD BOARD



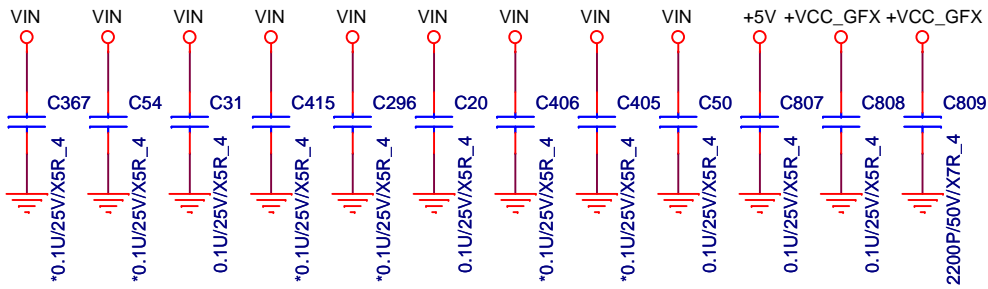


## Screw for ME

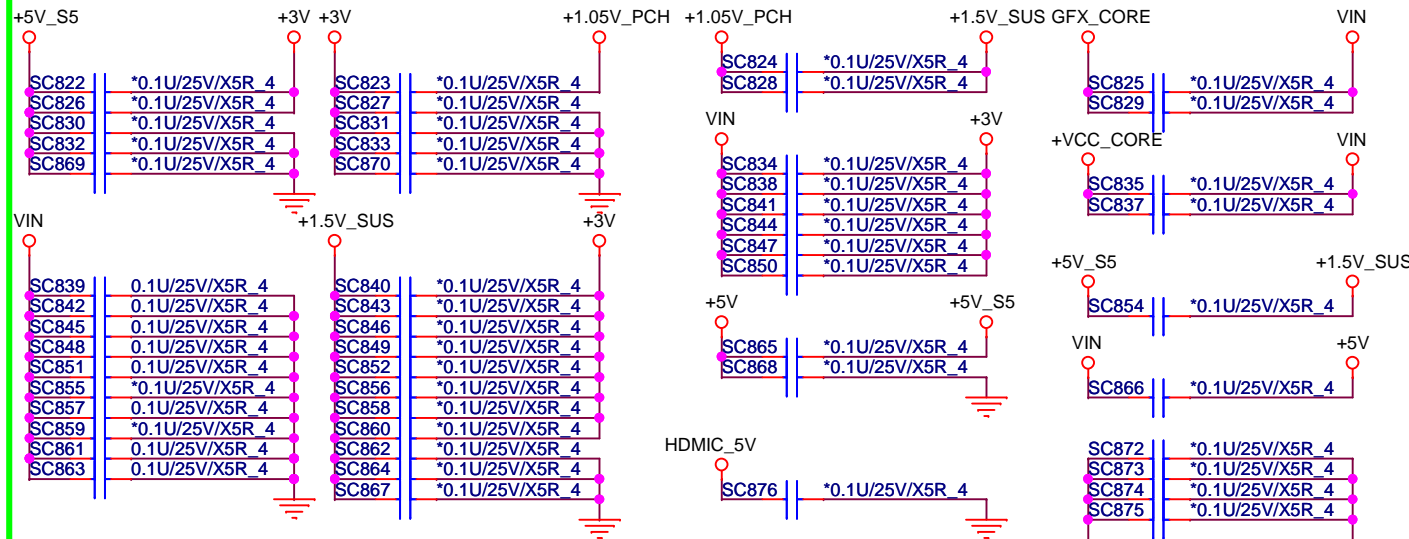
## CPU BKT



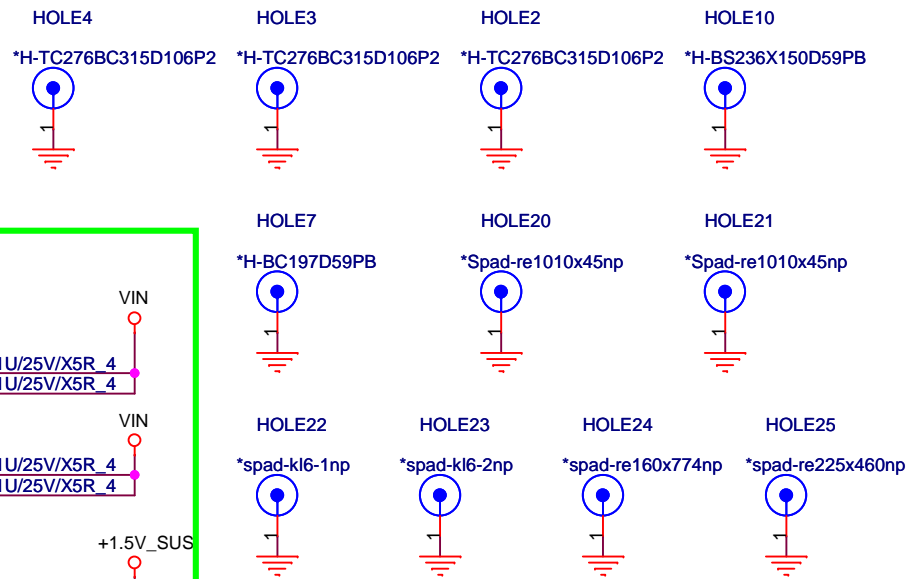
## EMI suggestion



## B-08



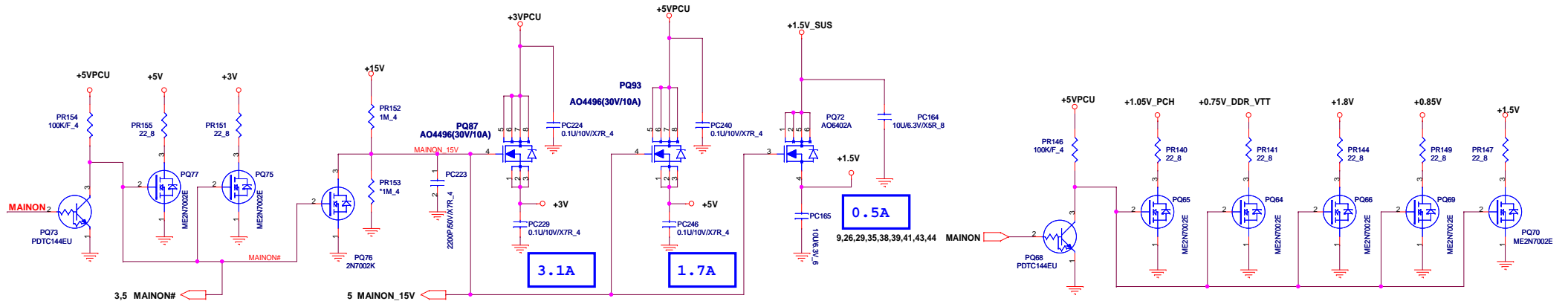
## ESD suggestion



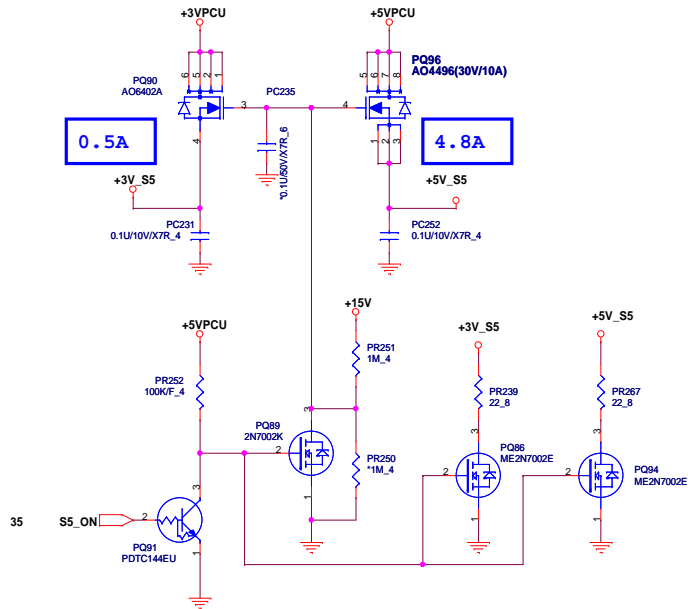
**PROJECT : KL6A**

**Quanta Computer Inc.**

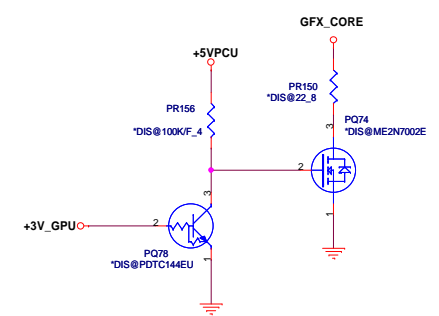
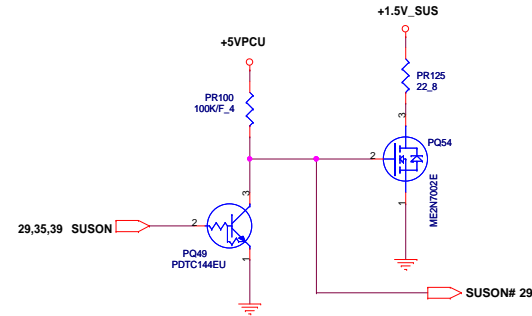
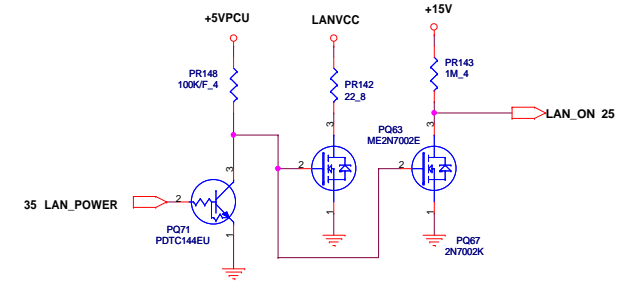
+3V, +5V, +1.5V

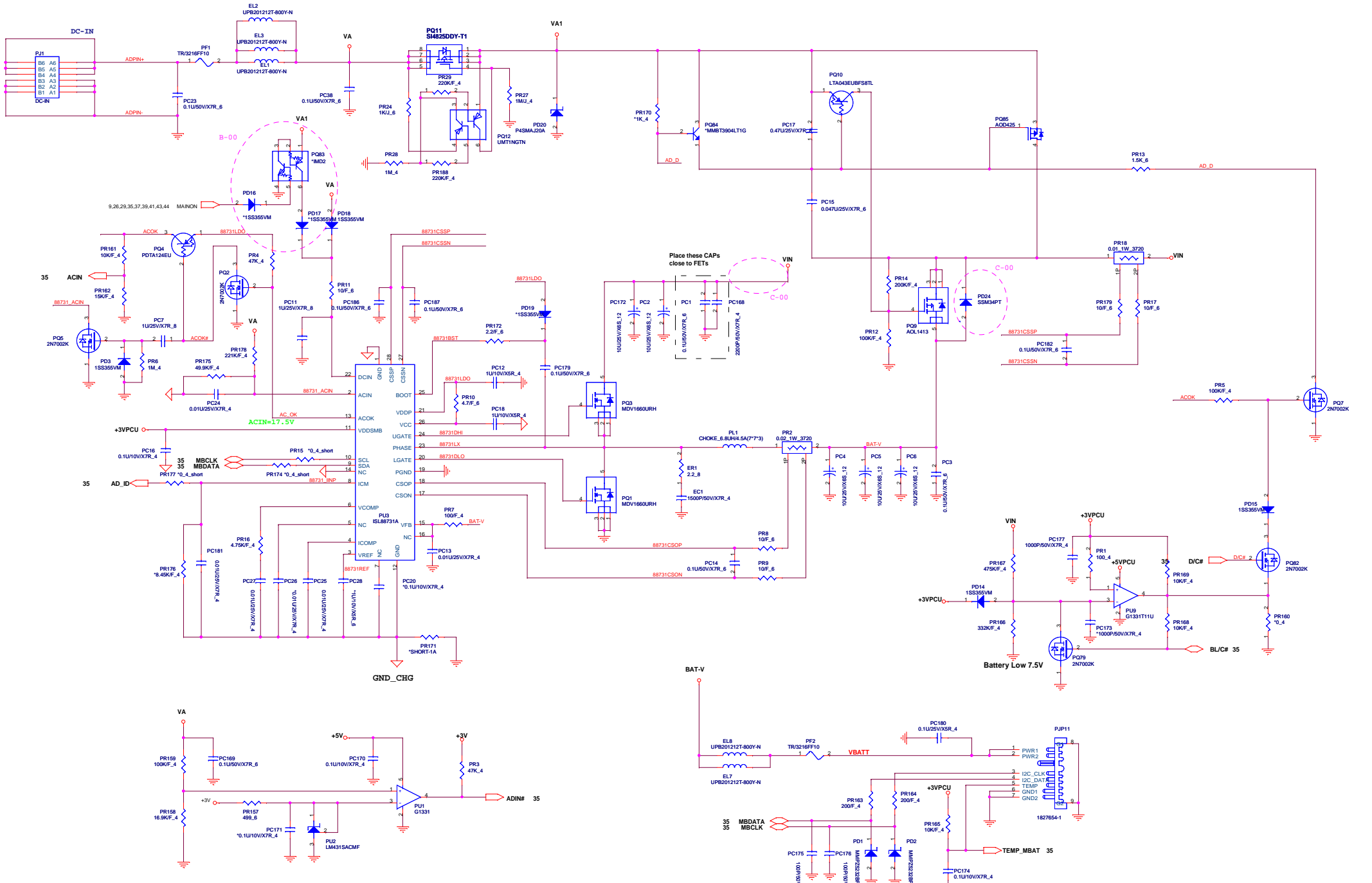


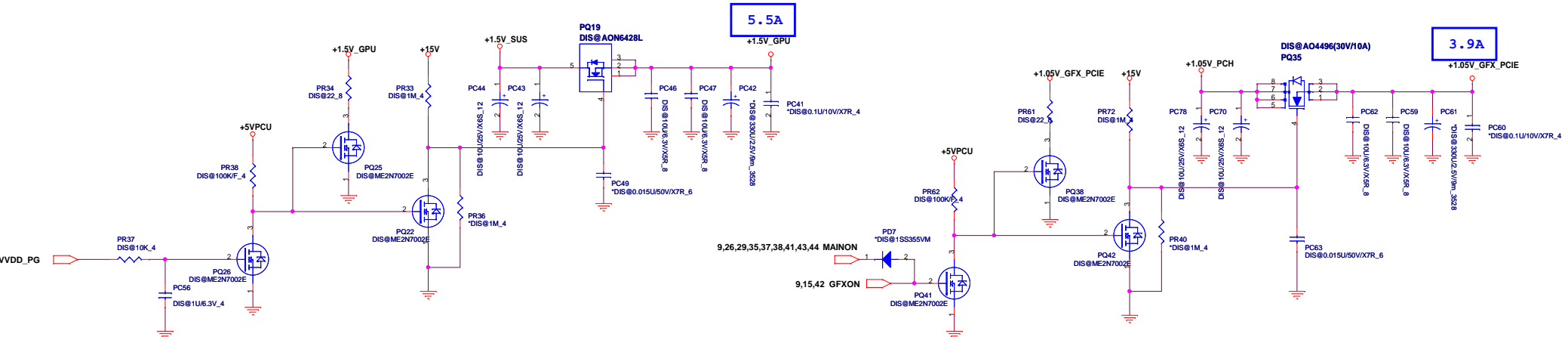
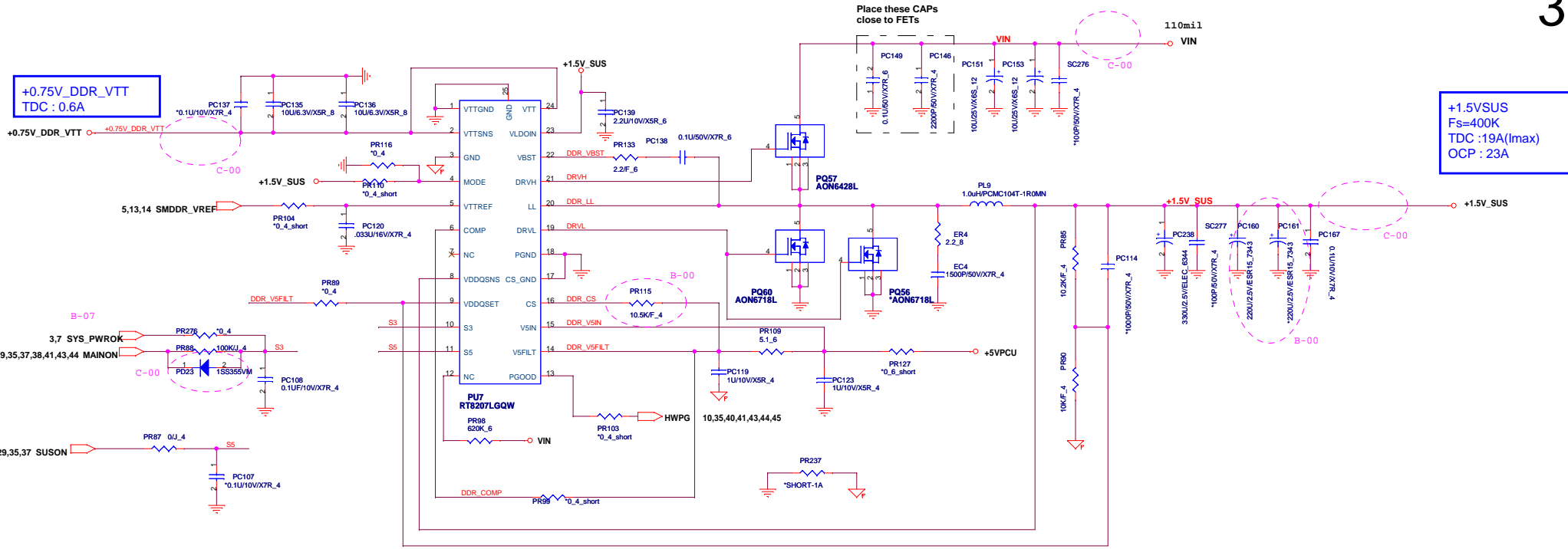
3V\_S5, 5V\_S5



LANVCC

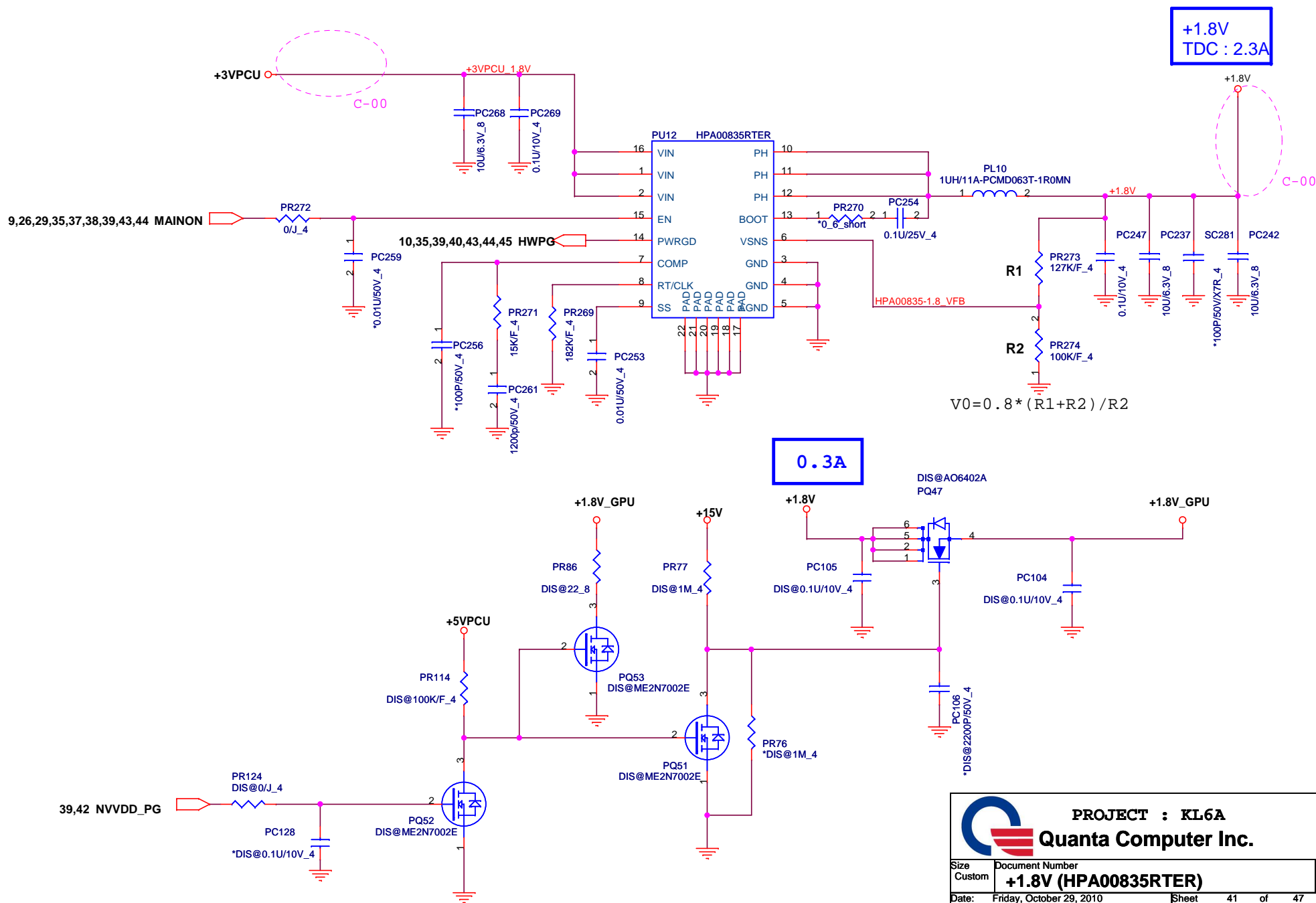


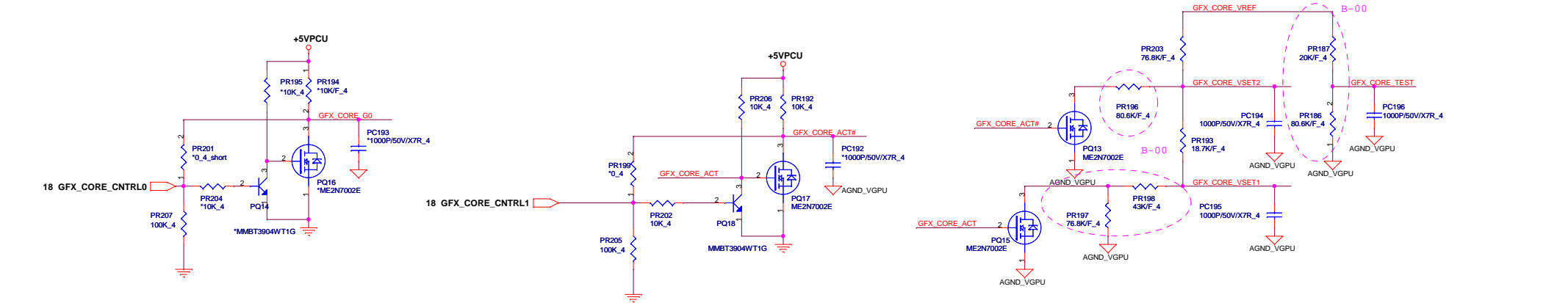
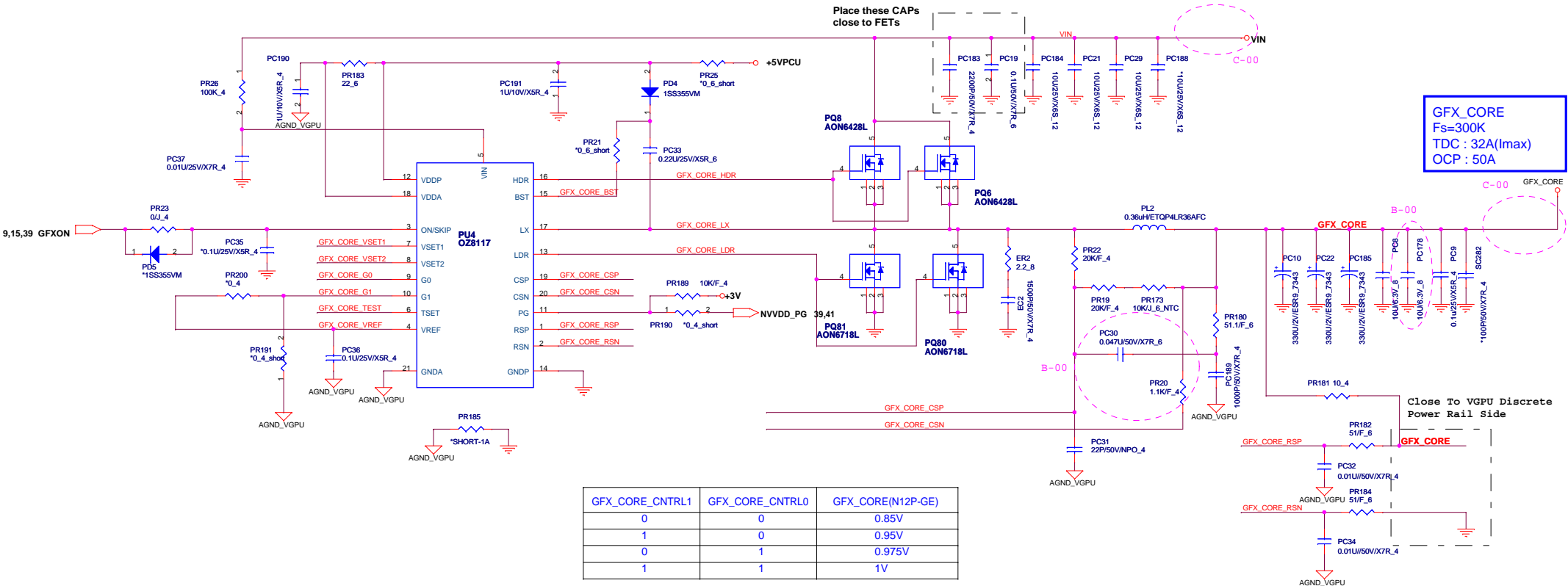


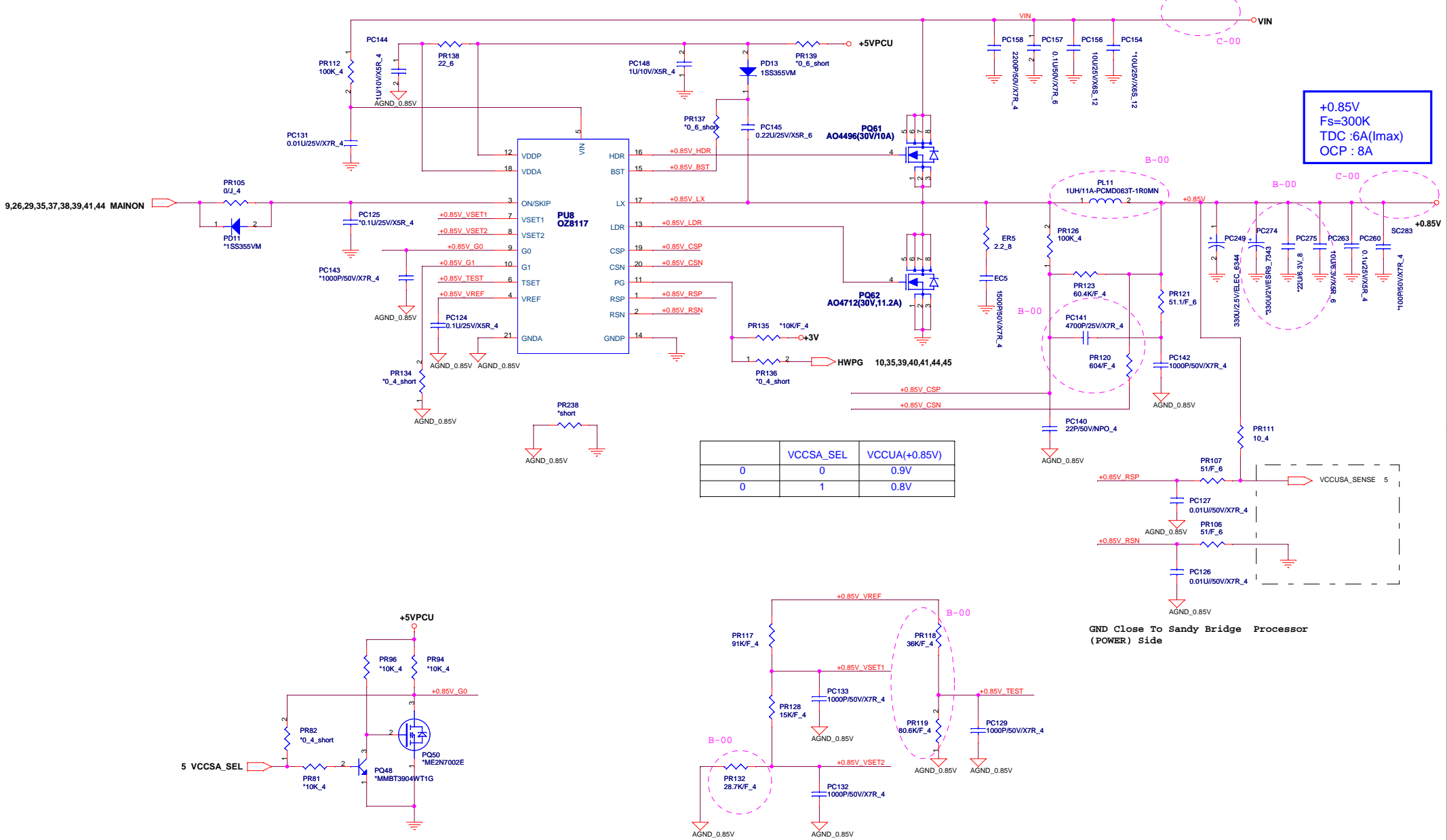








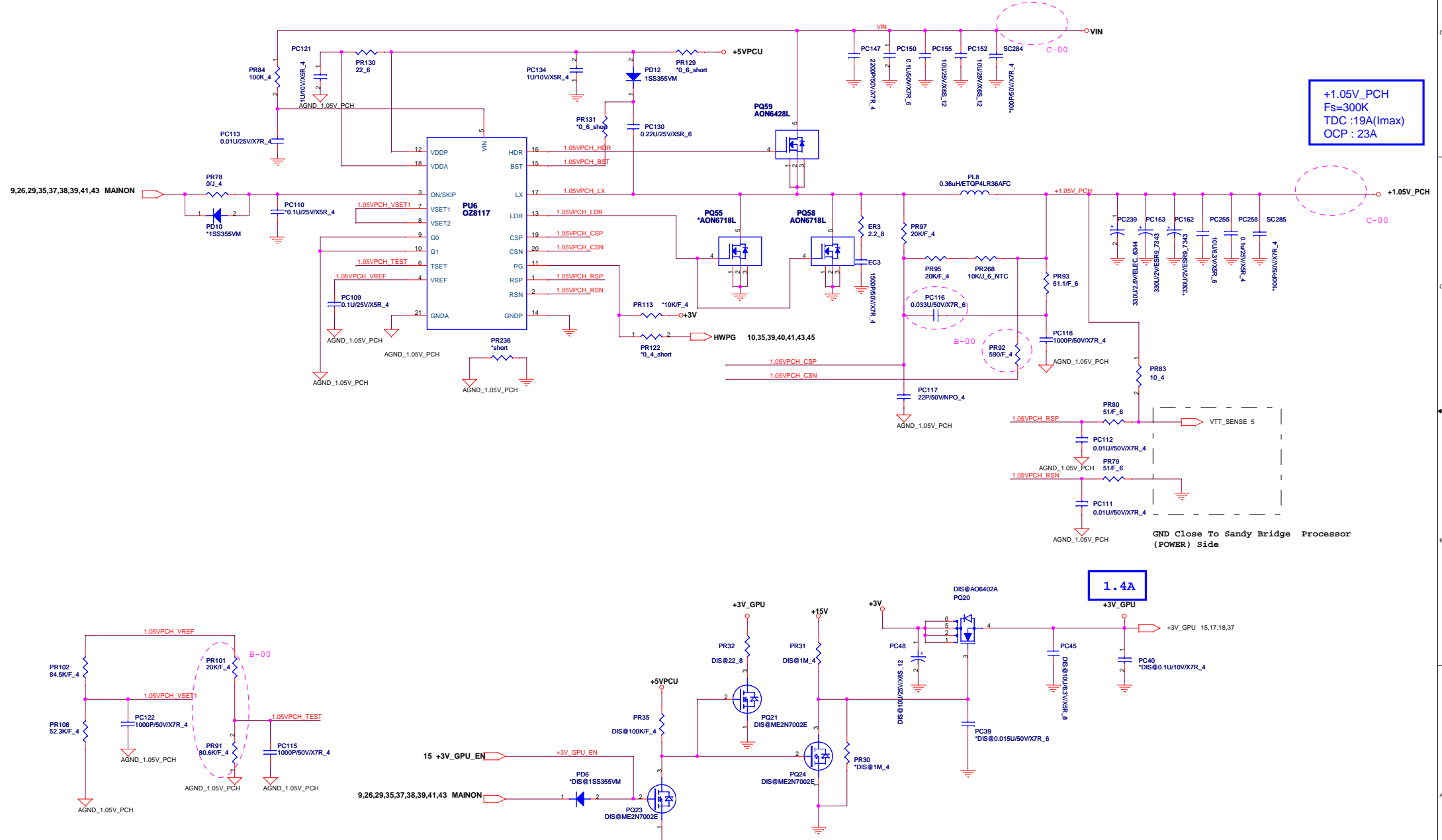




+0.85V  
Fs=300K  
TDC :6A(Imax)  
OCP : 8A

	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V

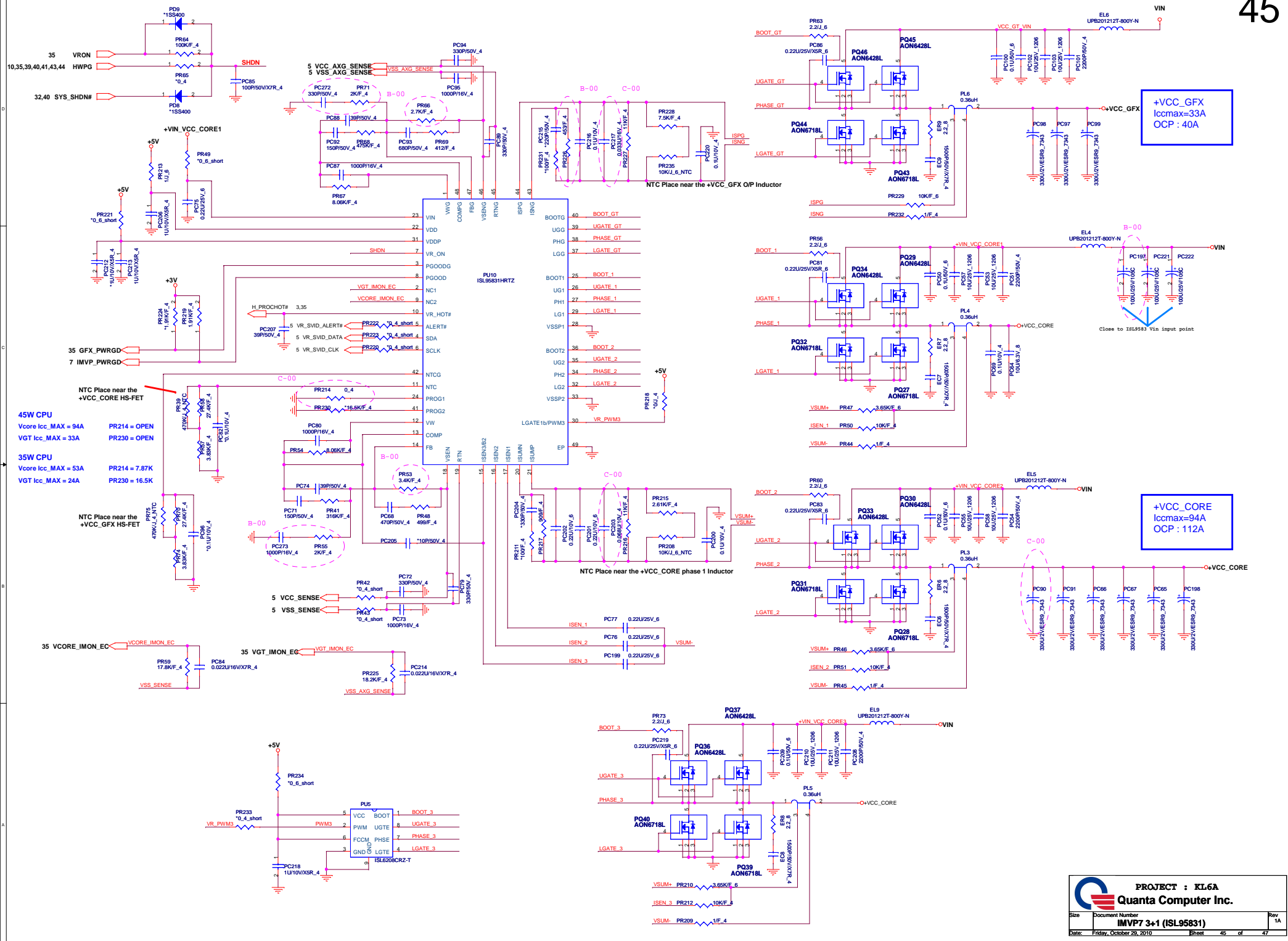
GND Close To Sandy Bridge Processor (POWER) Side



+1.05V\_PCH  
 Fs=300K  
 TDC :19A(I<sub>max</sub>)  
 OCP : 23A

1.4A

GND Close To Sandy Bridge Processor (POWER) side



35 VRON  
10,35,39,40,41,43,44 HWPG  
32,40 SYS\_SHDN#

+VIN VCC\_CORE1  
+5V  
PR221 0.6\_short  
PR222 0.4\_short  
PR223 0.4\_short

35 GFX\_PWRGD  
7 IMVP\_PWRGD

45W CPU  
Vcore lcc\_MAX = 94A  
VGT lcc\_MAX = 33A  
PR214 = OPEN  
PR230 = OPEN

35W CPU  
Vcore lcc\_MAX = 53A  
VGT lcc\_MAX = 24A  
PR214 = 7.87K  
PR230 = 16.5K

NTC Place near the +VCC\_CORE HS-FET  
PR214 0.4  
PR230 16.8K

NTC Place near the +VCC\_GFX HS-FET  
PR214 7.87K  
PR230 16.5K

5 VCC\_SENSE  
5 VSS\_SENSE

35 VCORE\_IMON\_EC  
35 VGT\_IMON\_EC

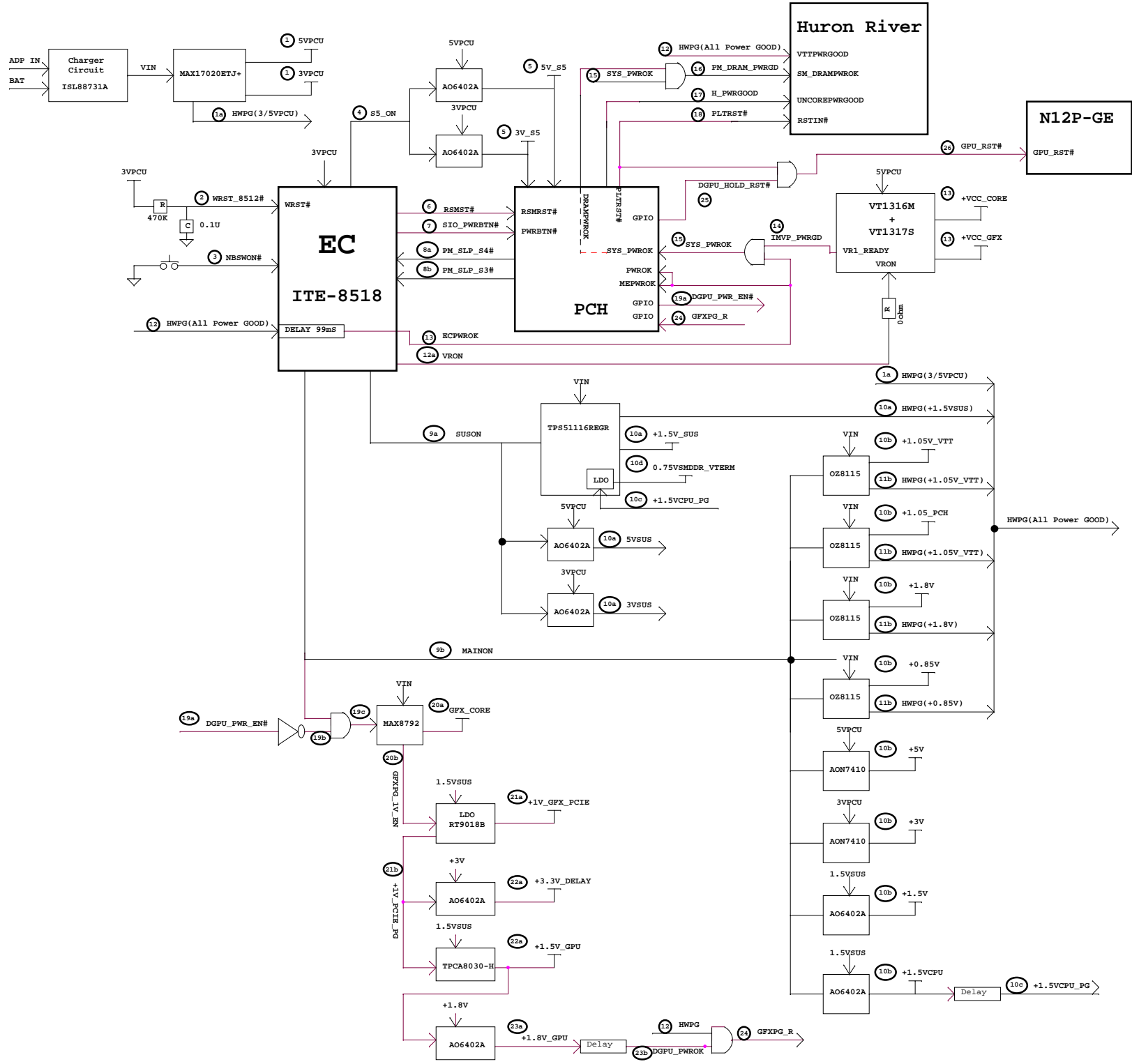
PR225 18.2K  
PR224 0.6\_short

VR\_PWM3  
PR233 0.4\_short

ISL95831HRTZ  
VCC BOOT  
PWM UGATE  
FCCM PHSE  
GND LGATE

+VCC\_GFX  
lccmax=33A  
OCP : 40A

+VCC\_CORE  
lccmax=94A  
OCP : 112A





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