

# P407-A00: G84M/86M MXM V1.3

256/512MB 128-BIT GDDR2

LVDS, DVI -A, DVI -B, TV-OUT, VGA, HDMI

SLI, HDCP SUPPORT

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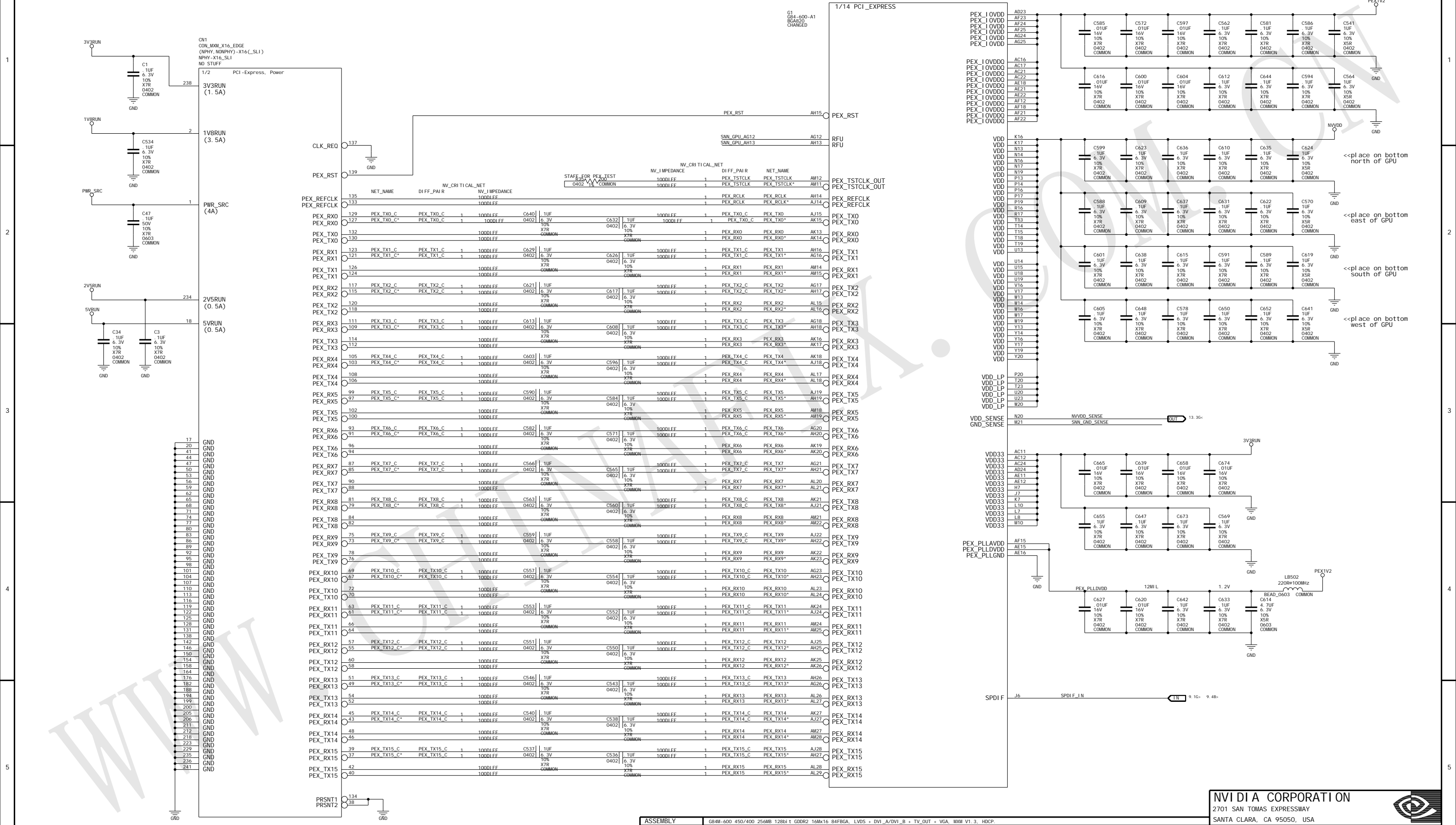
SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10407-9998-300	BASE LEVEL, GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKU0001	600-10407-0001-300	G84M-600 450/400 256MB 128bit 1 GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
2	SKU0002	600-10407-0002-300	G84M-600 450/400 512MB 128bit 1 GDDR2 32Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
3	SKU0003	600-10407-0003-300	G84M-700 500/400 512MB 128bit 1 GDDR2 32Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
4	SKU0003	600-10407-0004-300	G84M-770 500/400 256MB 128bit 1 GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
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6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

### P407\_A03 change list:

- 1) P407\_A03 is modified from P555\_A00 to insure they are exactly same, except 2 mounting holes and 4 thermal hole
- 2) Change mounting holes and thermal holes from MXM V2.0 to MXM V1.3

ASSEMBLY	G84M-600 450/400 256MB 128bit 1 GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	Cover Page

<b>NVIDIA CORPORATION</b>			
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NV_PN	600-10407-0001-300 A		
ID	p407_a03	PAGE	1 OF 18
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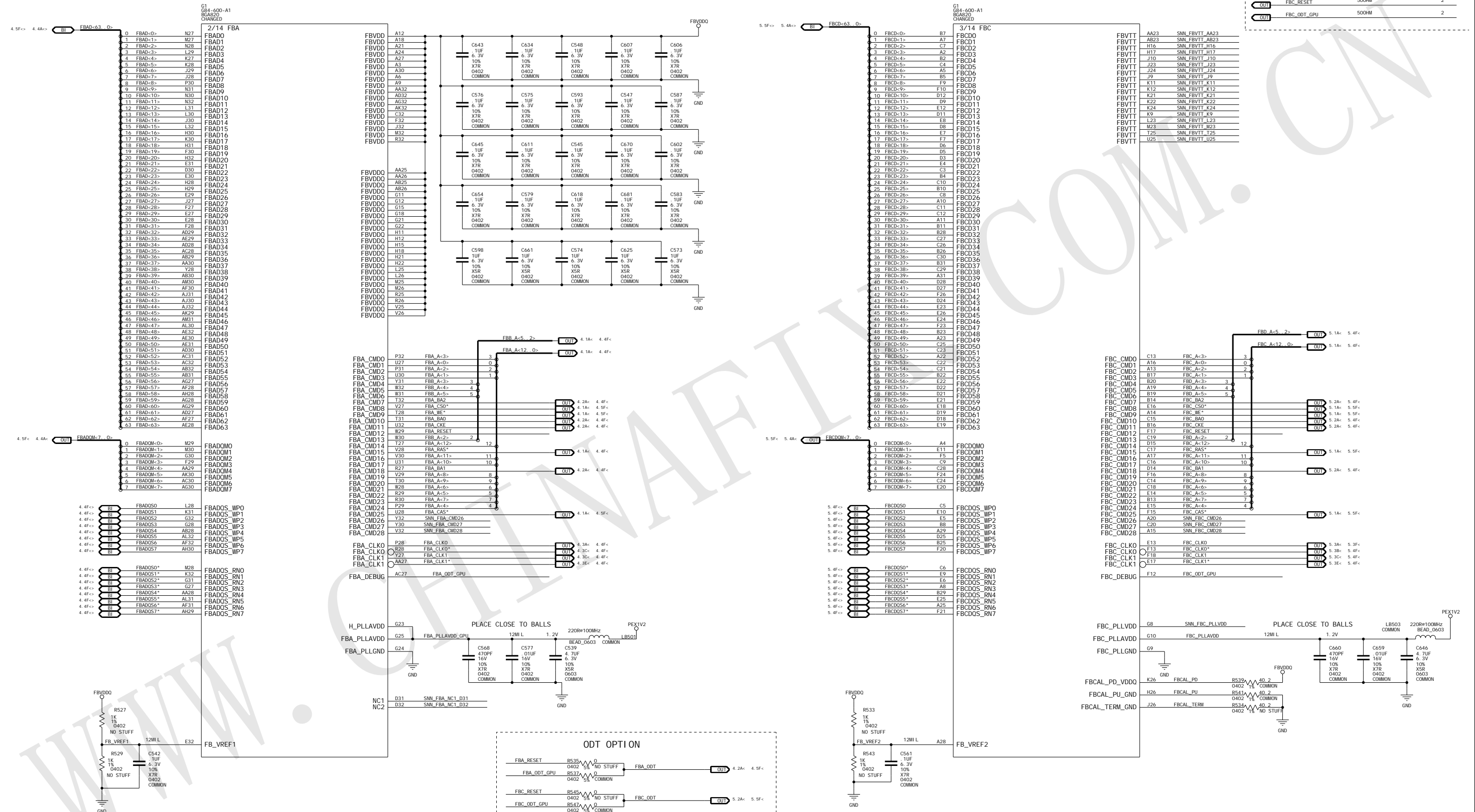
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ASSEMBLY PAGE DETAIL: GB4M-600 450/400 256MB 128bit 1 GDDR2 16Mx16 84FBGA, LVDS + DVI\_A/DVI\_B + TV\_OUT + VGA, MXM V1.3, HDCP, PCI EXPRESS Interface

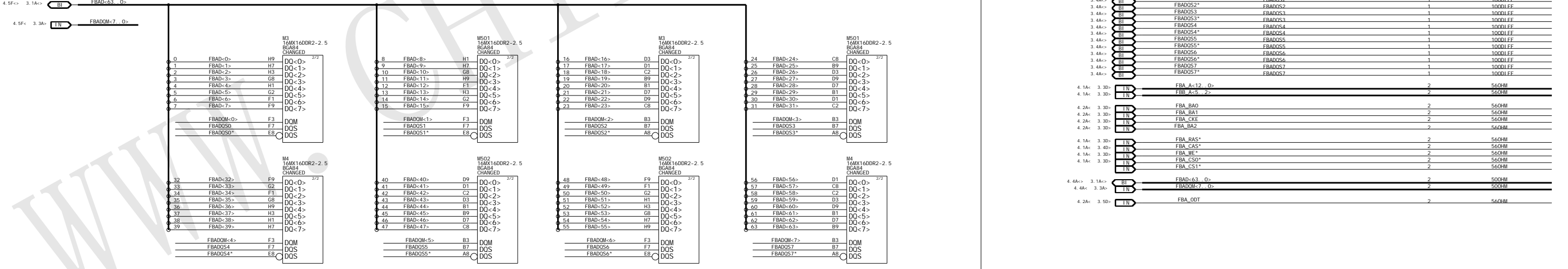
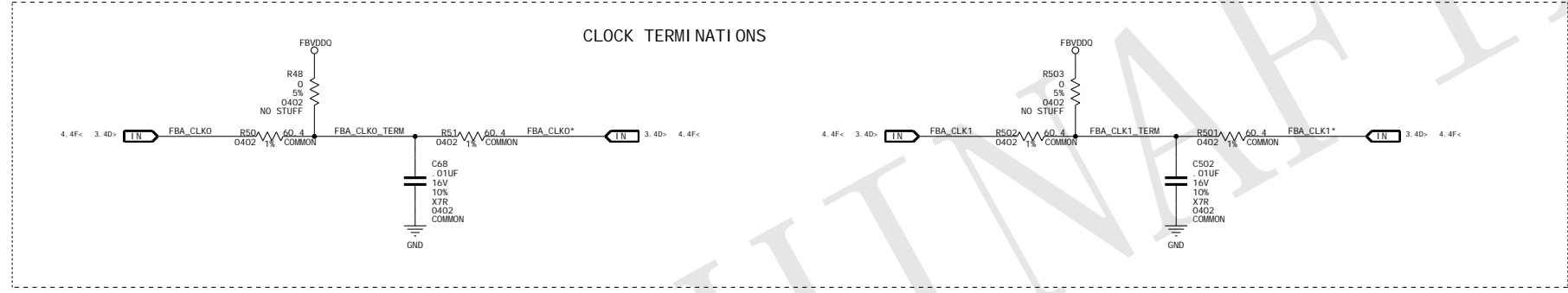
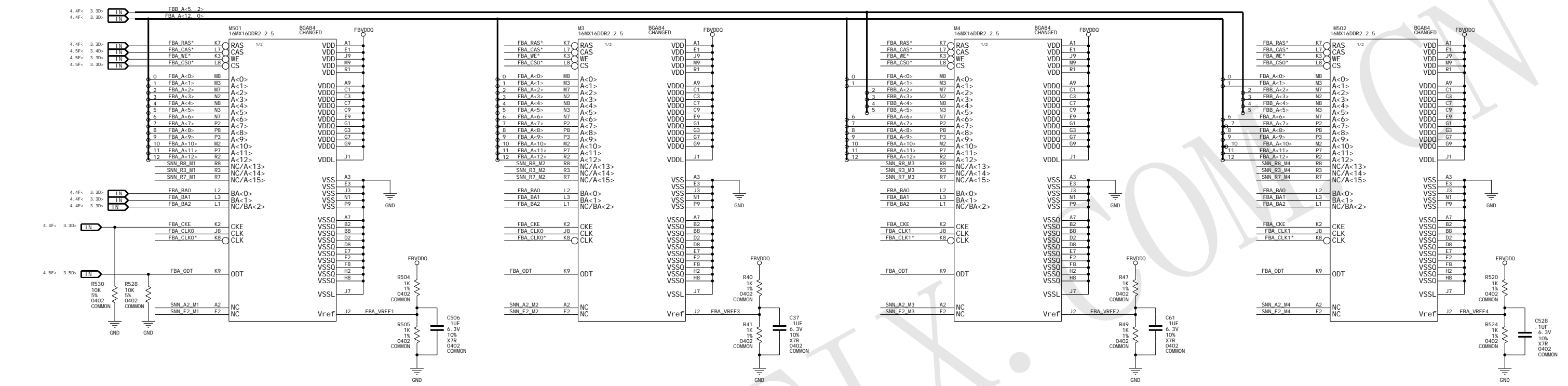
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NET	NV_I_MPDANCE	NV_CRI_T1_CAL_NET
FBA_RESET	500HM	2
FBA_ODT_GPU	500HM	2
FBC_RESET	500HM	2
FBC_ODT_GPU	500HM	2



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NET	MIN_LI_NE_WI_DTH	VOLTAGE
FBA_VREF1	16MIL	0.9V
FBA_VREF2	16MIL	0.9V
FBA_VREF3	16MIL	0.9V
FBA_VREF4	16MIL	0.9V

NET	DIFFPAIR	CRITICAL	IMPEDANCE
FBA_CLK0	FBA_CLK0	1	100DIF
FBA_CLK1	FBA_CLK1	1	100DIF
FBA_CLK1*	FBA_CLK1	1	100DIF
FBADOS0	FBADOS0	1	100DIF
FBADOS1	FBADOS1	1	100DIF
FBADOS1*	FBADOS1	1	100DIF
FBADOS2	FBADOS2	1	100DIF
FBADOS2*	FBADOS2	1	100DIF
FBADOS3	FBADOS3	1	100DIF
FBADOS3*	FBADOS3	1	100DIF
FBADOS4	FBADOS4	1	100DIF
FBADOS4*	FBADOS4	1	100DIF
FBADOS5	FBADOS5	1	100DIF
FBADOS5*	FBADOS5	1	100DIF
FBADOS6	FBADOS6	1	100DIF
FBADOS6*	FBADOS6	1	100DIF
FBADOS7	FBADOS7	1	100DIF
FBADOS7*	FBADOS7	1	100DIF

4.1A< 3.30>	FBA A<12>_O<2>	2	50OHM
4.1A< 3.30>	FBA A<5>_O<2>	2	50OHM
4.2A< 3.30>	FBA_BA0	2	50OHM
4.2A< 3.30>	FBA_BA1	2	50OHM
4.2A< 3.30>	FBA_CKE	2	50OHM
4.2A< 3.30>	FBA_BA2	2	50OHM
4.1A< 3.30>	FBA_RAS*	2	50OHM
4.1A< 3.40>	FBA_CAS*	2	50OHM
4.1A< 3.30>	FBA_WE*	2	50OHM
4.1A< 3.30>	FBA_CS0*	2	50OHM
4.1A< 3.30>	FBA_CS1*	2	50OHM
4.4A< 3.1A<	FBAD<63>_O<2>	2	50OHM
4.4A< 3.3A<	FBADOM<7>_O<2>	2	50OHM
4.2A< 3.50>	FBA_ODT	2	50OHM

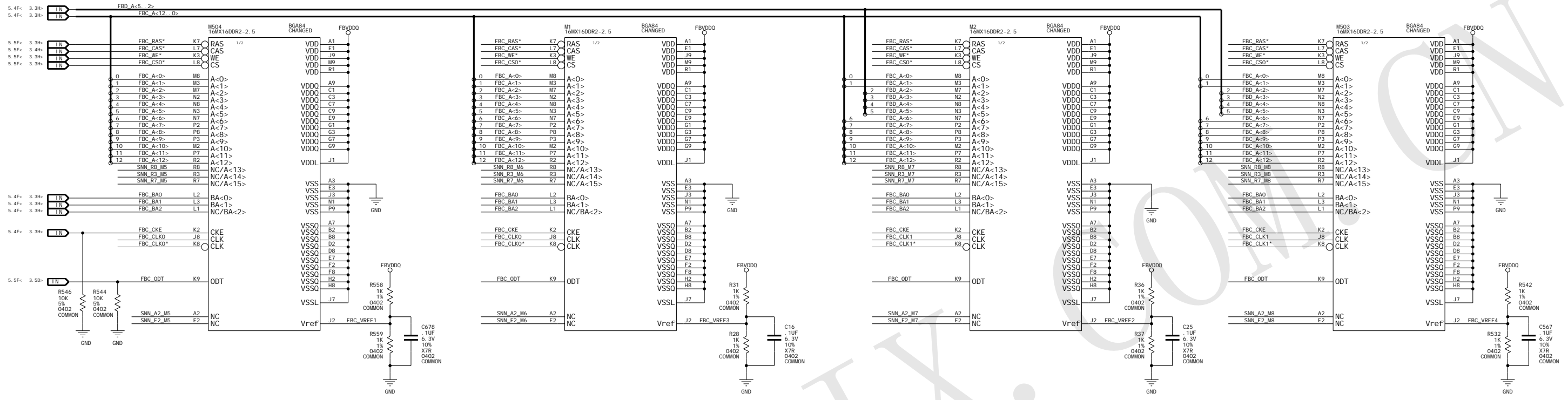
ASSEMBLY GB4M-600 450/400 256MB 128bi 1 GDDR2 16Mx16 84FBGA, LVDS + DVI\_A/DVI\_B + TV\_OUT + VGA, 16MX V1.3, HDCP.  
PAGE DETAIL Frame Buffer Partition A Memories

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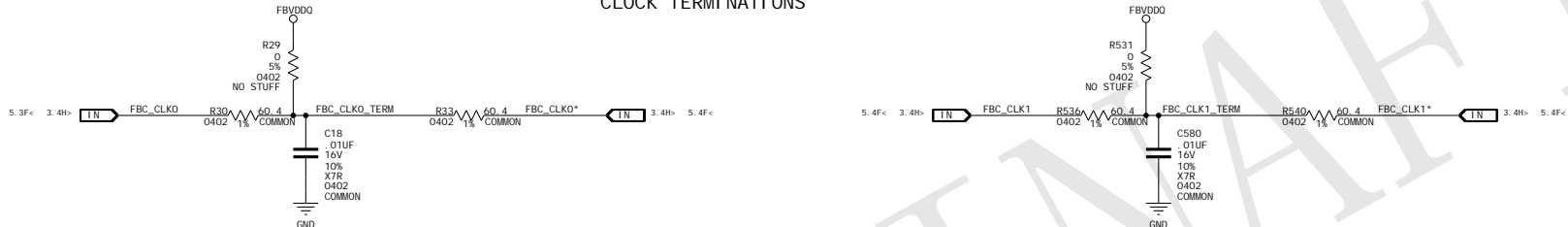
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CLOCK TERMINATIONS



NET	MI_N_L1_NE_WI_DTH	VOLTAGE
FBC_VREF1	16MLL	0.9V
FBC_VREF2	16MLL	0.9V
FBC_VREF3	16MLL	0.9V
FBC_VREF4	16MLL	0.9V

NET	DI_FFPAIR	CRITICAL	IMPEDANCE
FBC_CLK0	FBC_CLK0	1	10001 FF
FBC_CLK0*	FBC_CLK0	1	10001 FF
FBC_CLK1	FBC_CLK1	1	10001 FF
FBC_CLK1*	FBC_CLK1	1	10001 FF
FBCDQ0	FBCDQ0	1	10001 FF
FBCDQ0*	FBCDQ0	1	10001 FF
FBCDQ1	FBCDQ1	1	10001 FF
FBCDQ1*	FBCDQ1	1	10001 FF
FBCDQ2	FBCDQ2	1	10001 FF
FBCDQ2*	FBCDQ2	1	10001 FF
FBCDQ3	FBCDQ3	1	10001 FF
FBCDQ3*	FBCDQ3	1	10001 FF
FBCDQ4	FBCDQ4	1	10001 FF
FBCDQ4*	FBCDQ4	1	10001 FF
FBCDQ5	FBCDQ5	1	10001 FF
FBCDQ5*	FBCDQ5	1	10001 FF
FBCDQ6	FBCDQ6	1	10001 FF
FBCDQ6*	FBCDQ6	1	10001 FF
FBCDQ7	FBCDQ7	1	10001 FF
FBCDQ7*	FBCDQ7	1	10001 FF

FBC A<12>_0<	2	560HM
FBD A<5>_2<	2	560HM
FBC_BA0	2	560HM
FBC_BA1	2	560HM
FBC_CKE	2	560HM
FBC_BA2	2	560HM
FBC_RAS*	2	560HM
FBC_CAS*	2	560HM
FBC_WE*	2	560HM
FBC_CS0*	2	560HM
FBC_CS1*	2	560HM
FBCD<63>_0<	2	500HM
FBCDOM<7>_0<	2	500HM
FBC_ODT	2	560HM

MI	16MX16DDR2-2.5	MI	16MX16DDR2-2.5	MI	16MX16DDR2-2.5	MI	16MX16DDR2-2.5
0	FBCD<0>	8	FBCD<8>	16	FBCD<16>	24	FBCD<24>
1	FBCD<1>	9	FBCD<9>	17	FBCD<17>	25	FBCD<25>
2	FBCD<2>	10	FBCD<10>	18	FBCD<18>	26	FBCD<26>
3	FBCD<3>	11	FBCD<11>	19	FBCD<19>	27	FBCD<27>
4	FBCD<4>	12	FBCD<12>	20	FBCD<20>	28	FBCD<28>
5	FBCD<5>	13	FBCD<13>	21	FBCD<21>	29	FBCD<29>
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7	FBCD<7>	15	FBCD<15>	23	FBCD<23>	31	FBCD<31>
FBCDOM<0>		FBCDOM<1>		FBCDOM<2>		FBCDOM<3>	
FBCDOS1		FBCDOS1*		FBCDOS2		FBCDOS2*	
FBCDOS0*		FBCDOS1*		FBCDOS3		FBCDOS3*	

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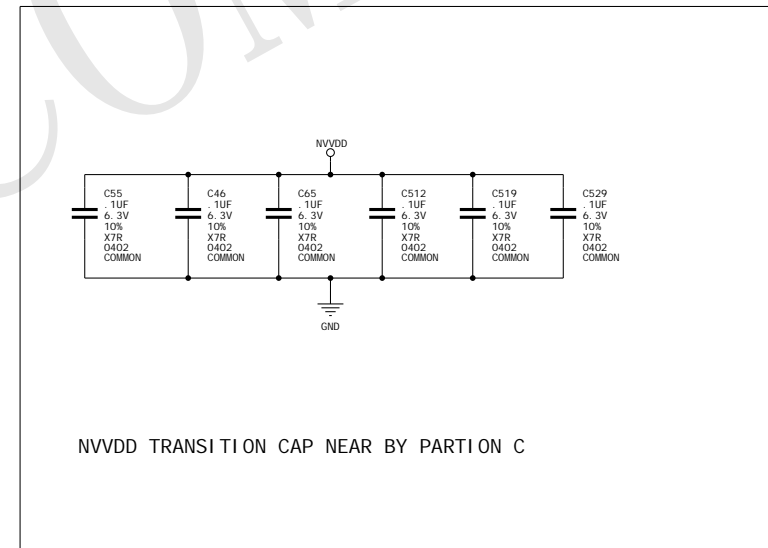
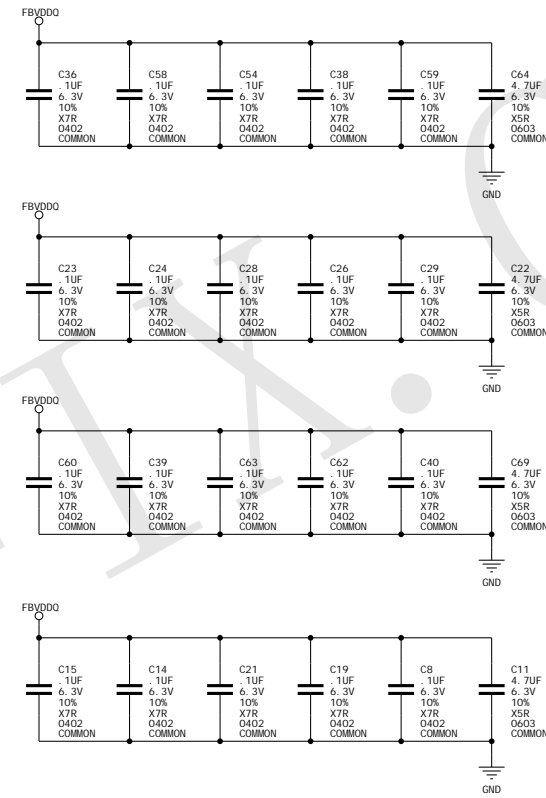
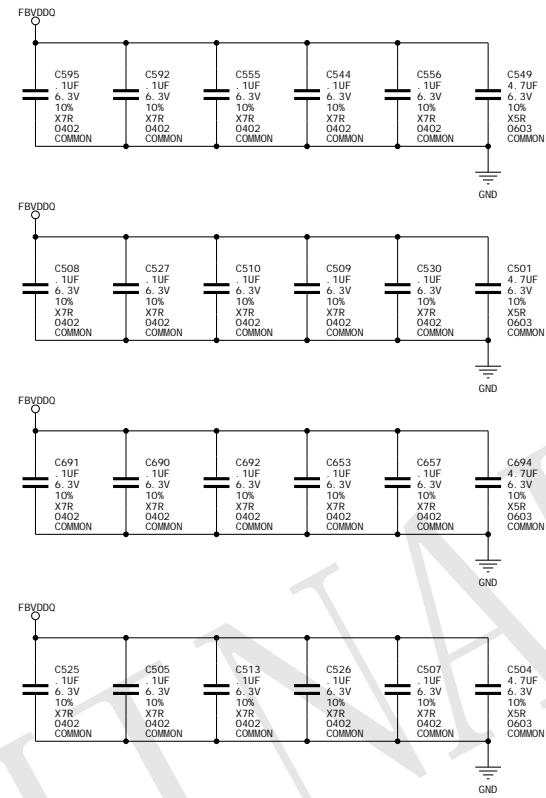
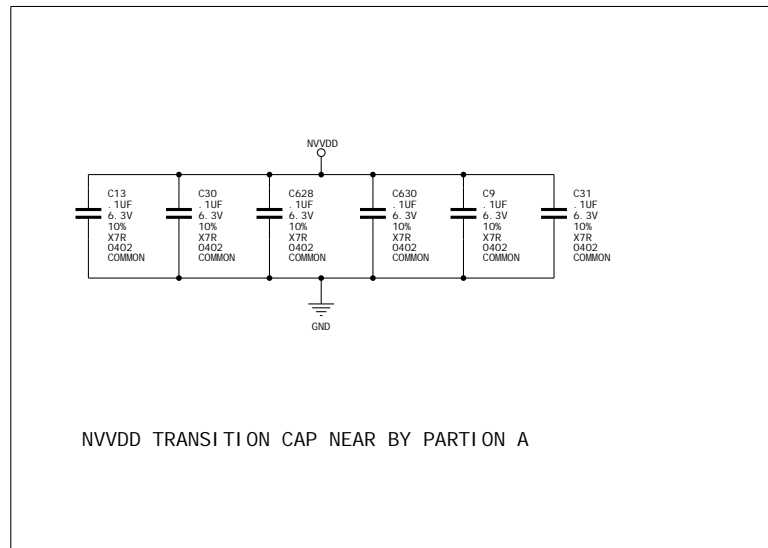
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ASSEMBLY: GB4M-600 450/400 256MB 128bit 1 GDDR2 16Mx16 84FBGA, LVDS + DVI\_A/DVI\_B + TV\_OUT + VGA, MXM V1.3, HDCP.  
 PAGE DETAIL: Frame Buffer Partition C Memory

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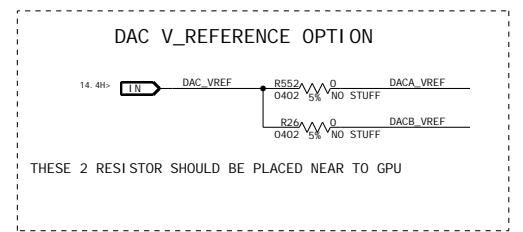
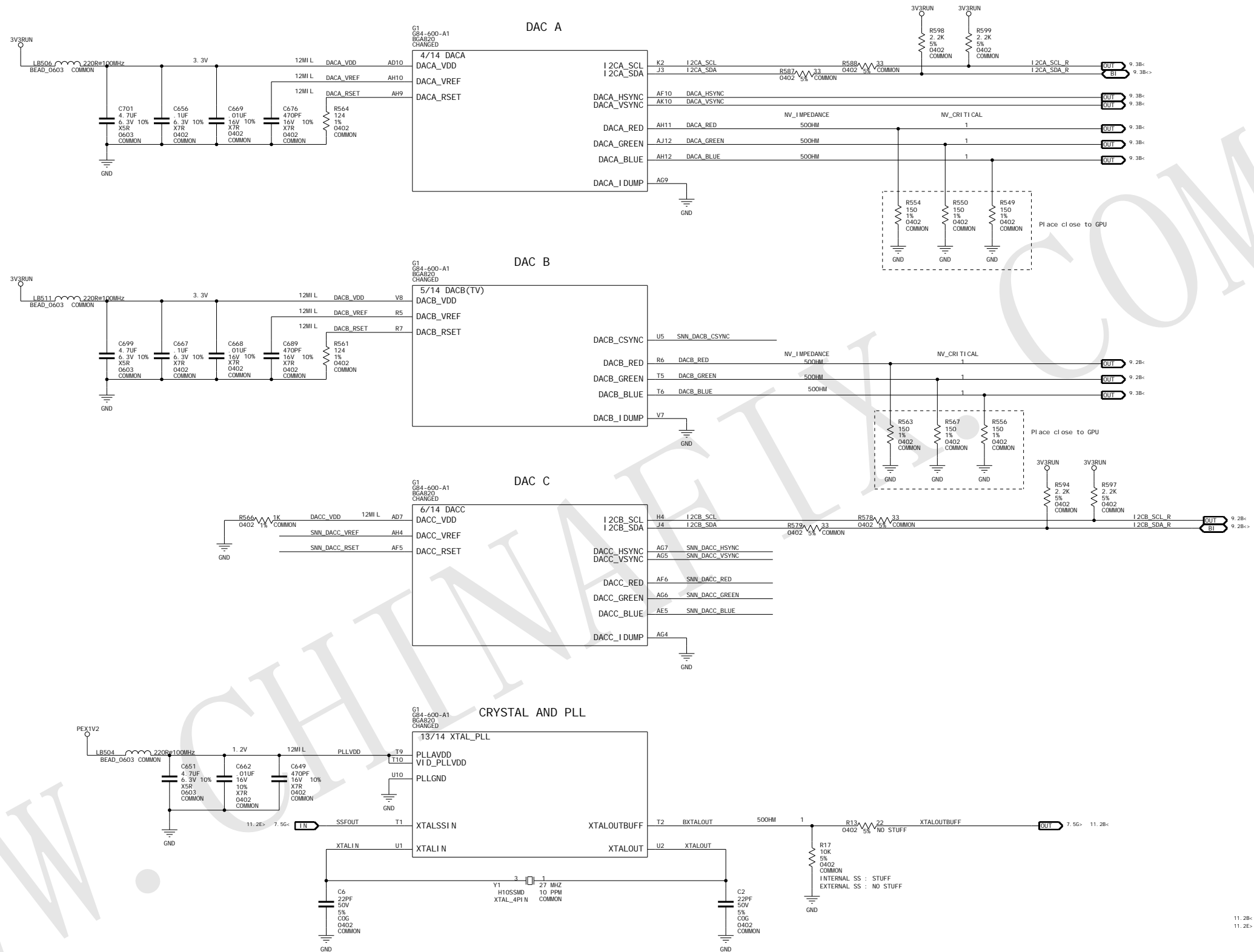
DECOUPLING CAPS FOR MEMORYS (PARTION A AND PARTION C)



ASSEMBLY	G84M-600 450/400 256MB 128bit 1 GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	Memory Decoupling Caps

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NET	NV_NET_NAME	NV_I_MPEDANCE	NV_CRITICAL_NET
XTALOUT	XTALOUT	500HM	1
XTALIN	XTALIN	500HM	1
XTALOUTBUFF	XTALOUTBUFF	500HM	1
SSFOUT	SSFOUT	500HM	1

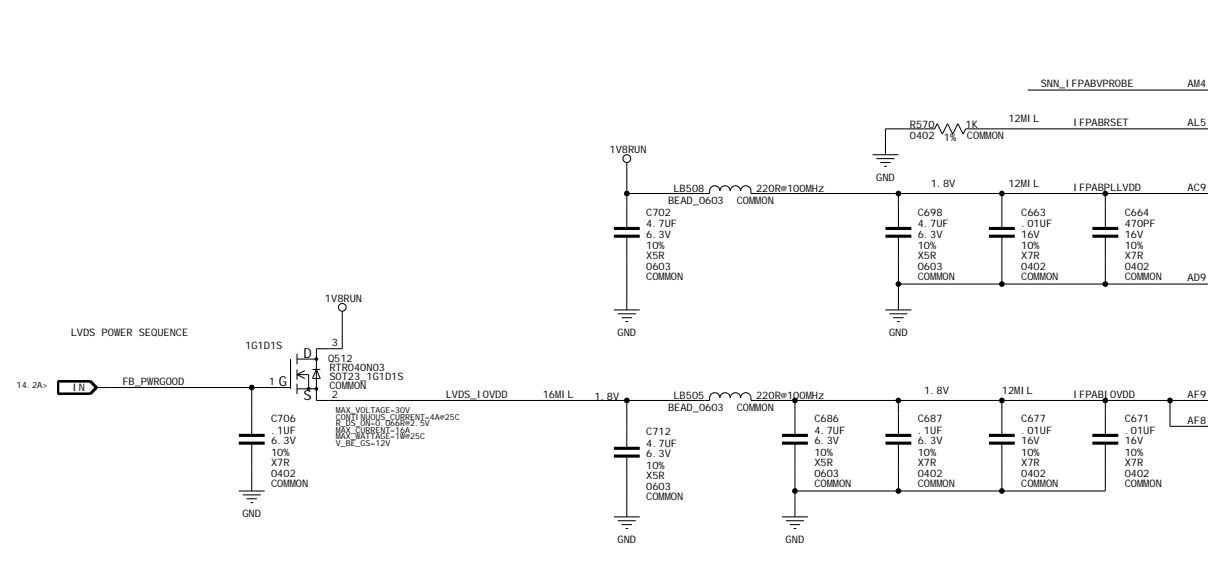
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ASSEMBLY	G84M-600 450/400 256MB 128bit 1 GDDR2 164x16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	DACs, Clock-Generation

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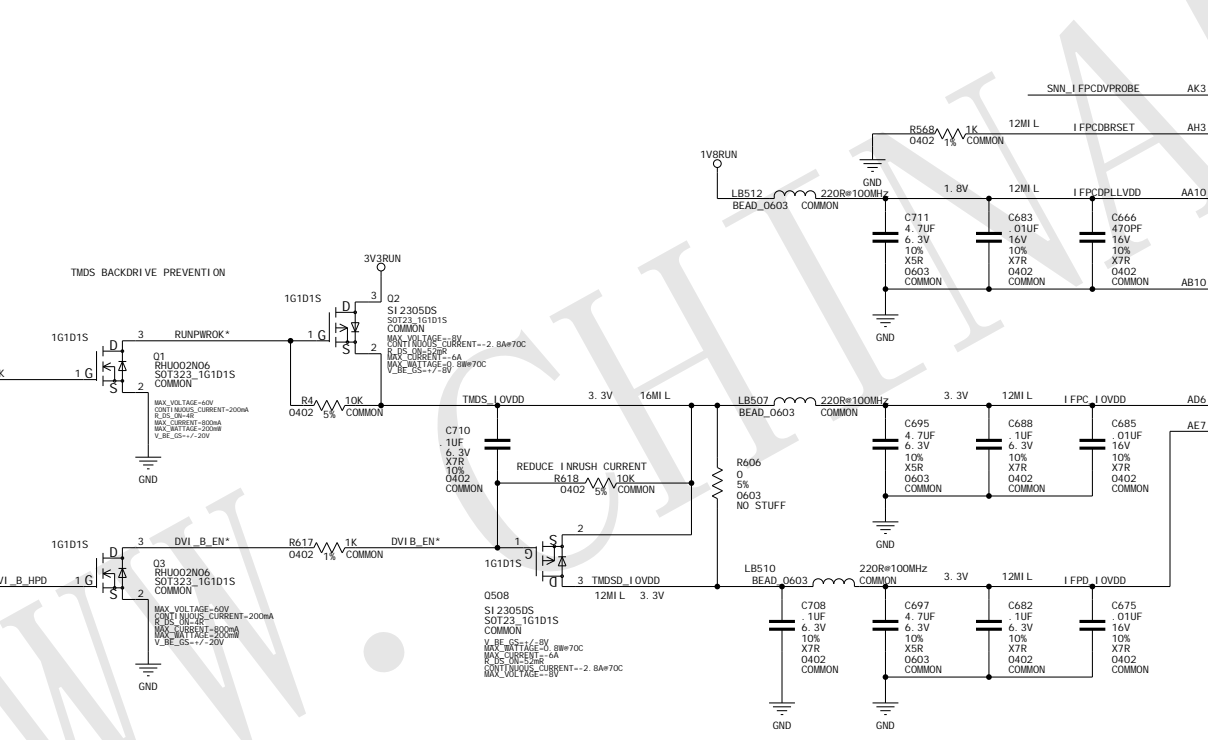
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LVDS

NET NAME	DI FFPAIR	NV_CRI TI CAL_NET	NV_I MPEDANCE
I FPA_TXC	AJ9	1	100DI FF
I FPA_TXC	AK9	1	100DI FF
I FPA_TXD0	AJ6	1	100DI FF
I FPA_TXD0	AH6	1	100DI FF
I FPA_TXD1	AH7	1	100DI FF
I FPA_TXD1	AH8	1	100DI FF
I FPA_TXD2	AK8	1	100DI FF
I FPA_TXD2	AJ8	1	100DI FF
I FPA_TXD3	AH5	1	100DI FF
I FPA_TXD3	AJ5	1	100DI FF
I FPB_TXC	AL4	1	100DI FF
I FPB_TXC	AK4	1	100DI FF
I FPB_TXD4	AM5	1	100DI FF
I FPB_TXD4	AM6	1	100DI FF
I FPB_TXD5	AL7	1	100DI FF
I FPB_TXD5	AM7	1	100DI FF
I FPB_TXD6	AK5	1	100DI FF
I FPB_TXD6	AK6	1	100DI FF
I FPB_TXD7	AL8	1	100DI FF
I FPB_TXD7	AK7	1	100DI FF



TMDS

NET NAME	DI FFPAIR	NV_CRI TI CAL_NET	NV_I MPEDANCE
I FPC_TXC	AM3	1	100DI FF
I FPC_TXC	AM2	1	100DI FF
I FPC_TXD0	AE1	1	100DI FF
I FPC_TXD0	AE2	1	100DI FF
I FPC_TXD1	AF2	1	100DI FF
I FPC_TXD1	AF1	1	100DI FF
I FPC_TXD2	AH1	1	100DI FF
I FPC_TXD2	AG1	1	100DI FF
I FPD_TXC	AH2	1	100DI FF
I FPD_TXC	AG3	1	100DI FF
I FPD_TXD4	AJ1	1	100DI FF
I FPD_TXD4	AK1	1	100DI FF
I FPD_TXD5	AL1	1	100DI FF
I FPD_TXD5	AL2	1	100DI FF
I FPD_TXD6	AJ3	1	100DI FF
I FPD_TXD6	AJ2	1	100DI FF

ASSEMBLY	G84-600 450/400 256MB 128bi 1 GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP
PAGE DETAIL	LVDS, TMDS GPU Interface

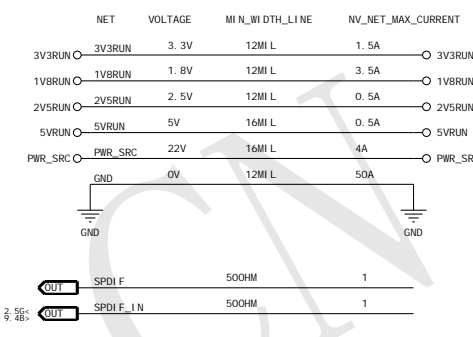
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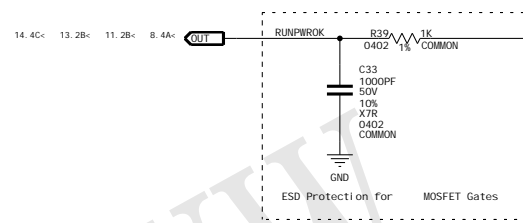
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MXM CONNECTOR

CON J00L\_X16\_EDGE (N\_NON)PHY-X16,-HE)\_SLI NPHY-X16\_SL1 NO STUFF

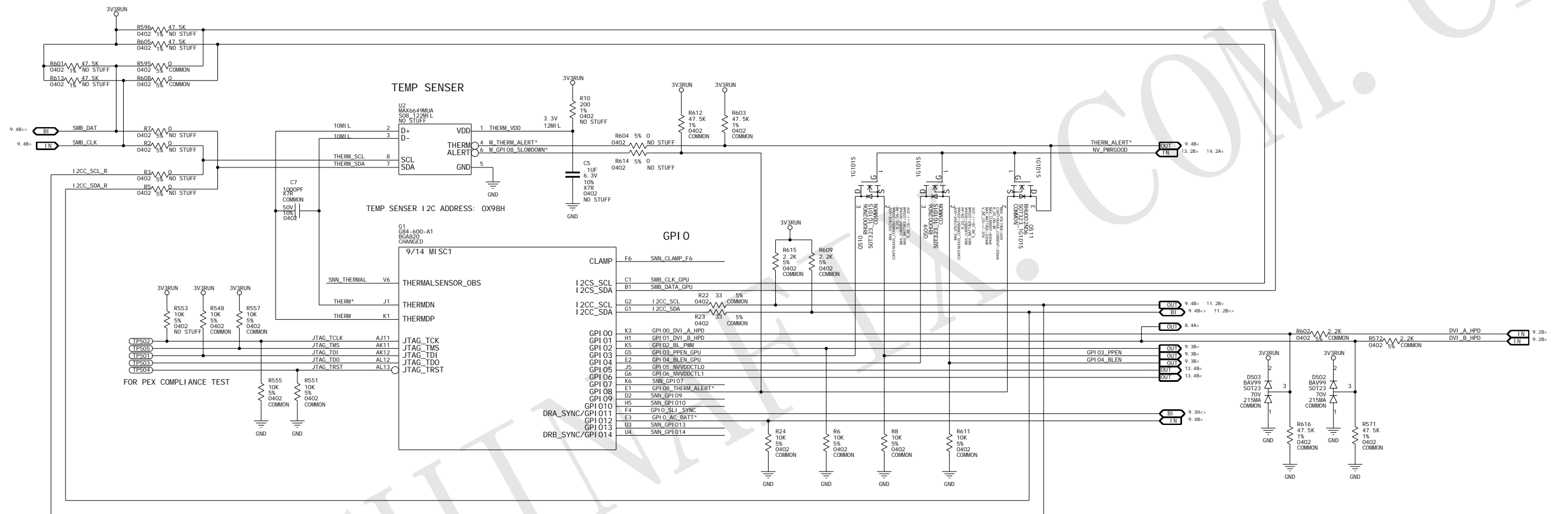


PLACE THESE COMPONENTS TO ISOLATE 2 TYPE SIGNALS AND BALANCE THE LOAD OF THE DIFF PAIR

ASSEMBLY	G84M-600 450/400 256MB 128bit 1 GDDR2 164x16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	MXM Connector, 10-Section

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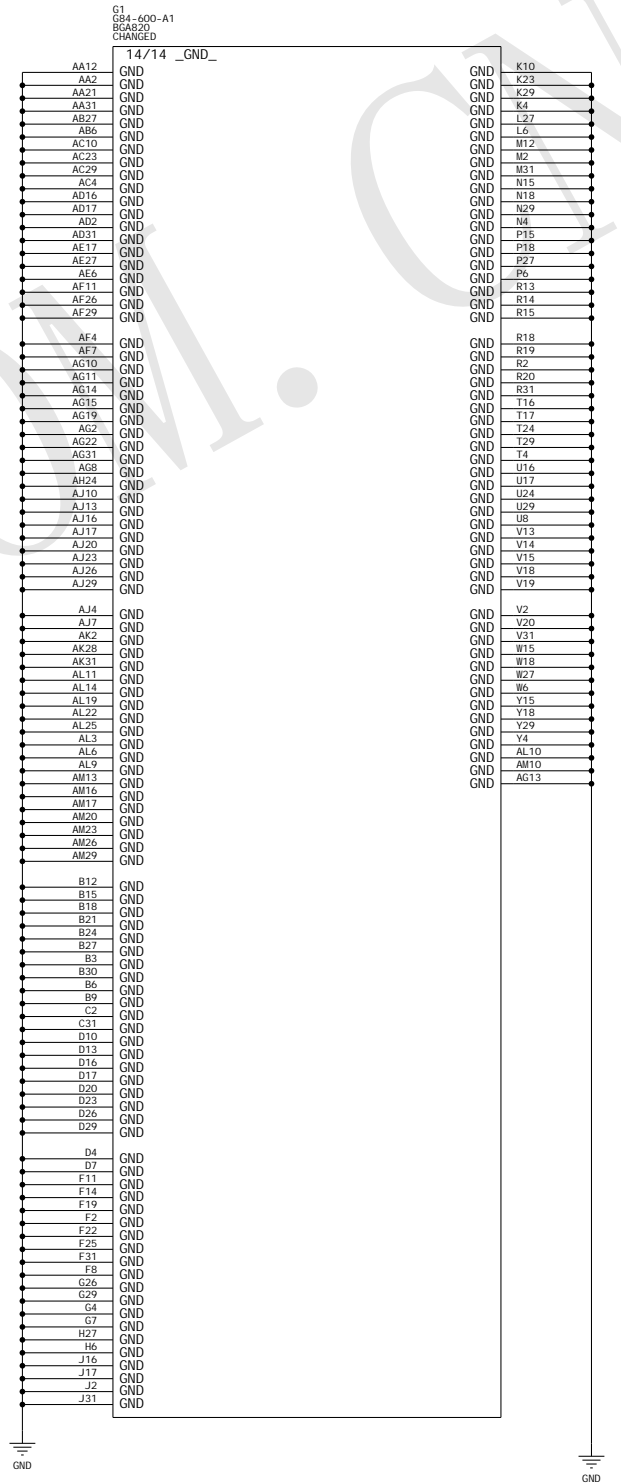
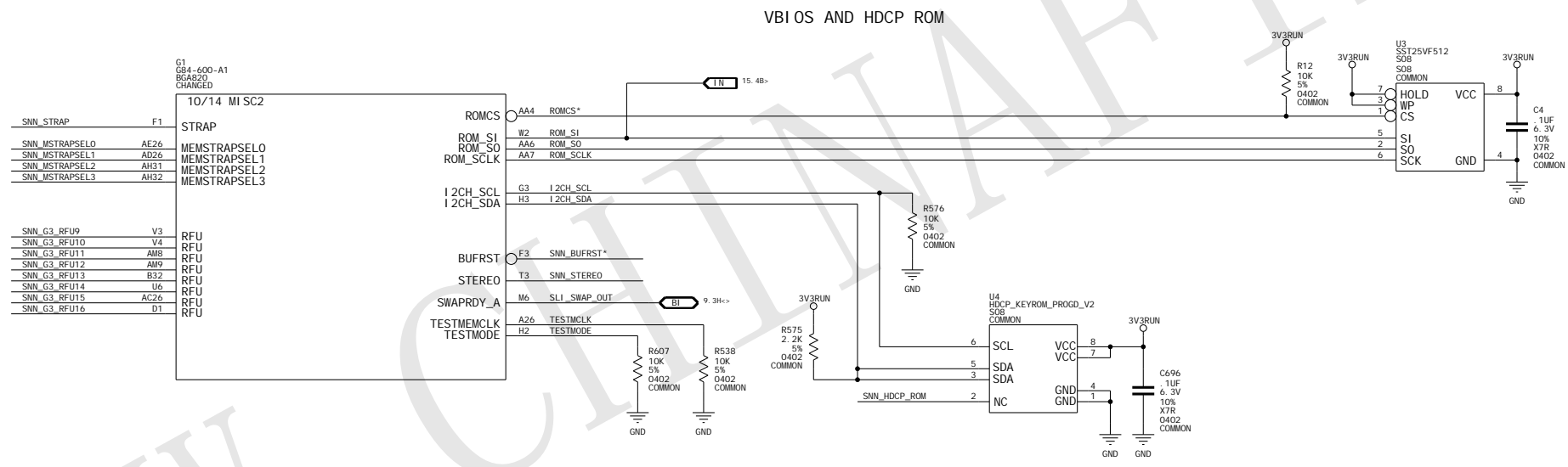
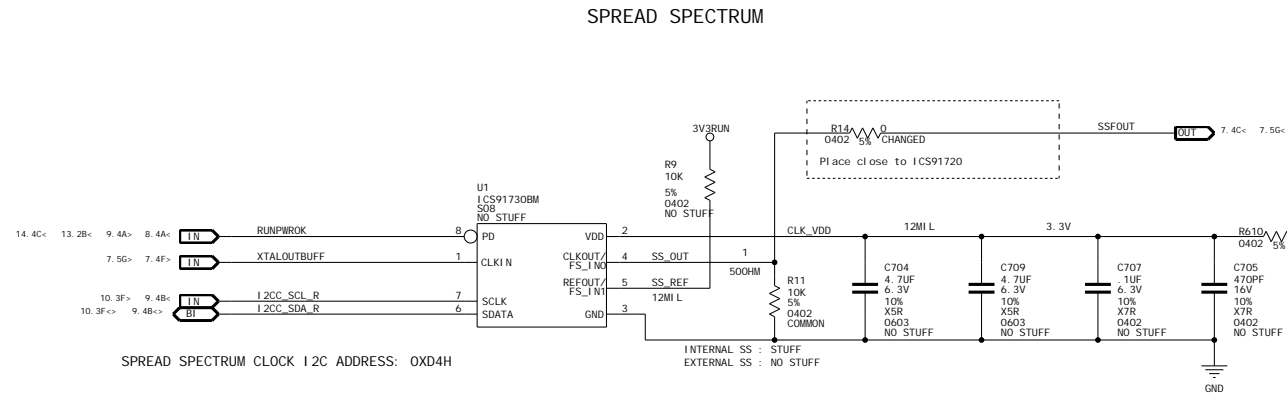
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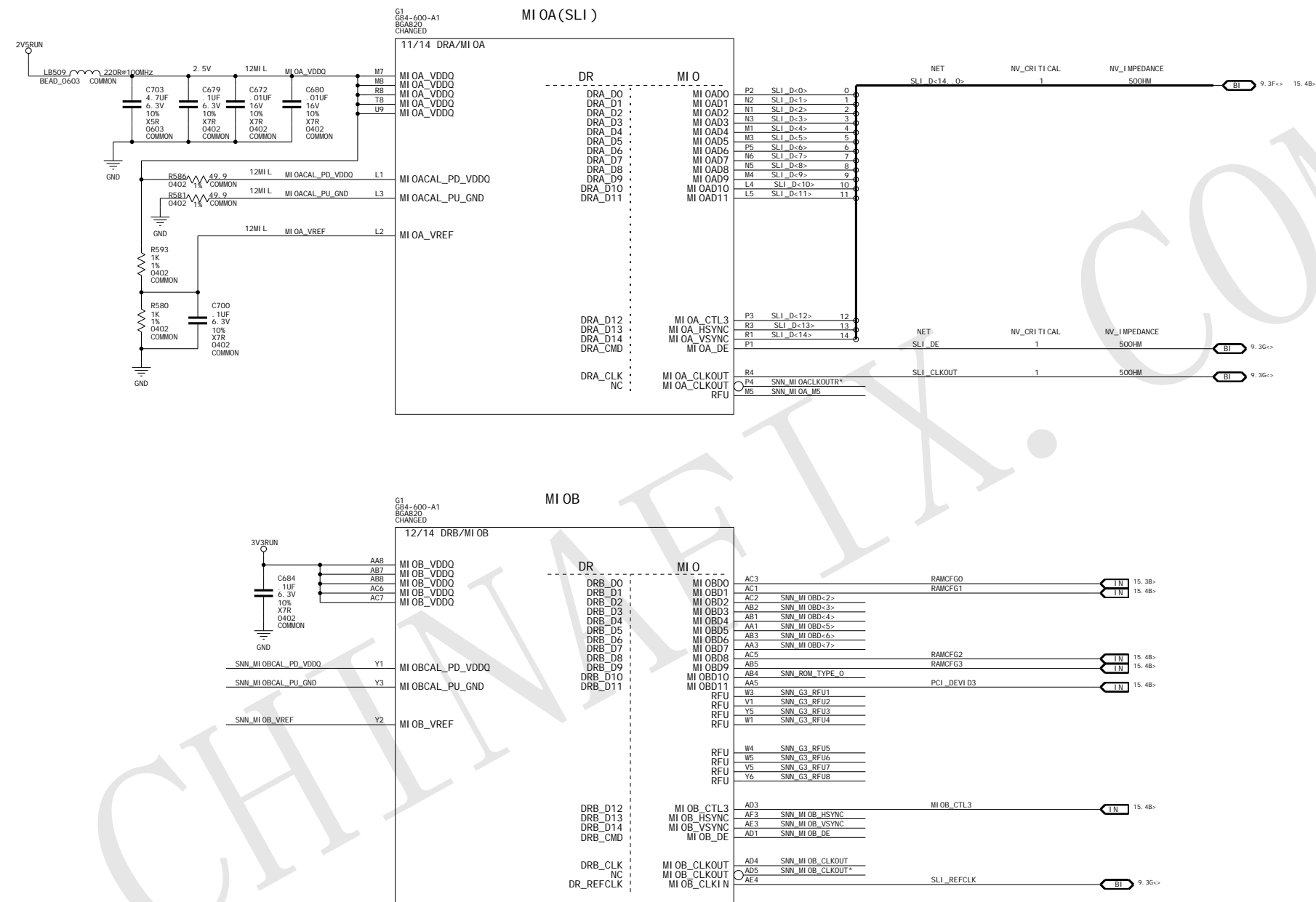
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ASSEMBLY	GBM-600 450/400 256MB 128bi 1 GDDR2 164x16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP
PAGE DETAIL	GPIOs, JTAG, Thermal Sensor

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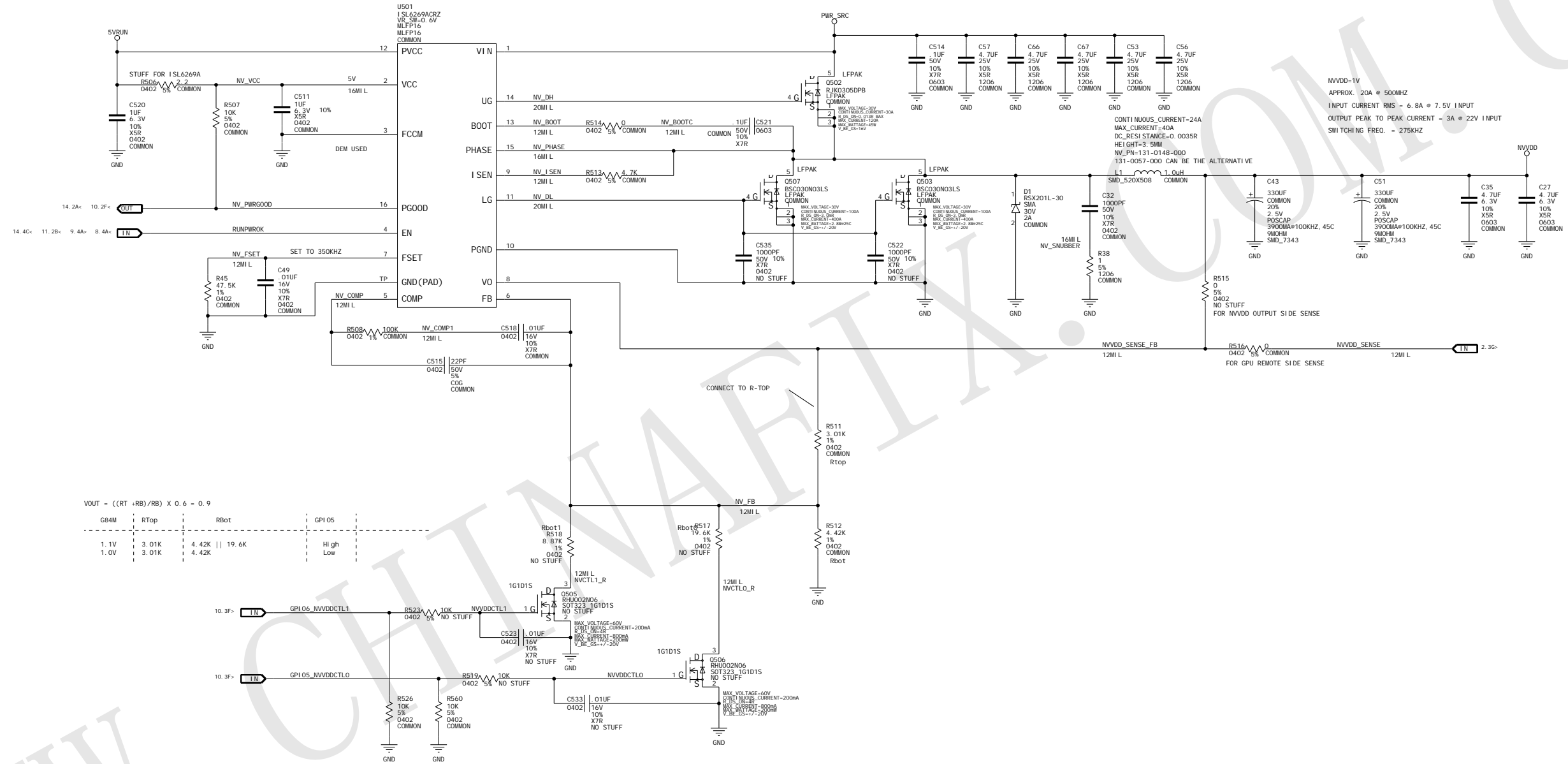


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NET	VOLTAGE	MIN_WIDTH	MIN_LENGTH	NV_NET_MAX_CURRENT
NVVDD	1V	12MIL		30A

NVVDD SWITCHER POWER SUPPLY



NVVDD-1V  
 APPROX. 20A @ 500MHZ  
 INPUT CURRENT RMS = 6.8A @ 7.5V INPUT  
 OUTPUT PEAK TO PEAK CURRENT = 3A @ 22V INPUT  
 SWITCHING FREQ. = 275KHZ

$$V_{OUT} = ((R_{TOP} + R_B) / R_B) \times 0.6 = 0.9$$

GB4M	RTOP	RBOT	GPI05
1.1V	3.01K	4.42K	High
1.0V	3.01K	4.42K	Low

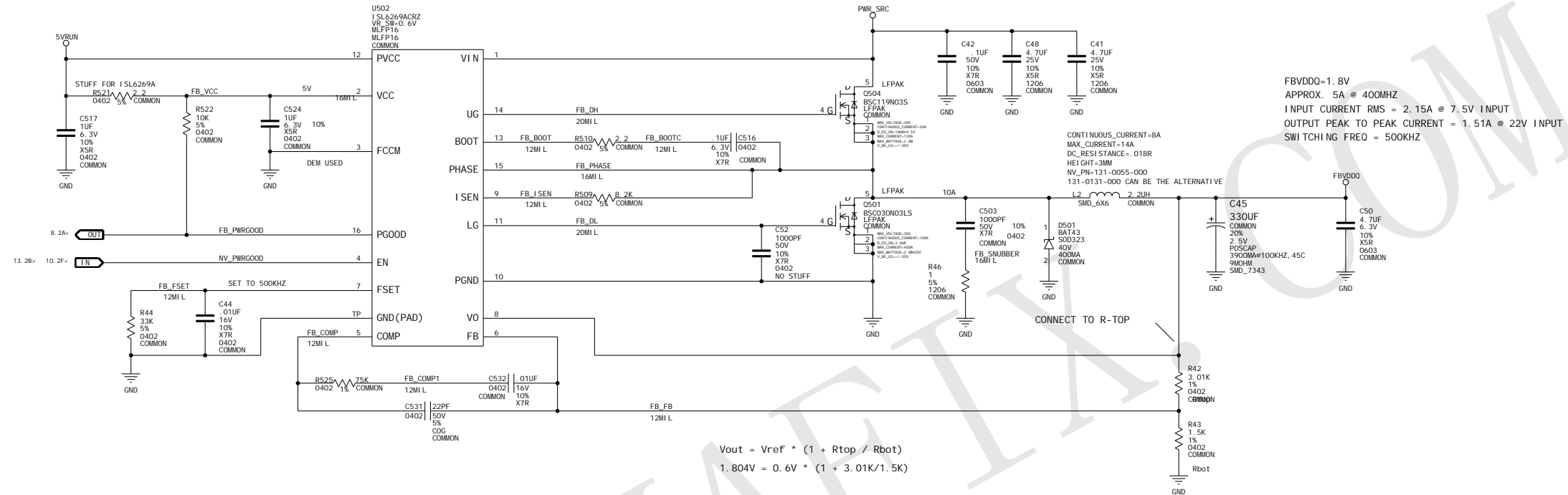
ASSEMBLY	GB4M-600 450/400 256MB 128bit 1 GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	NVVDD Power Supply

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NET	VOLTAGE	MIN_LENGTH	MAX_LENGTH	NET_MAX_CURRENT
PEX1V2	1.2V	12MIL	2A	PEX1V2
FBVDDQ	1.8V	12MIL	10A	FBVDDQ

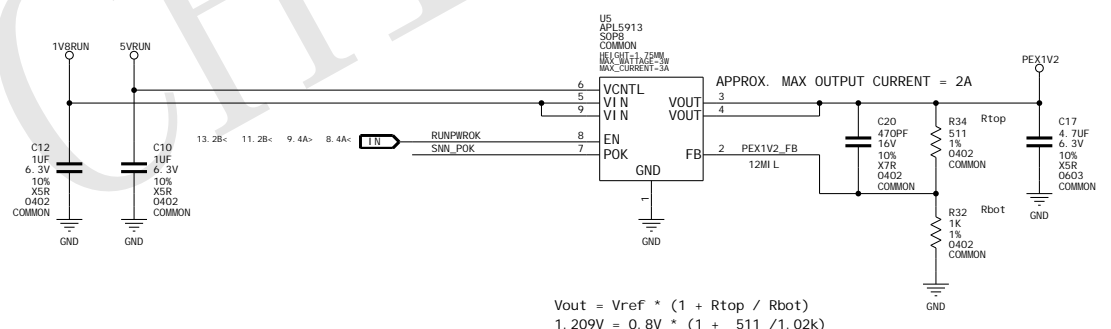
FBVDDQ SWITCHER POWER SUPPLY



$$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$$

$$1.804V = 0.6V * (1 + 3.01K / 1.5K)$$

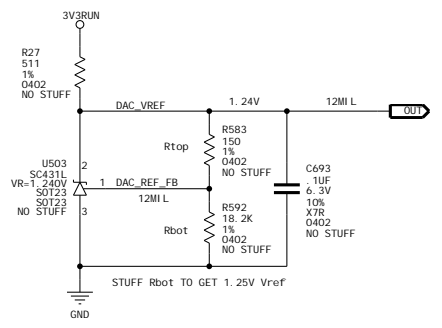
PEX1V2 LINEAR SUPPLY



$$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$$

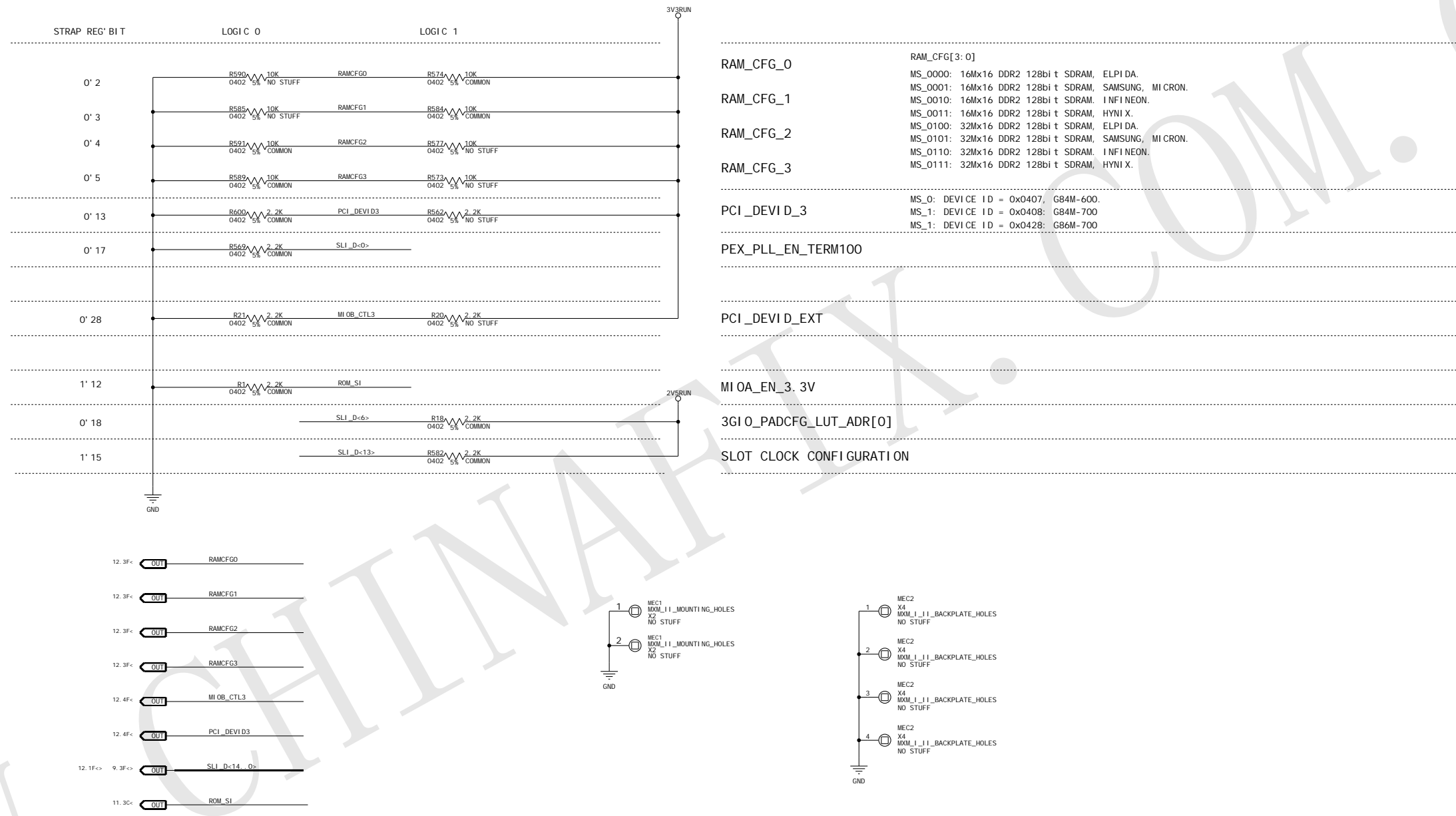
$$1.209V = 0.8V * (1 + 511 / 1.02K)$$

DAC V\_REFERENCE SUPPLY



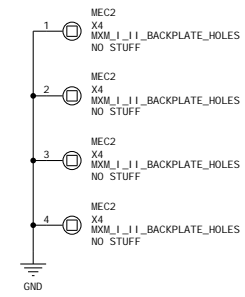
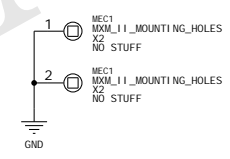
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RAM_CFG_0	RAM_CFG[3:0]
RAM_CFG_1	MS_000: 16Mx16 DDR2 128bi t SDRAM, ELPI DA.
RAM_CFG_2	MS_001: 16Mx16 DDR2 128bi t SDRAM, SAMSUNG, MICRON.
RAM_CFG_3	MS_010: 16Mx16 DDR2 128bi t SDRAM, INFI NEON.
	MS_0011: 16Mx16 DDR2 128bi t SDRAM, HYNI X.
	MS_0100: 32Mx16 DDR2 128bi t SDRAM, ELPI DA.
	MS_0101: 32Mx16 DDR2 128bi t SDRAM, SAMSUNG, MICRON.
	MS_0110: 32Mx16 DDR2 128bi t SDRAM, INFI NEON.
	MS_0111: 32Mx16 DDR2 128bi t SDRAM, HYNI X.
PCI_DEVID_3	MS_0: DEVICE ID = 0x0407: G84M-600.
	MS_1: DEVICE ID = 0x0408: G84M-700
	MS_1: DEVICE ID = 0x0428: G86M-700
PEX_PLL_EN_TERM100	
PCI_DEVID_EXT	
MI OA_EN_3_3V	
3GIO_PADCFG_LUT_ADR[0]	
SLOT_CLOCK_CONFIGURATION	

- 12.3F< OUT1 RAMCFG0
- 12.3F< OUT1 RAMCFG1
- 12.3F< OUT1 RAMCFG2
- 12.3F< OUT1 RAMCFG3
- 12.4F< OUT1 MI OB\_CTL3
- 12.4F< OUT1 PCI\_DEVID3
- 9.3F<> OUT1 SLI\_D<14..0>
- 11.3C< OUT1 ROM\_SI



ASSEMBLY	G84M-600 450/400 256MB 128bi t GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, M0M V1.3, HDCP.
PAGE DETAIL	STRAPS, TTP, MOUNTING HOLE

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Title: Basenet Report  
Desig: p555\_a00  
Date: Nov 30 11:00:17 2006

Base nets and synonyms for  
p407.lib.p555\_A00(ep407.lib.p555\_a00(sch\_1))

Base Signal Locati on([Zone][di r])

1

2

3

4

5

Table with columns for signal names and values. Includes entries like FBAD-59, FBAD-60, FBAD-61, etc.

Table with columns for signal names and values. Includes entries like FBAL\_TERM, FBAD-60, FBAD-61, etc.

Table with columns for signal names and values. Includes entries like FBC\_A-2, FBC\_A-3, FBC\_A-4, etc.

Table with columns for signal names and values. Includes entries like I2CC\_SCL\_R, I2CC\_SDA, I2CC\_SDA\_R, etc.

Table with columns for signal names and values. Includes entries like PEX\_RX3, PEX\_RX4, PEX\_RX5, etc.

Table with columns for signal names and values. Includes entries like RAMCFG3, ROMCS, ROM\_SCLK, etc.

1

2

3

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5

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ASSEMBLY G8M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI\_A/DVI\_B + TV\_OUT + VGA, MXM V1.3, HDCP.  
PAGE DETAIL <edit here to insert page detail>



SNN_G3_RFU11	11.4A
SNN_G3_RFU12	11.4A
SNN_G3_RFU13	11.4A
SNN_G3_RFU14	11.4A
SNN_G3_RFU15	11.4A
SNN_G3_RFU16	11.4A
SNN_GND_SENSE	2.3F
SNN_GPI07	10.3D
SNN_GPI09	10.3D
SNN_GPI010	10.3D
SNN_GPI013	10.3D
SNN_GPI014	10.3D
SNN_GPU_AG12	2.1D
SNN_GPU_AH13	2.2D
SNN_HDCP_ROM	11.4D
SNN_I1FPABVPROBE	8.1D
SNN_I1FPCDVPROBE	8.3D
SNN_MI_OACLKOUT*	12.2E
SNN_MI_OA_M5	12.2E
SNN_MI_OBCAL_PD_VDD	12.3C
0	
SNN_MI_OBCAL_PU_GND	12.3C
SNN_MI_OBD<2>	12.3E
SNN_MI_OBD<3>	12.3E
SNN_MI_OBD<4>	12.3E
SNN_MI_OBD<5>	12.3E
SNN_MI_OBD<6>	12.3E
SNN_MI_OBD<7>	12.3E
SNN_MI_OB_CLKOUT	12.4E
SNN_MI_OB_CLKOUT*	12.4E
SNN_MI_OB_DE	12.4E
SNN_MI_OB_HSYNC	12.4E
SNN_MI_OB_VREF	12.4C
SNN_MI_OB_VSYNC	12.4E
SNN_MSTRAPSEL0	11.3A
SNN_MSTRAPSEL1	11.3A
SNN_MSTRAPSEL2	11.3A
SNN_MSTRAPSEL3	11.3A
SNN_POK	14.4C
SNN_R3_M1	4.2A
SNN_R3_M2	4.2C
SNN_R3_M3	4.2E
SNN_R3_M4	4.2G
SNN_R3_M5	5.2A
SNN_R3_M6	5.2C
SNN_R3_M7	5.2E
SNN_R3_M8	5.2G
SNN_R7_M1	4.2A
SNN_R7_M2	4.2C
SNN_R7_M3	4.2E
SNN_R7_M4	4.2G
SNN_R7_M5	5.2A
SNN_R7_M6	5.2C
SNN_R7_M7	5.2E
SNN_R7_M8	5.2G
SNN_RB_M1	4.2A
SNN_RB_M2	4.2C
SNN_RB_M3	4.2E
SNN_RB_M4	4.2G
SNN_RB_M5	5.2A
SNN_RB_M6	5.2C
SNN_RB_M7	5.2E
SNN_RB_M8	5.2G
SNN_ROM_TYPE_0	12.3E
SNN_STEREO	11.4C
SNN_STRAP	11.3A
SNN_THERMAL	10.3B
SPDIF	9.1G> 9.4C
SPDIF_IN	2.5G< 9.1G> 9.4B>
SSFOUT	7.4C< 7.5G< 11.2E>
SS_OUT	11.2C
SS_REF	11.2C
TESTCLK	11.4C
TESTMODE	11.4C
THERM	10.3B
THERM*	10.3B
THERM_ALERT*	9.4B< 10.2F>
THERM_SCL	10.2B
THERM_SDA	10.2B
THERM_VDD	10.2C
TMDS_I_OVDD	8.4C
TMDS_I_OVDD	8.4B
XTALIN	7.4C 7.5G<
XTALOUT	7.4D 7.5G>
XTALOUTBUFF	7.4F> 7.5G> 11.2B<

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ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	<edit here to insert page detail>

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