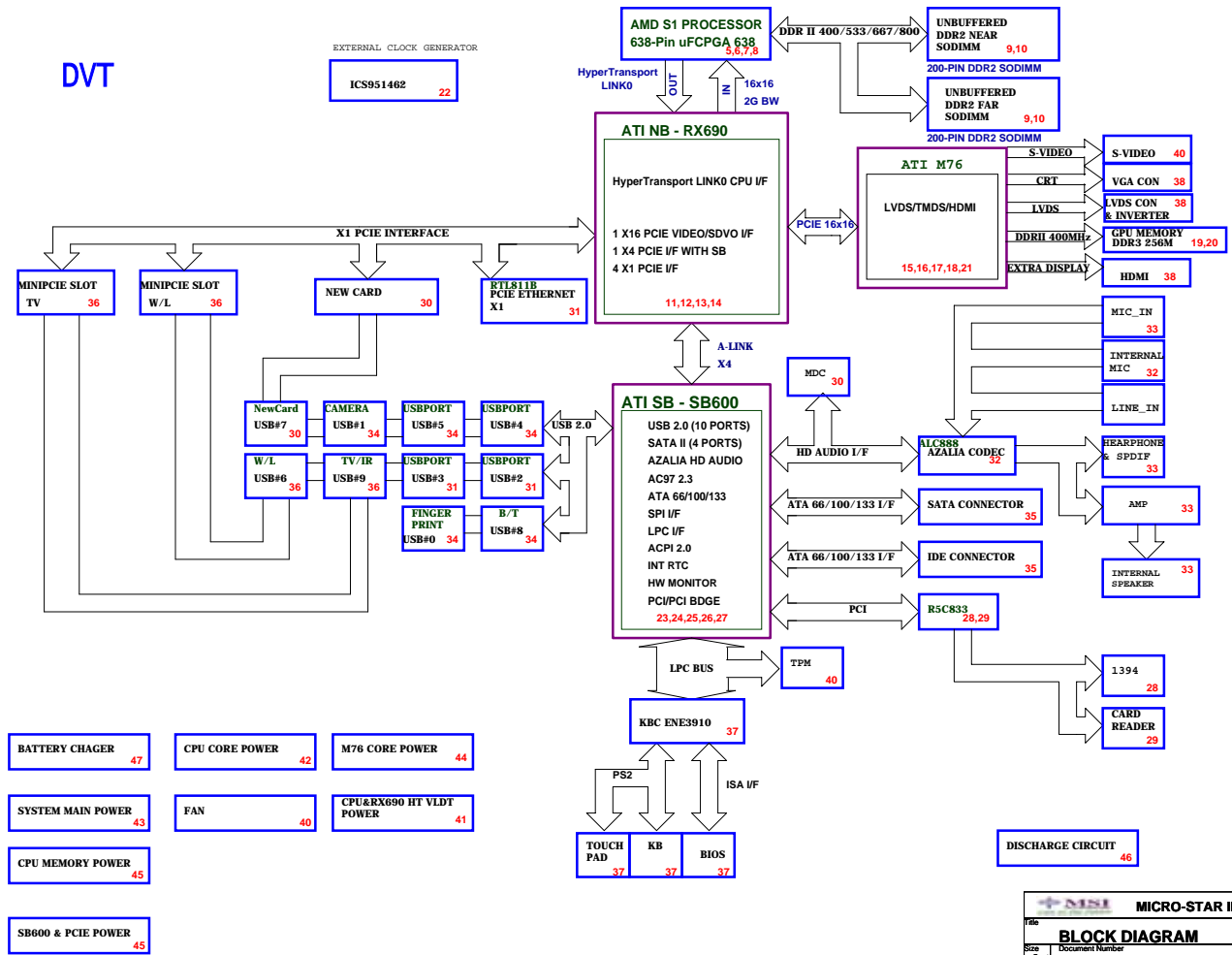
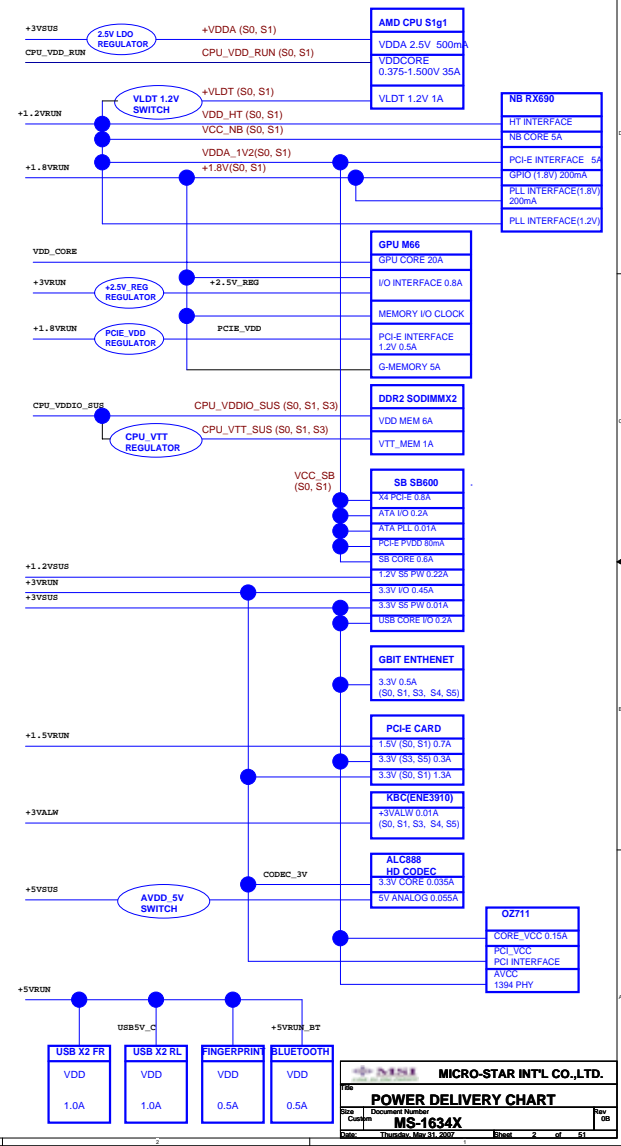
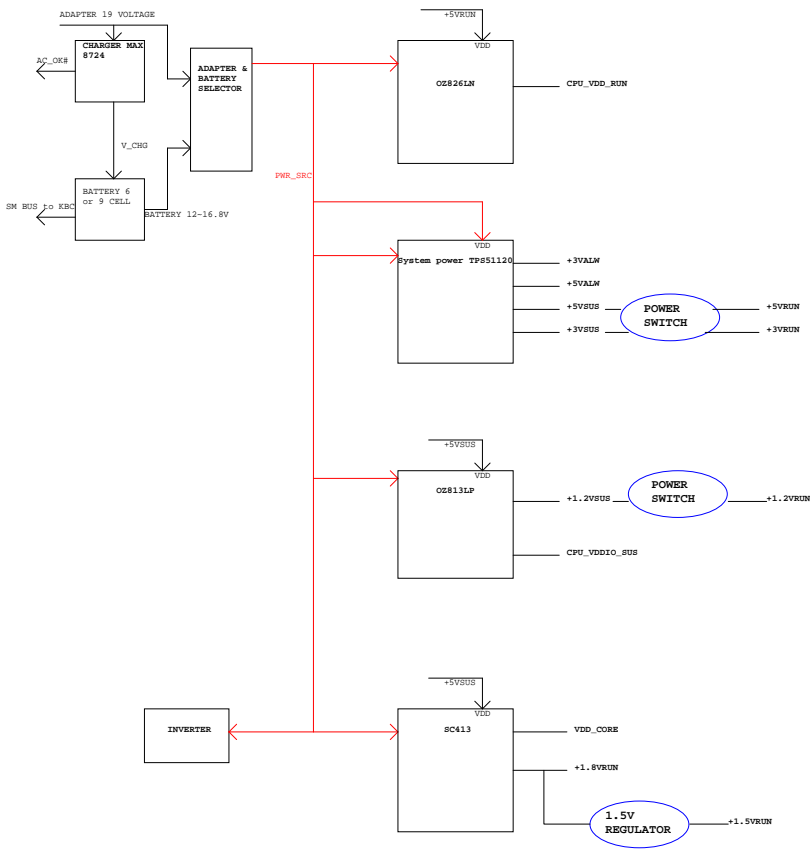
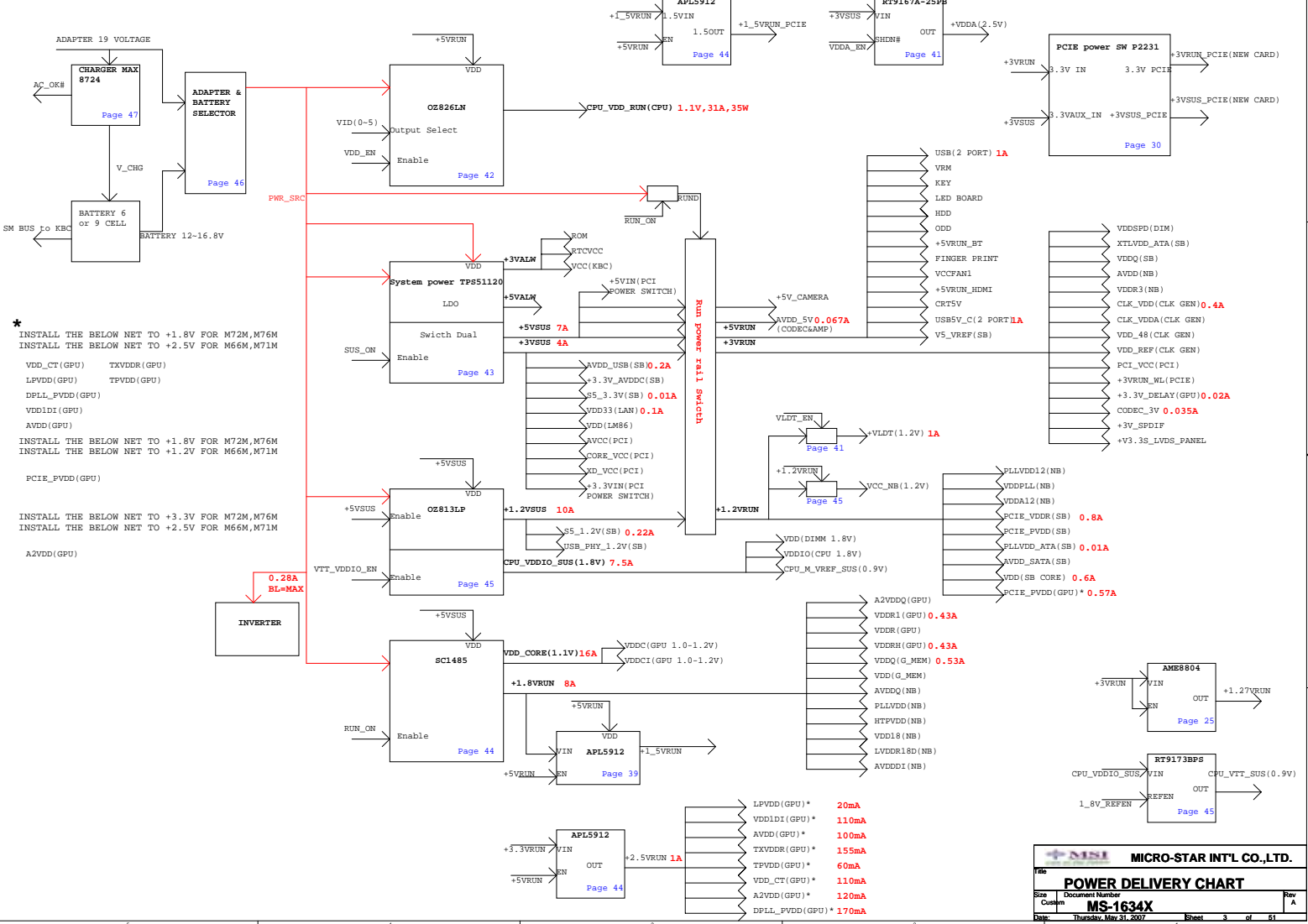


DVT





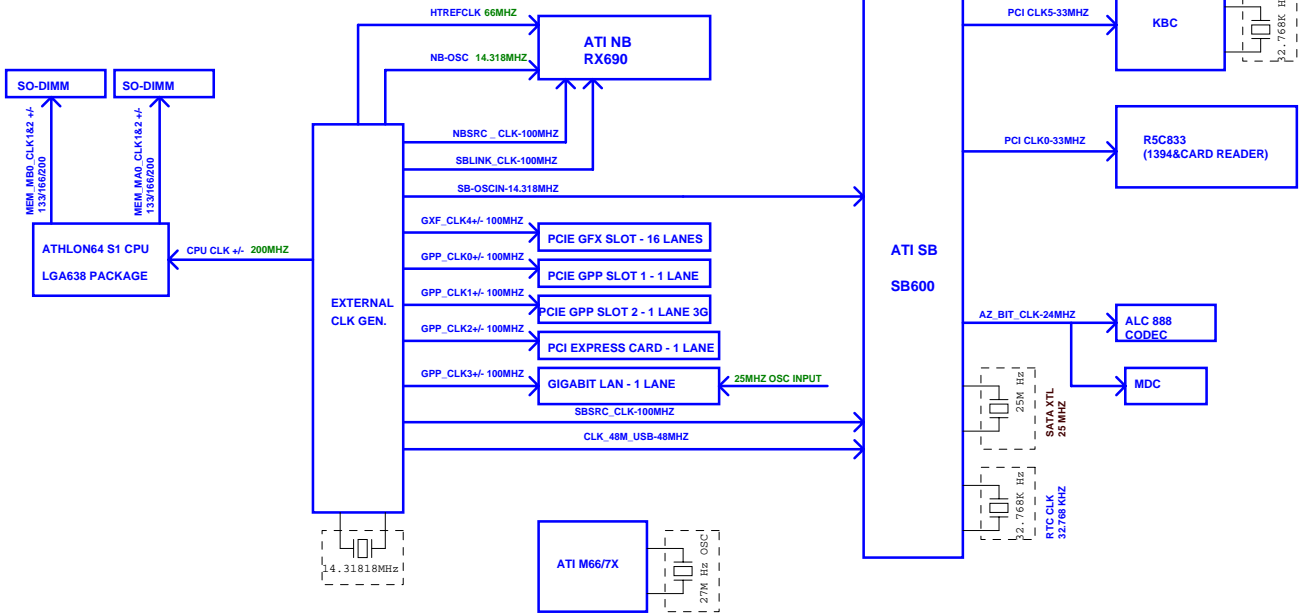


MICRO-STAR INT'L CO., LTD.

File: **POWER DELIVERY CHART**

Size: Custom Document Number: **MS-1634X**

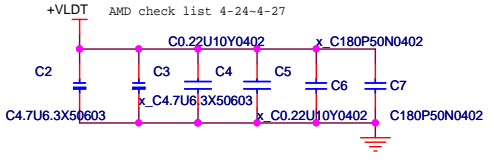
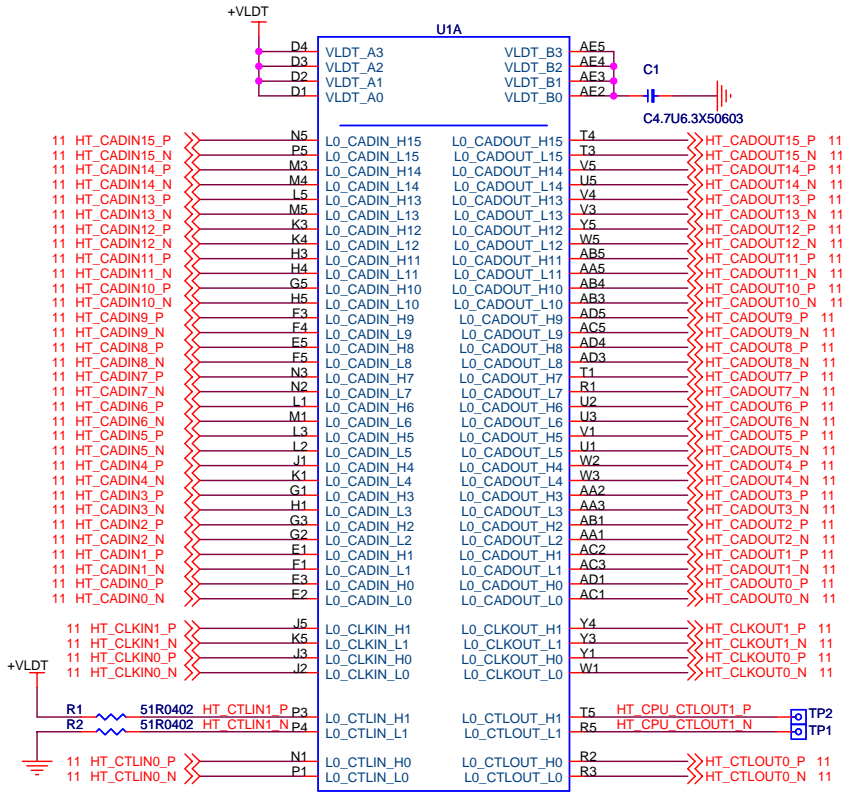
Date: Thursday, May 31, 2007 Sheet 3 of 51





PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



LAYOUT: Place bypass cap on topside of board



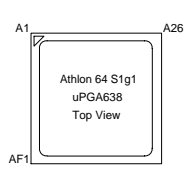
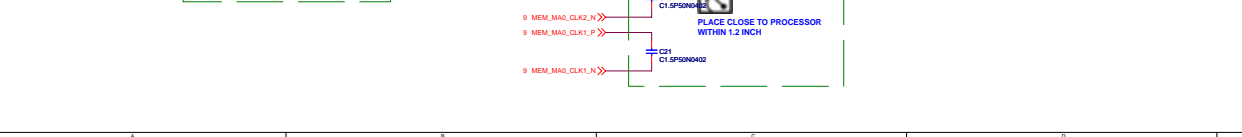
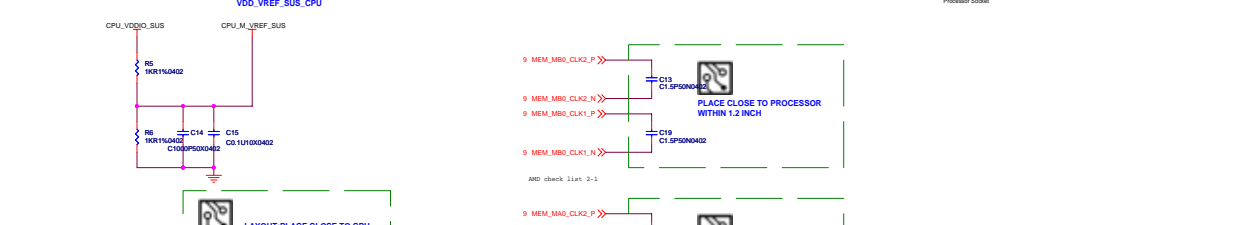
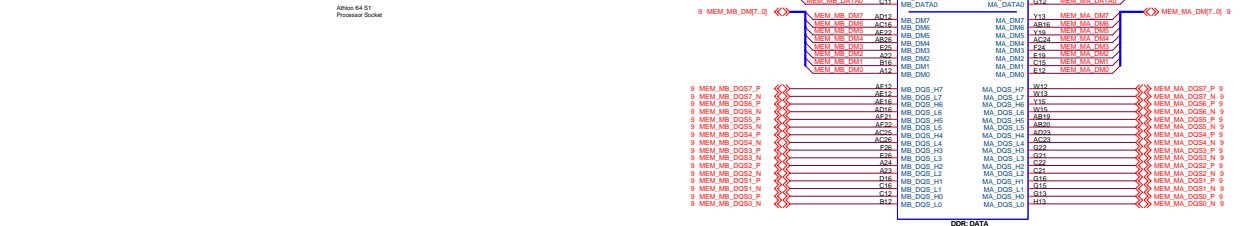
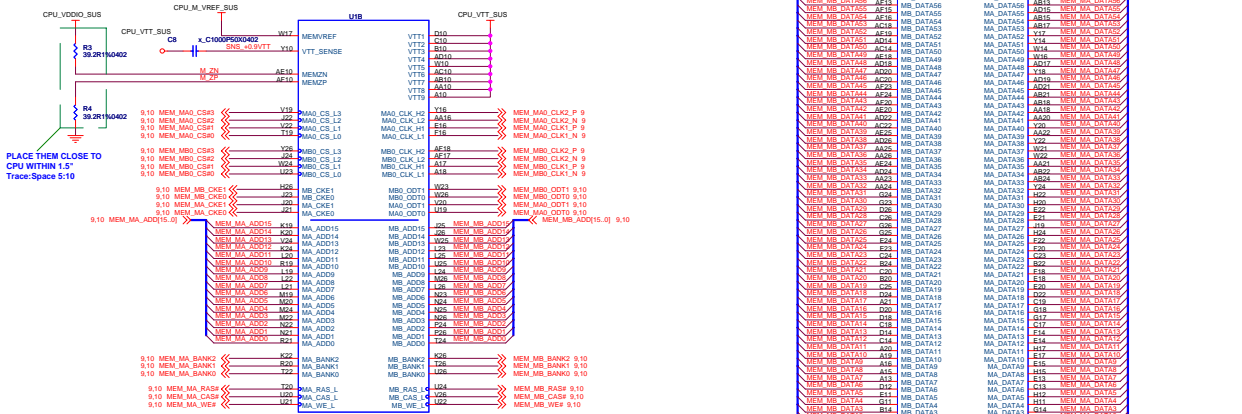
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

Athlon 64 S1
Processor
Socket

		MICRO-STAR INT'L CO.,LTD.	
Title			
SOCKET S1 HT I/F			
Size	Document Number	Rev	
Custom	MS-1634X	0B	
Date:	Thursday, May 31, 2007	Sheet	5 of 51

Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS_POWER SUPPLY THROUGH THE PACKAGE DR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



MSI MICRO-STAR INT'L CO., LTD.

File: **SOCKET S1 DDR2 MEMORY I/F**

Docu: **MS-1634X**

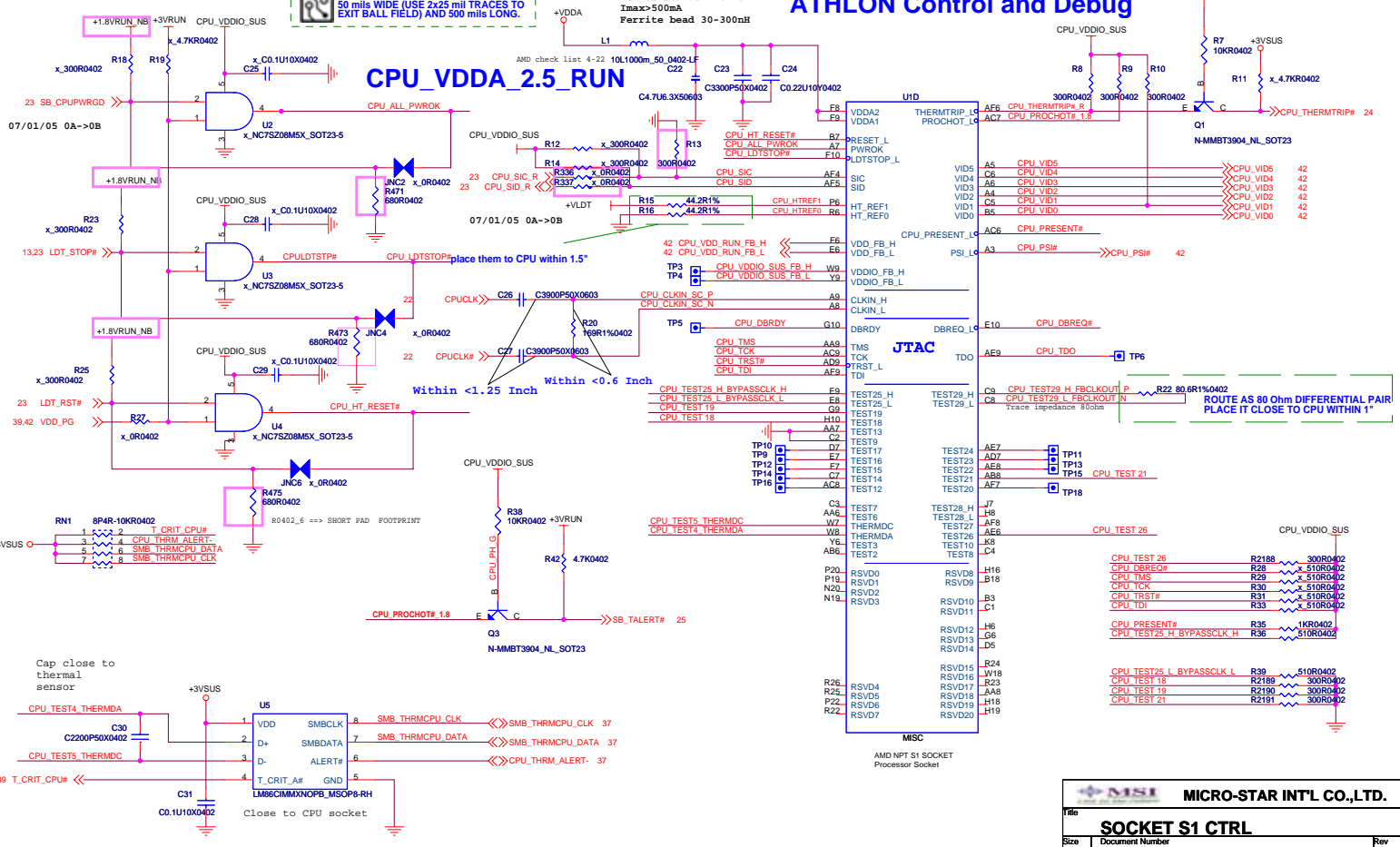
Date: **Thursday, Mar 31, 2005** Page: **6** of **16**

LAYOUT: ROUTE VDDA TRACE APPROX. 80 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

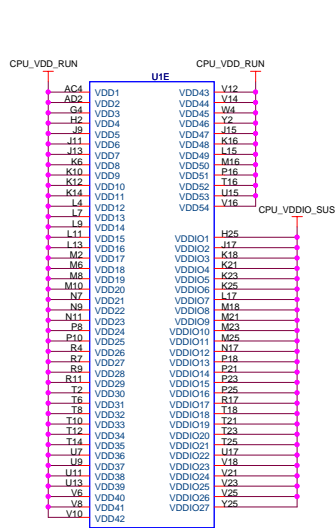
Impedance 35 ohm
DC Resistance <40m ohm
Imax>500mA
Ferrite bead 30-300nH

ATHLON Control and Debug

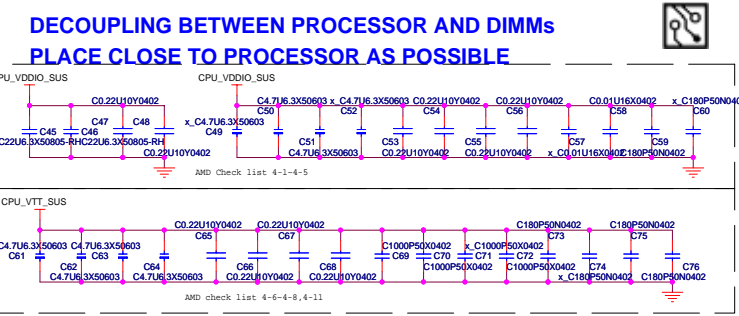
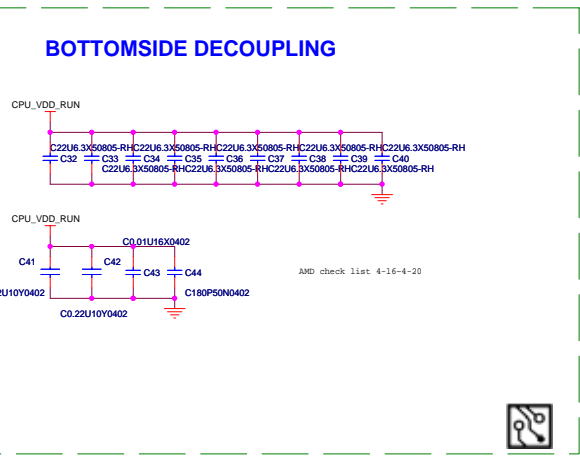
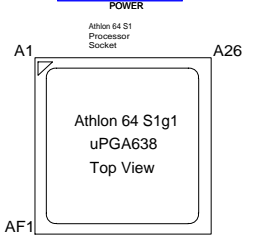
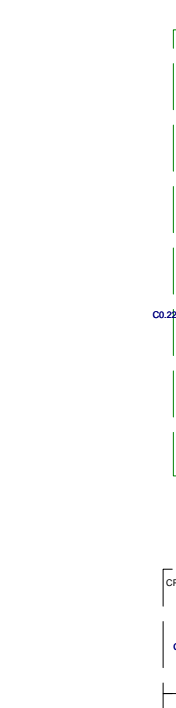
CPU_VDDA_2.5_RUN



MSI MICRO-STAR INTL CO.,LTD.	
File	SOCKET S1 CTRL
Size	Document Number
B	MS-1634X
Date:	Thursday, May 31, 2007
Sheet	7 of 51
Rev	0B



U1E	U1F
AA4	VSS1
AA11	VSS2
AA13	VSS3
AA15	VSS4
AA17	VSS5
AA19	VSS6
AB2	VSS7
AB7	VSS8
AB9	VSS9
AB23	VSS10
AB25	VSS11
AC11	VSS12
AC13	VSS13
AC15	VSS14
AC17	VSS15
AC19	VSS16
AC21	VSS17
AD6	VSS18
AD8	VSS19
AD25	VSS20
AE11	VSS21
AE13	VSS22
AE15	VSS23
AE17	VSS24
AE19	VSS25
AE21	VSS26
AE23	VSS27
B4	VSS28
B6	VSS29
B8	VSS30
B9	VSS31
B11	VSS32
B13	VSS33
B15	VSS34
B17	VSS35
B19	VSS36
B21	VSS37
B23	VSS38
B25	VSS39
D6	VSS40
D8	VSS41
D9	VSS42
D11	VSS43
D13	VSS44
D15	VSS45
D17	VSS46
D19	VSS47
D21	VSS48
D23	VSS49
D25	VSS50
E4	VSS51
F1	VSS52
F11	VSS53
F13	VSS54
F15	VSS55
F17	VSS56
F19	VSS57
F21	VSS58
F23	VSS59
F25	VSS60
H7	VSS61
H9	VSS62
H21	VSS63
H23	VSS64
H4	VSS65



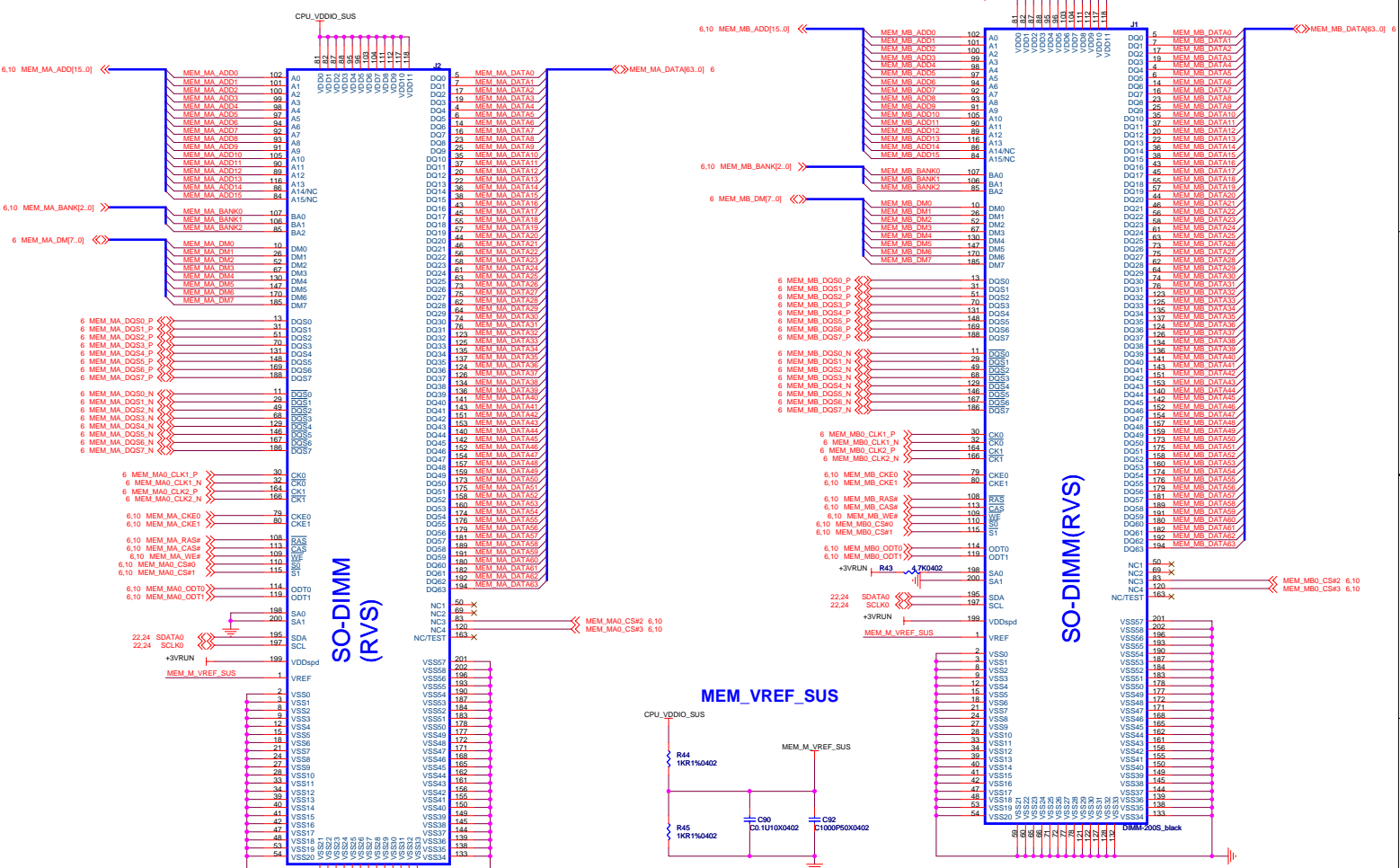
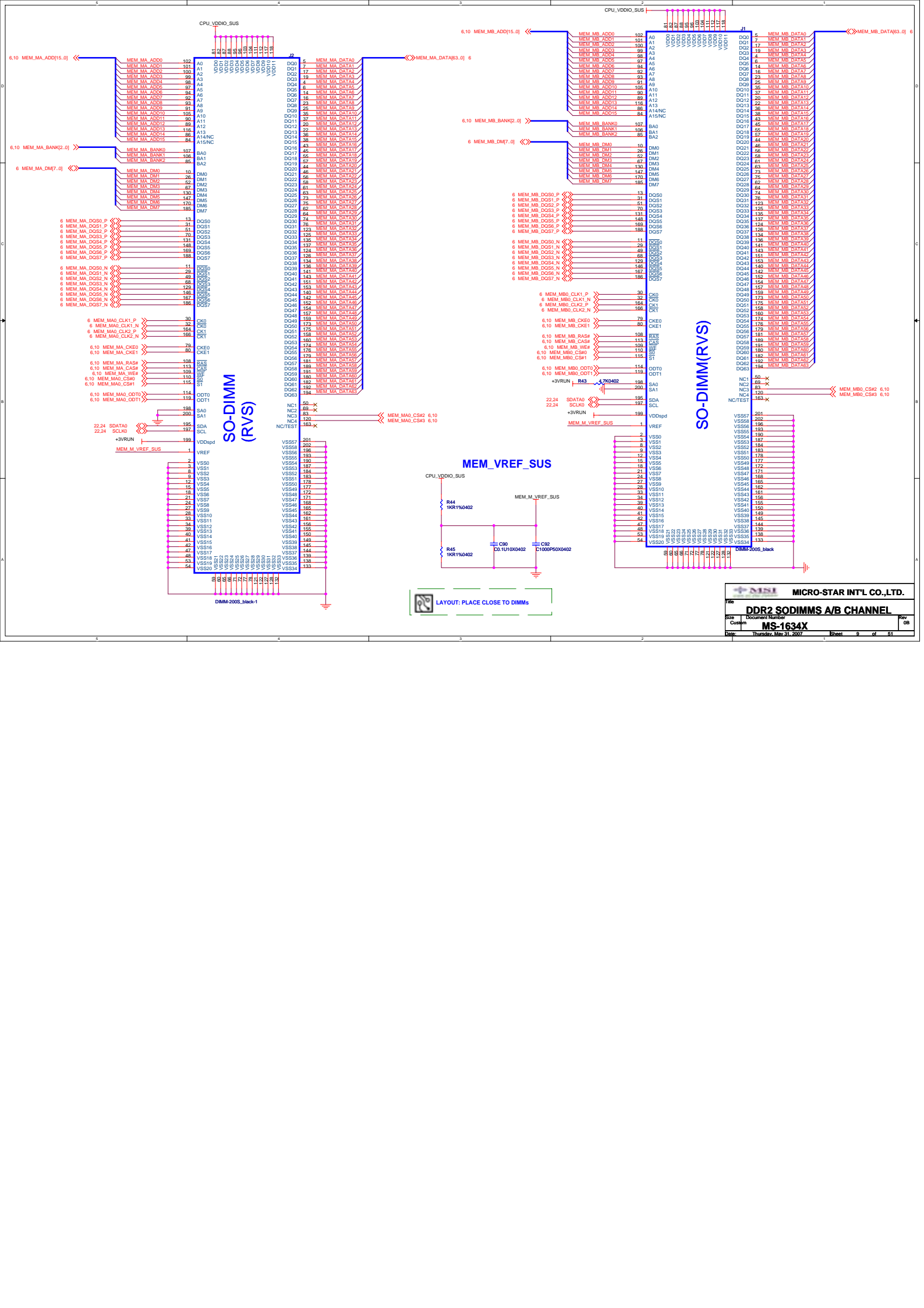
PROCESSOR POWER AND GROUND

MSI MICRO-STAR INT'L CO.,LTD.

File: **SOCKET S1 PWR & GND**

Size B Document Number: **MS-1634X** Rev 0B

Date: Thursday, May 31, 2007 Sheet 8 of 51



LAYOUT: PLACE CLOSE TO DIMMS

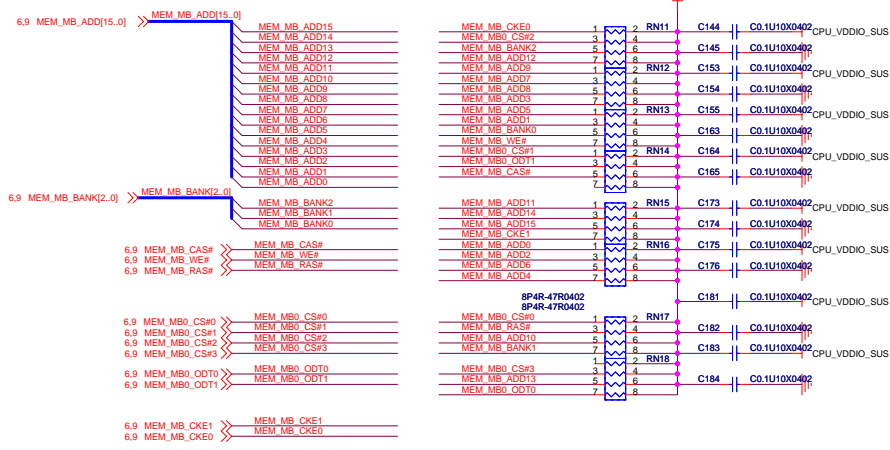
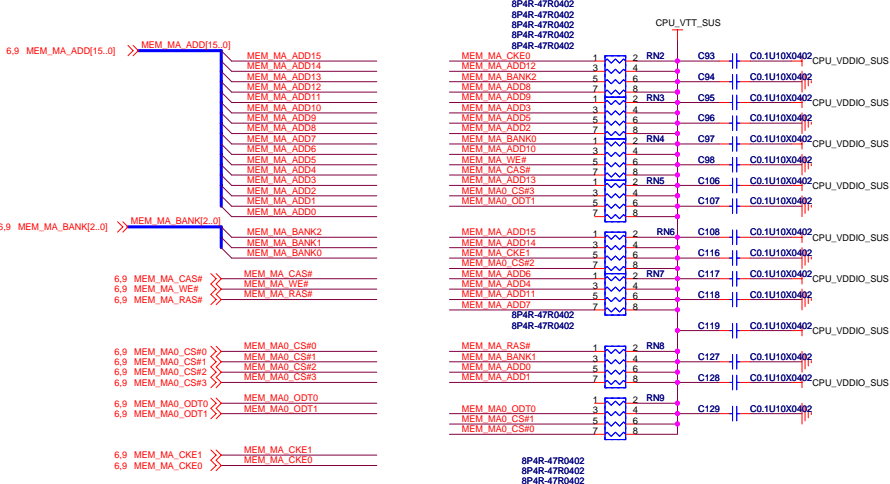
MICRO-STAR INT'L CO., LTD.


Part: **DDR2 SODIMMS A/B CHANNEL**

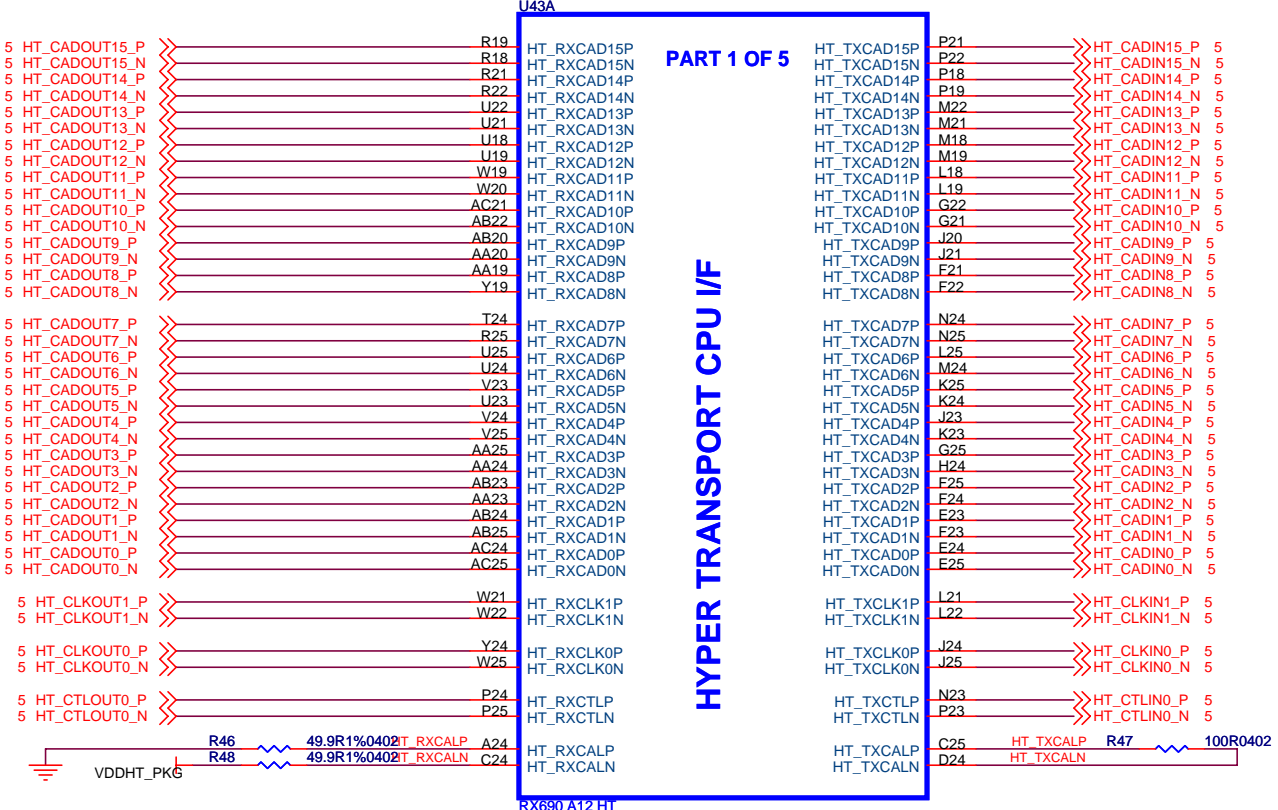
Customer: **MS-1634X**

Date: Thursday, Mar 31, 2007

Sheet: 9 of 91




		MICRO-STAR INT'L CO., LTD.	
DDR2 SODIMMS TERMINATIONS			
Size	Document Number	Rev	
Custom	MS-1634X	06	
Date:	Thursday, May 31, 2007	Sheet	10 of 51

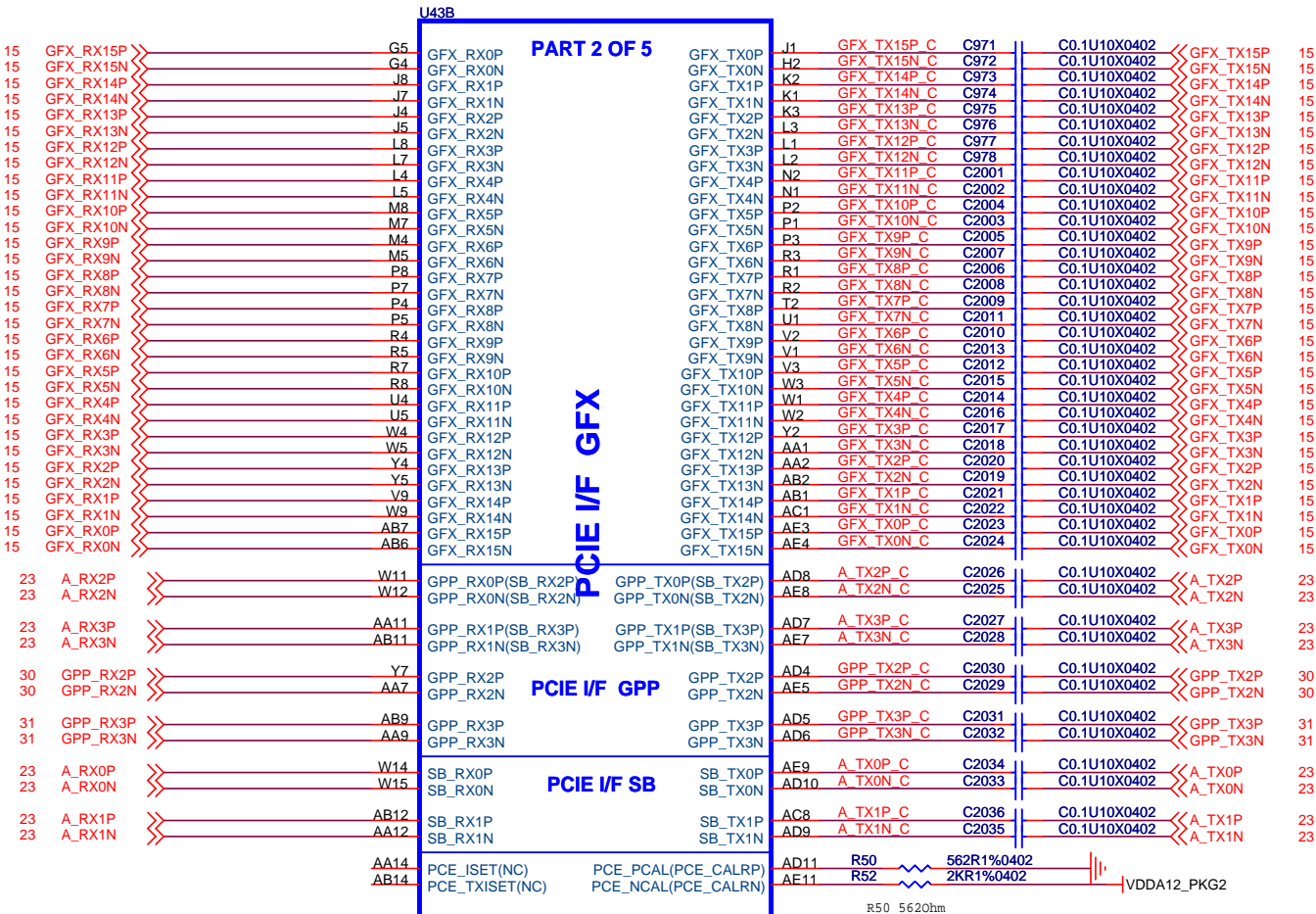


PART 1 OF 5

HYPER TRANSPORT CPU I/F

RX690 A12 HT

 MICRO-STAR INT'L CO.,LTD.	
Title	
RX690 HT LINK I/F	
Size	Document Number
A	MS-1634X
Date:	Thursday, May 31, 2007
Sheet	11 of 51
Rev	0B



RX690 A12 HT

R52 2K0hm

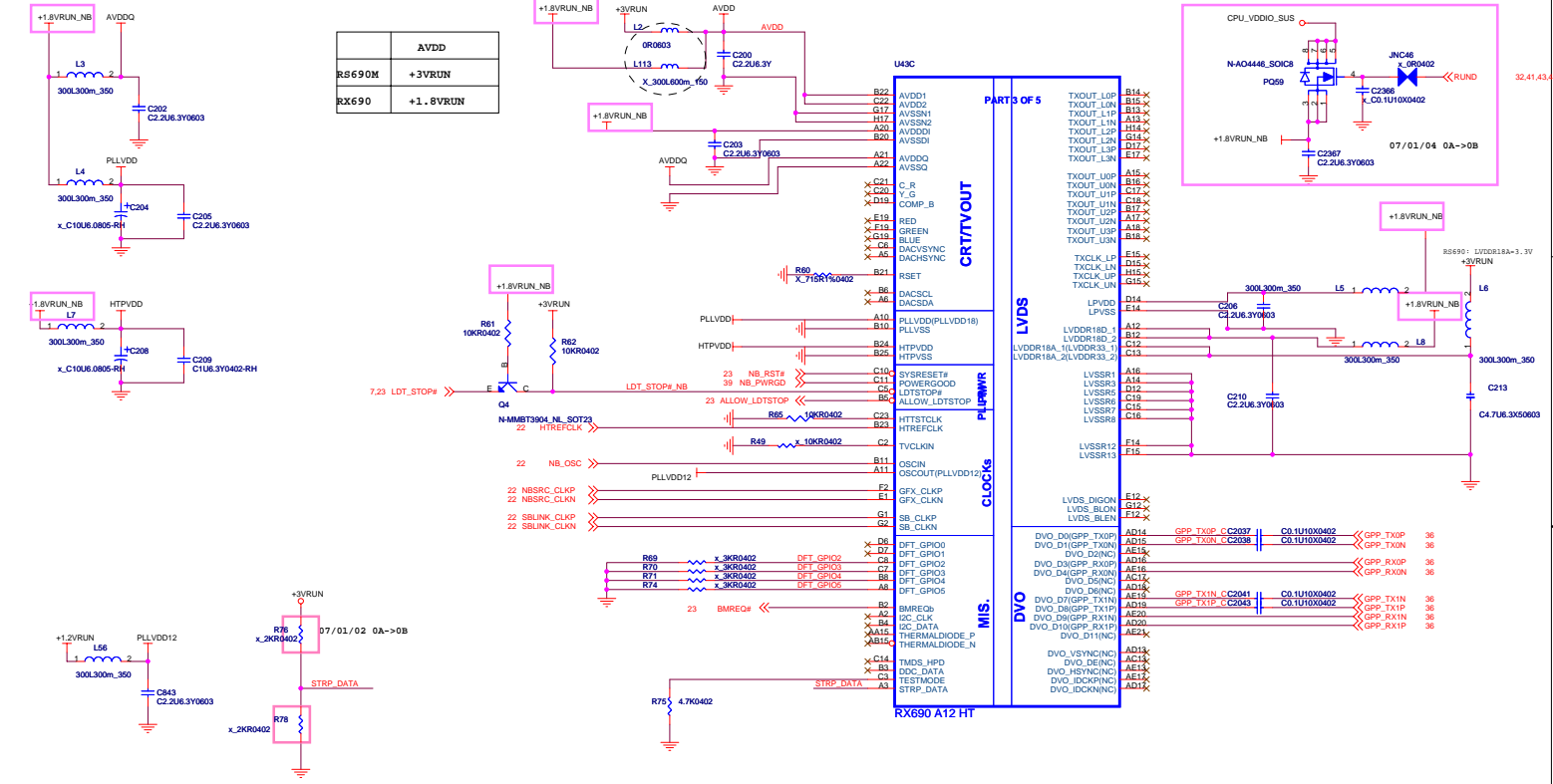
R50 5620hm

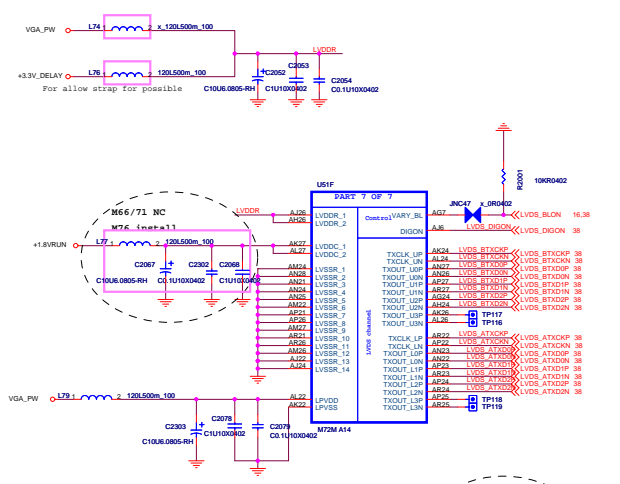
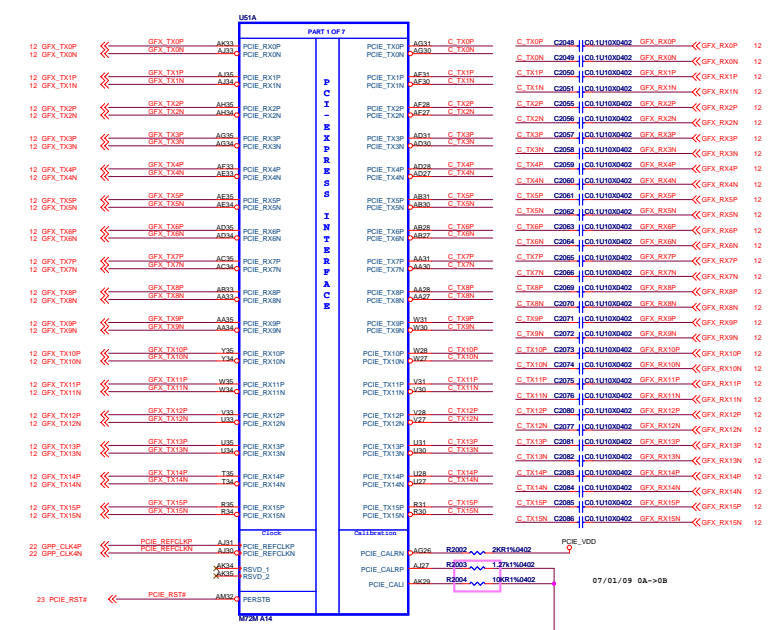
MSI MICRO-STAR INT'L CO.,LTD.

Title: **RX690 PCI-E LINK&HDMI I/F**

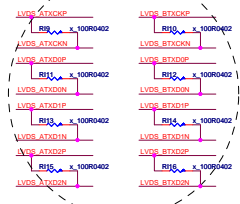
Size A Document Number **MS-1634X** Rev 0B

Date: Thursday, May 31, 2007 Sheet 12 of 51



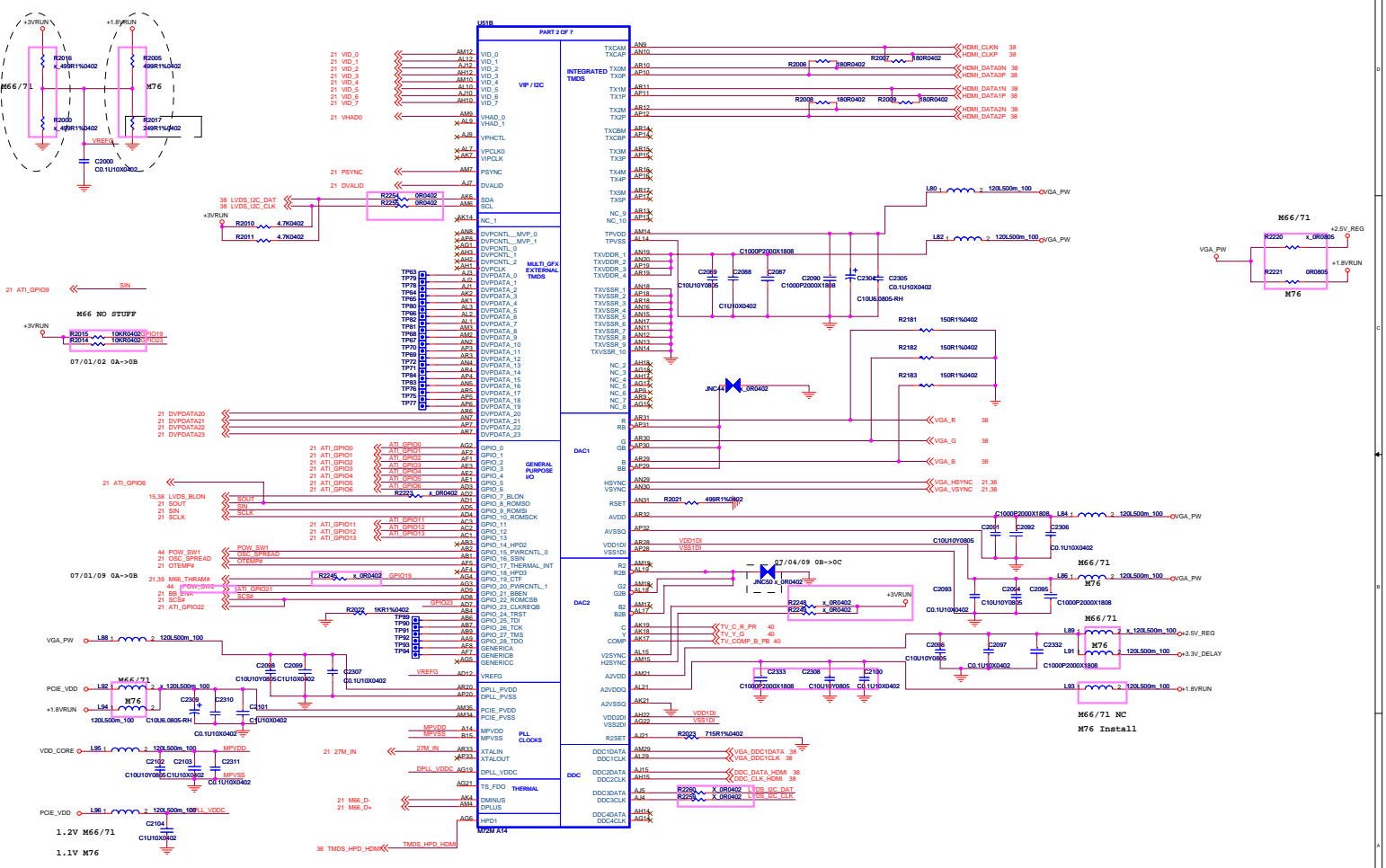


PIN	M72M,M76M	M66M,M71M
LVDD0	LVDD018	LVDD025
LVDDC	LVDDC18	NC
LVDDR	LVDDR36+LPVDD1.8	LVDDR25



PIN	M72M,M76M	M66M,M71M
PCIE_CALRP	27K 1% ± R11-1371212-W08	562 1% ± R11-5620112-W08
PCIE_CALI	10K 1% ± R11-0107112-W05	1.47K 1% ± R11-1471212-W08

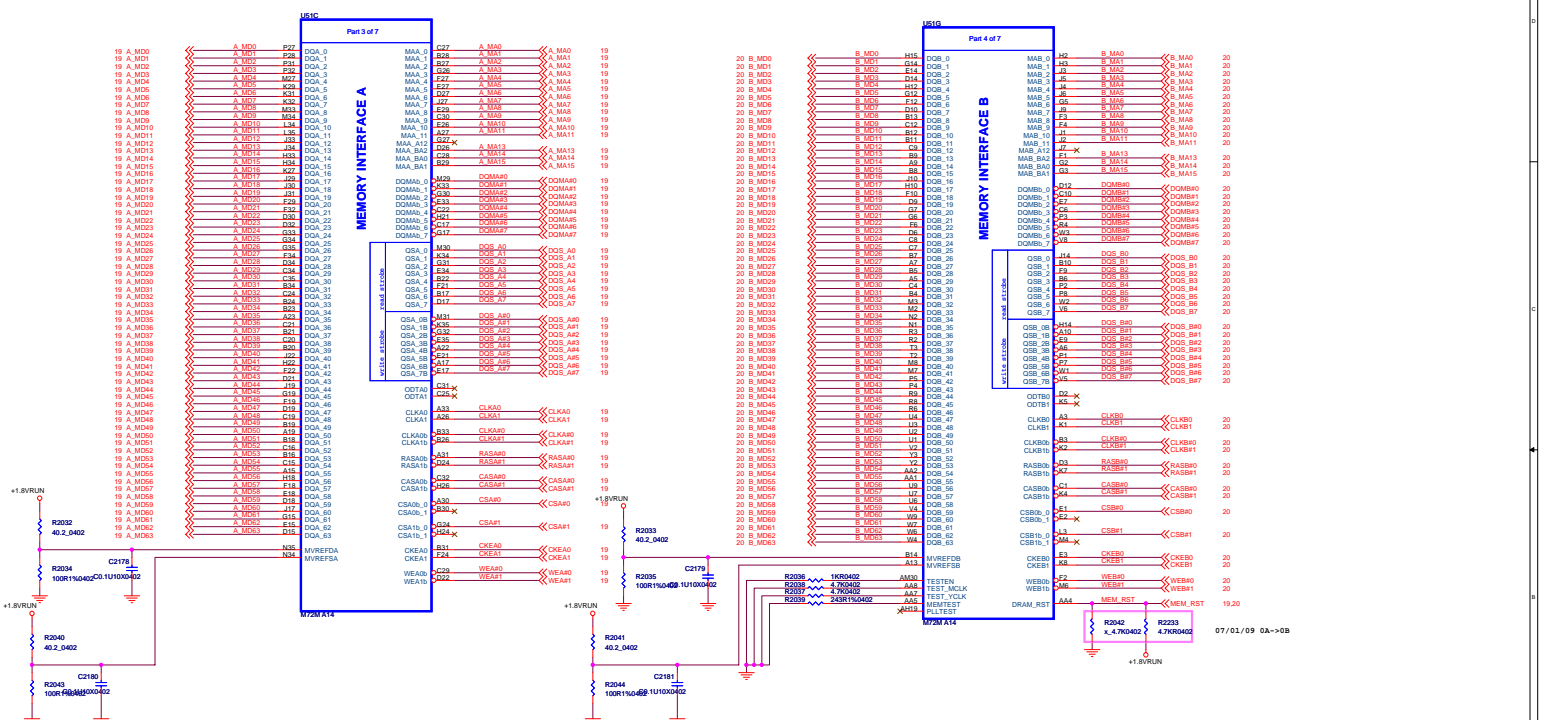
M66/71 3.3V/2+1.65V
M76 1.8V/3+0.6V

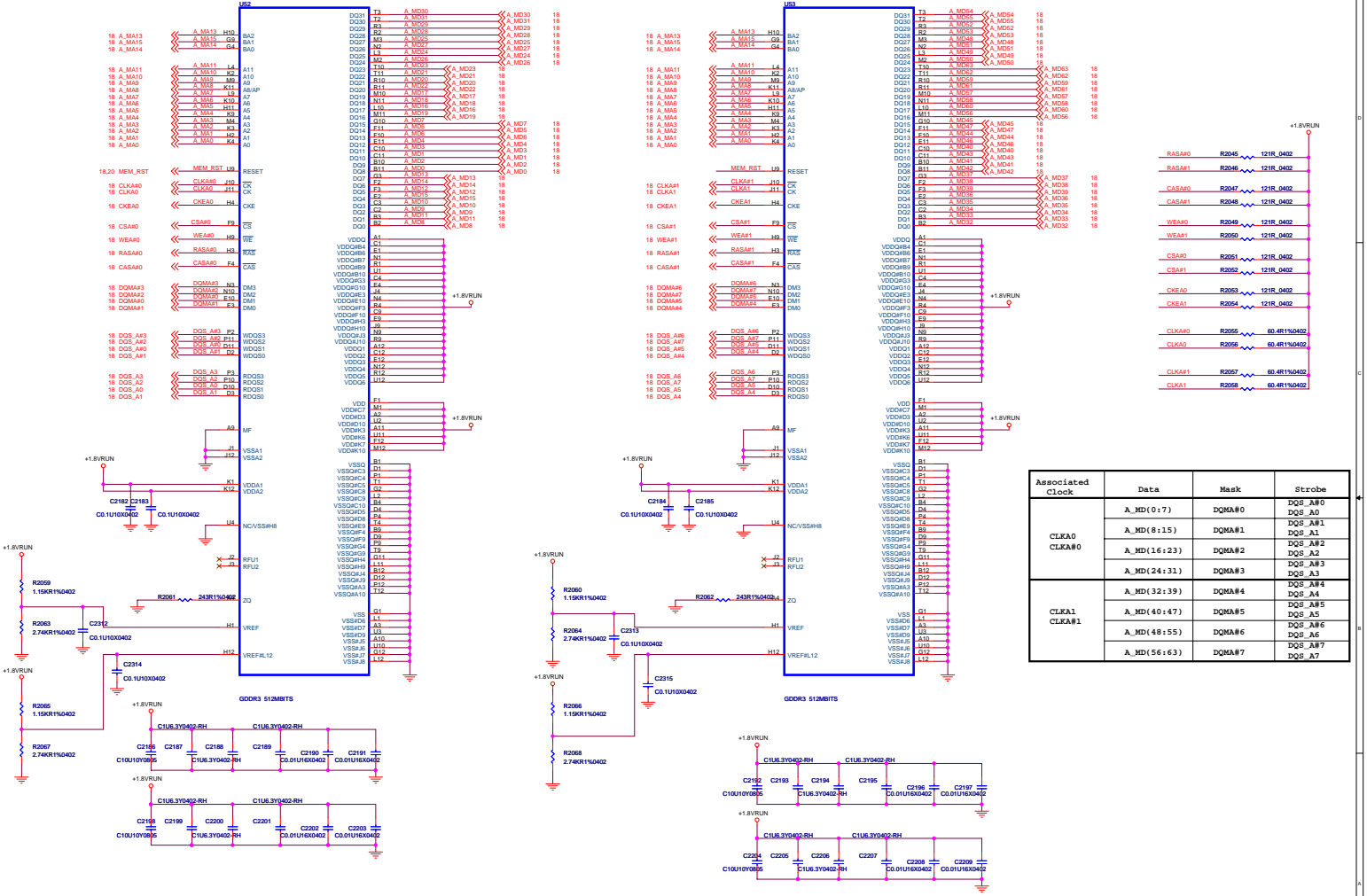


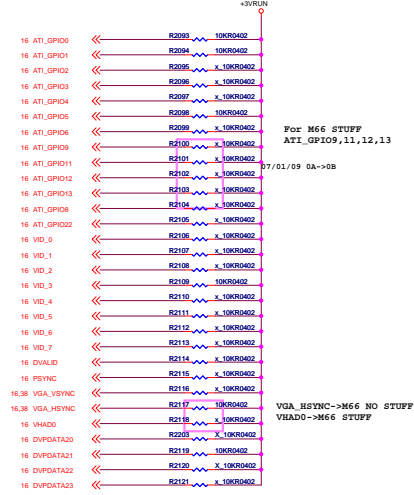
U56

Part 6 of 7

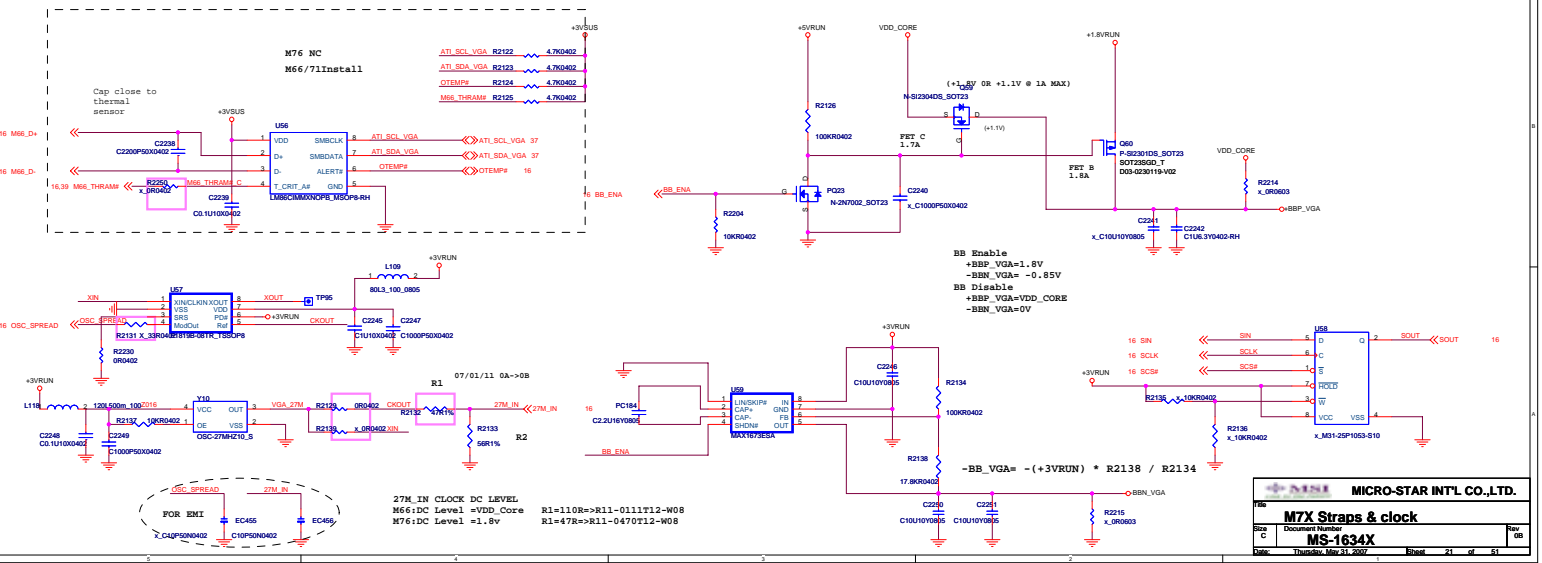
P31	PCIE_VSS_1	VSS_65	L33
P34	PCIE_VSS_2	VSS_66	R1
P37	PCIE_VSS_3	VSS_67	M2
P40	PCIE_VSS_4	VSS_68	M3
P43	PCIE_VSS_5	VSS_69	K28
P46	PCIE_VSS_6	VSS_70	K29
P49	PCIE_VSS_7	VSS_71	N14
P52	PCIE_VSS_8	VSS_72	N15
P55	PCIE_VSS_9	VSS_73	N16
P58	PCIE_VSS_10	VSS_74	N17
P61	PCIE_VSS_11	VSS_75	N18
P64	PCIE_VSS_12	VSS_76	N19
P67	PCIE_VSS_13	VSS_77	R1
P70	PCIE_VSS_14	VSS_78	P12
P73	PCIE_VSS_15	VSS_79	L18
P76	PCIE_VSS_16	VSS_80	M2
P79	PCIE_VSS_17	VSS_81	M3
P82	PCIE_VSS_18	VSS_82	K28
P85	PCIE_VSS_19	VSS_83	K29
P88	PCIE_VSS_20	VSS_84	N14
P91	PCIE_VSS_21	VSS_85	N15
P94	PCIE_VSS_22	VSS_86	N16
P97	PCIE_VSS_23	VSS_87	N17
P100	PCIE_VSS_24	VSS_88	N18
P103	PCIE_VSS_25	VSS_89	N19
P106	PCIE_VSS_26	VSS_90	R1
P109	PCIE_VSS_27	VSS_91	P12
P112	PCIE_VSS_28	VSS_92	L18
P115	PCIE_VSS_29	VSS_93	M2
P118	PCIE_VSS_30	VSS_94	M3
P121	PCIE_VSS_31	VSS_95	K28
P124	PCIE_VSS_32	VSS_96	K29
P127	PCIE_VSS_33	VSS_97	N14
P130	PCIE_VSS_34	VSS_98	N15
P133	PCIE_VSS_35	VSS_99	N16
P136	PCIE_VSS_36	VSS_100	N17
P139	PCIE_VSS_37	VSS_101	N18
P142	PCIE_VSS_38	VSS_102	N19
P145	PCIE_VSS_39	VSS_103	R1
P148	PCIE_VSS_40	VSS_104	P12
P151	PCIE_VSS_41	VSS_105	L18
P154	PCIE_VSS_42	VSS_106	M2
P157	PCIE_VSS_43	VSS_107	M3
P160	PCIE_VSS_44	VSS_108	K28
P163	PCIE_VSS_45	VSS_109	K29
P166	PCIE_VSS_46	VSS_110	N14
P169	PCIE_VSS_47	VSS_111	N15
P172	PCIE_VSS_48	VSS_112	N16
P175	PCIE_VSS_49	VSS_113	N17
P178	PCIE_VSS_50	VSS_114	N18
P181	PCIE_VSS_51	VSS_115	N19
P184	PCIE_VSS_52	VSS_116	R1
P187	PCIE_VSS_53	VSS_117	P12
P190	PCIE_VSS_54	VSS_118	L18
P193	PCIE_VSS_55	VSS_119	M2
P196	PCIE_VSS_56	VSS_120	M3
P199	PCIE_VSS_57	VSS_121	K28
P202	PCIE_VSS_58	VSS_122	K29
P205	PCIE_VSS_59	VSS_123	N14
P208	PCIE_VSS_60	VSS_124	N15
P211	PCIE_VSS_61	VSS_125	N16
P214	PCIE_VSS_62	VSS_126	N17
P217	PCIE_VSS_63	VSS_127	N18
P220	PCIE_VSS_64	VSS_128	N19
P223	PCIE_VSS_65	VSS_129	R1
P226	PCIE_VSS_66	VSS_130	P12
P229	PCIE_VSS_67	VSS_131	L18
P232	PCIE_VSS_68	VSS_132	M2
P235	PCIE_VSS_69	VSS_133	M3
P238	PCIE_VSS_70	VSS_134	K28
P241	PCIE_VSS_71	VSS_135	K29
P244	PCIE_VSS_72	VSS_136	N14
P247	PCIE_VSS_73	VSS_137	N15
P250	PCIE_VSS_74	VSS_138	N16
P253	PCIE_VSS_75	VSS_139	N17
P256	PCIE_VSS_76	VSS_140	N18
P259	PCIE_VSS_77	VSS_141	N19
P262	PCIE_VSS_78	VSS_142	R1
P265	PCIE_VSS_79	VSS_143	P12
P268	PCIE_VSS_80	VSS_144	L18
P271	PCIE_VSS_81	VSS_145	M2
P274	PCIE_VSS_82	VSS_146	M3
P277	PCIE_VSS_83	VSS_147	K28
P280	PCIE_VSS_84	VSS_148	K29
P283	PCIE_VSS_85	VSS_149	N14
P286	PCIE_VSS_86	VSS_150	N15
P289	PCIE_VSS_87	VSS_151	N16
P292	PCIE_VSS_88	VSS_152	N17
P295	PCIE_VSS_89	VSS_153	N18
P298	PCIE_VSS_90	VSS_154	N19
P301	PCIE_VSS_91	VSS_155	R1
P304	PCIE_VSS_92	VSS_156	P12
P307	PCIE_VSS_93	VSS_157	L18
P310	PCIE_VSS_94	VSS_158	M2
P313	PCIE_VSS_95	VSS_159	M3
P316	PCIE_VSS_96	VSS_160	K28
P319	PCIE_VSS_97	VSS_161	K29
P322	PCIE_VSS_98	VSS_162	N14
P325	PCIE_VSS_99	VSS_163	N15
P328	PCIE_VSS_100	VSS_164	N16
P331	PCIE_VSS_101	VSS_165	N17
P334	PCIE_VSS_102	VSS_166	N18
P337	PCIE_VSS_103	VSS_167	N19
P340	PCIE_VSS_104	VSS_168	R1
P343	PCIE_VSS_105	VSS_169	P12
P346	PCIE_VSS_106	VSS_170	L18
P349	PCIE_VSS_107	VSS_171	M2
P352	PCIE_VSS_108	VSS_172	M3
P355	PCIE_VSS_109	VSS_173	K28
P358	PCIE_VSS_110	VSS_174	K29
P361	PCIE_VSS_111	VSS_175	N14
P364	PCIE_VSS_112	VSS_176	N15
P367	PCIE_VSS_113	VSS_177	N16
P370	PCIE_VSS_114	VSS_178	N17
P373	PCIE_VSS_115	VSS_179	N18
P376	PCIE_VSS_116	VSS_180	N19
P379	PCIE_VSS_117	VSS_181	R1
P382	PCIE_VSS_118	VSS_182	P12
P385	PCIE_VSS_119	VSS_183	L18
P388	PCIE_VSS_120	VSS_184	M2
P391	PCIE_VSS_121	VSS_185	M3
P394	PCIE_VSS_122	VSS_186	K28
P397	PCIE_VSS_123	VSS_187	K29
P400	PCIE_VSS_124	VSS_188	N14
P403	PCIE_VSS_125	VSS_189	N15
P406	PCIE_VSS_126	VSS_190	N16
P409	PCIE_VSS_127	VSS_191	N17
P412	PCIE_VSS_128	VSS_192	N18
P415	PCIE_VSS_129	VSS_193	N19
P418	PCIE_VSS_130	VSS_194	R1
P421	PCIE_VSS_131	VSS_195	P12
P424	PCIE_VSS_132	VSS_196	L18
P427	PCIE_VSS_133	VSS_197	M2
P430	PCIE_VSS_134	VSS_198	M3
P433	PCIE_VSS_135	VSS_199	K28
P436	PCIE_VSS_136	VSS_200	K29
P439	PCIE_VSS_137	VSS_201	N14
P442	PCIE_VSS_138	VSS_202	N15
P445	PCIE_VSS_139	VSS_203	N16
P448	PCIE_VSS_140	VSS_204	N17
P451	PCIE_VSS_141	VSS_205	N18
P454	PCIE_VSS_142	VSS_206	N19
P457	PCIE_VSS_143	VSS_207	R1
P460	PCIE_VSS_144	VSS_208	P12
P463	PCIE_VSS_145	VSS_209	L18
P466	PCIE_VSS_146	VSS_210	M2
P469	PCIE_VSS_147	VSS_211	M3
P472	PCIE_VSS_148	VSS_212	K28
P475	PCIE_VSS_149	VSS_213	K29
P478	PCIE_VSS_150	VSS_214	N14
P481	PCIE_VSS_151	VSS_215	N15
P484	PCIE_VSS_152	VSS_216	N16
P487	PCIE_VSS_153	VSS_217	N17
P490	PCIE_VSS_154	VSS_218	N18
P493	PCIE_VSS_155	VSS_219	N19
P496	PCIE_VSS_156	VSS_220	R1
P499	PCIE_VSS_157	VSS_221	P12
P502	PCIE_VSS_158	VSS_222	L18
P505	PCIE_VSS_159	VSS_223	M2
P508	PCIE_VSS_160	VSS_224	M3
P511	PCIE_VSS_161	VSS_225	K28
P514	PCIE_VSS_162	VSS_226	K29
P517	PCIE_VSS_163	VSS_227	N14
P520	PCIE_VSS_164	VSS_228	N15
P523	PCIE_VSS_165	VSS_229	N16
P526	PCIE_VSS_166	VSS_230	N17
P529	PCIE_VSS_167	VSS_231	N18
P532	PCIE_VSS_168	VSS_232	N19
P535	PCIE_VSS_169	VSS_233	R1
P538	PCIE_VSS_170	VSS_234	P12
P541	PCIE_VSS_171	VSS_235	L18
P544	PCIE_VSS_172	VSS_236	M2
P547	PCIE_VSS_173	VSS_237	M3
P550	PCIE_VSS_174	VSS_238	K28
P553	PCIE_VSS_175	VSS_239	K29
P556	PCIE_VSS_176	VSS_240	N14
P559	PCIE_VSS_177	VSS_241	N15
P562	PCIE_VSS_178	VSS_242	N16
P565	PCIE_VSS_179	VSS_243	N17
P568	PCIE_VSS_180	VSS_244	N18
P571	PCIE_VSS_181	VSS_245	N19
P574	PCIE_VSS_182	VSS_246	R1
P577	PCIE_VSS_183	VSS_247	P12
P580	PCIE_VSS_184	VSS_248	L18
P583	PCIE_VSS_185	VSS_249	M2
P586	PCIE_VSS_186	VSS_250	M3
P589	PCIE_VSS_187	VSS_251	K28
P592	PCIE_VSS_188	VSS_252	K29
P595	PCIE_VSS_189	VSS_253	N14
P598	PCIE_VSS_190	VSS_254	N15
P601	PCIE_VSS_191	VSS_255	N16
P604	PCIE_VSS_192	VSS_256	N17
P607	PCIE_VSS_193	VSS_257	N18
P610	PCIE_VSS_194	VSS_258	N19
P613	PCIE_VSS_195	VSS_259	R1
P616	PCIE_VSS_196	VSS_260	P12
P619	PCIE_VSS_197	VSS_261	L18
P622	PCIE_VSS_198	VSS_262	M2
P625	PCIE_VSS_199	VSS_263	M3
P628	PCIE_VSS_200	VSS_264	K28
P631	PCIE_VSS_201	VSS_265	K29
P634	PCIE_VSS_202	VSS_266	N14
P637	PCIE_VSS_203	VSS_267	N15
P640	PCIE_VSS_204	VSS_268	N16
P643	PCIE_VSS_205	VSS_269	N17
P646	PCIE_VSS_206	VSS_270	N18
P649	PCIE_VSS_207	VSS_271	N19
P652	PCIE_VSS_208	VSS_272	R1
P655	PCIE_VSS_209	VSS_273	P12
P658	PCIE_VSS_210	VSS_274	L18
P661	PCIE_VSS_211	VSS_275	M2
P664	PCIE_VSS_212	VSS_276	M3
P667	PCIE_VSS_213	VSS_277	K28
P670	PCIE_VSS_214	VSS_278	K29
P673	PCIE_VSS_215	VSS_279	N14
P676	PCIE_VSS_216	VSS_280	N15
P679	PCIE_VSS_217	VSS_281	N16
P682	PCIE_VSS_218	VSS_282	N17
P685	PCIE_VSS_219	VSS_283	N18
P688	PCIE_VSS_220	VSS_284	N19
P691	PCIE_VSS_221	VSS_285	R1
P694	PCIE_VSS_222	VSS_286	P12
P697	PCIE_VSS_223	VSS_287	L18
P700	PCIE_VSS_224	VSS_288	M2
P703	PCIE_VSS_225	VSS_289	M3
P706	PCIE_VSS_226	VSS_290	K28
P709	PCIE_VSS_227	VSS_291	K29
P712	PCIE_VSS_228	VSS_292	N14
P715	PCIE_VSS_229	VSS_293	N15
P718	PCIE_VSS_230	VSS_294	N16
P721	PCIE_VSS_231	VSS_295	N17
P724	PCIE_VSS_232	VSS_296	N18
P727	PCIE_VSS_233	VSS_297	N19
P730	PCIE_VSS_234	VSS_298	R1
P733	PCIE_VSS_235	VSS_299	P12
P736	PCIE_VSS_236	VSS_300	L18
P739	PCIE_VSS_237	VSS_301	M2
P742	PCIE_VSS_238	VSS_302	M3
P745	PCIE_VSS_239	VSS_303	K28
P748	PCIE_VSS_240	VSS_304	K29
P751	PCIE_VSS_241	VSS_305	N14
P754	PCIE_VSS_242	VSS_306	N15
P757	PCIE_VSS_243	VSS_307	N16
P760	PCIE_VSS_244	VSS_308	N17
P763	PCIE_VSS_245	VSS_309	N18
P766	PCIE_VSS_246	VSS_310	N19
P769	PCIE_VSS_247	VSS_311	R1
P772	PCIE_VSS_248	VSS_312	P12
P775	PCIE_VSS_249	VSS_313	L18
P778	PCIE_VSS_250	VSS_314	M2
P781	PCIE_VSS_251	VSS_315	M3
P784	PCIE_VSS_252	VSS_316	K28
P787	PCIE_VSS_253	VSS_317	K29
P790	PCIE_VSS_254	VSS_318	N14
P793	PCIE_VSS_255	VSS_319	N15
P796	PCIE_VSS_256	VSS_320	N16
P799	PCIE_VSS_257	VSS_321	N17
P802	PCIE_VSS_258	VSS_322	N18
P805	PCIE_VSS_259	VSS_323	N19
P808	PCIE_VSS_260	VSS_324	R1
P811	PCIE_VSS_261	VSS_325	P12
P814	PCIE_VSS_262	VSS_326	L18
P817	PCIE_VSS_263	VSS_327	M2
P820	PCIE_VSS_264	VSS_328	M3
P823	PCIE_VSS_265	VSS_329	K28
P826	PCIE_VSS_266	VSS_330	K29
P829	PCIE_VSS_267	VSS_331	N14
P832	PCIE_VSS_268	VSS_332	N15
P835	PCIE_VSS_269	VSS_333	N16
P838	PCIE_VSS_270	VSS_334	N17
P841	PCIE_VSS_271	VSS_335	N18
P844	PCIE_VSS_272	VSS_336	N19
P847	PCIE_VSS_273	VSS_337	R1
P850	PCIE_VSS_274	VSS_338	P12
P853	PCIE_VSS_275	VSS_339	L18
P856	PCIE_VSS_276	VSS_340	M2
P859	PCIE_VSS_277	VSS_341	M3
P862	PCIE_VSS_278	VSS_342	K28
P865	PCIE_VSS_279	VSS_343	K29
P868	PCIE_VSS_280	VSS_344	N14
P871	PCIE_VSS_281	VSS_345	N15
P874	PCIE_VSS_282	VSS_346	N16
P877	PCIE_VSS_283	VSS_347	N17
P880	PCIE_VSS_284	VSS_348	N18
P883	PCIE_VSS_285	VSS_349	N19
P886	PCIE_VSS_286	VSS_350	R1
P889	PCIE_VSS_287	VSS_351	P12
P892	PCIE_VSS_288	VSS_352	L18
P895	PCIE_VSS_289	VSS_353	M2
P898	PCIE_VSS_290	VSS_354	M3
P901	PCIE_VSS_291	VSS_355	K28
P904	PCIE_VSS_292	VSS_356	K29

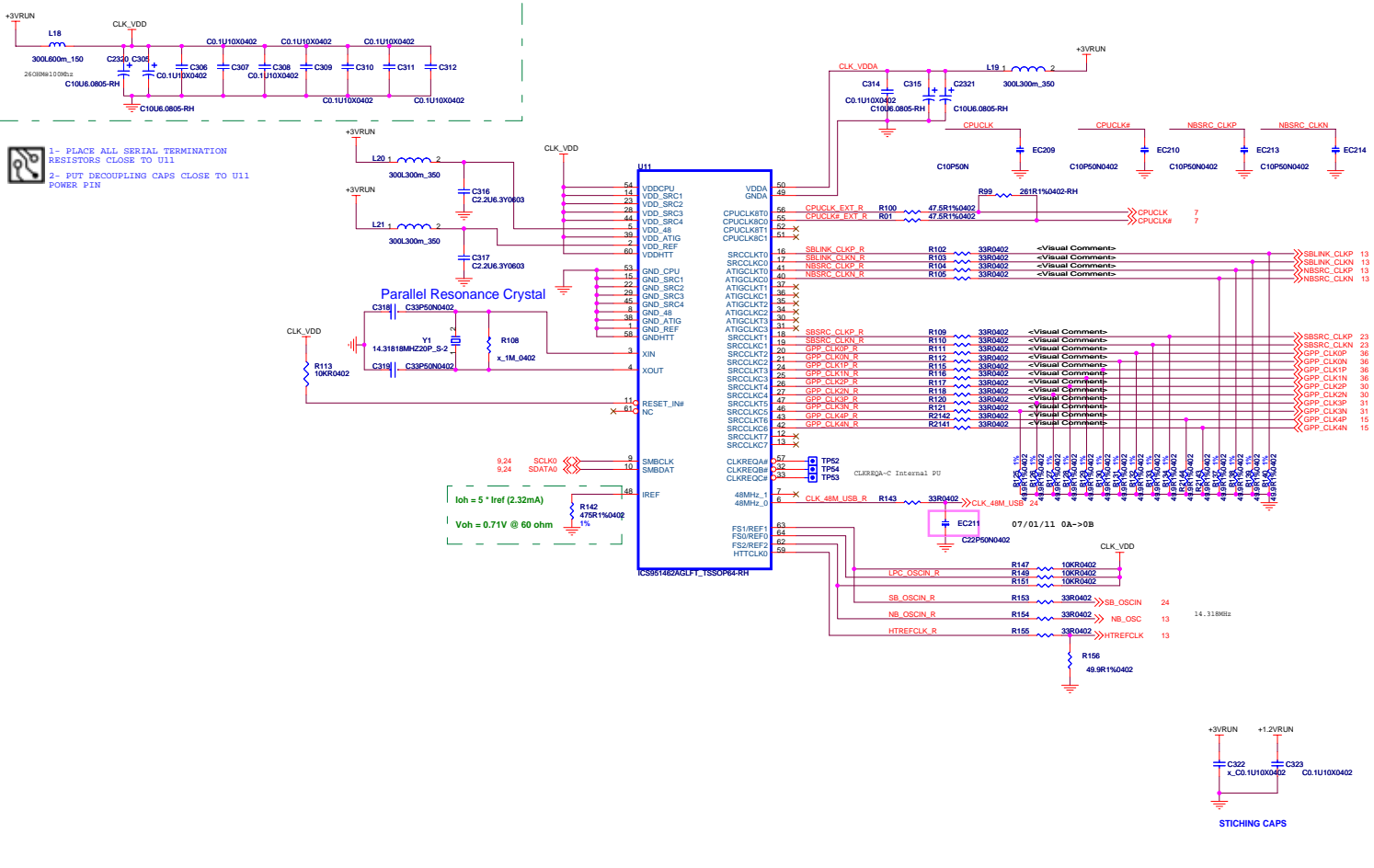






CONFIGURATION STRAPS			RECOMMENDED SETTINGS	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M66M,M71M	
			M72M,M76M	
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0	0
PLL_IBIAS_RD_1	GPIO6	(M66/71)BIAS CURRENT FOR PCIE PHY PLL MSBIT (M72/76)RSVD	0	0
PLL_IBIAS_RD_0	GPIO5	(M66/71)BIAS CURRENT FOR PCIE PHY PLL MSBIT (M72/76)RSVD	1	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13,11,19]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX XX	XX XX
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	X	X
BIF_VGA_DIS	PSYNC	VGA ENABLED	NA	0
MEM_TYPE	UNUSED DVDPDATA [23.22.21.20]	MEMORY TYPE,MAKE AND SIZE INFO	XXXX	XXXX
Samsung		GPU Ver .A14 K4J52324QC-BC14->M12-K4J5285-S02	1000	0001
Infineon		HYB18H512321BF-14->M12-18H5185-Q16 GPU Ver.A15	0010	0010 1001 1010



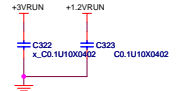


- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U11 POWER PIN
- 2- PUT DECOUPLING CAPS CLOSE TO U11

$I_{oh} = 5 \cdot I_{ref} (2.32mA)$
 $V_{oh} = 0.71V @ 60 \text{ ohm}$

MICRO-STAR INT'L CO., LTD.
 File: **CLOCK GENERATOR**
 Size: **MS-1634X**
 Date: Thursday, Mar 31, 2007

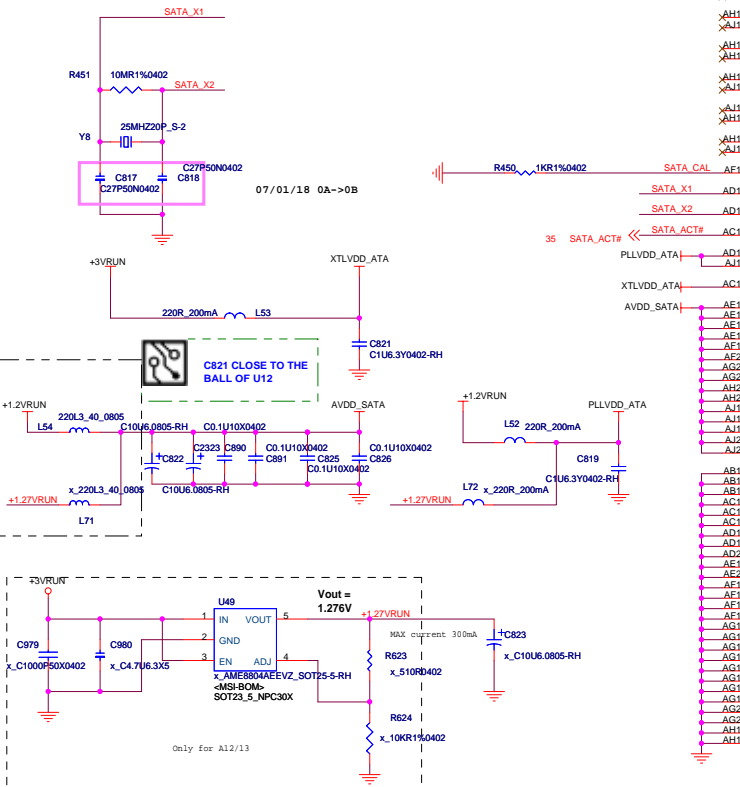
STITCHING CAPS



35 SATA_TX0+ C << SATA_TX0+ C C812 C0.01U16X0402 SATA_TX0+ AH21
 35 SATA_TX0- C << SATA_TX0- C C813 C0.01U16X0402 SATA_TX0- AJ21
 35 SATA_RX0+ C << SATA_RX0+ C C814 C0.01U16X0402 SATA_RX0+ AH20
 35 SATA_RX0- C << SATA_RX0- C C815 C0.01U16X0402 SATA_RX0+ AJ20

U48
 AH18 SATA_TX1+
 AJ18 SATA_TX1-
 AH17 SATA_RX1+
 AJ17 SATA_RX1-
 AH13 SATA_TX2+
 AJ13 SATA_TX2-
 AH16 SATA_RX2+
 AJ16 SATA_RX2-
 AH11 SATA_TX3+
 AJ11 SATA_TX3-
 AH13 SATA_RX3+
 AJ13 SATA_RX3-
 SATA_CAL AF12
 SATA_X1 AD16
 SATA_X2 AD18
 SATA_ACT# AC12
 PLLVDD_ATA# AD14
 PLLVDD_SATA_1 AJ10
 PLLVDD_SATA_2 AJ10
 XTLLVDD_ATA# AC16
 XTLLVDD_SATA_1 AE18
 XTLLVDD_SATA_2 AE18
 AVDD_SATA_1 AE19
 AVDD_SATA_2 AE19
 AVDD_SATA_3 AE19
 AVDD_SATA_4 AE19
 AVDD_SATA_5 AE19
 AVDD_SATA_6 AE19
 AVDD_SATA_7 AE19
 AVDD_SATA_8 AE19
 AVDD_SATA_9 AE19
 AVDD_SATA_10 AE19
 AVDD_SATA_11 AE19
 AVDD_SATA_12 AE19
 AVDD_SATA_13 AE19
 AVDD_SATA_14 AE19
 AVDD_SATA_15 AE19
 AVSS_SATA_1 AB14
 AVSS_SATA_2 AB16
 AVSS_SATA_3 AB18
 AVSS_SATA_4 AB18
 AVSS_SATA_5 AB18
 AVSS_SATA_6 AB18
 AVSS_SATA_7 AB18
 AVSS_SATA_8 AB18
 AVSS_SATA_9 AE12
 AVSS_SATA_10 AE12
 AVSS_SATA_11 AE11
 AVSS_SATA_12 AE11
 AVSS_SATA_13 AE14
 AVSS_SATA_14 AE18
 AVSS_SATA_15 AE18
 AVSS_SATA_16 AG11
 AVSS_SATA_17 AG12
 AVSS_SATA_18 AG13
 AVSS_SATA_19 AG14
 AVSS_SATA_20 AG16
 AVSS_SATA_21 AG17
 AVSS_SATA_22 AG18
 AVSS_SATA_23 AG19
 AVSS_SATA_24 AG20
 AVSS_SATA_25 AH10
 AVSS_SATA_26 AH10
 AVSS_SATA_27 AH19

SB600 SB 23x23mm
 Part 2 of 4
 IDE_IORDY# AB29 << IDE_IORDY# 35
 IDE_IRQ AA28 << IDE_IRQ 35
 IDE_A0 AB29 << IDE_A0 35
 IDE_A1 AB27 << IDE_A1 35
 IDE_A2 Y28 << IDE_A2 35
 IDE_DACK# AB29 << IDE_DACK# 35
 IDE_DRQ AC27 << IDE_DRQ 35
 IDE_IOR# AC28 << IDE_IOR# 35
 IDE_IOW# AC28 << IDE_IOW# 35
 IDE_CS1# W28 << IDE_CS1# 35
 IDE_CS3# W27 << IDE_CS3# 35
 IDE_D0 AD28 << IDE_D0 35
 IDE_D1 AD28 << IDE_D1 35
 IDE_D2 AE29 << IDE_D2 35
 IDE_D3 AF27 << IDE_D3 35
 IDE_D4 AG29 << IDE_D4 35
 IDE_D5 AH28 << IDE_D5 35
 IDE_D6 AJ28 << IDE_D6 35
 IDE_D7 AJ27 << IDE_D7 35
 IDE_D8 AH27 << IDE_D8 35
 IDE_D9 AG29 << IDE_D9 35
 IDE_D10 AF28 << IDE_D10 35
 IDE_D11 AE29 << IDE_D11 35
 IDE_D12 AF28 << IDE_D12 35
 IDE_D13 AE29 << IDE_D13 35
 IDE_D14 AD29 << IDE_D14 35
 IDE_D15 AD29 << IDE_D15 35
 IDE_D15_01 << IDE_D(15_0) 35
 SPI_DI#GPI012 J3 x
 SPI_DQ#GPI011 C3 x
 SPI_CLK#GPI047 C3 x
 SPI_HOLD#GPI031 C6 x
 SPI_CS#GPI032 C6 x
 LAN_RST#GPI013 M4 x
 ROM_RST#GPI014 M4 x
 FANOUT0#GPI03 T3 x
 FANOUT1#GPI048 T4 x
 FANOUT2#GPI049 T4 x
 FANIN0#GPI050 N3 x
 FANIN1#GPI051 N3 x
 FANIN2#GPI052 N3 x
 TEMP_COMM P5 x
 TEMPIN#GPI061 P7 x
 TEMPIN1#GPI062 P8 x
 TEMPIN2#GPI063 P8 x
 EMPIN#GPI064 T7 x
 VINO#GPI053 L5 x
 VIN1#GPI054 L7 x
 VIN2#GPI055 MR x
 VIN3#GPI056 Y6 x
 VIN4#GPI057 Y6 x
 VIN5#GPI058 PM x
 VIN6#GPI059 M2 x
 VIN7#GPI060 V7 x
 AVDD N1
 AVSS M1



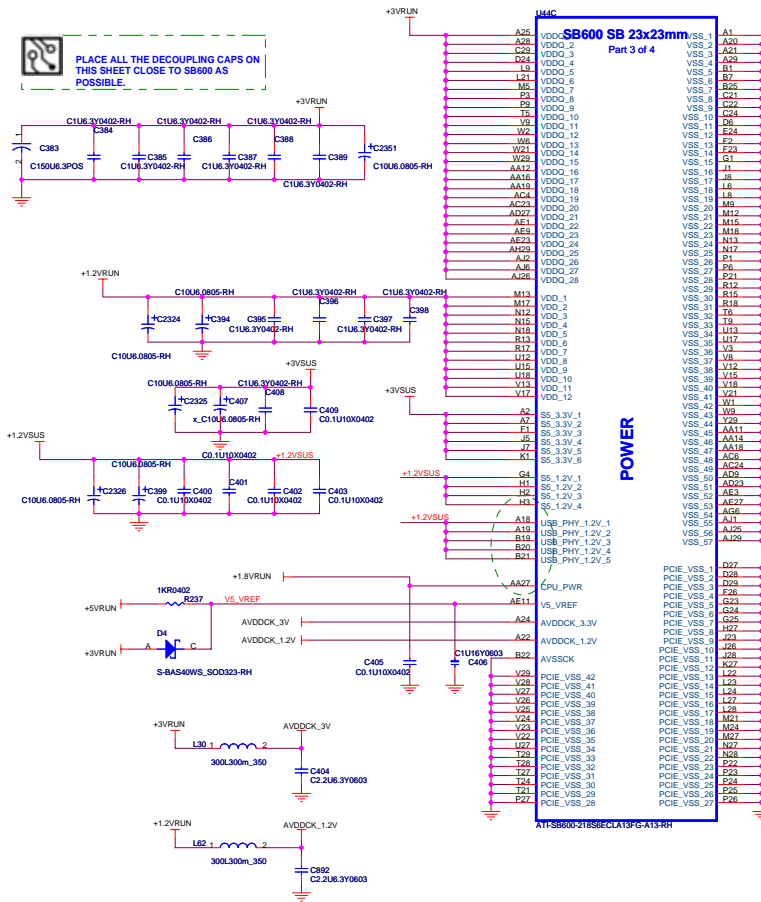
MSI MICRO-STAR INT'L CO., LTD.

File: **SB600 SATA/IDE/HWM/SPI**

Size: B Document Number: **MS-1634X** Rev: 08

Date: Thursday, May 31, 2007 Sheet 25 of 51

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB600 AS POSSIBLE.



MICRO-STAR INT'L CO.,LTD.

File: **SB600 POWER & GND**

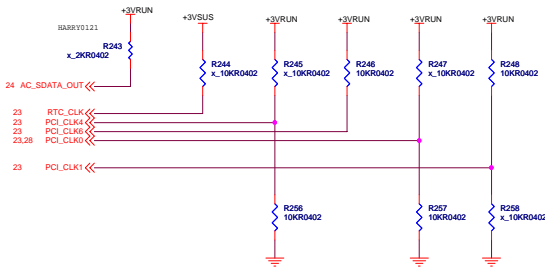
Size: **MS-1634X**

Date: Thursday, Mar 31, 2007

Sheet: 26 of 51

REQUIRED STRAPS

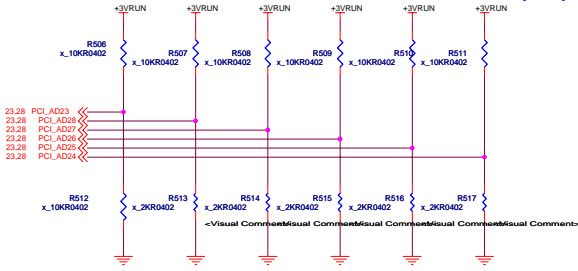
NPTE: FOR SB460, EXTERNAL PU/PD ARE REQUIRED



SB600						
	AC_SDOOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT	

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[31:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	Bootfall timer disable default default
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Bootfall timer enable

MICRO-STAR INT'L CO.,LTD.

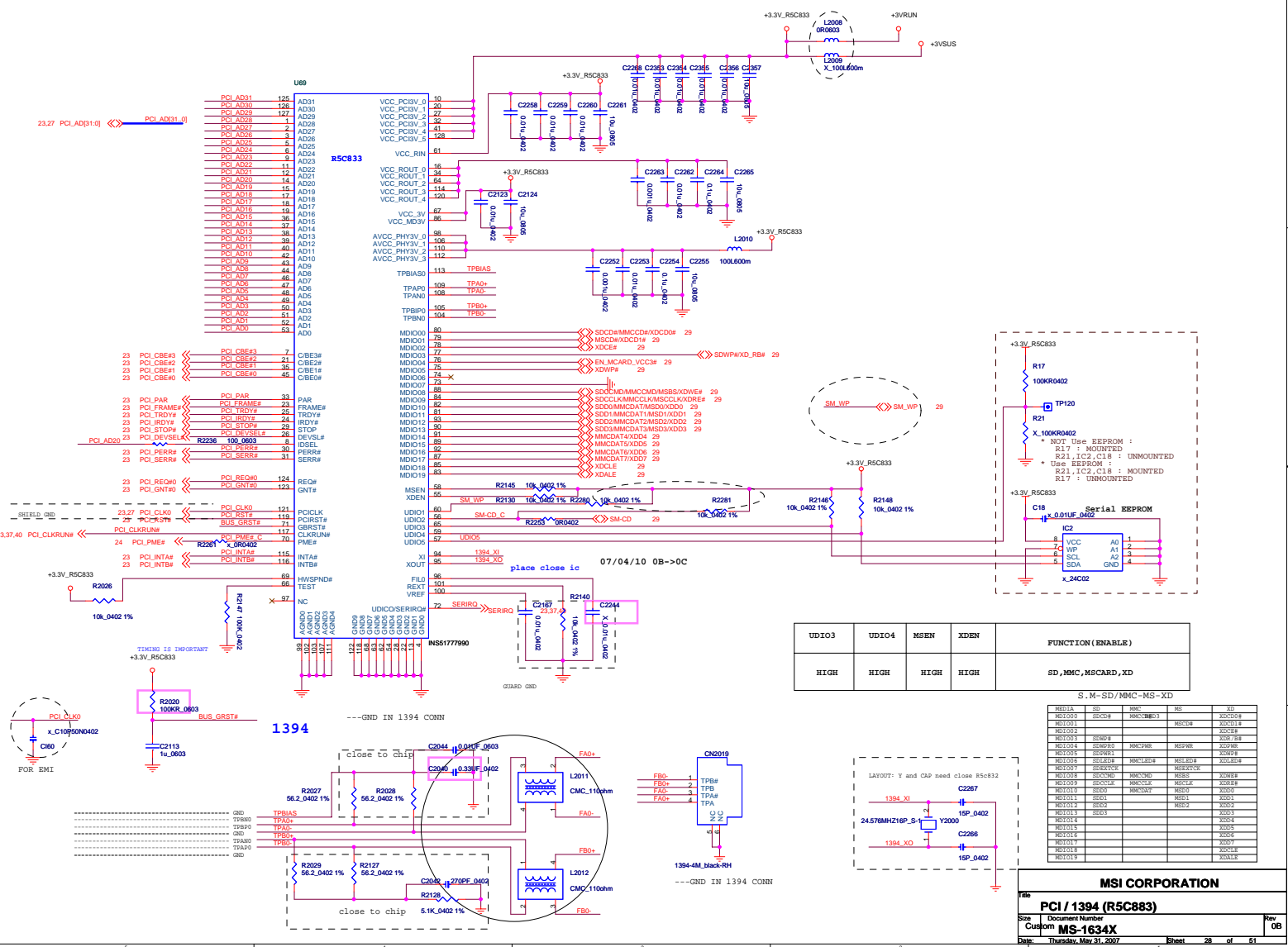
File: **SB600 STRAPS**

Size: Custom Document Number

Date: Thursday, Mar 31, 2007

Sheet 27 of 51

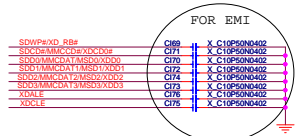
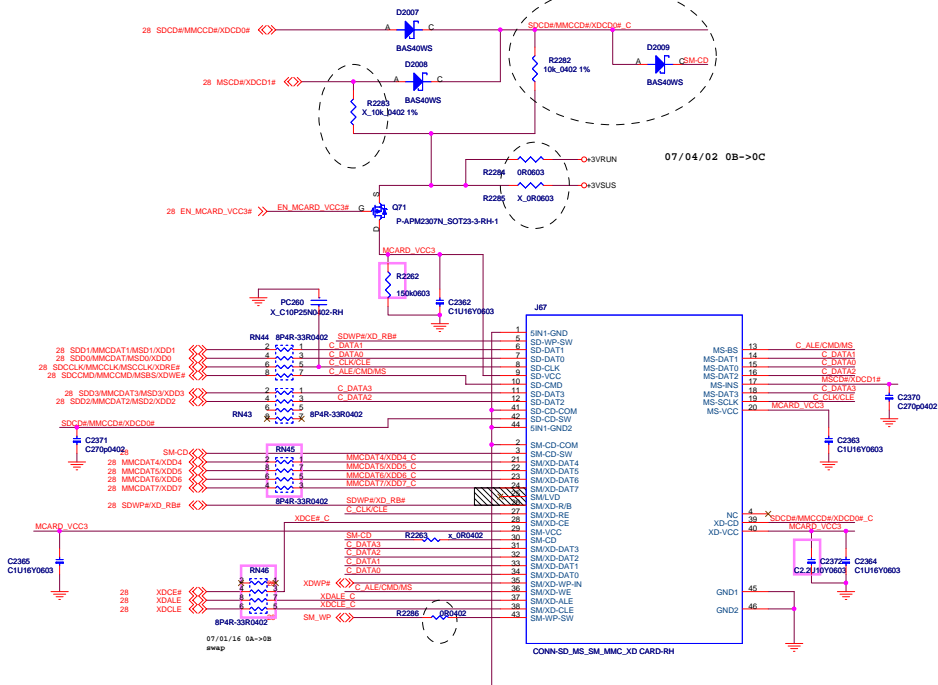
Rev 0B



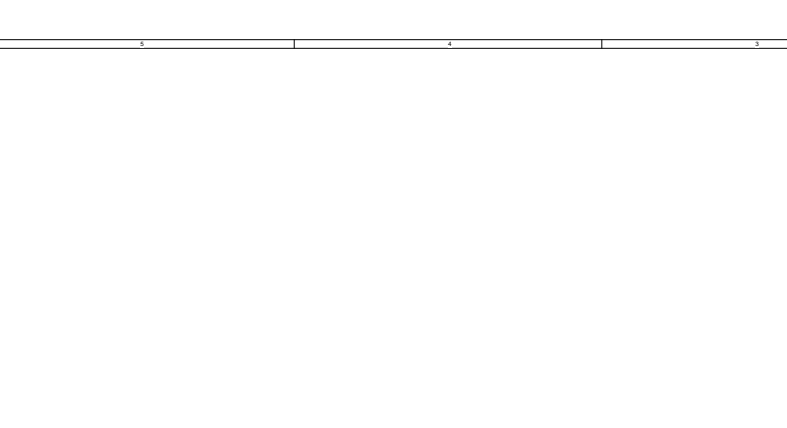
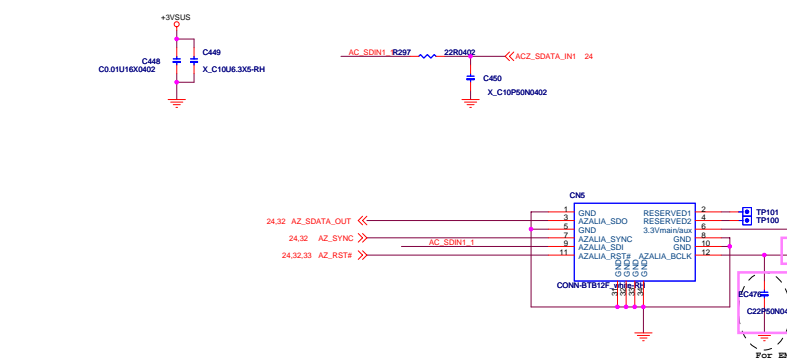
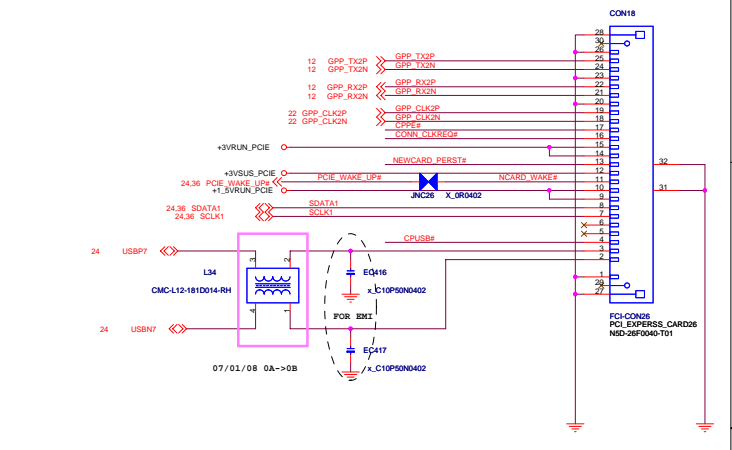
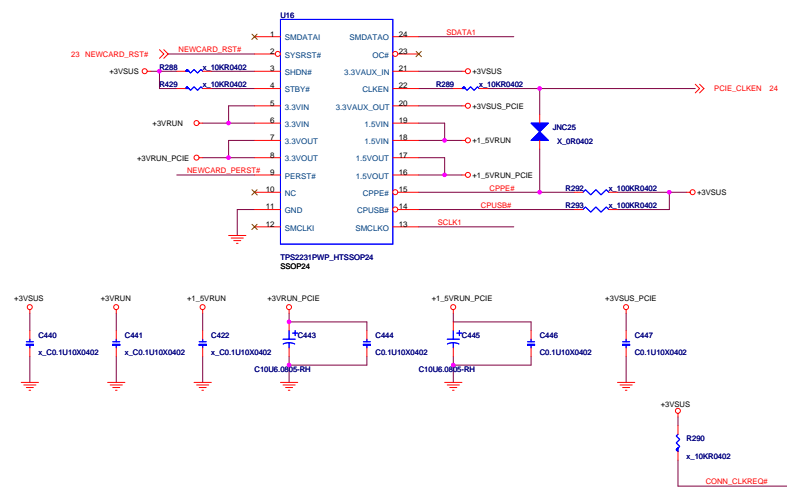
UDIO3	UDIO4	MSEN	XDEN	FUNCTION (ENABLE)
HIGH	HIGH	HIGH	HIGH	SD, MMC, MSCARD, XD

S, M-SD / MMC-MS-XD

MDIO00	SD	MMC	MS	XD
MDIO00	SD00	MMC00	MS00	XD00
MDIO01	SD01	MMC01	MS01	XD01
MDIO02	SD02	MMC02	MS02	XD02
MDIO03	SD03	MMC03	MS03	XD03
MDIO04	SD04	MMC04	MS04	XD04
MDIO05	SD05	MMC05	MS05	XD05
MDIO06	SD06	MMC06	MS06	XD06
MDIO07	SD07	MMC07	MS07	XD07
MDIO08	SD08	MMC08	MS08	XD08
MDIO09	SD09	MMC09	MS09	XD09
MDIO10	SD10	MMC10	MS10	XD10
MDIO11	SD11	MMC11	MS11	XD11
MDIO12	SD12	MMC12	MS12	XD12
MDIO13	SD13	MMC13	MS13	XD13
MDIO14	SD14	MMC14	MS14	XD14
MDIO15	SD15	MMC15	MS15	XD15
MDIO16	SD16	MMC16	MS16	XD16
MDIO17	SD17	MMC17	MS17	XD17
MDIO18	SD18	MMC18	MS18	XD18
MDIO19	SD19	MMC19	MS19	XD19
MDIO20	SD20	MMC20	MS20	XD20
MDIO21	SD21	MMC21	MS21	XD21
MDIO22	SD22	MMC22	MS22	XD22
MDIO23	SD23	MMC23	MS23	XD23
MDIO24	SD24	MMC24	MS24	XD24
MDIO25	SD25	MMC25	MS25	XD25
MDIO26	SD26	MMC26	MS26	XD26
MDIO27	SD27	MMC27	MS27	XD27
MDIO28	SD28	MMC28	MS28	XD28
MDIO29	SD29	MMC29	MS29	XD29
MDIO30	SD30	MMC30	MS30	XD30
MDIO31	SD31	MMC31	MS31	XD31
MDIO32	SD32	MMC32	MS32	XD32
MDIO33	SD33	MMC33	MS33	XD33
MDIO34	SD34	MMC34	MS34	XD34
MDIO35	SD35	MMC35	MS35	XD35
MDIO36	SD36	MMC36	MS36	XD36
MDIO37	SD37	MMC37	MS37	XD37
MDIO38	SD38	MMC38	MS38	XD38
MDIO39	SD39	MMC39	MS39	XD39
MDIO40	SD40	MMC40	MS40	XD40
MDIO41	SD41	MMC41	MS41	XD41
MDIO42	SD42	MMC42	MS42	XD42
MDIO43	SD43	MMC43	MS43	XD43
MDIO44	SD44	MMC44	MS44	XD44
MDIO45	SD45	MMC45	MS45	XD45
MDIO46	SD46	MMC46	MS46	XD46
MDIO47	SD47	MMC47	MS47	XD47
MDIO48	SD48	MMC48	MS48	XD48
MDIO49	SD49	MMC49	MS49	XD49
MDIO50	SD50	MMC50	MS50	XD50
MDIO51	SD51	MMC51	MS51	XD51
MDIO52	SD52	MMC52	MS52	XD52
MDIO53	SD53	MMC53	MS53	XD53
MDIO54	SD54	MMC54	MS54	XD54
MDIO55	SD55	MMC55	MS55	XD55
MDIO56	SD56	MMC56	MS56	XD56
MDIO57	SD57	MMC57	MS57	XD57
MDIO58	SD58	MMC58	MS58	XD58
MDIO59	SD59	MMC59	MS59	XD59
MDIO60	SD60	MMC60	MS60	XD60
MDIO61	SD61	MMC61	MS61	XD61
MDIO62	SD62	MMC62	MS62	XD62
MDIO63	SD63	MMC63	MS63	XD63
MDIO64	SD64	MMC64	MS64	XD64
MDIO65	SD65	MMC65	MS65	XD65
MDIO66	SD66	MMC66	MS66	XD66
MDIO67	SD67	MMC67	MS67	XD67
MDIO68	SD68	MMC68	MS68	XD68
MDIO69	SD69	MMC69	MS69	XD69
MDIO70	SD70	MMC70	MS70	XD70
MDIO71	SD71	MMC71	MS71	XD71
MDIO72	SD72	MMC72	MS72	XD72
MDIO73	SD73	MMC73	MS73	XD73
MDIO74	SD74	MMC74	MS74	XD74
MDIO75	SD75	MMC75	MS75	XD75
MDIO76	SD76	MMC76	MS76	XD76
MDIO77	SD77	MMC77	MS77	XD77
MDIO78	SD78	MMC78	MS78	XD78
MDIO79	SD79	MMC79	MS79	XD79
MDIO80	SD80	MMC80	MS80	XD80
MDIO81	SD81	MMC81	MS81	XD81
MDIO82	SD82	MMC82	MS82	XD82
MDIO83	SD83	MMC83	MS83	XD83
MDIO84	SD84	MMC84	MS84	XD84
MDIO85	SD85	MMC85	MS85	XD85
MDIO86	SD86	MMC86	MS86	XD86
MDIO87	SD87	MMC87	MS87	XD87
MDIO88	SD88	MMC88	MS88	XD88
MDIO89	SD89	MMC89	MS89	XD89
MDIO90	SD90	MMC90	MS90	XD90
MDIO91	SD91	MMC91	MS91	XD91
MDIO92	SD92	MMC92	MS92	XD92
MDIO93	SD93	MMC93	MS93	XD93
MDIO94	SD94	MMC94	MS94	XD94
MDIO95	SD95	MMC95	MS95	XD95
MDIO96	SD96	MMC96	MS96	XD96
MDIO97	SD97	MMC97	MS97	XD97
MDIO98	SD98	MMC98	MS98	XD98
MDIO99	SD99	MMC99	MS99	XD99
MDIO100	SD100	MMC100	MS100	XD100

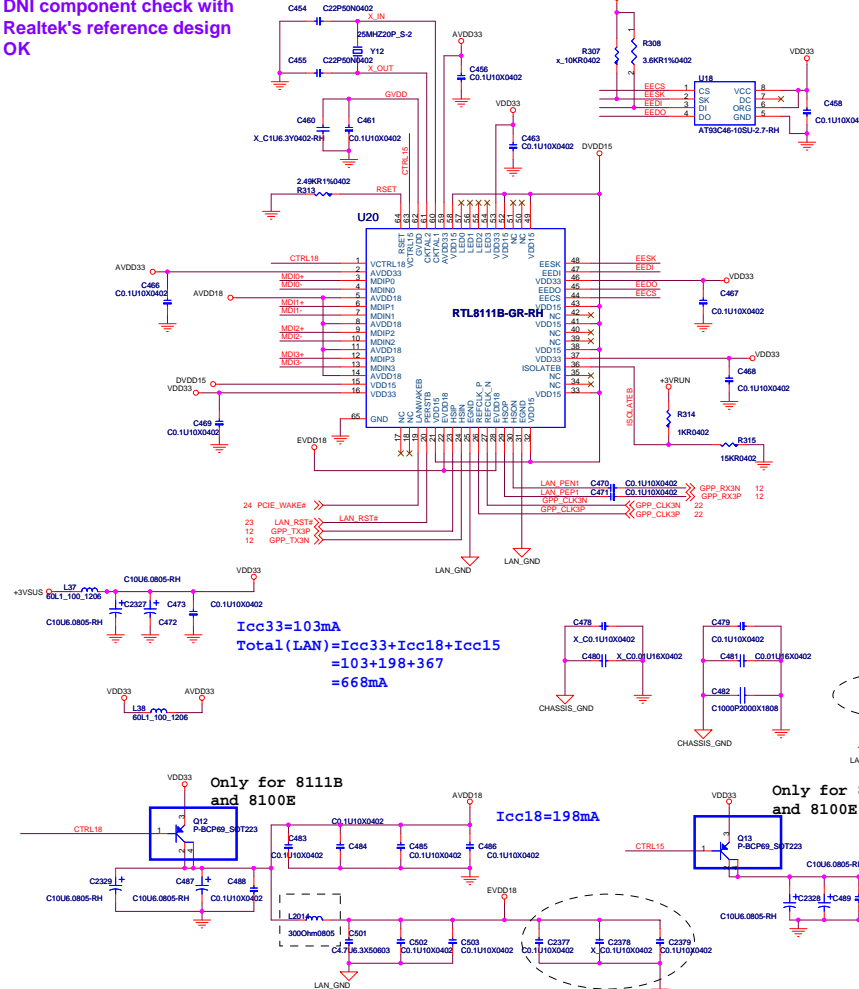


MSI CORPORATION		
MS-1634X		
Size	Document Number	Rev
Custom	MS-1634X	0B
Date: Thursday, May 31, 2007	Sheet	29 of 51



MICRO-STAR INT'L CO.,LTD.	
File	NEW CARD & MDC
Size	Customer
Date	Thursday, May 31, 2007
Sheet	50 of 51

DNI component check with
Realtek's reference design
OK



$I_{cc33}=103mA$
 $Total(LAN)=I_{cc33}+I_{cc18}+I_{cc15}$
 $=103+198+367$
 $=668mA$

Only for 8111B
and 8100E

$I_{cc18}=198mA$

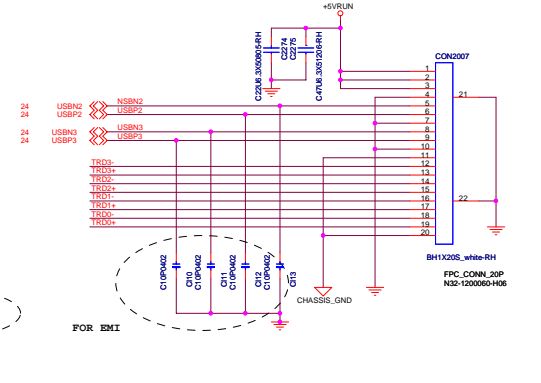
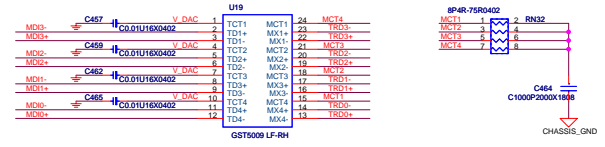
Only for 8111B
and 8100E

$I_{cc15}=367mA$

07/04/09 0B->0C
FOR EMI

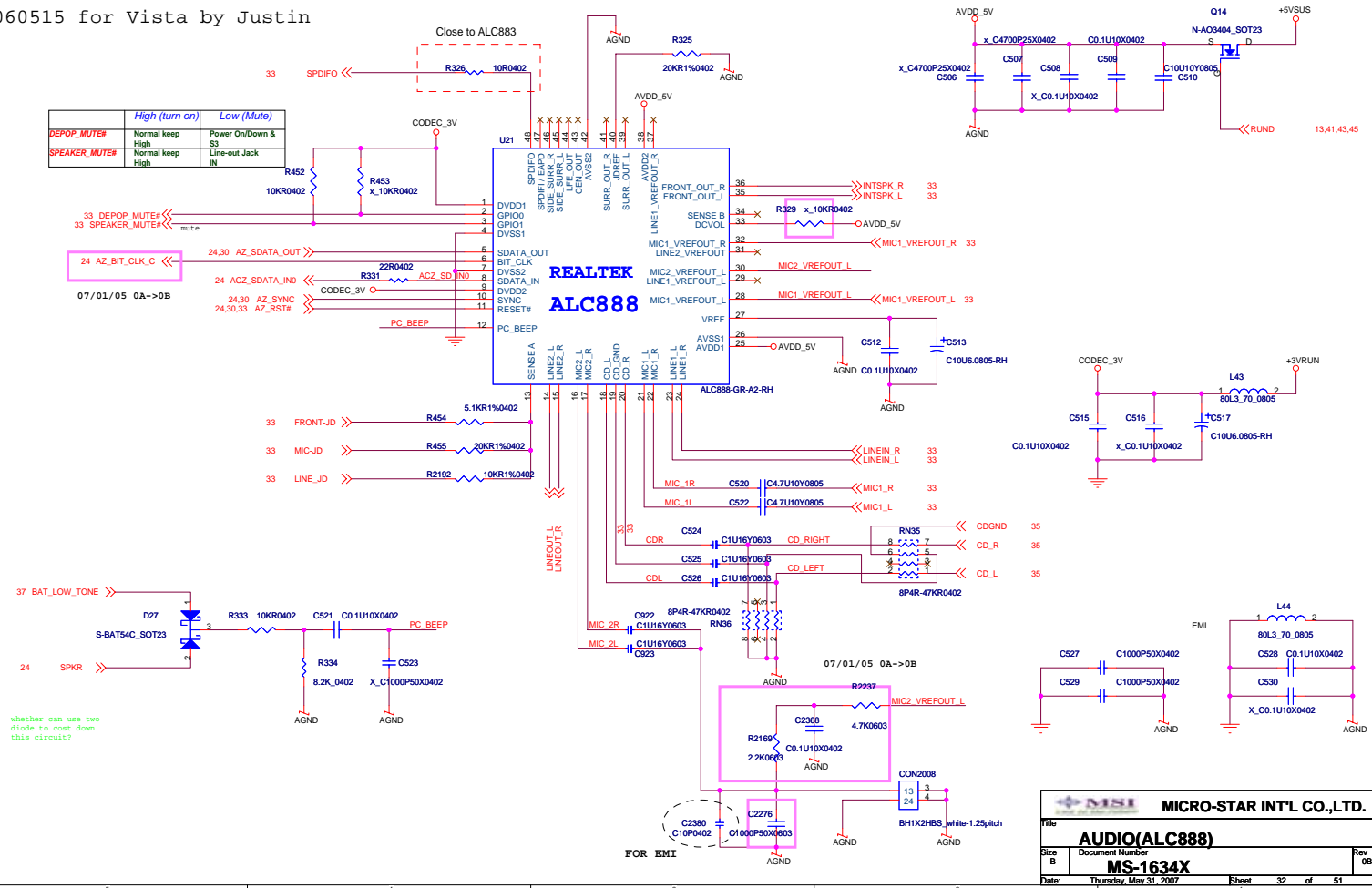
07/04/03 0B->0C
FOR EMI

LAN MAGNETICS

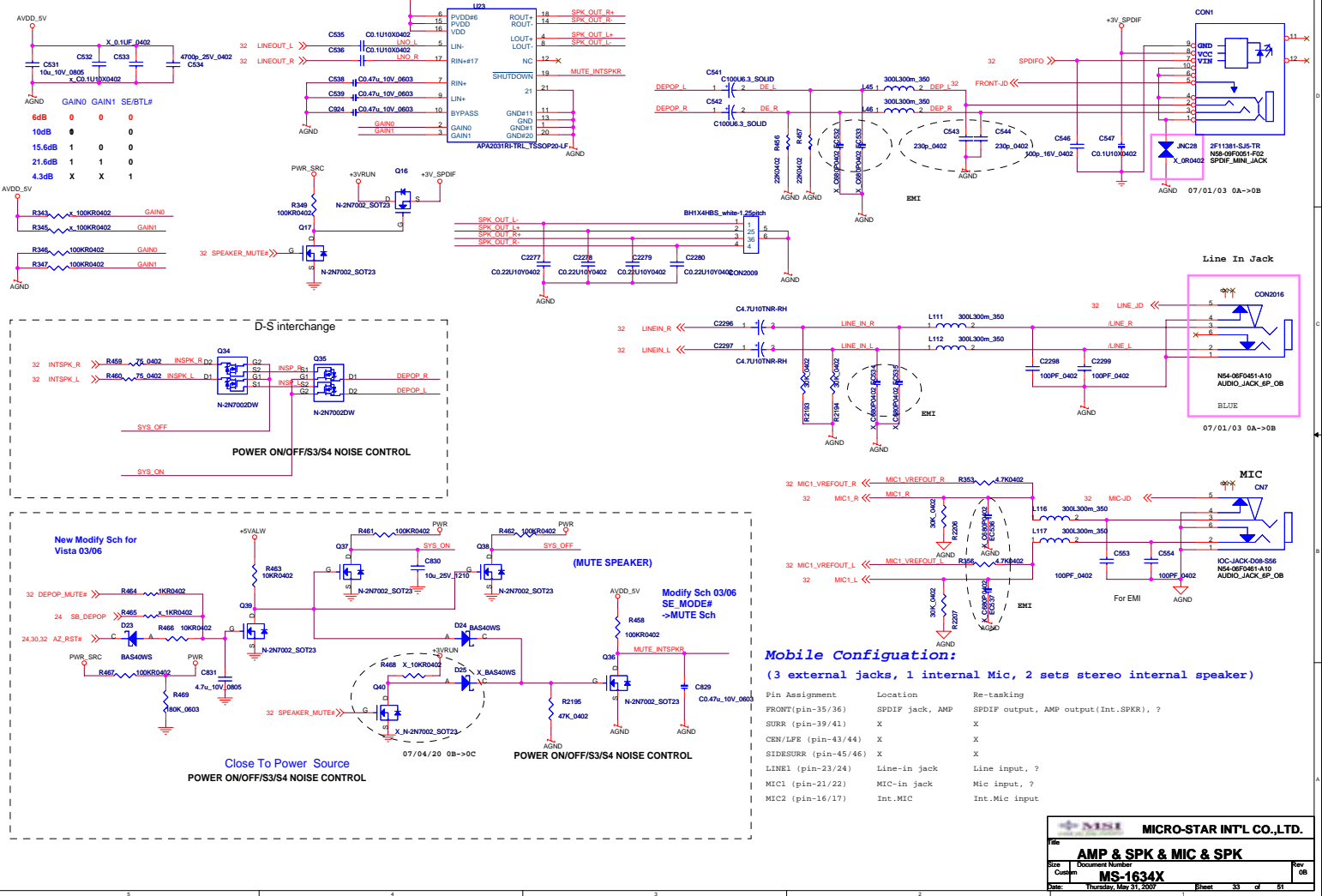


MICRO-STAR INT'L CO.,LTD.			
File	GIGA LAN (RTL8111B)		
Size	Document Number		
Custom	MS-1634X		Rev 08
Date	Tuesday, May 31, 2007		Sheet 51 of 51

	High (turn on)	Low (Mute)
DEPOP_MUTEN#	Normal keep High	Power On/Down & S3
SPEAKER_MUTEN#	Normal keep High	Line-out Jack IN



MICRO-STAR INT'L CO., LTD.	
AUDIO(ALC888)	
File	Document Number
Size B	MS-1634X
Date: Thursday, May 31, 2007	Sheet 32 of 51
	Rev 0B



Mobile Configuration:

(3 external jacks, 1 internal Mic, 2 sets stereo internal speaker)

Pin Assignment	Location	Re-tasking
FRONT(p1n-35/36)	SPDIF jack, AMP	SPDIF output, AMP output(Int.SPKR), ?
SURR (pin-39/41)	X	X
CEN/LPE (pin-43/44)	X	X
SIDESURR (pin-45/46)	X	X
LINE1 (pin-23/24)	Line-in jack	Line input, ?
MIC1 (pin-21/22)	MIC-in jack	Mic input, ?
MIC2 (pin-16/17)	Int.MIC	Int.Mic input

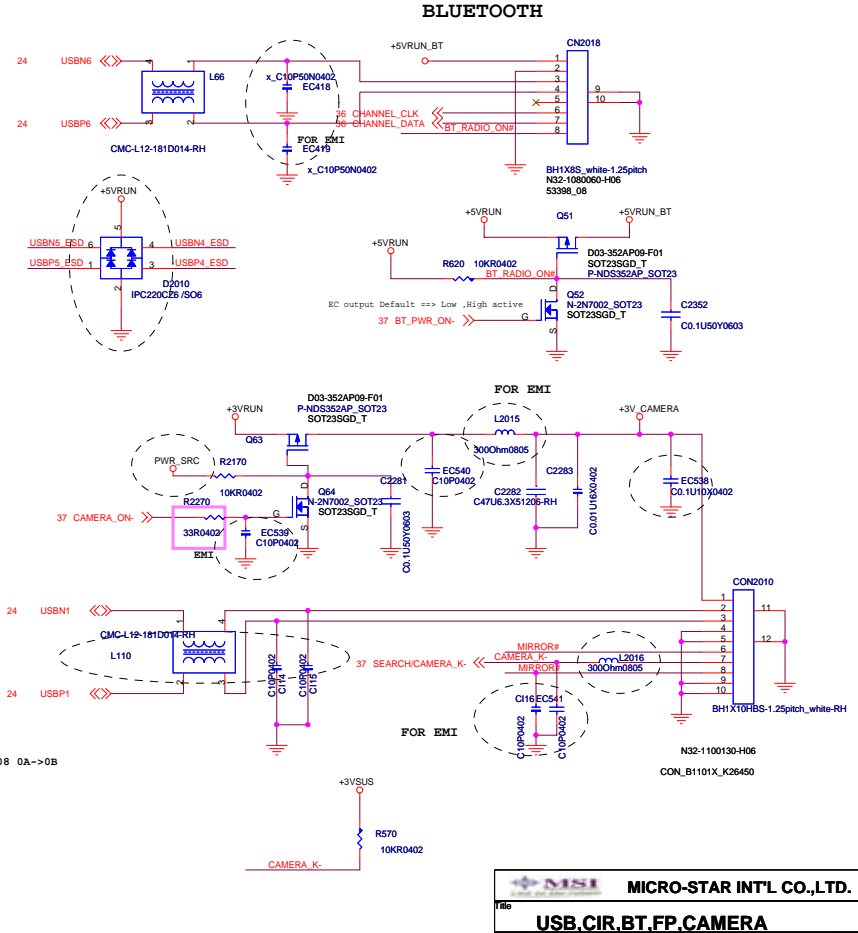
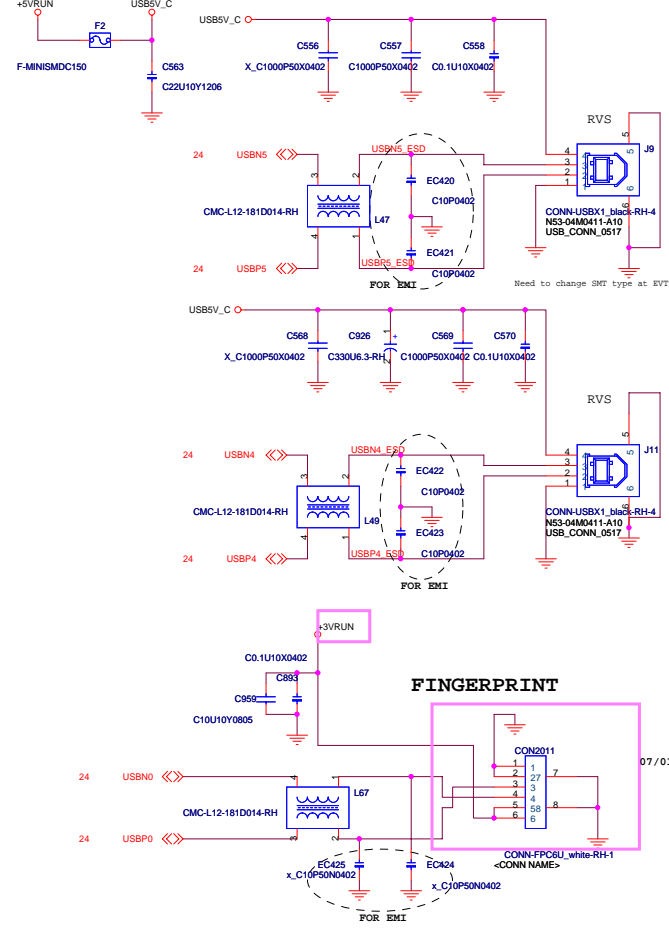
MICRO-STAR INT'L CO.,LTD.

File: **AMP & SPK & MIC & SPK**

Size: **MS-1634X**

Date: **Thursday, May 31, 2007**

Sheet: **33** of **51**



MICRO-STAR INT'L CO.,LTD.

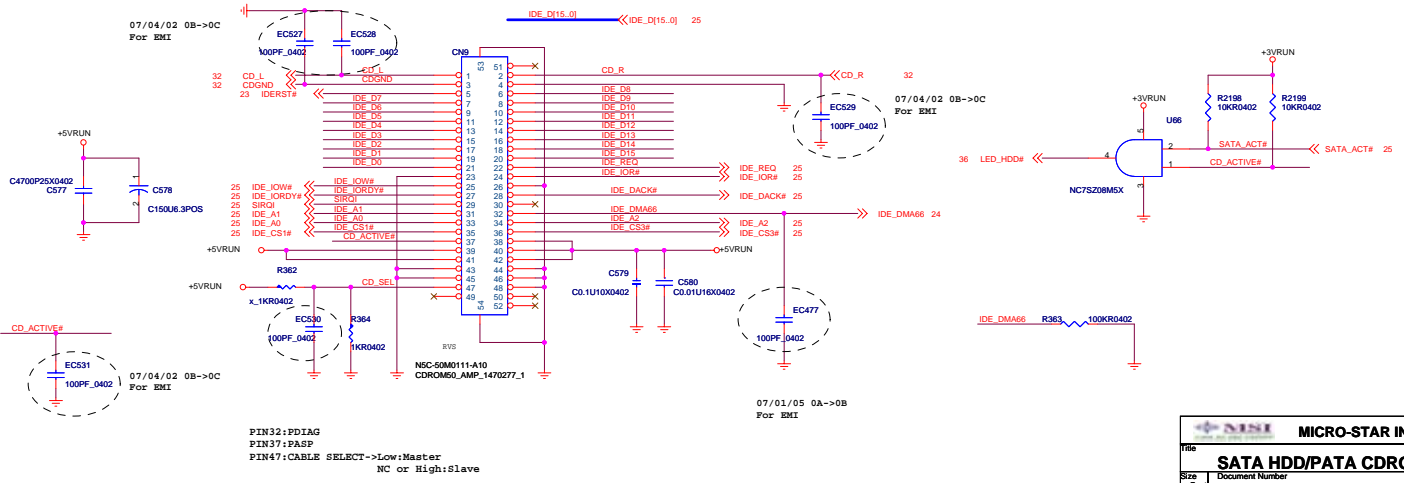
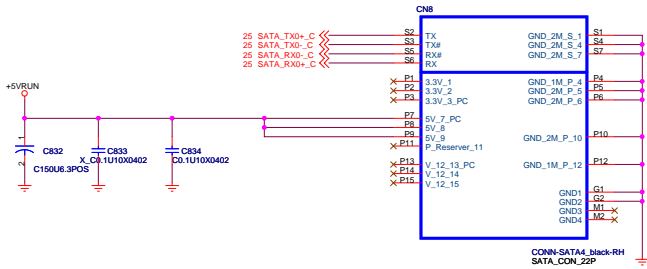
File: **USB_CIR_BT_FP_CAMERA**

Size: **MS-1634X**

Date: Thursday, May 31, 2007

Sheet 34 of 51

2.5" HD DRIVE

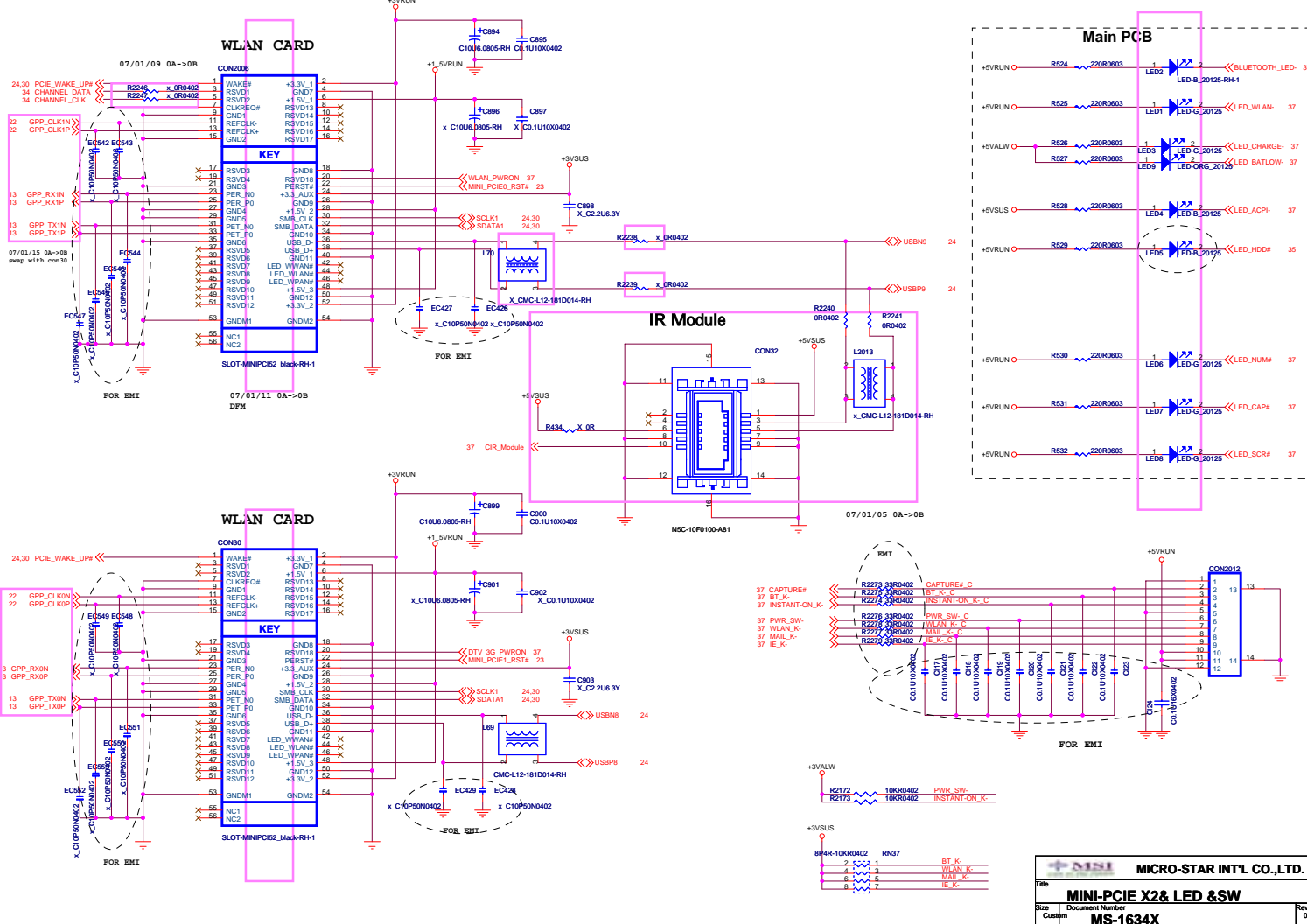


MICRO-STAR INT'L CO.,LTD.

File: **SATA HDD/PATA CDROM CONN**

Size: Custom Document Number: **MS-1634X** Rev: 08

Date: Thursday, May 31, 2007 Sheet: 35 of 61



MICRO-STAR INT'L CO., LTD.

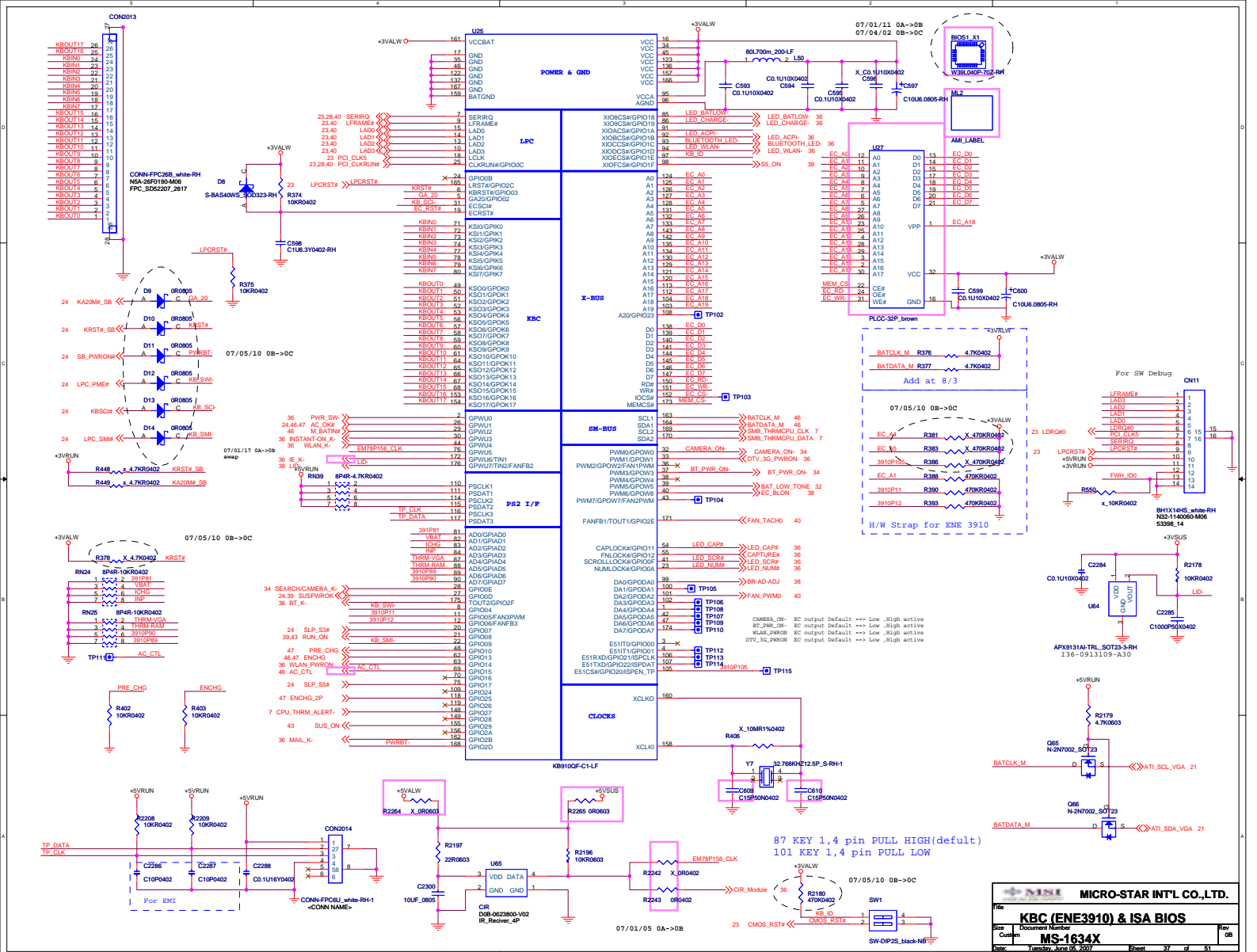
Title: **MINI-PCIE X2& LED & SW**

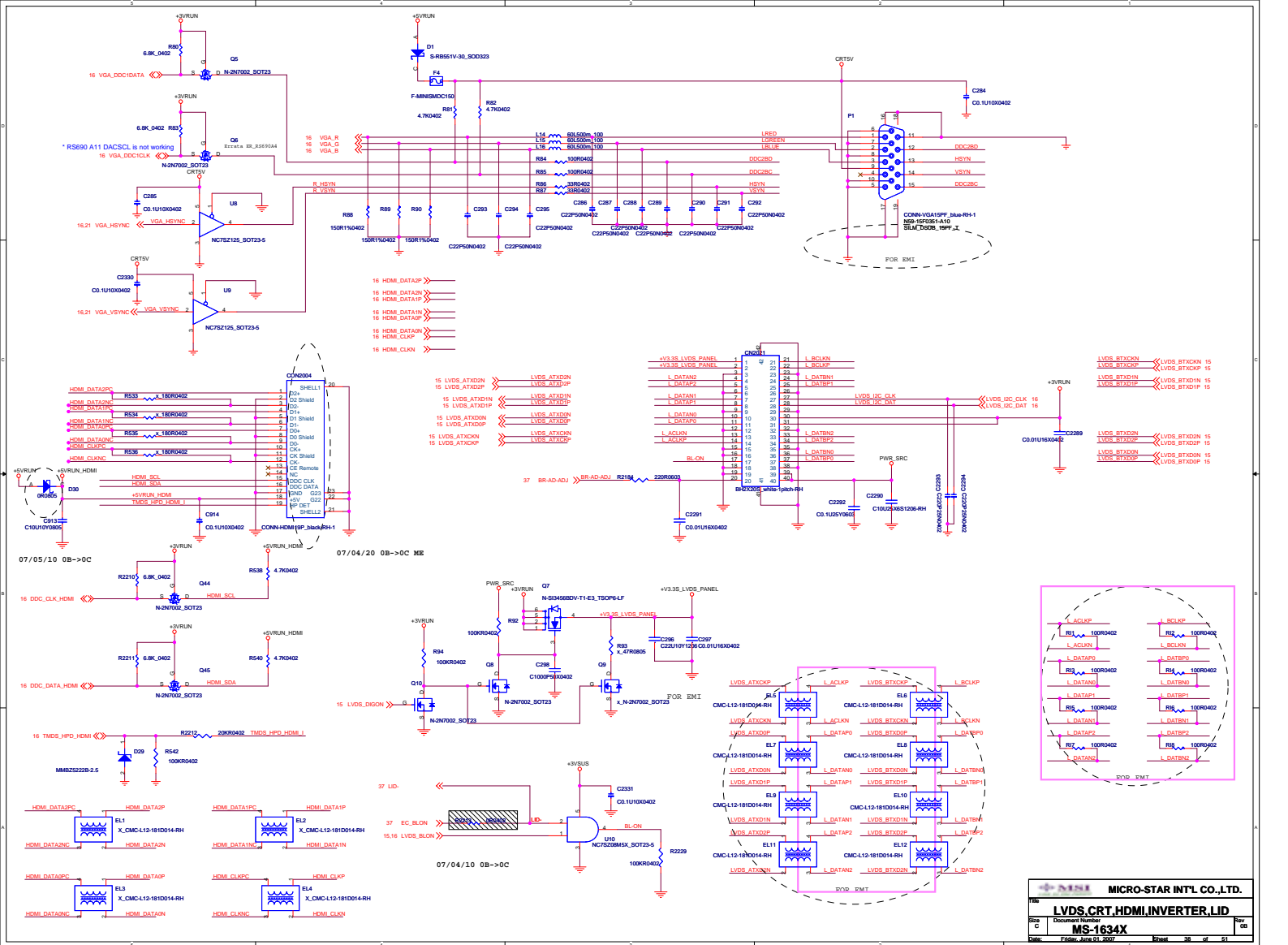
Size: Document Number

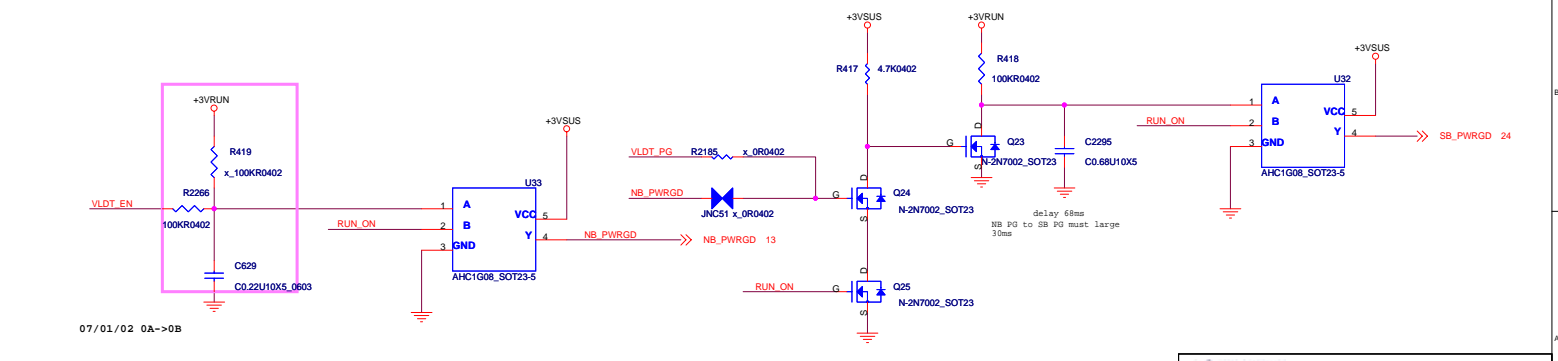
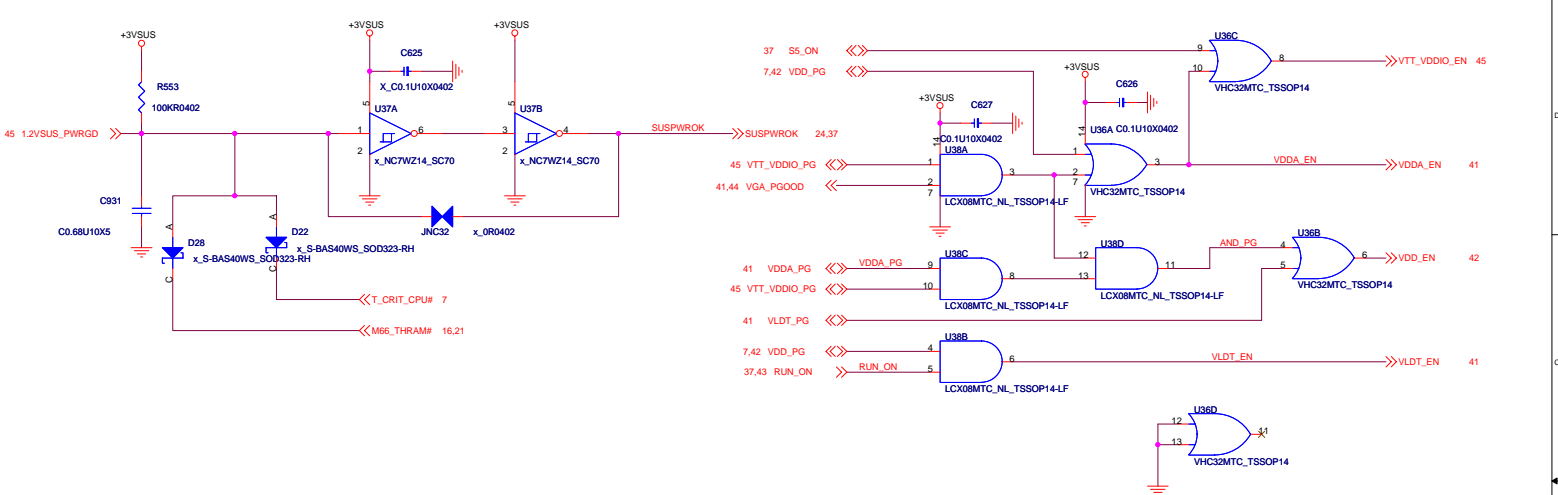
Customer: **MS-1634X**

Date: Thursday, May 31, 2007

Sheet 38 of 51

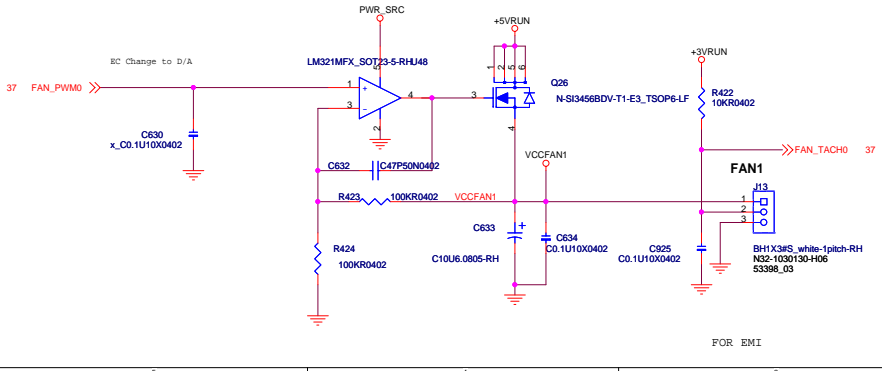
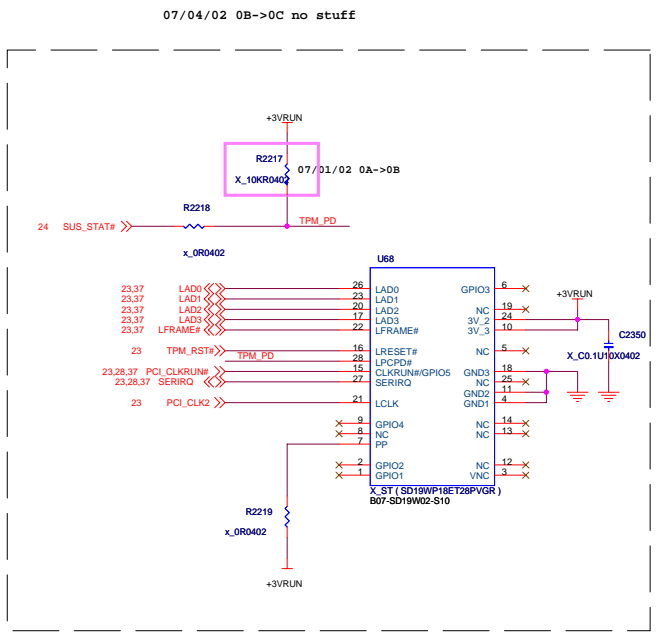
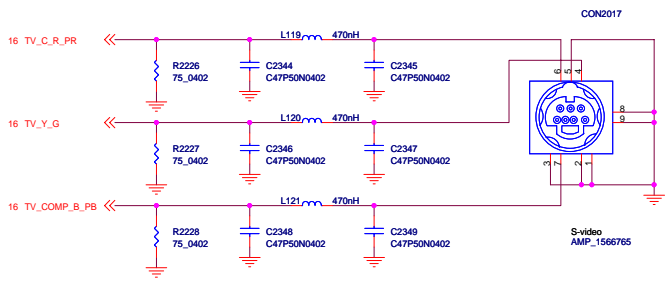




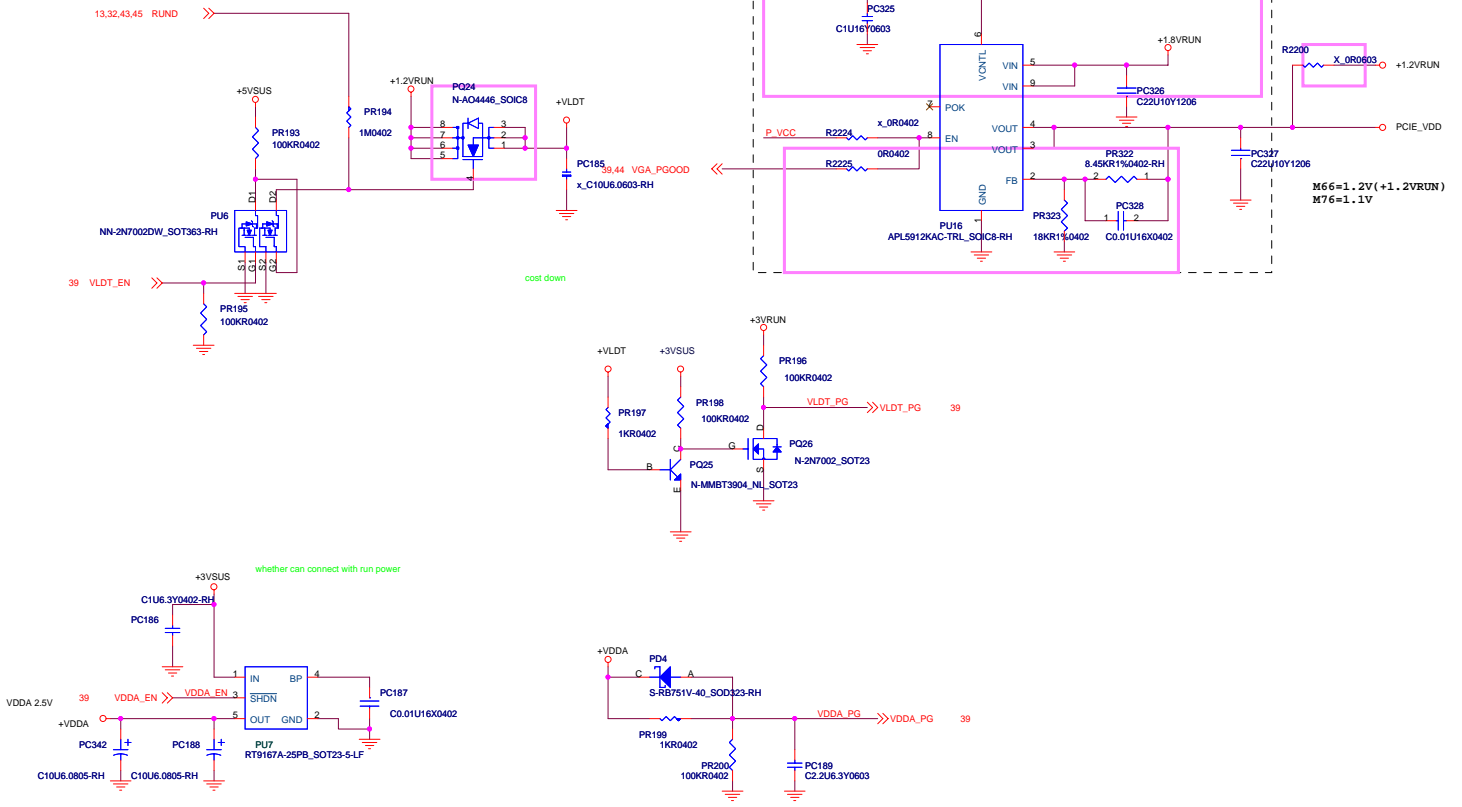


MICRO-STAR INT'L CO.,LTD.	
File	PWRGD
Size	Document Number
MS-1634X	
Date:	Thursday, May 31, 2007
Sheet	39 of 51

07/01/02 0A->0B



MICRO-STAR INT'L CO., LTD.	
File	FAN&TRM&S-VIDEO
Size	Document Number
MS-1634X	
Date:	Thursday, May 31, 2007
Sheet	40 of 51
Rev	0B

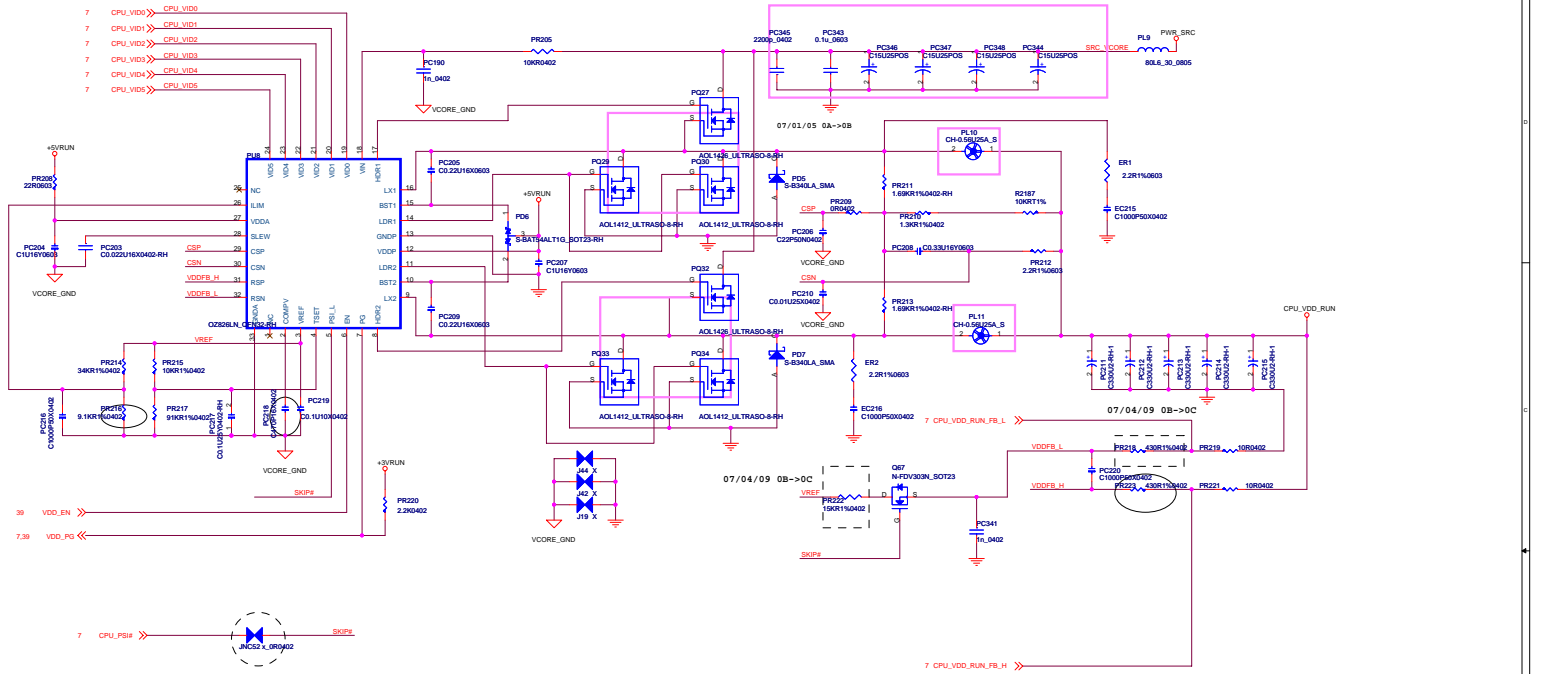


MICRO-STAR INT'L CO.,LTD.

File: **VDDA 2.5V VLDT**

Size B Document Number **MS-1634X** Rev 08

Date: Thursday, May 31, 2007 Sheet 41 of 51

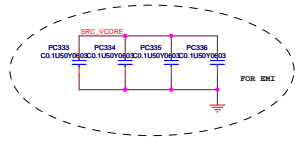


CPU_VDDIO_BUS

RN28	8F4R-10K0402	CPU_VDD1
PC303	CO.102U16X0402-RH	CPU_VDD1
PC304	CO.102U16X0402-RH	CPU_VDD1
PC305	CO.102U16X0402-RH	CPU_VDD1
PC306	CO.102U16X0402-RH	CPU_VDD1
PC307	CO.102U16X0402-RH	CPU_VDD1
PC308	CO.102U16X0402-RH	CPU_VDD1
PC309	CO.102U16X0402-RH	CPU_VDD1
PC310	CO.102U16X0402-RH	CPU_VDD1
PC311	CO.102U16X0402-RH	CPU_VDD1
PC312	CO.102U16X0402-RH	CPU_VDD1
PC313	CO.102U16X0402-RH	CPU_VDD1
PC314	CO.102U16X0402-RH	CPU_VDD1
PC315	CO.102U16X0402-RH	CPU_VDD1
PC316	CO.102U16X0402-RH	CPU_VDD1
PC317	CO.102U16X0402-RH	CPU_VDD1
PC318	CO.102U16X0402-RH	CPU_VDD1
PC319	CO.102U16X0402-RH	CPU_VDD1
PC320	CO.102U16X0402-RH	CPU_VDD1
PC321	CO.102U16X0402-RH	CPU_VDD1
PC322	CO.102U16X0402-RH	CPU_VDD1
PC323	CO.102U16X0402-RH	CPU_VDD1
PC324	CO.102U16X0402-RH	CPU_VDD1
PC325	CO.102U16X0402-RH	CPU_VDD1
PC326	CO.102U16X0402-RH	CPU_VDD1
PC327	CO.102U16X0402-RH	CPU_VDD1
PC328	CO.102U16X0402-RH	CPU_VDD1
PC329	CO.102U16X0402-RH	CPU_VDD1
PC330	CO.102U16X0402-RH	CPU_VDD1
PC331	CO.102U16X0402-RH	CPU_VDD1
PC332	CO.102U16X0402-RH	CPU_VDD1
PC333	CO.102U16X0402-RH	CPU_VDD1
PC334	CO.102U16X0402-RH	CPU_VDD1
PC335	CO.102U16X0402-RH	CPU_VDD1
PC336	CO.102U16X0402-RH	CPU_VDD1
PC337	CO.102U16X0402-RH	CPU_VDD1
PC338	CO.102U16X0402-RH	CPU_VDD1
PC339	CO.102U16X0402-RH	CPU_VDD1
PC340	CO.102U16X0402-RH	CPU_VDD1
PC341	CO.102U16X0402-RH	CPU_VDD1
PC342	CO.102U16X0402-RH	CPU_VDD1
PC343	CO.102U16X0402-RH	CPU_VDD1
PC344	CO.102U16X0402-RH	CPU_VDD1
PC345	CO.102U16X0402-RH	CPU_VDD1
PC346	CO.102U16X0402-RH	CPU_VDD1
PC347	CO.102U16X0402-RH	CPU_VDD1
PC348	CO.102U16X0402-RH	CPU_VDD1
PC349	CO.102U16X0402-RH	CPU_VDD1
PC350	CO.102U16X0402-RH	CPU_VDD1
PC351	CO.102U16X0402-RH	CPU_VDD1
PC352	CO.102U16X0402-RH	CPU_VDD1
PC353	CO.102U16X0402-RH	CPU_VDD1
PC354	CO.102U16X0402-RH	CPU_VDD1
PC355	CO.102U16X0402-RH	CPU_VDD1
PC356	CO.102U16X0402-RH	CPU_VDD1
PC357	CO.102U16X0402-RH	CPU_VDD1
PC358	CO.102U16X0402-RH	CPU_VDD1
PC359	CO.102U16X0402-RH	CPU_VDD1
PC360	CO.102U16X0402-RH	CPU_VDD1
PC361	CO.102U16X0402-RH	CPU_VDD1
PC362	CO.102U16X0402-RH	CPU_VDD1
PC363	CO.102U16X0402-RH	CPU_VDD1
PC364	CO.102U16X0402-RH	CPU_VDD1
PC365	CO.102U16X0402-RH	CPU_VDD1
PC366	CO.102U16X0402-RH	CPU_VDD1
PC367	CO.102U16X0402-RH	CPU_VDD1
PC368	CO.102U16X0402-RH	CPU_VDD1
PC369	CO.102U16X0402-RH	CPU_VDD1
PC370	CO.102U16X0402-RH	CPU_VDD1
PC371	CO.102U16X0402-RH	CPU_VDD1
PC372	CO.102U16X0402-RH	CPU_VDD1
PC373	CO.102U16X0402-RH	CPU_VDD1
PC374	CO.102U16X0402-RH	CPU_VDD1
PC375	CO.102U16X0402-RH	CPU_VDD1
PC376	CO.102U16X0402-RH	CPU_VDD1
PC377	CO.102U16X0402-RH	CPU_VDD1
PC378	CO.102U16X0402-RH	CPU_VDD1
PC379	CO.102U16X0402-RH	CPU_VDD1
PC380	CO.102U16X0402-RH	CPU_VDD1
PC381	CO.102U16X0402-RH	CPU_VDD1
PC382	CO.102U16X0402-RH	CPU_VDD1
PC383	CO.102U16X0402-RH	CPU_VDD1
PC384	CO.102U16X0402-RH	CPU_VDD1
PC385	CO.102U16X0402-RH	CPU_VDD1
PC386	CO.102U16X0402-RH	CPU_VDD1
PC387	CO.102U16X0402-RH	CPU_VDD1
PC388	CO.102U16X0402-RH	CPU_VDD1
PC389	CO.102U16X0402-RH	CPU_VDD1
PC390	CO.102U16X0402-RH	CPU_VDD1
PC391	CO.102U16X0402-RH	CPU_VDD1
PC392	CO.102U16X0402-RH	CPU_VDD1
PC393	CO.102U16X0402-RH	CPU_VDD1
PC394	CO.102U16X0402-RH	CPU_VDD1
PC395	CO.102U16X0402-RH	CPU_VDD1
PC396	CO.102U16X0402-RH	CPU_VDD1
PC397	CO.102U16X0402-RH	CPU_VDD1
PC398	CO.102U16X0402-RH	CPU_VDD1
PC399	CO.102U16X0402-RH	CPU_VDD1
PC400	CO.102U16X0402-RH	CPU_VDD1

Components encircled are not necessary because the PSL-2 signal input of 02230 is fully compliant with AMD specification

CPU_PSI# can be directly connected to SKIP#



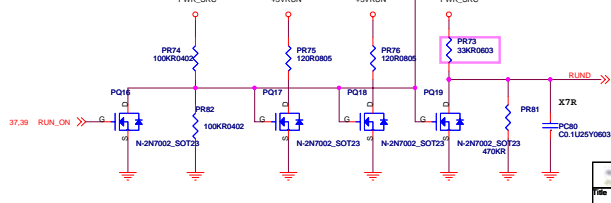
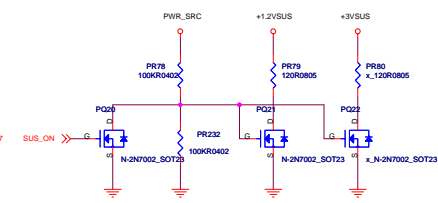
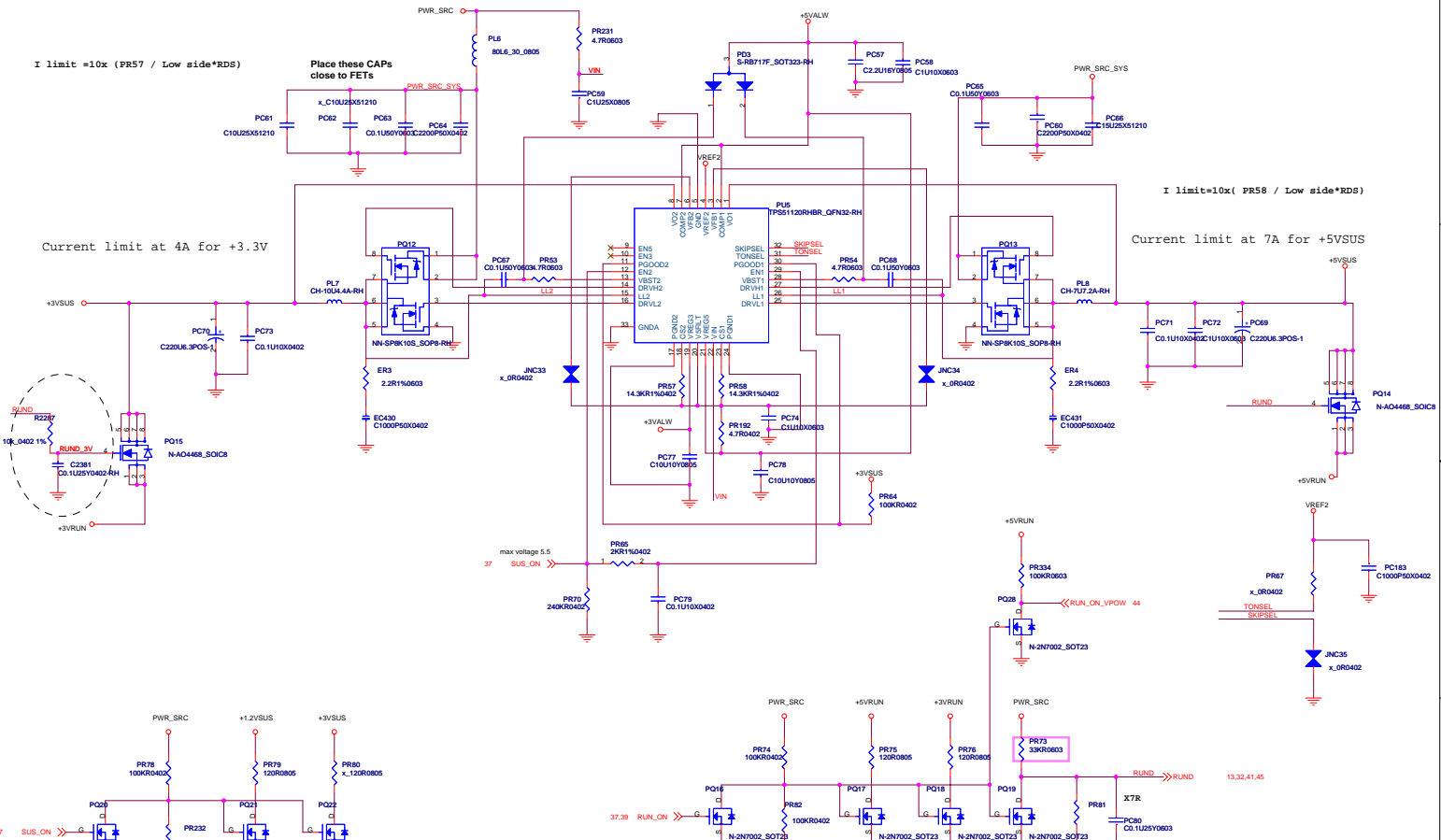
I limit =10x (PR57 / Low side*RDS)

Place these CAPs close to FETs

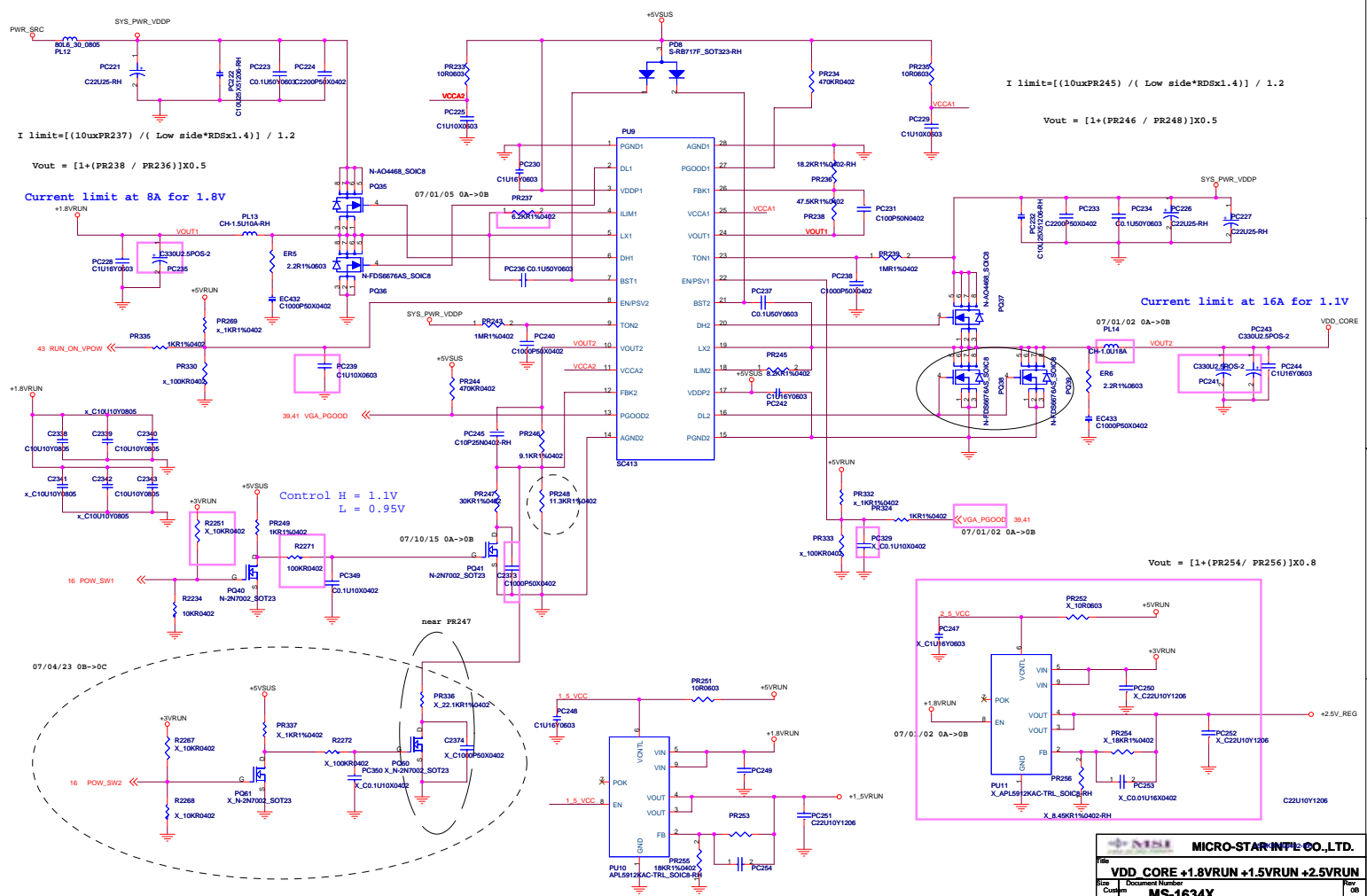
Current limit at 4A for +3.3V

I limit=10x(PR58 / Low side*RDS)

Current limit at 7A for +5VSUS

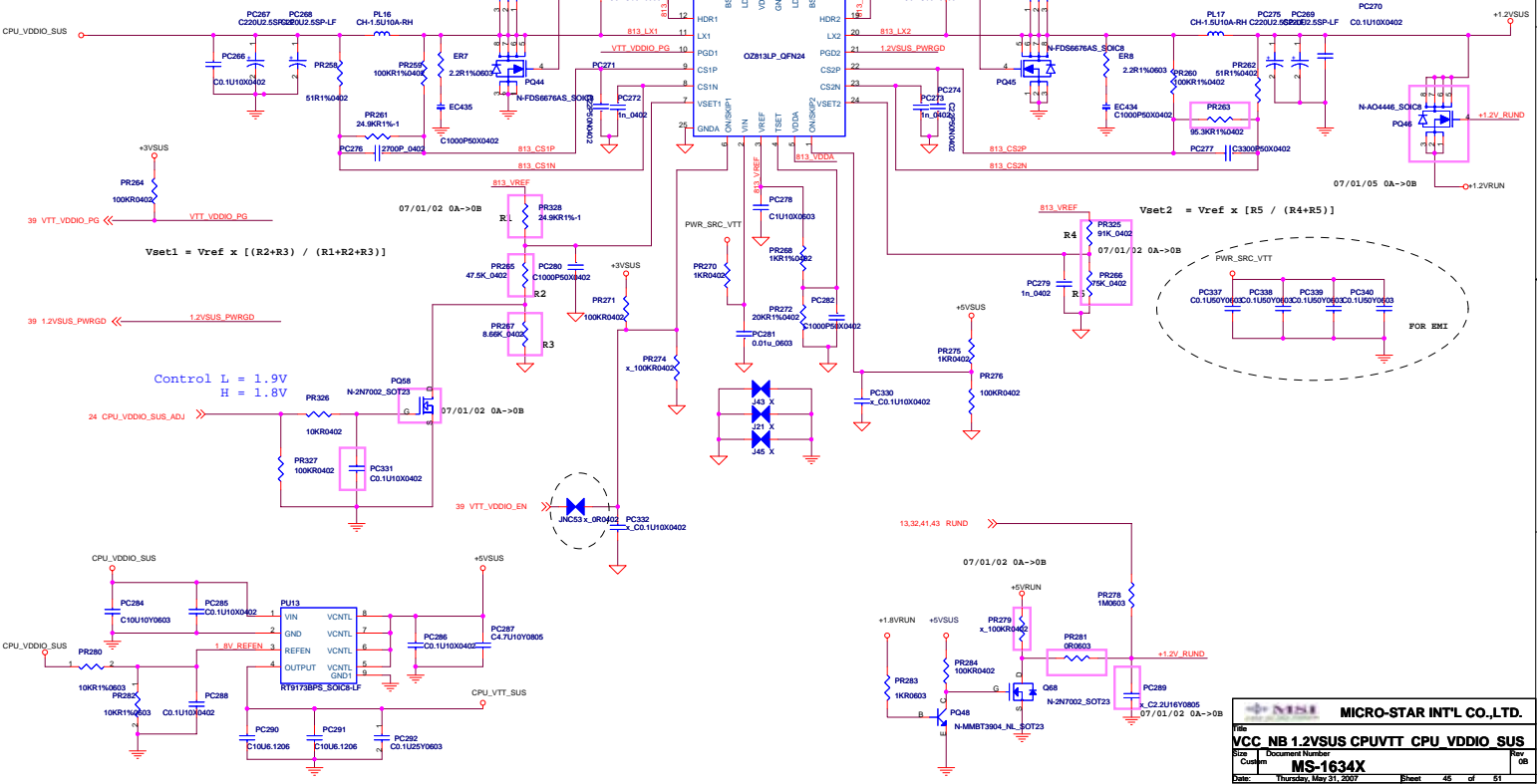


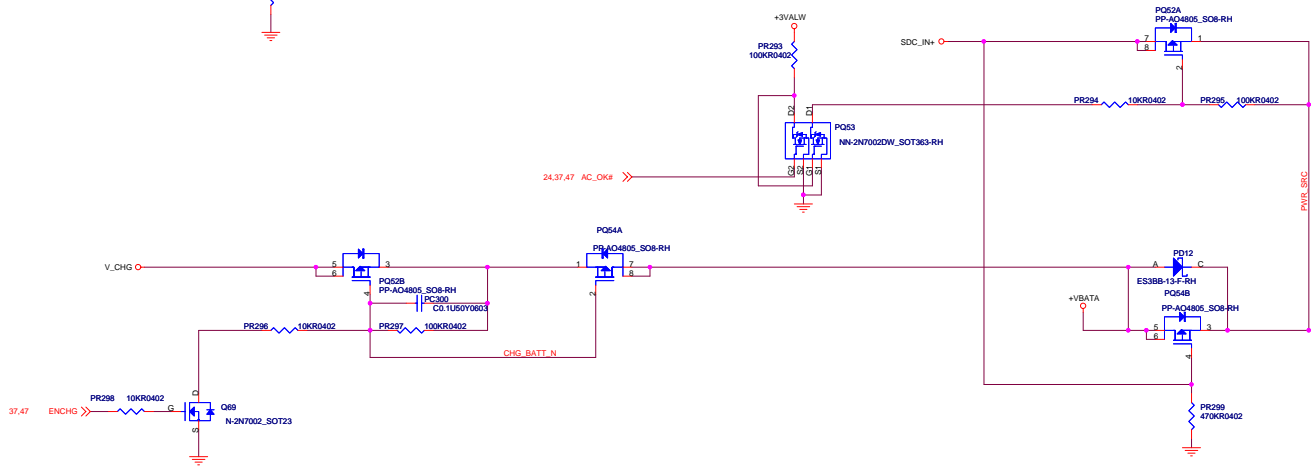
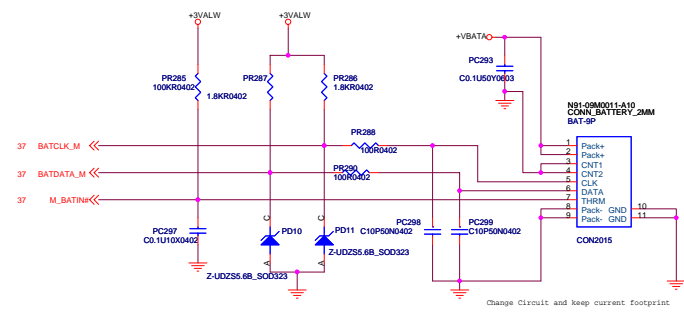
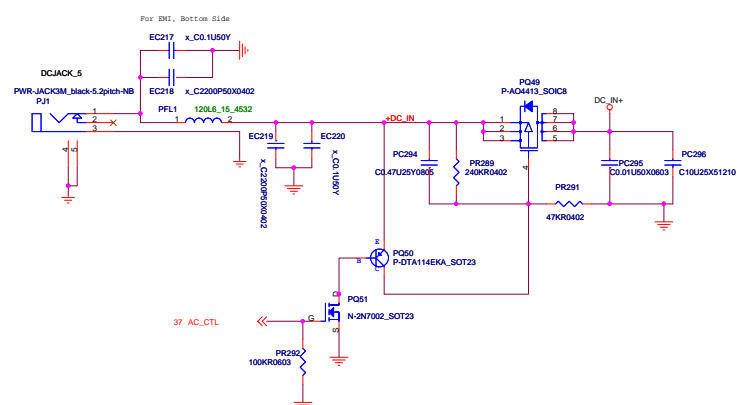
MICRO-STAR INT'L CO.,LTD.	
SYSTEM POWER 3/5V 2.5VSUS	
Size	Document Number
MS-1634X	
Date	Version
Tuesday, June 05, 2007	Sheet 43 of 51



The Limited Current = 7.5A

Current Limit at 10 Amp





MICRO-STAR INT'L CO.,LTD.	
Title	Battery Select
Size	Document Number
Customer	MS-1634X
Date: Thursday, May 31, 2007	Rev 08

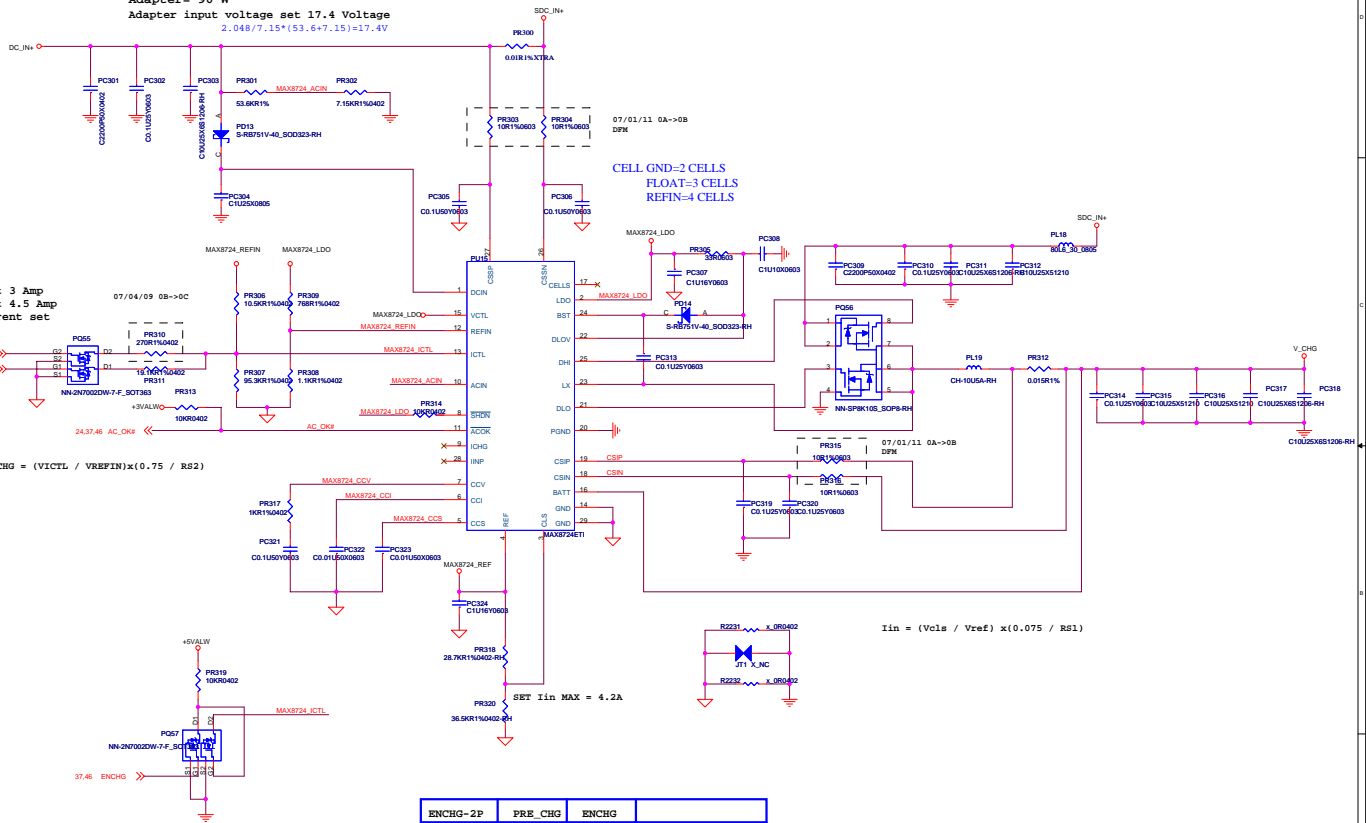
Adapter= 90 W
 Adapter input voltage set 17.4 Voltage
 $2.048/7.15 \times (53.6+7.15) = 17.4V$

382P: Charge current set 3 Amp
 383P: Charge current set 4.5 Amp
 Pre-charge: Charge current set 220mA

37 PRE_CHG
 37 ENCHG_2P
 37 ENCHG_2P

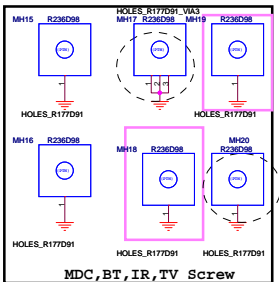
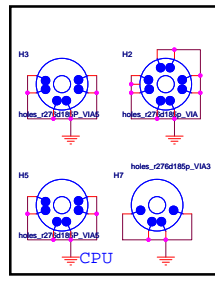
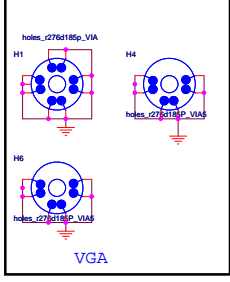
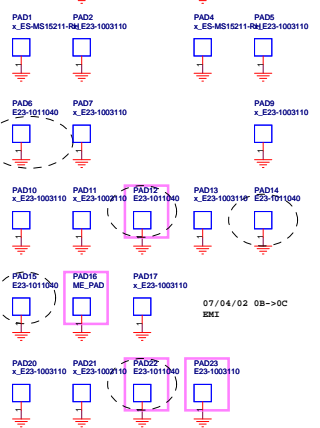
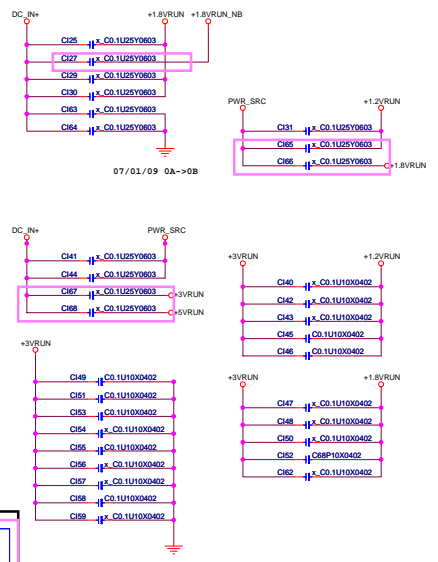
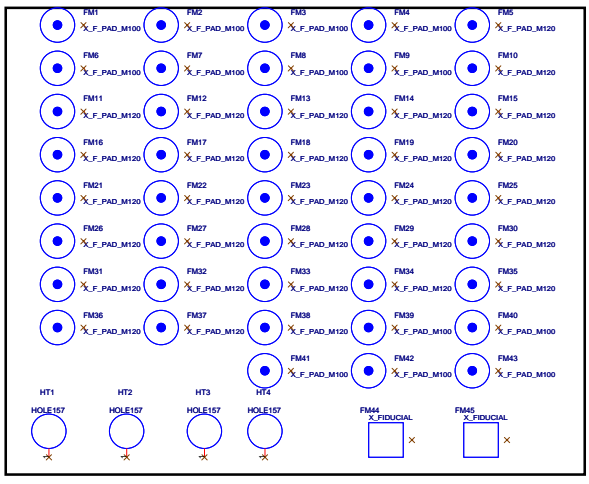
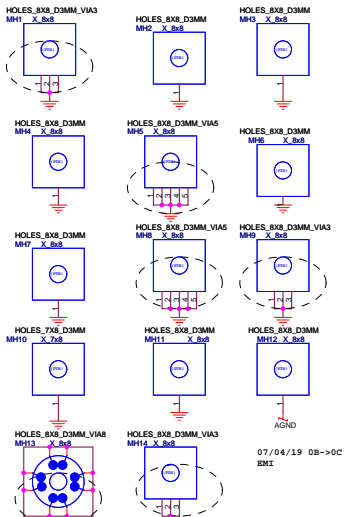
$ICHG = (VICTL / VREFIN) \times (0.75 / RS2)$

37.46 ENCHG
 37.46 ENCHG

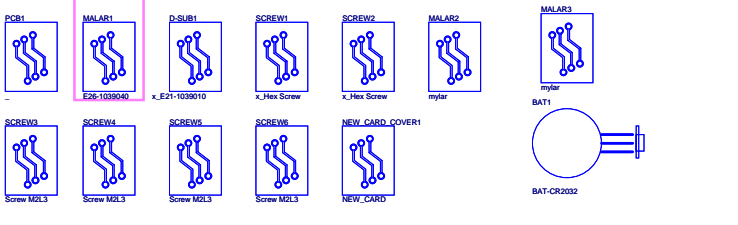
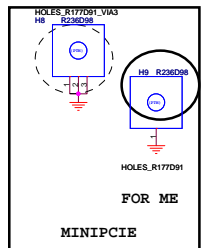


ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	382P-Fast charge
0	0	1	383P-Fast charge
0	0	0	STOP CHARGE

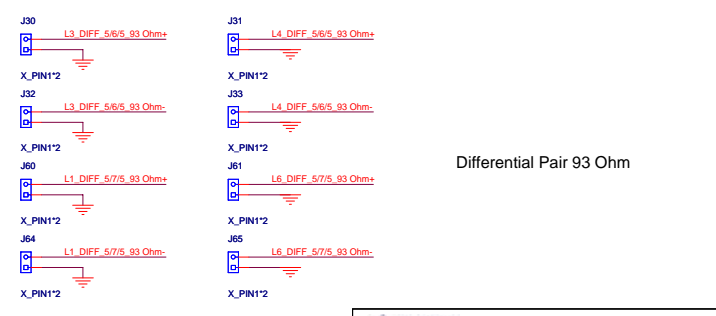
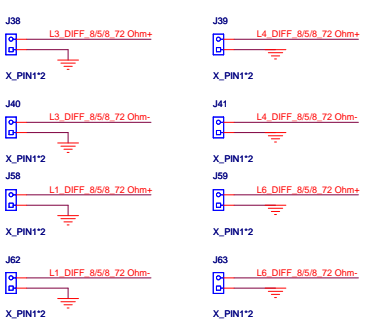
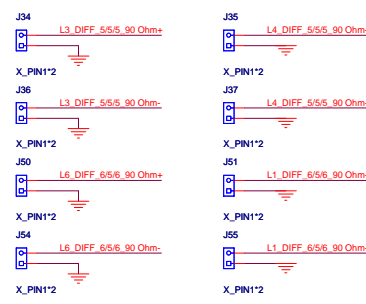
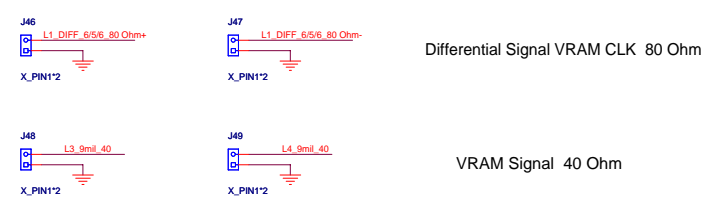
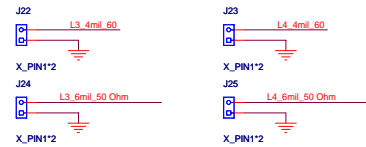
$Iin = (Vels / VrefE) \times (0.075 / RS1)$




FOR EMI



MSI CORPORATION			
File	Screw		
Size	Document Number		Rev
Custom	MS-1634X		0B
Date	Thursday, May 31, 2007	Sheet	48 of 51

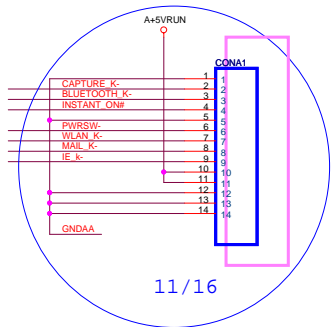
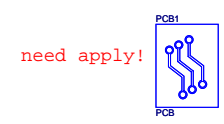
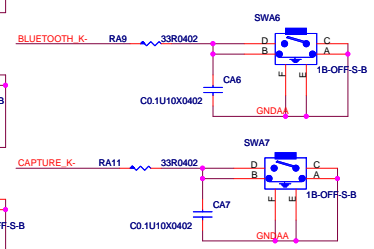
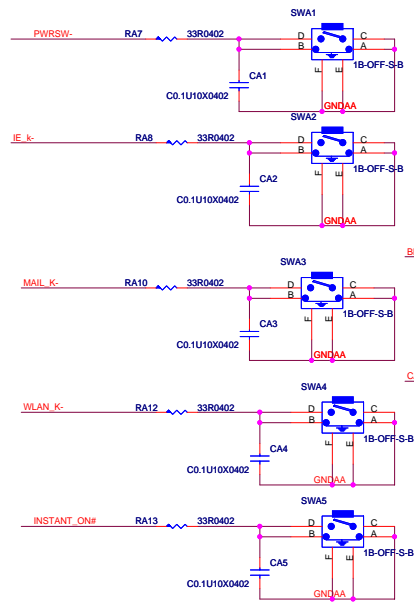
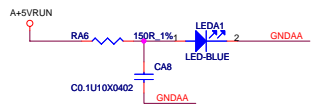


 MICRO-STAR INT'L CO.,LTD.	
IMPEDANCE	
File	Document Number
Size	MS-1634X
Date:	Thursday, May 31, 2007
Sheet	49 of 51
Rev	08

<p>REFERENCE DESIGN</p> <p>THESE SCHEMATICS ARE SUBJECT TO MODIFICATION AND DESIGN IMPROVEMENTS. PLEASE CONTACT ATI FIELD APPLICATION ENGINEERS</p>	<p>RESTRICTION NOTICE</p> <p>THESE SCHEMATICS CONTAIN INFORMATION WHICH IS PROPRIETARY TO AND IS THE PROPERTY OF ATI, AND MAY NOT BE USED, REPRODUCED OR DISCLOSED IN ANY MANNER WITHOUT PERMISSION</p>
--	--

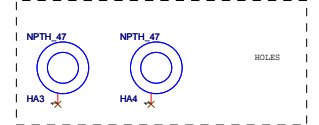
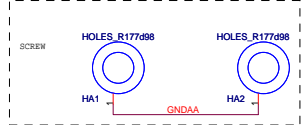
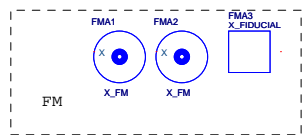
- 01:P13:NB +1.8VRUN change to +1.8VRUN_NB for timing control.
- 02:P07:R471,R473,R475 from 10K to 680 ohm.
- P14:C2047 from 10u 0805 to 0.1u 0402.
- P16:R2017 from 499R to 249R.
- P16:U51.V2SYNC & U51.H2SYNC PU TO +3.3VRUN.
- P16:U51.R2B,U51.G2B,U51.B2B PD 37.5 OHM TO GND.
- P17:ADD +1.8VRUN TO CONTROL, +3.3V_DELAY TIMING FOR M76.
- P17:Q58 FROM 2N7002 TO BSS138.
- P21:R2132 FROM 110R TO 47R.
- P22:EC211 FROM 10pf TO 22pf.
- P23:REMOVE "CARDBUS_RST-" NET FOR R5C833.
- P23:ADD "PCI_INTB#" FOR R5C833 CARD READER.
- P24:USB8 PAIR SWAP WITH USB6 PAIR.
- P28:CARD READER CHIP FROM O2711 TO R5C833.
- P29:REMOVE CARD BUS FUNCTION.
- P32:REMOVE "PCMSPK" FUNCTION.
- P32:ADD R2237,C2368 TO REDUCE MIC NOISE.
- P33:MODIFY LINE IN JACK(CON2016) PIN DEFINE.
- P34:MODIFY GINGER PRINT CONNECTOR(CON2011) PIN DEFINE.
- P36:CHANGE MINI-PCIE CONN FOR DFM.
- P36:GPP_TX,GPP_RX,GPP_CLK SWAP WITH CON2006 & CON30.
- P36:ADD IR MODULE.
- P37:SWAP PIN WITH AC_CTL & IR_K-.
- P37:IR RECIVER POWER FROM +5VALW TO +5VSUS.
- P37:BIOS FROM 4M TO 8M.

NOTE		
File		
Size	Document Number	Rev
Custom	MS-1634X	0B
Date:	Thursday, May 31, 2007	Sheet 51 of 51

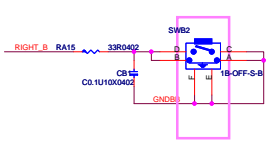
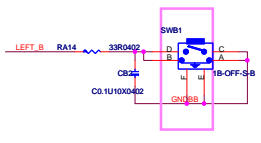


07/01/09 0A->0B

11/16

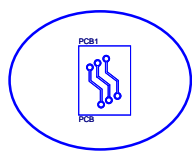
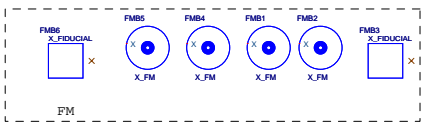
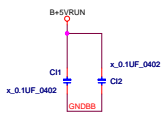
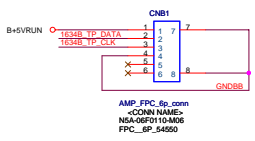
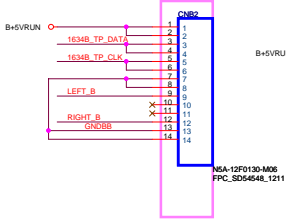


MICRO-STAR INT'L CO.,LTD.	
File	POWER BOARD
Size	Document Number
B	MS-1634A
Date:	Friday, June 01, 2007
Sheet	51 of 53
Rev	0B

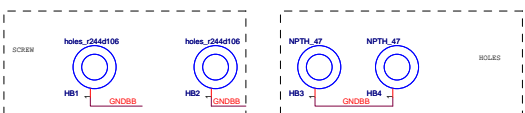


07/01/26 0A->0B ME
07/04/02 0B->0C swap

FOR TM61P-307 Pin define



Need to apply



File		TP Board	
Size	Document Number		
Custom	MS-1634B	Rev	110
Date	Friday, June 01, 2007	Sheet	02 of 03