

MS-7680 Ver:3.2 m-ATX : 245 X 210mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61,Co-lay H67)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71889AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

PWM:

Controller:VRD12 UP1625 4+1 Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT CPU SA

Controller:uP6103

DDR PCH

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX6 Front x8

D-SUB *1

DVI-D PORT*1

HDMI *1

TPM Header *1

COM Header *1

LPT Header *1

on BOARD BUZZER

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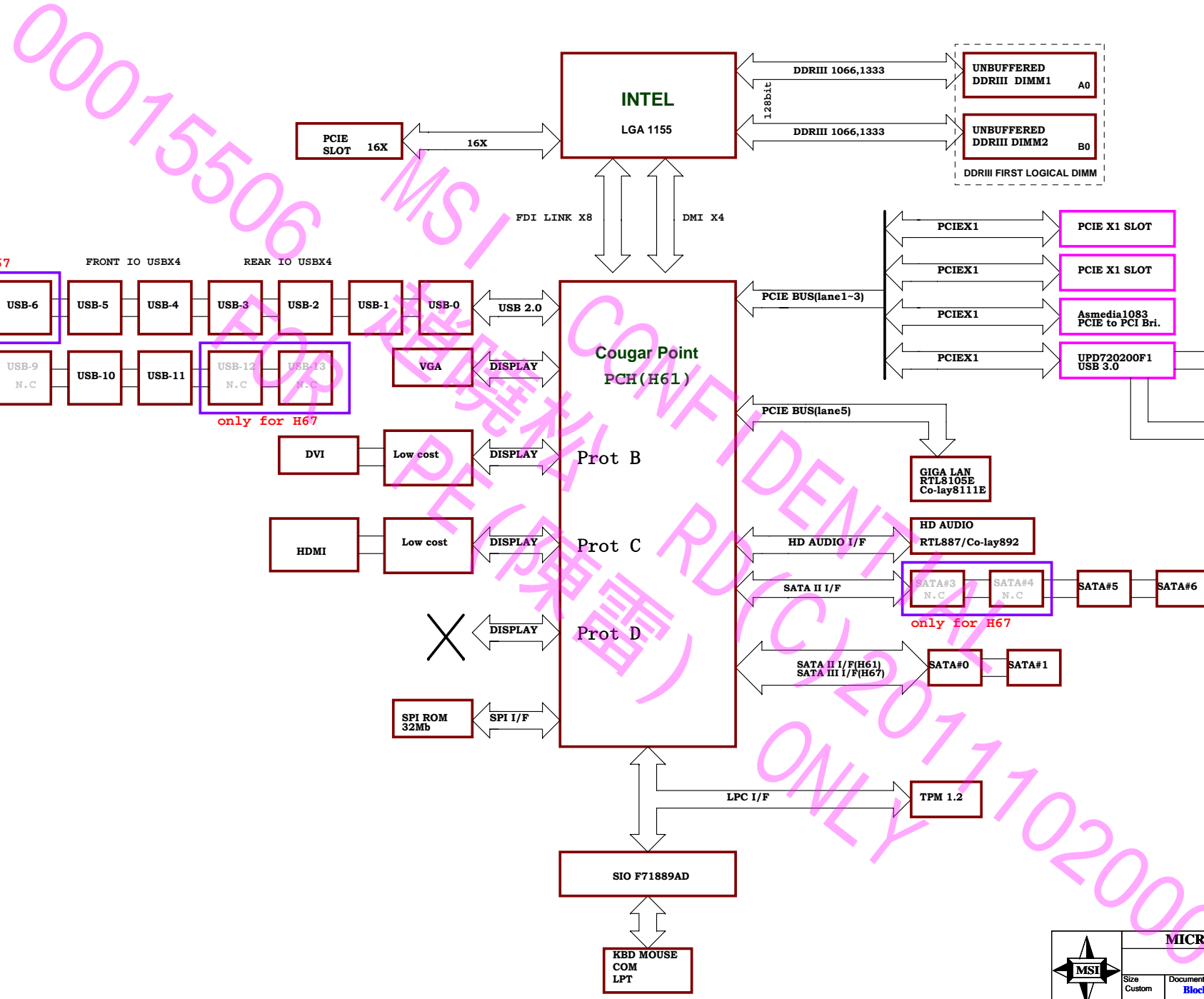


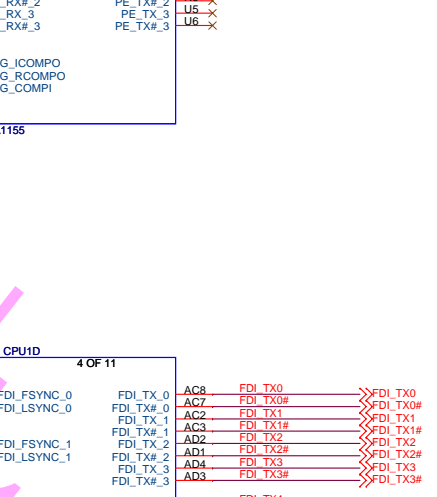
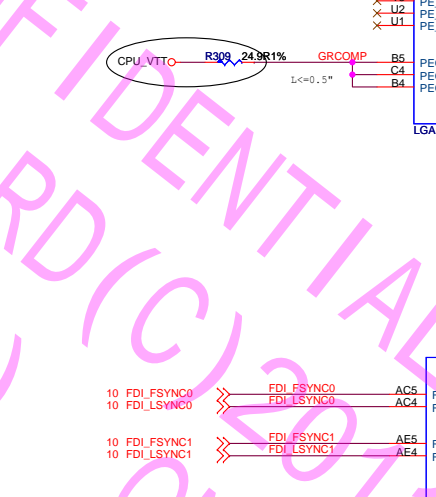
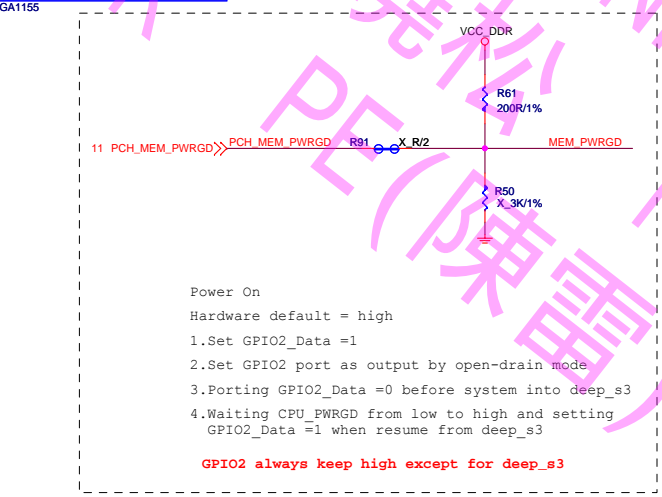
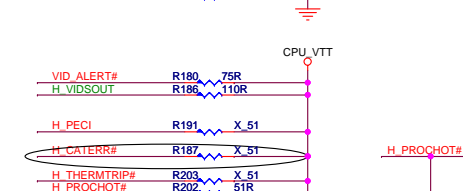
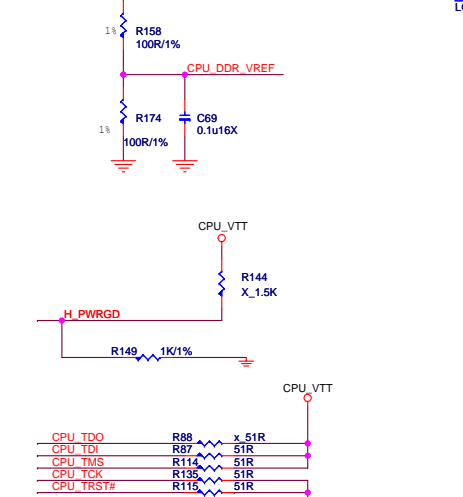
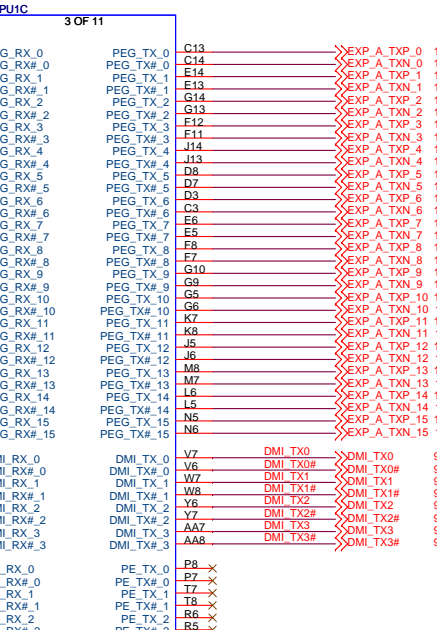
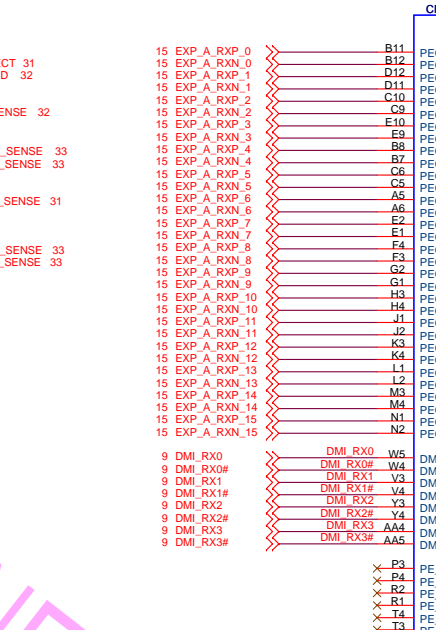
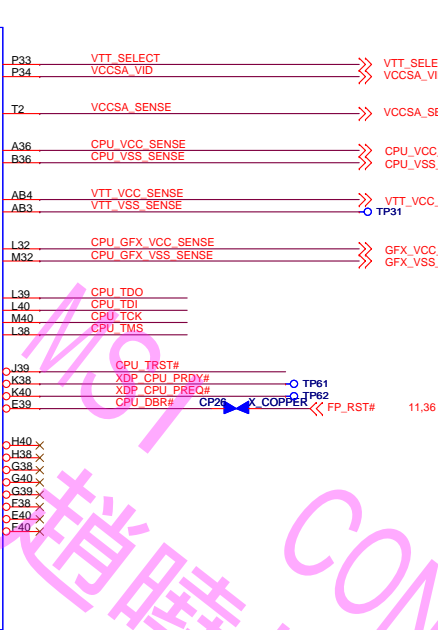
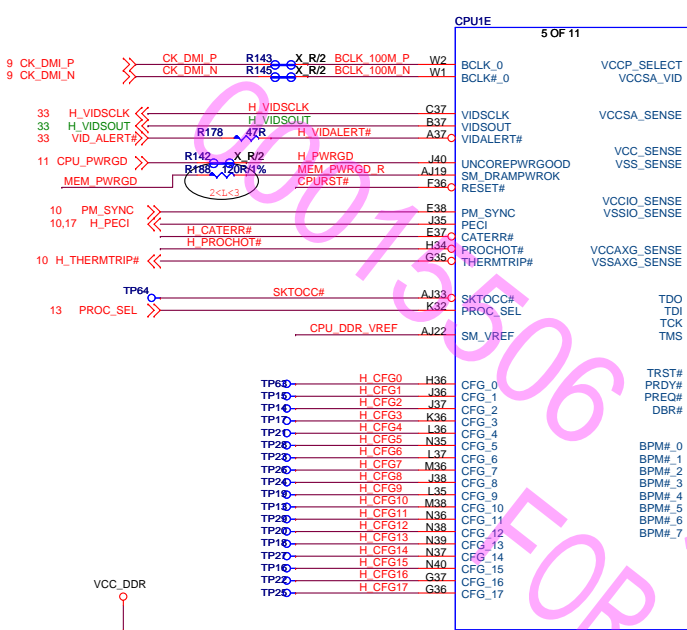
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Size	Document Description	Rev
Custom	Cover Sheet	3.2

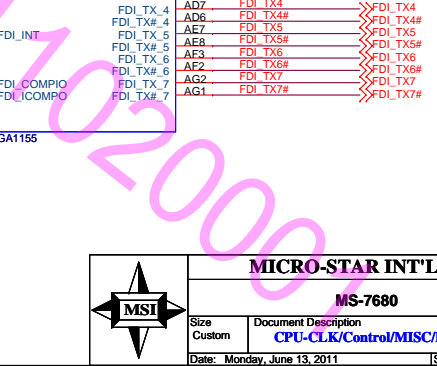
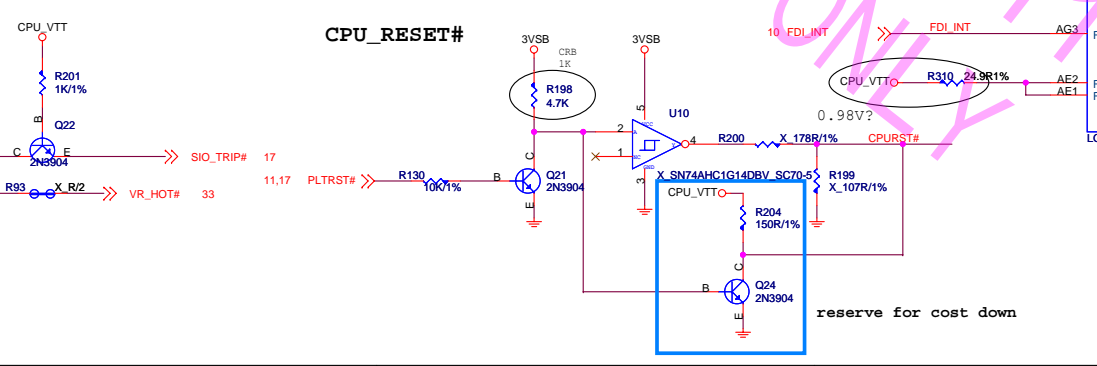
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PEG CONFIG TABLE

SEL2	SEL1	SEL0	PCIe CONFIG
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1	1	0	2 X 8

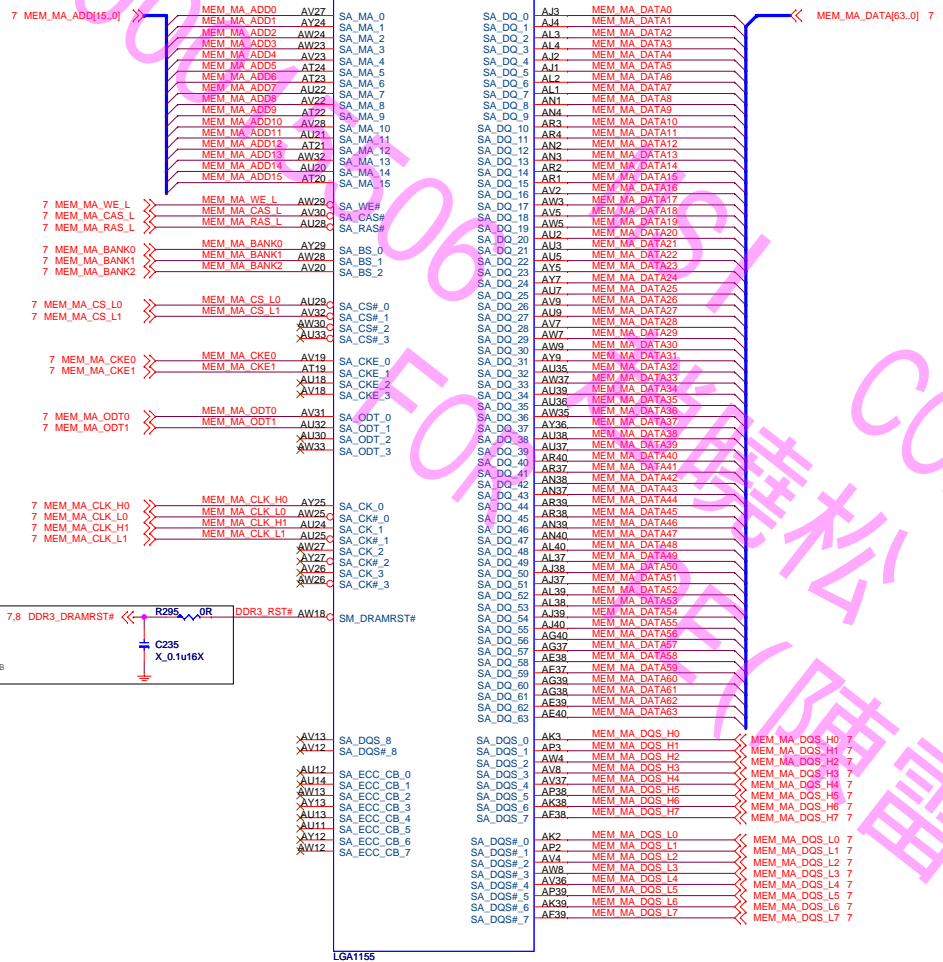


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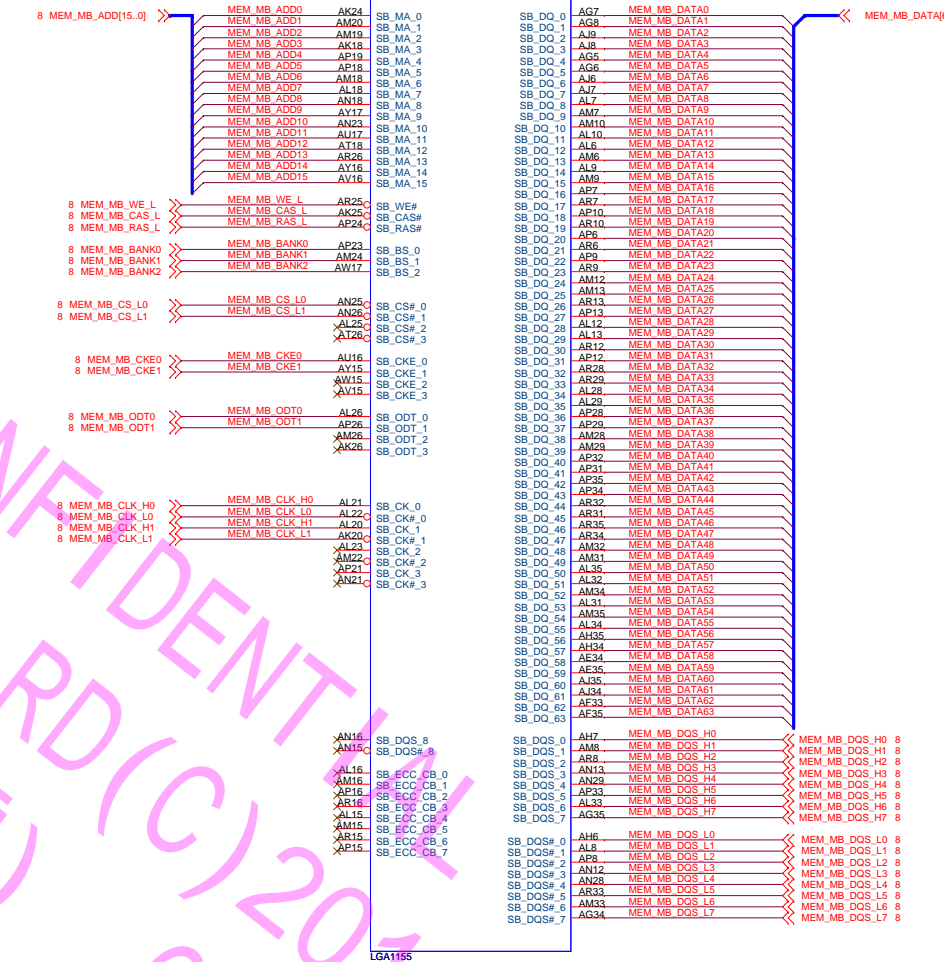
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Size Custom Document Description **GPU-CLK/Control/MISC/PEG** Rev 3.2

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LGA1155



LGA1155

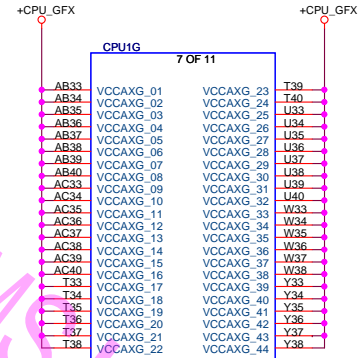
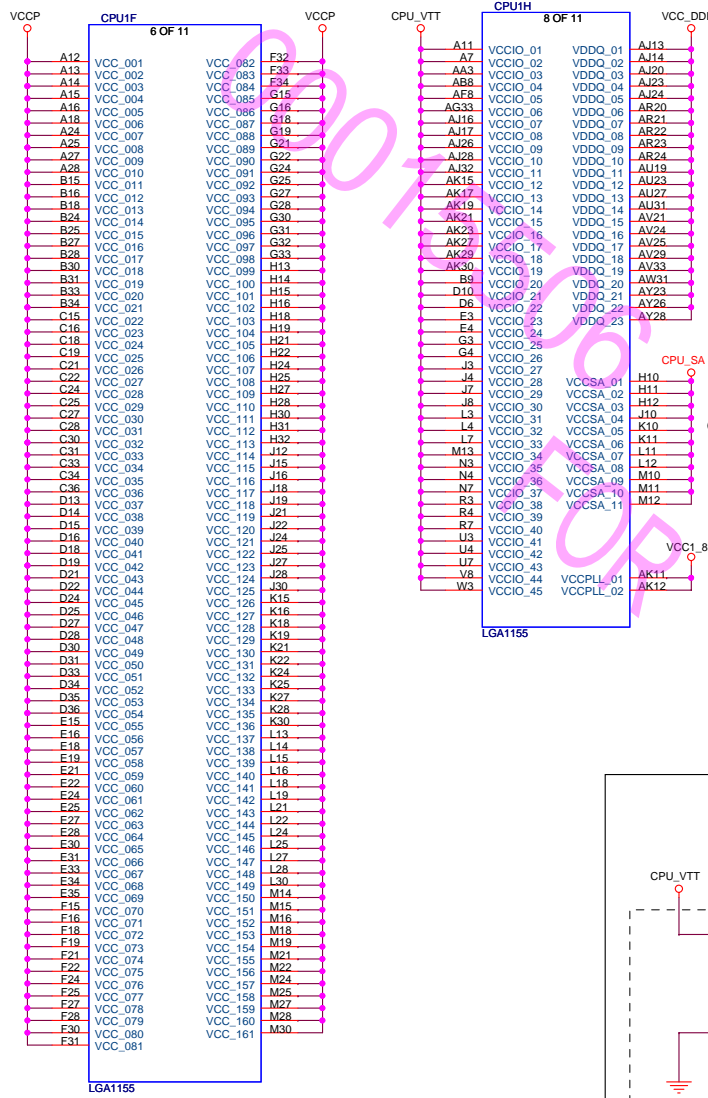
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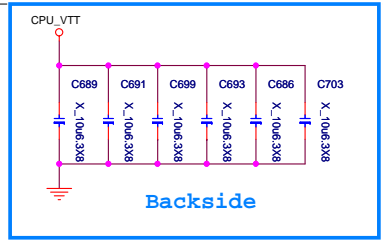
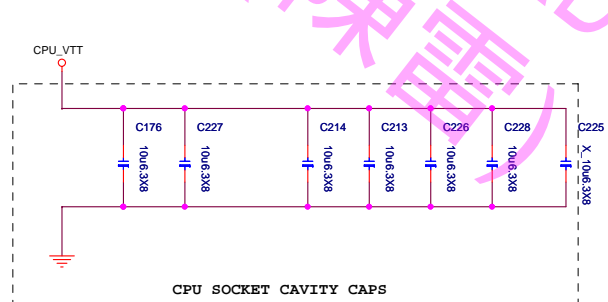
Size Custom	Document Description CPU-Memory	Rev 3.2
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(1.05V / 1.00V)

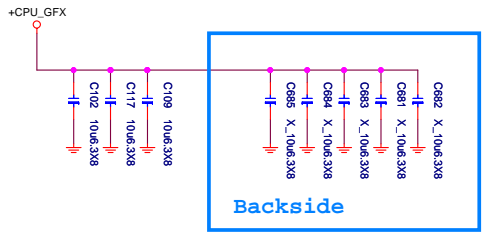


VCCP: 112A
 CPU_VTT: 8.2A
 CPU_SA: 8.8A
 VCC_DDR: 4.5A
 VCC1_8: 1.6A

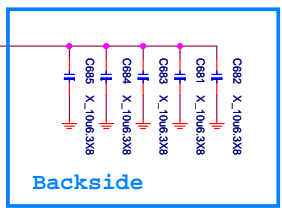
+CPU_VTT Decoupling



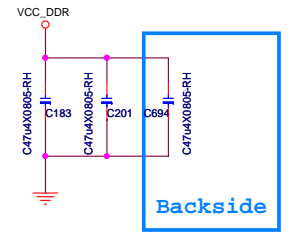
+CPU_GFX Decoupling



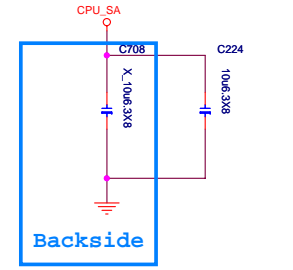
CPU SOCKET CAVITY CAPS



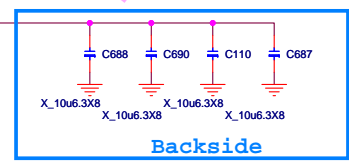
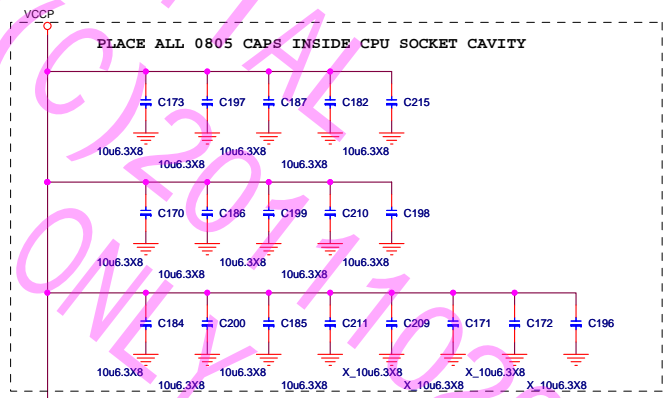
+1.5V_DDR3-Decoupling



CPU SOCKET CAVITY CAPS



+CPU_VCCP-Decoupling



CPU1I
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A17	VSS_001	VSS_091	AM27
A23	VSS_002	VSS_092	AM30
A26	VSS_003	VSS_093	AM36
A29	VSS_004	VSS_094	AM37
A35	VSS_005	VSS_095	AM38
AA33	VSS_006	VSS_096	AM40
AA34	VSS_007	VSS_097	AM5
AA35	VSS_008	VSS_098	AM4
AA36	VSS_009	VSS_099	AM10
AA37	VSS_010	VSS_100	AM11
AA38	VSS_011	VSS_101	AM14
AA6	VSS_012	VSS_102	AM17
AB5	VSS_013	VSS_103	AM19
AC1	VSS_014	VSS_104	AM22
AC6	VSS_015	VSS_105	AM24
AD33	VSS_016	VSS_106	AM27
AD36	VSS_017	VSS_107	AM30
AD38	VSS_018	VSS_108	AM32
AD39	VSS_019	VSS_109	AM33
AD40	VSS_020	VSS_110	AM34
AD5	VSS_021	VSS_111	AM36
AD8	VSS_022	VSS_112	AM37
AE3	VSS_023	VSS_113	AM5
AE33	VSS_024	VSS_114	AM6
AE36	VSS_025	VSS_115	AM7
AF1	VSS_026	VSS_116	AM9
AF34	VSS_027	VSS_117	AM9
AF36	VSS_028	VSS_118	AM9
AF37	VSS_029	VSS_119	AM9
AF40	VSS_030	VSS_120	AP1
AF5	VSS_031	VSS_121	AP11
AF6	VSS_032	VSS_122	AP14
AF7	VSS_033	VSS_123	AP17
AG36	VSS_034	VSS_124	AP22
AH2	VSS_035	VSS_125	AP25
AH3	VSS_036	VSS_126	AP27
AH33	VSS_037	VSS_127	AP30
AH36	VSS_038	VSS_128	AP36
AH37	VSS_039	VSS_129	AP37
AH38	VSS_040	VSS_130	AP4
AH39	VSS_041	VSS_131	AP4
AH40	VSS_042	VSS_132	AP5
AH5	VSS_043	VSS_133	AR11
AH8	VSS_044	VSS_134	AR12
AJ12	VSS_045	VSS_135	AR14
AJ15	VSS_046	VSS_136	AR17
AJ18	VSS_047	VSS_137	AR18
AJ21	VSS_048	VSS_138	AR19
AJ25	VSS_049	VSS_139	AR27
AJ27	VSS_050	VSS_140	AR30
AJ36	VSS_051	VSS_141	AR36
AJ5	VSS_052	VSS_142	AR5
AK1	VSS_053	VSS_143	AT1
AK10	VSS_054	VSS_144	AT10
AK13	VSS_055	VSS_145	AT12
AK14	VSS_056	VSS_146	AT13
AK16	VSS_057	VSS_147	AT15
AK22	VSS_058	VSS_148	AT16
AK28	VSS_059	VSS_149	AT17
AK31	VSS_060	VSS_150	AT2
AK32	VSS_061	VSS_151	AT25
AK33	VSS_062	VSS_152	AT27
AK34	VSS_063	VSS_153	AT28
AK35	VSS_064	VSS_154	AT29
AK36	VSS_065	VSS_155	AT3
AK37	VSS_066	VSS_156	AT30
AK4	VSS_067	VSS_157	AT31
AK40	VSS_068	VSS_158	AT32
AK5	VSS_069	VSS_159	AT33
AK6	VSS_070	VSS_160	AT34
AK7	VSS_071	VSS_161	AT35
AK8	VSS_072	VSS_162	AT36
AK9	VSS_073	VSS_163	AT37
AL11	VSS_074	VSS_164	AT38
AL14	VSS_075	VSS_165	AT39
AL17	VSS_076	VSS_166	AT4
AL19	VSS_077	VSS_167	AT40
AL24	VSS_078	VSS_168	AT5
AL27	VSS_079	VSS_169	AT6
AL30	VSS_080	VSS_170	AT7
AL36	VSS_081	VSS_171	AT8
AL5	VSS_082	VSS_172	AT9
AM1	VSS_083	VSS_173	AU1
AM11	VSS_084	VSS_174	AU15
AM14	VSS_085	VSS_175	AU26
AM17	VSS_086	VSS_176	AU34
AM2	VSS_087	VSS_177	AU4
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AM25	VSS_090	VSS_180	AV10

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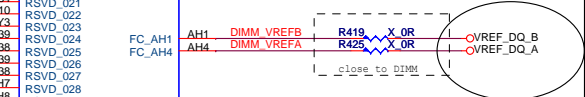
CPU1J
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AV11	VSS_181	VSS_281	H37
AV14	VSS_182	VSS_282	H39
AV17	VSS_183	VSS_283	H5
AV3	VSS_184	VSS_284	H6
AV35	VSS_185	VSS_285	H9
AV38	VSS_186	VSS_286	H11
AV6	VSS_187	VSS_287	H17
AW10	VSS_188	VSS_288	H20
AW11	VSS_189	VSS_289	H23
AW14	VSS_190	VSS_290	H26
AW16	VSS_191	VSS_291	H29
AW36	VSS_192	VSS_292	H32
AW6	VSS_193	VSS_293	H31
AY11	VSS_194	VSS_294	K12
AY14	VSS_195	VSS_295	K13
AY18	VSS_196	VSS_296	K14
AY35	VSS_197	VSS_297	K17
AY4	VSS_198	VSS_298	K2
AY6	VSS_199	VSS_299	K20
AY8	VSS_200	VSS_300	K23
B10	VSS_201	VSS_301	K26
B13	VSS_202	VSS_302	K29
B14	VSS_203	VSS_303	K33
B17	VSS_204	VSS_304	K35
B23	VSS_205	VSS_305	K37
B25	VSS_206	VSS_306	K39
B26	VSS_207	VSS_307	K5
B32	VSS_208	VSS_308	K6
B35	VSS_209	VSS_309	L10
B38	VSS_210	VSS_310	L17
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C17	VSS_214	VSS_314	L29
C17	VSS_215	VSS_315	L4
C20	VSS_216	VSS_316	M1
C22	VSS_217	VSS_317	M17
C26	VSS_218	VSS_318	M2
C29	VSS_219	VSS_319	M20
C32	VSS_220	VSS_320	M23
C35	VSS_221	VSS_321	M26
C7	VSS_222	VSS_322	M29
C8	VSS_223	VSS_323	M33
D17	VSS_224	VSS_324	M37
D2	VSS_225	VSS_325	M39
D20	VSS_226	VSS_326	M43
D23	VSS_227	VSS_327	M5
D26	VSS_228	VSS_328	M6
D29	VSS_229	VSS_329	M9
D32	VSS_230	VSS_330	M21
D37	VSS_231	VSS_331	N8
D39	VSS_232	VSS_332	P1
D4	VSS_233	VSS_333	P2
D9	VSS_234	VSS_334	P26
D9	VSS_235	VSS_335	P38
E11	VSS_236	VSS_336	P40
E12	VSS_237	VSS_337	P5
E17	VSS_238	VSS_338	P6
E20	VSS_239	VSS_339	R33
E23	VSS_240	VSS_340	R35
E26	VSS_241	VSS_341	R37
E29	VSS_242	VSS_342	R39
E32	VSS_243	VSS_343	R8
E36	VSS_244	VSS_344	T1
E7	VSS_245	VSS_345	T5
E8	VSS_246	VSS_346	T6
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F13	VSS_249	VSS_349	V2
F14	VSS_250	VSS_350	V33
F17	VSS_251	VSS_351	V34
F2	VSS_252	VSS_352	V35
F20	VSS_253	VSS_353	V36
F23	VSS_254	VSS_354	V37
F26	VSS_255	VSS_355	V38
F29	VSS_256	VSS_356	V39
F35	VSS_257	VSS_357	V40
F37	VSS_258	VSS_358	V5
F39	VSS_259	VSS_359	V6
F5	VSS_260	VSS_360	V5
F6	VSS_261	VSS_360	V8
F9	VSS_262	VSS_360	V8
G11	VSS_263	VSS_360	V8
G12	VSS_264	VSS_360	V8
G17	VSS_265	VSS_360	V8
G20	VSS_266	VSS_360	V8
G23	VSS_267	VSS_360	V8
G26	VSS_268	VSS_360	V8
G29	VSS_269	VSS_360	V8
G34	VSS_270	VSS_360	V8
G7	VSS_271	VSS_360	V8
G8	VSS_272	VSS_360	V8
H1	VSS_273	VSS_NCTF_01	A4
H17	VSS_274	VSS_NCTF_02	AV39
H2	VSS_275	VSS_NCTF_03	AY37
H20	VSS_276	VSS_NCTF_04	B3
H23	VSS_277	VSS_NCTF_04	B3
H26	VSS_278	VSS_NCTF_04	B3
H29	VSS_279	VSS_NCTF_04	B3
H33	VSS_280	VSS_NCTF_04	B3
H35	VSS_280	VSS_NCTF_04	B3

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×C40	RSVD_001	RSVD_036	L33 ×
×D40	RSVD_002	RSVD_037	L34 ×
×AB6	RSVD_003	RSVD_038	L9 ×
×AB7	RSVD_004	RSVD_039	M34 ×
×AD37	RSVD_005	RSVD_040	N33 ×
×AE6	RSVD_006	RSVD_041	N34 ×
×AE4	RSVD_007	RSVD_043	P26 ×
×AG4	RSVD_008	RSVD_044	P37 ×
×A111	RSVD_009	RSVD_045	P39 ×
×AJ29	RSVD_010	RSVD_046	R34 ×
×AJ30	RSVD_011	RSVD_047	R36 ×
×AJ31	RSVD_012	RSVD_048	R38 ×
×AN20	RSVD_013	RSVD_049	R40 ×
×AP20	RSVD_014	RSVD_050	J31 ×
×AT11	RSVD_015	RSVD_051	AD34 ×
×AT14	RSVD_016	RSVD_052	AD35 ×
×AU10	RSVD_017	RSVD_053	K31 ×
×AV1	RSVD_018	RSVD_053	K31 ×
×AV34	RSVD_019	RSVD_053	K31 ×
×AW2	RSVD_020	RSVD_053	K31 ×
×AW34	RSVD_021	RSVD_053	K31 ×
×AY10	RSVD_022	RSVD_053	K31 ×
×AY3	RSVD_023	RSVD_053	K31 ×
×B39	RSVD_024	RSVD_053	K31 ×
×C38	RSVD_025	RSVD_053	K31 ×
×C39	RSVD_026	RSVD_053	K31 ×
×D38	RSVD_027	RSVD_053	K31 ×
×H7	RSVD_028	RSVD_053	K31 ×
×H6	RSVD_029	RSVD_053	K31 ×
×J33	RSVD_030	RSVD_053	K31 ×
×J34	RSVD_031	RSVD_053	K31 ×
×J9	RSVD_032	RSVD_053	K31 ×
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×K9	RSVD_034	RSVD_053	K31 ×
×L31	RSVD_035	RSVD_053	K31 ×

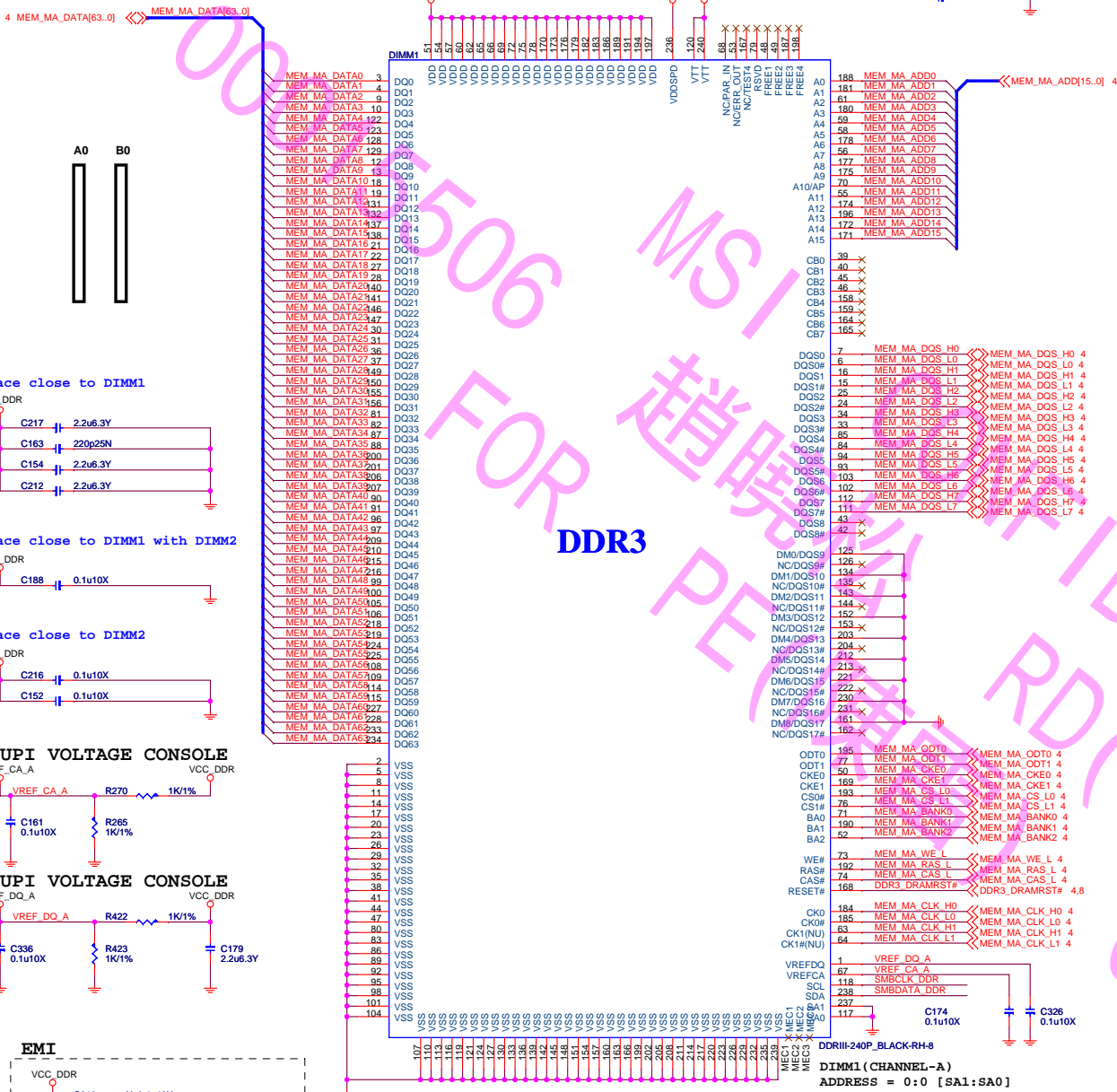


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	MICRO-STAR INT'L CO.,LTD	
	MS-7680	
Size Custom	Document Description CPU-GND	Rev 3.2
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DDRIII DIMM_A0

DDRIII DIMM_A1



Place close to DIMM1

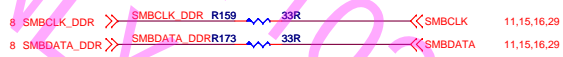
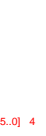
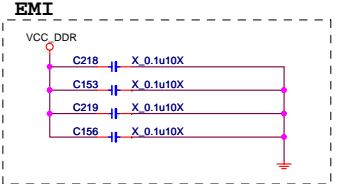
Place close to DIMM1 with DIMM2

Place close to DIMM2

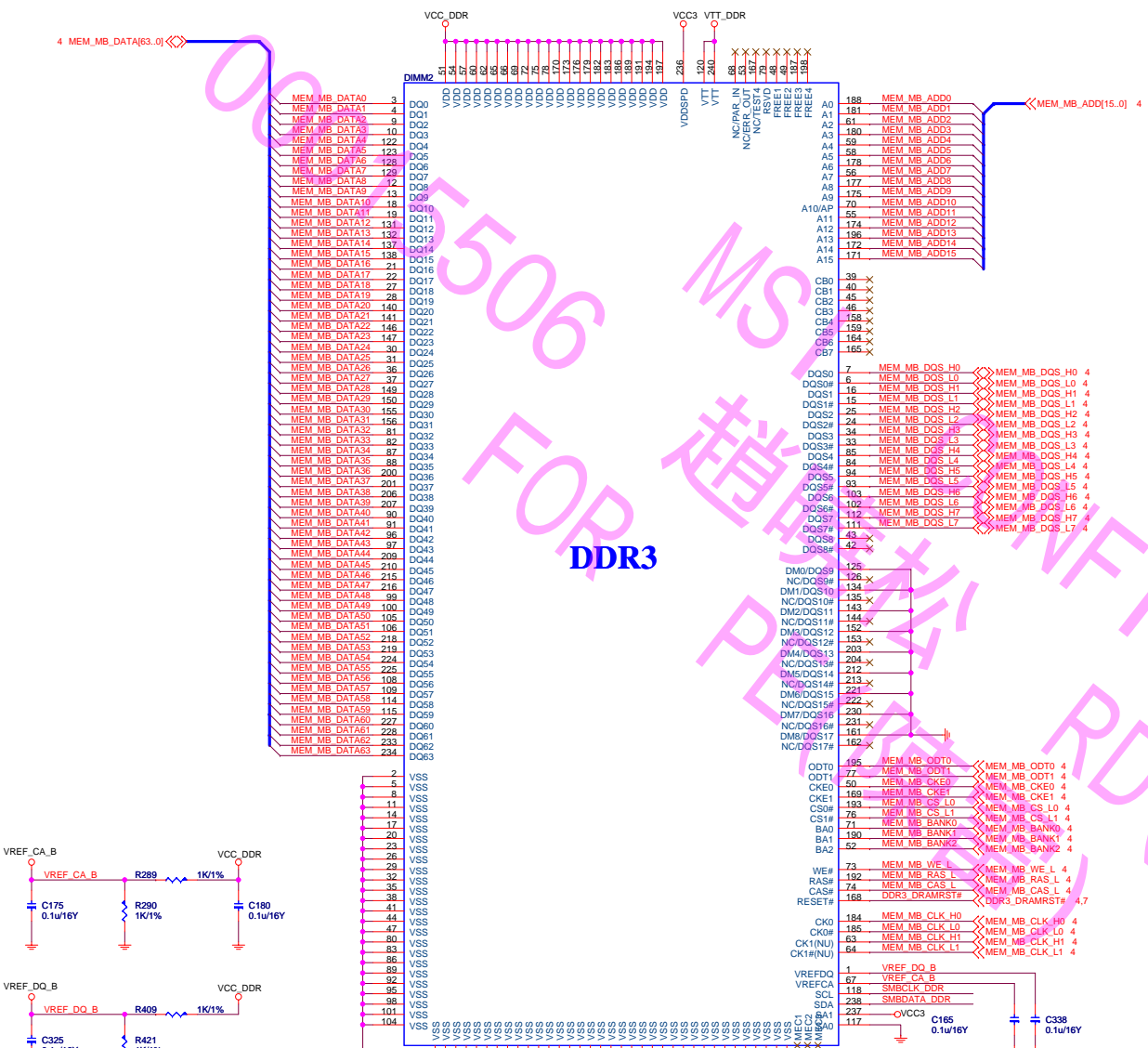
UPI VOLTAGE CONSOLE

UPI VOLTAGE CONSOLE

DDR3



DDR3 DIMM_B0



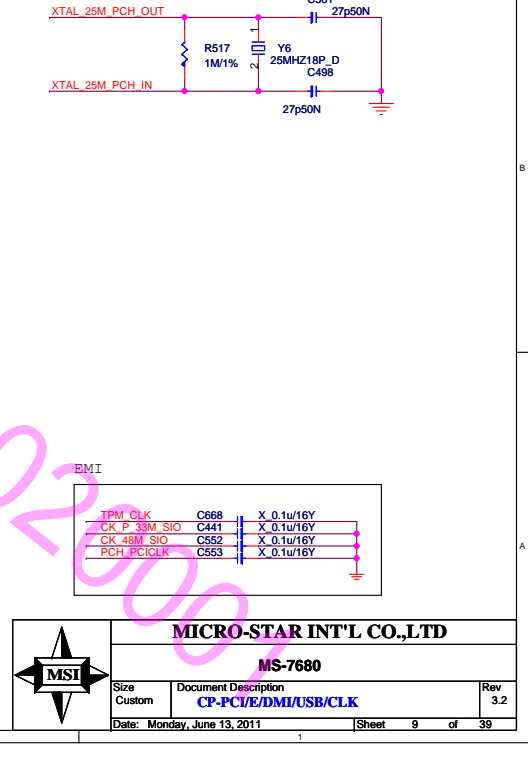
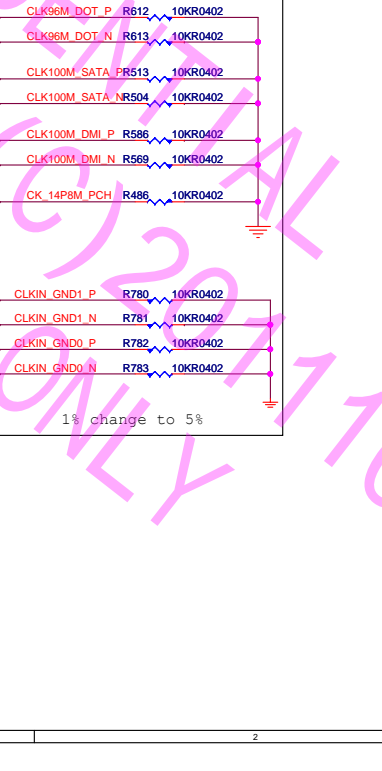
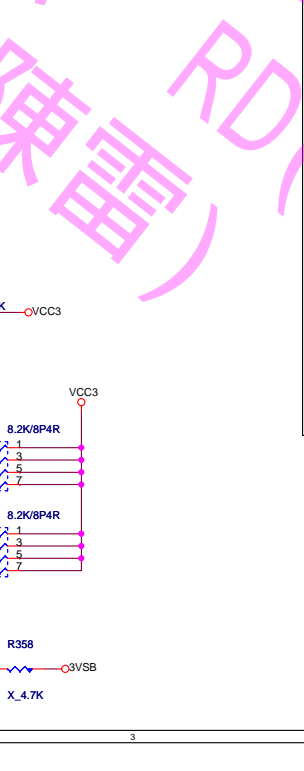
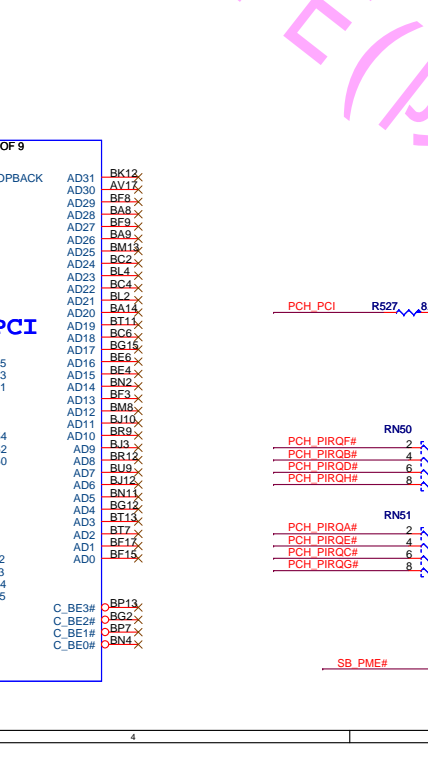
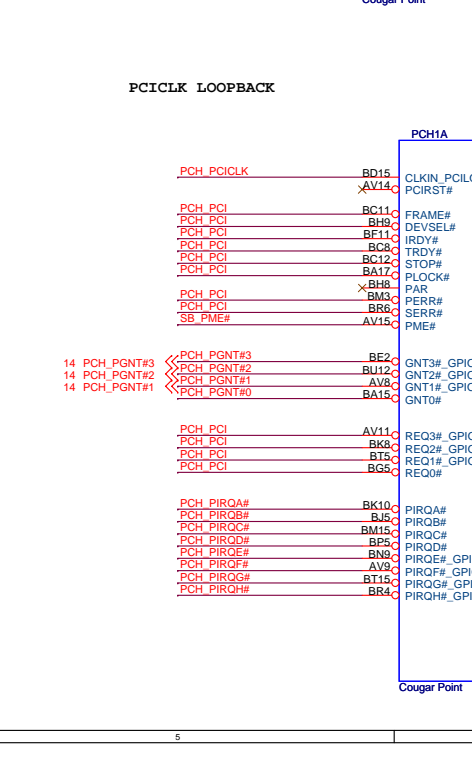
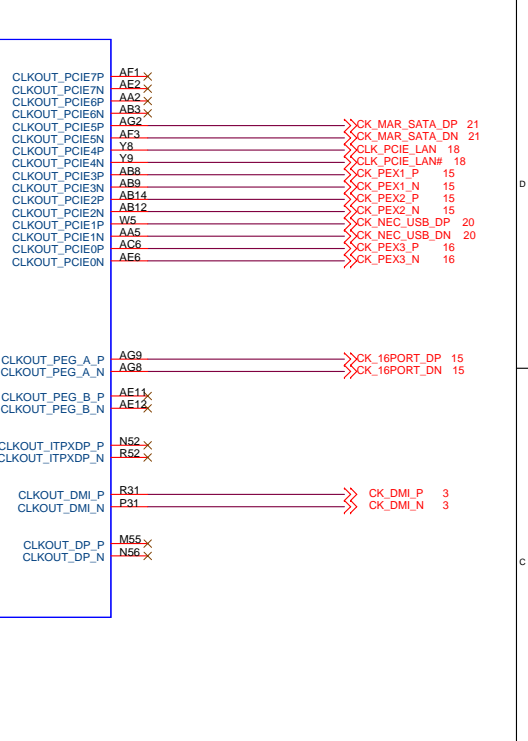
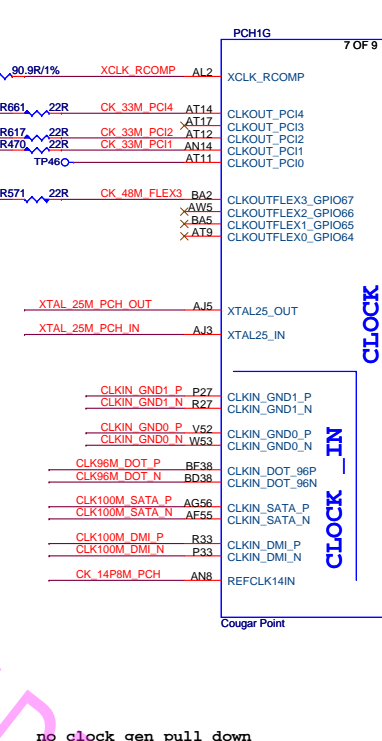
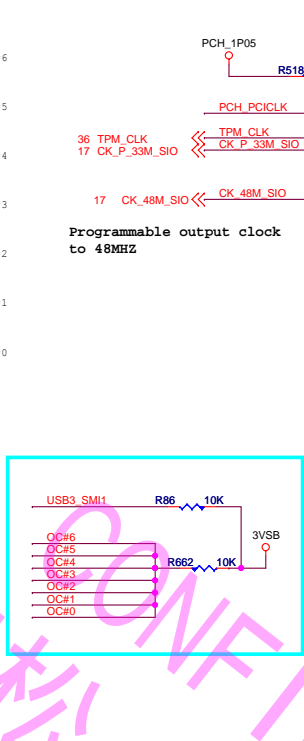
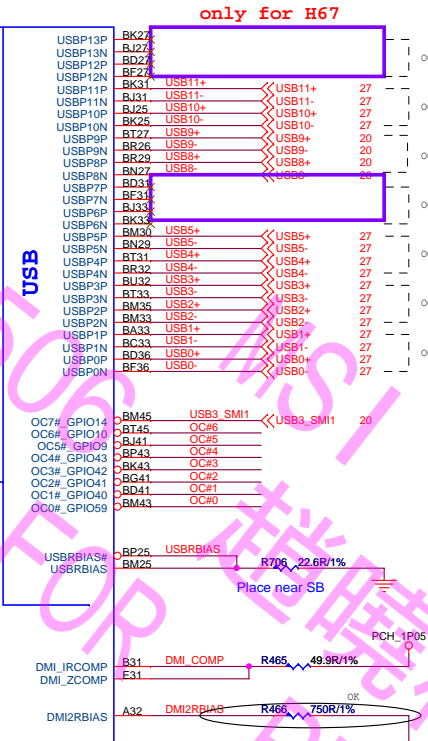
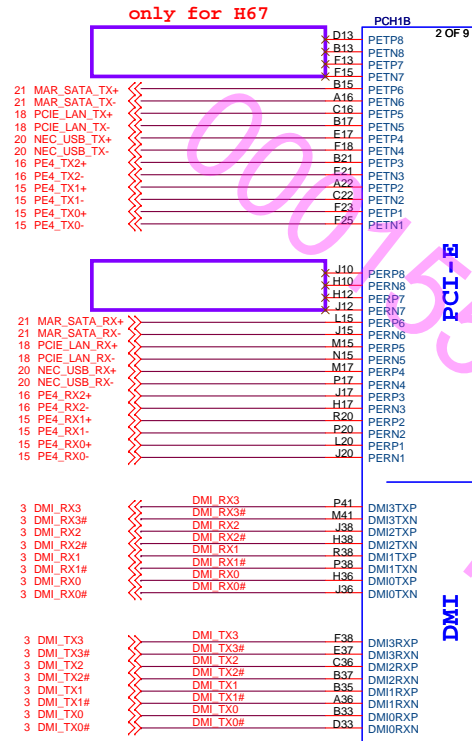
DDR3

506 MS 建興科技 WFI IDENTICAL 2011102000
 FOR 建興科技 WFI IDENTICAL 2011102000

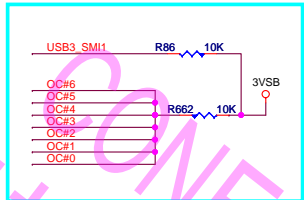
DDR3-240P_BLACK-RH-8
 DIMM2 (CHANNEL-B)
 ADDRESS = 1:0 [SA1:SA0]

SMBCLK_DDR << SMBCLK_DDR 7
 SMBDATA_DDR << SMBDATA_DDR 7

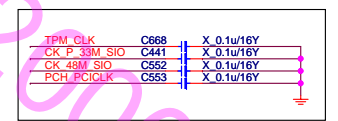
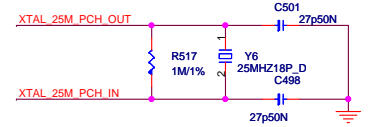
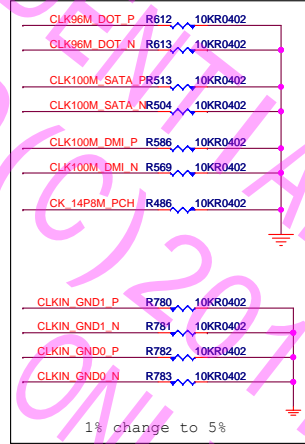
		MICRO-STAR INT'L CO.,LTD	
MS-7680			
Size	Document Description	Rev	
Custom	DDR III DIMM 3 / DIMM 4	3.2	
Date:	Monday, June 13, 2011	Sheet	8 of 39



Programmable output clock to 48MHZ



no clock gen pull down



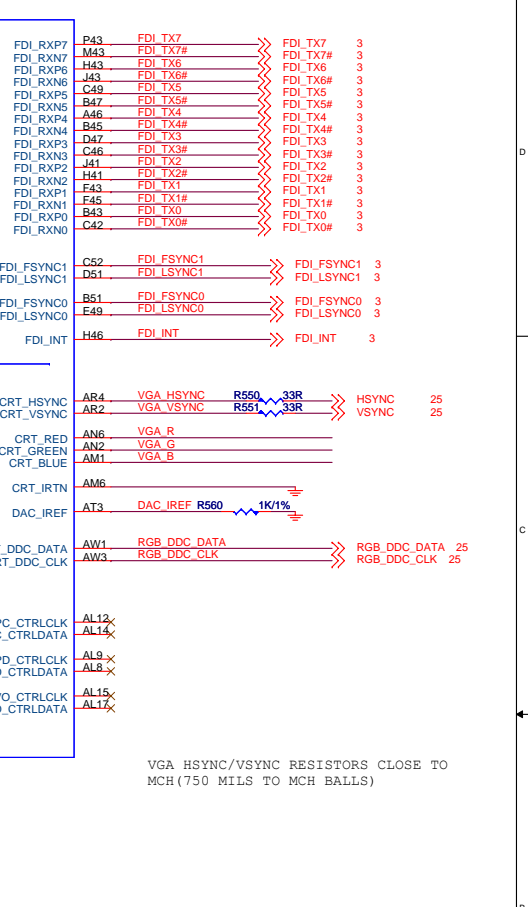
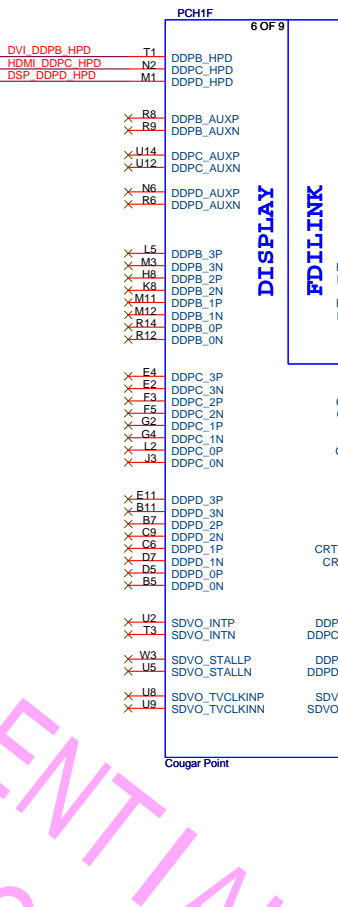
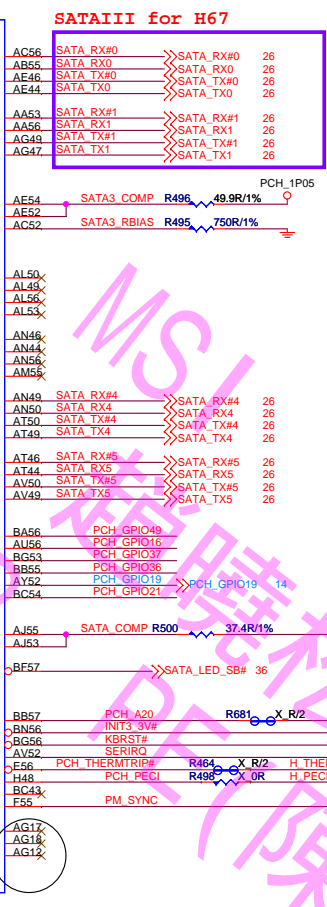
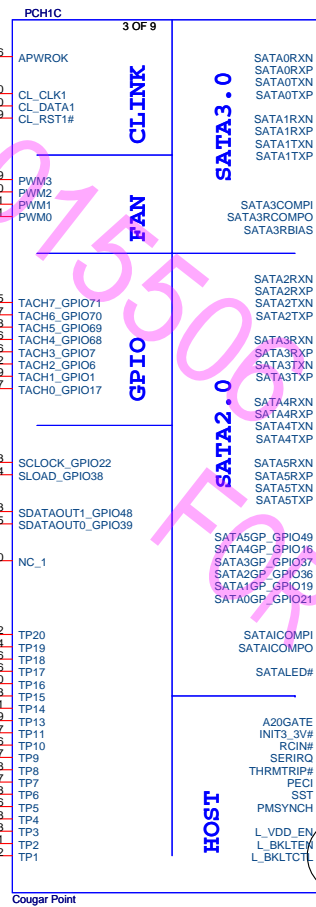
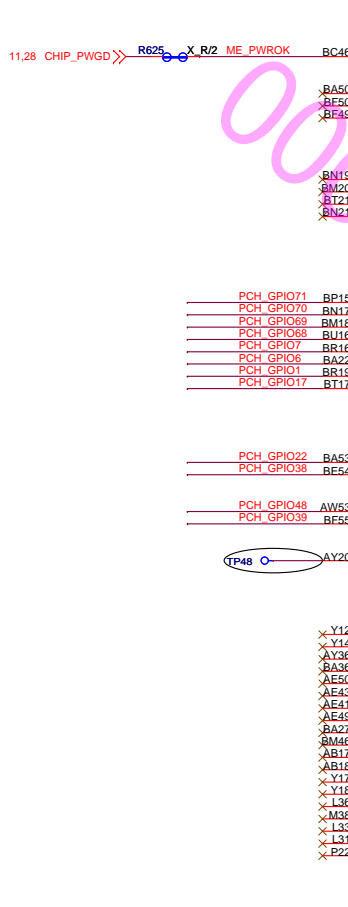
MSI

MICRO-STAR INT'L CO.,LTD

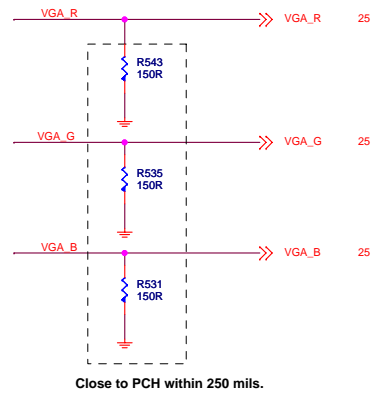
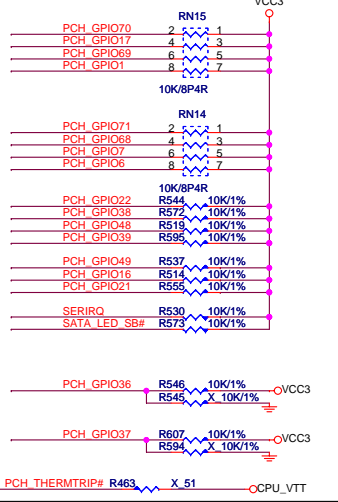
MS-7680

Size Custom Document Description CP-PCI/E/DMI/USB/CLK Rev 3.2

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Pull HIGH for PCH



No VGA(pull down)

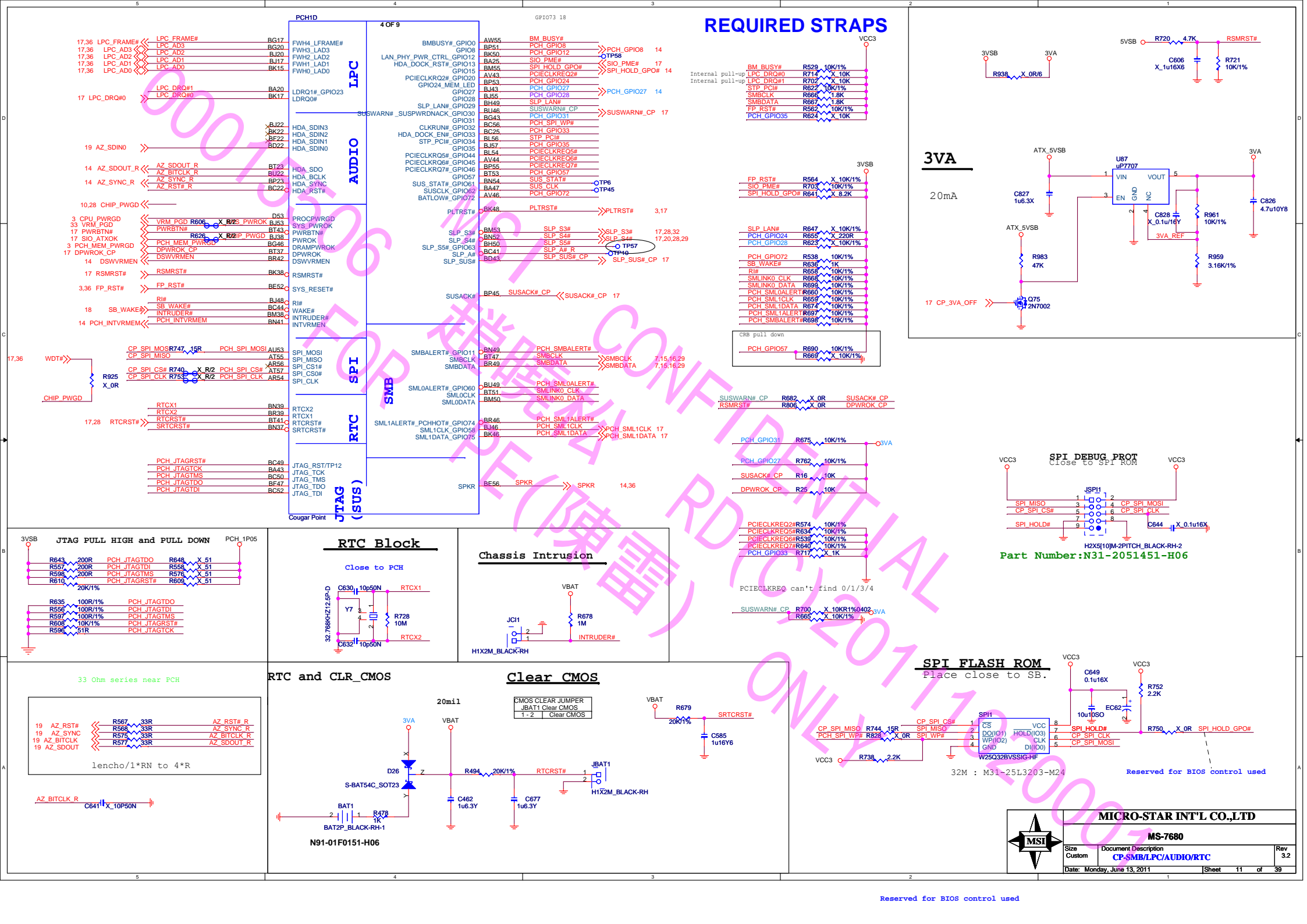
Enable VGA(CTRLCLK/DATA Pull High)



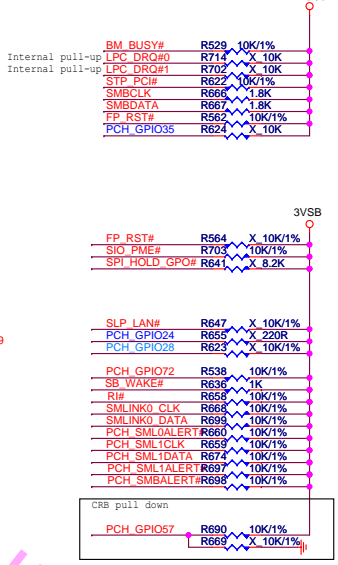
MICRO-STAR INT'L CO.,LTD

MS-7680

Size Custom	Document Description CP-SATA/HOST/FAN/GPIO/VGA	Rev 3.2
Date: Monday, June 13, 2011	Sheet 10 of 39	

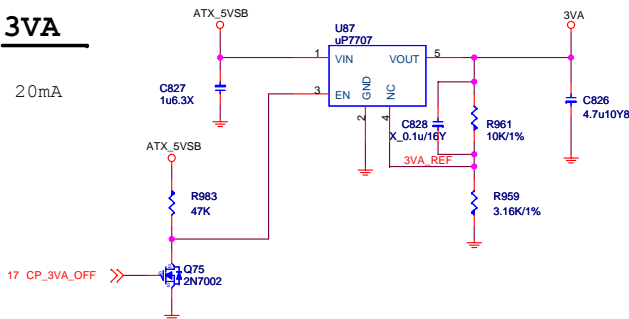


REQUIRED STRAPS

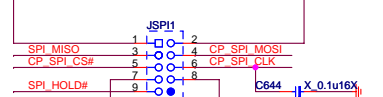


3VA

20mA



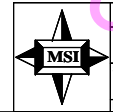
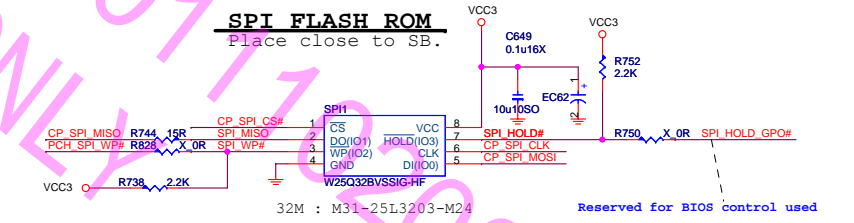
SPI DEBUG PROT



Part Number: N31-2051451-H06

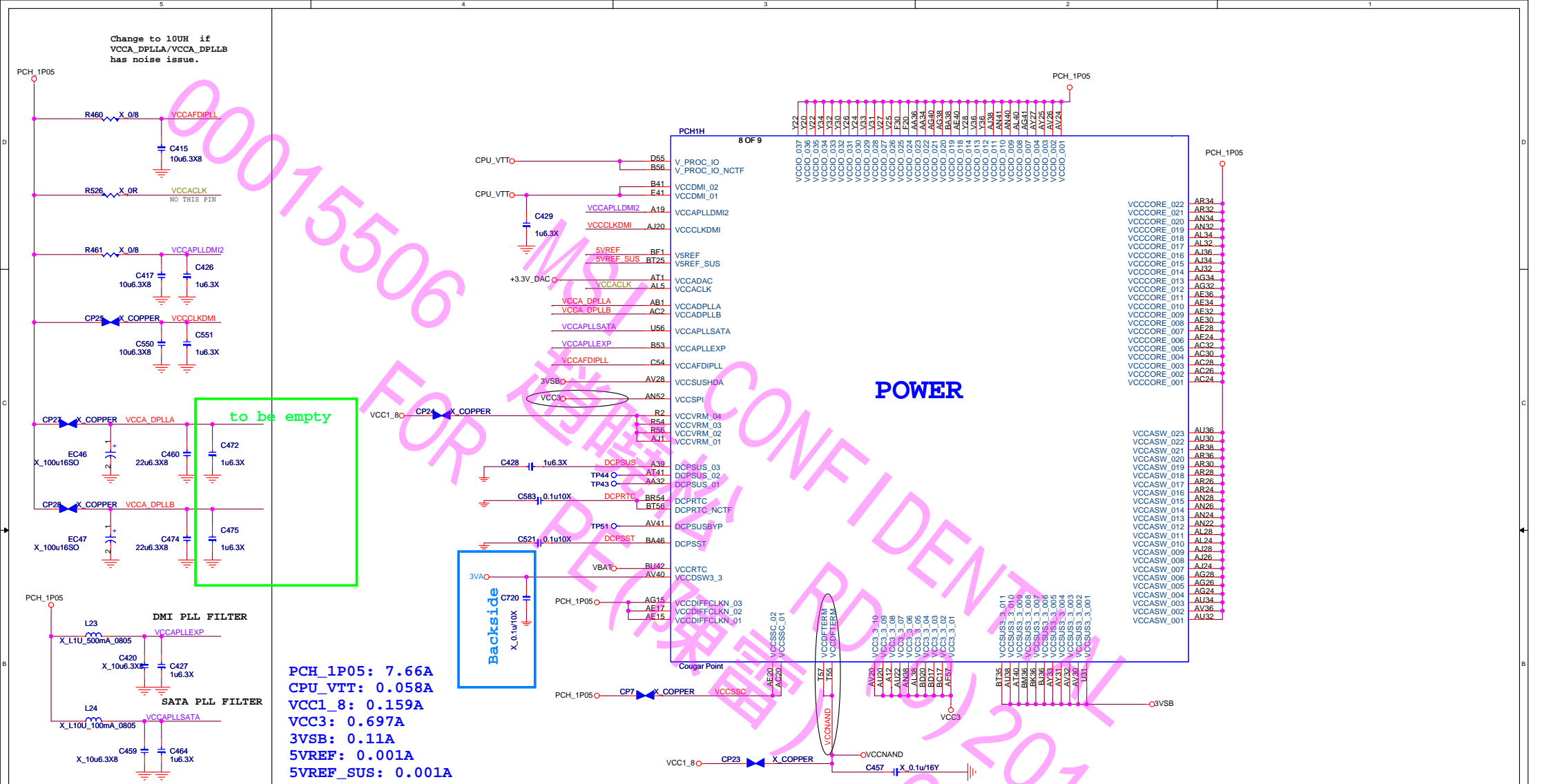
SPI FLASH ROM

Place close to SB.

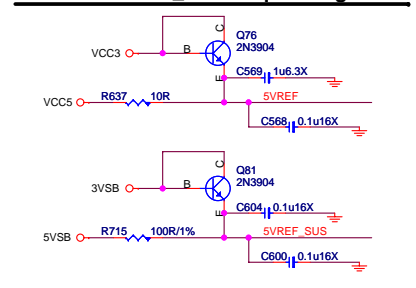


MICRO-STAR INT'L CO.,LTD

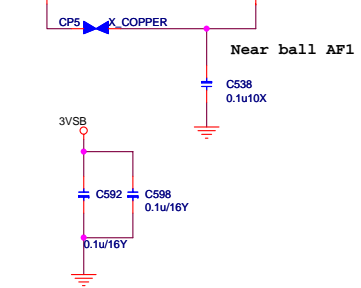
MSI	MS-7680		Rev 3.2
Size Custom	Document Description	CP-SMB/LPC/AUDIO/RTC	
Date: Monday, June 13, 2011	Sheet	11	of 39



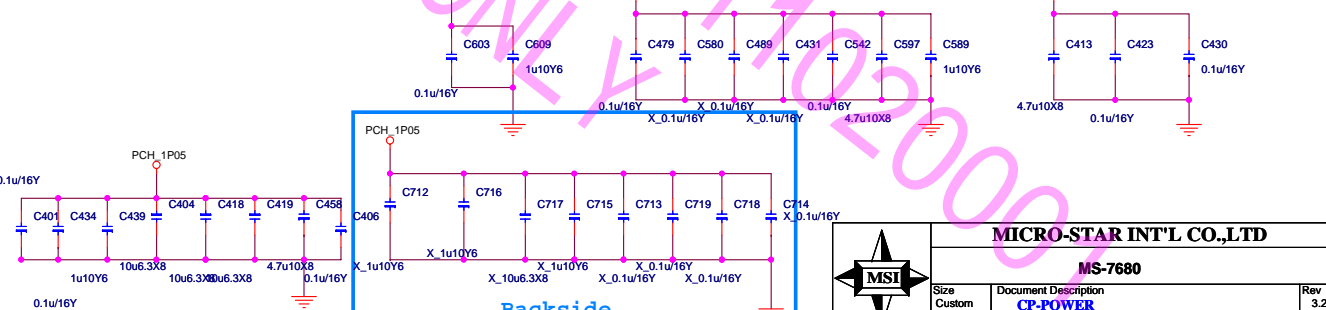
5VREF & 5VREF_SUS Sequencing Circuit



Near ball AF1



PCH decoupling cap

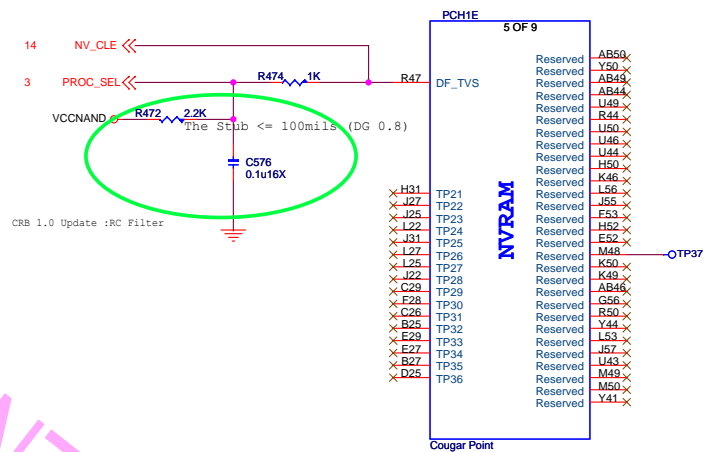
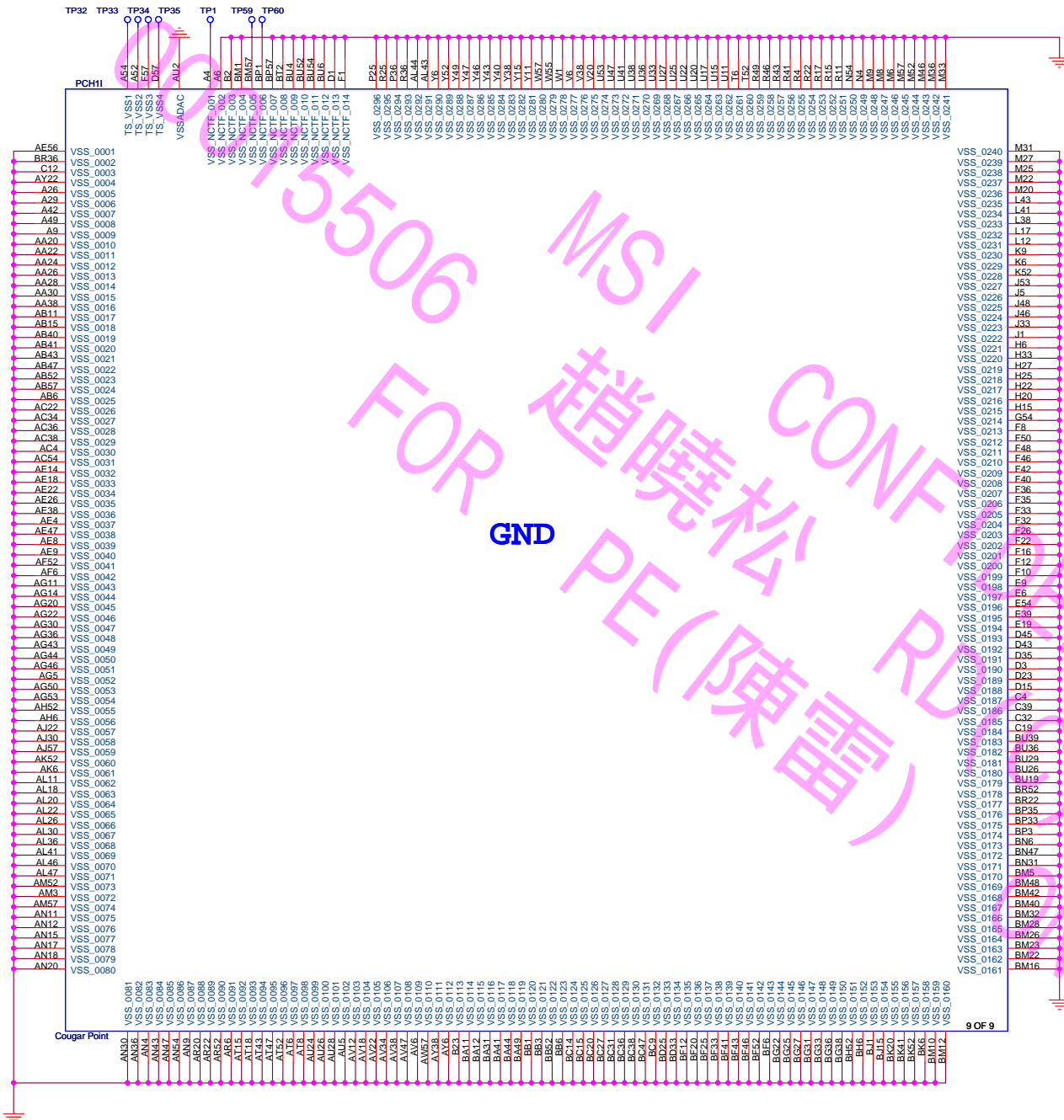


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CP-POWER	3.2

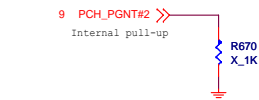
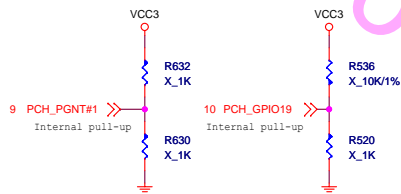
Date: Monday, June 13, 2011 | Sheet 12 of 39



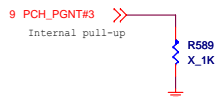
		MICRO-STAR INT'L CO.,LTD	
		MS-7680	
Size Custom	Document Description CP-GND/NVRAM		Rev 3.2
Date: Monday, June 13, 2011		Sheet 13 of 39	

PCH Straps

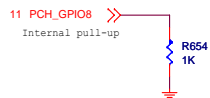
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



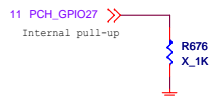
DMI AC/DC MODE
0 : AC
1 : DC *



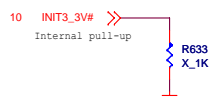
Topblock swap override when pull-low
Signal has a weak internal pull-up



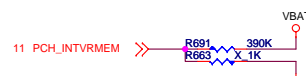
GPIO8
0 : Integrated Clocking Enable (FCIM) *
1 : Buffer Through Mode Enable (BTM)



GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INIT3_3V#
0 : ??????????????????
1 : ?????????????????? *



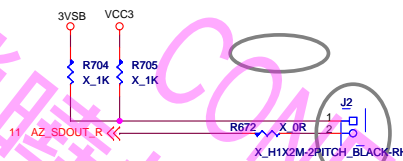
INTVRMEM
0 : DISABLE INTERNAL VRM
1 : ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



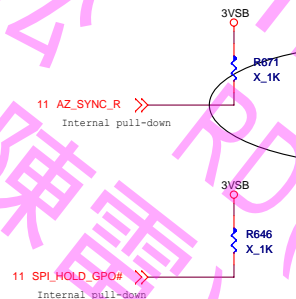
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.



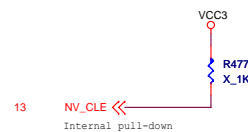
HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

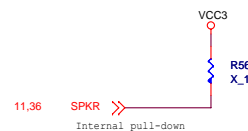


HDA_SYNC
OD PLL VR SUPPLY SEL
0 : 1.8V SUPPLY *
1 : 1.5V SUPPLY

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



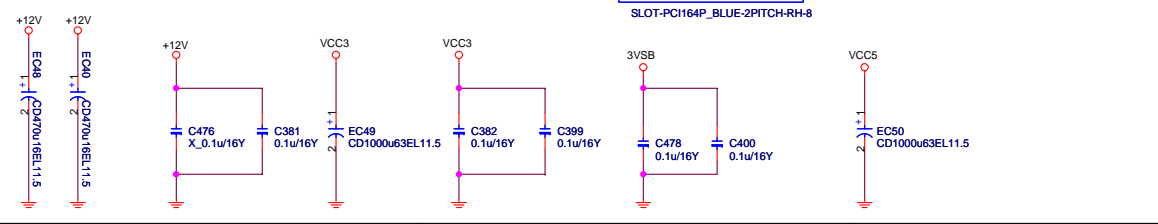
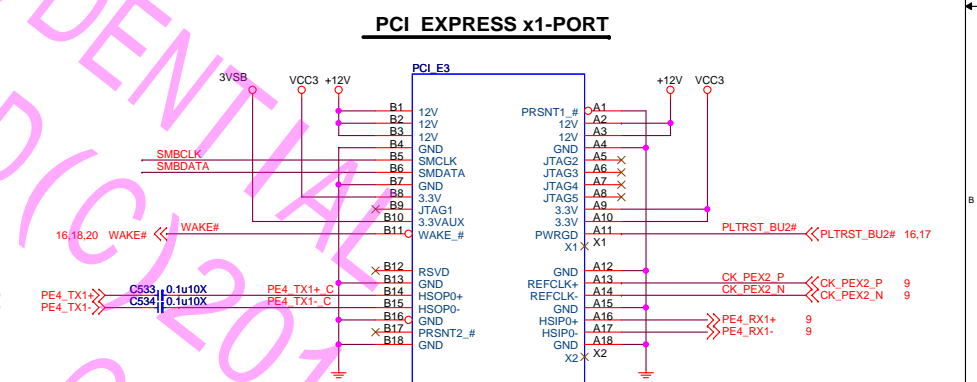
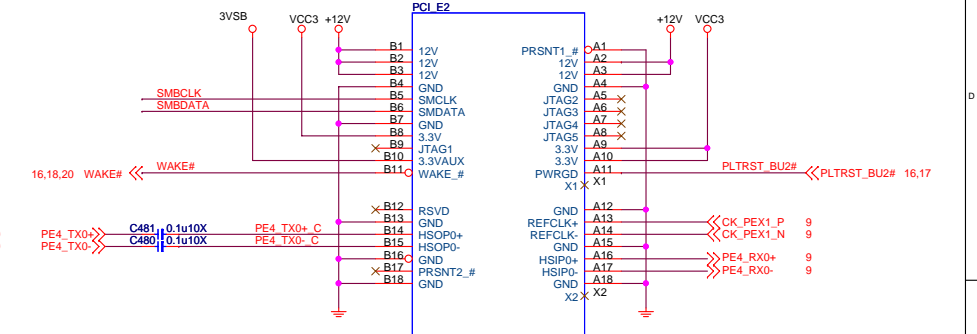
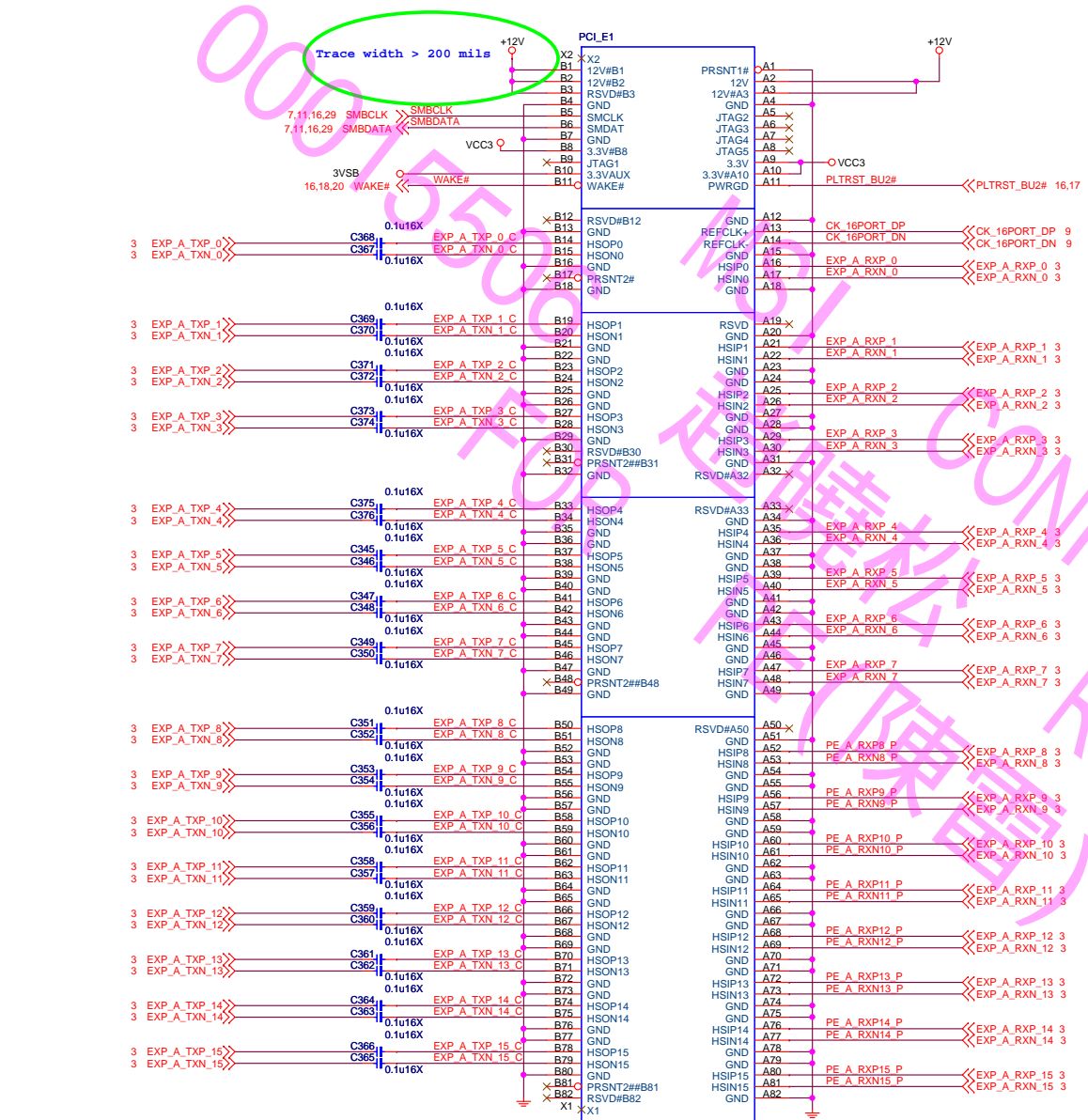
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

	MICRO-STAR INT'L CO.,LTD	
	MS-7680	
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PCI_Express X16 slot

PCI EXPRESS x1-PORT

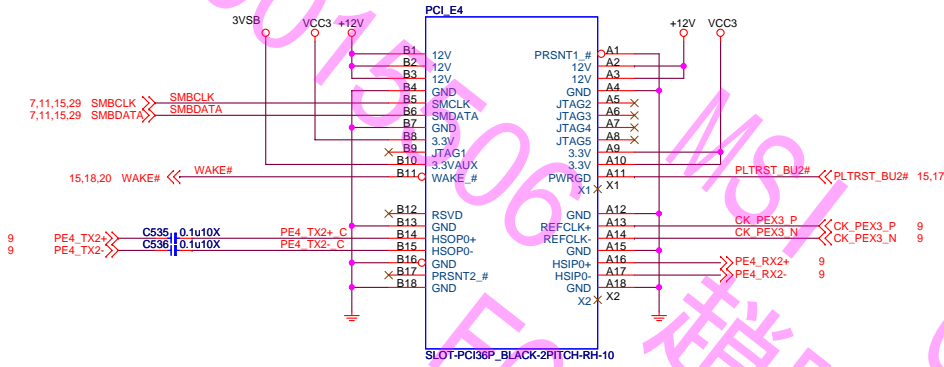


MICRO-STAR INT'L CO.,LTD

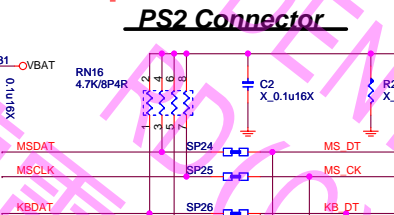
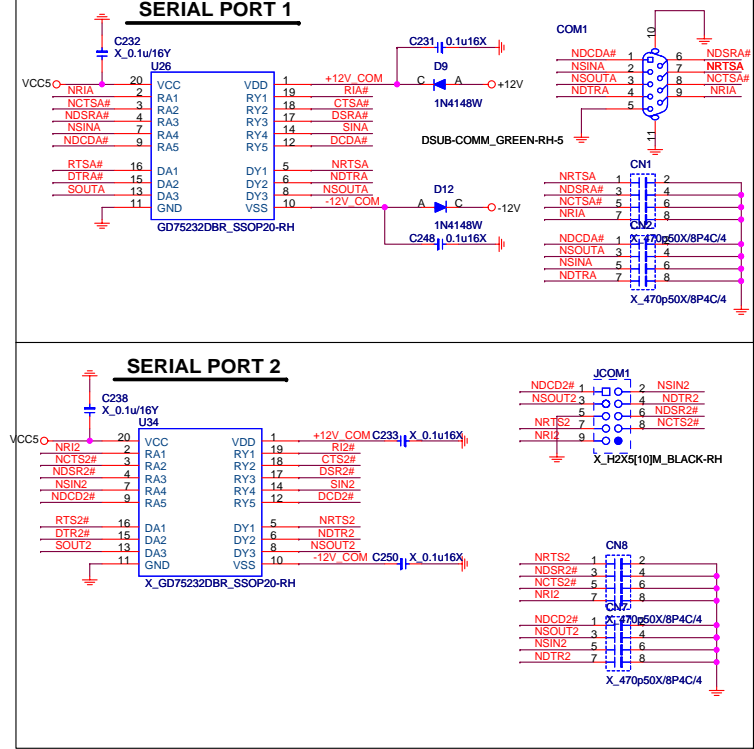
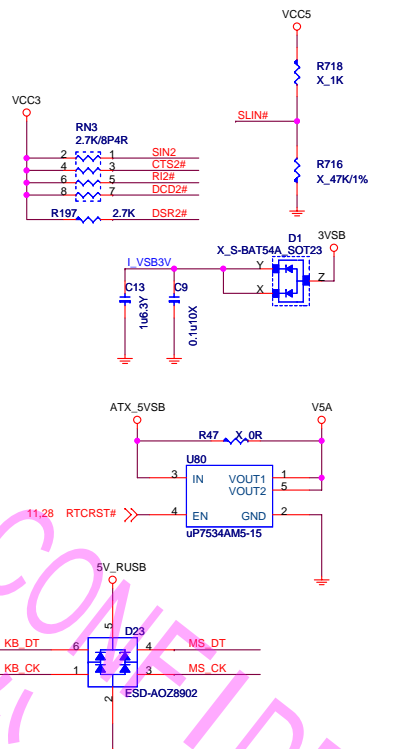
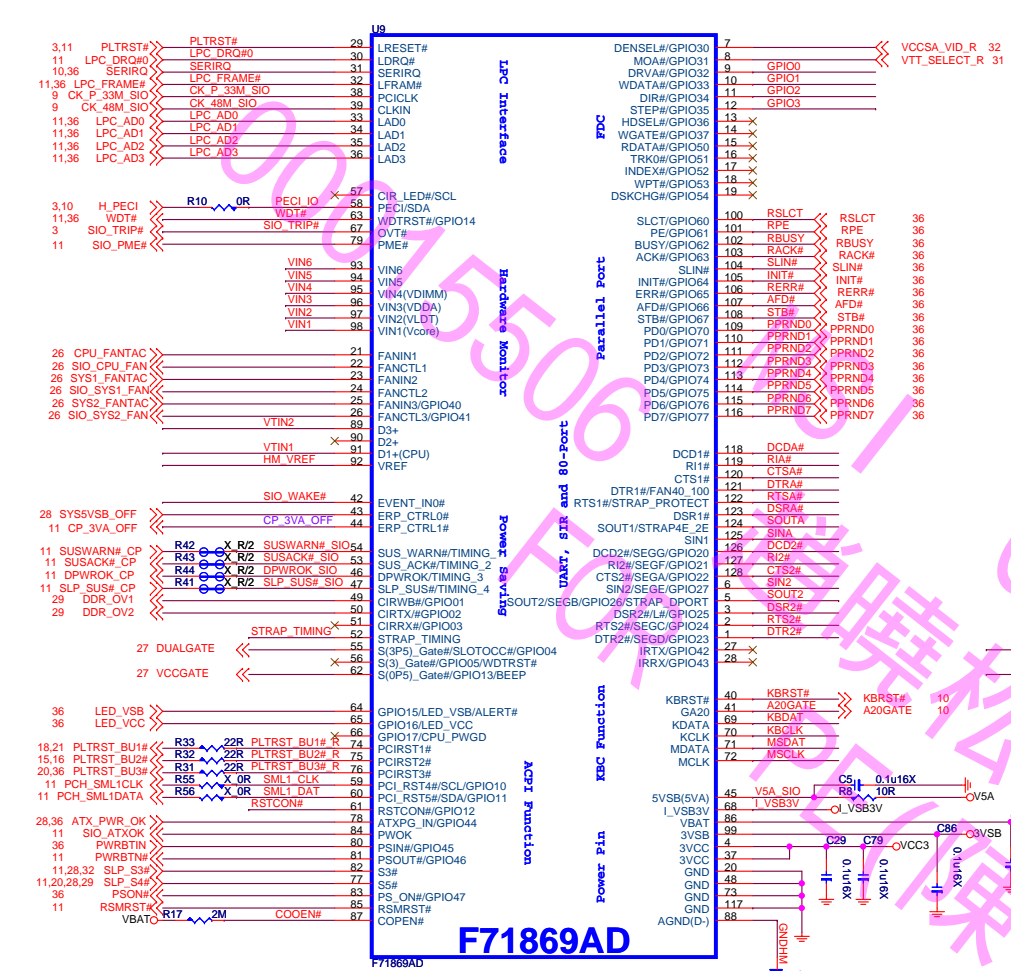
MS-7680

Size Custom	Document Description PCIe x16 x1/x1	Rev 3.2
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PCI EXPRESS x1-PORT

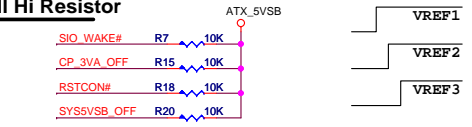


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 FOR 趙曉松 RD(C)2011102000 ONLY

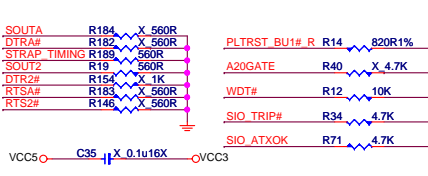


LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

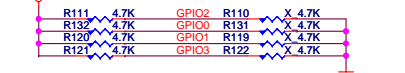
STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT	Enable 80 Port	Disable 80 Port
RTSA#		



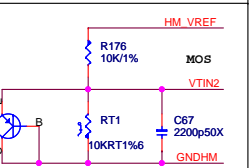
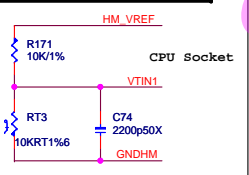
	GPIO0	GPIO1	GPIO2	GPIO3
H61M-P35 (STD)	1	1	1	1
H61M-P21 (OPT:E)	1	1	1	0
H61M-P23 (OPT:C)	1	1	0	0
H61M-P23 (OPT:I)	1	1	0	1



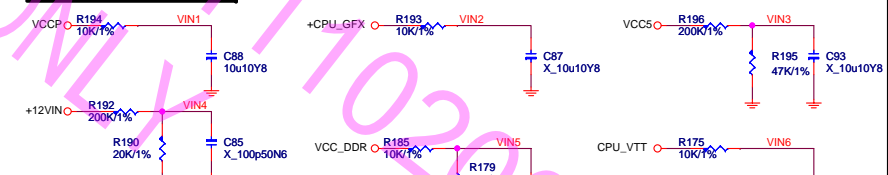
OPT BOM



HW Monitor - Thermal



HW Monitor - Voltage



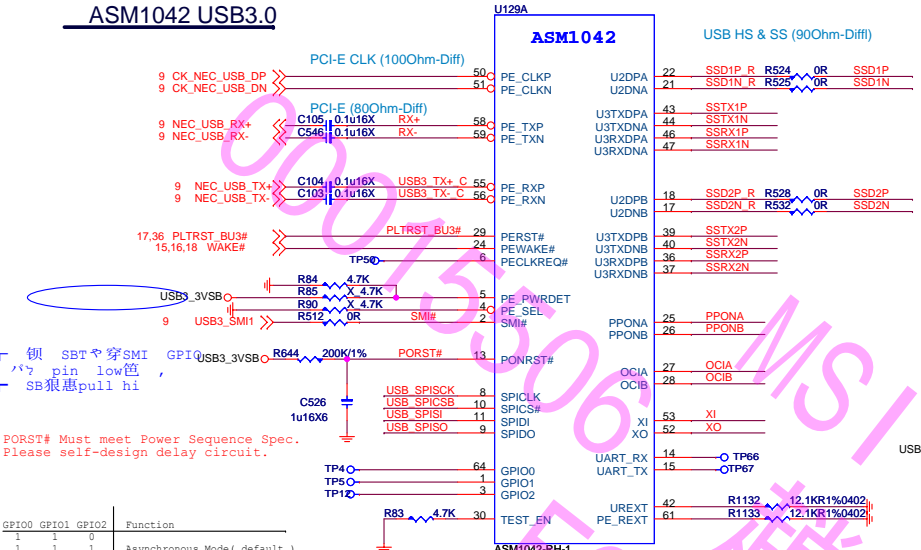
MICRO-STAR INT'L CO.,LTD

MS-7680

Size Custom Document Description SIO-Fintek F71869AD(EUP) Rev 3.2

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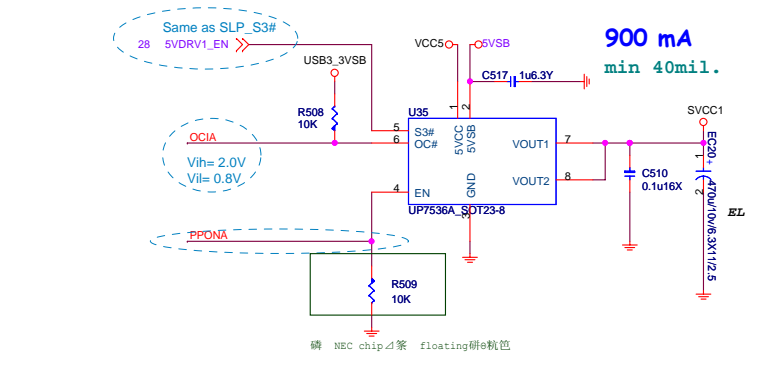
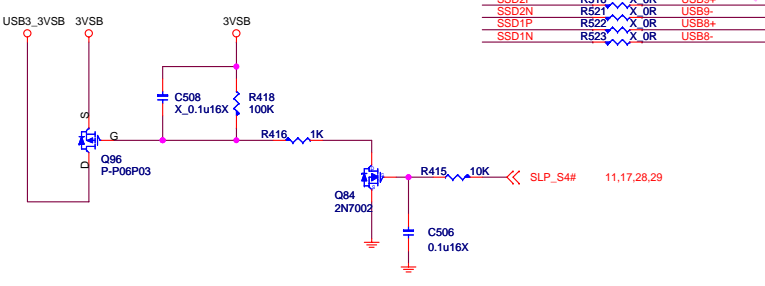
ASM1042 USB3.0



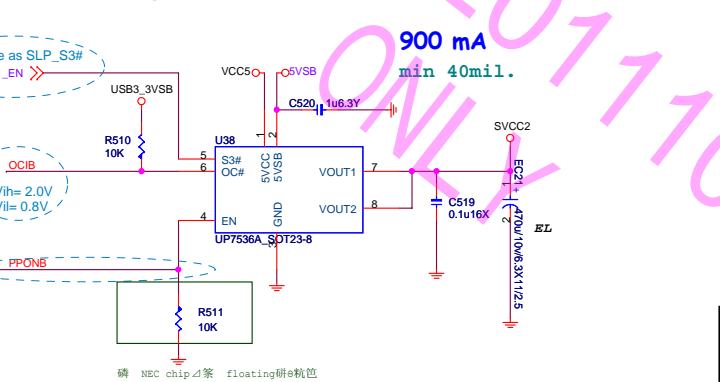
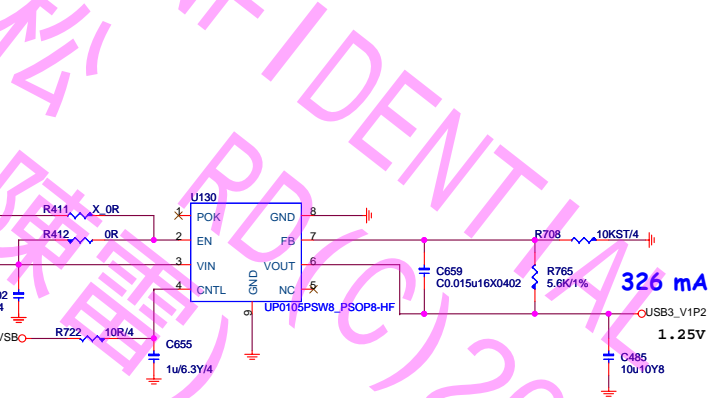
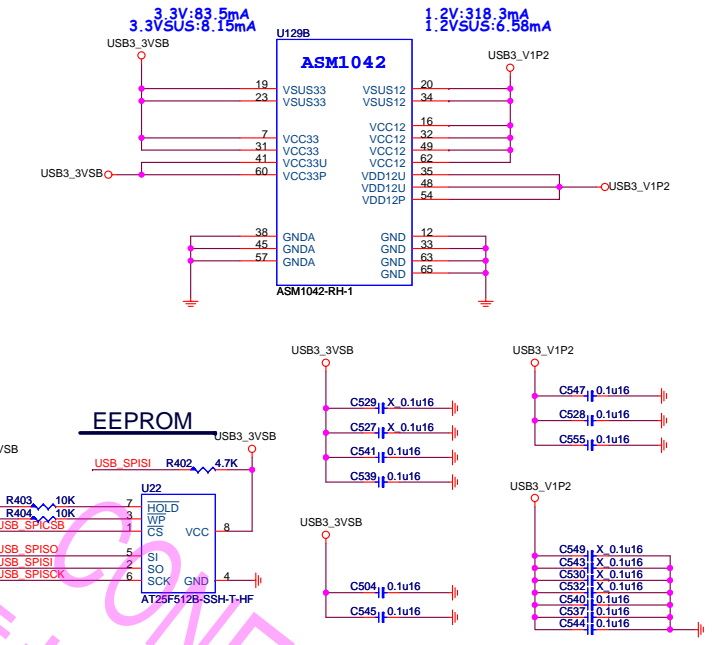
GPIO0	GPIO1	GPIO2	Function
1	1	0	Asynchronous Mode (default)
0	0	x	Debug/Test Mode

* GPIO0 GPIO1 GPIO2 internal Pull-high

3V_Dual Circuit



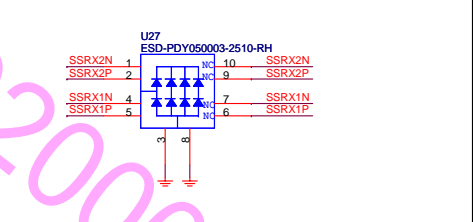
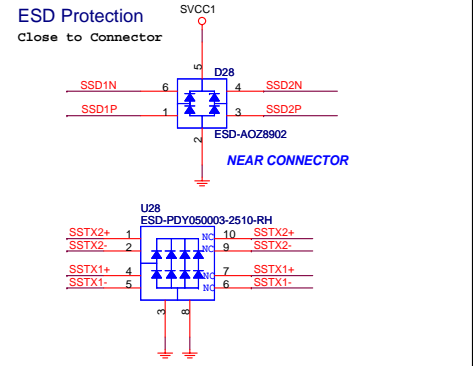
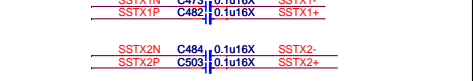
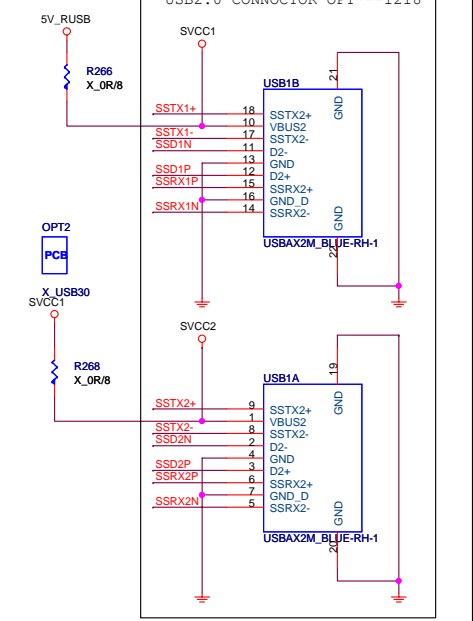
請 NEC chip 案 floating 解軌苞



請 NEC chip 案 floating 解軌苞

remove usb30 stuff

Rear USB3.0

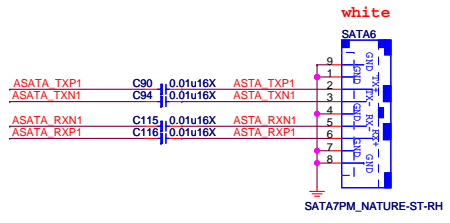
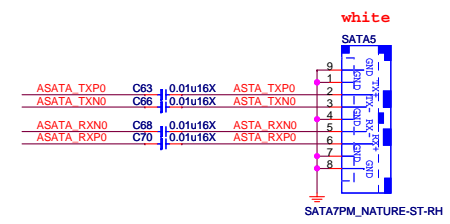
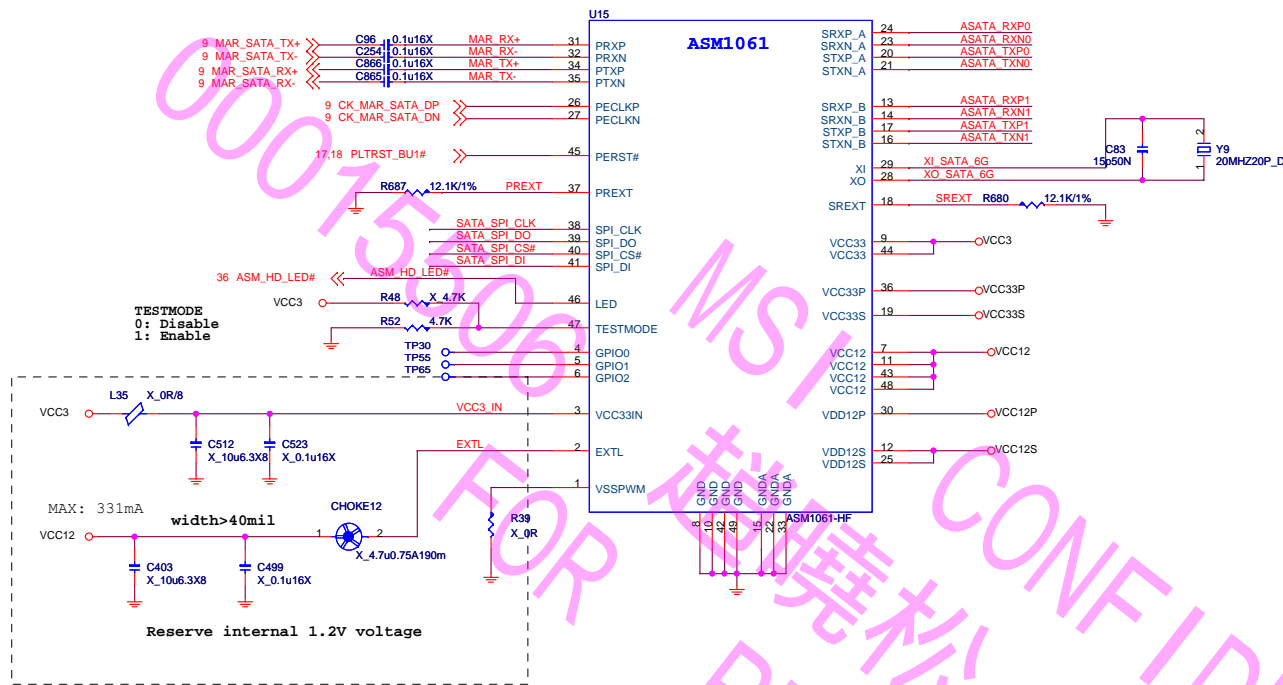


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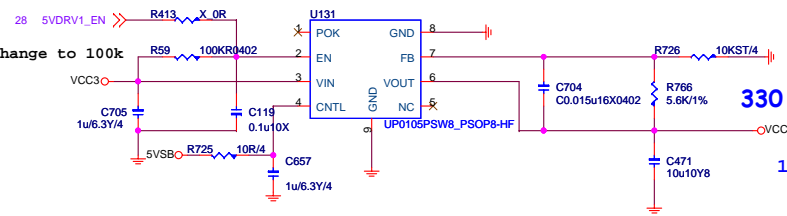
MS-7680

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ASM1061 SATA6G

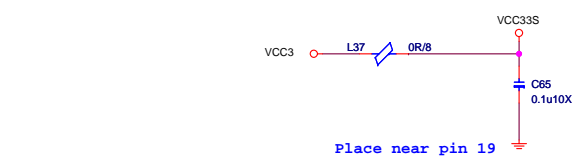
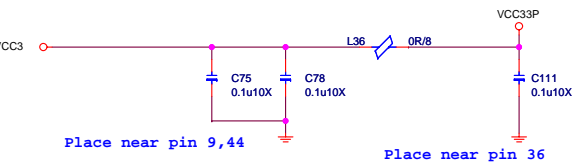
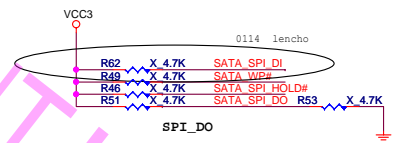


1.2V delay from 3.3V 90% > 0ms



ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



MICRO-STAR INT'L CO.,LTD

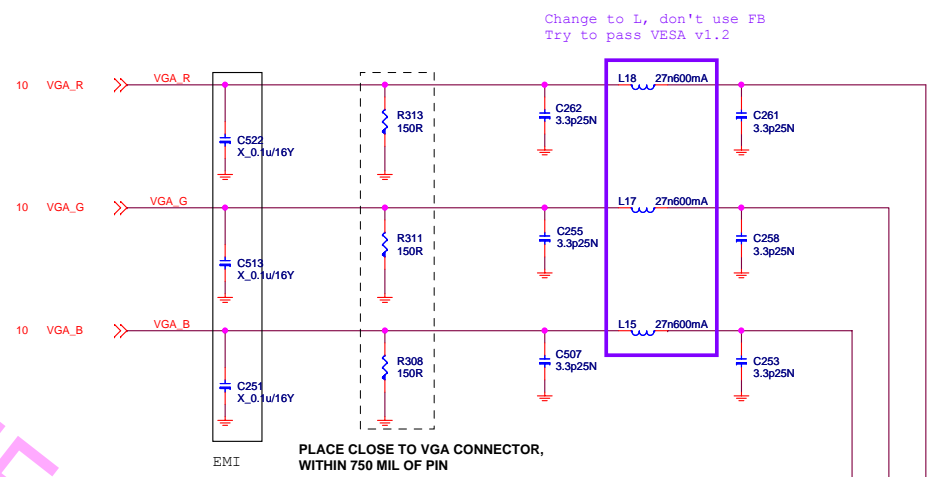
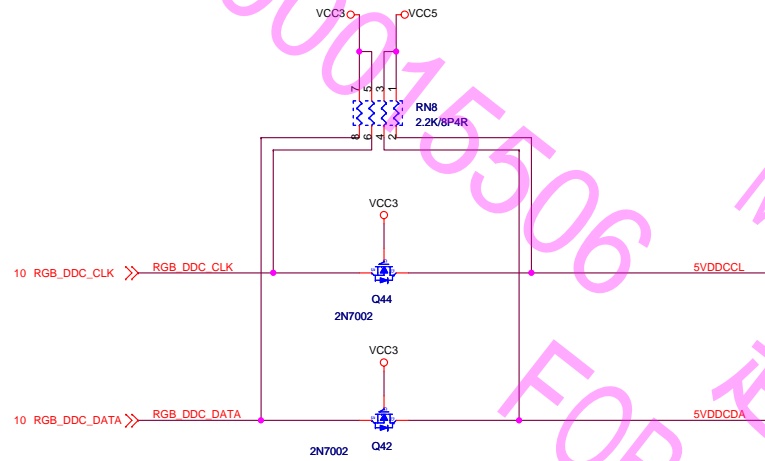
MS-7680

Size	Document Description	Rev
Custom	ASM1061 SATA6G	3.2
Date: Monday, June 13, 2011		Sheet 21 of 39

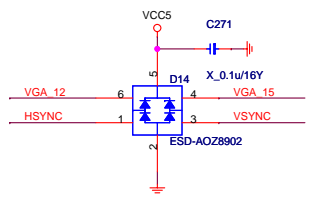
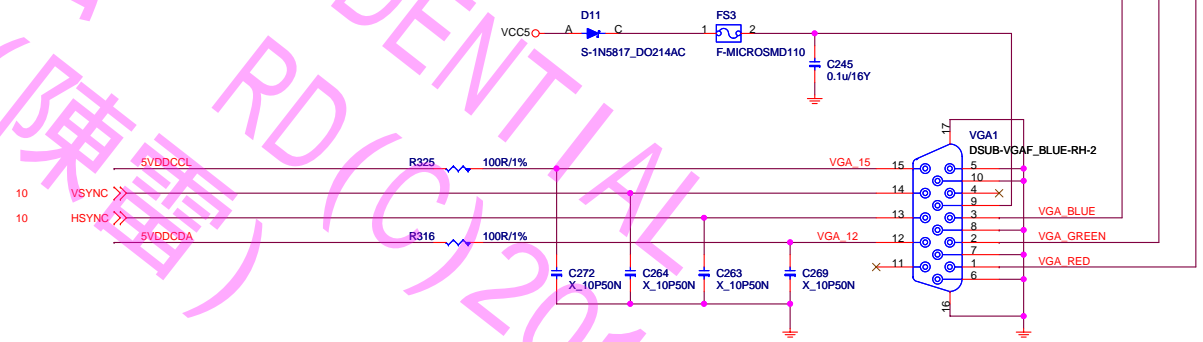
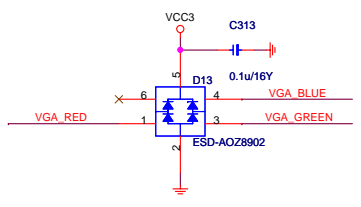
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Levelshift



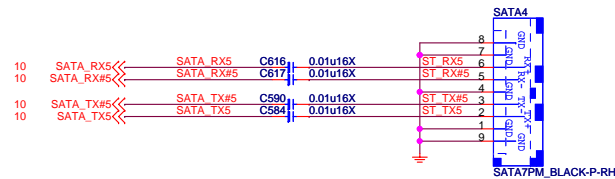
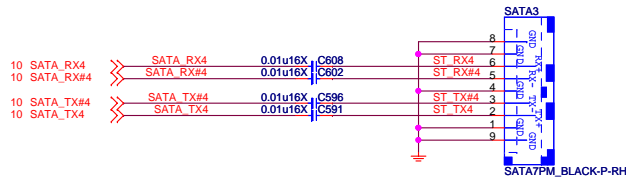
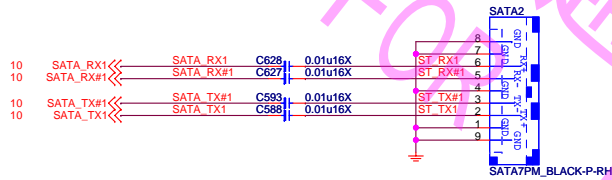
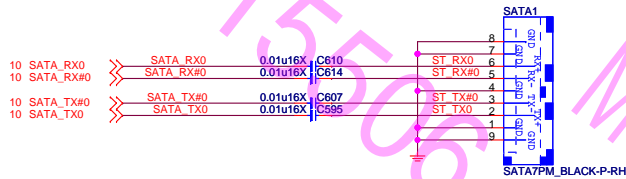
PLACE CLOSE TO VGA CONNECTOR, WITHIN 750 MIL OF PIN



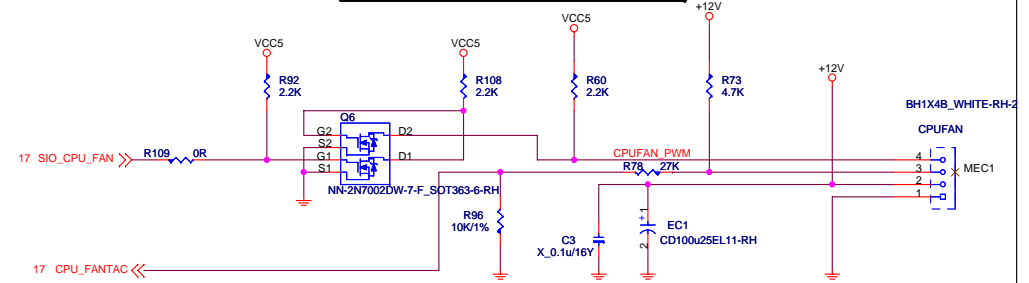
MSI		
MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size Custom	Document Description VGA	Rev 3.2
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SATA 6G PORT 0,1

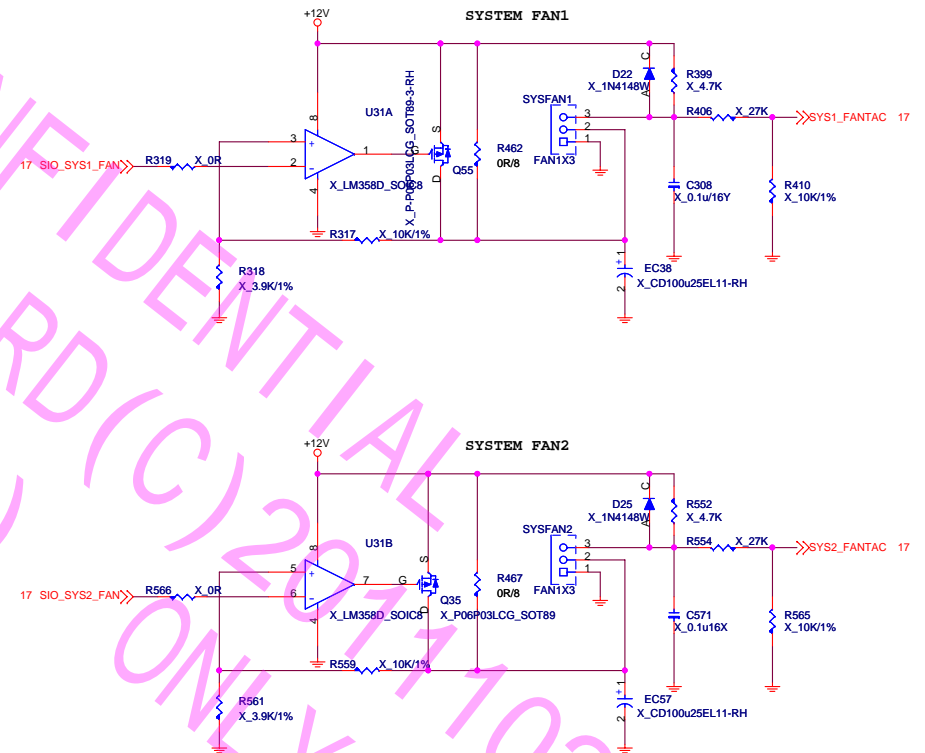
H61 PORT 0/1 3G
H67 PORT 0/1 6G



CPU FAN-COUNTROL CIRCUIT



SYSTEM FAN-COUNTROL CIRCUIT

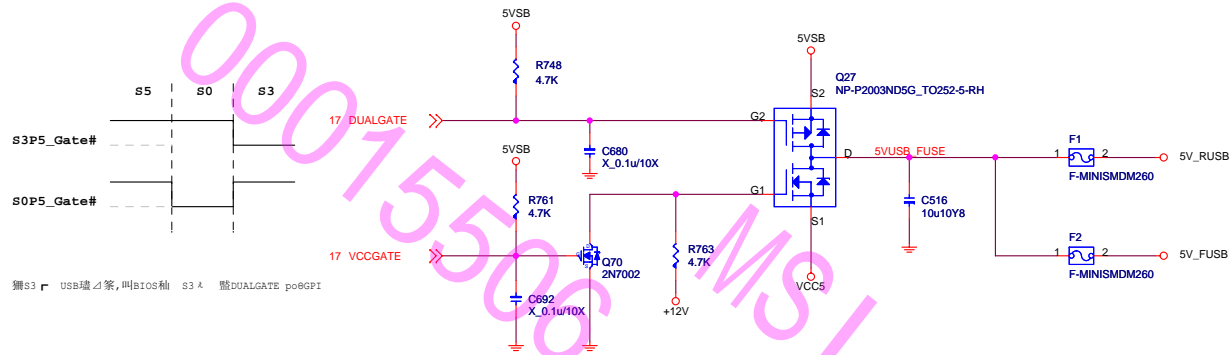


MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description SATA / FAN Control	Rev 3.2
Date: Tuesday, June 28, 2011	Sheet 26 of 39	

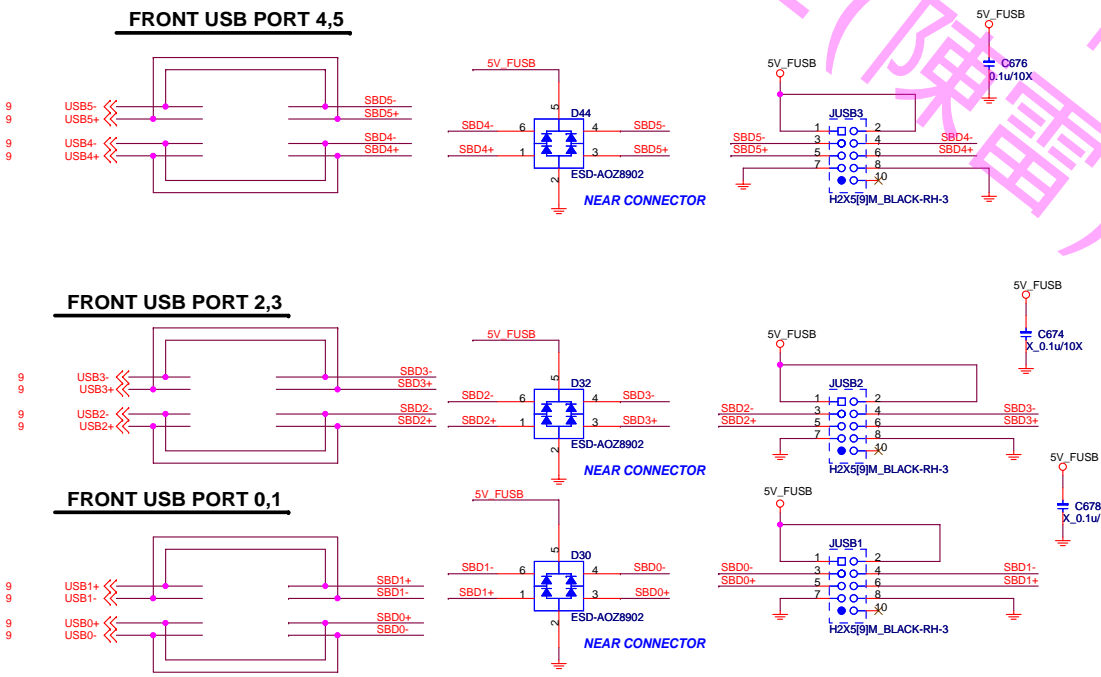
5V_RUSB Switch



圖S3 USB端之接,叫BIOS軸 S3之 雙DUALGATE poeGPI

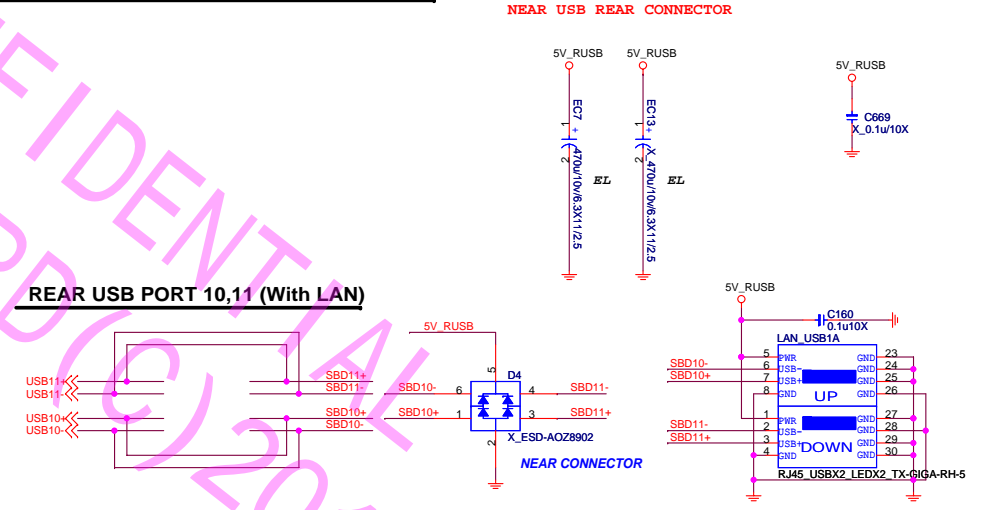
Front USB Connector

For H61 6,7,12,13 Port should be remove



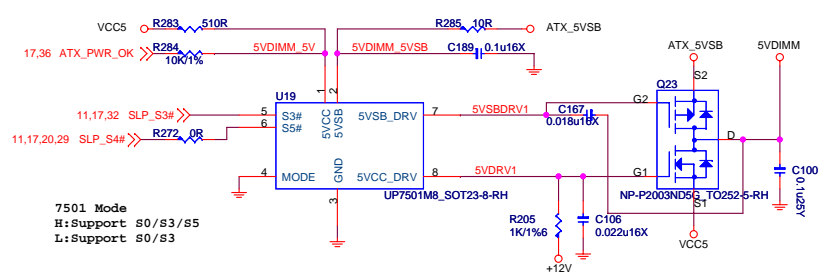
Rear USB Connector

REAR USB PORT 10,11 (With LAN)

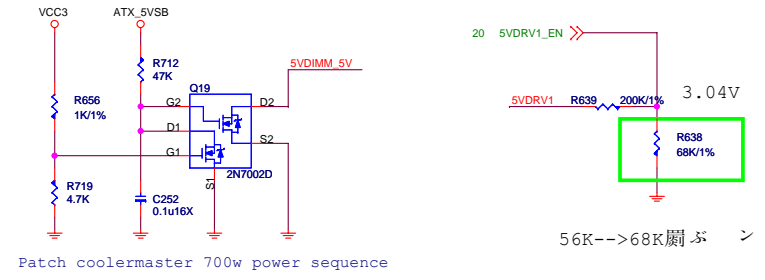


	MICRO-STAR INT'L CO.,LTD	
	MS-7680	
Size Custom	Document Description USB Connector	Rev 3.2
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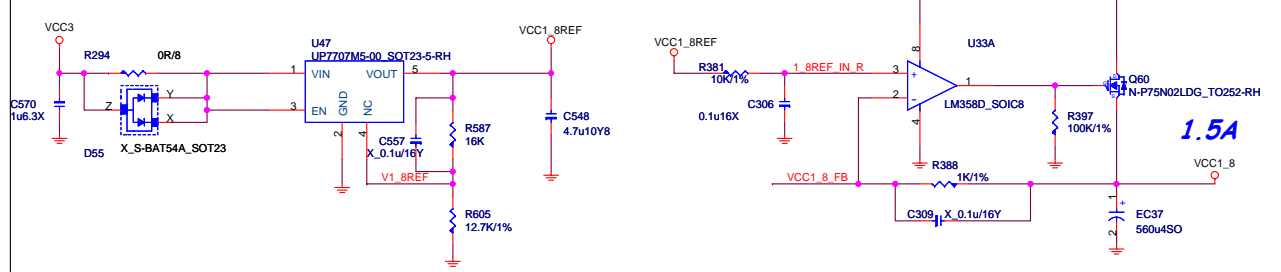
5VDIMM FOR DDR



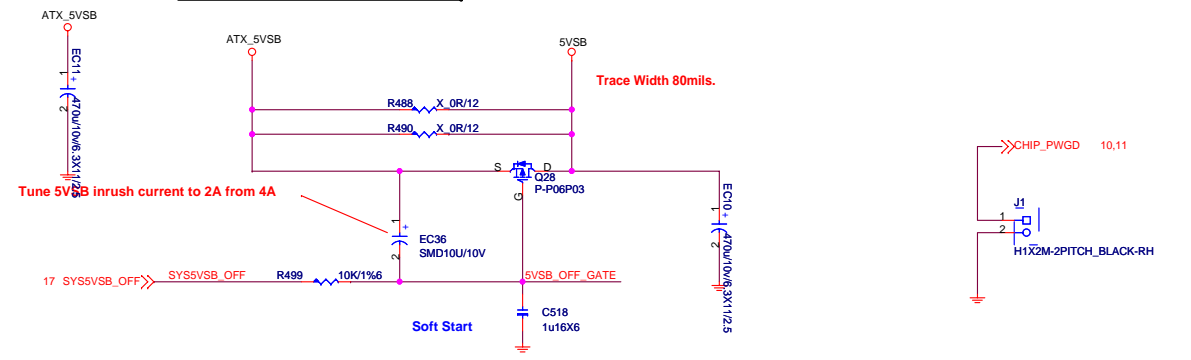
USB MODE



VCC1_8REF

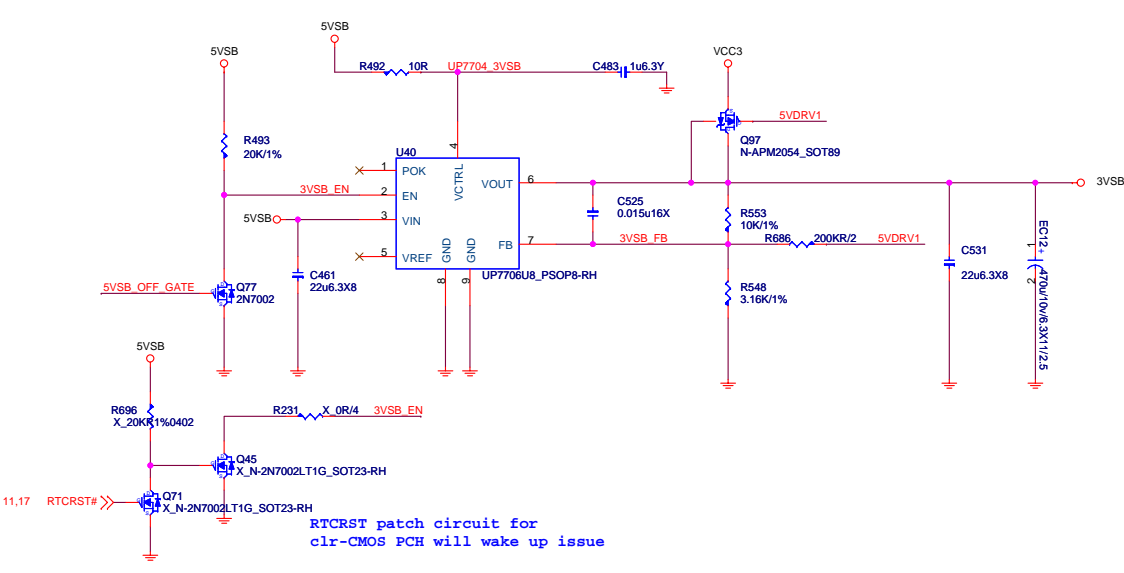


5VSB Power Switch



3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.

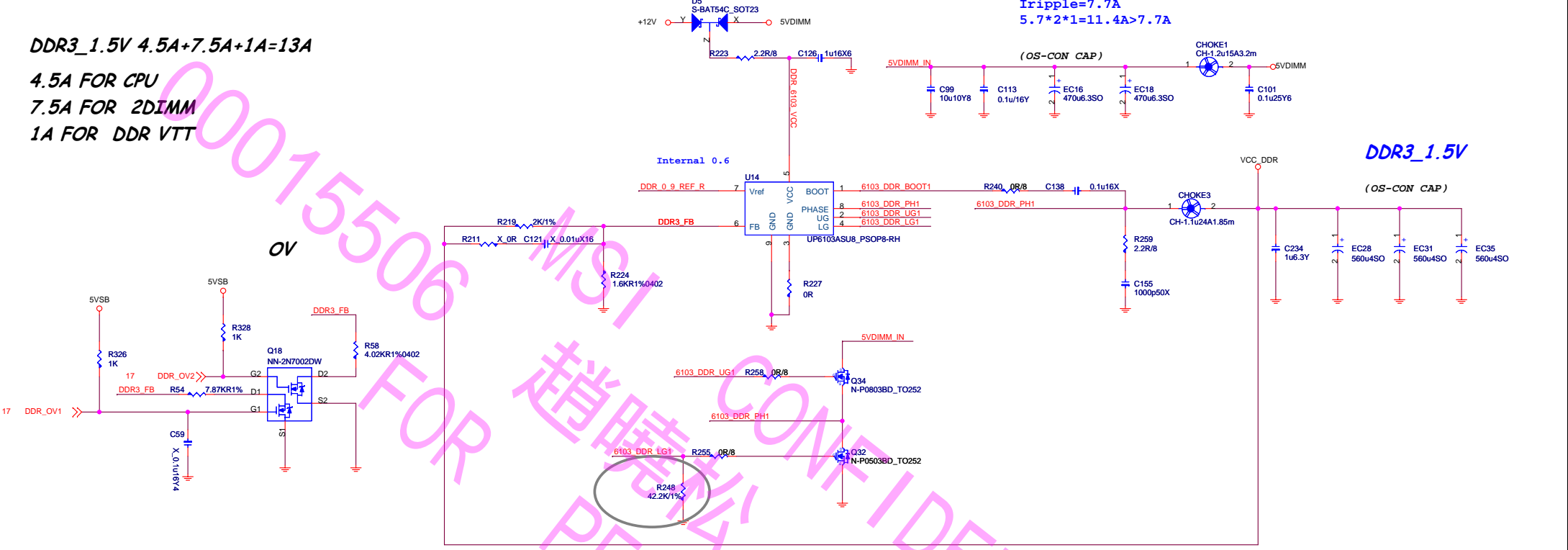


RTC RST# patch circuit for
clr-CMOS PCH will wake up issue

			MICRO-STAR INT'L CO.,LTD	
			MS-7680	
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DDR3_1.5V 4.5A+7.5A+1A=13A

4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT

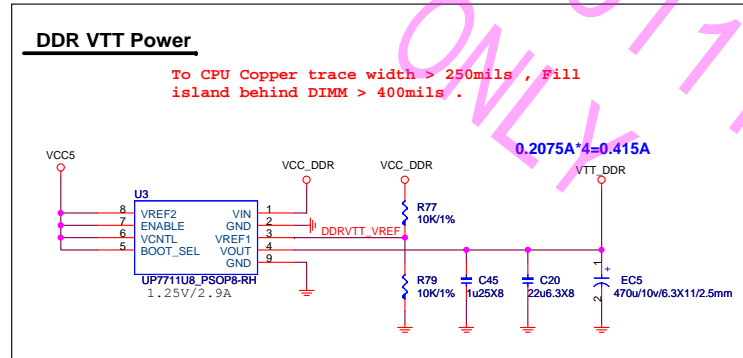
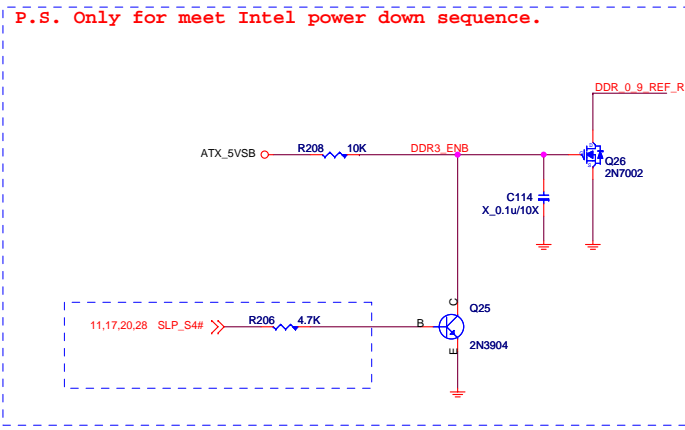


OV

UPI VOLTAGE CONSOLE

0x20:RH=1.0K,RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils.

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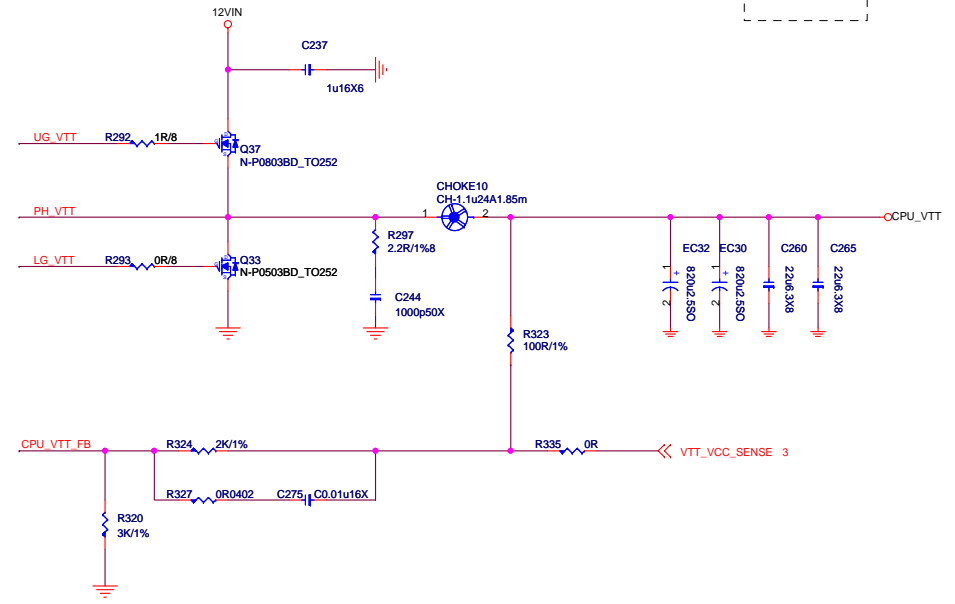
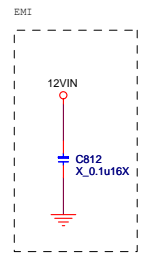
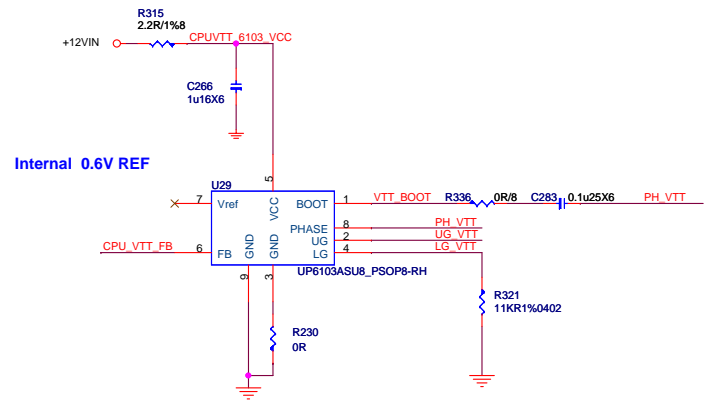
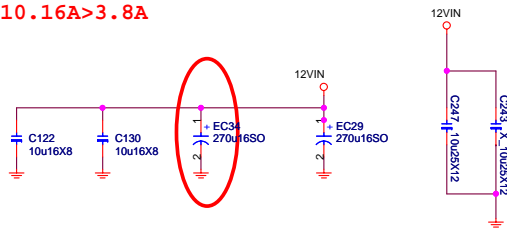
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Size Custom	Document Description DDR Power - uP6103 1-Phase	Rev 3.2
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CPU_VTT:1.05/1.00

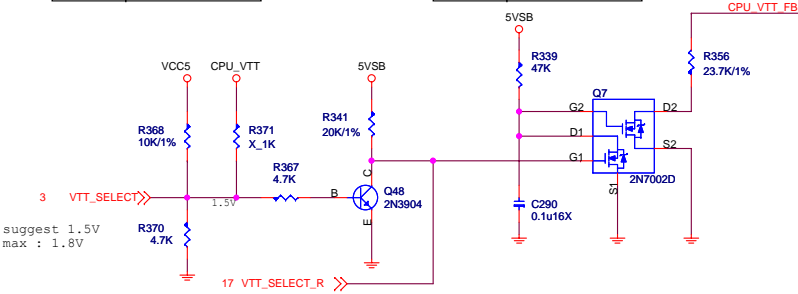
CPU VTT 8.5A + SA Core = 8.8A = 17.3A

$I_{ripple} = 1.92(vtt) + 1.88(sa)$
 $5.08 * 2 = 10.16A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

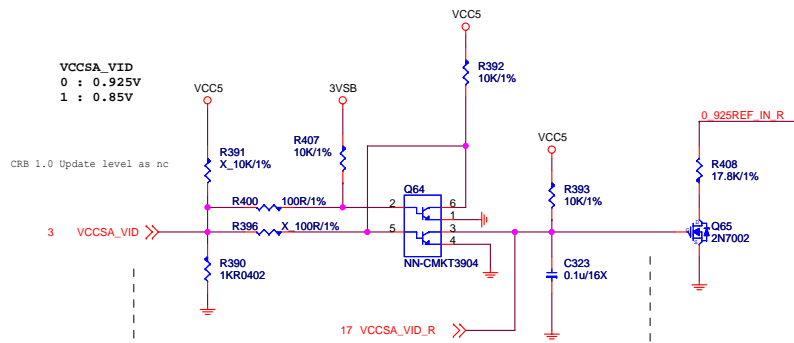
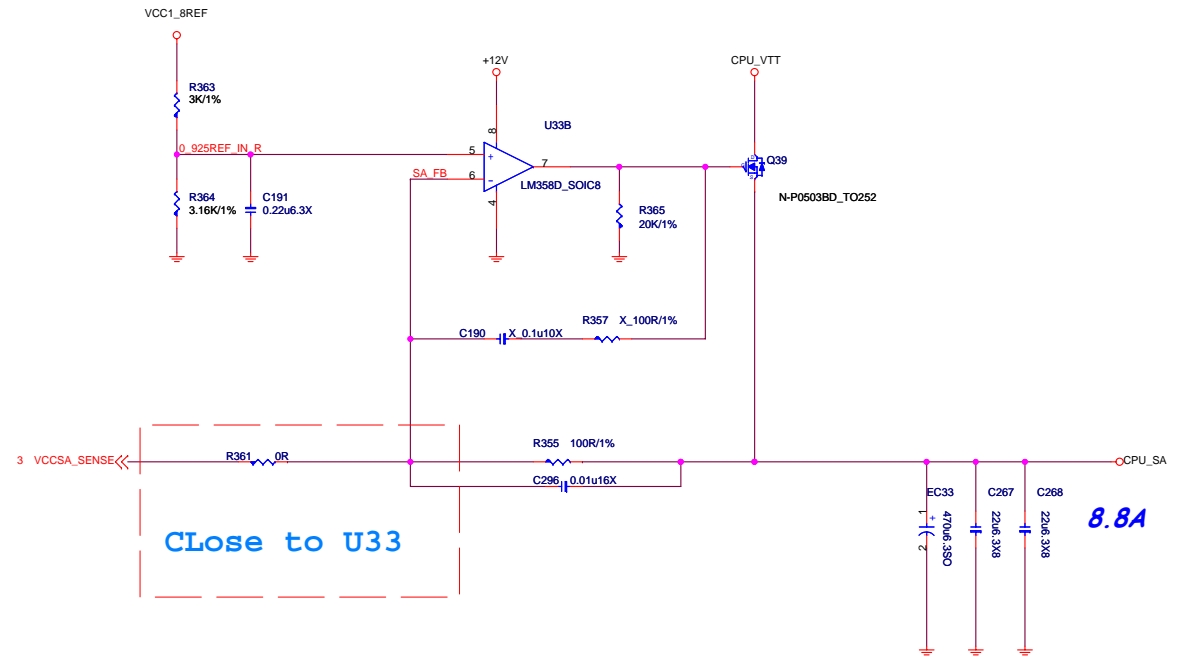
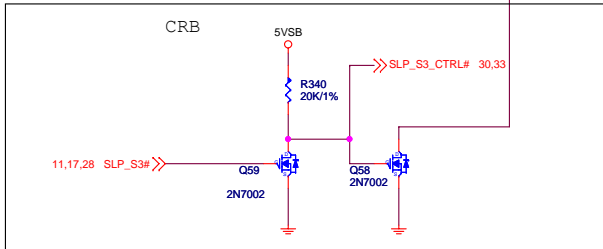
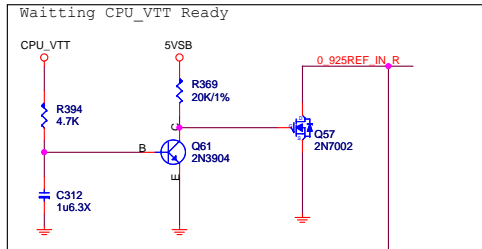
VTT_SELECT Table	
Low	1.05V
High	1.0V



MICRO-STAR INT'L CO.,LTD		
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Size	Document Description	Rev
Custom	CPU_VTT - uP6103- 1-Phase	3.2
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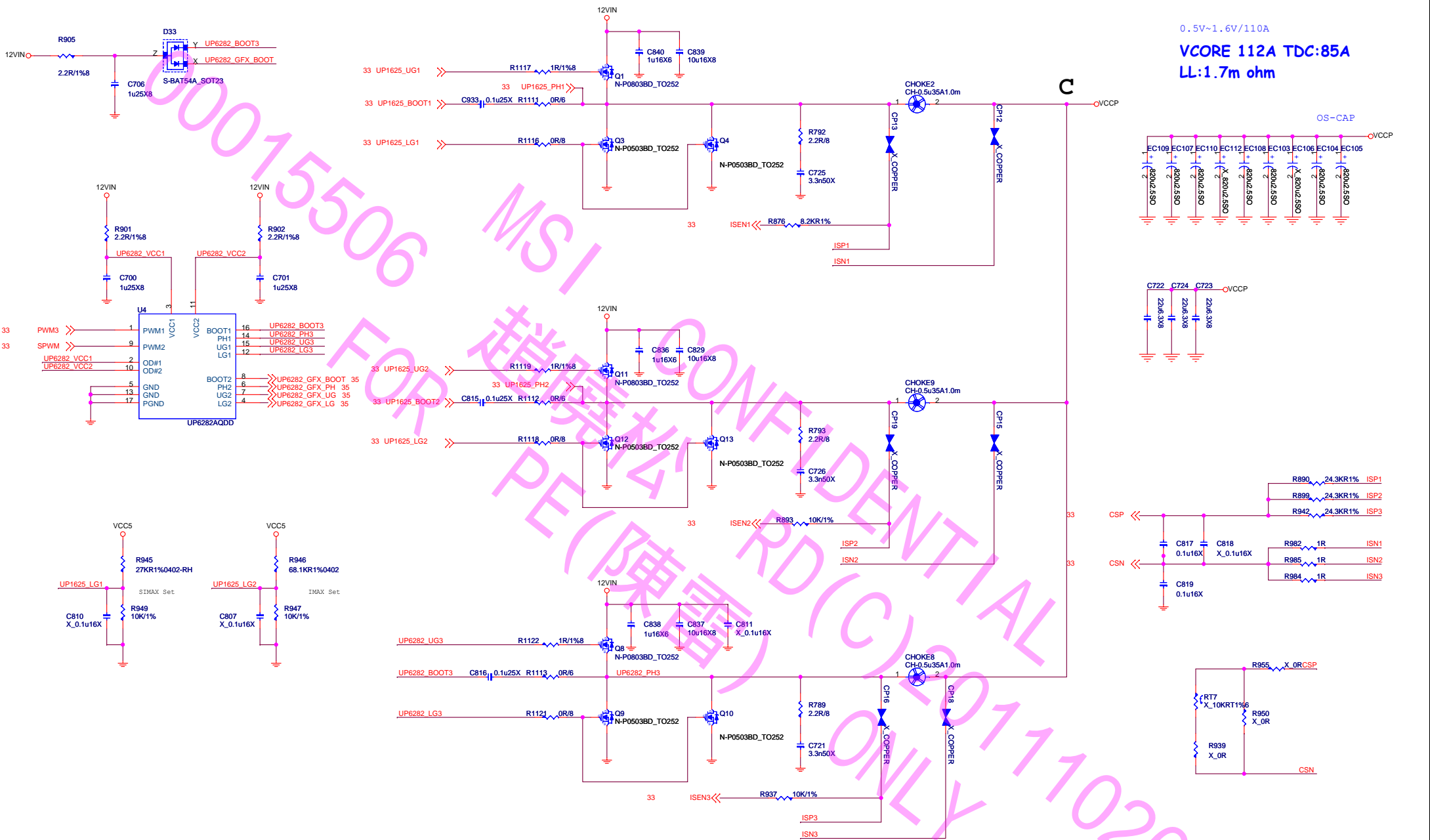
CPU_SA:0.925/0.85

SA Core = 8.8A

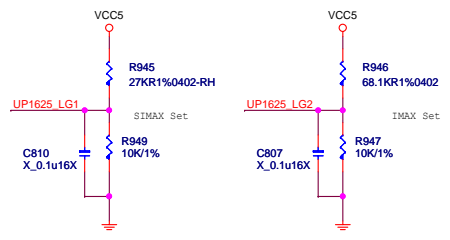
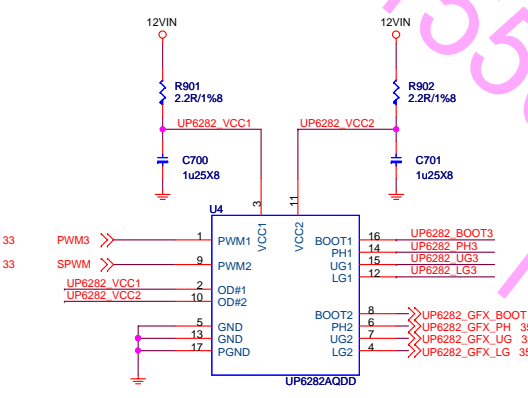
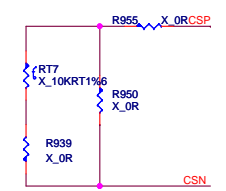
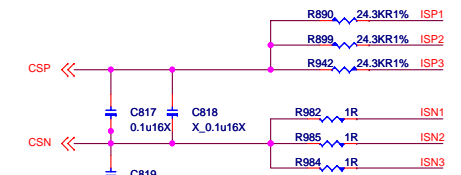
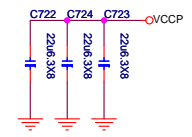
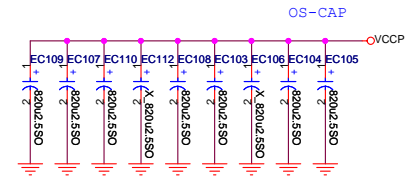


VCCSA_VID	
Low	0.925V
High	0.85V

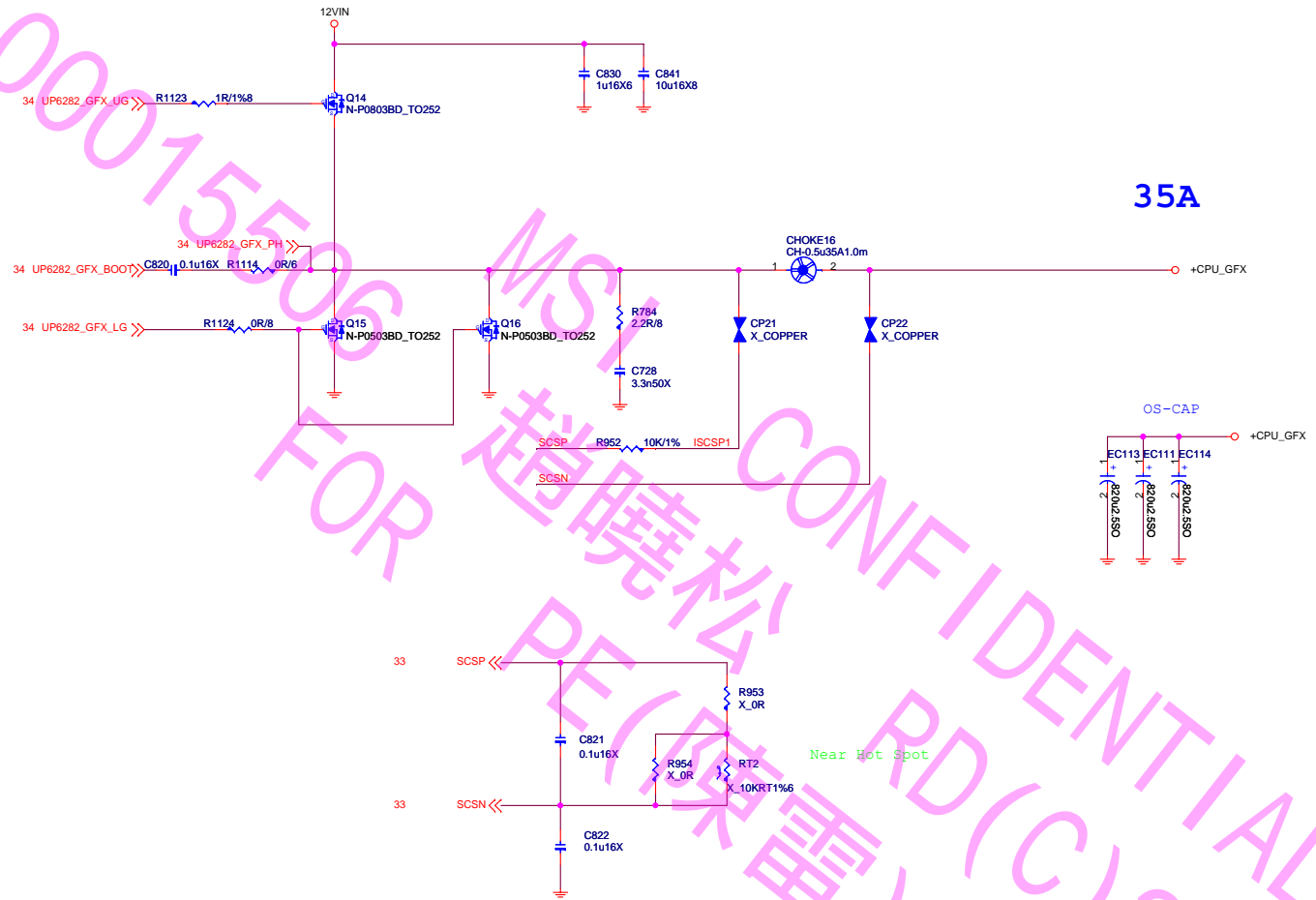
VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V



0.5V~1.6V/110A
VCORE 112A TDC:85A
LL:1.7m ohm



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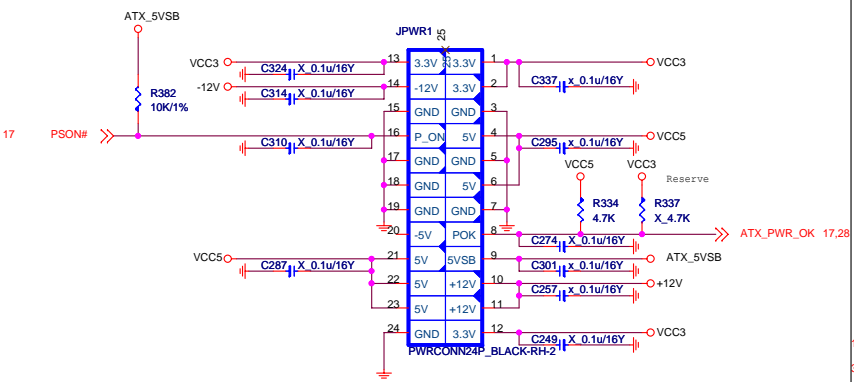
35A

Near Hot Spot

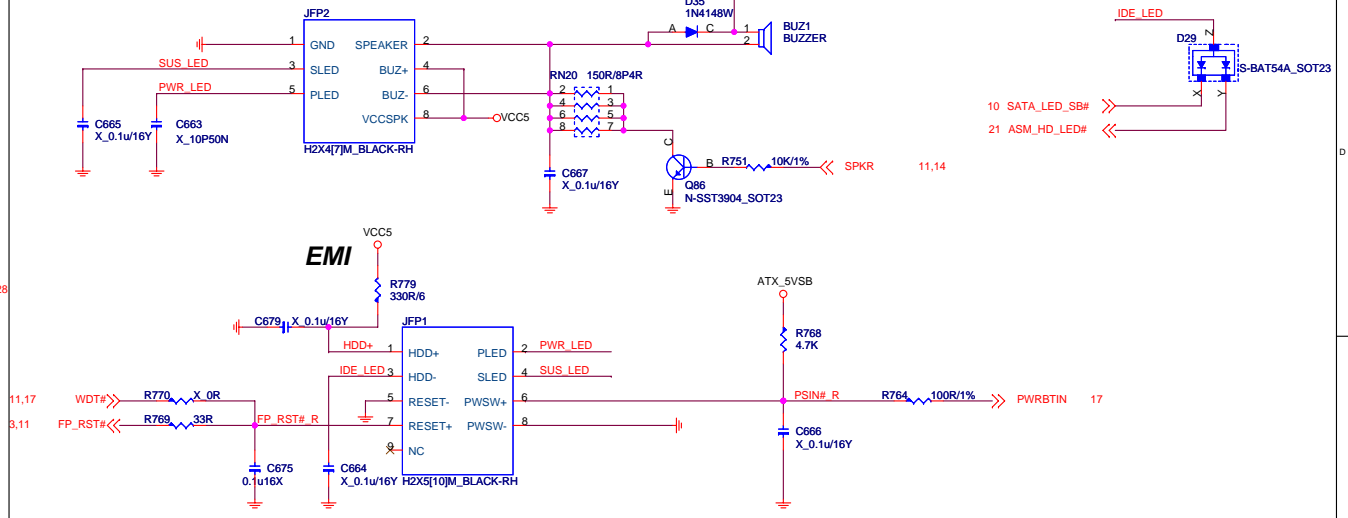


MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size Custom	Document Description UP6234 1-Phase GPU	Rev 3.2
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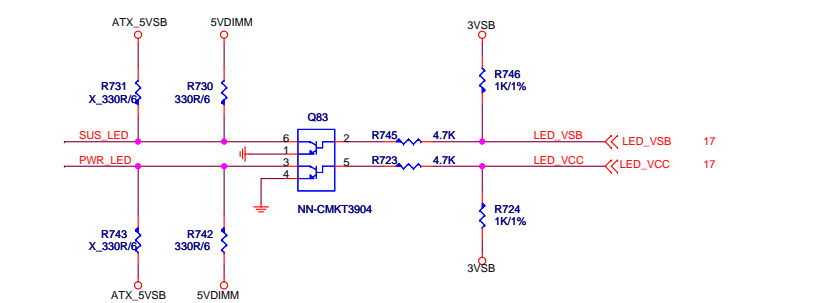
ATX POWER CONNECTOR



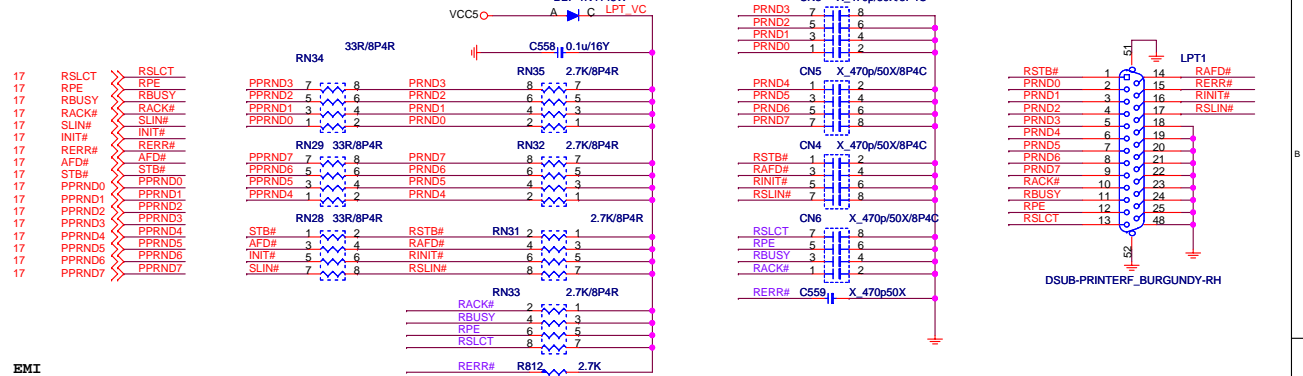
FRONT PANEL



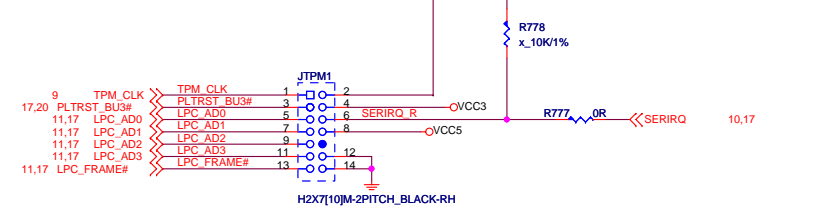
LED (for Fintek 71889)



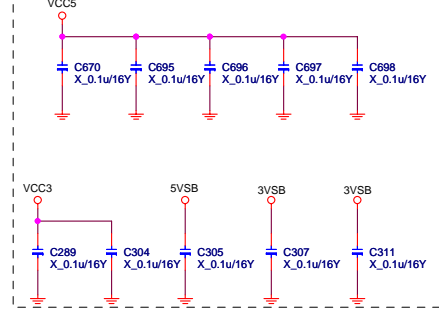
PARALLAL PORT



TPM/JLPC



EMI



MICRO-STAR INT'L CO.,LTD

MS-7680

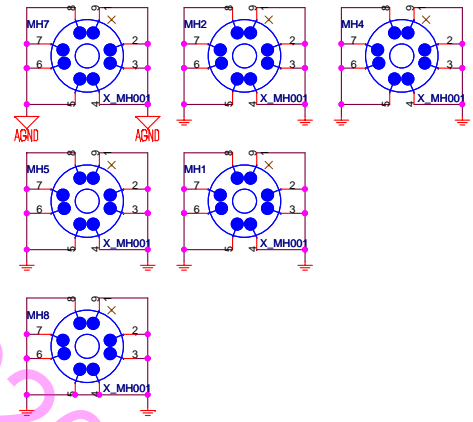
Size	Document Description	Rev
Custom	ATX PWR-Connector & Front Panel & EMI	3.2
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00015506 MSI CONFIDENTIAL ONLY 趙曉松 RD (C) 2011/10/20 PE (陳雷)

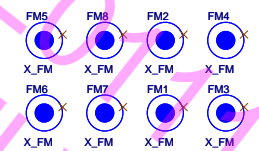
PCH XDP PWRGD/RESET



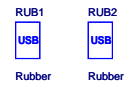
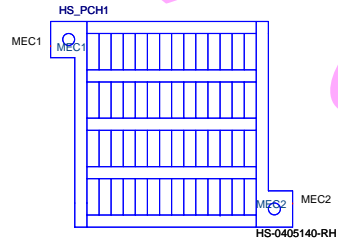
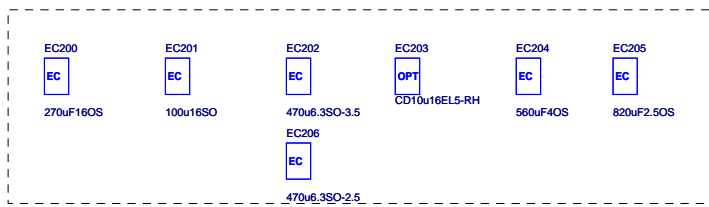
Mounting Holes



Optical Fiducial Marks-120



EL/OS OPT.



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	MS-7680		
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