





POWER	
Discharge	PG 38
RUN POWER SW 3VSUS, 5VSUS, 3V_S5, 5V_S5 +3V, +5V	PG 38
AC/BATT CONNECTOR	PG 42
BATT CHARGER	PG 39
REGULATOR (DDR3) 1.5VSUS, 0.75VSMDDR_VTERM, 1.5V 1.5V_GPU, 1.5V_CPU	PG 40
REGULATOR +1.05V_VTT, +1.8V	PG 41
DC/DC 3VPCU, 5VPCU, +15V	PG 42
CPU Core	PG 43
GFX_CORE Discrete 1.8V_GPU, +1.05V_GPU, +3V_GPU	PG 44
VGA Core UMA	PG 45

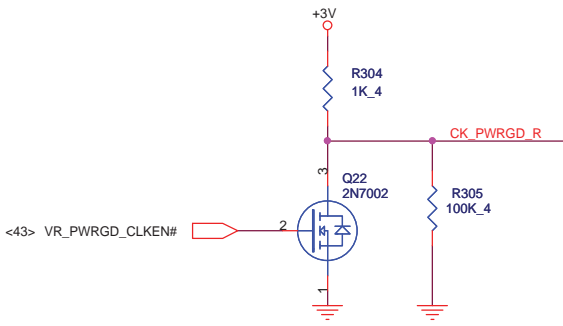
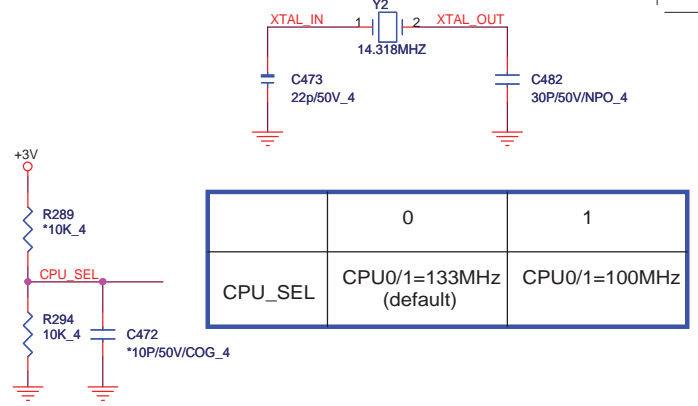
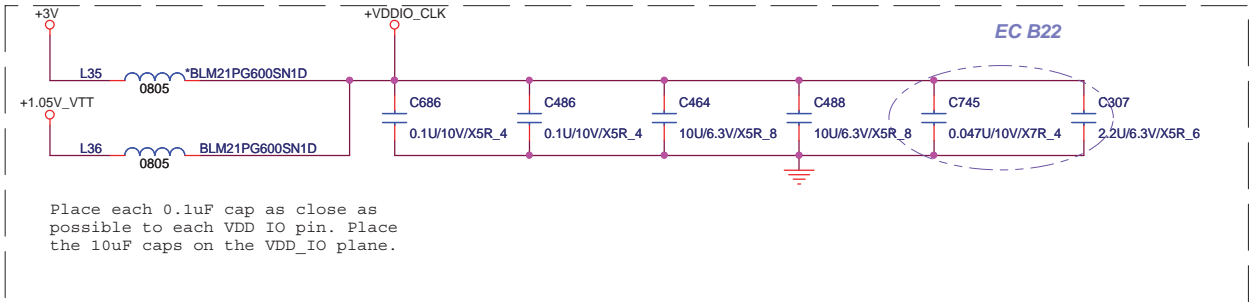
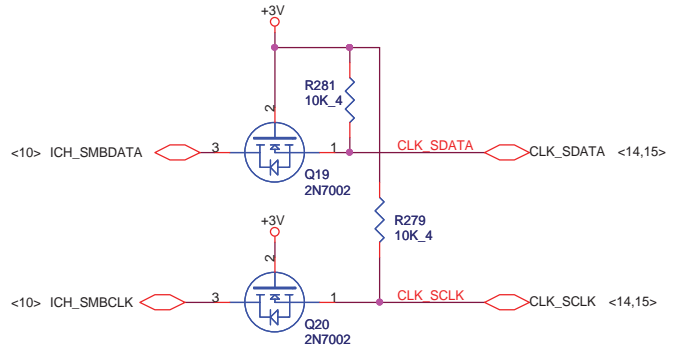
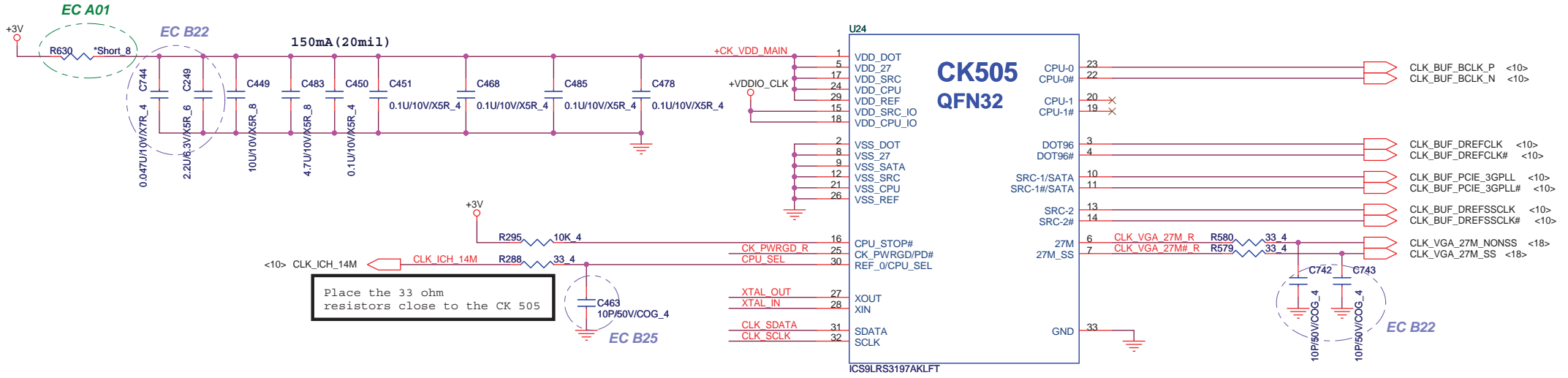
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25	CRT Conn.
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45	GFX_VCC (MAX17028)
46	Power Block Dianram
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Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0-S5
+RTC_CELL	+3V~+3.3V	RTC		S0-S5
+3VPCU	+3.3V	8051 POWER	3V5V_EN	S0-S5
+5VPCU	+5V	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
+15V	+15V	LARGE POWER	3V5V_EN	S0-S5
VCC3_LAN	+3.3V	LAN POWER	LAN_ON	
+5VSUS	+5V	SLP_S4# CTRLD POWER	SUSON	
+3VSUS	+3.3V	SLP_S4# CTRLD POWER	SUSON	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAIN_ON	
+5V	+5V	SLP_S3# CTRLD POWER	MAIN_ON	
+3V	+3.3V	SLP_S3# CTRLD POWER	MAIN_ON	
+1.8V	+1.8V	CPU,PCH POWER	MAIN_ON	
+1.5V	+1.5V	PCH POWER	MAIN_ON	
+1.05V_VTT	+1.05V~+1.1V	CPU POWER	MAIN_ON	
+1.05V_PCH	+1.05V	PCH POWER	1.05V_RUN_ON	
VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	ENVDD	
BAT-V	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V	PCH SUS POWER	S5_ON	
+3V_S5	+3.3V	Sys Management,PCH Resume Well	S5_ON	

GND PLANE	PAGE	DESCRIPTION
 LANGND	26	
 IT8512_AGND	36	
 ADOGND	27	
 GND	ALL	



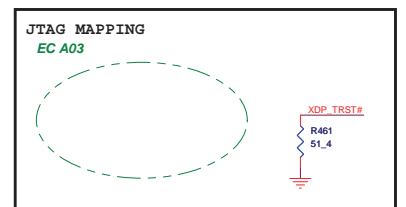
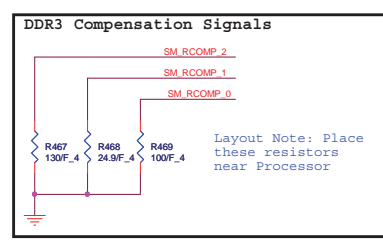
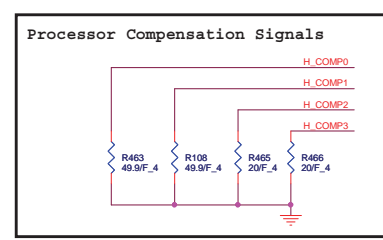
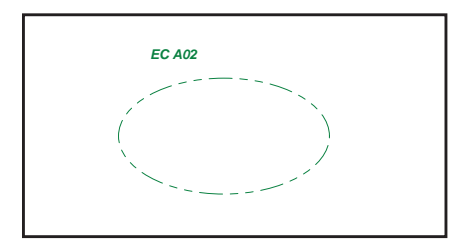
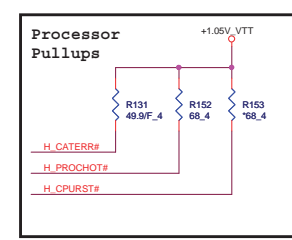
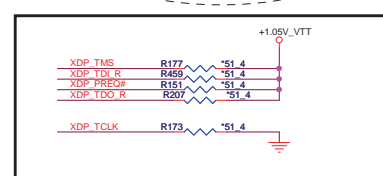
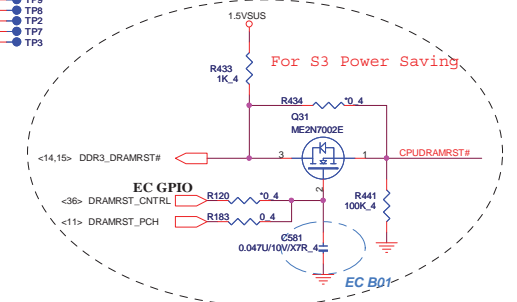
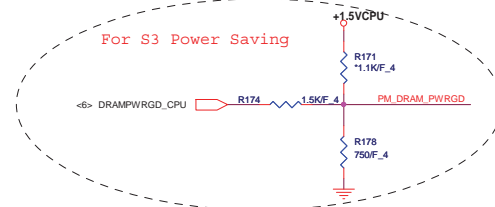
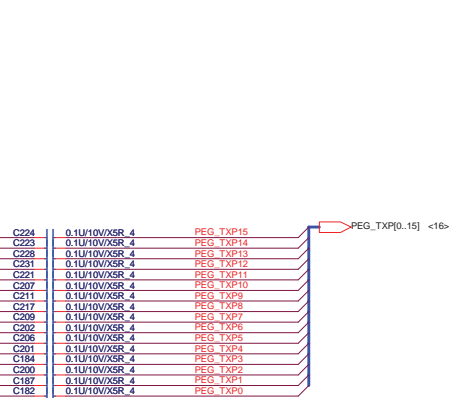
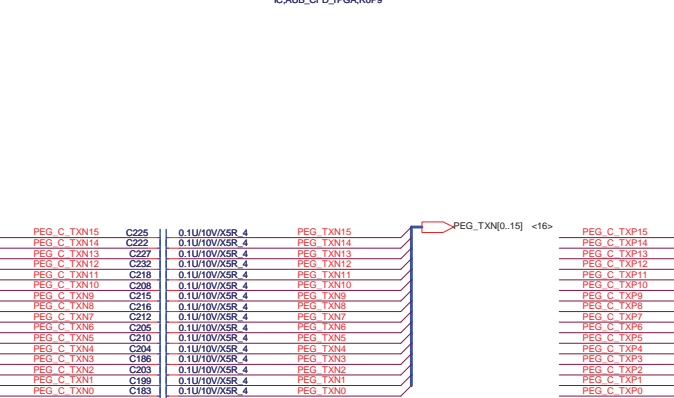
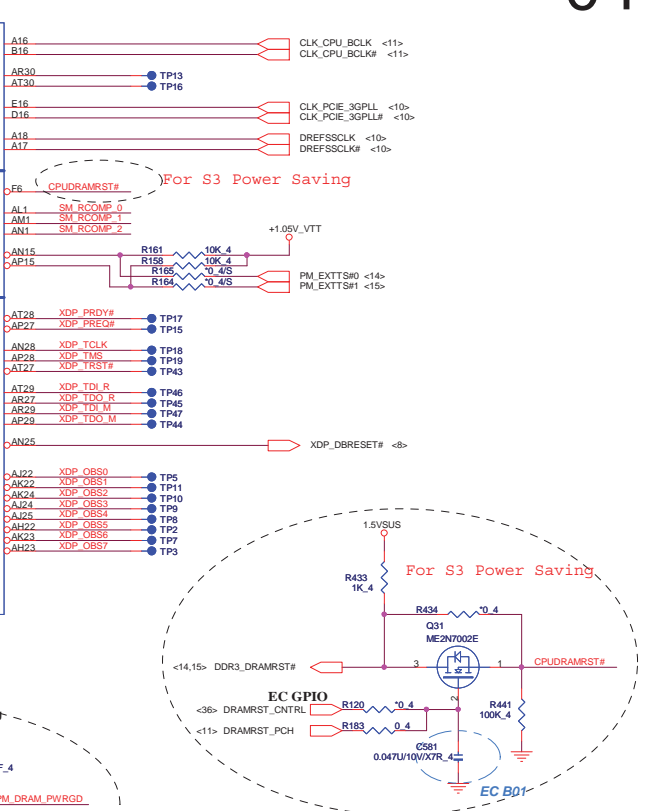
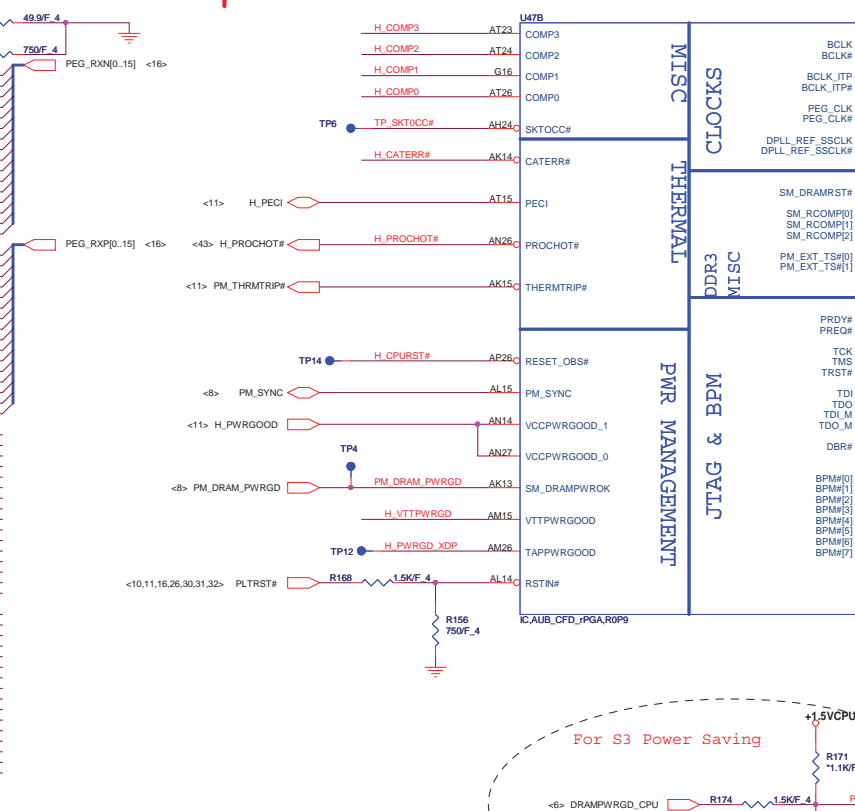
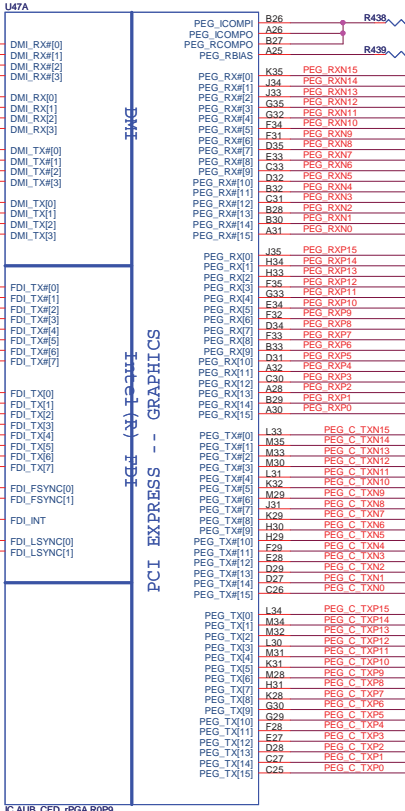
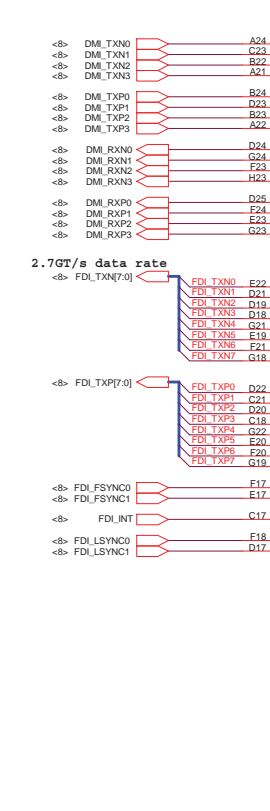
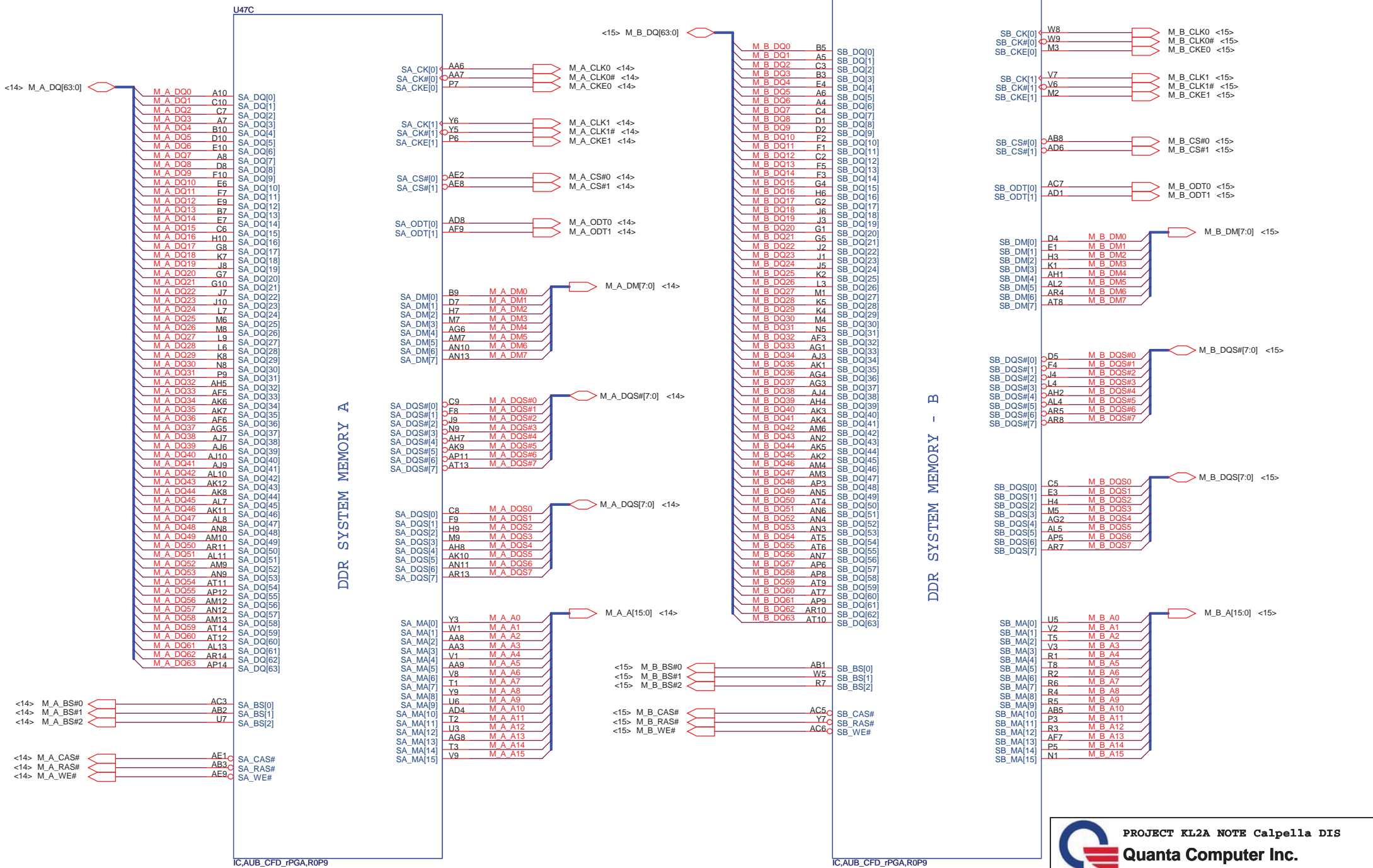


Table with 2 columns: Scan Chain (Default, CPU Only, GMCH Only) and STUFF/NO STUFF configurations for resistors R421, R411, R422, R430, R429, R412.



IC:AUB_CFD_IPGA,R0P9

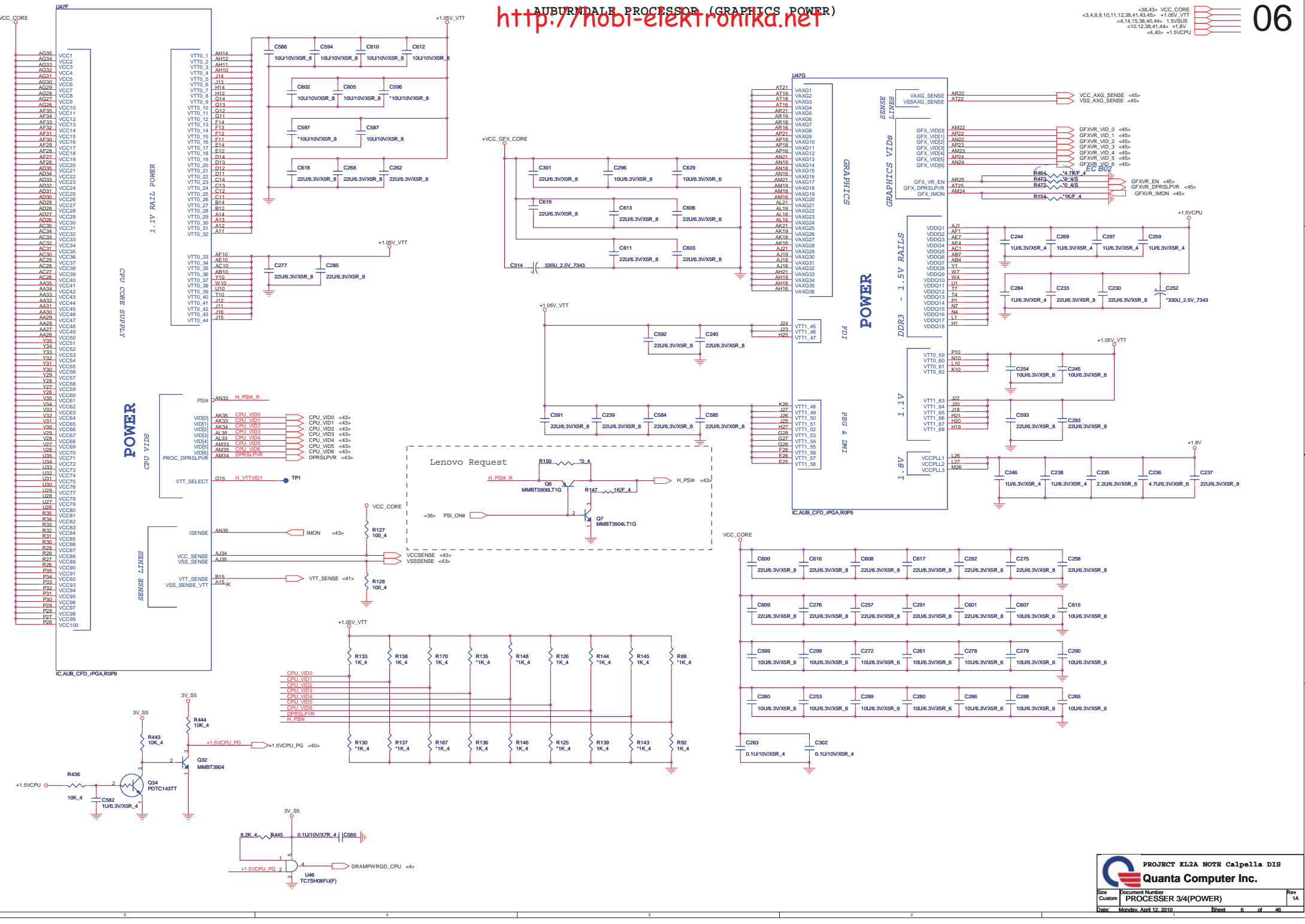
IC:AUB_CFD_IPGA,R0P9

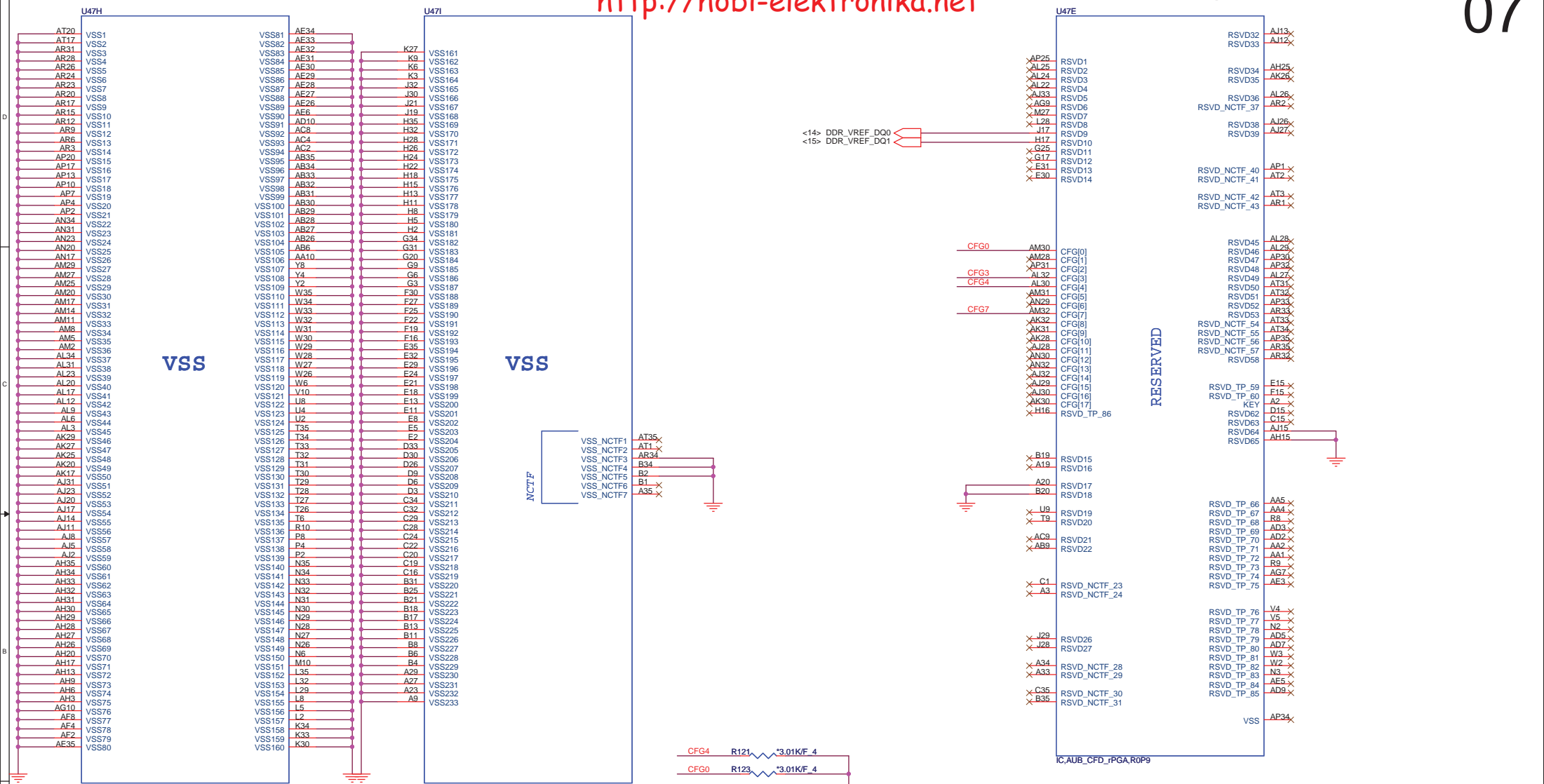
PROJECT KL2A NOTE Calpella DIS

Quanta Computer Inc.

Size Custom Document Number PROCESSOR 2/4(DDR)

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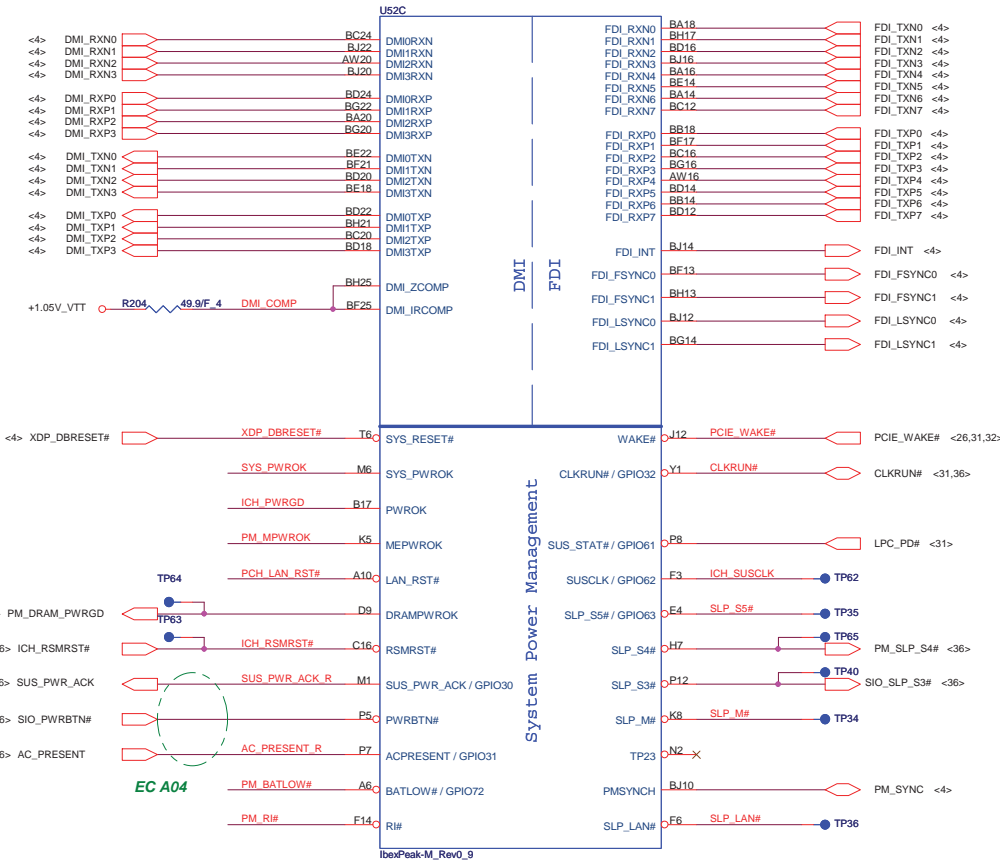
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

CFG4 R121 3.01K/F 4
 CFG0 R123 3.01K/F 4
 CFG3 R124 3.01K/F 4
 CFG7 R163 3.01K/F 4

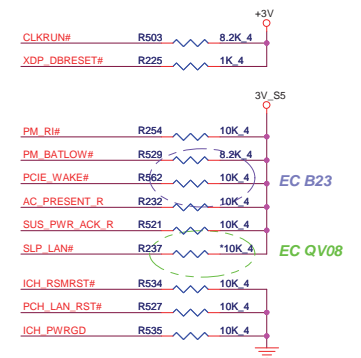
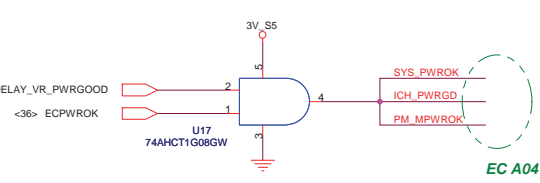
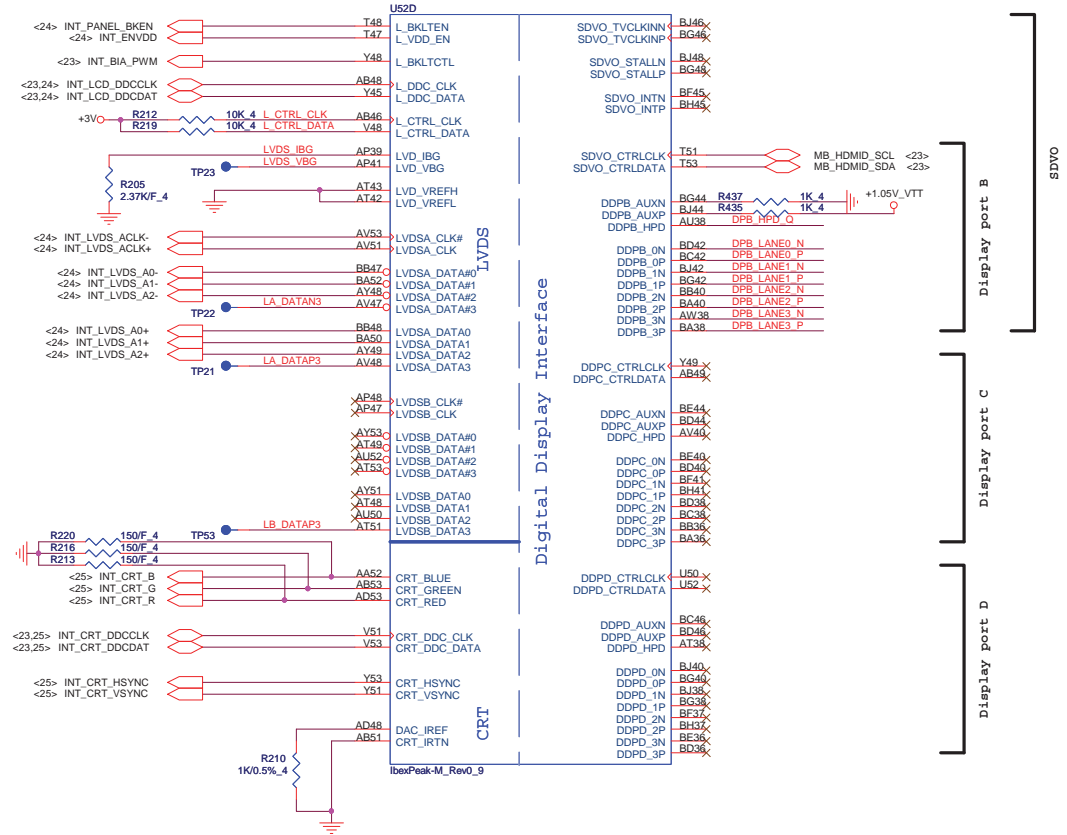
CFG[1:0] - PCI Express Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Express Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Express Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

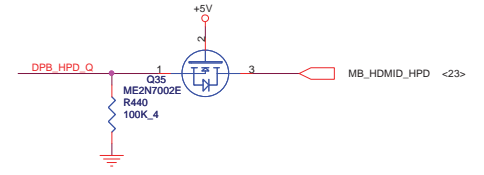
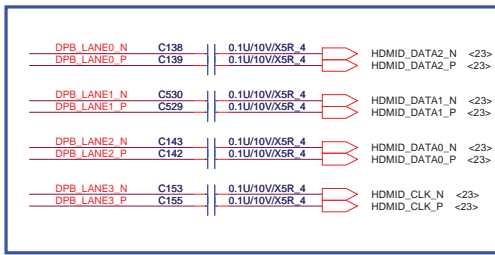
IBEX PEAK-M (DMI, FDI, GPIO)



IBEX PEAK-M (LVDS, DDI)

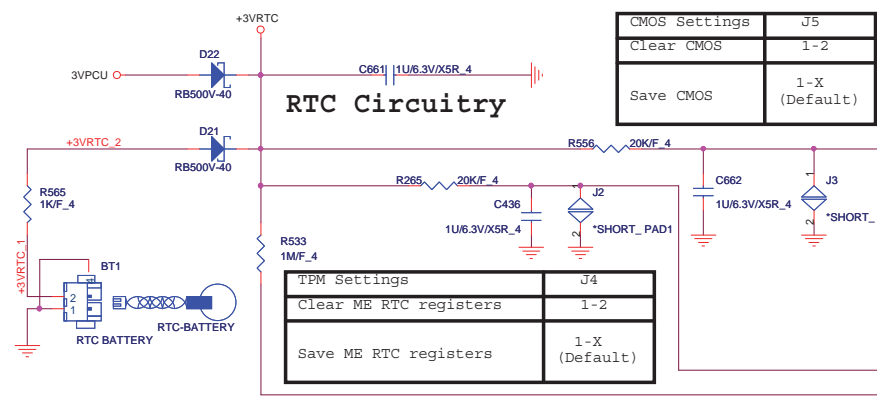


For UMA HDMI Function



<24,26,34,35,36,38,39,41,42,44> +3VRTC
 <3,4,8,10,11,12,14,15,23,24,25,26,27,28,29,30,31,32,33,34,35,36,38,39,43,44> +3V
 <6,8,10,11,12,16,31,38> 3V_S5
 <3,4,6,8,10,11,12,38,41,43,45> +1.05V_VTT

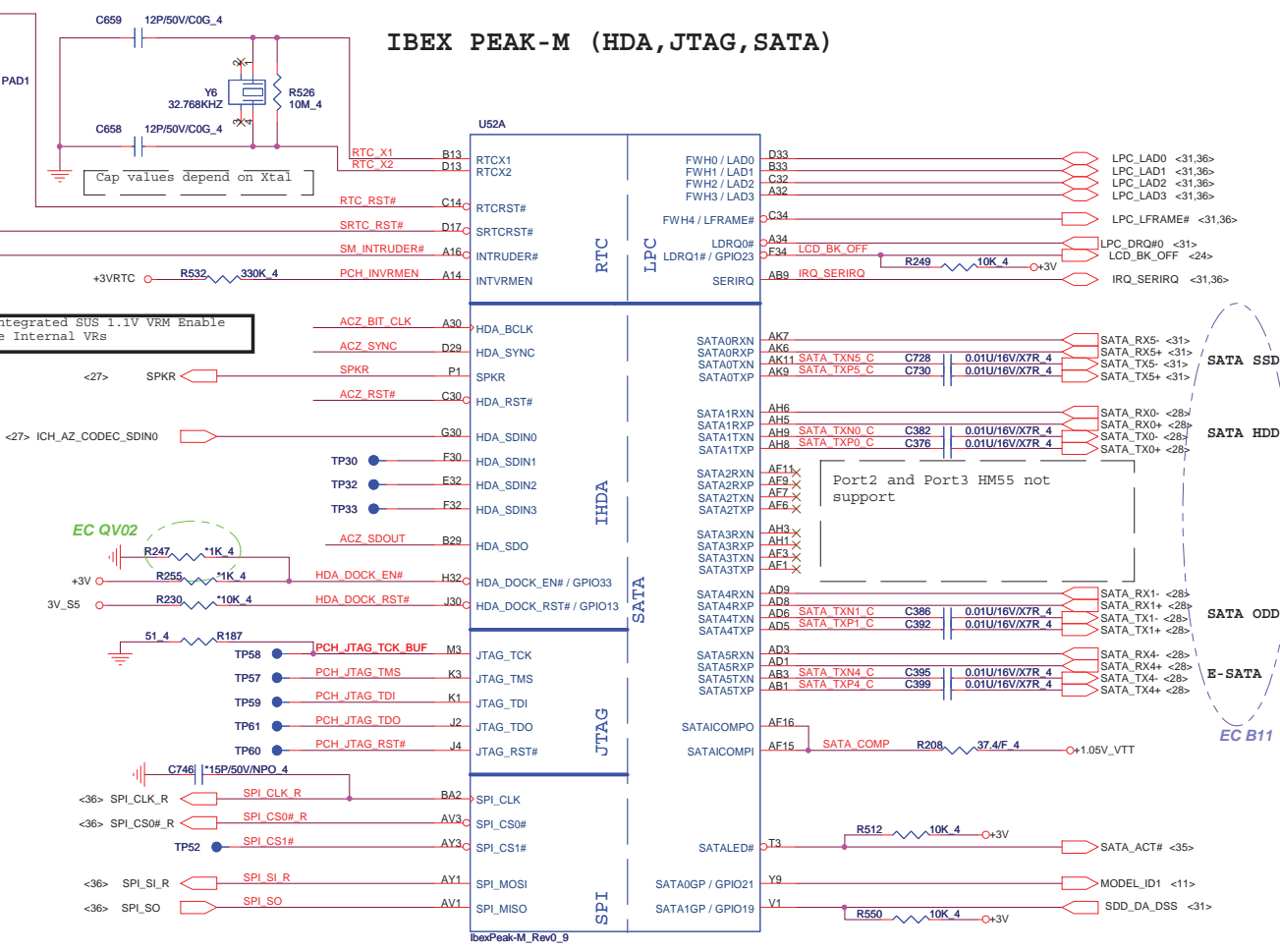
RTC Circuitry



CMOS Settings	J5
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J4
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

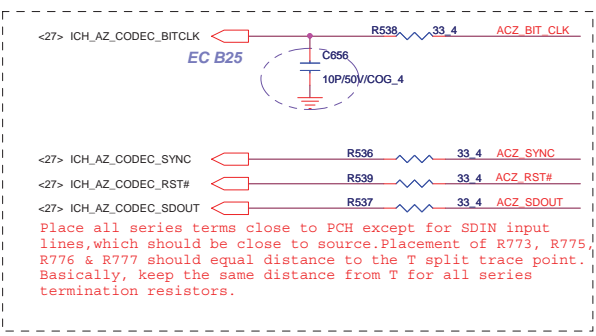
IBEX PEAK-M (HDA, JTAG, SATA)



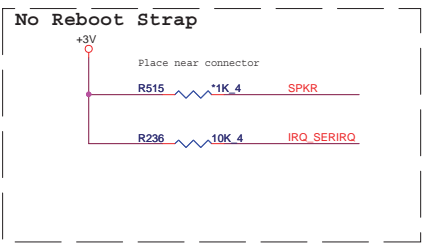
INVRMEN - Integrated SUS 1.1V VRM Enable
 High - Enable Internal VRs

Port2 and Port3 HM55 not support

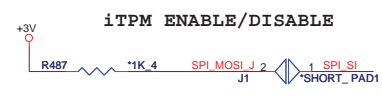
SATA SSD
 SATA HDD
 SATA ODD
 E-SATA



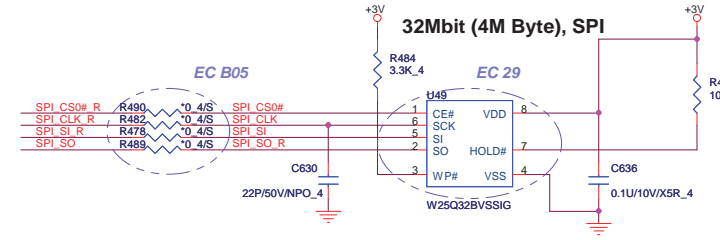
Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

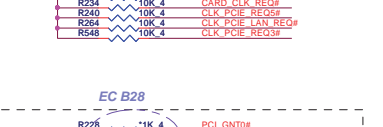
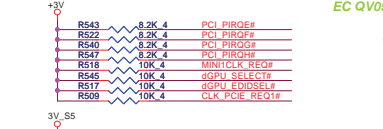
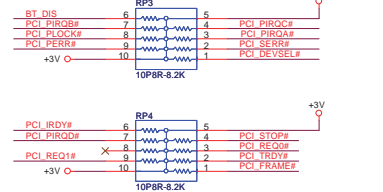
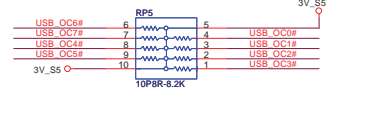
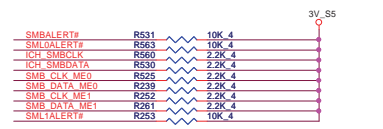
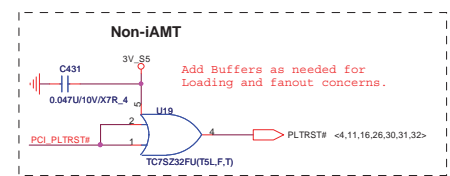
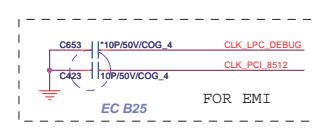
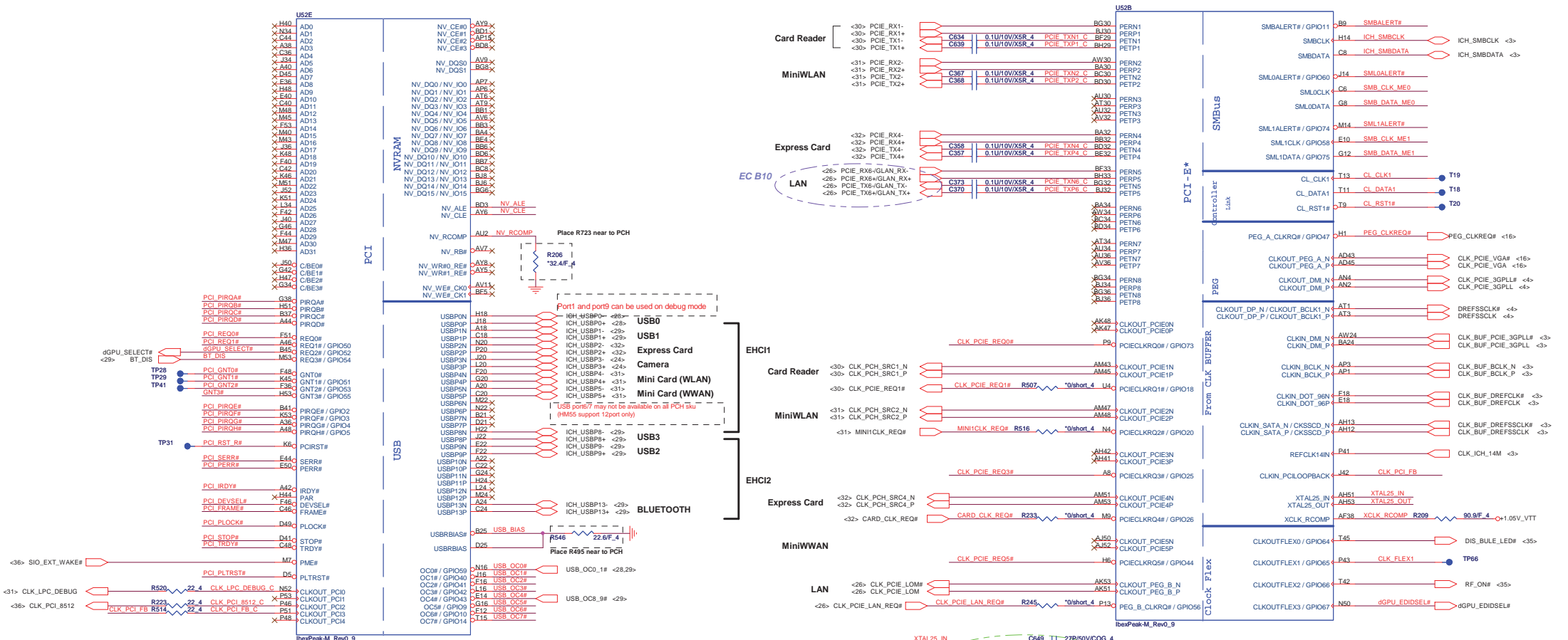


TPM Function	R487
Enable	Stuff
Disable	NC (Default)

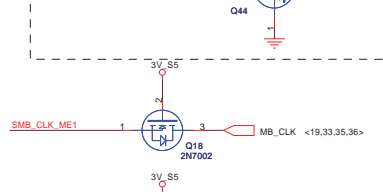
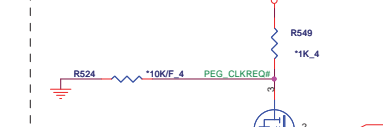
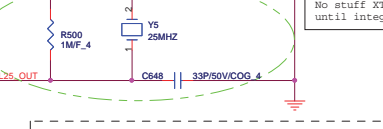


For PCH
 32Mbit (4M Byte), SPI





PCI_GNT0#	PCI_GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



DMI Termination Voltage

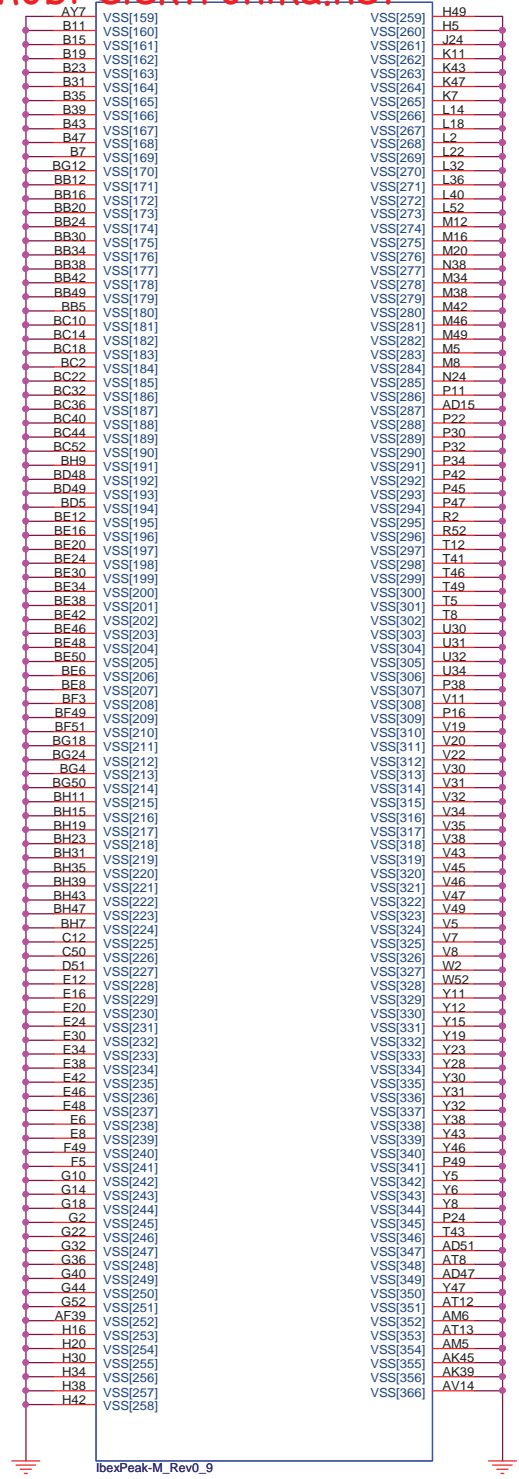
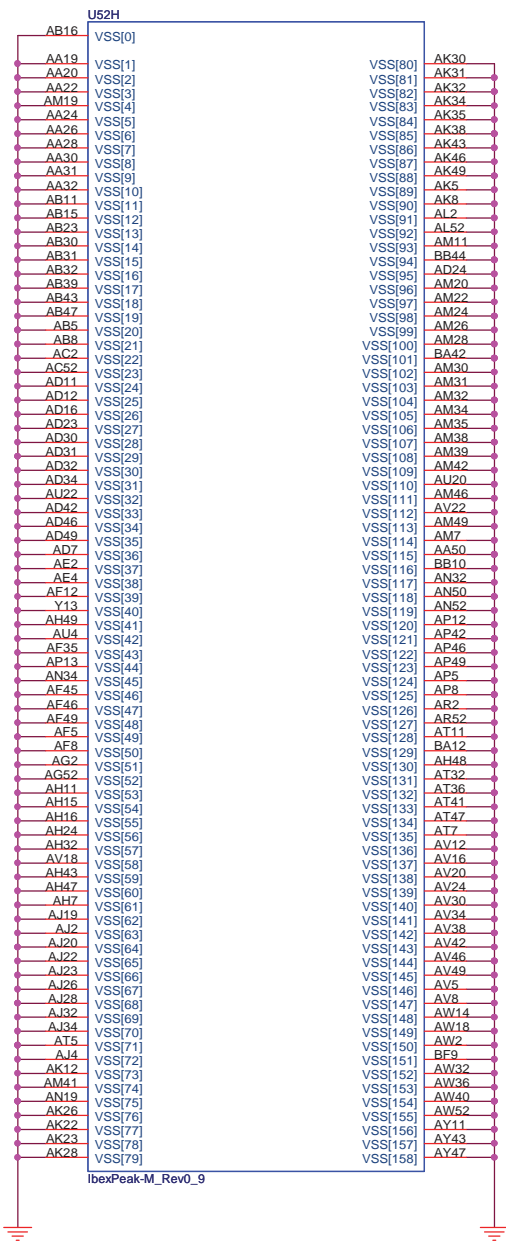
NV_CLE Set to Vcc when LOW
Set to Vcc/2 when HIGH

Danbury Technology Enabled

NV_ALE High = Enable
Low = Disable

A16 swap override strap/Top-Block Swap override jumper

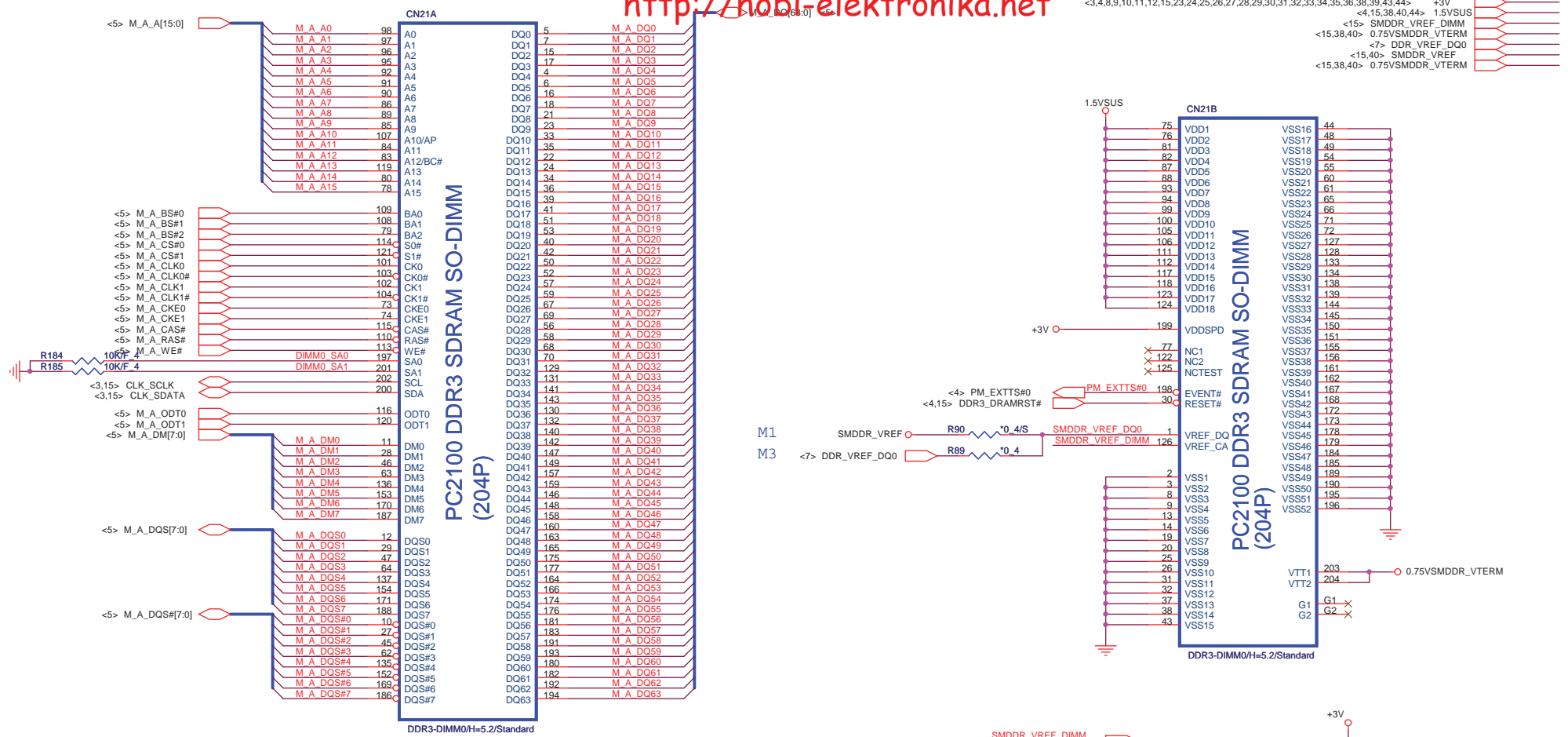
GN13# Low = A16 swap override/Top-Block Swap Override enabled
High = Default



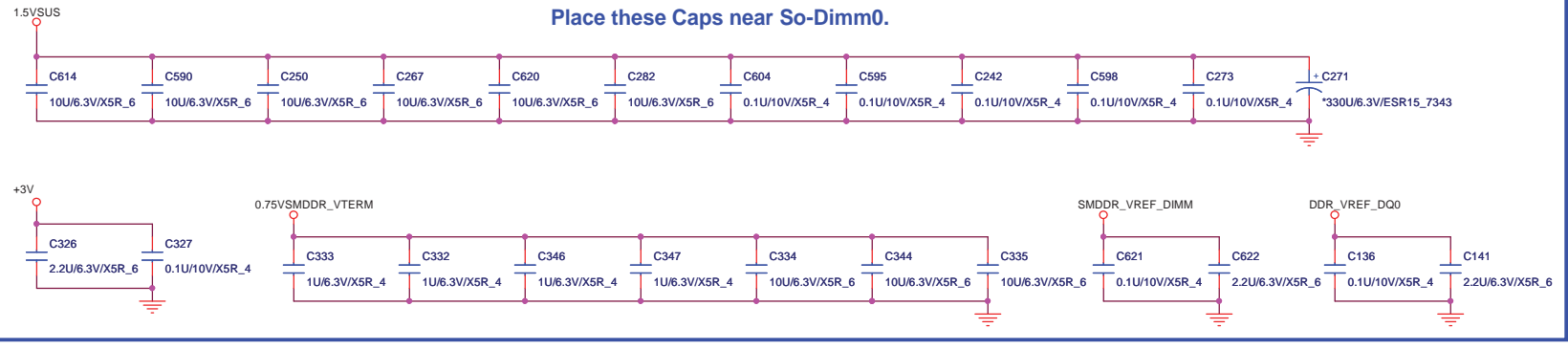
PROJECT KL2A NOTE Calpella DIS
Quanta Computer Inc.

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 Document Number: PCH 6/6 (GND)
 Date: Monday, April 12, 2010

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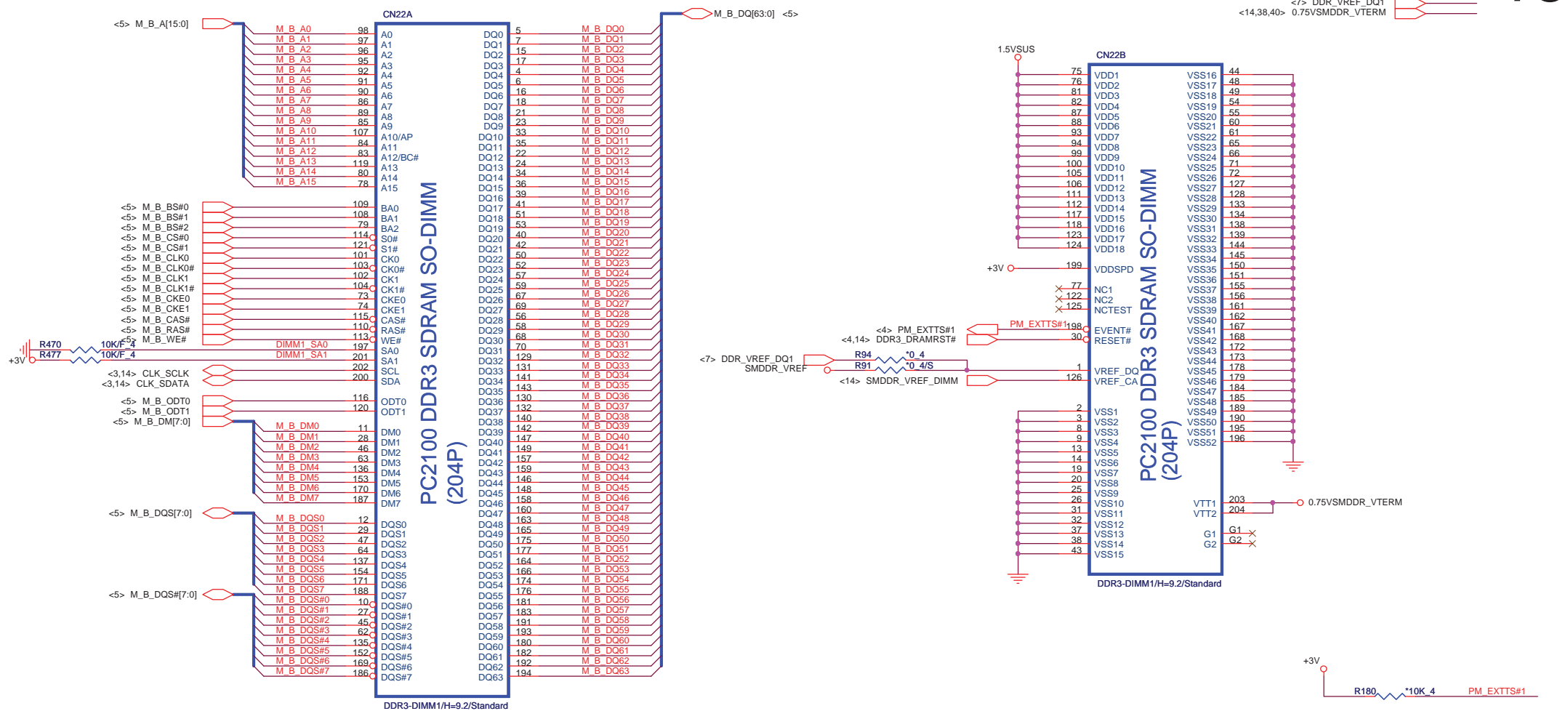


Place these Caps near So-Dimm0.

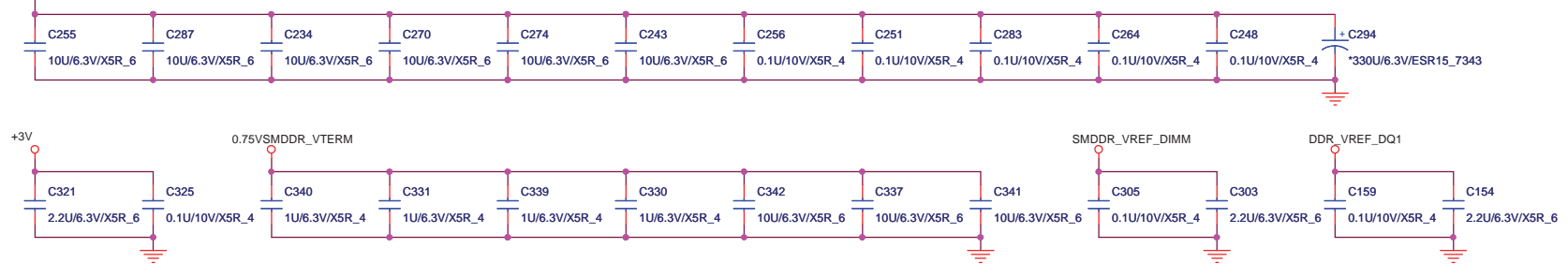


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Place these Caps near So-Dimm1.



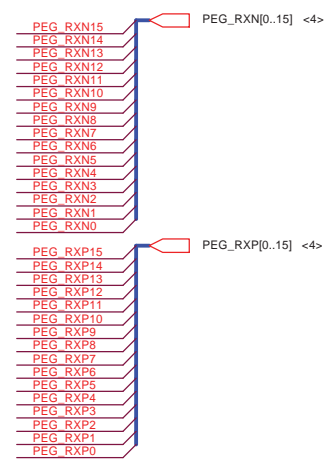
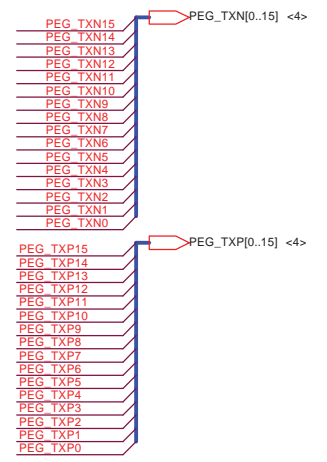
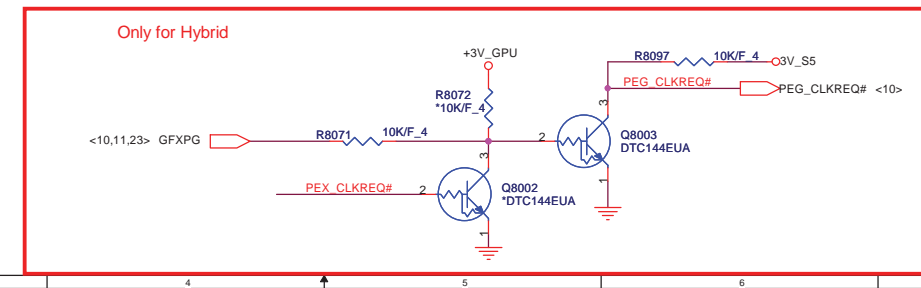
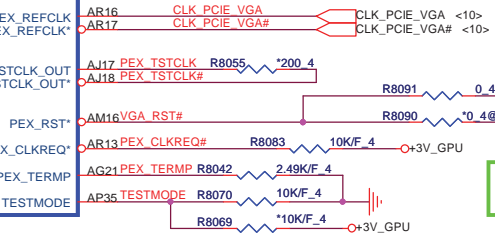
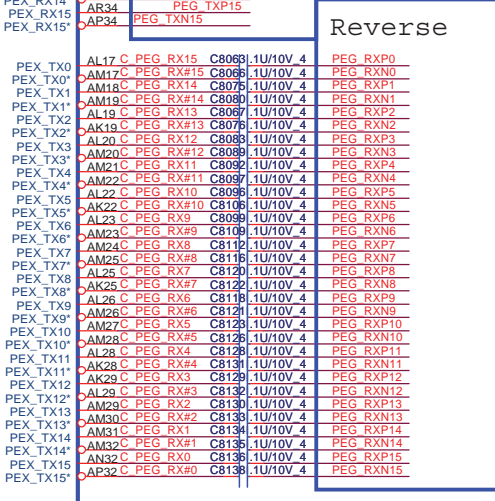
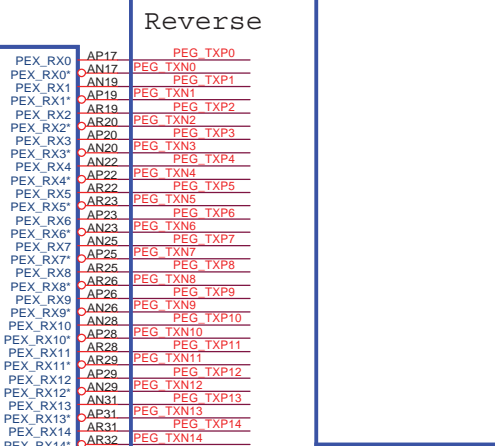
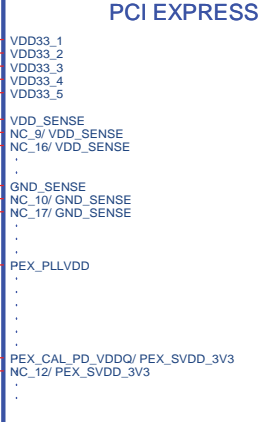
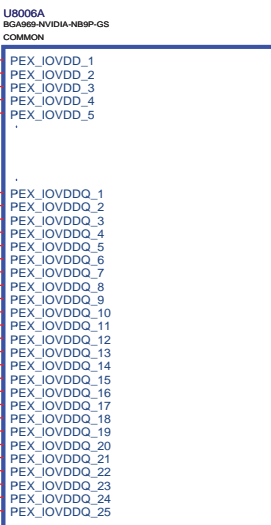
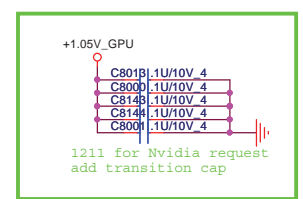
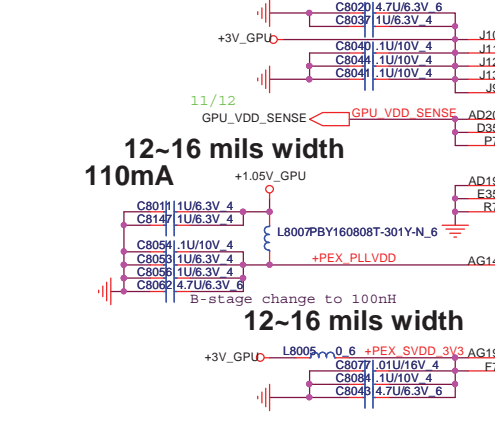
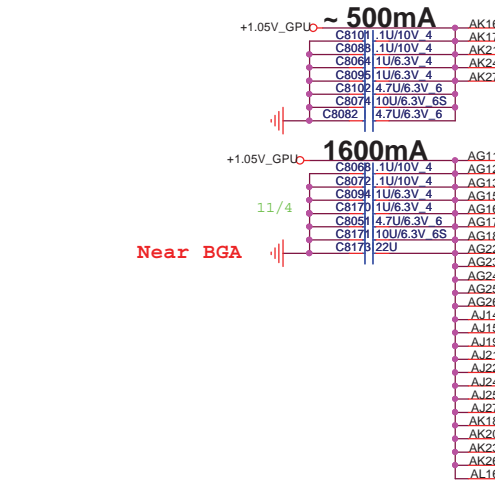
PROJECT KL2A NOTE Calpella DIS
Quanta Computer Inc.

Size Custom Document Number
 Custom DDR3 DIMM-1(H=9.2)

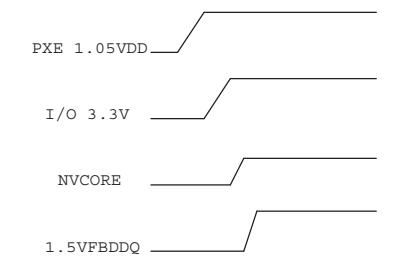
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PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

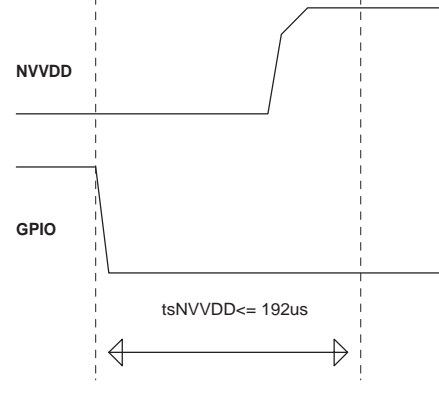
U8006A
DG4090-NVIDIA-NB9P-GS
COMMON



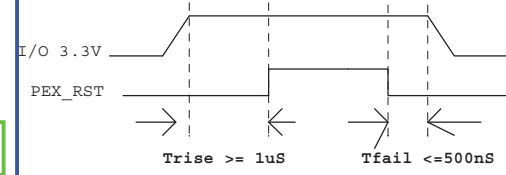
power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V NVVDD Maximum Settling Time



PEX_RST timing



PROJECT KL2A NOTE Calpella DIS
Quanta Computer Inc.
 Size Custom Document Number N10P-GE (PCIE I/F) 1/5 Rev 3B
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U8006B
BG989-NVIDIA-NB9P-GS
COMMON

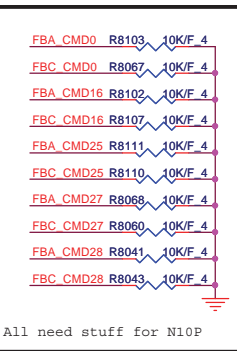
12/02 modify
package for N10

U8006C
BG989-NVIDIA-NB9P-GS
COMMON

12/02 modify
package for N10

<21> FBA_CMD0	V32	FBA_CMD0
<21> FBA_CMD1	W31	FBA_CMD1
<21> FBA_CMD2	Y32	FBA_CMD2
<21> FBA_CMD3	AB34	FBA_CMD3
<21> FBA_CMD4	AB35	FBA_CMD4
<21> FBA_CMD5	W35	FBA_CMD5
<21> FBA_CMD6	W33	FBA_CMD6
<21> FBA_CMD7	W30	FBA_CMD7
<21> FBA_CMD8	T34	FBA_CMD8
<21> FBA_CMD9	T35	FBA_CMD9
<21> FBA_CMD10	T35	FBA_CMD10
<21> FBA_CMD11	AB31	FBA_CMD11
<21> FBA_CMD12	Y30	FBA_CMD12
<21> FBA_CMD13	W32	FBA_CMD13
<21> FBA_CMD14	AA30	FBA_CMD14
<21> FBA_CMD15	AA32	FBA_CMD15
<21> FBA_CMD16	Y33	FBA_CMD16
<21> FBA_CMD17	U32	FBA_CMD17
<21> FBA_CMD18	U34	FBA_CMD18
<21> FBA_CMD19	U34	FBA_CMD19
<21> FBA_CMD20	Y35	FBA_CMD20
<21> FBA_CMD21	W34	FBA_CMD21
<21> FBA_CMD22	W34	FBA_CMD22
<21> FBA_CMD23	V30	FBA_CMD23
<21> FBA_CMD24	U35	FBA_CMD24
<21> FBA_CMD25	U39	FBA_CMD25
<21> FBA_CMD26	U33	FBA_CMD26
<21> FBA_CMD27	AB30	FBA_CMD27
<21> FBA_CMD28	AB33	FBA_CMD28
<21> FBA_CMD29	T33	FBA_CMD29
<21> FBA_CMD30	W29	FBA_CMD30

FBA_D00	L32	VMA_DQ0
FBA_D01	L33	VMA_DQ1
FBA_D02	N34	VMA_DQ2
FBA_D03	N34	VMA_DQ3
FBA_D04	N35	VMA_DQ4
FBA_D05	P35	VMA_DQ5
FBA_D06	P33	VMA_DQ6
FBA_D07	P34	VMA_DQ7
FBA_D08	K35	VMA_DQ8
FBA_D09	K33	VMA_DQ9
FBA_D10	K34	VMA_DQ10
FBA_D11	H33	VMA_DQ11
FBA_D12	G34	VMA_DQ12
FBA_D13	G33	VMA_DQ13
FBA_D14	E34	VMA_DQ14
FBA_D15	E33	VMA_DQ15
FBA_D16	G31	VMA_DQ16
FBA_D17	F30	VMA_DQ17
FBA_D18	G30	VMA_DQ18
FBA_D19	K30	VMA_DQ19
FBA_D20	K32	VMA_DQ20
FBA_D21	K32	VMA_DQ21
FBA_D22	H30	VMA_DQ22
FBA_D23	K31	VMA_DQ23
FBA_D24	L30	VMA_DQ24
FBA_D25	M32	VMA_DQ25
FBA_D26	N30	VMA_DQ26
FBA_D27	M30	VMA_DQ27
FBA_D28	M30	VMA_DQ28
FBA_D29	P31	VMA_DQ29
FBA_D30	R32	VMA_DQ30
FBA_D31	R30	VMA_DQ31
FBA_D32	AG30	VMA_DQ32
FBA_D33	AG32	VMA_DQ33
FBA_D34	AH31	VMA_DQ34
FBA_D35	AF31	VMA_DQ35
FBA_D36	AE30	VMA_DQ36
FBA_D37	AC32	VMA_DQ37
FBA_D38	AD30	VMA_DQ38
FBA_D39	AN33	VMA_DQ39
FBA_D40	AL31	VMA_DQ40
FBA_D41	AM33	VMA_DQ41
FBA_D42	AL33	VMA_DQ42
FBA_D43	AK30	VMA_DQ43
FBA_D44	AK32	VMA_DQ44
FBA_D45	AJ30	VMA_DQ45
FBA_D46	AH30	VMA_DQ46
FBA_D47	AH35	VMA_DQ47
FBA_D48	AH33	VMA_DQ48
FBA_D49	AH34	VMA_DQ49
FBA_D50	AH32	VMA_DQ50
FBA_D51	AJ33	VMA_DQ51
FBA_D52	AL35	VMA_DQ52
FBA_D53	AM34	VMA_DQ53
FBA_D54	AM35	VMA_DQ54
FBA_D55	AE33	VMA_DQ55
FBA_D56	AE32	VMA_DQ56
FBA_D57	AF34	VMA_DQ57
FBA_D58	AE35	VMA_DQ58
FBA_D59	AE34	VMA_DQ59
FBA_D60	AE33	VMA_DQ60
FBA_D61	AB32	VMA_DQ61
FBA_D62	AC35	VMA_DQ62
FBA_D63	AC35	VMA_DQ63



<22> FBC_CMD0	C17	FBC_CMD0
<22> FBC_CMD1	B18	FBC_CMD1
<22> FBC_CMD2	F21	FBC_CMD2
<22> FBC_CMD3	A23	FBC_CMD3
<22> FBC_CMD4	D21	FBC_CMD4
<22> FBC_CMD5	B23	FBC_CMD5
<22> FBC_CMD6	E20	FBC_CMD6
<22> FBC_CMD7	C21	FBC_CMD7
<22> FBC_CMD8	F20	FBC_CMD8
<22> FBC_CMD9	F19	FBC_CMD9
<22> FBC_CMD10	F23	FBC_CMD10
<22> FBC_CMD11	A22	FBC_CMD11
<22> FBC_CMD12	G22	FBC_CMD12
<22> FBC_CMD13	B22	FBC_CMD13
<22> FBC_CMD14	F24	FBC_CMD14
<22> FBC_CMD15	C25	FBC_CMD15
<22> FBC_CMD16	E22	FBC_CMD16
<22> FBC_CMD17	G20	FBC_CMD17
<22> FBC_CMD18	B20	FBC_CMD18
<22> FBC_CMD19	A22	FBC_CMD19
<22> FBC_CMD20	D22	FBC_CMD20
<22> FBC_CMD21	D20	FBC_CMD21
<22> FBC_CMD22	E19	FBC_CMD22
<22> FBC_CMD23	D19	FBC_CMD23
<22> FBC_CMD24	F18	FBC_CMD24
<22> FBC_CMD25	C18	FBC_CMD25
<22> FBC_CMD26	F22	FBC_CMD26
<22> FBC_CMD27	C23	FBC_CMD27
<22> FBC_CMD28	B20	FBC_CMD28
<22> FBC_CMD29	B20	FBC_CMD29
<22> FBC_CMD30	A20	FBC_CMD30

FBC_D00	B13	VMC_DQ0
FBC_D01	D13	VMC_DQ1
FBC_D02	A14	VMC_DQ2
FBC_D03	C16	VMC_DQ3
FBC_D04	C16	VMC_DQ4
FBC_D05	B16	VMC_DQ5
FBC_D06	A17	VMC_DQ6
FBC_D07	C13	VMC_DQ7
FBC_D08	B11	VMC_DQ8
FBC_D09	C11	VMC_DQ9
FBC_D10	B11	VMC_DQ10
FBC_D11	A11	VMC_DQ11
FBC_D12	C10	VMC_DQ12
FBC_D13	C8	VMC_DQ13
FBC_D14	A8	VMC_DQ14
FBC_D15	E8	VMC_DQ15
FBC_D16	F8	VMC_DQ16
FBC_D17	F8	VMC_DQ17
FBC_D18	F40	VMC_DQ18
FBC_D19	F9	VMC_DQ19
FBC_D20	D8	VMC_DQ20
FBC_D21	D11	VMC_DQ21
FBC_D22	D11	VMC_DQ22
FBC_D23	E11	VMC_DQ23
FBC_D24	D12	VMC_DQ24
FBC_D25	F13	VMC_DQ25
FBC_D26	F14	VMC_DQ26
FBC_D27	F15	VMC_DQ27
FBC_D28	F16	VMC_DQ28
FBC_D29	F16	VMC_DQ29
FBC_D30	F17	VMC_DQ30
FBC_D31	D29	VMC_DQ31
FBC_D32	F27	VMC_DQ32
FBC_D33	F28	VMC_DQ33
FBC_D34	E28	VMC_DQ34
FBC_D35	E28	VMC_DQ35
FBC_D36	D26	VMC_DQ36
FBC_D37	F25	VMC_DQ37
FBC_D38	E25	VMC_DQ38
FBC_D39	F32	VMC_DQ39
FBC_D40	E32	VMC_DQ40
FBC_D41	F33	VMC_DQ41
FBC_D42	D33	VMC_DQ42
FBC_D43	C33	VMC_DQ43
FBC_D44	F30	VMC_DQ44
FBC_D45	D30	VMC_DQ45
FBC_D46	F29	VMC_DQ46
FBC_D47	E29	VMC_DQ47
FBC_D48	B29	VMC_DQ48
FBC_D49	C29	VMC_DQ49
FBC_D50	B31	VMC_DQ50
FBC_D51	C32	VMC_DQ51
FBC_D52	B32	VMC_DQ52
FBC_D53	B32	VMC_DQ53
FBC_D54	B35	VMC_DQ54
FBC_D55	A28	VMC_DQ55
FBC_D56	B28	VMC_DQ56
FBC_D57	A28	VMC_DQ57
FBC_D58	C28	VMC_DQ58
FBC_D59	C28	VMC_DQ59
FBC_D60	E25	VMC_DQ60
FBC_D61	D25	VMC_DQ61
FBC_D62	A25	VMC_DQ62
FBC_D63	A25	VMC_DQ63

12/02 modify
package for N10

VMA_DM0	H32	FBA_DQM0
VMA_DM1	H34	FBA_DQM1
VMA_DM2	H30	FBA_DQM2
VMA_DM3	F30	FBA_DQM3
VMA_DM4	AF32	FBA_DQM4
VMA_DM5	AL32	FBA_DQM5
VMA_DM6	AL34	FBA_DQM6
VMA_DM7	AF35	FBA_DQM7
VMA_WDQ50	H34	FBA_DQS_WP0
VMA_WDQ52	H32	FBA_DQS_WP1
VMA_WDQ53	H31	FBA_DQS_WP2
VMA_WDQ54	AF31	FBA_DQS_WP3
VMA_WDQ55	AF32	FBA_DQS_WP4
VMA_WDQ56	AF34	FBA_DQS_WP5
VMA_WDQ57	AC33	FBA_DQS_WP6
VMA_RDQ50	H35	FBA_DQS_RN0
VMA_RDQ51	G35	FBA_DQS_RN1
VMA_RDQ52	H31	FBA_DQS_RN2
VMA_RDQ53	H32	FBA_DQS_RN3
VMA_RDQ54	AD32	FBA_DQS_RN4
VMA_RDQ55	AF31	FBA_DQS_RN5
VMA_RDQ56	AF35	FBA_DQS_RN6
VMA_RDQ57	AF34	FBA_DQS_RN7

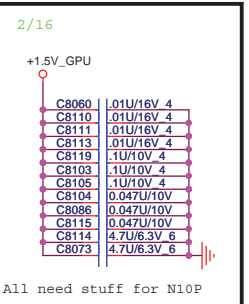
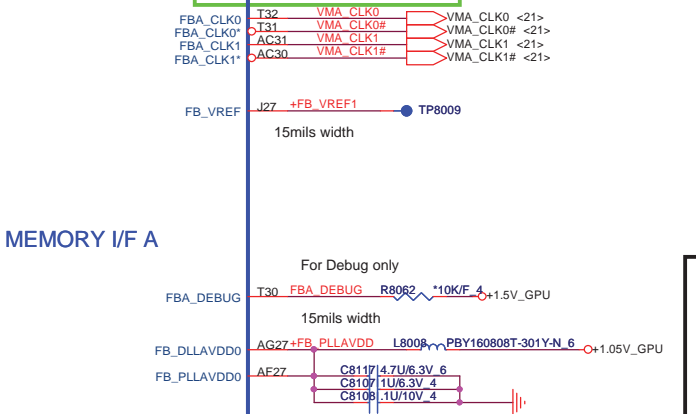
12/02 modify
package for N10

VMC_DM0	A16	FBC_DQM0
VMC_DM1	D10	FBC_DQM1
VMC_DM2	F11	FBC_DQM2
VMC_DM3	D15	FBC_DQM3
VMC_DM4	D27	FBC_DQM4
VMC_DM5	D34	FBC_DQM5
VMC_DM6	A34	FBC_DQM6
VMC_DM7	D28	FBC_DQM7
VMC_WDQ50	C14	FBC_DQS_WP0
VMC_WDQ51	A10	FBC_DQS_WP1
VMC_WDQ52	E10	FBC_DQS_WP2
VMC_WDQ53	D14	FBC_DQS_WP3
VMC_WDQ54	E26	FBC_DQS_WP4
VMC_WDQ55	D32	FBC_DQS_WP5
VMC_WDQ56	A32	FBC_DQS_WP6
VMC_WDQ57	B26	FBC_DQS_WP7
VMC_RDQ50	B14	FBC_DQS_RN0
VMC_RDQ51	B10	FBC_DQS_RN1
VMC_RDQ52	D9	FBC_DQS_RN2
VMC_RDQ53	E14	FBC_DQS_RN3
VMC_RDQ54	F26	FBC_DQS_RN4
VMC_RDQ55	D31	FBC_DQS_RN5
VMC_RDQ56	A31	FBC_DQS_RN6
VMC_RDQ57	A26	FBC_DQS_RN7

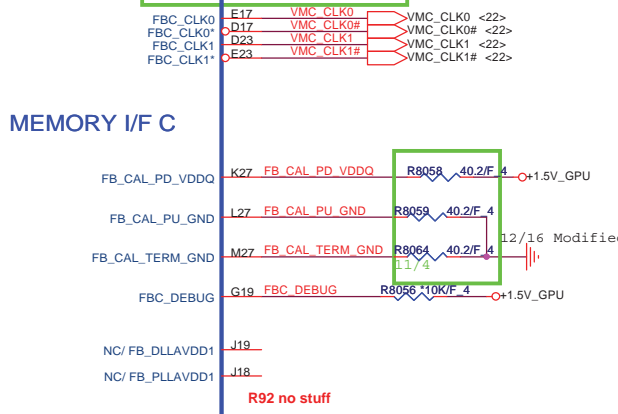
12/02 modify
package for N10

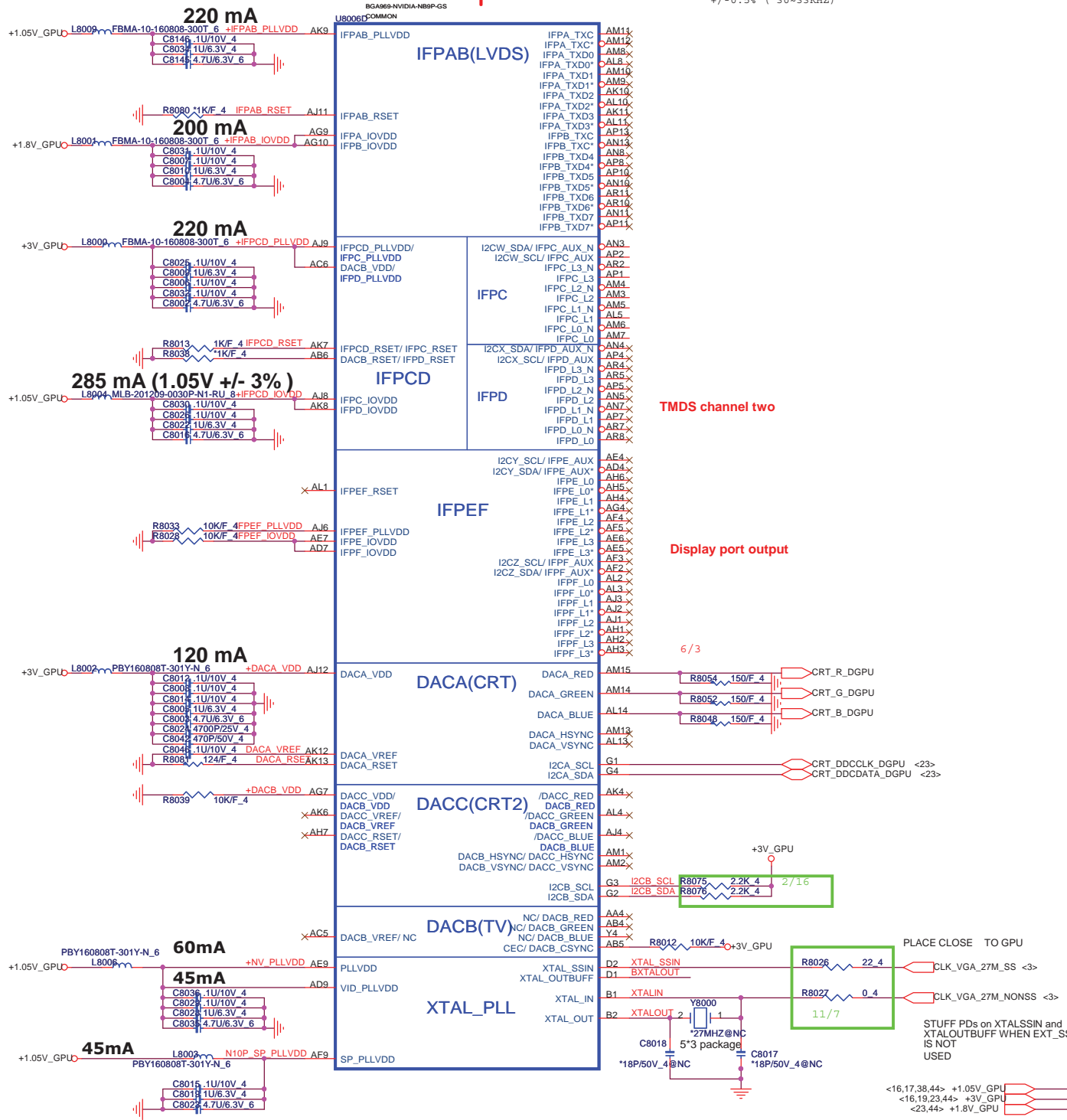
VMC_DM0	A16	FBC_DQM0
VMC_DM1	D10	FBC_DQM1
VMC_DM2	F11	FBC_DQM2
VMC_DM3	D15	FBC_DQM3
VMC_DM4	D27	FBC_DQM4
VMC_DM5	D34	FBC_DQM5
VMC_DM6	A34	FBC_DQM6
VMC_DM7	D28	FBC_DQM7
VMC_WDQ50	C14	FBC_DQS_WP0
VMC_WDQ51	A10	FBC_DQS_WP1
VMC_WDQ52	E10	FBC_DQS_WP2
VMC_WDQ53	D14	FBC_DQS_WP3
VMC_WDQ54	E26	FBC_DQS_WP4
VMC_WDQ55	D32	FBC_DQS_WP5
VMC_WDQ56	A32	FBC_DQS_WP6
VMC_WDQ57	B26	FBC_DQS_WP7
VMC_RDQ50	B14	FBC_DQS_RN0
VMC_RDQ51	B10	FBC_DQS_RN1
VMC_RDQ52	D9	FBC_DQS_RN2
VMC_RDQ53	E14	FBC_DQS_RN3
VMC_RDQ54	F26	FBC_DQS_RN4
VMC_RDQ55	D31	FBC_DQS_RN5
VMC_RDQ56	A31	FBC_DQS_RN6
VMC_RDQ57	A26	FBC_DQS_RN7

MEMORY I/F A



MEMORY I/F C





TMD5 channel two

Display port output

6/3

XTAL SSIN R8025 *10K/F 4
 BXTALOUT R8015 *10K/F 4
 11/4

10 kΩ pull-down only if no spread chip used.

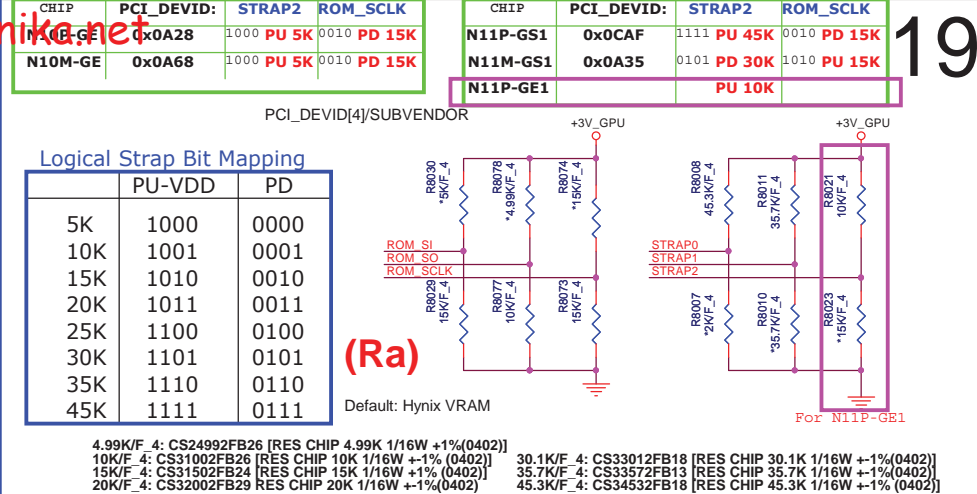
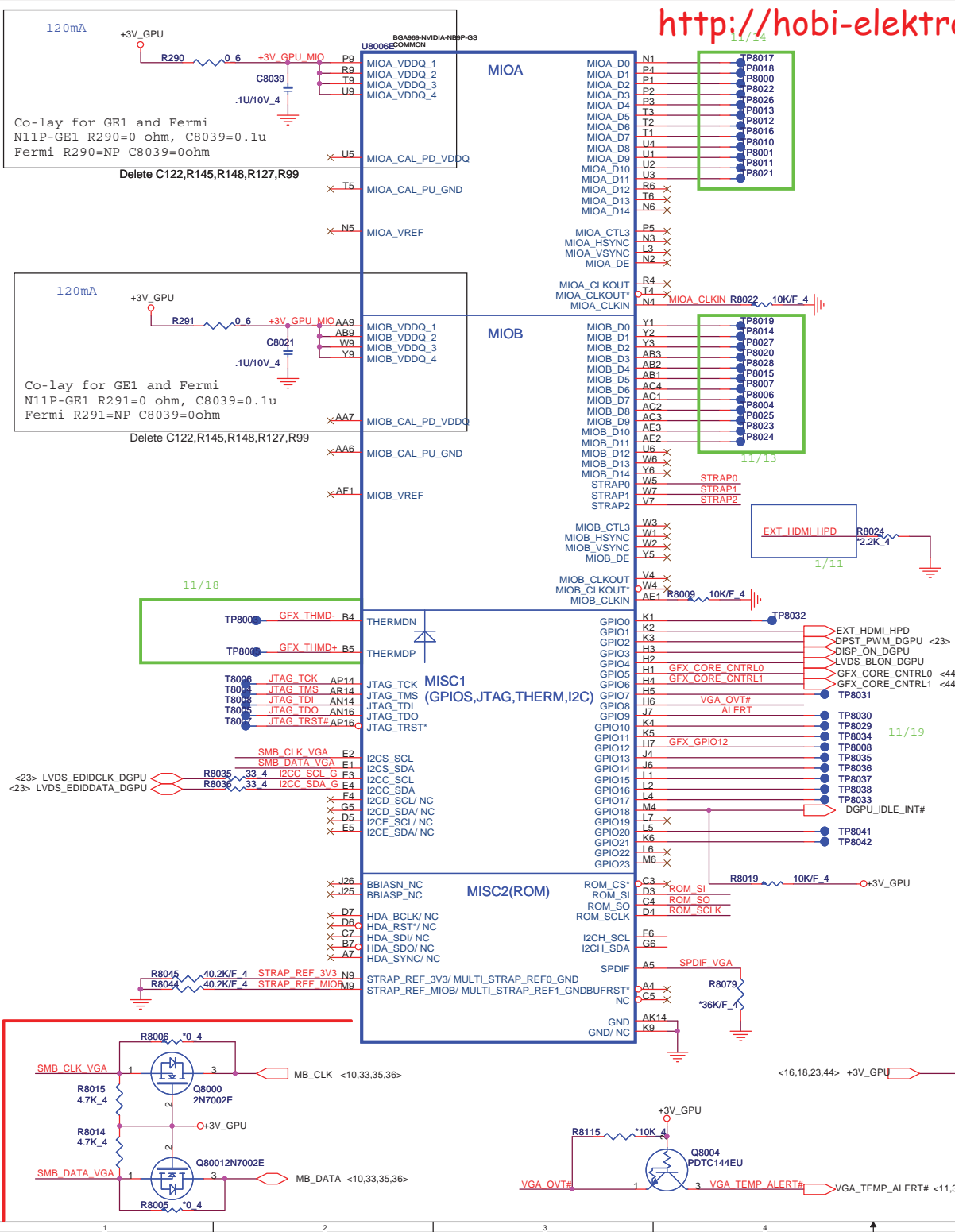
STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

<16,17,38,44> +1.05V_GPU
 <16,19,23,44> +3V_GPU
 <23,44> +1.8V_GPU

PROJECT KL2A NOTE Calpella DIS
Quanta Computer Inc.

Size Custom Document Number N10P-GE (DISPLAY) 3/5 Rev 3B

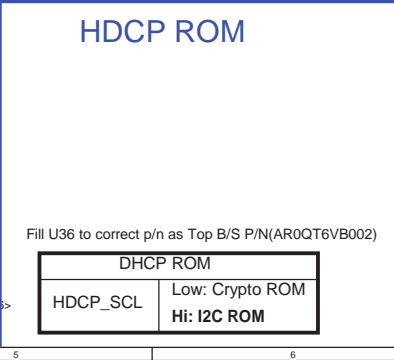
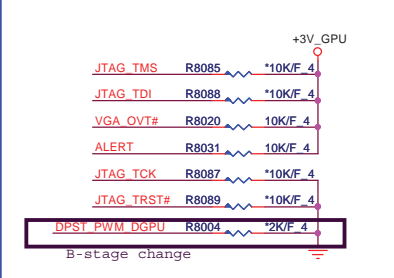
Date: Monday, April 12, 2010 Sheet 18 of 46

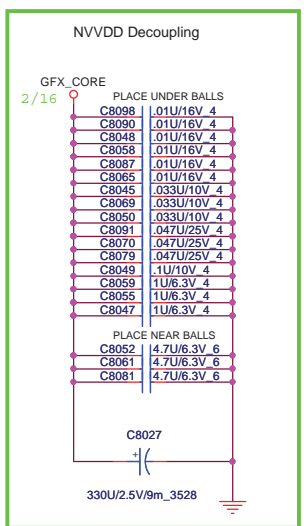
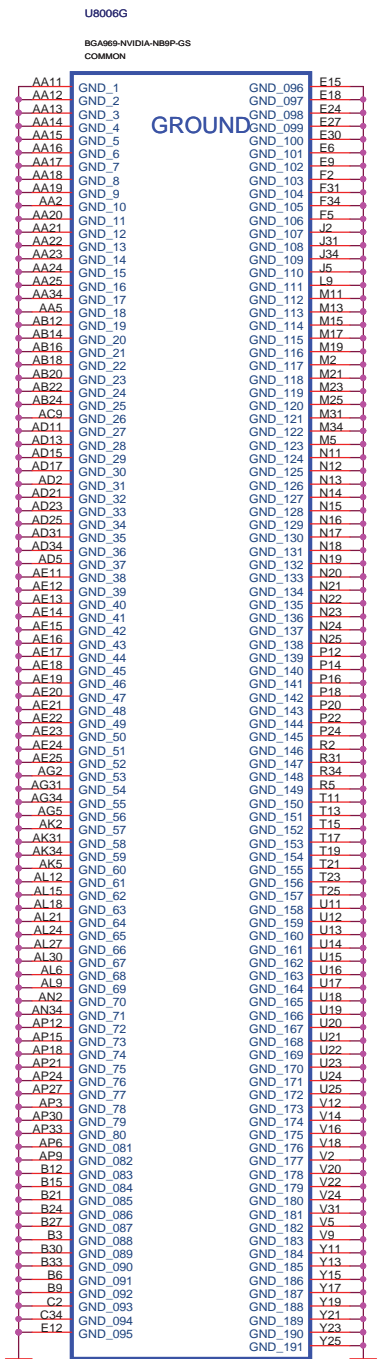
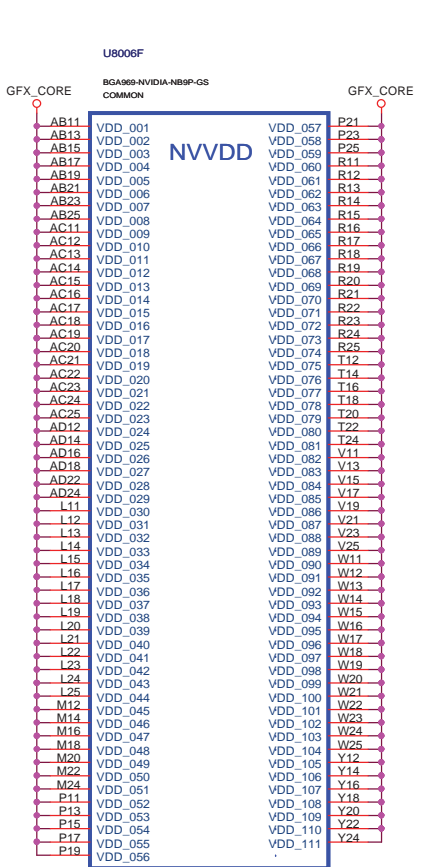


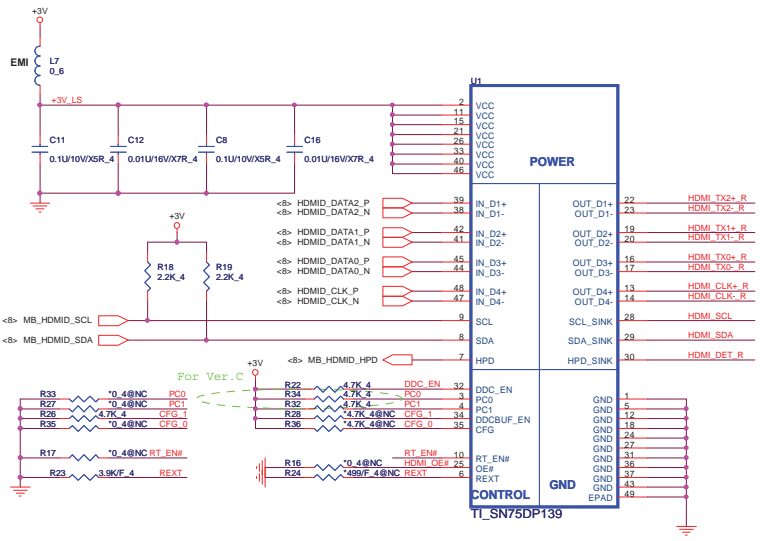
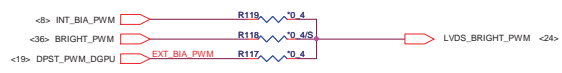
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	NB10X	XCLK_417	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	Reserved	Reserved	Reserved	
0001	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101	Reserved	Reserved	Reserved	
0110	Reserved	Reserved	Reserved	
XXXX	DDR3 64Mx16x8, 128bit, 1GB, 667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB, 667MHz	Samsung	K4W1G1646D-EC12	

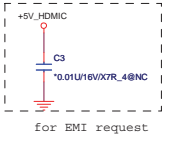




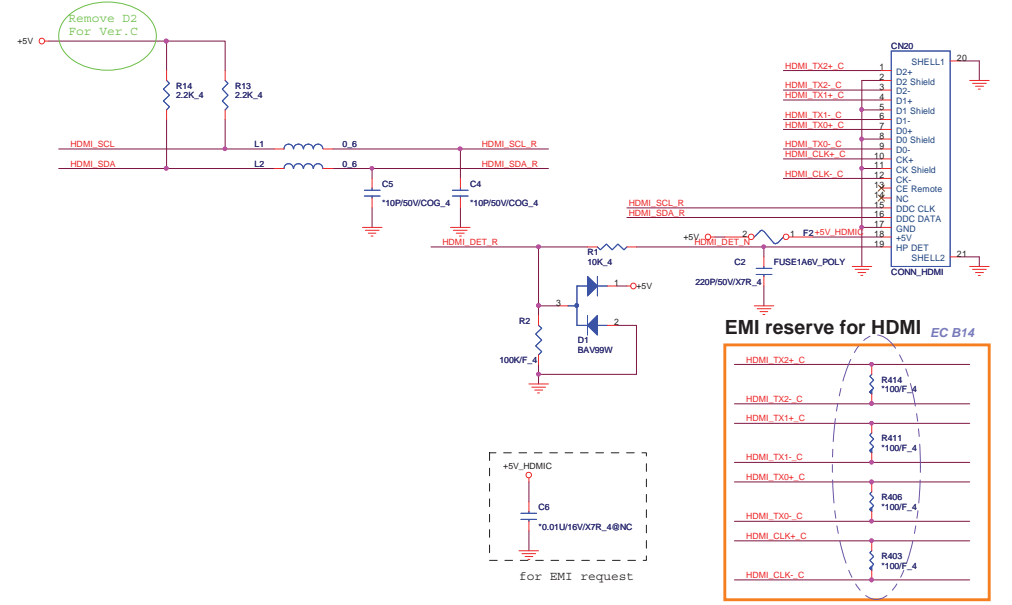


EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

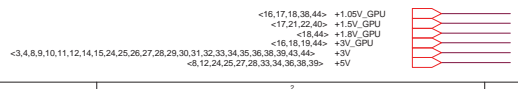
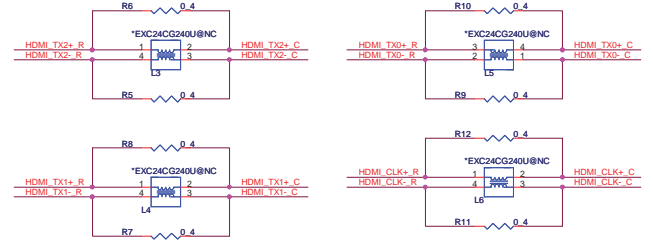
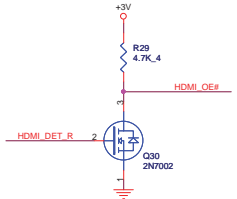
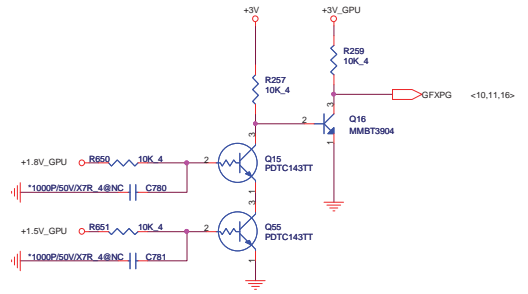
PS8101 Pin34/35 is NC
 SCLZ/SDAZ Low-level input/output Voltage
 CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
 CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
 CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
 CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V



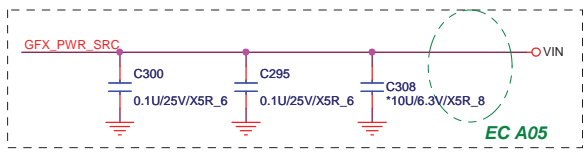
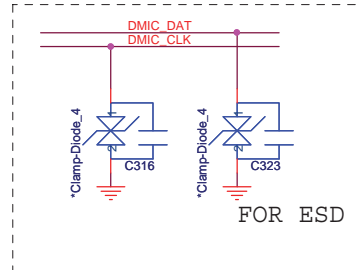
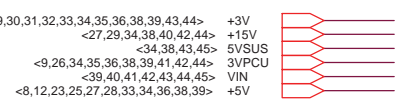
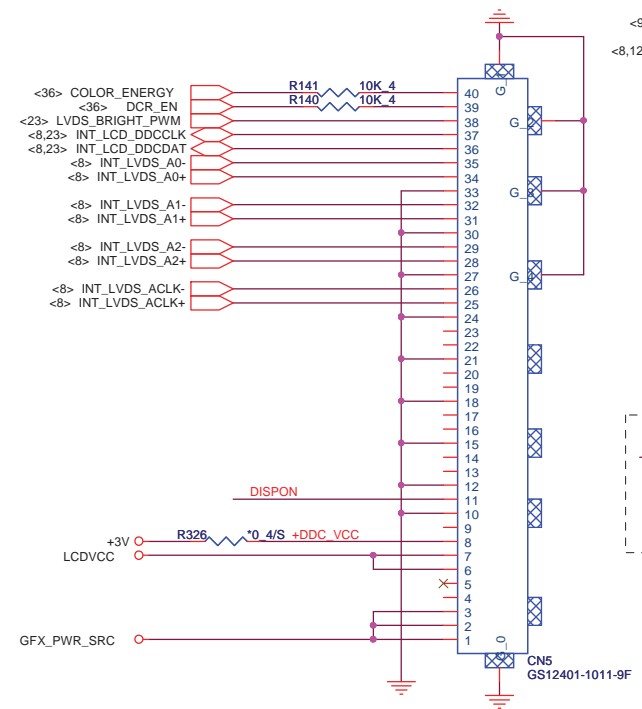
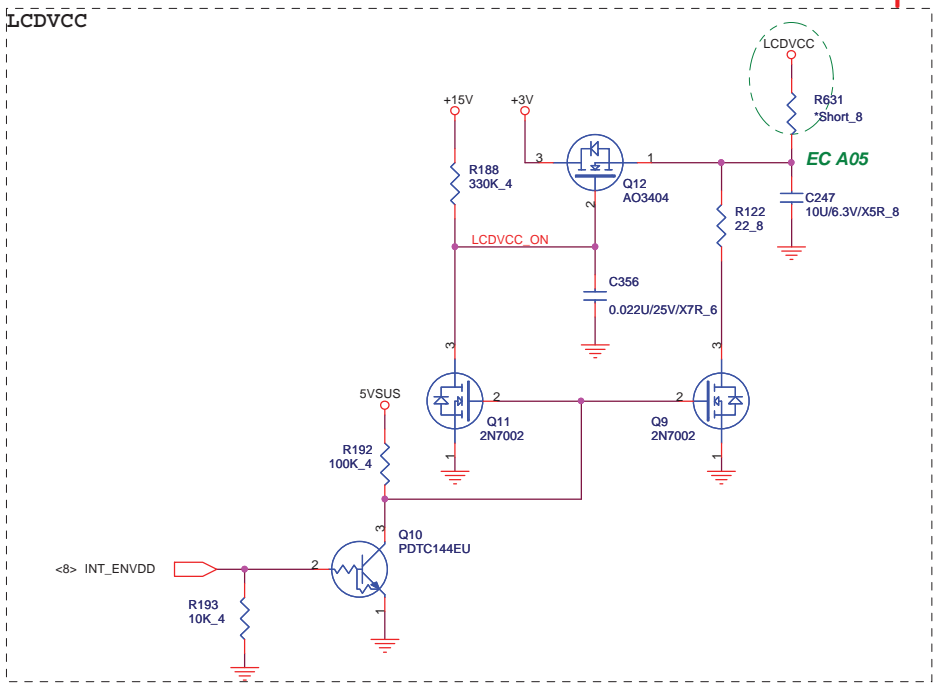
HDMI



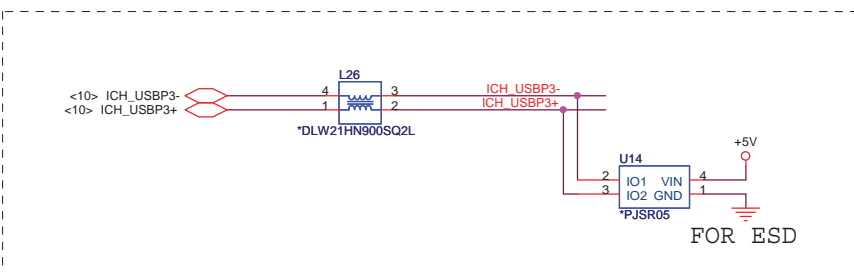
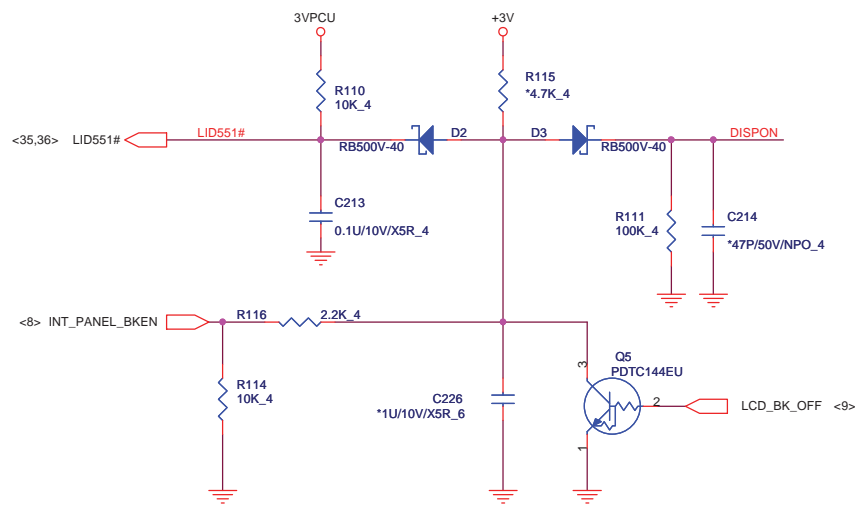
GPU all PWROK



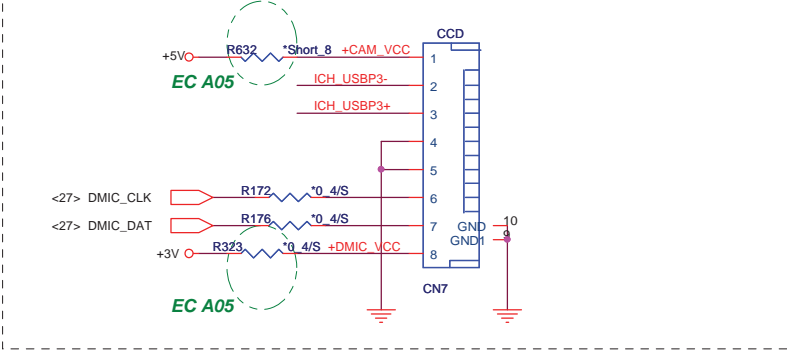
PROJECT KL2A NOTE Calpella DIS
Quanta Computer Inc.
 Size: Document Number
 Custom: Madison LVDS/HDMI/CRT switchable
 Date: Monday, April 12, 2010 Sheet: 23 of 46



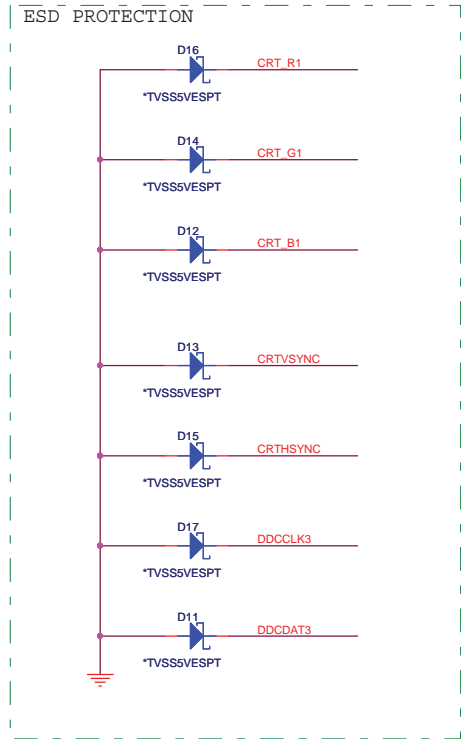
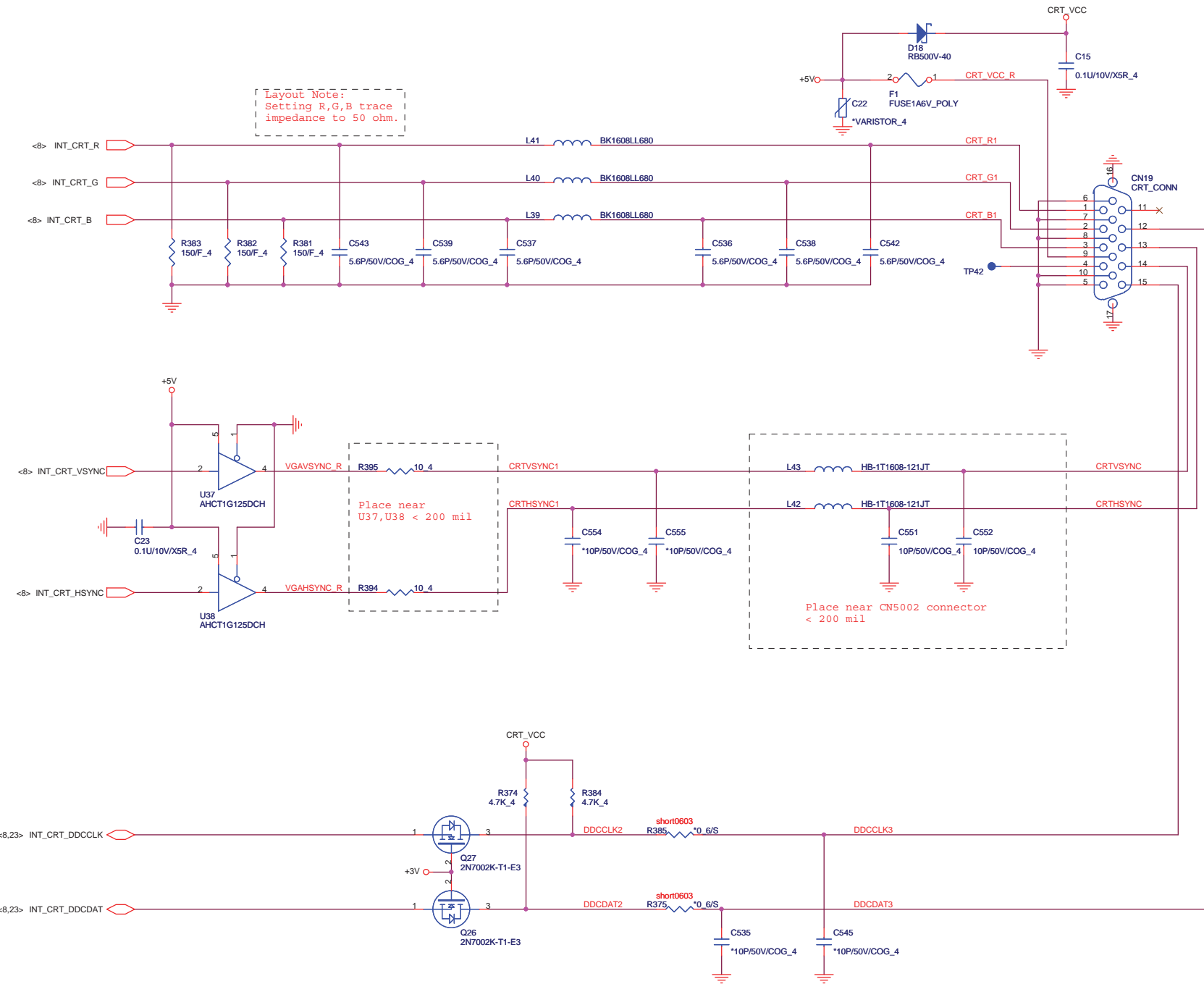
back light



CAMERA

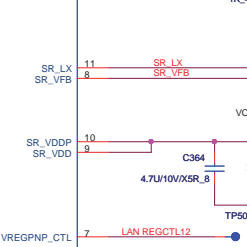
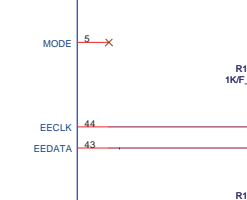
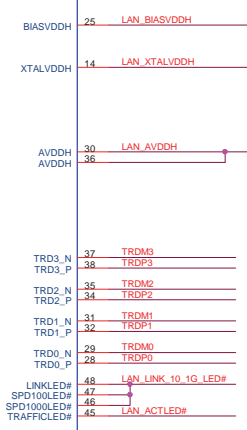
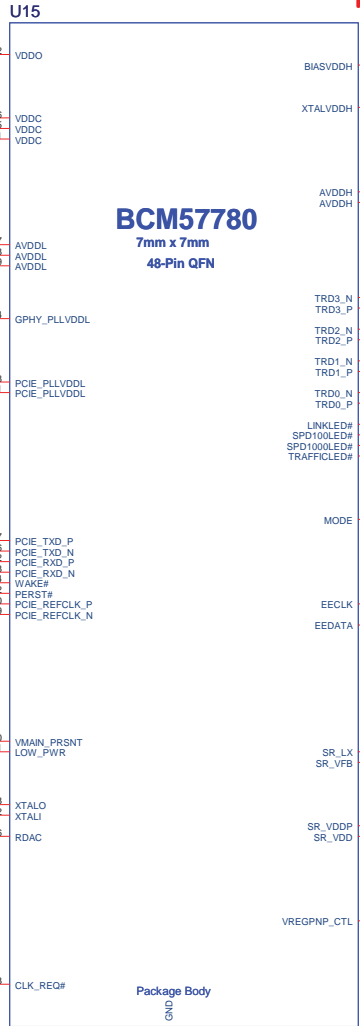
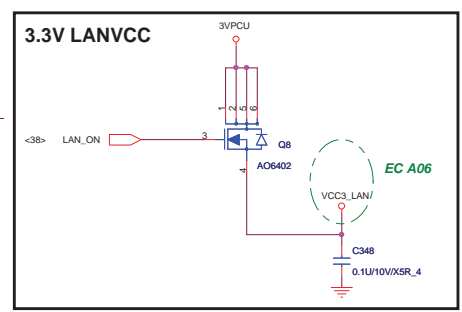
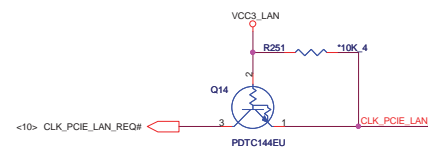
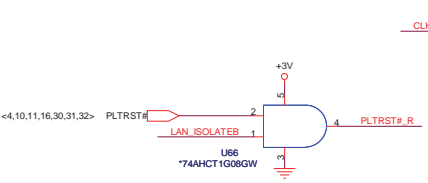
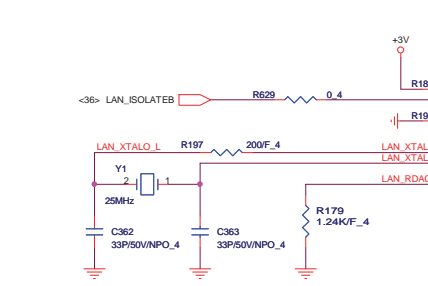
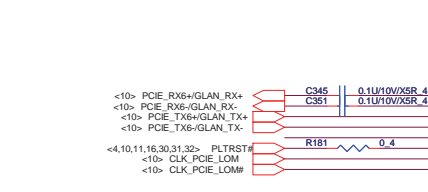
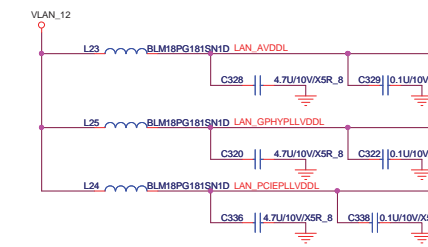
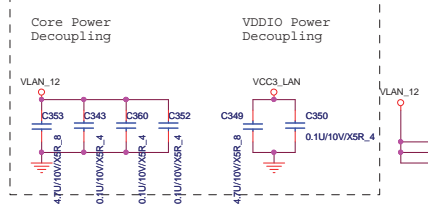


Layout Note:
Setting R,G,B trace impedance to 50 ohm.

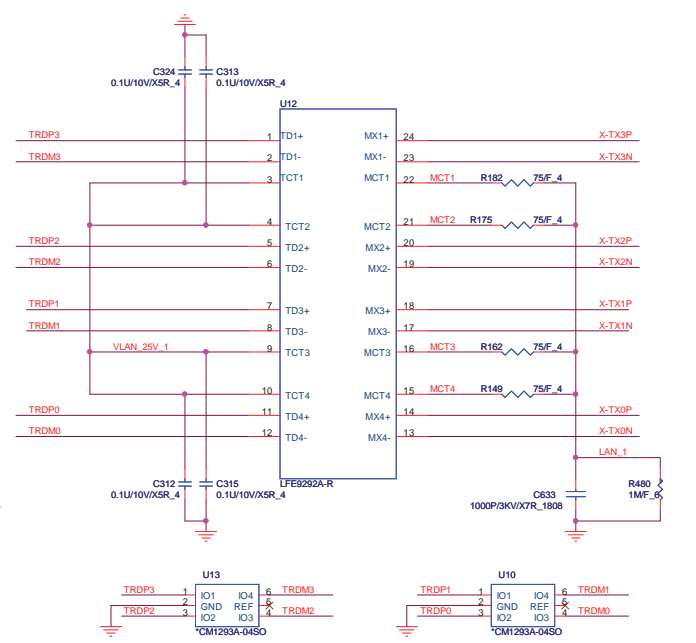


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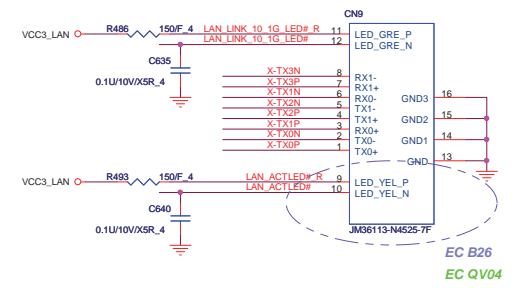
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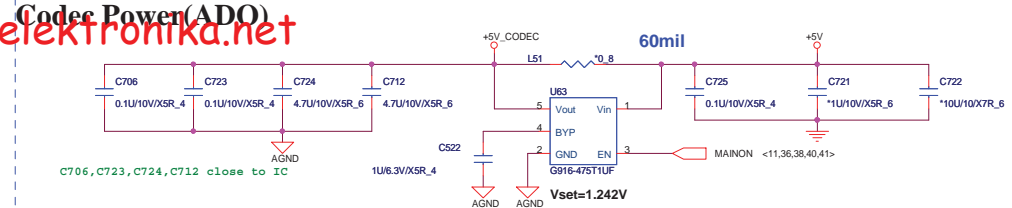
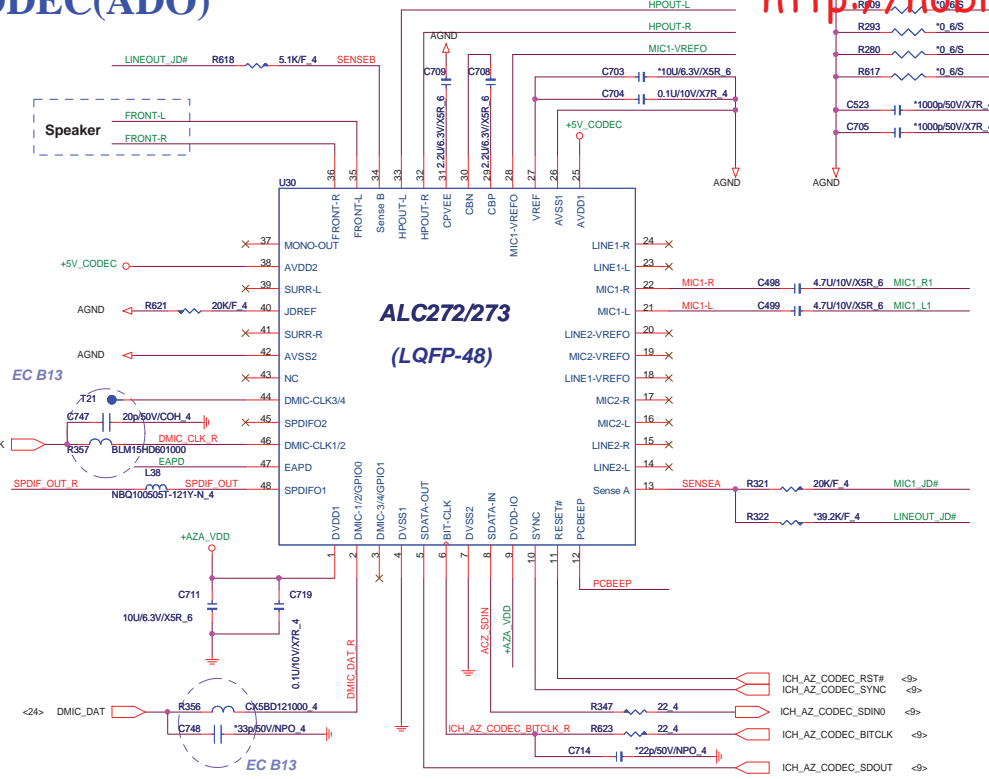


Transformer

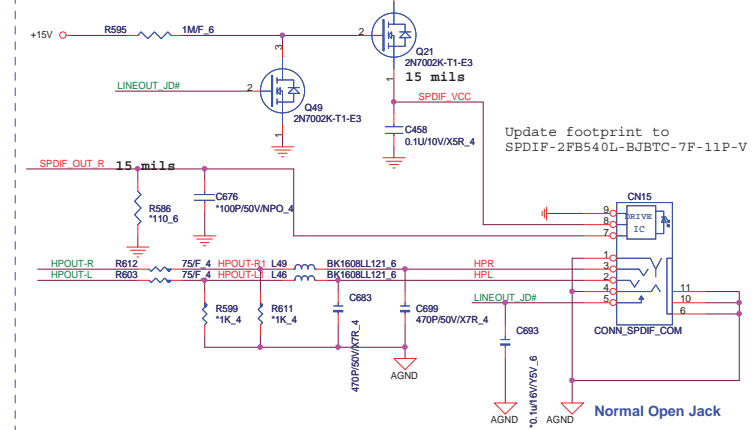


RJ45 Connector

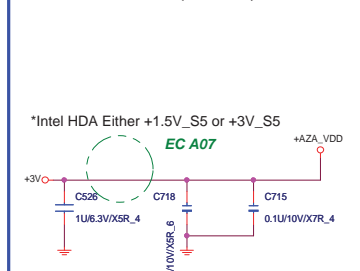




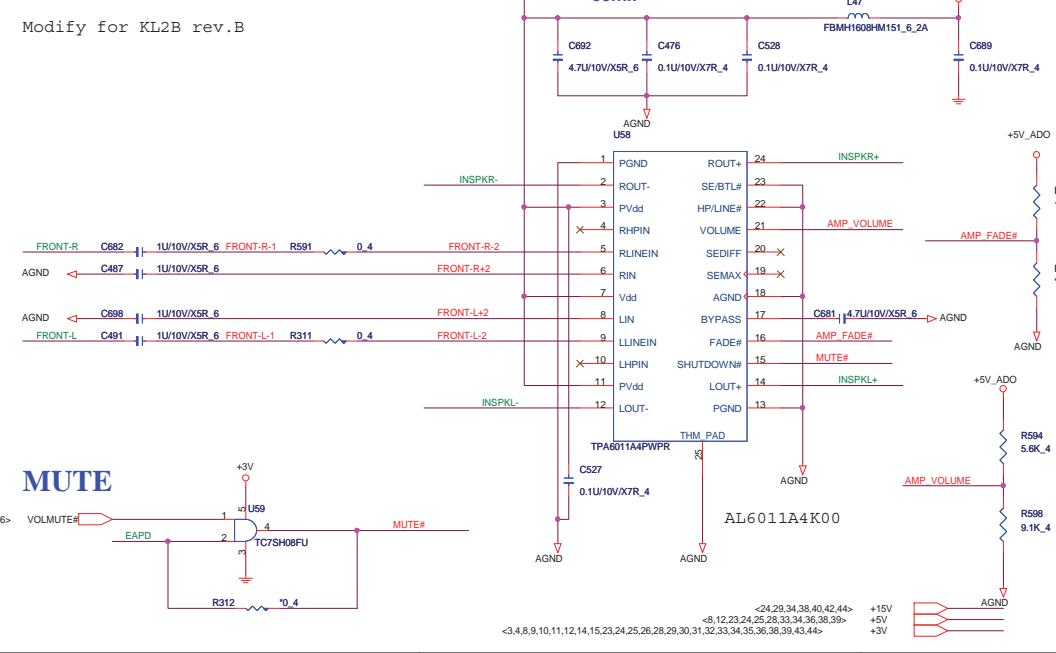
Earphone(AMP)



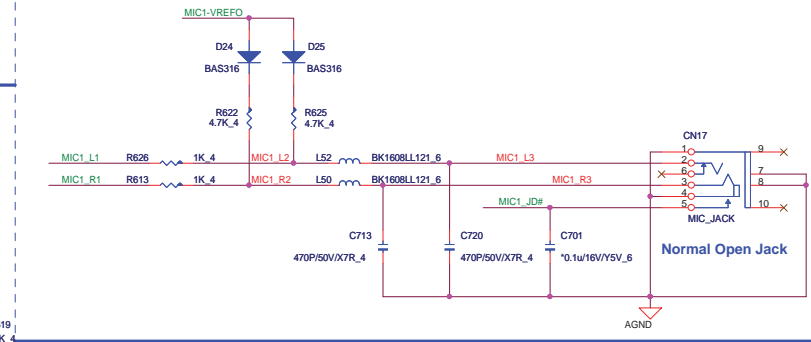
HDA Power(ADO)



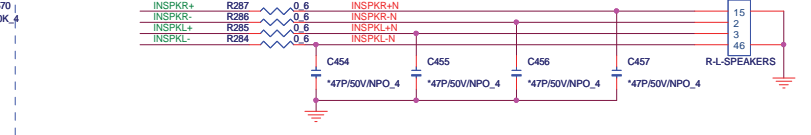
Speaker Amplifier(AMP)



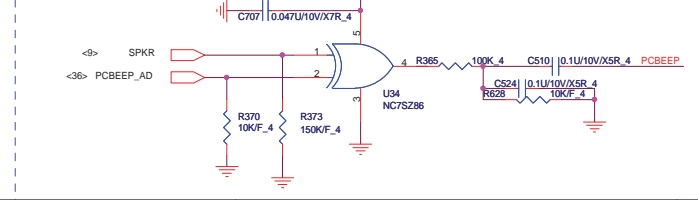
System MIC(AMP)



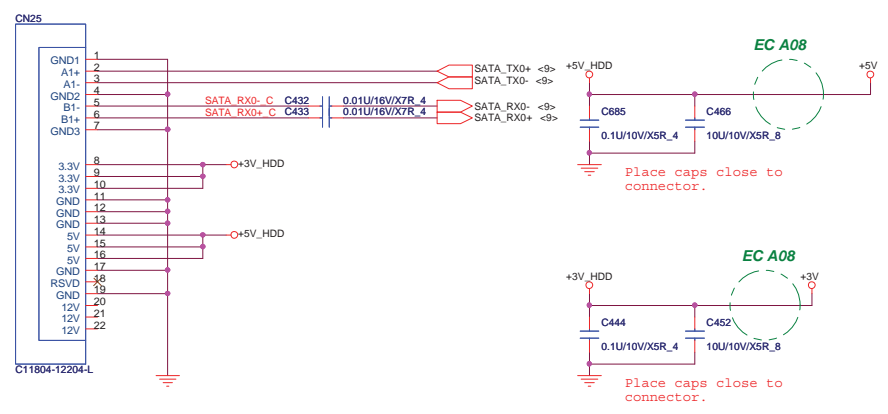
Speaker(AMP)



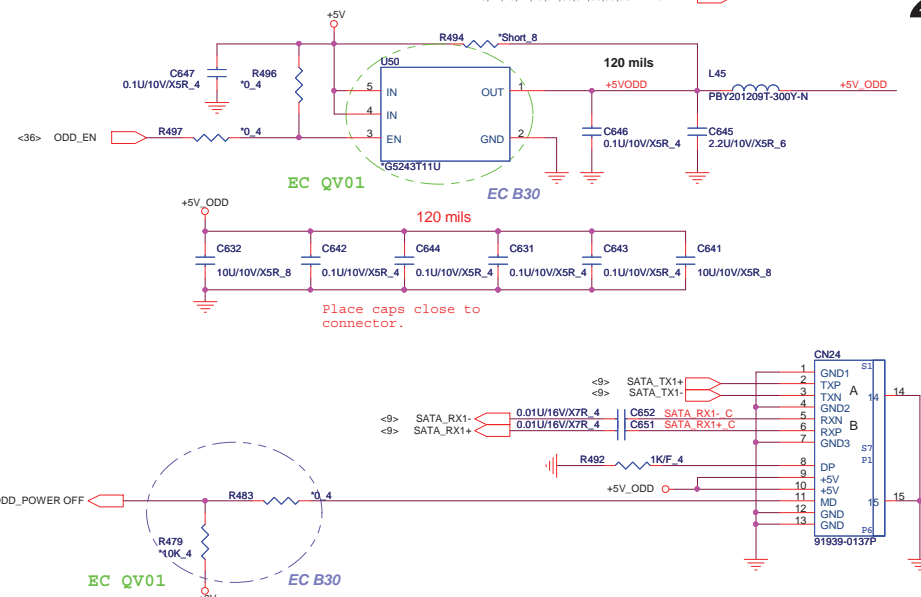
PC BEEP



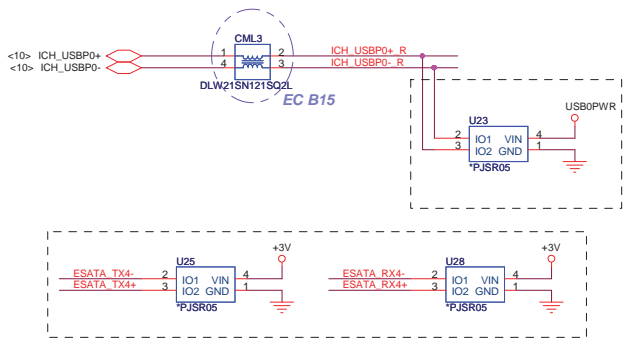
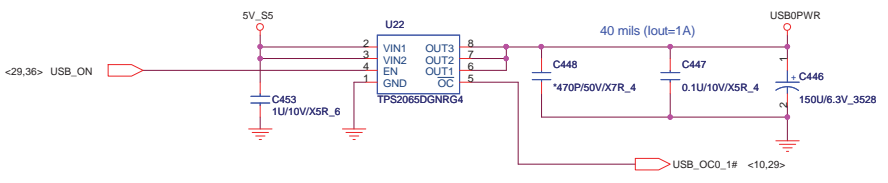
SATA HDD Connector.



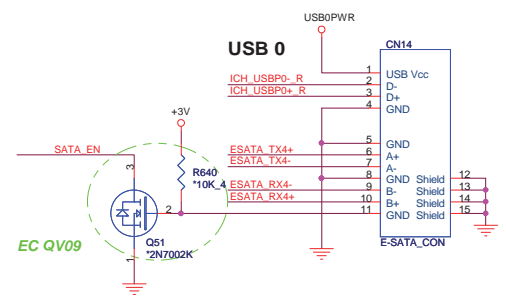
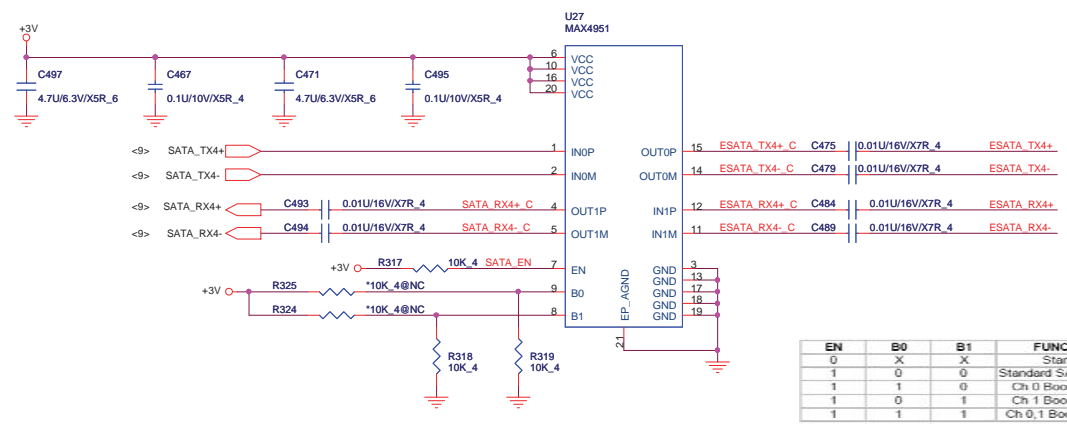
SATA ODD Connector



USB + E-SATA

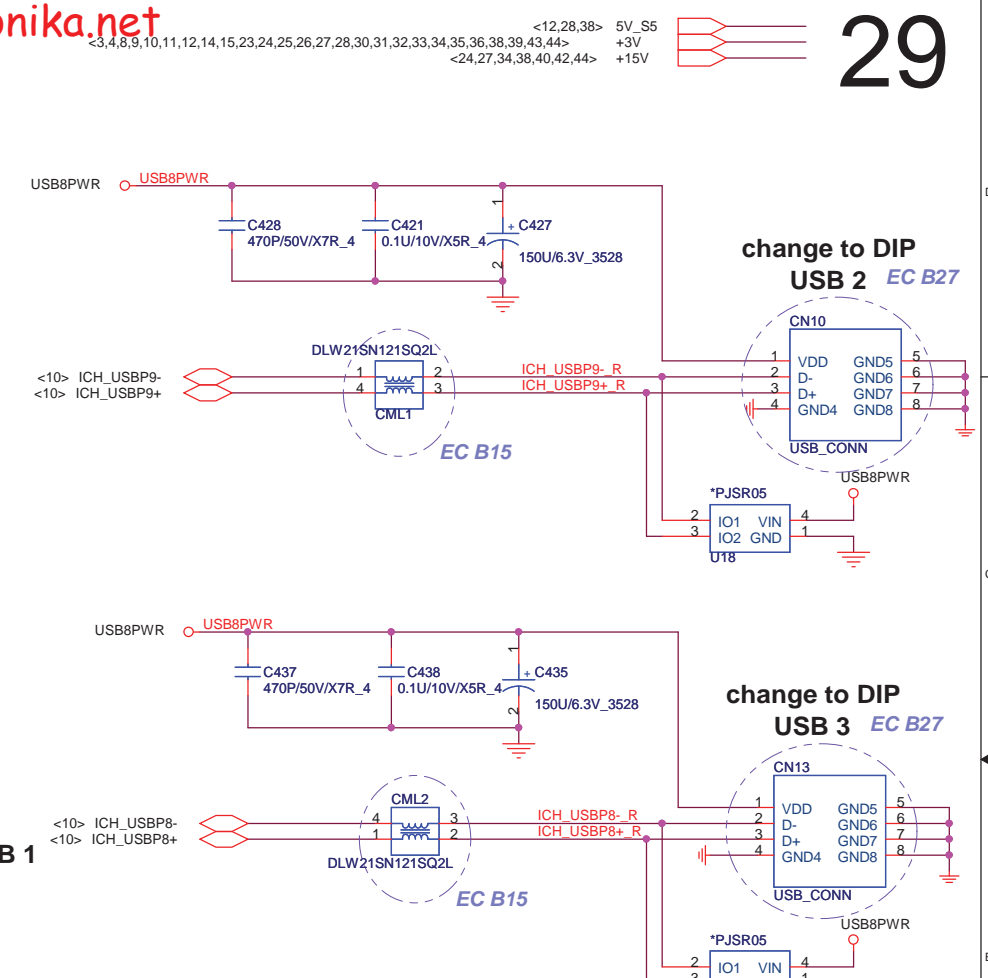
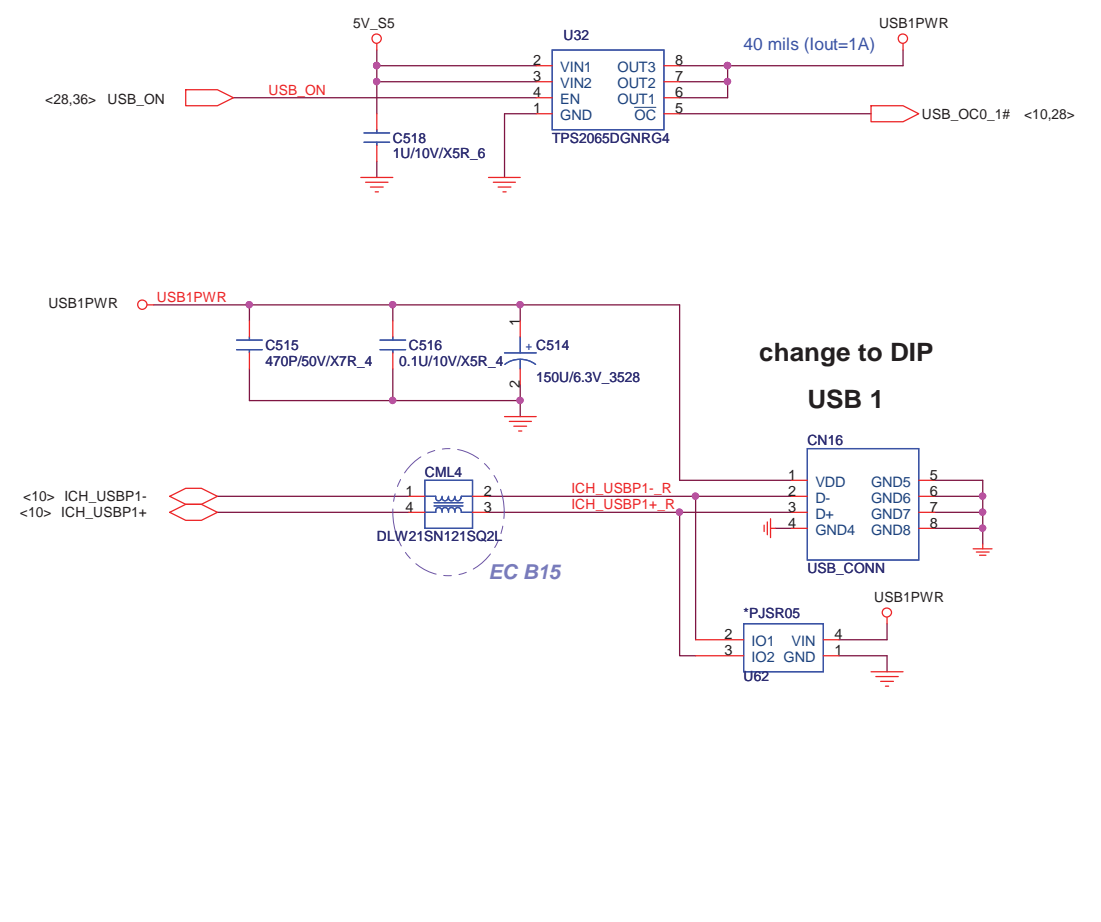


E-SATA RE-DRIVER

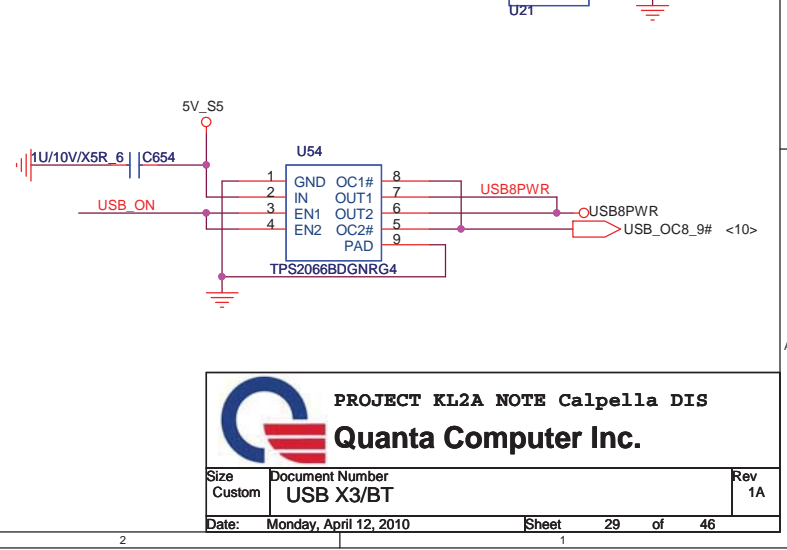
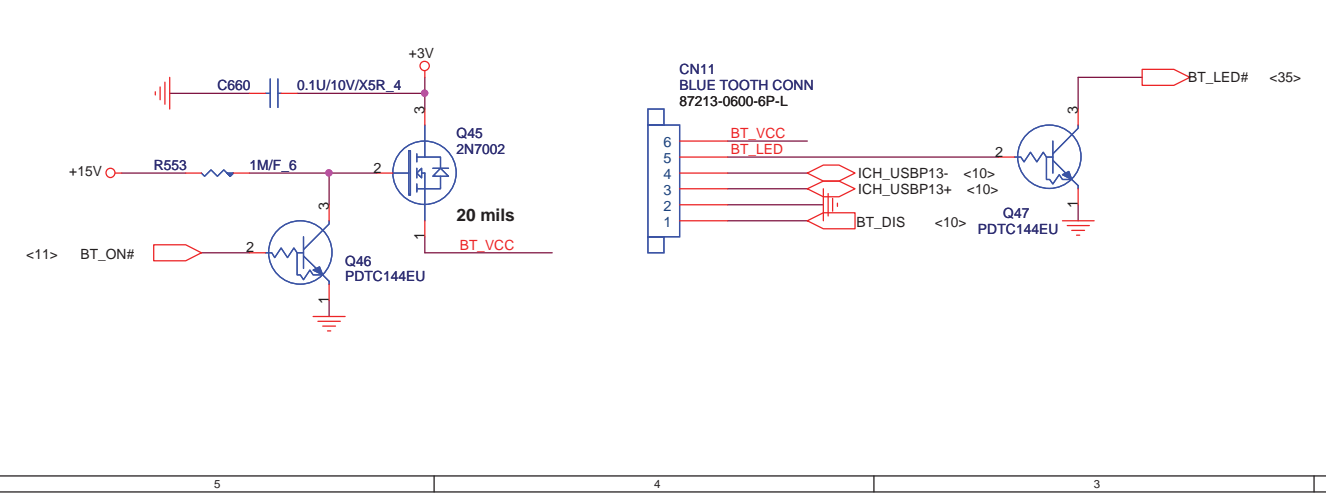


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

USB3

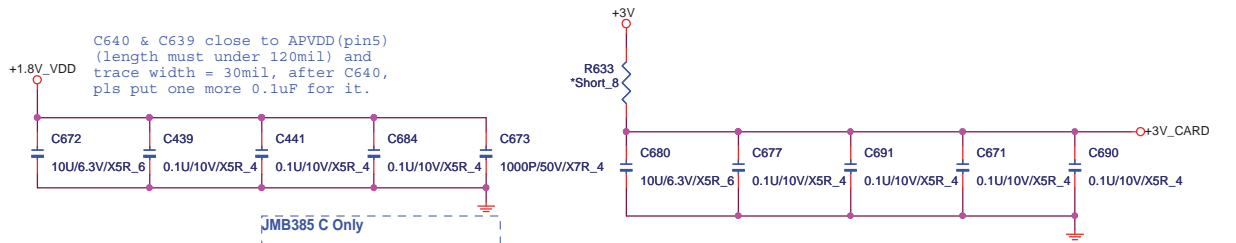


BLUETOOTH

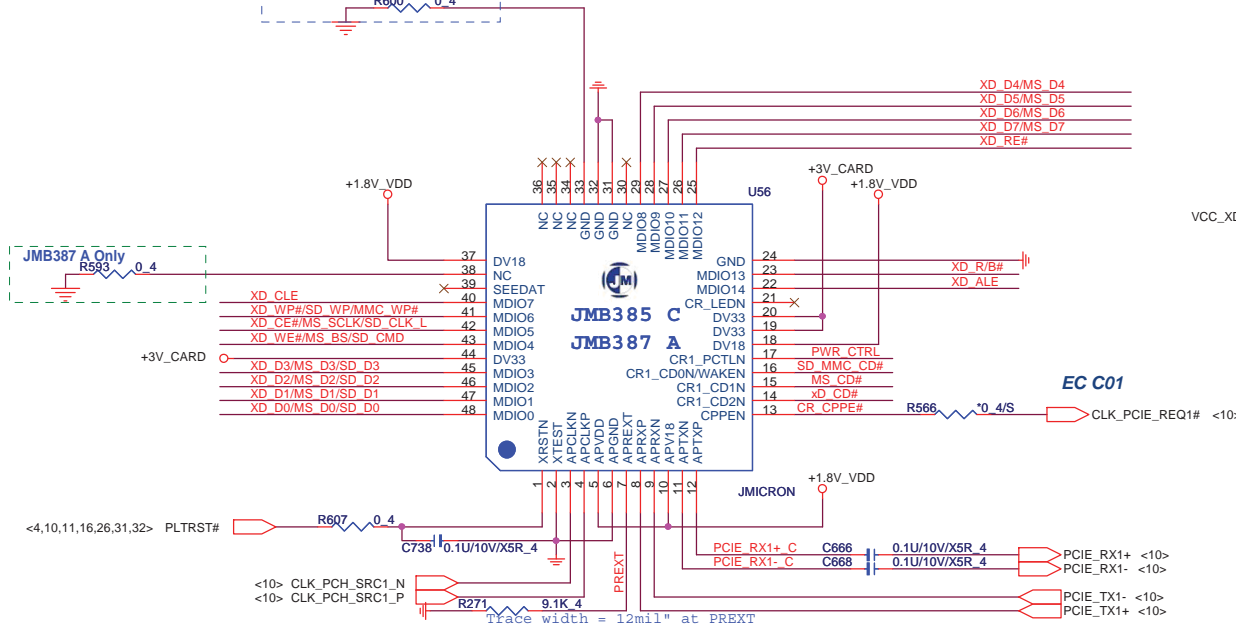
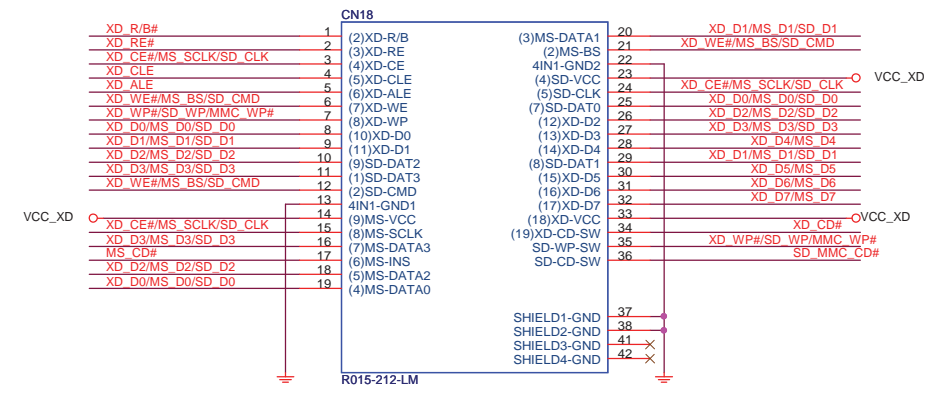


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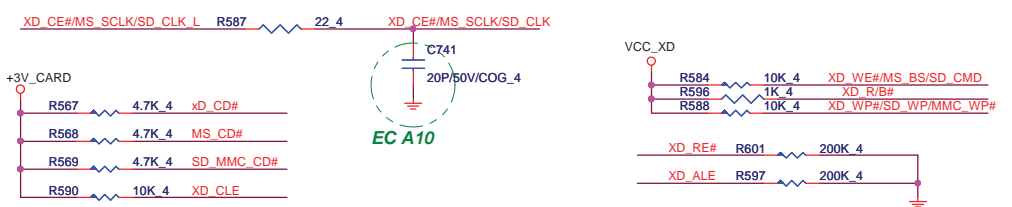
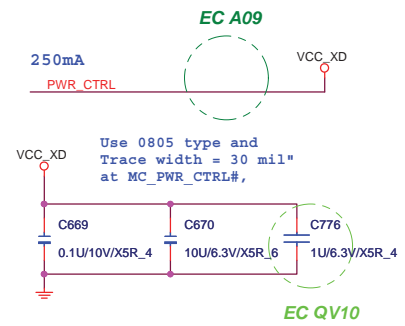
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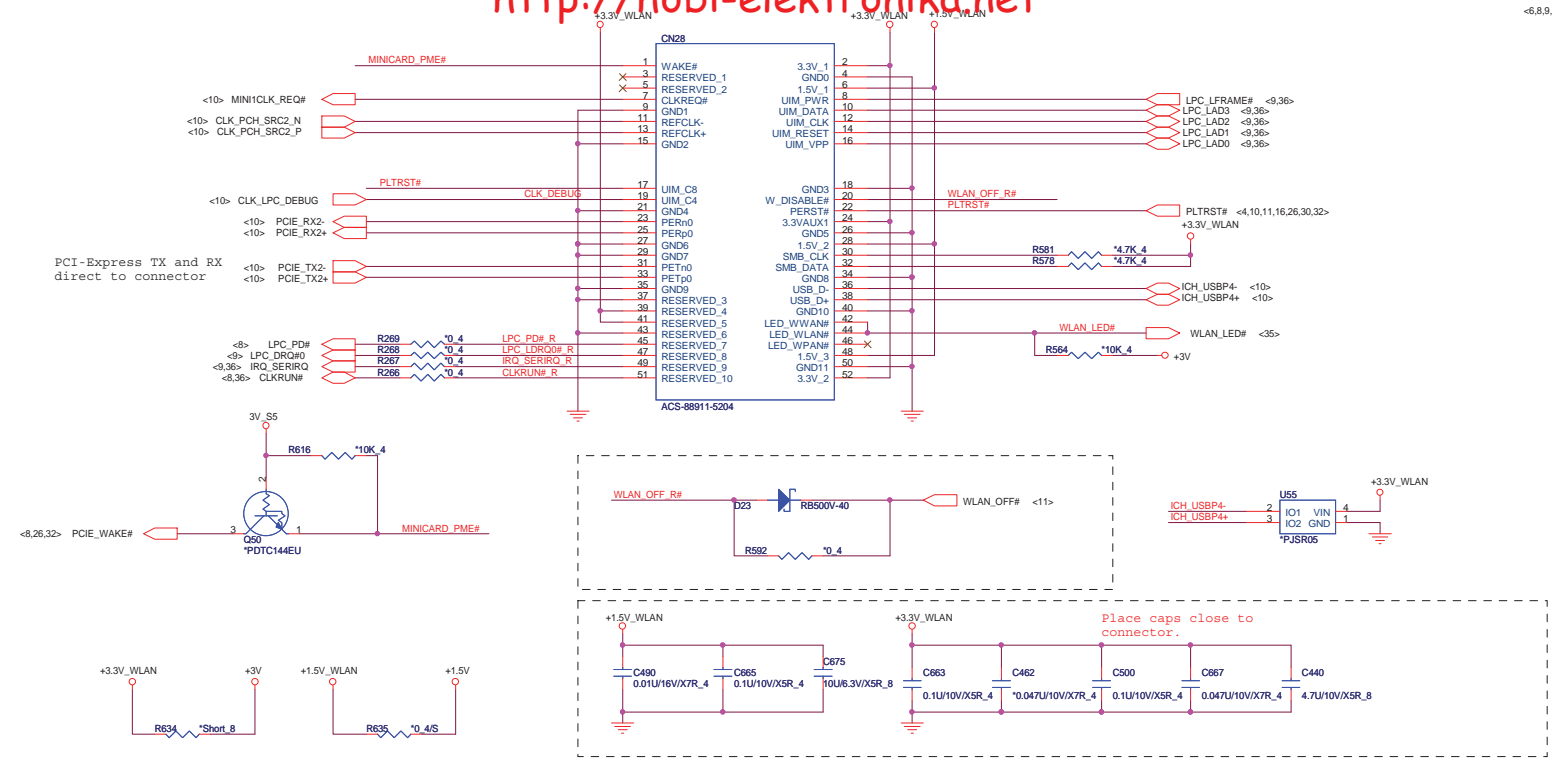


7 IN 1 CARD READER

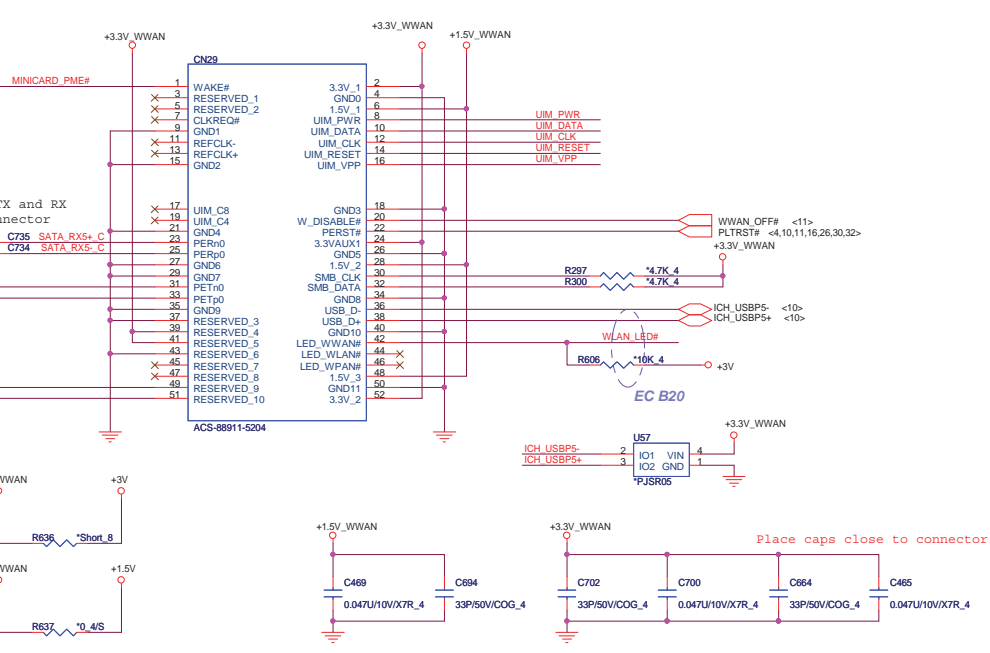


Memory Card Power Supply

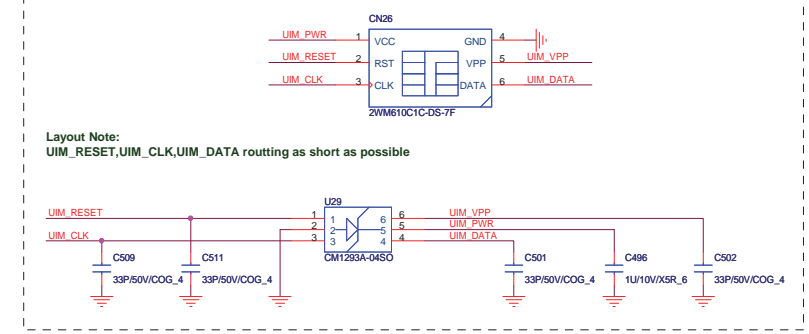




MiniCard WWAN/SATA SSD connector

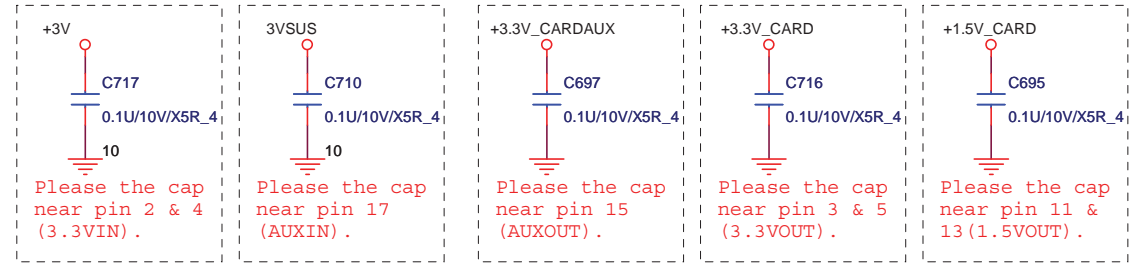
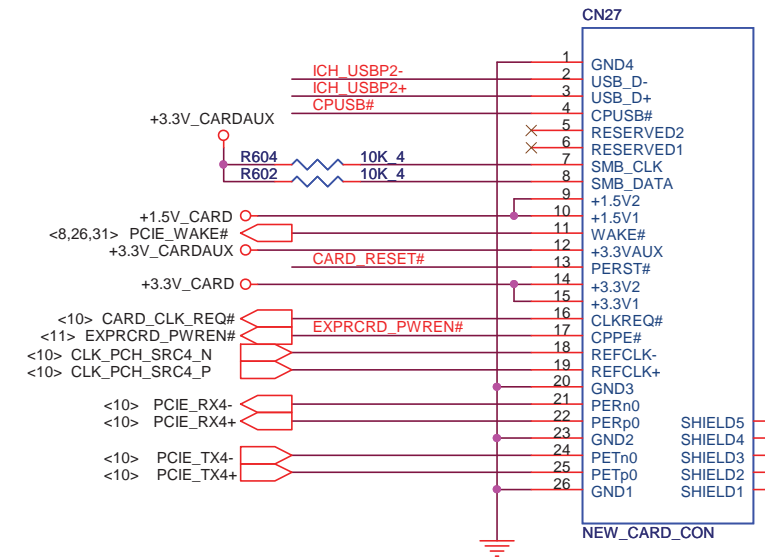
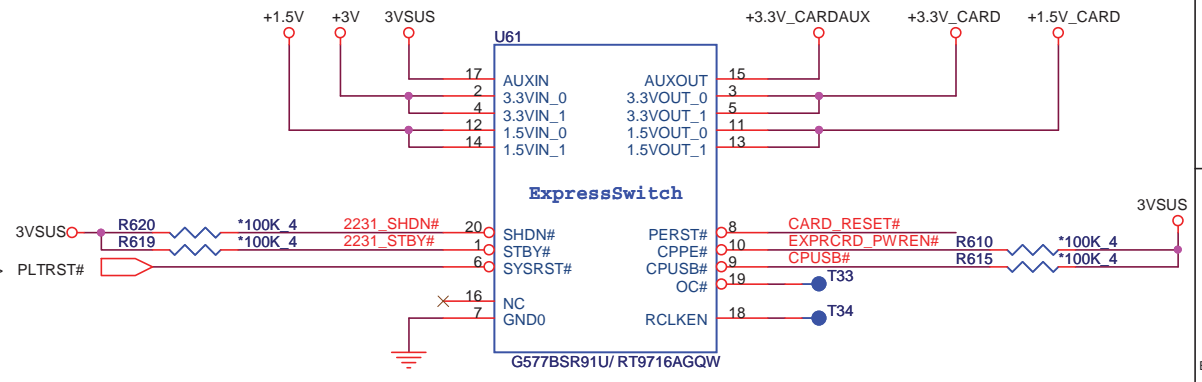
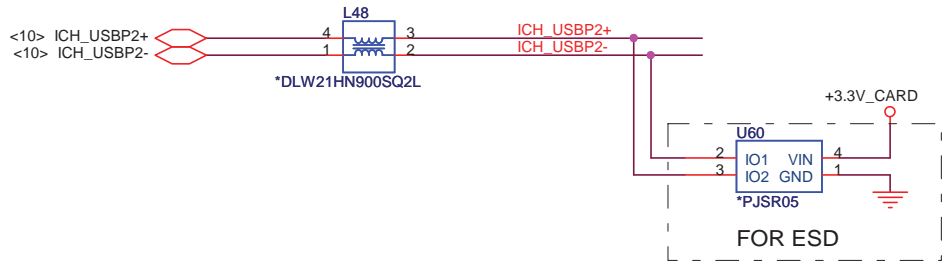


SIM Card CONN



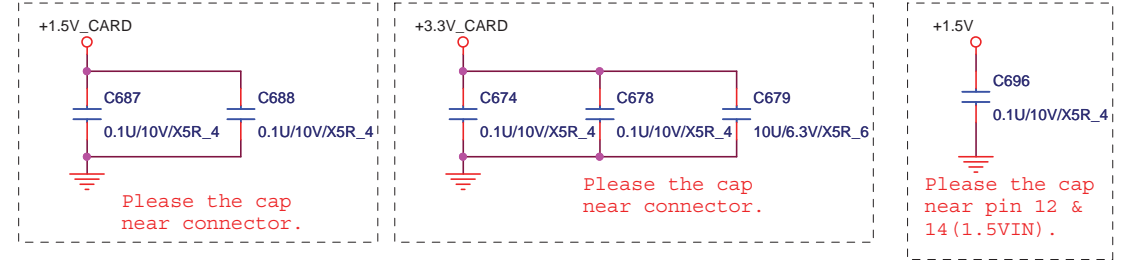


+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector.

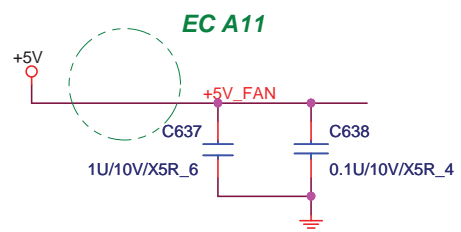
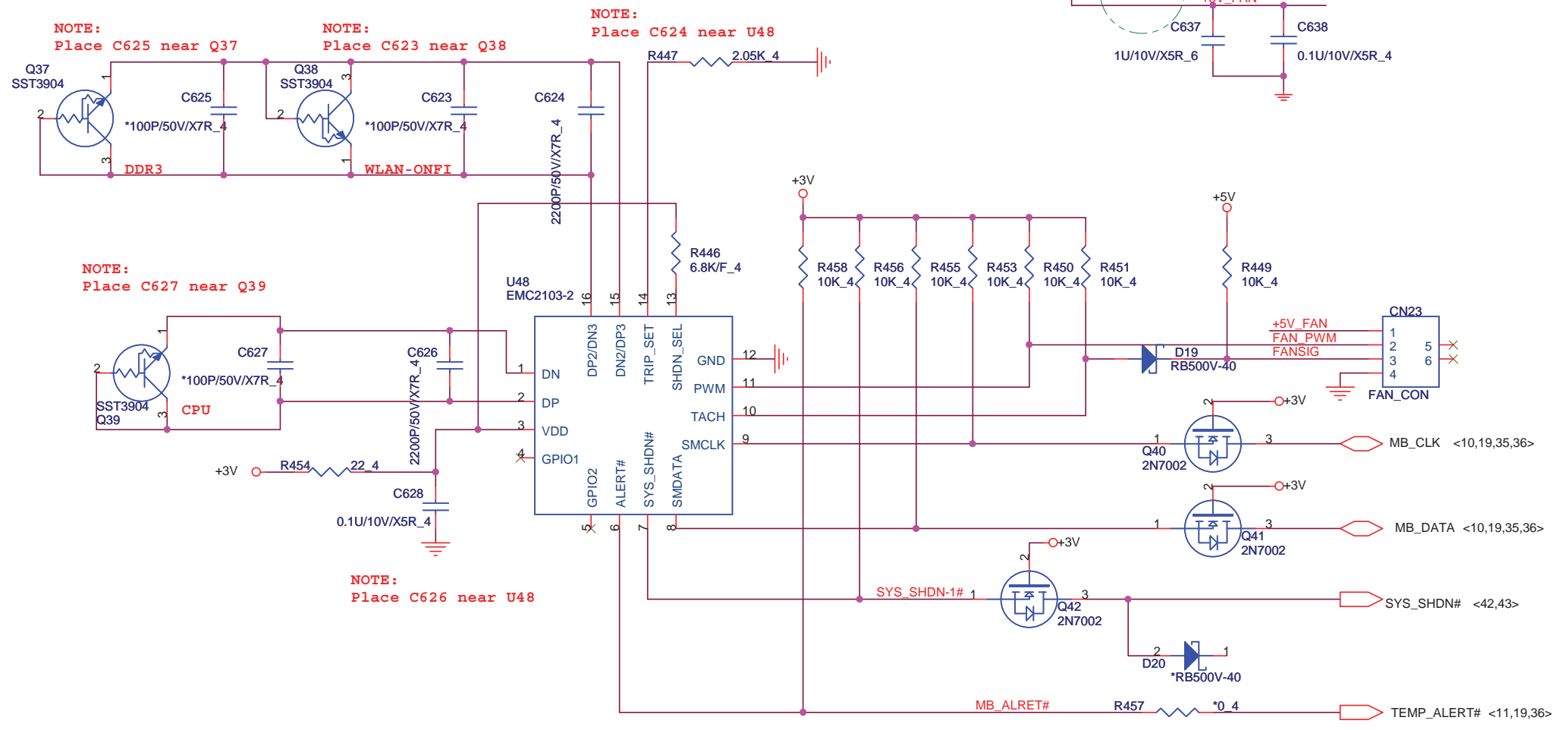
JAE PX10FS16PH-26P



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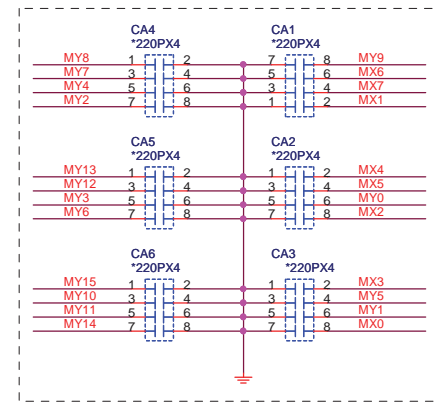
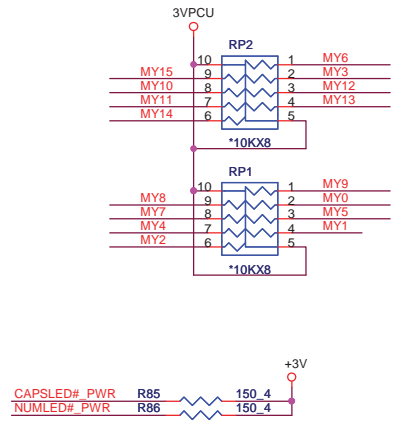
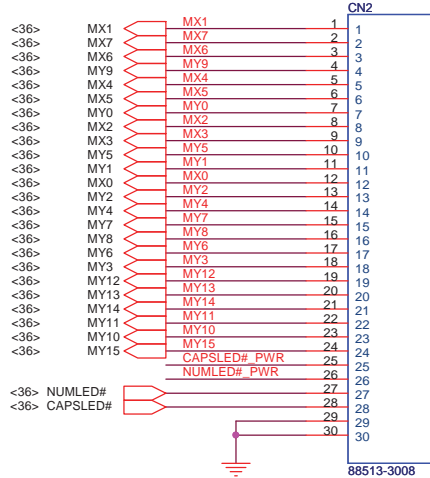
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FAN CONTROL



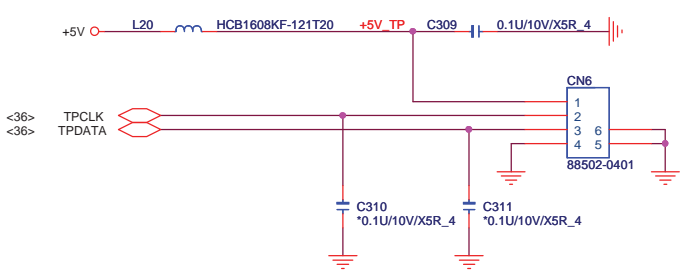
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Quanta Computer Inc.

Size Custom	Document Number FAN / THERMAL	Rev 2A
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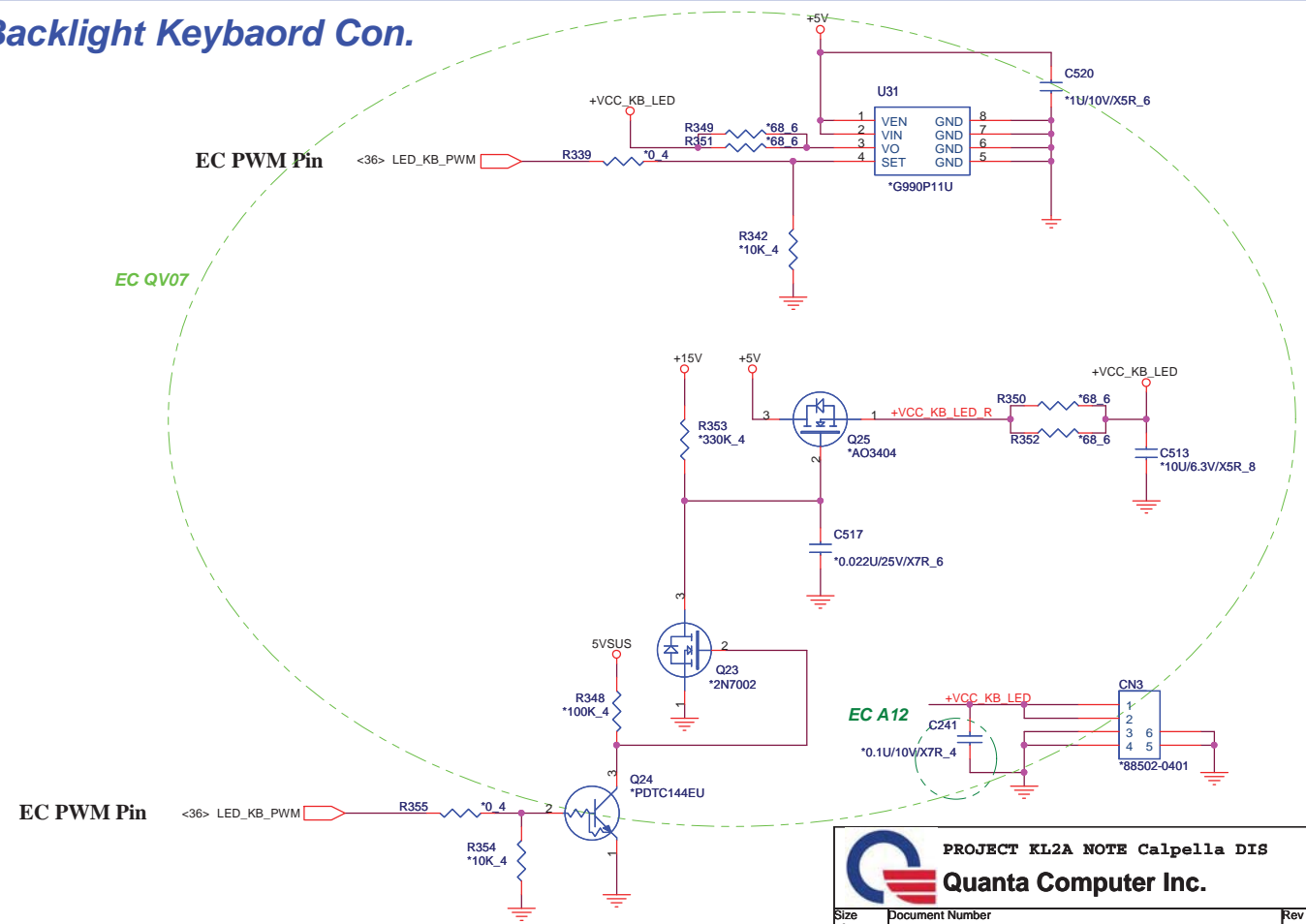


For EMI request

Touch pad



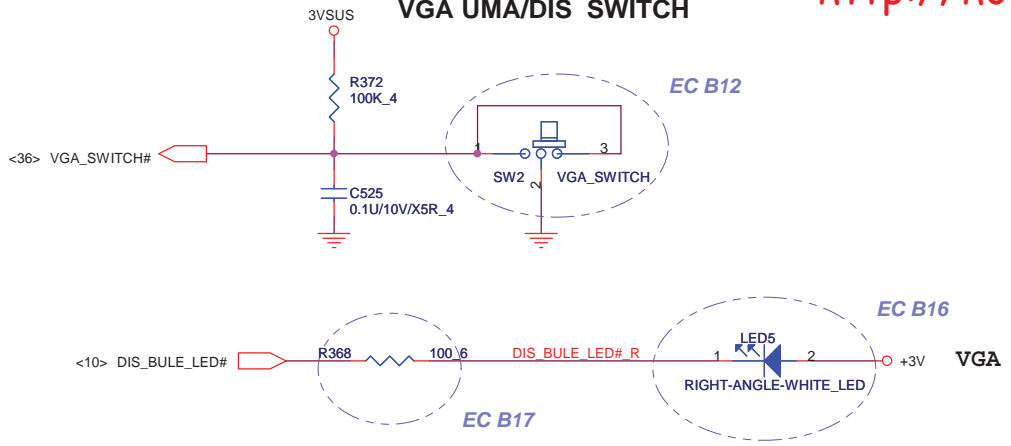
Backlight Keyboard Con.



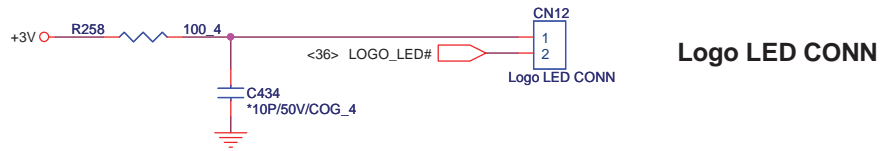
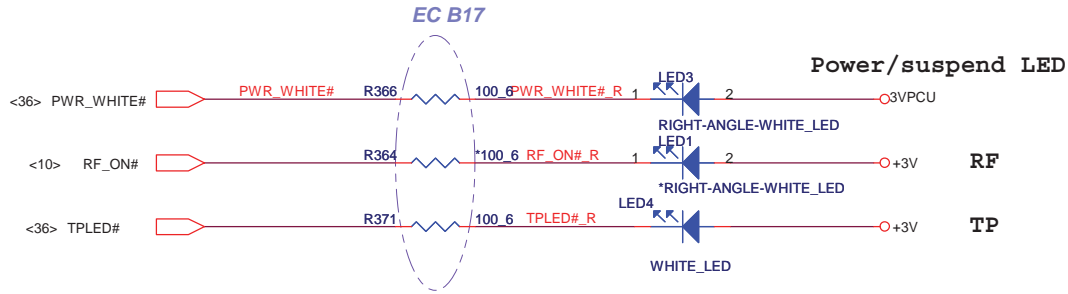
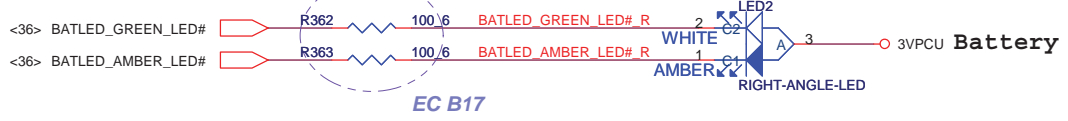
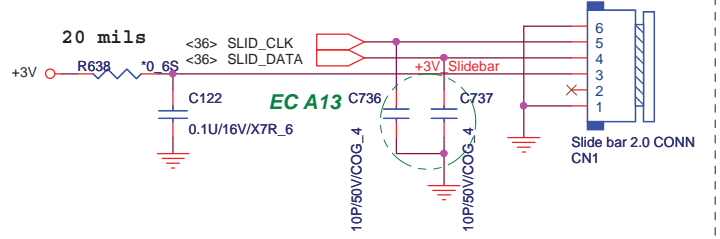
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Quanta Computer Inc.

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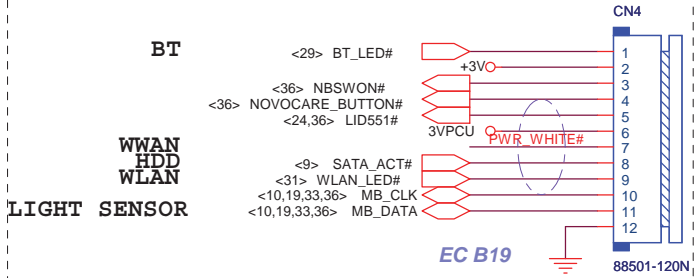
VGA UMA/DIS SWITCH

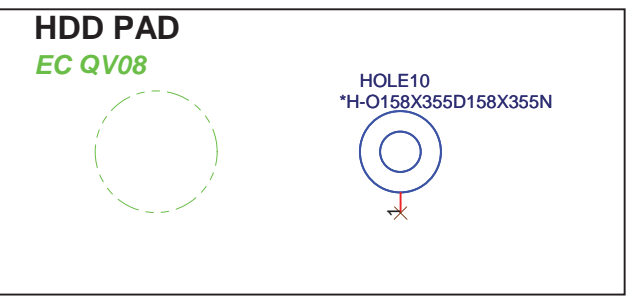
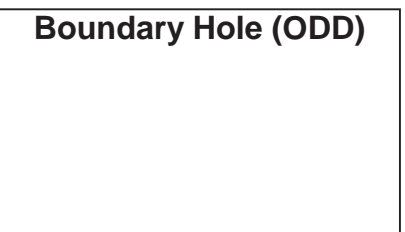
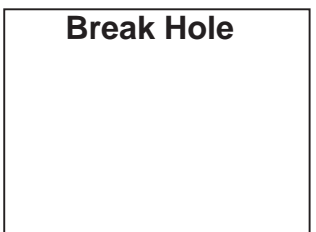
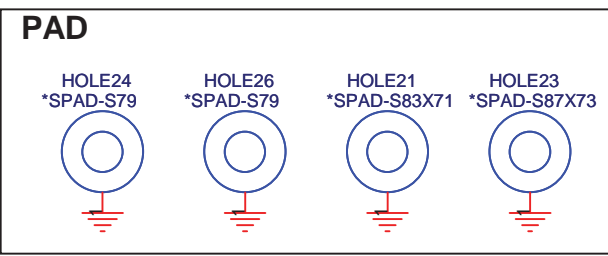
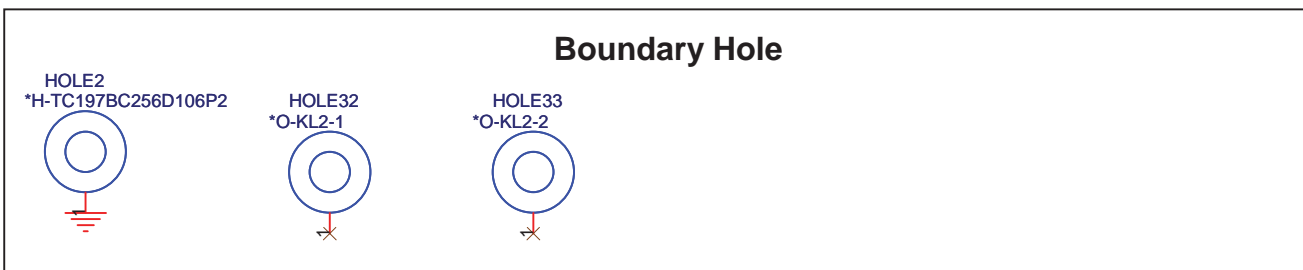
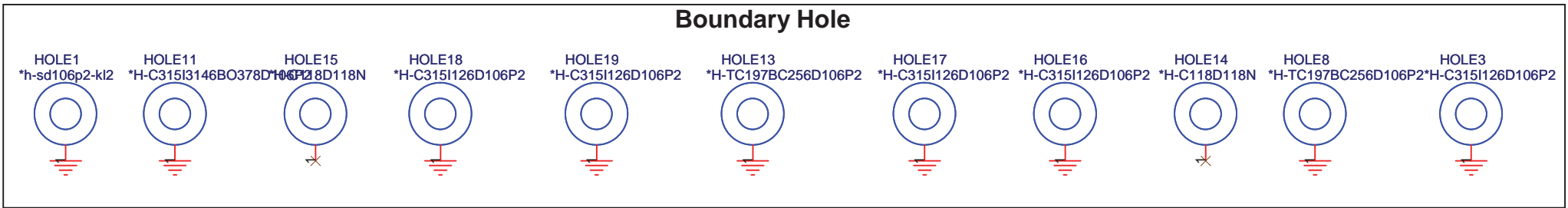
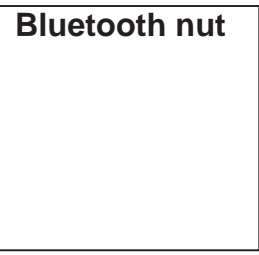
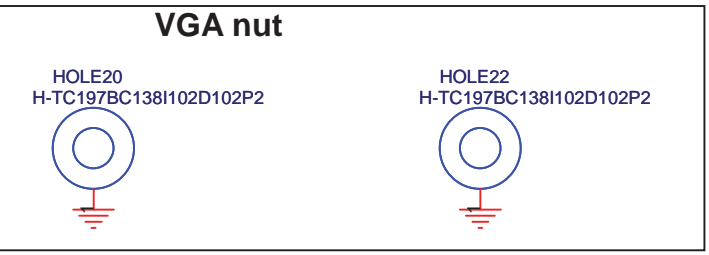
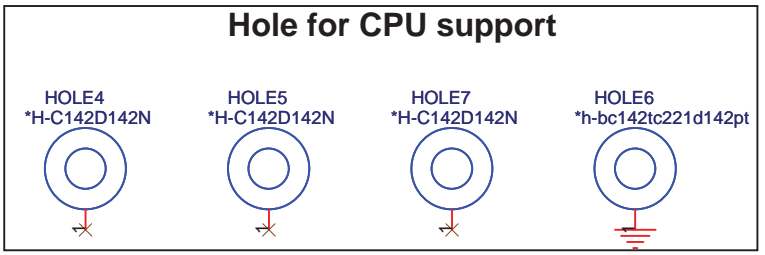
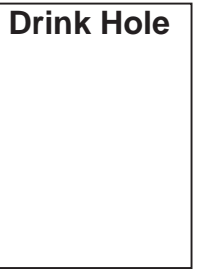
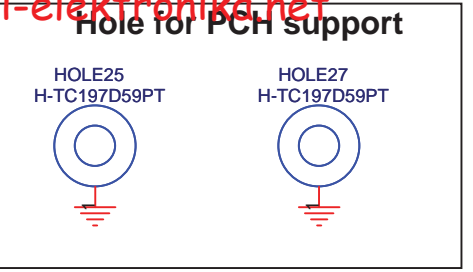
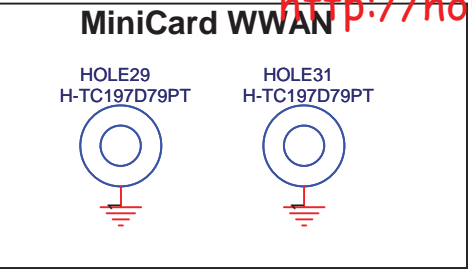
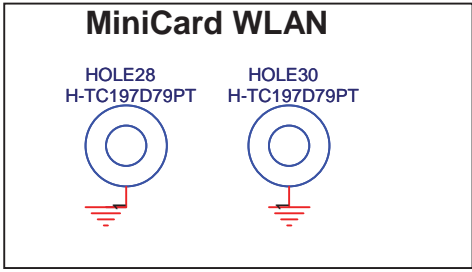


Slide bar 2.0



POWER BOARD





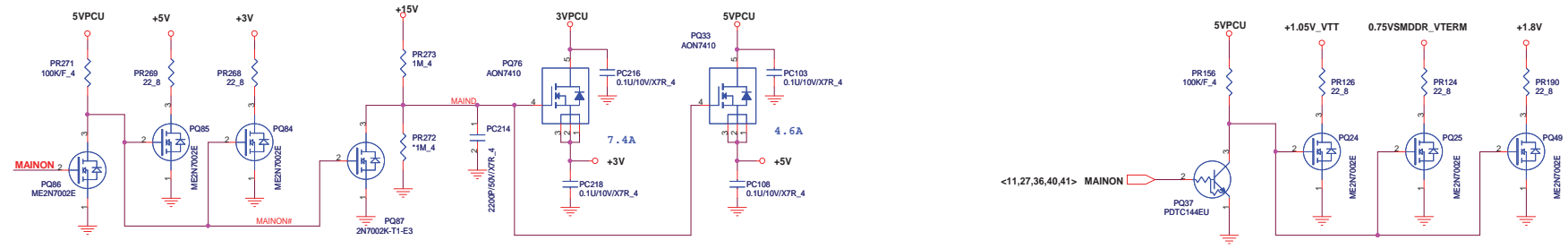
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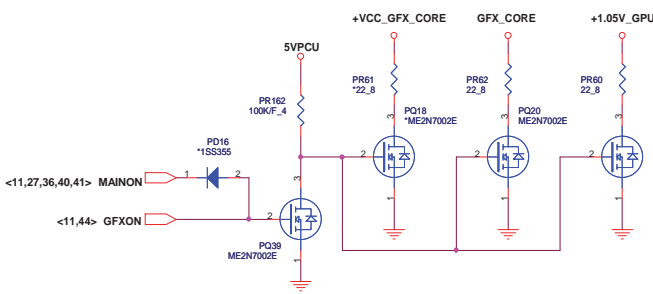
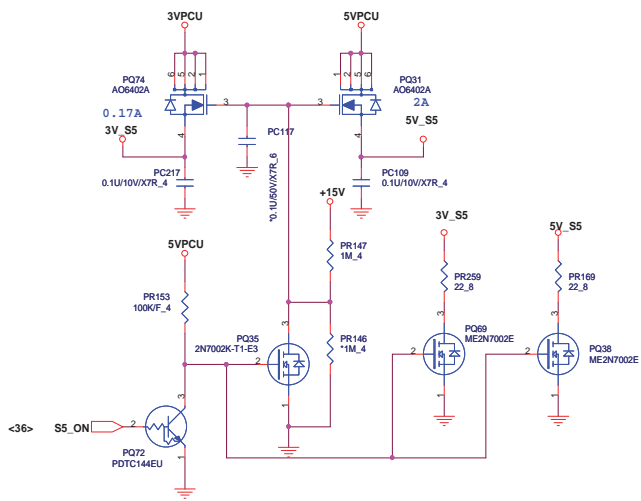
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DISCHARGE

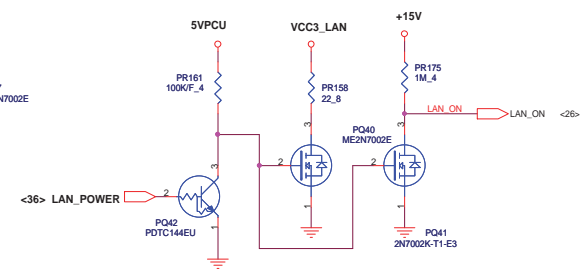
+3V, +5V



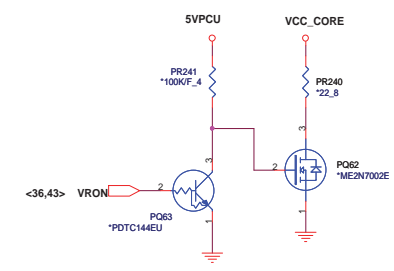
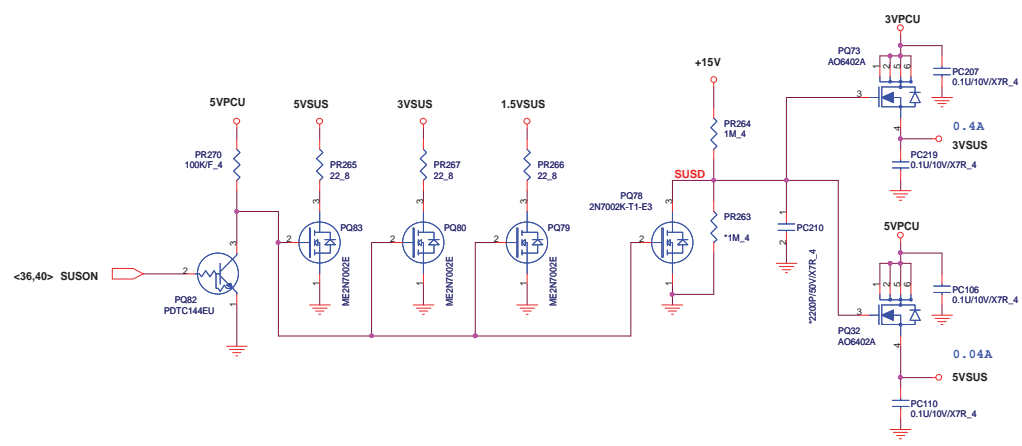
3V_S5, 5V_S5

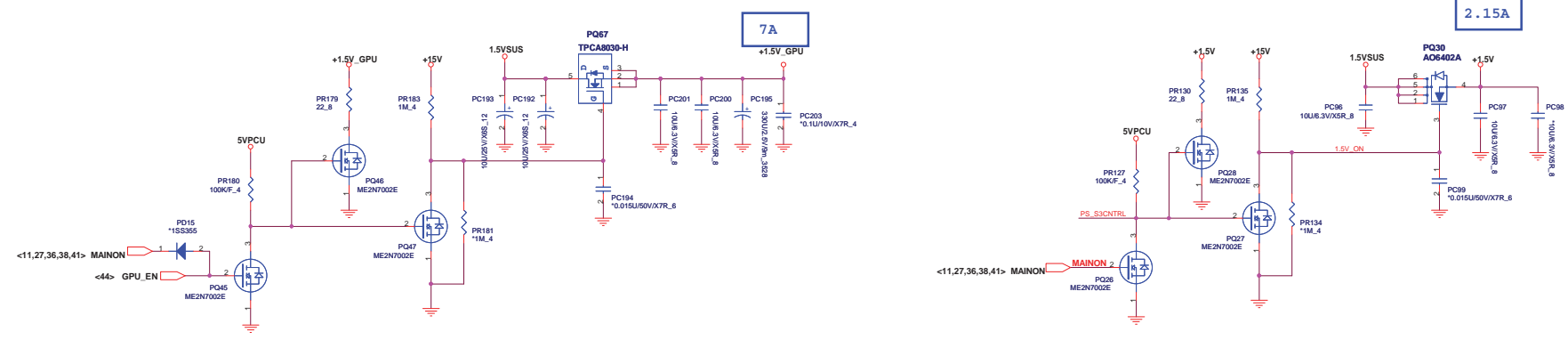
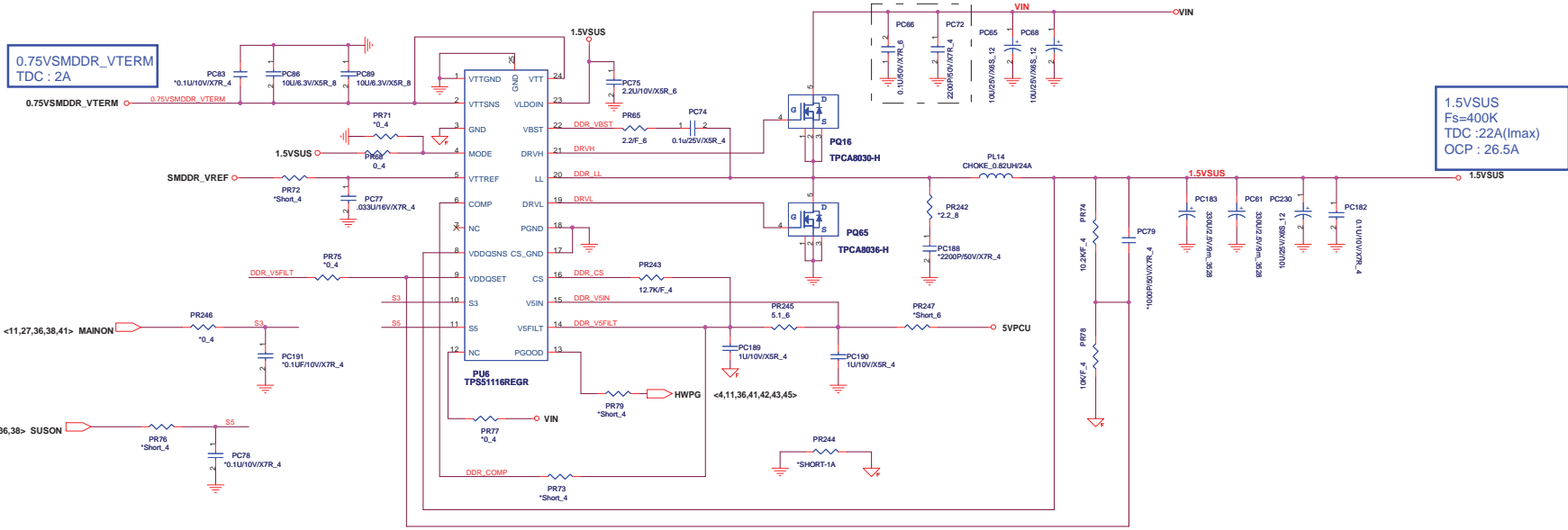


LANVCC

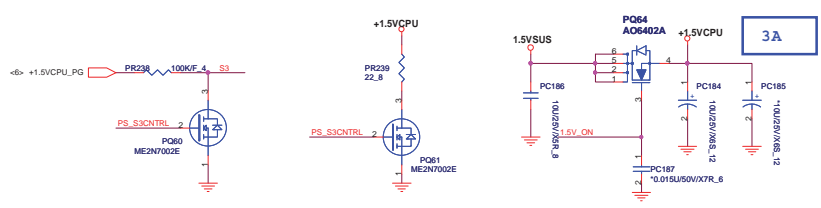


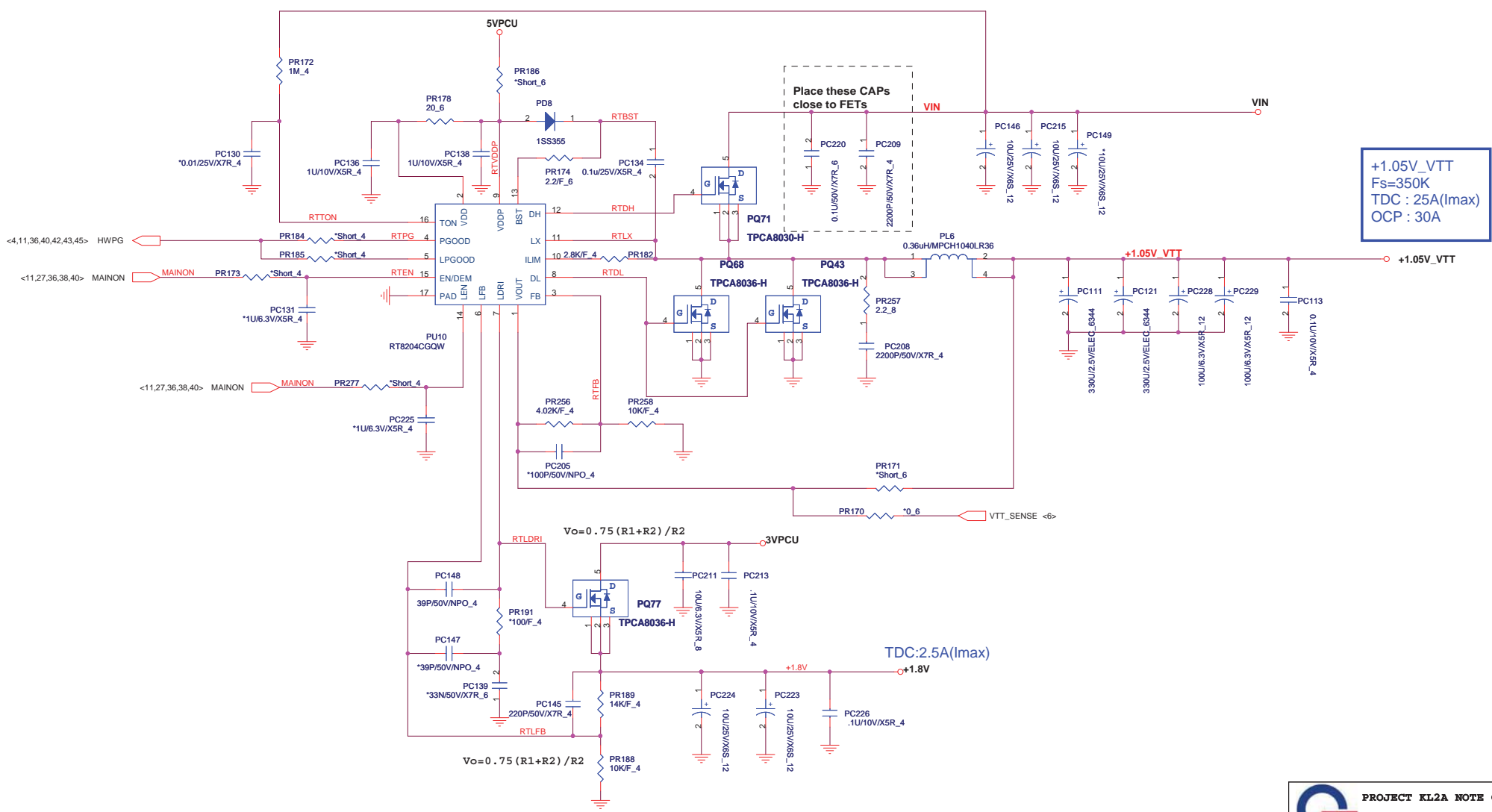
3VSUS, 5VSUS



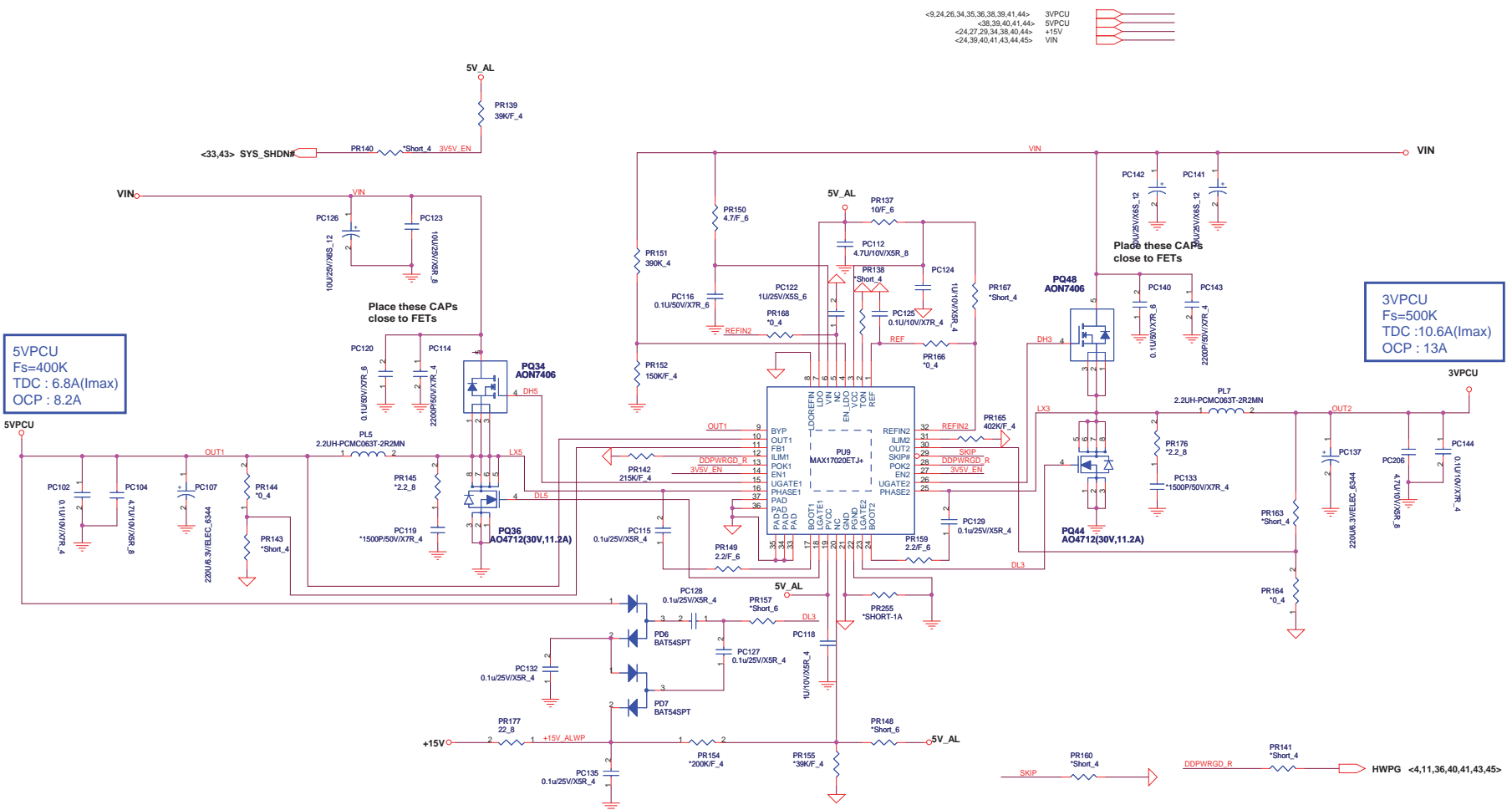


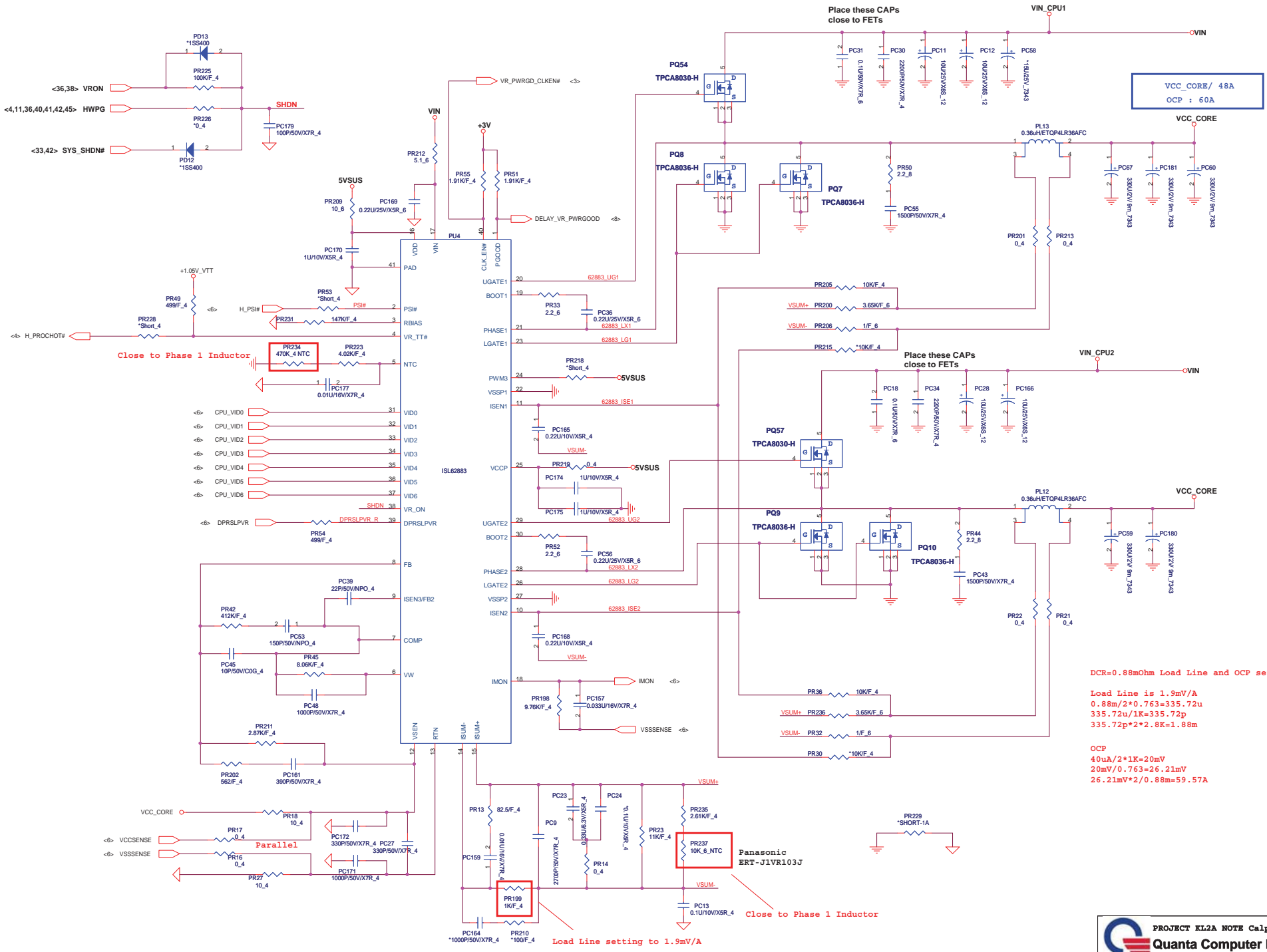
For S3 Power Saving





+1.05V_VTT
 Fs=350K
 TDC : 25A(Imax)
 OCP : 30A





VCC_CORE/ 48A
OCP : 60A

DCR=0.88mOhm Load Line and OCP setting

Load Line is 1.9mV/A
 $0.88m/2 + 0.763 = 335.72\mu$
 $335.72\mu/1K = 335.72p$
 $335.72p * 2.8K = 1.88m$

OCP
 $40\mu A / 2 * 1K = 20mV$
 $20mV / 0.763 = 26.21mV$
 $26.21mV * 2 / 0.88m = 59.57A$

Load Line setting to 1.9mV/A

Close to Phase 1 Inductor

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