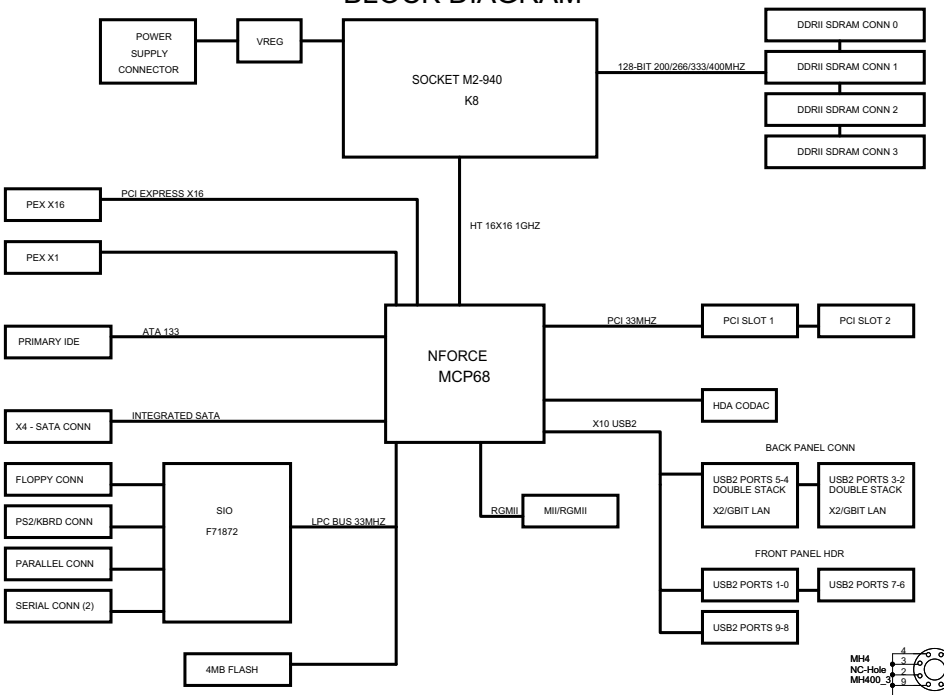
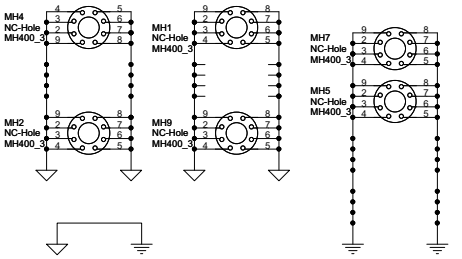
Jetway Information Co. Ltd.

Route :

1. HT_STOP- : 5mil width/5 mil space BGA breakout.
   5mil width/10 mil to CPU and other.
2. PCI Express differential signal groups :
   5 mil length matching each pair.
   Maximum mismatch between pairs is 3000 mil.
   Maximum length of any pairs is 12000 mil.
   All trace should be referenced to Ground.
   Maximum 4 vias pre TX trace. no more 2 vias pre RX trace.
3. SP_TERMP/SP_TERMN :
   Place resistor within 500 mil of MCP55.
4. IDE interface :
   60 ohm interface, routed 5 mil trace with 10 mil spacing.
   Trace length should be less then 6.5 inchs.
   P(S)IDEIORJ length within +/- 100 mil of P(S)IDERDY.
5. USB : Trace length < 12 inches (less than 8 inches desired).
6. SMBus : With termination pull-up resistors at end of the trace.
   Strongly discourage the T topology.

BLOCK DIAGRAM

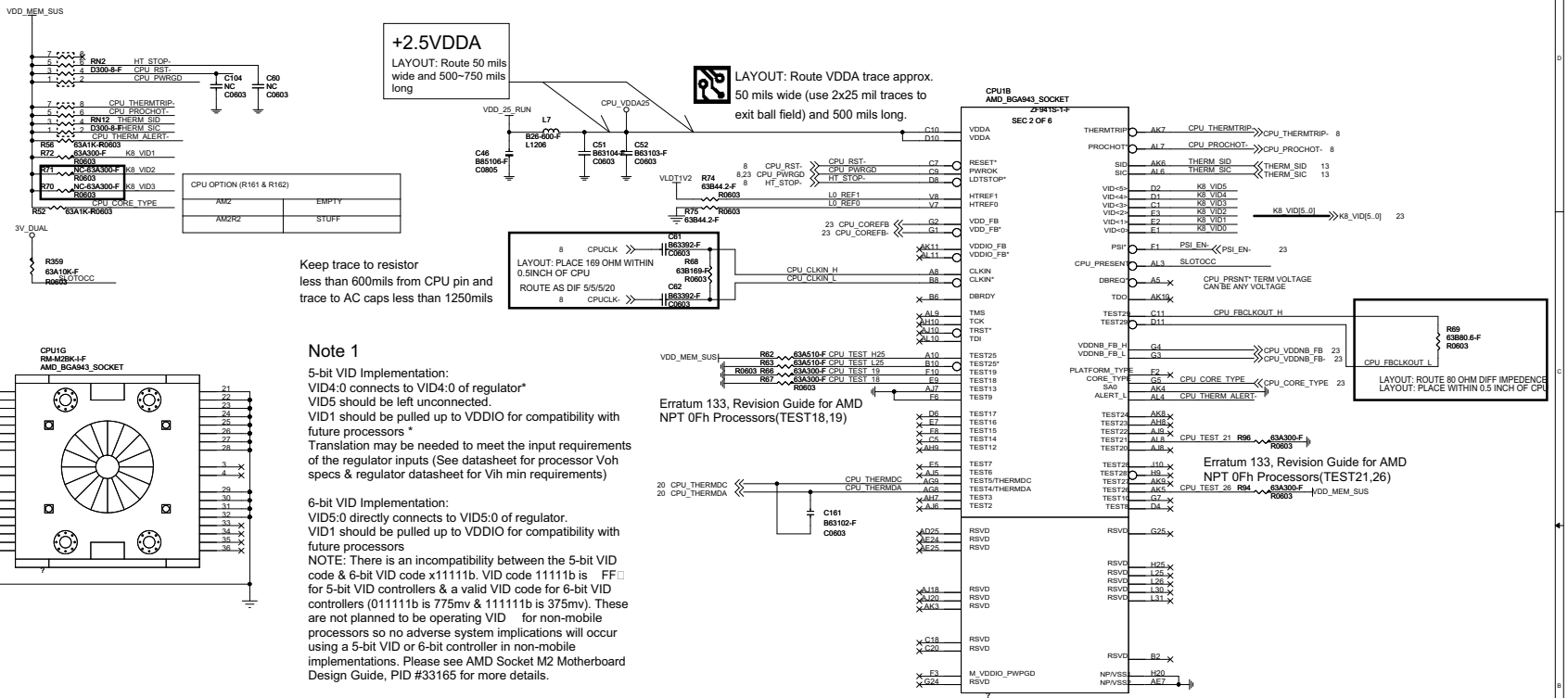


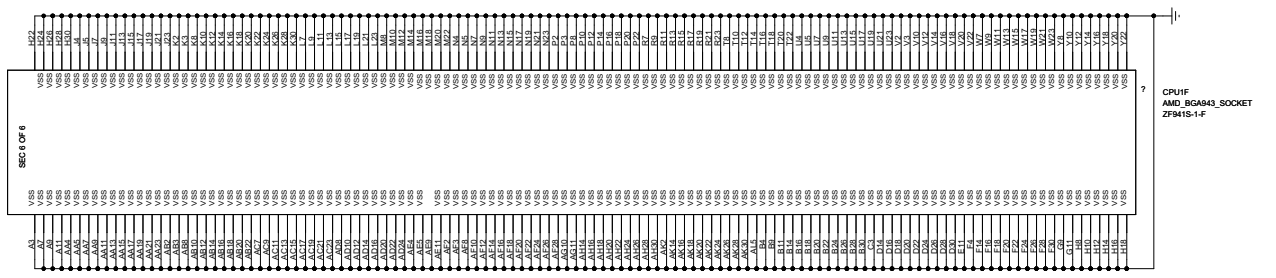


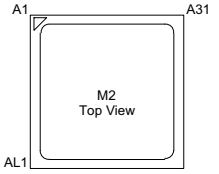
FIL1 FIL2 FIL3

JETWAY INFORMATION CO.,LTD.				
Title: COVER PAGE				
Size: E	Document Number: MCP61JTD3			Rev: 1.0
Date: Thursday, April 01, 2010		Sheet 1 of 24		

ATHLON Control and Debug





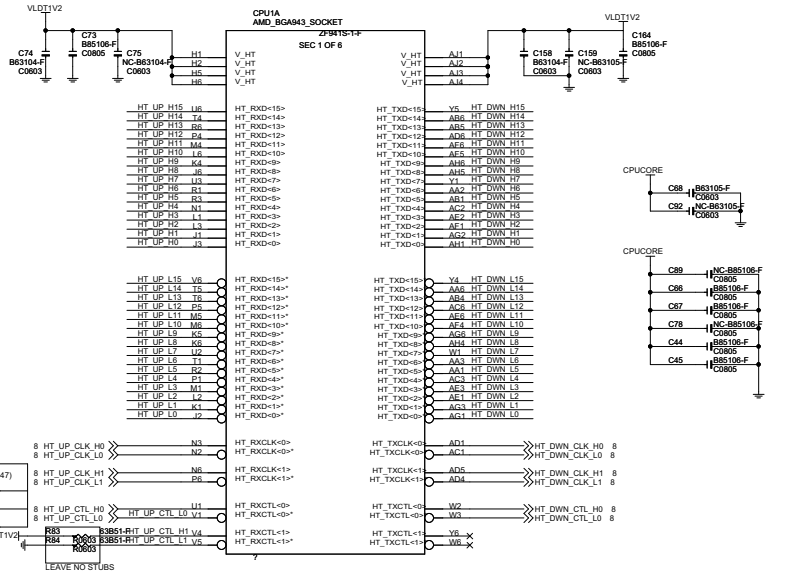


JETWAY INFORMATION CO.,LTD.			
Title: CPU_M2-940 CTRL&DEBUG			
Size: C	Document Number: MCP61JTD3		Rev: 1.0
Date: Thursday, April 01, 2010		Sheet 2 of 25	

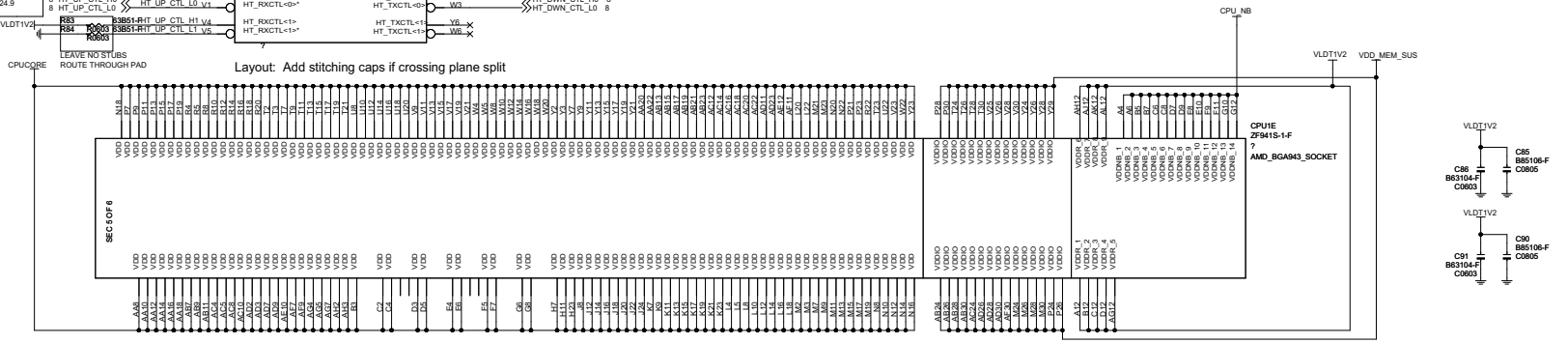
Processor Power and Ground

Processor HyperTransport Interface

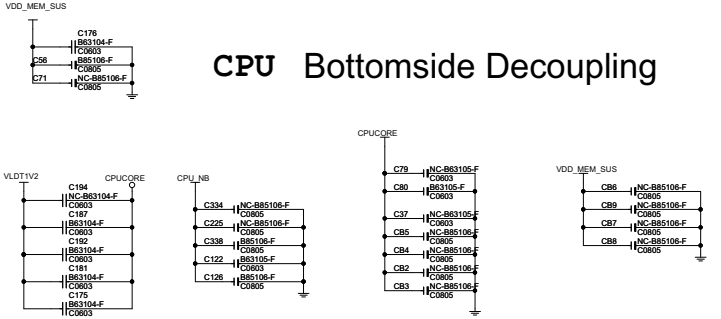
VDDLDTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



Layout: Add stitching caps if crossing plane split

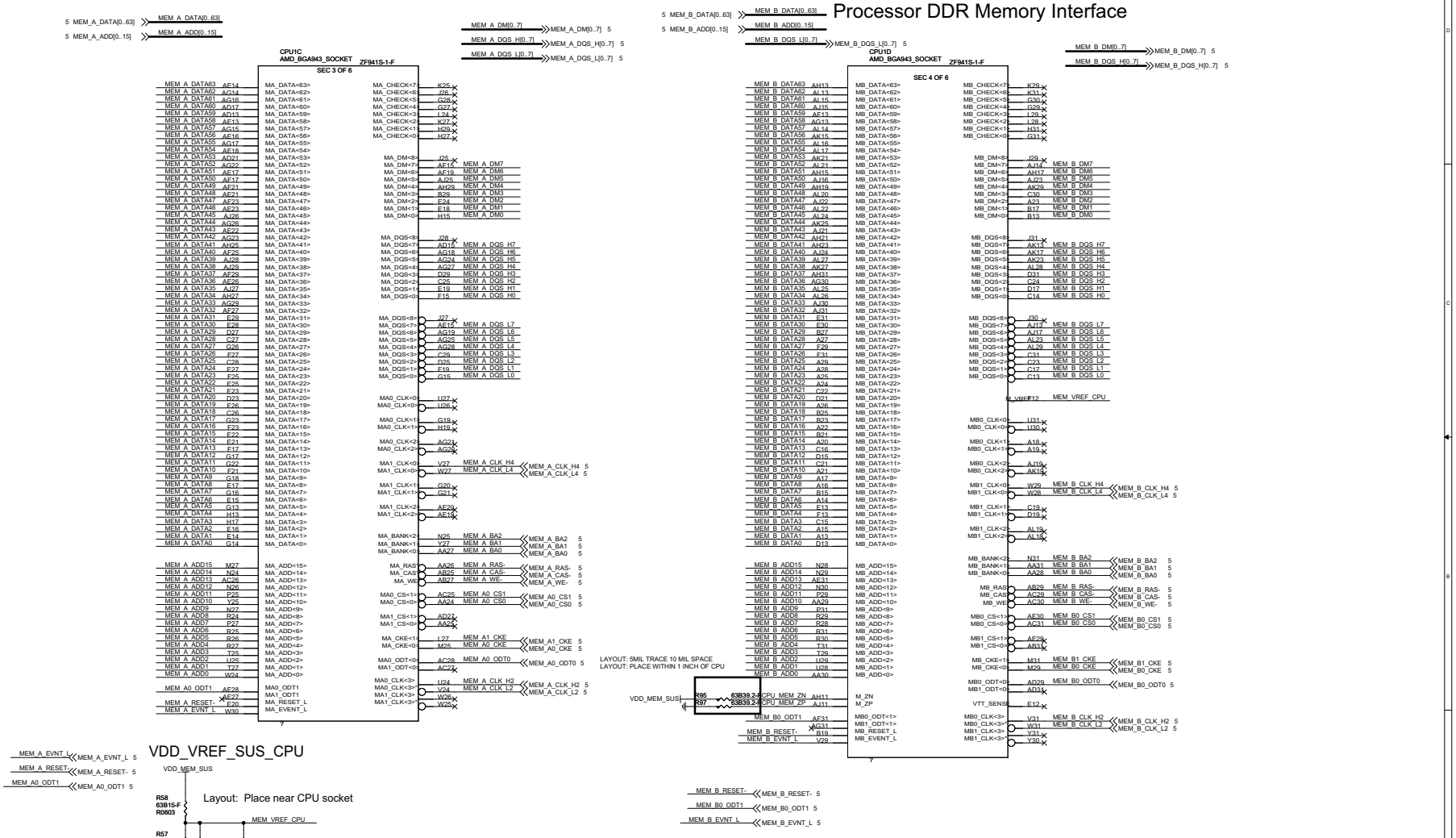


CPU Bottomside Decoupling



JETWAY INFORMATION CO.,LTD.	
Title: CPU_M2-940 HT I/F, PWR & GND	
Size: C	Document Number: MCP61JTD3	Rev: 1.0
Date: Thursday, April 01, 2010	Sheet 3 of 25	

Processor DDR Memory Interface



VDD_VREF_SUS_CPU

Company	JETWAY INFORMATION CO.,LTD.
Title	CPU_M2-940 DDRII MEMORY I/F
Size	C
Document Number	MCP61JTD3
Rev	1.0
Date:	Thursday, April 01, 2010
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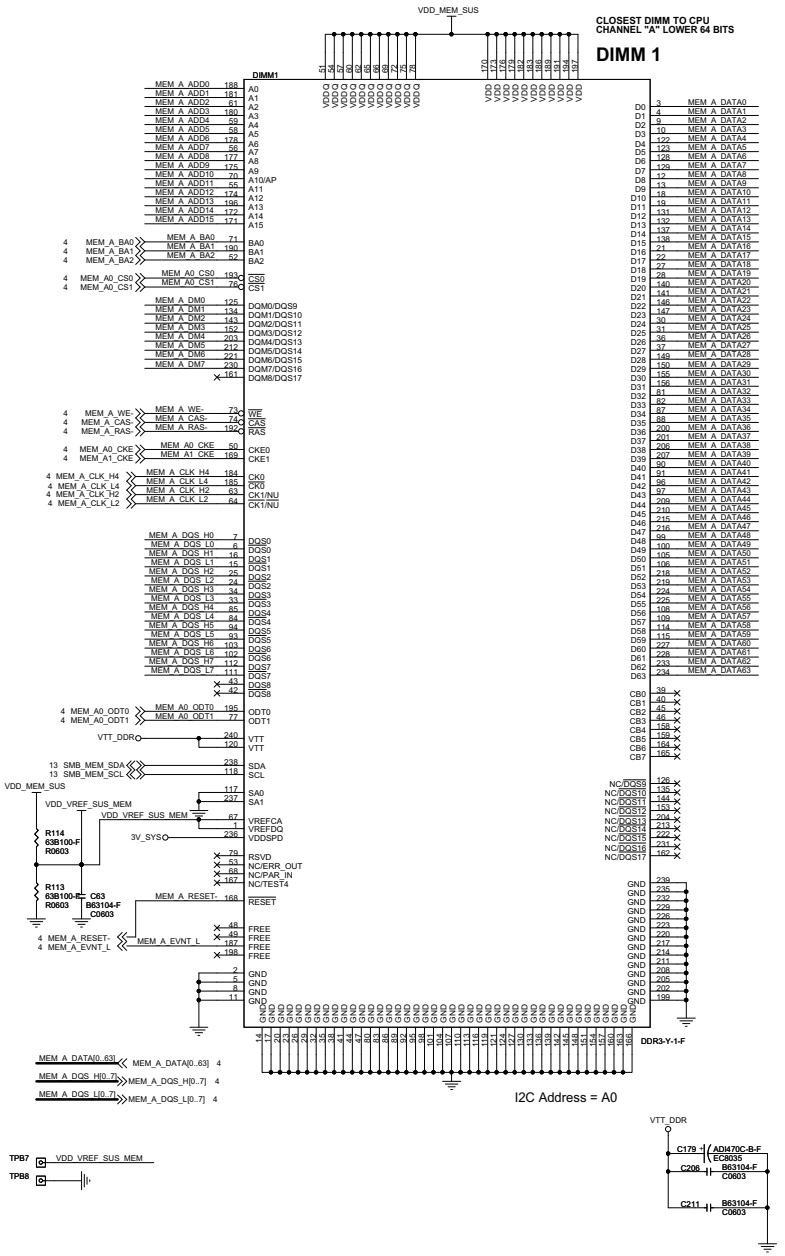
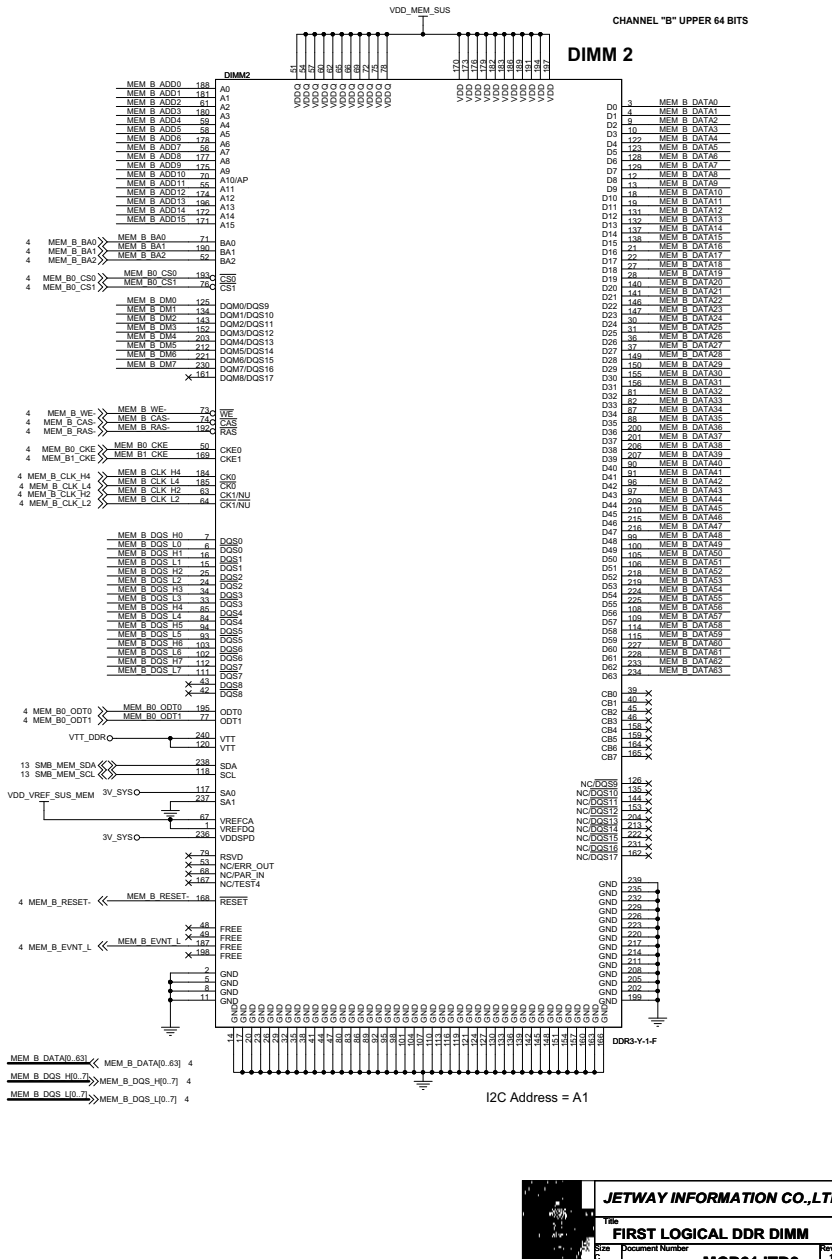




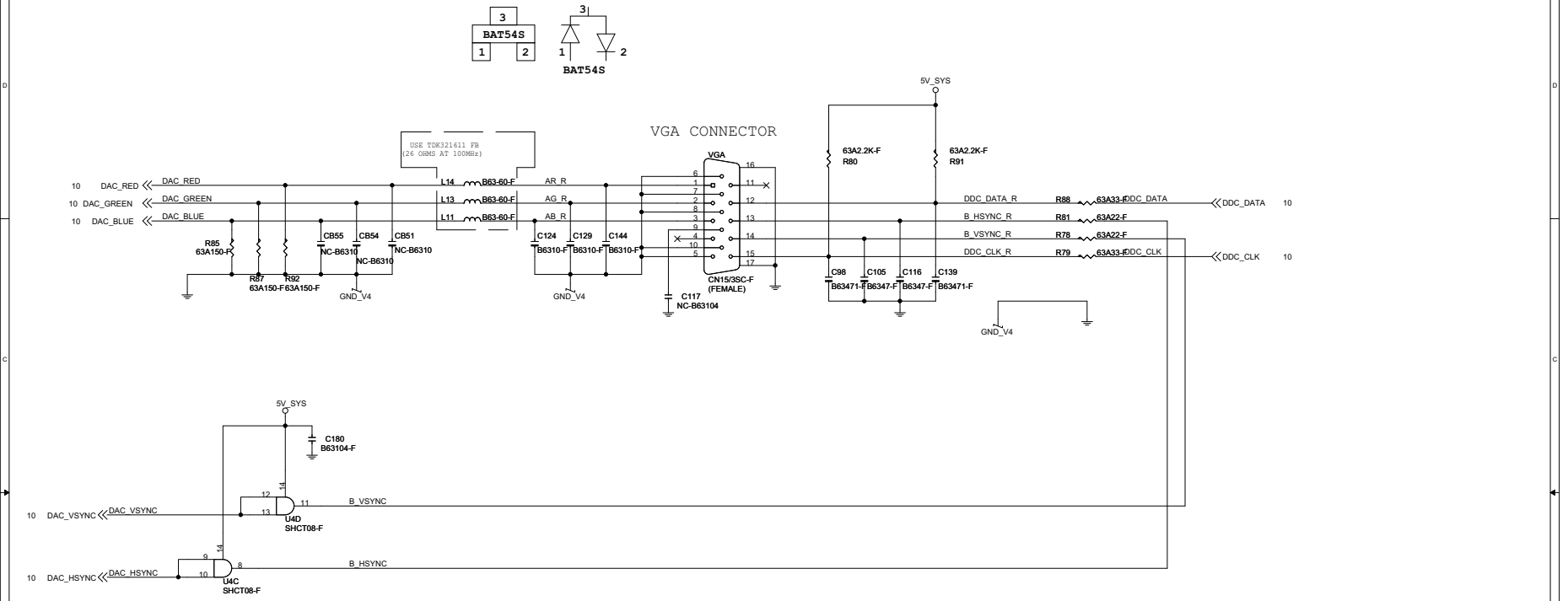
JETWAY INFORMATION CO.,LTD.

Title: FIRST LOGICAL DDR DIMM

Size: C | Document Number: MCP61JTD3 | Rev: 1.0

Date: Thursday, April 01, 2010 | Sheet 5 of

http://adf.ly/3o8pJ



JETWAY INFORMATION CO.,LTD.	
Title: VGA TV-OUT CONNECTOR	
Size: E	Document Number: MCP61JTD3
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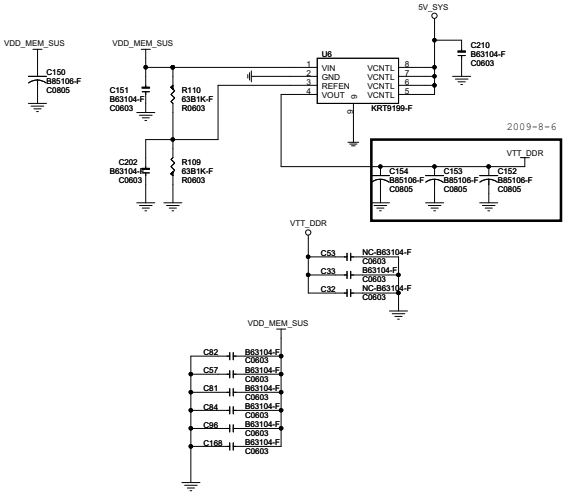
Date: Thursday, April 01, 2010	Sheet 6 of 24

http://adf.ly/3o8pJ



JETWAY INFORMATION CO.,LTD.

Title: DDRII TERMINATION

Size: C | Document Number: MCP61JTD3 | Rev: 1.0

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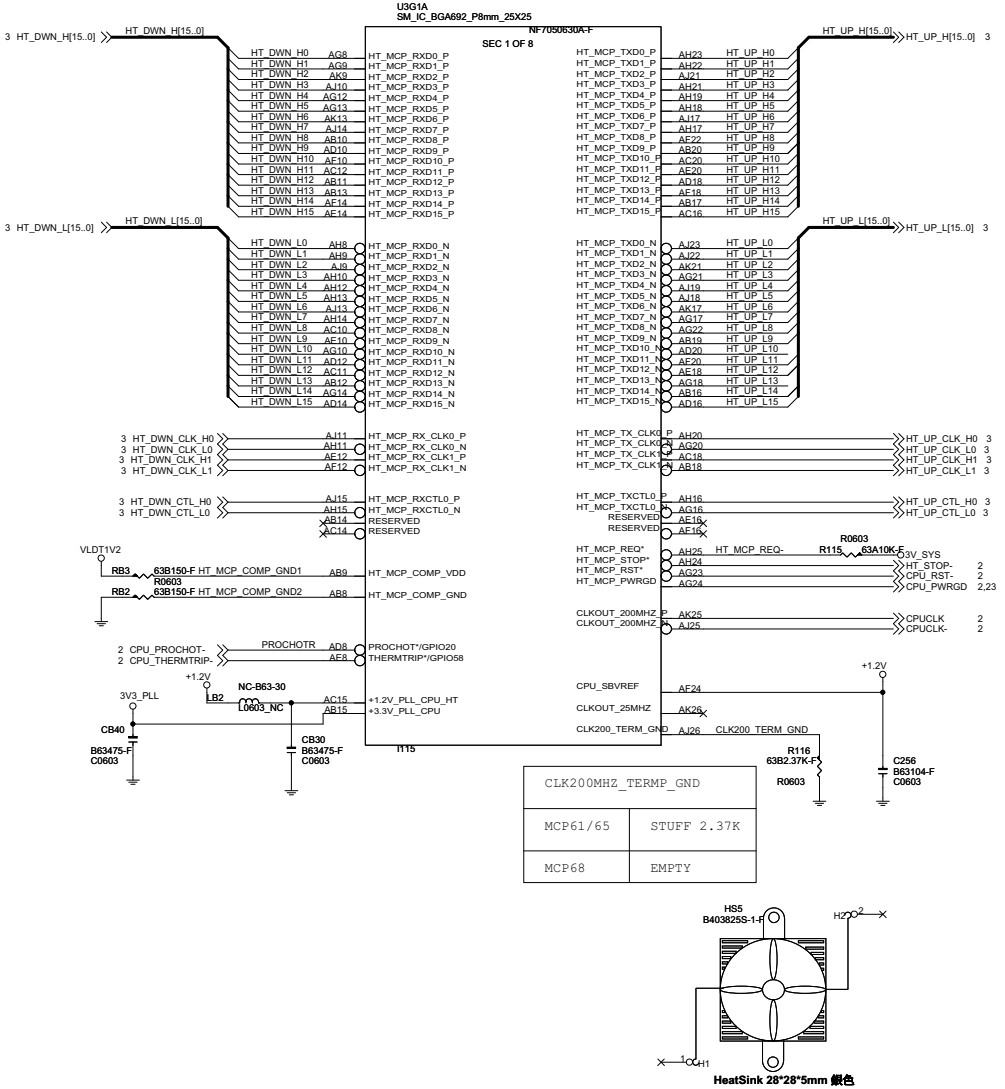
http://adf.ly/3o8pJ



CLK200MHZ_TERMP_GND	
MCP61/65	STUFF 2.37K
MCP68	EMPTY

2006/08/03

Del:R173,R177,R155,R176,R174,R175,R178,R179,R180,R156,R157,R158,U11
R255

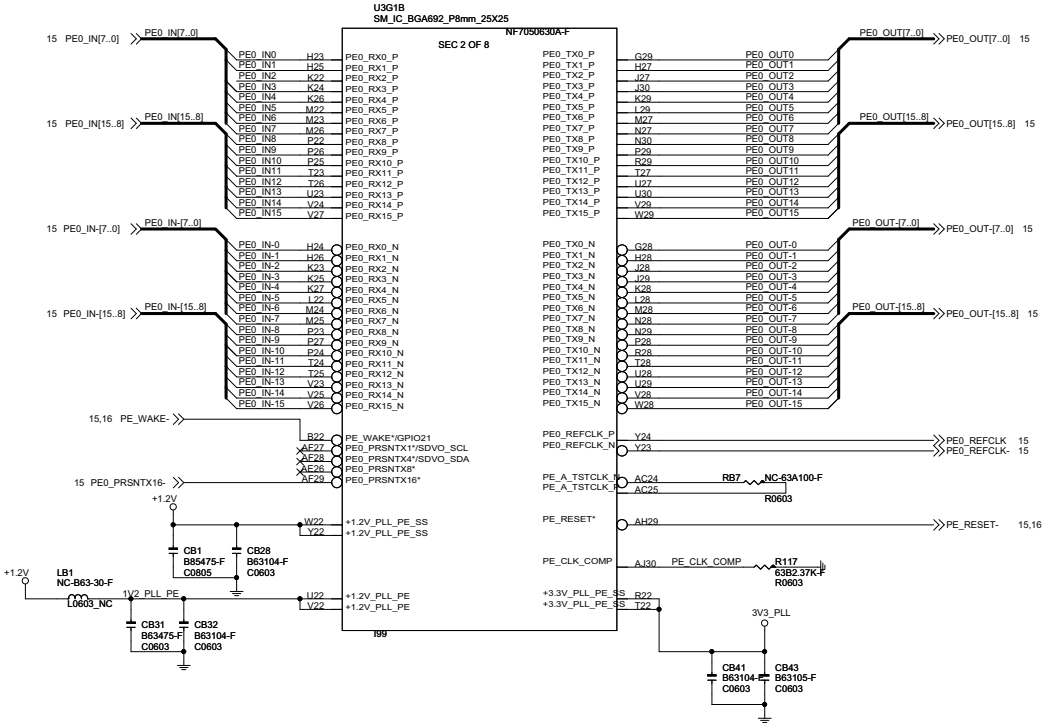
JETWAY INFORMATION CO.,LTD.

Title: MCP61 HT I/F

Size: Custom | Document Number: MCP61JTD3 | Rev: 1.0

Date: Thursday, April 01, 2010 | Sheet 8 of 24

http://adf.ly/3o8pJ



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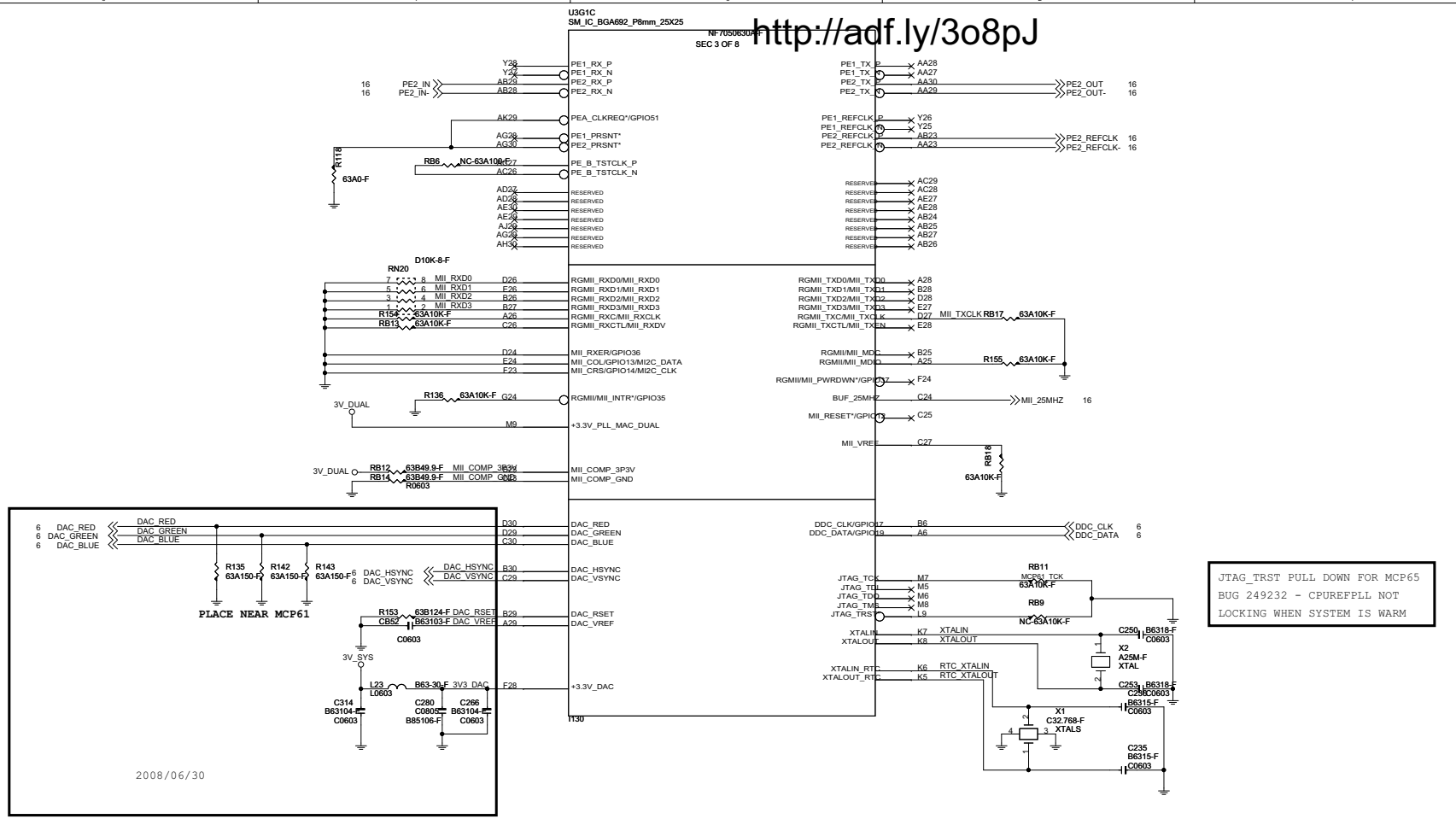
Title: MCP61 PCI-E LINK I/F

Size: Custom | Document Number: MCP61JTD3 | Rev: 1.0

Date: Thursday, April 01, 2010 | Sheet 9 of 24



JTAG_TRST PULL DOWN FOR MCP65
BUG 249232 - CPUREFPLL NOT
LOCKING WHEN SYSTEM IS WARM

JETWAY INFORMATION CO.,LTD.	
Title	MCP61 PCI-E 1X RGMII DAC
Size: Custom	Document Number: MCP61JTD3
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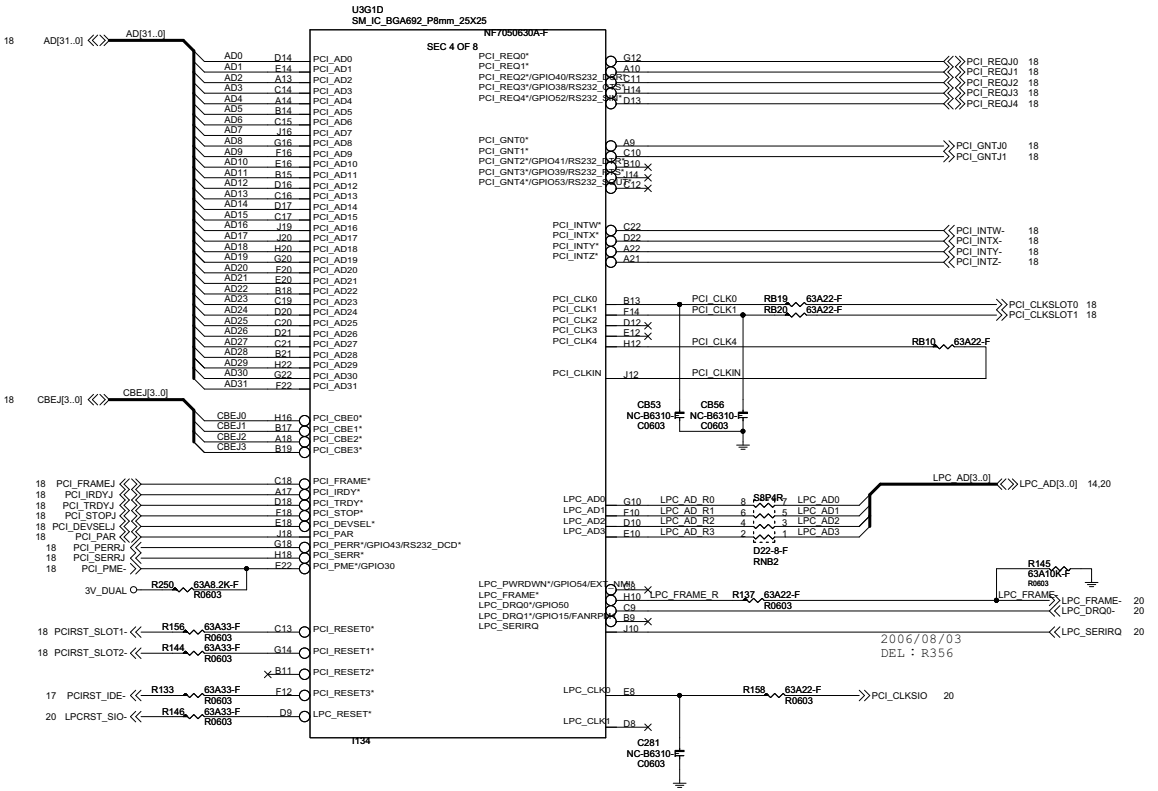
http://adf.ly/3o8pJ



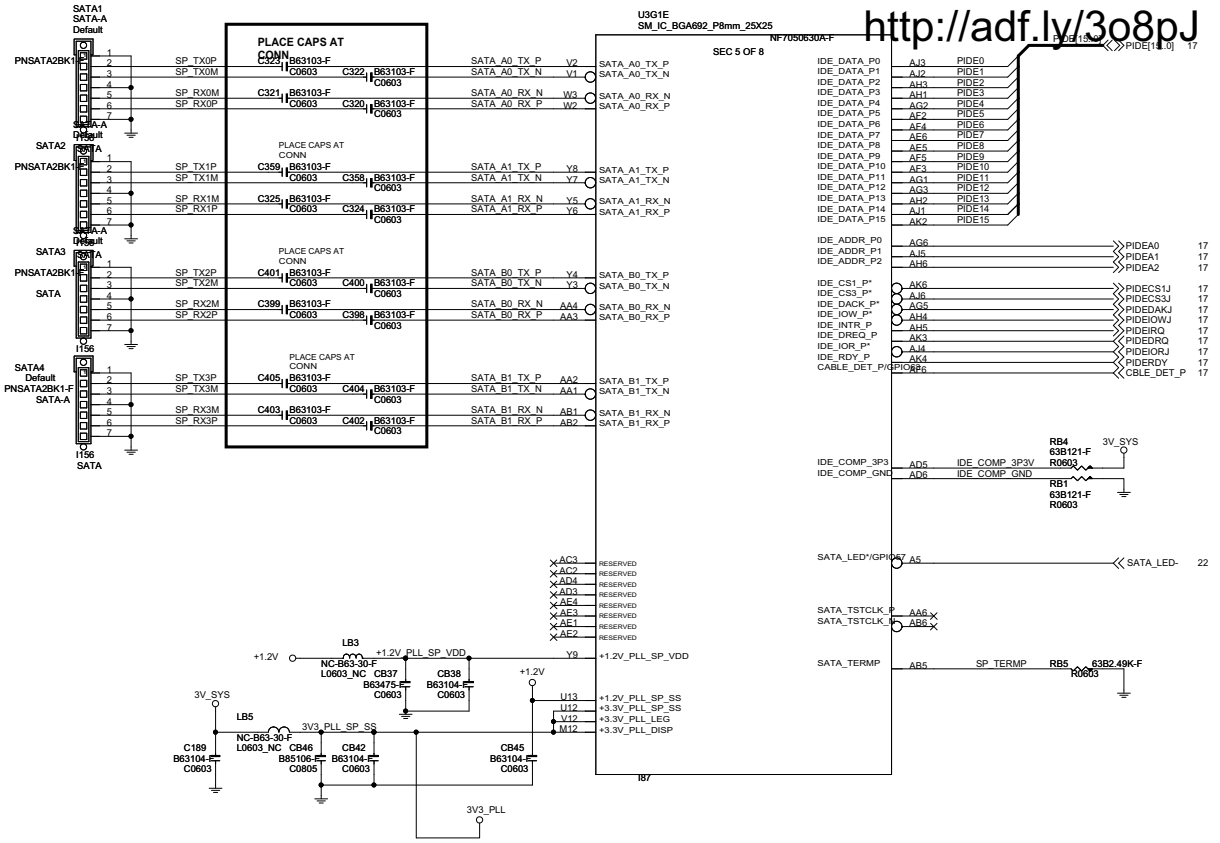
STRAP		
HDA_SDOUT	LPC_FRAME	
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS
1	1	RESERVED

JETWAY INFORMATION CO.,LTD.

Title: MCP61 PCI & LPC I/F

Size: Custom | Document Number: MCP61JTD3 | Rev: 1.0

Date: Thursday, April 01, 2010 | Sheet 11 of 24



Company	JETWAY INFORMATION CO.,LTD.
Title	MCP61 SATA & IDE
Size	Custom
Document Number	MCP61JTD3
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Date:	Thursday, April 01, 2010
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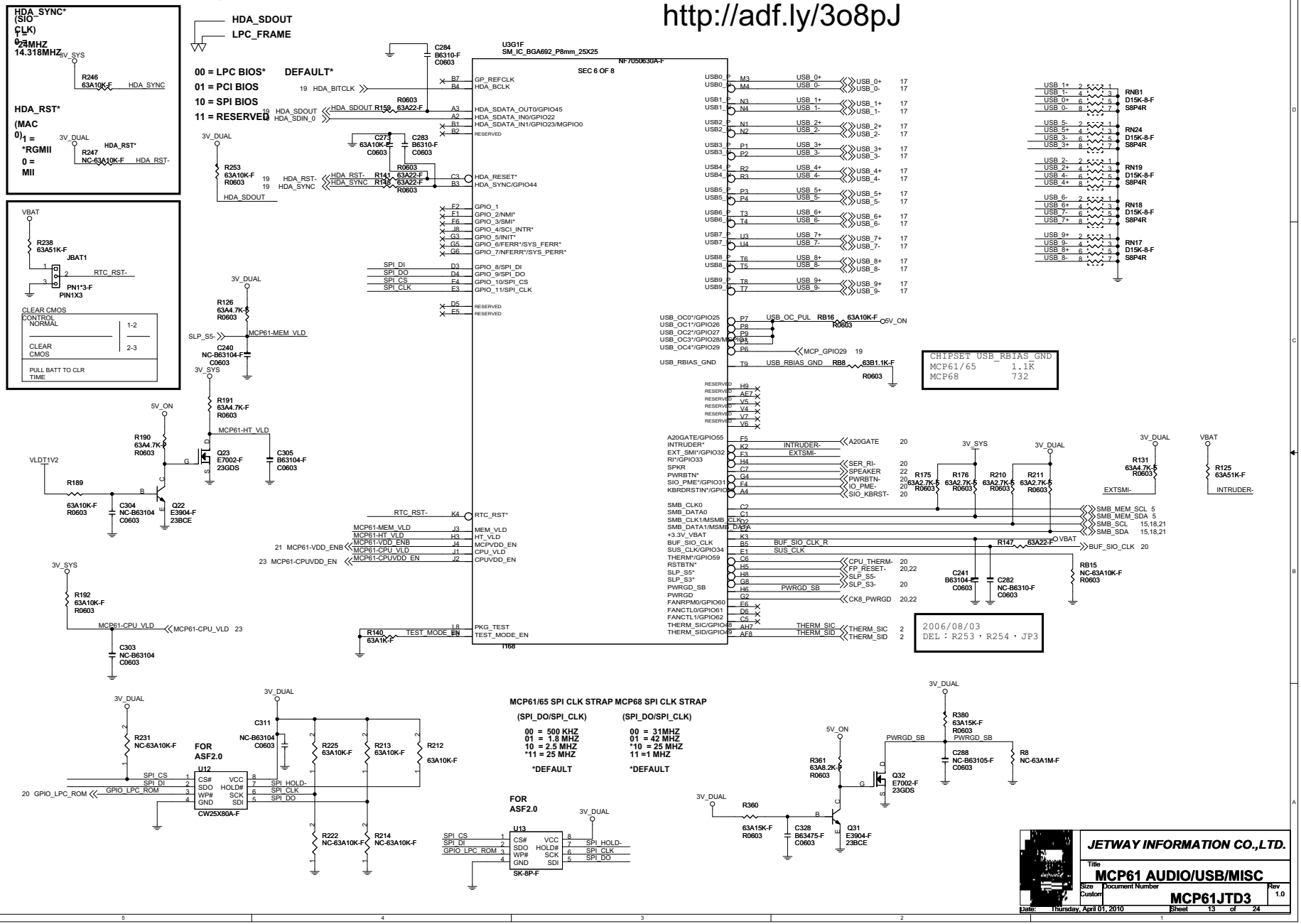
STRAP
HDA_SDOUT
LPC_FRAME
http://adf.ly/3o8pJ
HDA_SYNC* (SIO_CLK) 0= 24MHZ 14.318MHZ
HDA_RST* (MAC 0)1 = *RGMII 0 = MII
00 = LPC BIOS* DEFAULT*
01 = PCI BIOS
10 = SPI BIOS
11 = RESERVED
U3G1F
SM_IC_BGA692_P8mm_25X25
NF7050630A-F
SEC 6 OF 8
CLEAR CMOS
CONTROL
NORMAL 1-2
CLEAR CMOS 2-3
PULL BATT TO CLR TIME
CHIPSET USB_RBIAS_GND
MCP61/65 1.1K
MCP68 732
2006/08/03
DEL : R253 , R254 , JP3
MCP61 AUDIO/USB/MISC
MCP61JTD3
JETWAY INFORMATION CO.,LTD.
Thursday, April 01, 2010
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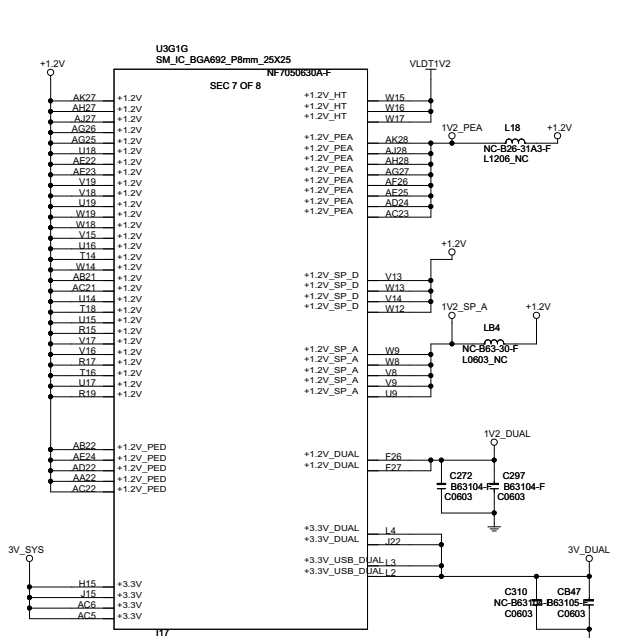
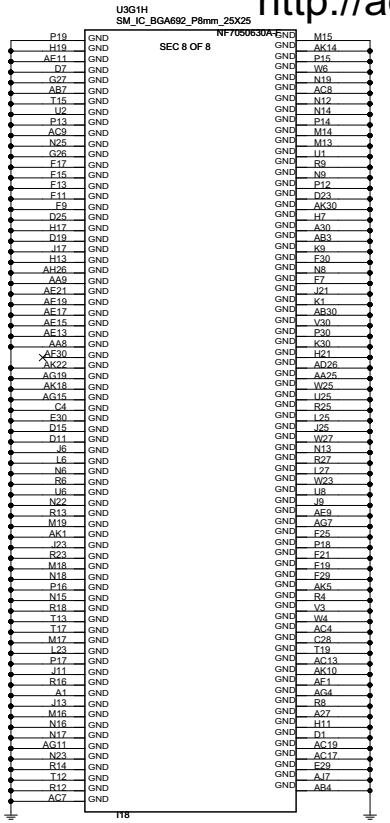
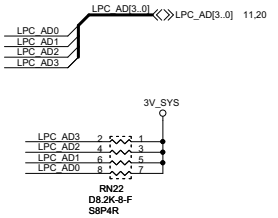
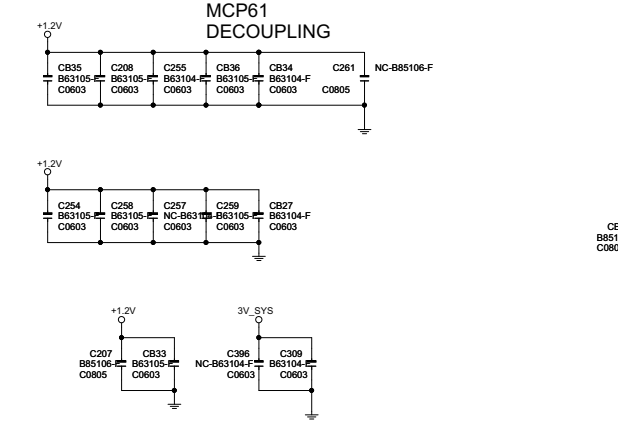
MCP61/65 SPI CLK STRAP MCP68 SPI CLK STRAP
(SPI_DO/SPI_CLK)
00 = 500 KHZ
01 = 1.8 MHZ
10 = 2.5 MHZ
*11 = 25 MHZ
*DEFAULT
(SPI_DO/SPI_CLK)
00 = 31MHZ
01 = 42 MHZ
*10 = 25 MHZ
11 =1 MHZ
*DEFAULT
FOR ASF2.0
FOR ASF2.0

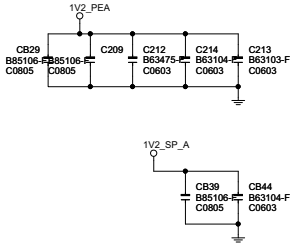
http://adf.ly/3o8pJ











MCP61 INTERNAL PULL-UP/DWN'S	
PE0_PRSNTX16*	10K PU TO 3.3V
PE0_PRSNTX8*	10K PU TO 3.3V
PE1_PRSNT*	10K PU TO 3.3V
PE2_PRSNT*	10K PU TO 3.3V
PE1_CLKREQ*	10K PU TO 3.3V
PCI_PME*/GPIO_30	8.2K PU TO 3.3V_DUAL
LPC_AD0	8.2K PU TO 3.3V
LPC_AD1	8.2K PU TO 3.3V
LPC_AD2	8.2K PU TO 3.3V
LPC_AD3	8.2K PU TO 3.3V
LPC_DRQ1/LPC_CS*	8.2K PU TO 3.3V
LPC_DRQ0*	8.2K PU TO 3.3V
LPC_SERIRQ	10K PU TO 3.3V
HDA_SDATA_IN1/GPIO_23/MGPIO_0	10K PD TO GND
HDA_SDATA_IN0/GPIO_22	10K PD TO GND
JTAG_TMS	10K PU TO 3.3V
JTAG_TRST*	10K PU TO 3.3V
JTAG_TDI	10K PU TO 3.3V
A20GATE	10K PU TO 3.3V
PE_WAKE*	10K PU TO 3.3V_DUAL
EXT_SMI*/GPIO32	10K PU TO 3.3V_DUAL
THERM*/GPIO_59	10K PU TO 3.3V
KBRDRSTIN*/GPIO_58	10K PU TO 3.3V
RI*/GPIO_33	10K PU TO 3.3V_DUAL
SIO_PME*/GPIO_31/MGPIO_2	10K PU TO 3.3V_DUAL
PWRBTN*	10K PU TO 3.3V_DUAL
RSTBTN*	10K PU TO 3.3V_DUAL

JETWAY INFORMATION CO.,LTD.

Title: MCP61 PWR/GND

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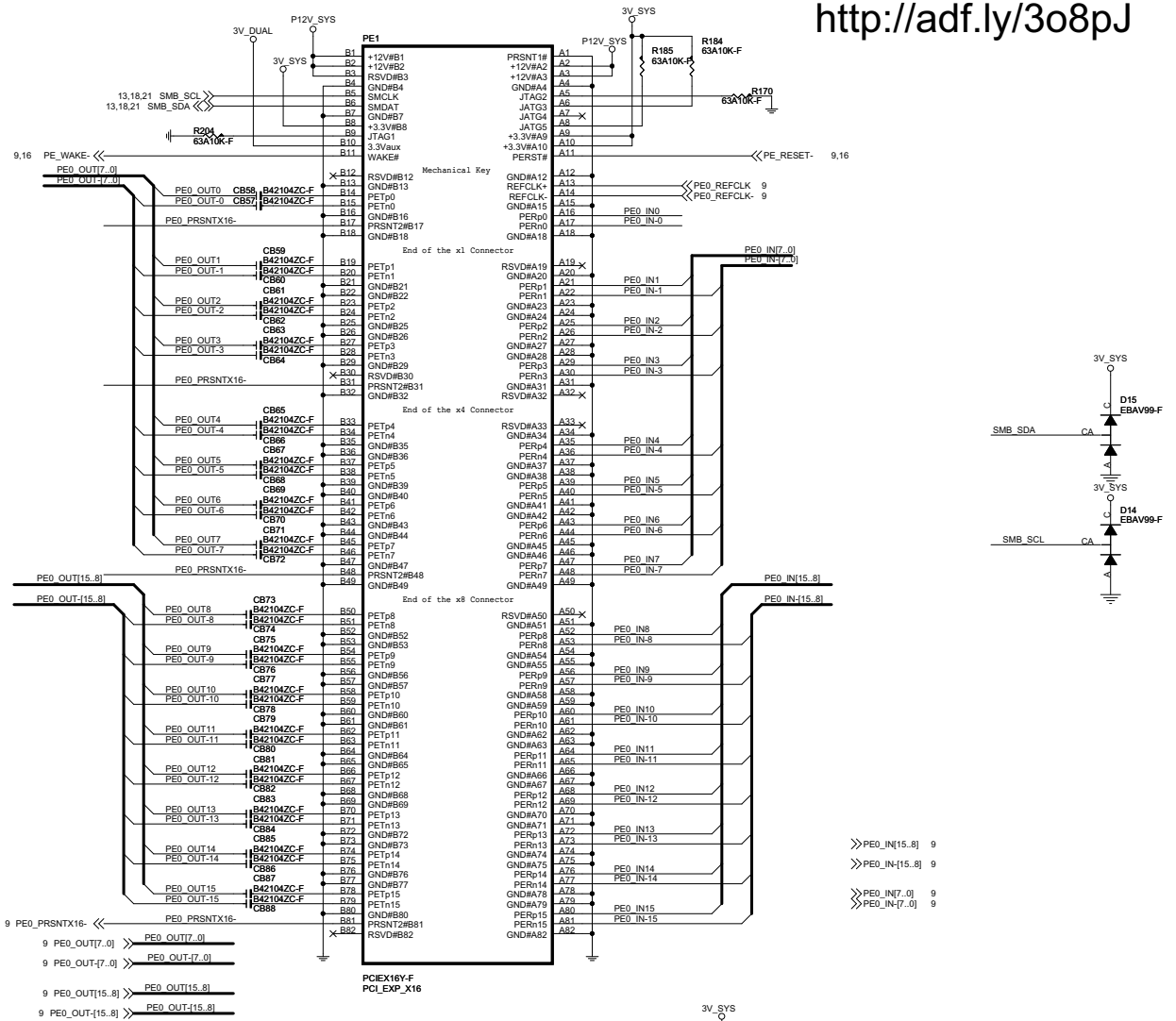

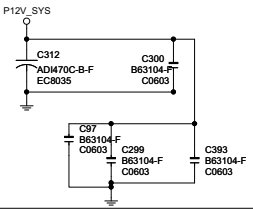

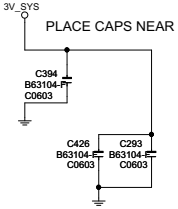

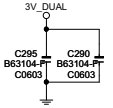

JETWAY INFORMATION CO.,LTD.	
Title: PCI-E by 16 & by 1 Slots	
Size: E	Document Number: MCP61JTD3
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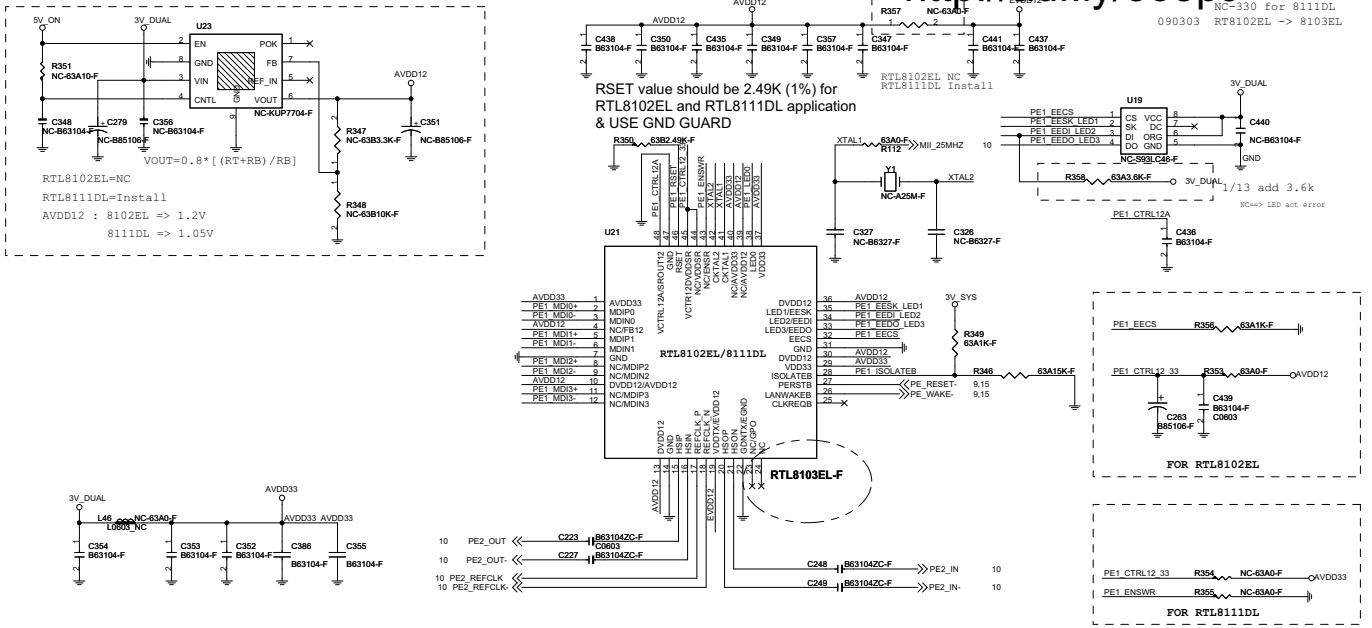
090303 RT8102EL -> 8103EL
NC-330 for 8111DL
NC-330 for 8102EL



JETWAY INFORMATION CO.,LTD.			
Title: RTL8102E/8111C			
Size: Custom	Document Number: MCP61JTD3		Rev: 1.0
Date: Thursday, April 01, 2010		Sheet 16 of 24	

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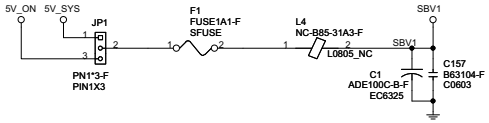

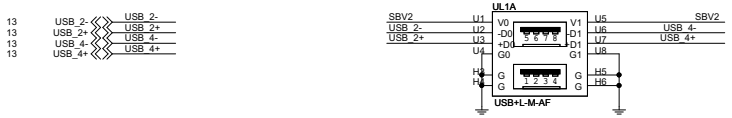

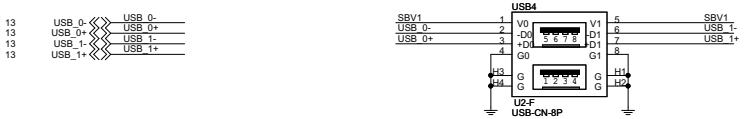

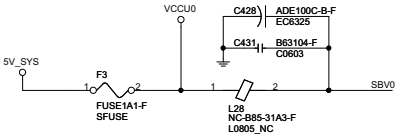

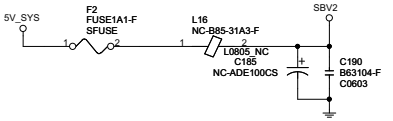

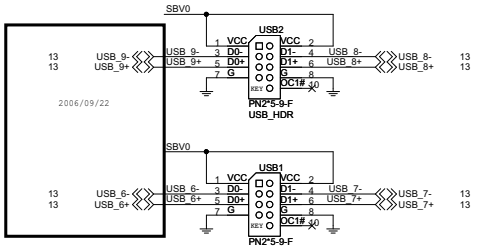

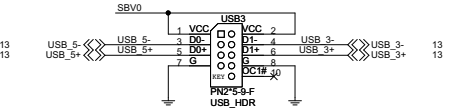

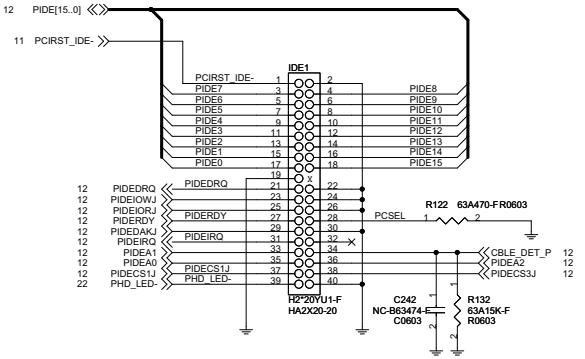

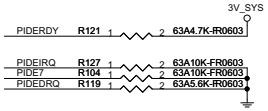

JETWAY INFORMATION CO.,LTD.

Title: **USB Ports & PATA CONN.**

Size: E | Document Number: MCP61JTD3 | Rev: 1.0

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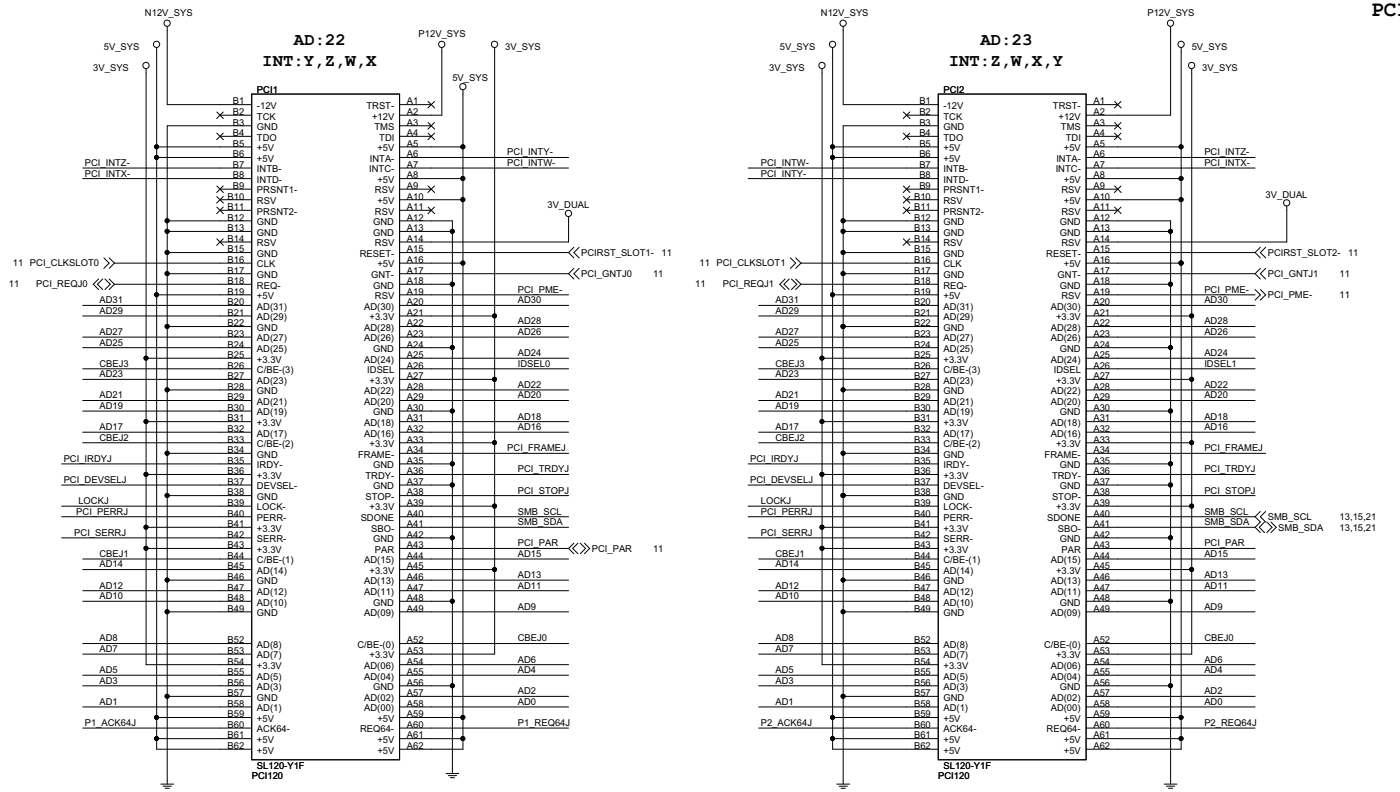
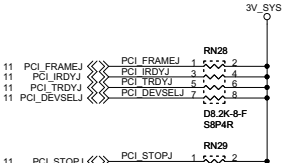
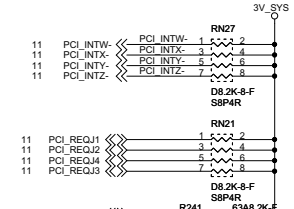
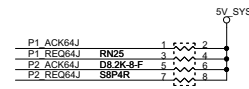
http://adf.ly/3o8pJ

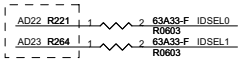


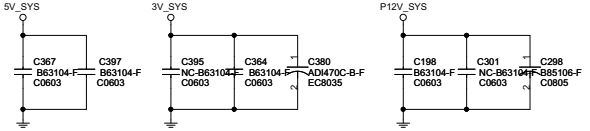
PCI Pull up/down resistor

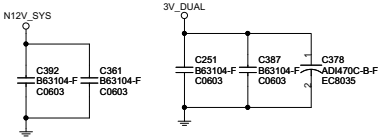












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Title: PCI SLOT 1 & 2

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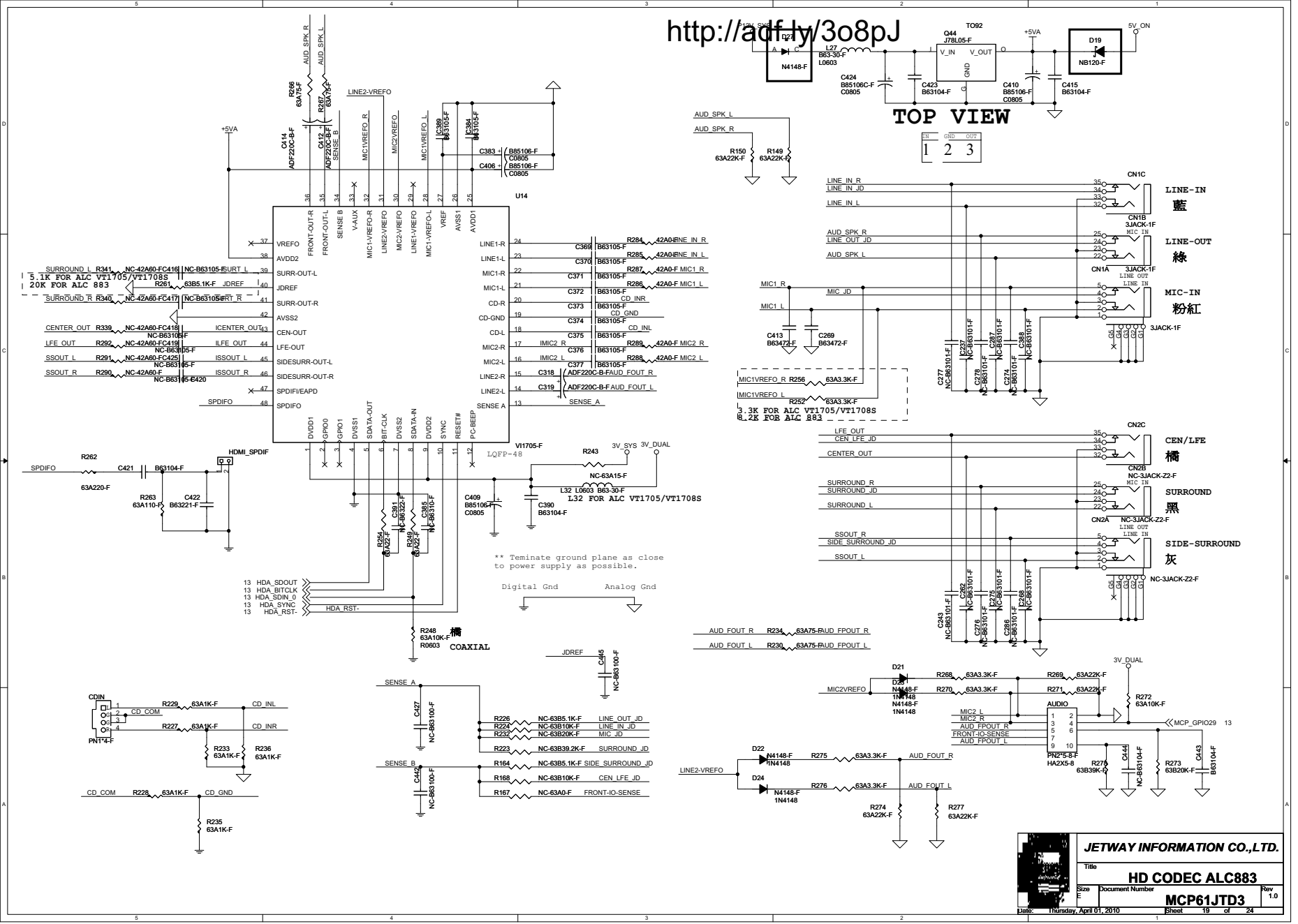

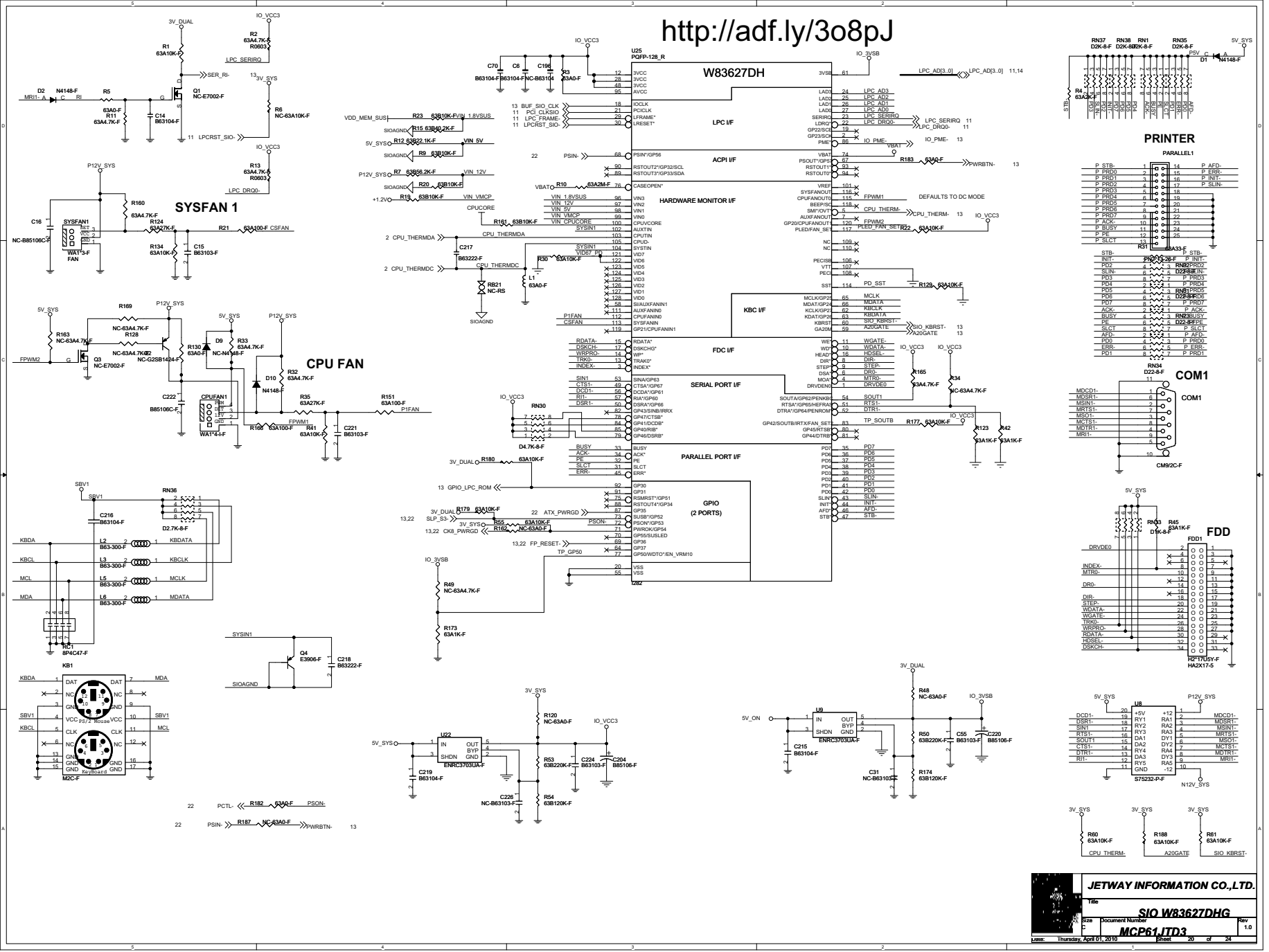
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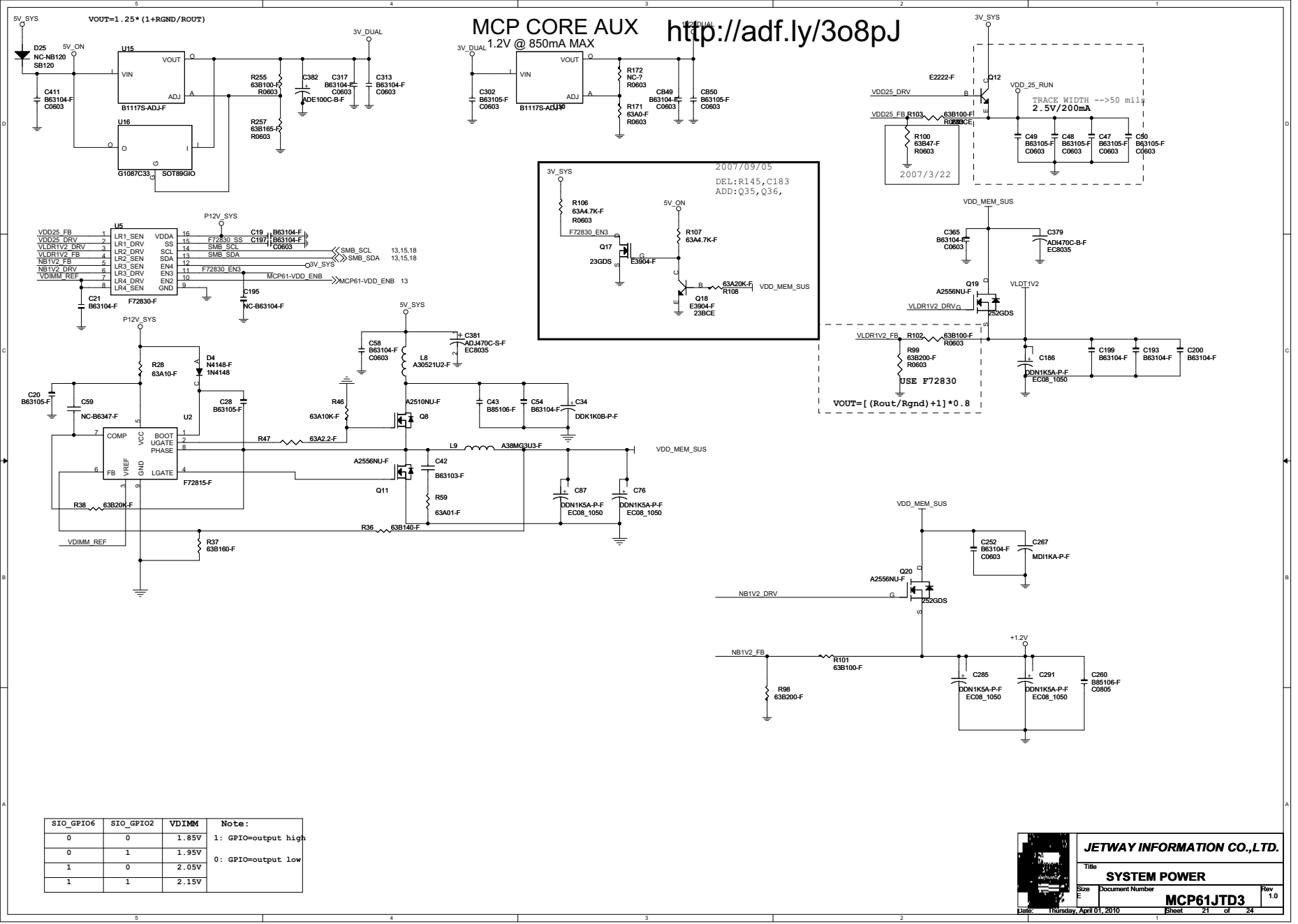
W83627DH
SYSFAN 1
CPU FAN
PRINTER
COM1
FDD
LPC I/F
ACPI I/F
HARDWARE MONITOR I/F
KBC I/F
FDC I/F
SERIAL PORT I/F
PARALLEL PORT I/F
GPIO
(2 PORTS)
JETWAY INFORMATION CO.,LTD.
SIO W83627DHG
MCP61JTD3
Thursday, April 01, 2010



SIO_GPIO6	SIO_GPIO2	VDIMM
0	0	1.85V
0	1	1.95V
1	0	2.05V
1	1	2.15V

Note:
1: GPIO=output high
0: GPIO=output low

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Title: SYSTEM POWER

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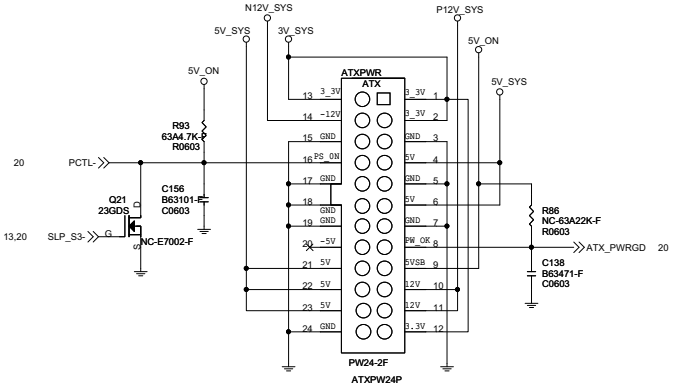
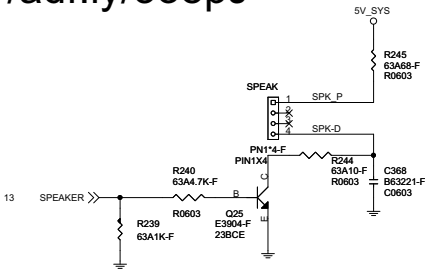
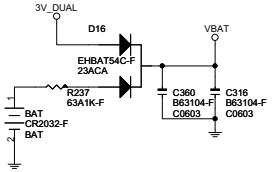
http://adf.ly/3o8pJ

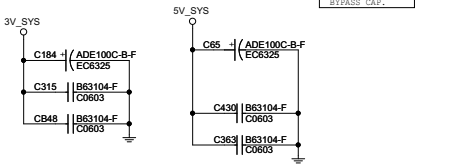


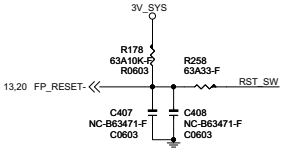


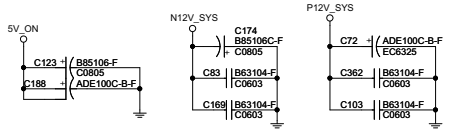


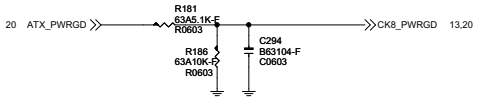
POWER CONN DECOUPING

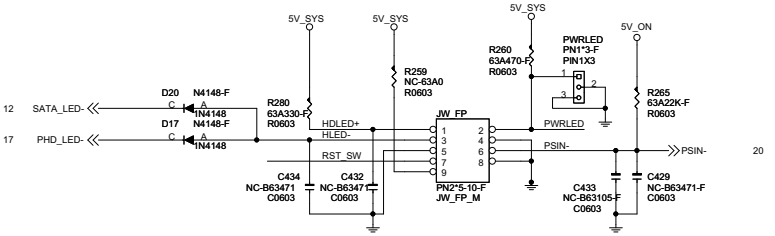
ATX CONN. NEED BYPASS CAP.











2006/08/03
DEL : R328 , R329 , R348 , R349 , R363
C453 , C466 , Q34 , Q35 , Q37

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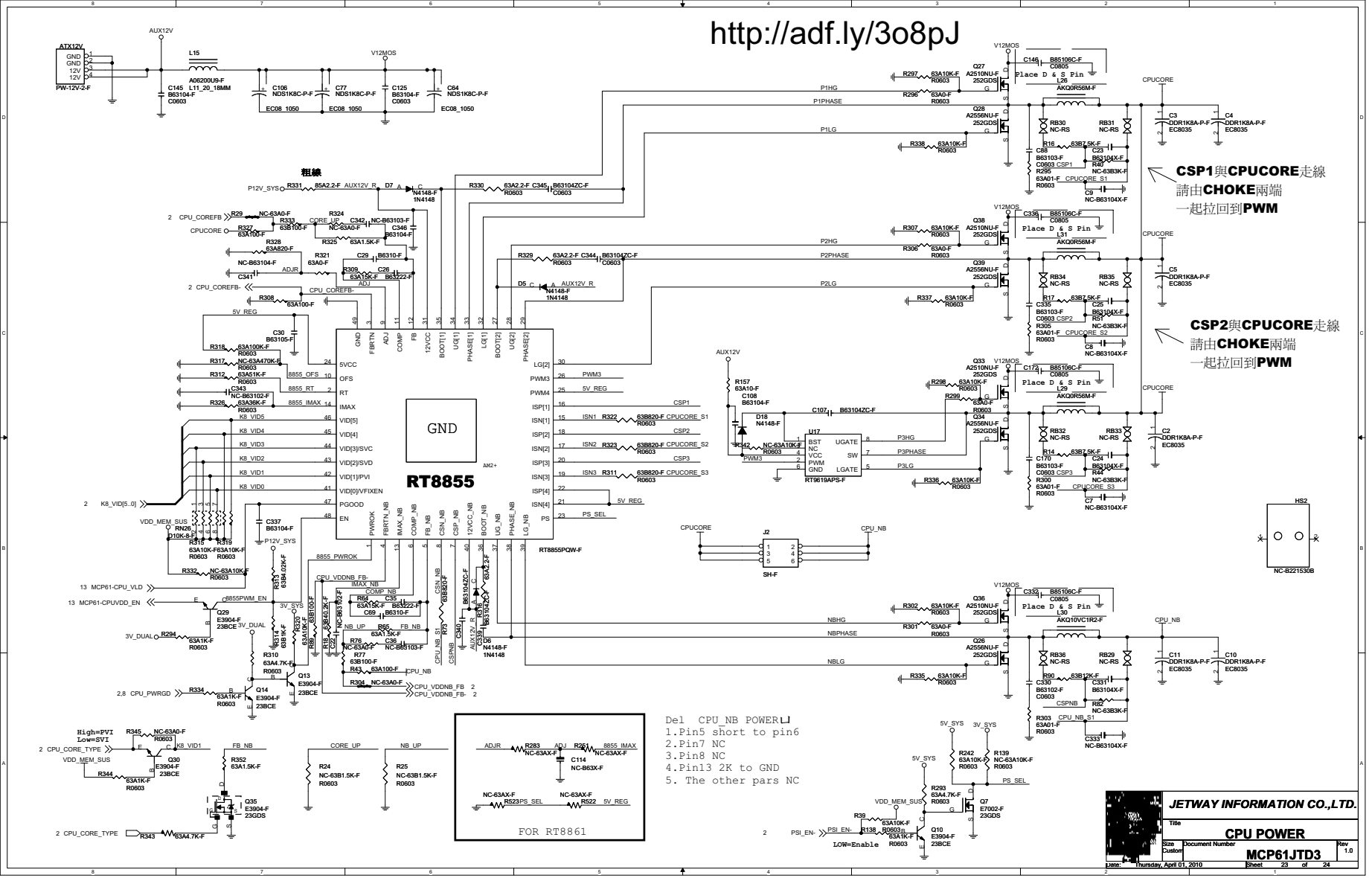
http://adf.ly/3o8pJ
RT8855
RT8855PQW-F
GND
CSP1與CPUCORE走線
請由CHOKE兩端
一起拉回到PWM
CSP2與CPUCORE走線
請由CHOKE兩端
一起拉回到PWM
Del CPU_NB POWER
1.Pin5 short to pin6
2.Pin7 NC
3.Pin8 NC
4.Pin13 2K to GND
5. The other pars NC
FOR RT8861
JETWAY INFORMATION CO.,LTD.
CPU POWER
MCP61JTD3