GIGABYTE™

GA-Z87X-D3H Rev 1.0

Structure Introductions

Power Sequence

Measure Points

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Curriculum Content

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Intel Shark Bay Platform Introduction

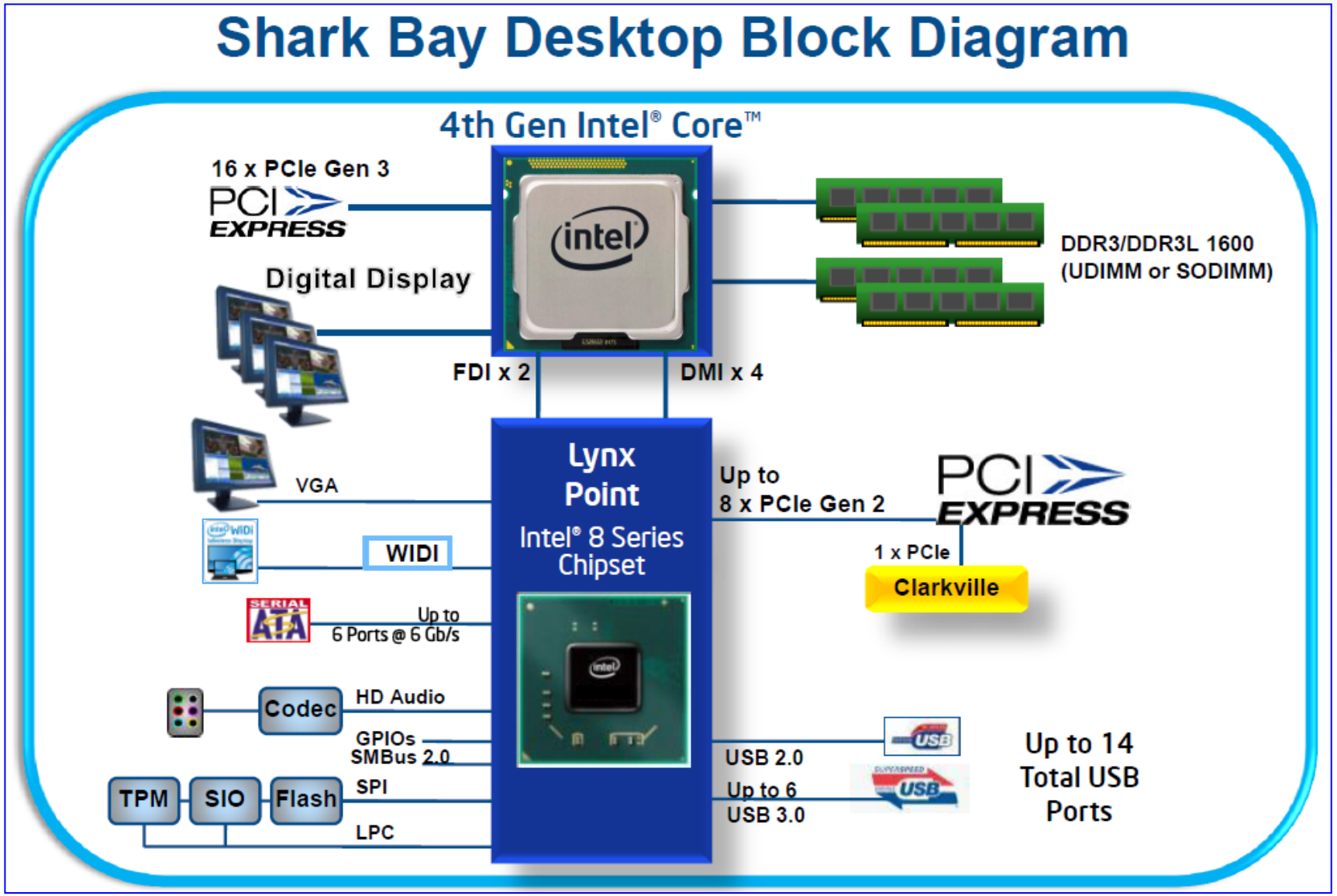
1. Introduction : The Shark Bay platform based on the Haswell processor and Lynx Point Platform Controller Hub (PCH) , The Haswell Processor along with the Lynx Point PCH is designed for a 2-chip platform enabling higher performance, lower cost, easier validation and improved x-y footprint.

– **The Haswell Processor**: The processor has the Memory Interface, PCI Express* and the Direct Media Interface (DMI) integrated into the processor .The processor includes Integrated Display Engine, GPU , Integrated memory controller and three DDI ports. Each DDI port supports Display Port or HDMI or DVI. The processor supports two channels of DDR3/DDR3L @ 1.5V with a maximum of two UDIMMs per channel. Denlow-WS supports UDIMM ECC. The PCI Express* port(s) are fully-compliant with the PCI Express Base Specification, Revision 3.0.

– **The Lynx Point PCH** : The Lynx Point PCH connects to the processor via the Direct Media Interface and Flexible Display Interface. The PCH is ACPI compliant and can support the Full-on, Suspend to RAM, Suspend to Disk, Soft-Off and Deep Sx power management states. The PCH is capable of supporting up to 8 PCI Express 2.0 compliant root ports; up to 6 SATA ports at 1.5 Gbps, 3 Gbps and 6 Gbps; and up to 14 USB 2.0 ports that can be mapped to a single xHCI controller or shared across two separate EHCI controllers.

Furthermore, up to 6 of the 14 possible USB 2.0 ports can be configured as USB 3.0 ports mapped to the xHCI controller. Flexible IO technology allows some high speed signals to be used as PCI Express ports, SATA ports or USB 3.0 ports. Refer to the Lynx Point External Design Specification for more details about supported features and capabilities.

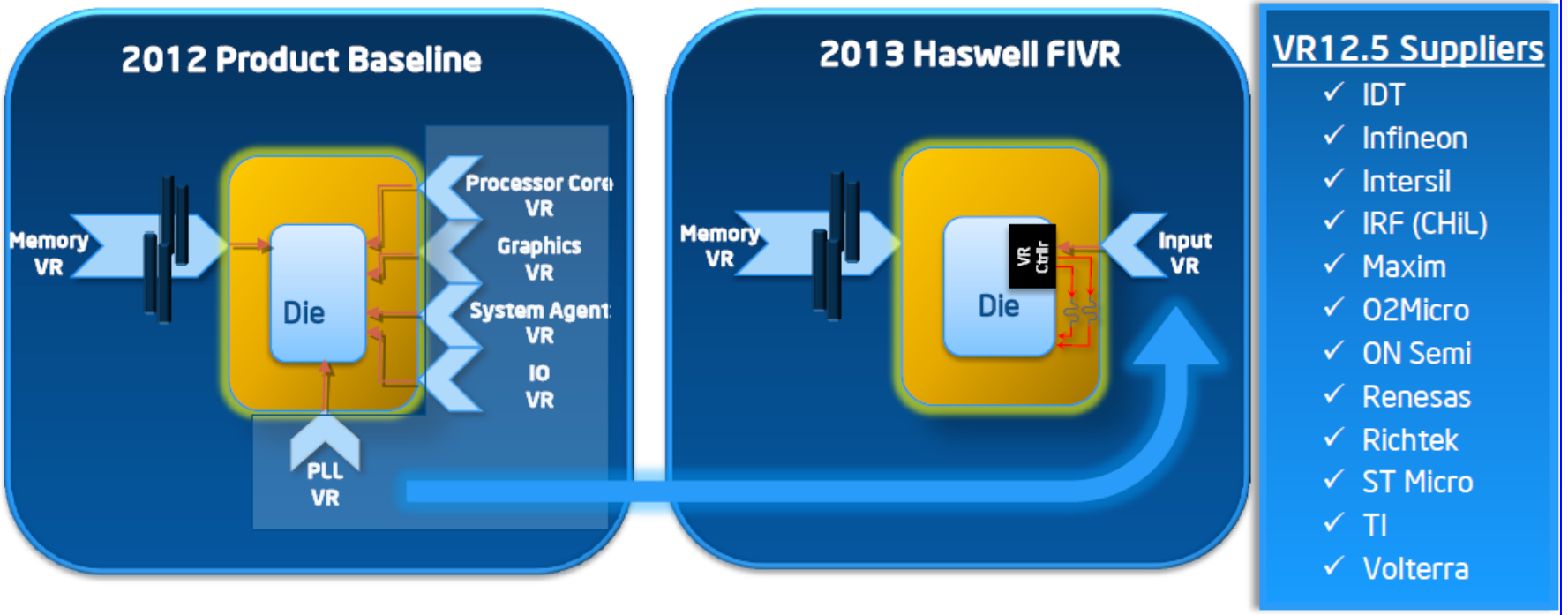
System Block Diagram (Haswell + Lynx Point)



Fully Integrated Voltage Regulator (FIVR)

Fully Integrated Voltage Regulator (FIVR)

FIVR Simplifies Platform Power Delivery Design

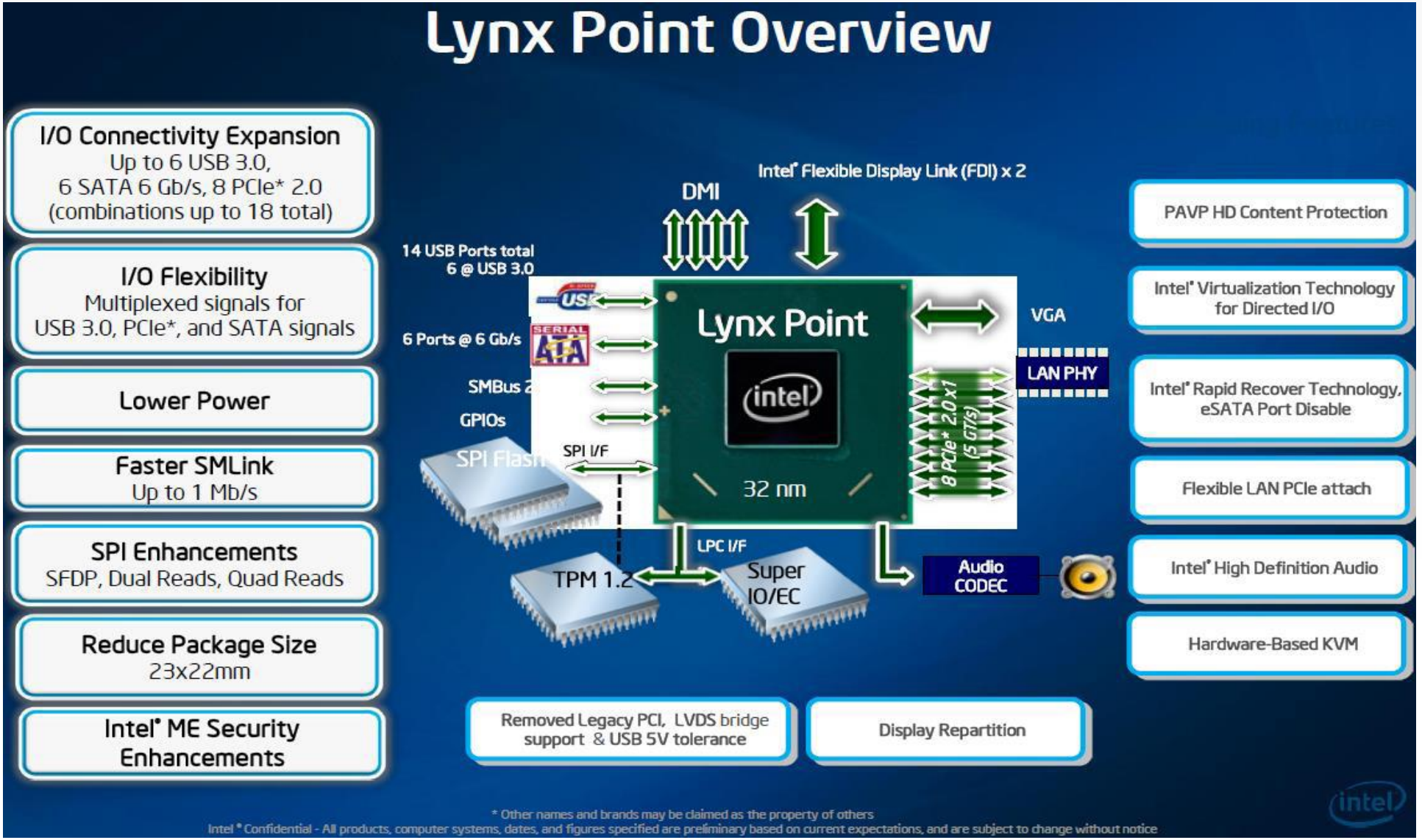


VR12.5 Suppliers

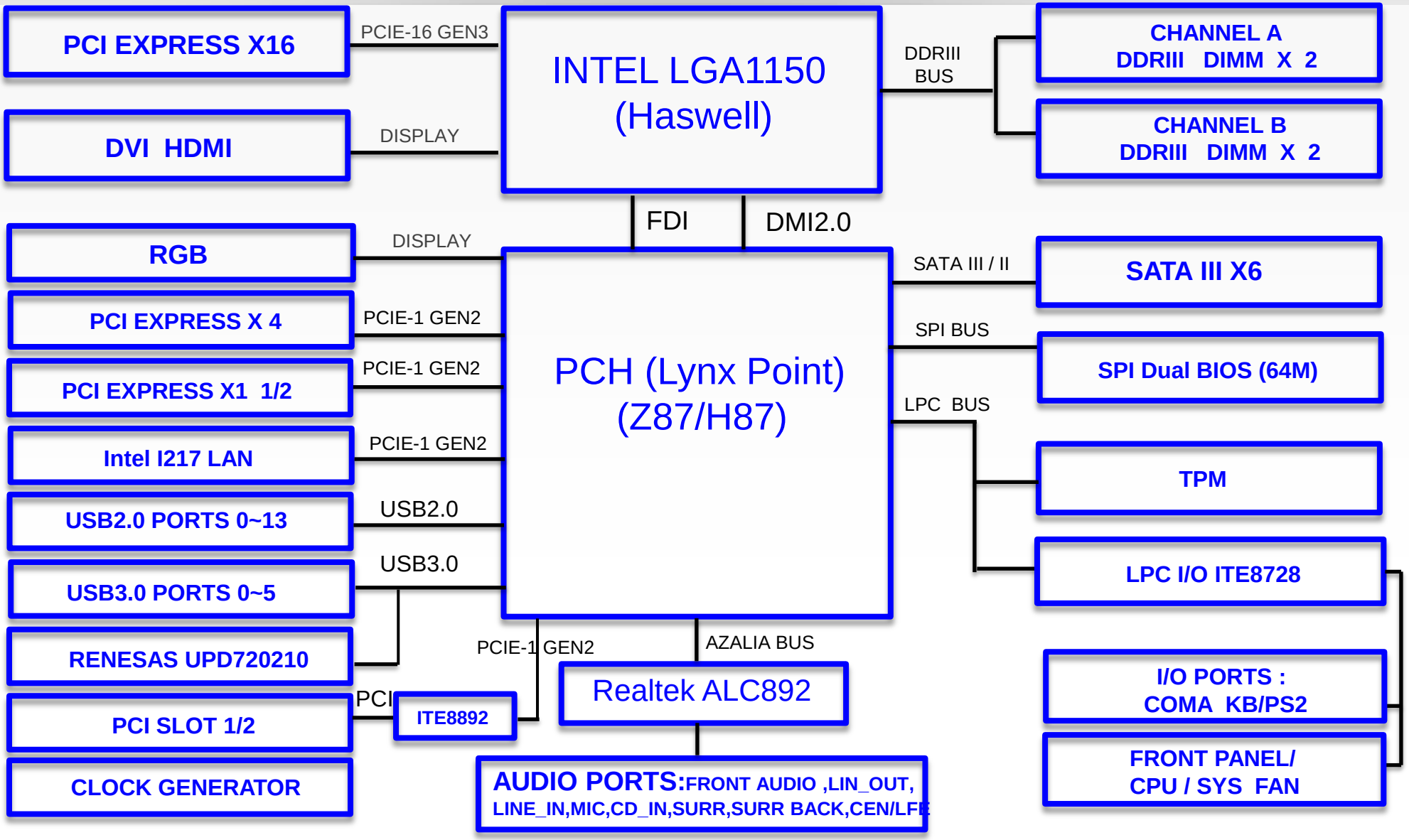
- ✓ IDT
- ✓ Infineon
- ✓ Intersil
- ✓ IRF (CHiL)
- ✓ Maxim
- ✓ O2Micro
- ✓ ON Semi
- ✓ Renesas
- ✓ Richtek
- ✓ ST Micro
- ✓ TI
- ✓ Volterra

- FIVR integrates legacy power delivery onto processor pkg/die
- Greatly simplifies platform power design; consolidates five platform VRs to one
- Better arch flexibility and finer-grain on-die processor delivery control

Lynx Point Overview



Z87X-D3H Block Diagram



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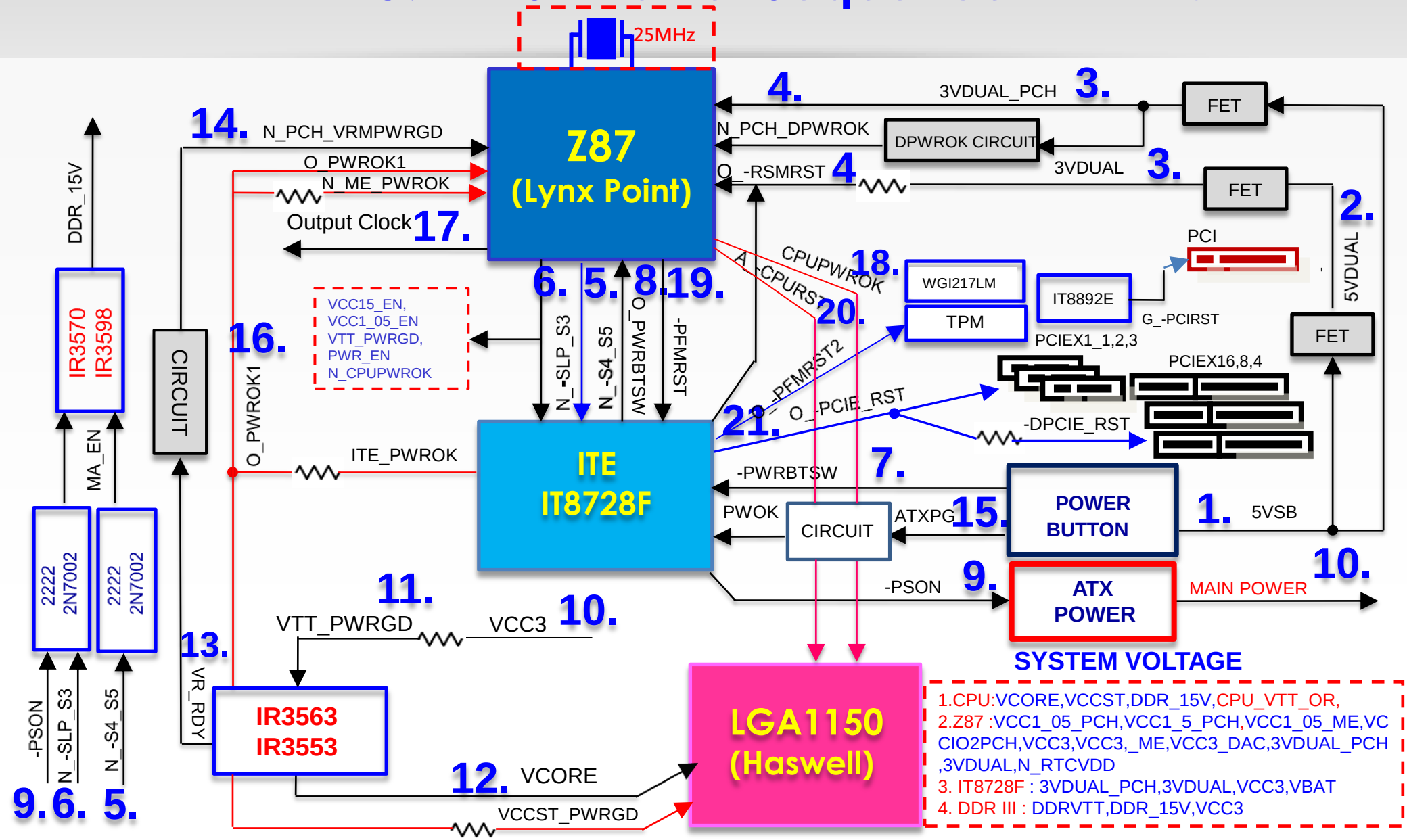
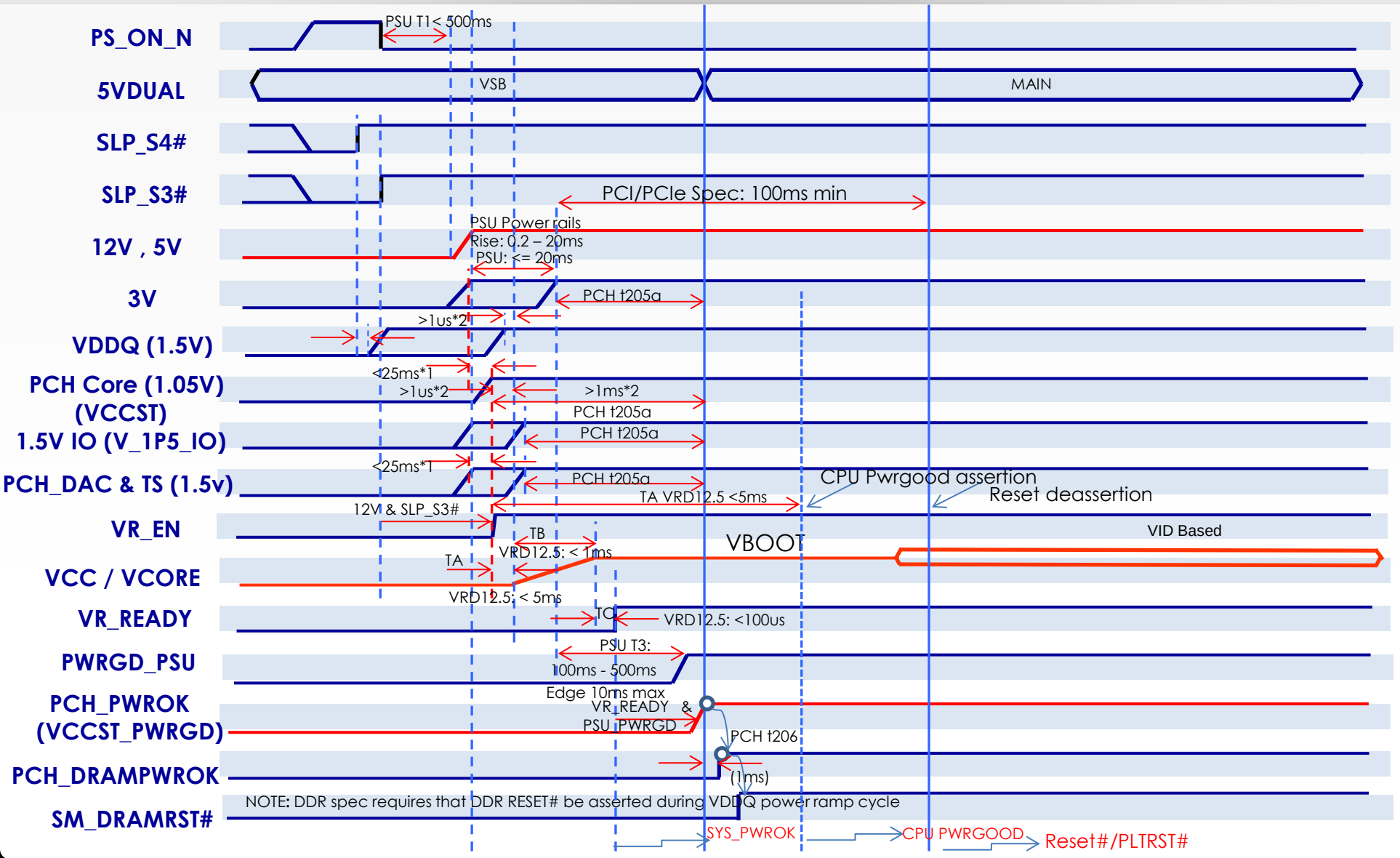
Z87X-D3H Power Sequence Rev 1.0



SYSTEM VOLTAGE

1.CPU:VCORE,VCCST,DDR_15V,CPU_VTT_OR,
2.Z87 :VCC1_05_PCH,VCC1_5_PCH,VCC1_05_ME,VCCIO2PCH,VCC3,VCC3,_ME,VCC3_DAC,3VDUAL_PCH,3VDUAL,N_RTCVDD
3. IT8728F : 3VDUAL_PCH,3VDUAL,VCC3,VBAT
4. DDR III : DDRVTT,DDR_15V,VCC3

Z87 Power Sequencing and Timing - 1



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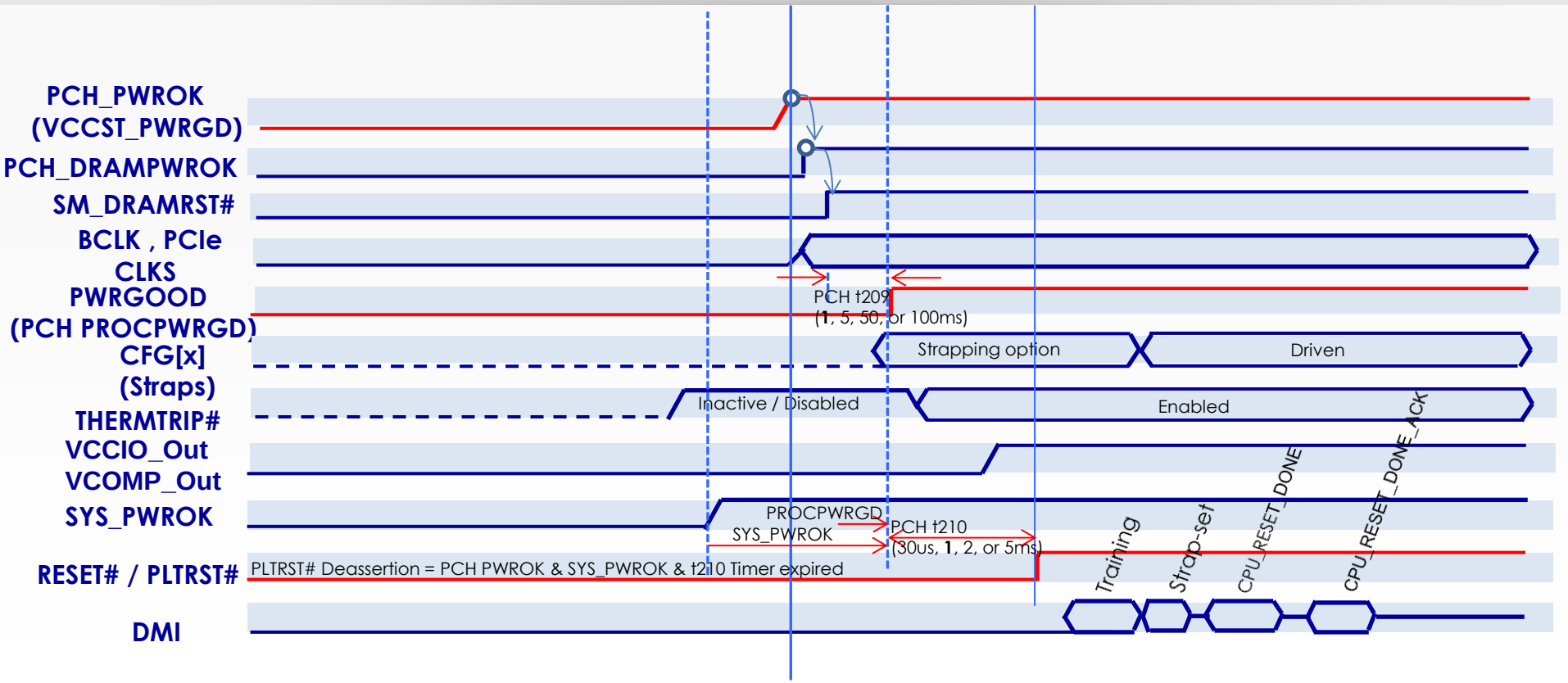
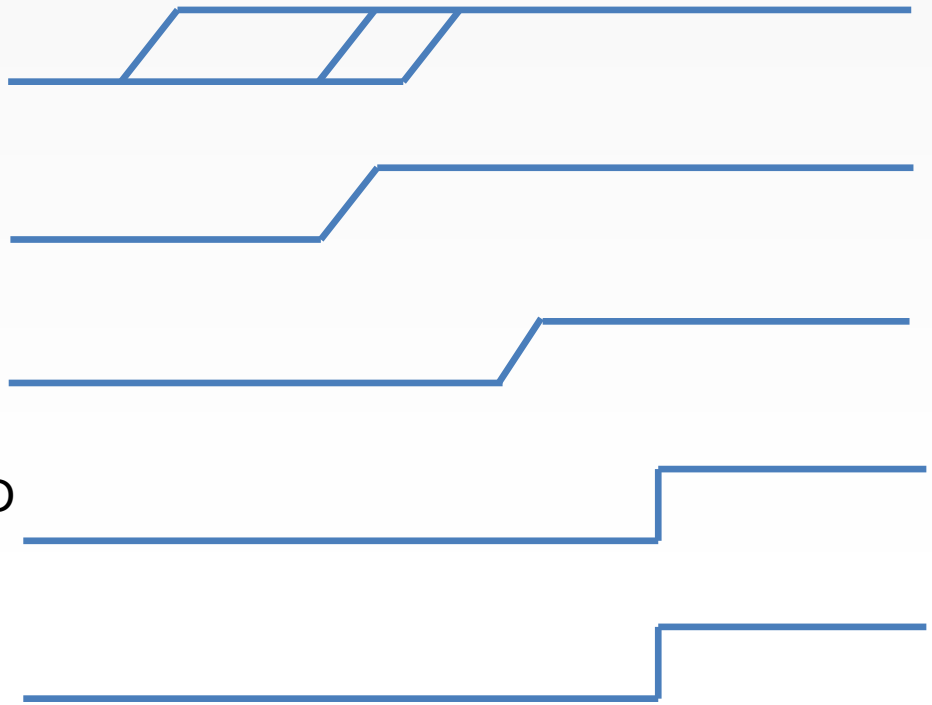
Z87 Power Sequencing and Timing - 2

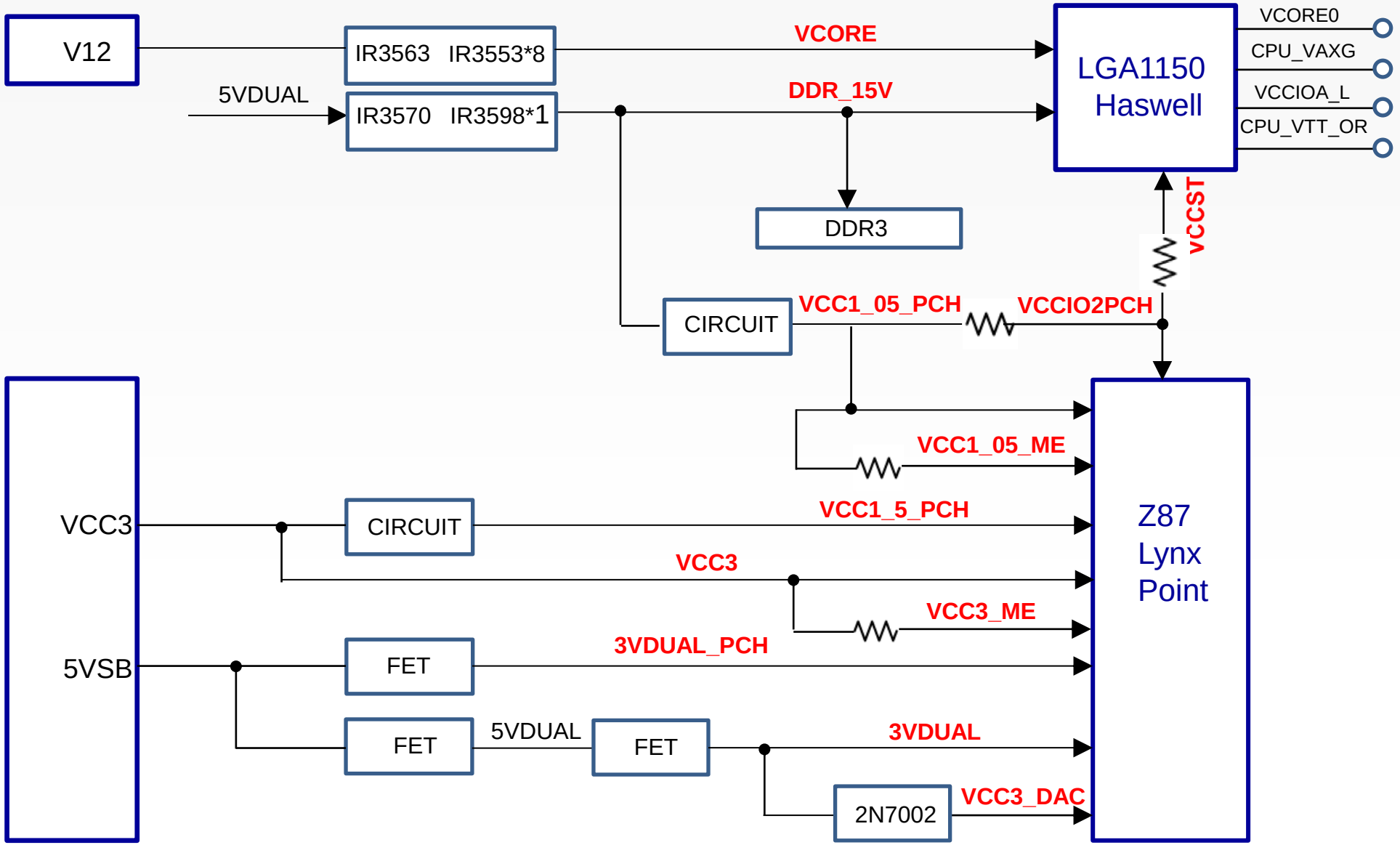


VCCST Power Rail Sequencing

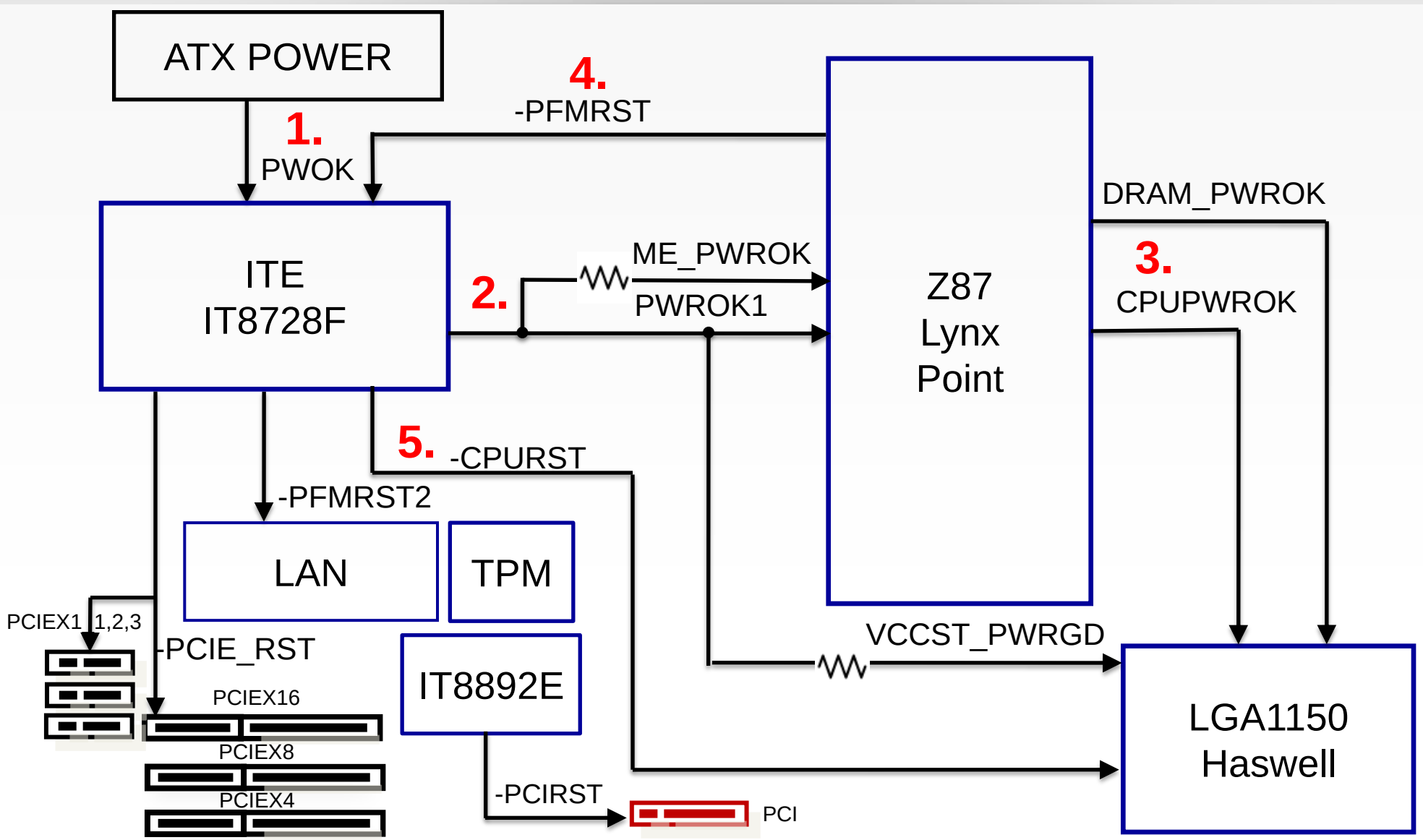
Source	Destination	Signal
VRs	CPU	VDDQ(1.5V)
VRs	CPU	VccST (VCC1_05_PCH)
VRs	CPU	VCCIN
Logic	CPU	VccST_PWRGD
Logic	PCH	PWROK



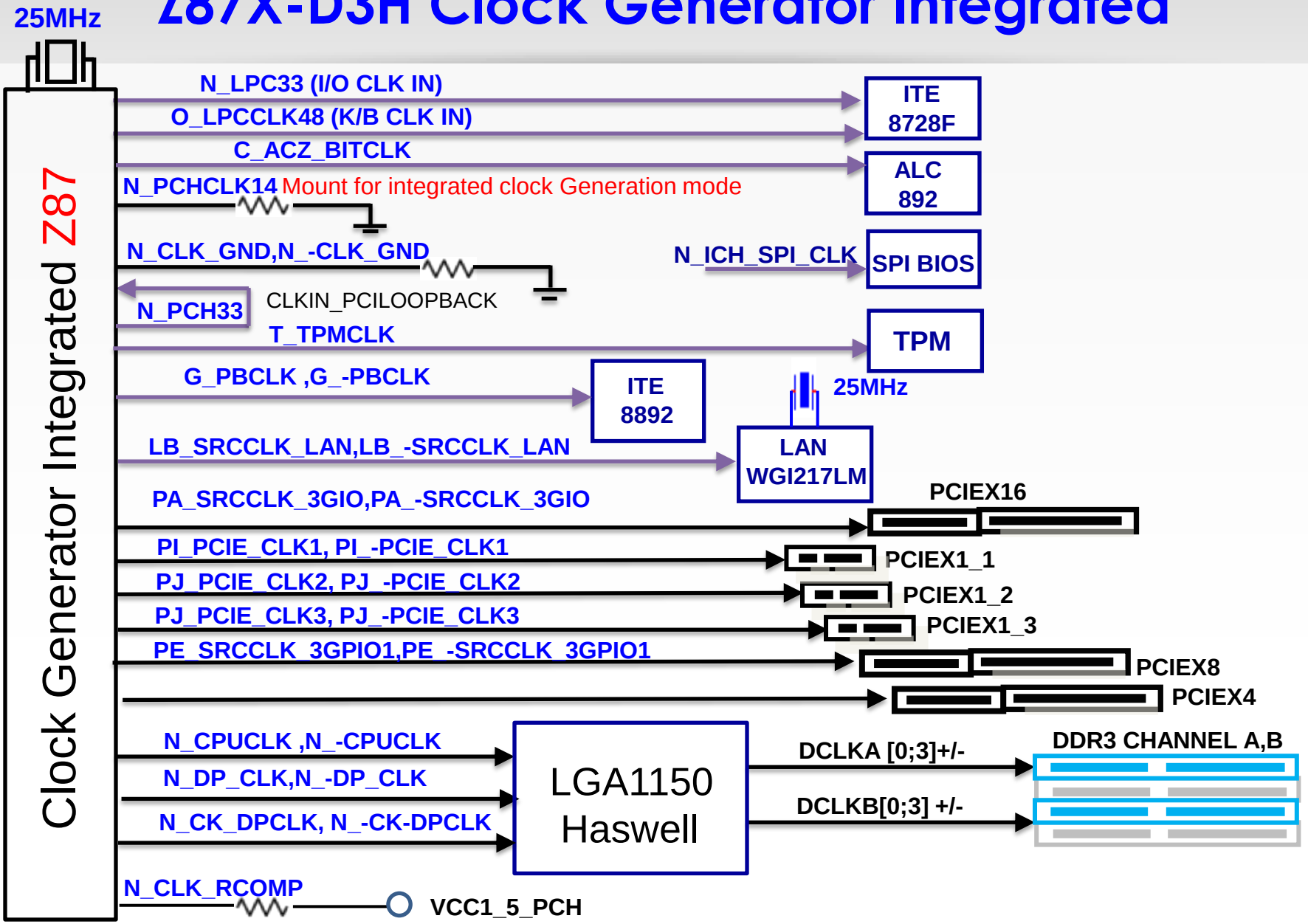
Z87X-D3H All Voltage Block Diagram



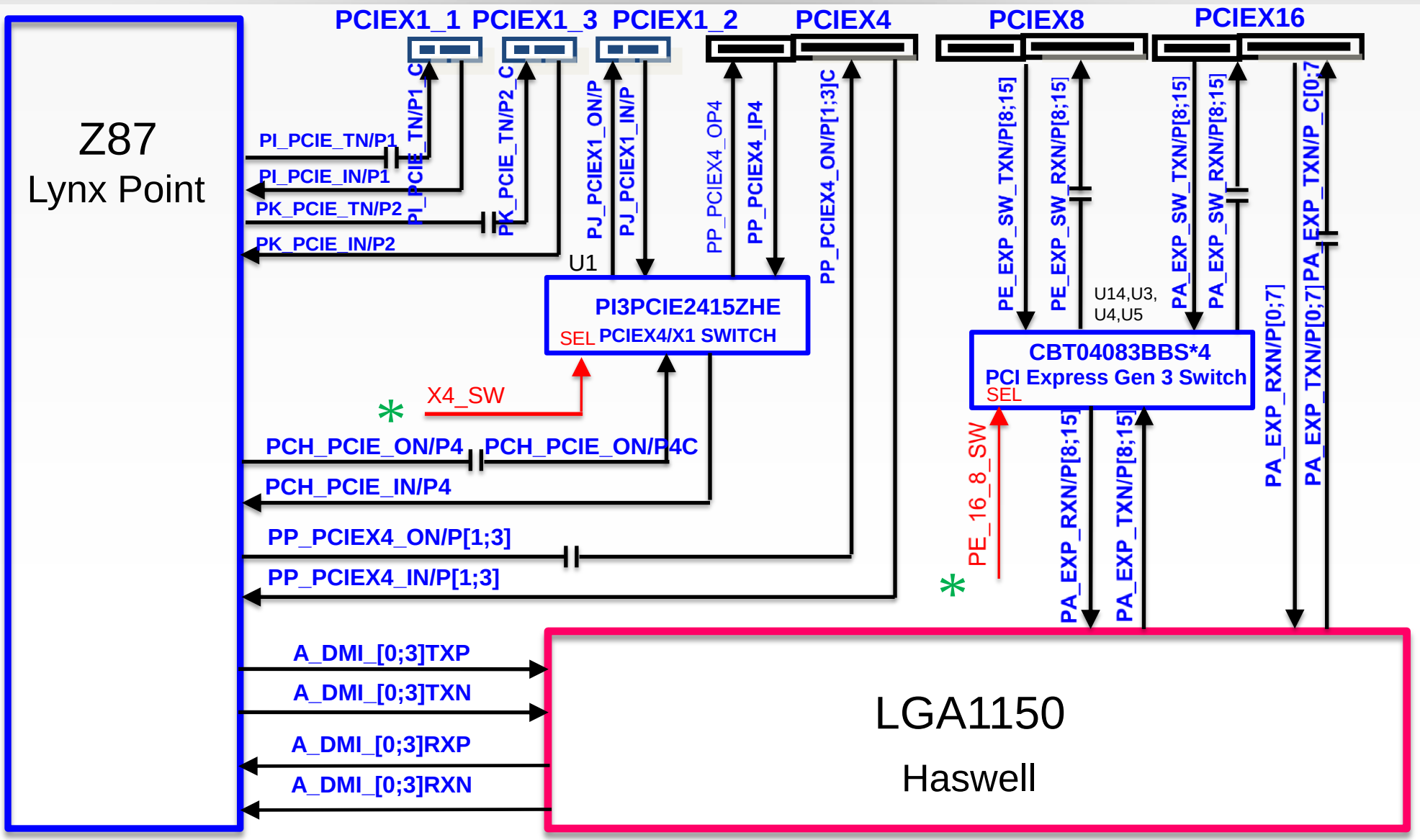
Z87X-D3H PWOK / RESET Block Diagram



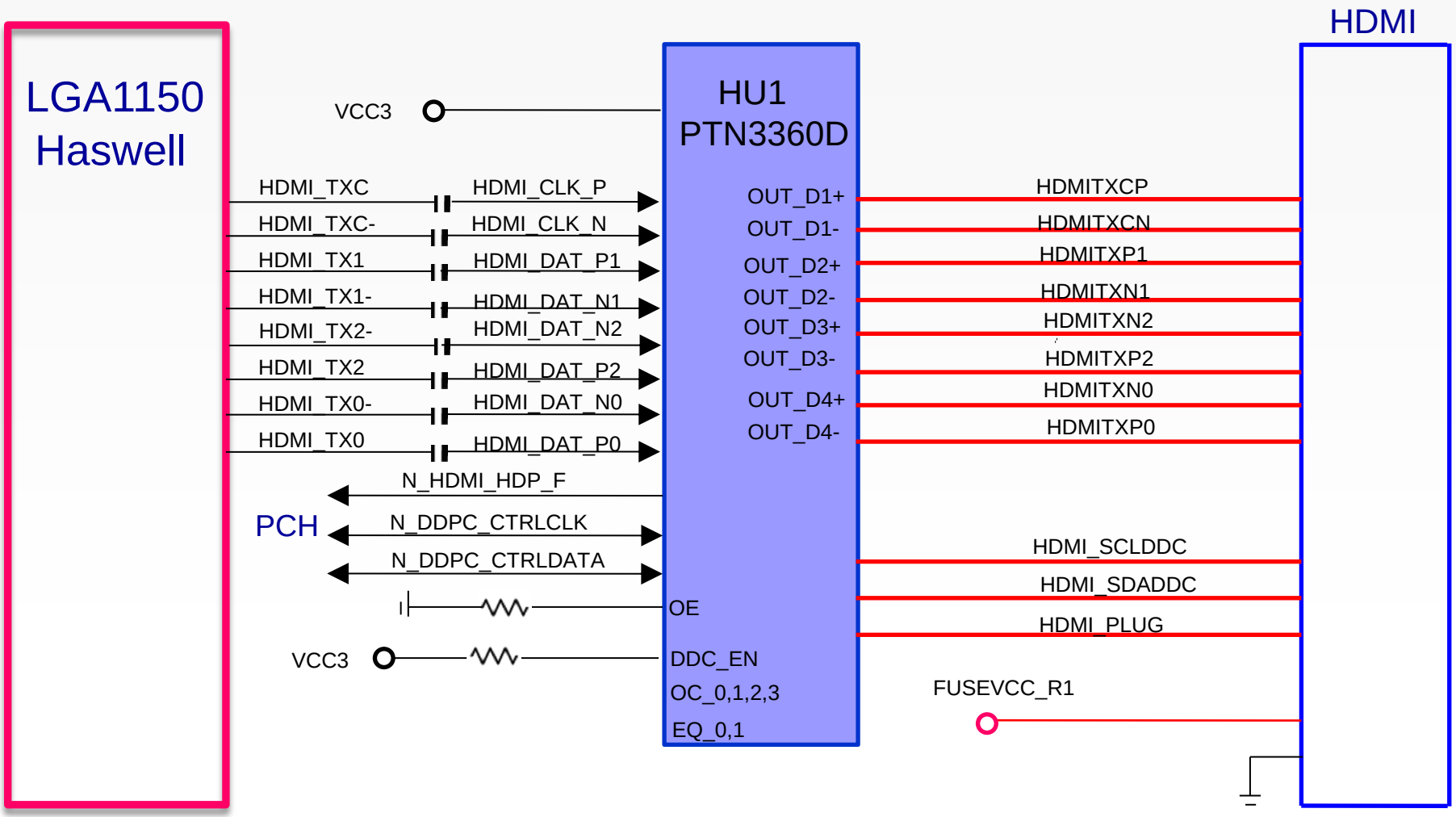
Z87X-D3H Clock Generator Integrated



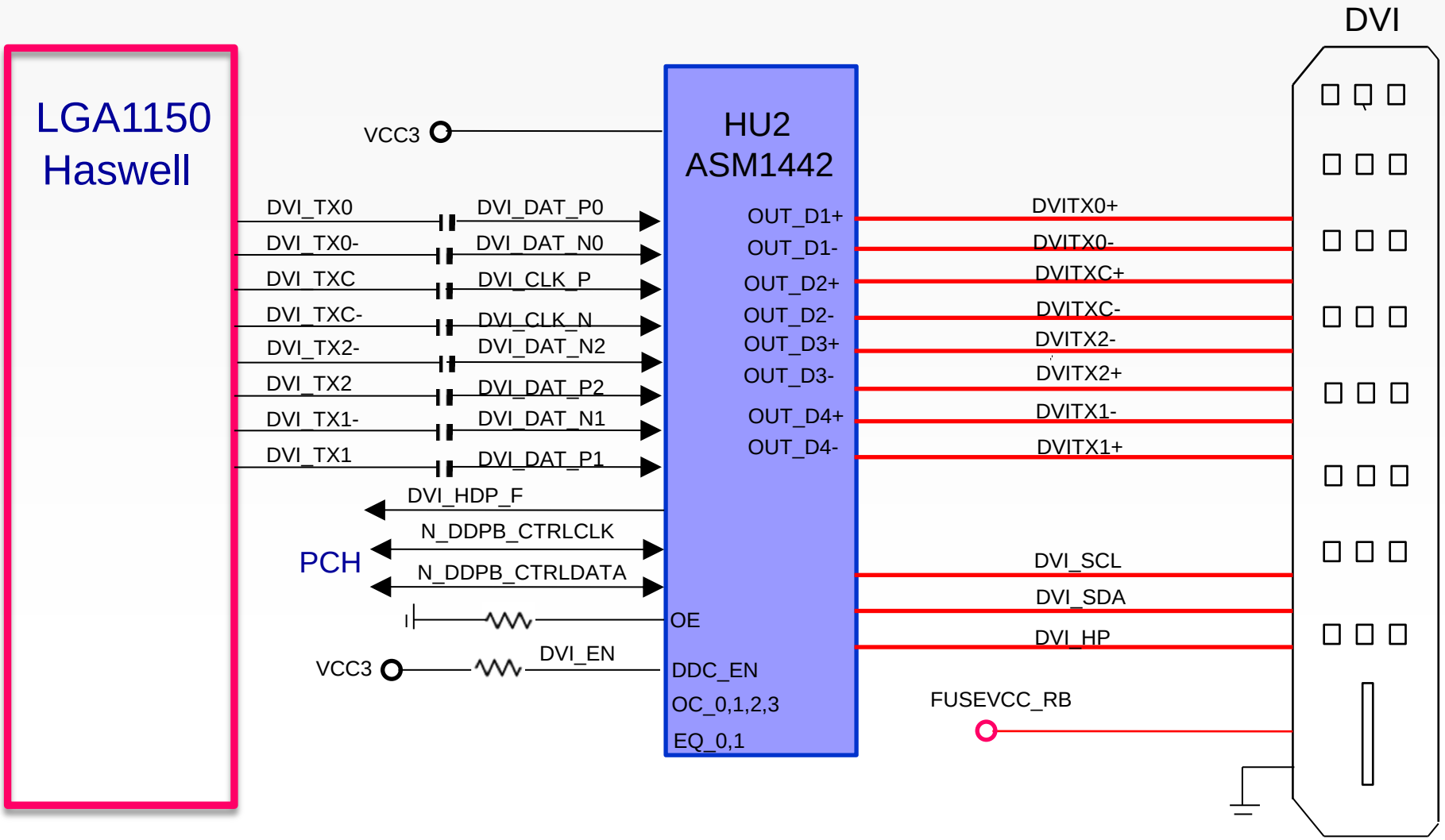
6 PCI Express Slot Connectivity Circuit



HDMI Block Diagram



DVI Block Diagram



VGA Block Diagram