

# GA-MA770T-UD3 *Revision : 3.1*

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# Model Name:GA-MA770T-UD3

## Component value change history

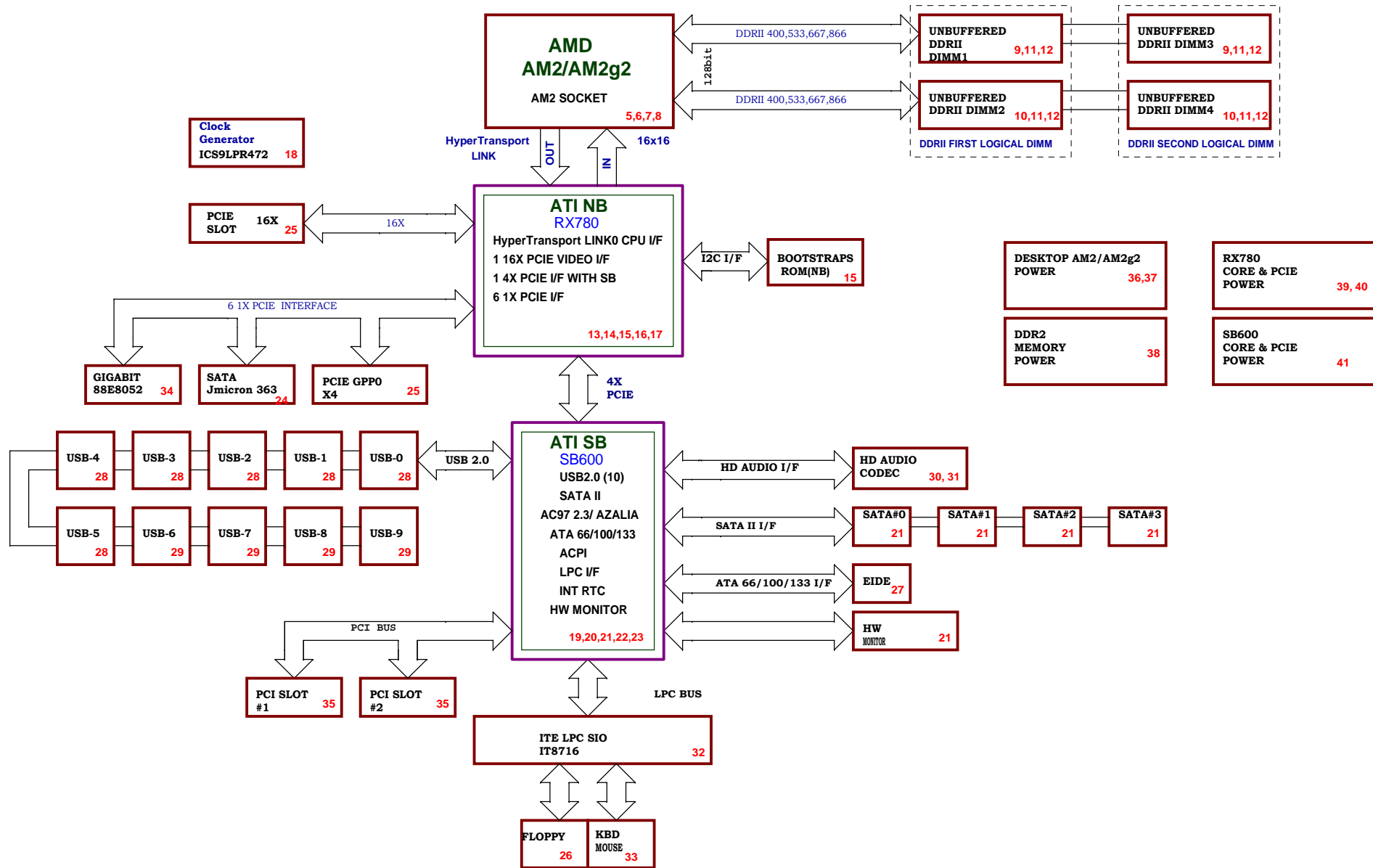
Date	Change Item	Reason
	1.0A	
2009.10.15	First PBOM release	
	1.1B	
2010.01.21	remove r3219	改善UPI6262被靜電打穿ISSUE
	1.1C	
2010.01.29	R3843 0/4 ==> 2.2/4	改善UPI6262被靜電打穿ISSUE
	1.3A	
2010.04.15	U149, U150 remove UPI7534	Support USB power 3X
	F1, F2 add SMD1812P350SLR/S	Support USB power 3X
	1.4A	
2010.06.09	CU1 ALC888 ==> ALC892 CR109, CR56 remove	change to Codec ALC892
	CBC42 Add 10u/8/X5R/6.3V/K CR55 Add 0/4	change to Codec ALC892
	LU3 RTL8111C ==> RTL8111D LR12, LR13 remove 150/6	change to LAN 81111D
	1.4B PBOM	
2010.06.18	U116, U124 change to NCT3931 R3485 0/4 ==> 2.2/4	For better reliability
	1.4C	
2010.06.22	Remove R2455 , Add R2457 8.2K/4	For up6262 change to NCT3931
	1.4C	
2010.08.18	Remove CR67 CD1 CD2 CQ4 , Add CR68 CD5 CBC43	change codec ALC892R TO ALC892
	1.5A	
2010.09.02	change LAN8111D==>8111E	
	3.1A	
2011.02.10	ADD R8,R9	
	3.1B	
2011.02.17	U196,U197 to 16M	

## Circuit or PCB layout change for next version

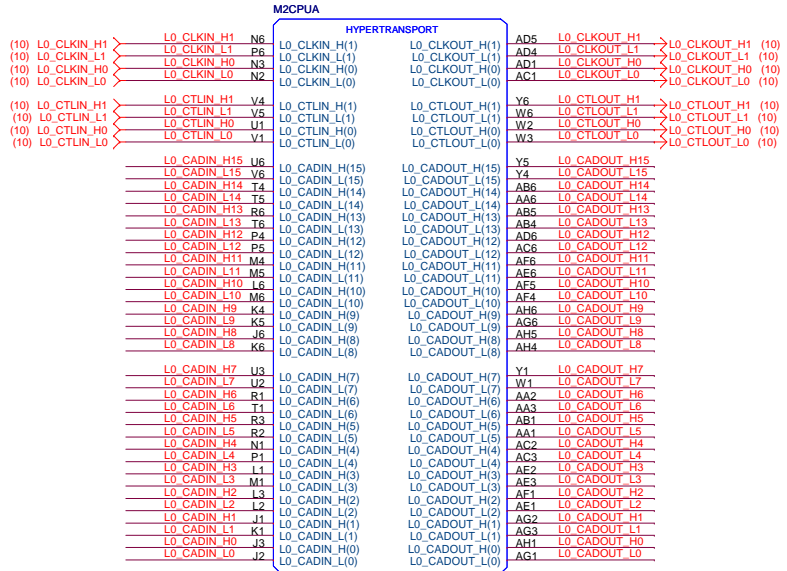
Date	Change Item	Reason
	1.01	
2009.10.08	Add ESD protect IC on SMBUS	
	1.1	
2009.12.08	Add EUP function	
	1.1B	
2010.01.21	remove DDRVTT over voltage	
	1.1C	
2010.01.29	fix UPI6262 burn issue	
	1.3	
2010.04.15	U149, U150 update footprint to MASK	Support USB power 3X
	Change silkscreen to 1.3	Support USB power 3X
	Change silkscreen EuP to ErP	
	1.4	
2010.06.09	only Change silkscreen to 1.4	Support ALC892 & 8111D
	1.5	
2010.09.02	change LAN8111D==>8111E	
	3.1	
2011.02.10	support AM3+	

<b>GIGABYTE™</b>		
Title <b>BOM &amp; PCB HISTORY</b>		
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# RX780 CUSTOMER DESKTOP REFERENCE DESIGN



L0\_CADIN\_L[0..15] < L0\_CADIN\_L[0..15] (10)  
 L0\_CADIN\_H[0..15] < L0\_CADIN\_H[0..15] (10)  
 L0\_CADOUT\_L[0..15] < L0\_CADOUT\_L[0..15] (10)  
 L0\_CADOUT\_H[0..15] < L0\_CADOUT\_H[0..15] (10)



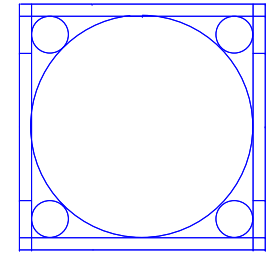
CPU-SK941AM3+/BK/S/GF/[10SC1-A01942-02R]

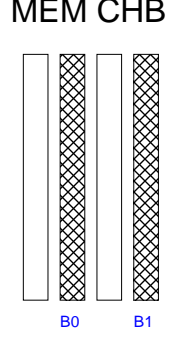
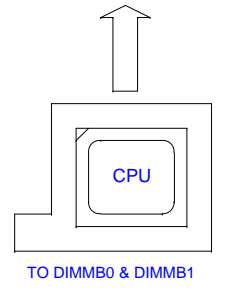
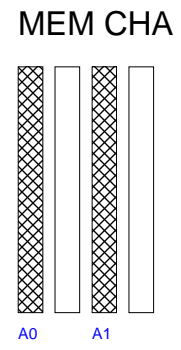
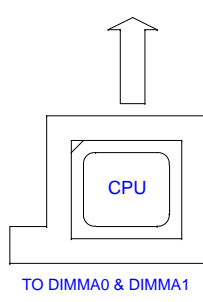
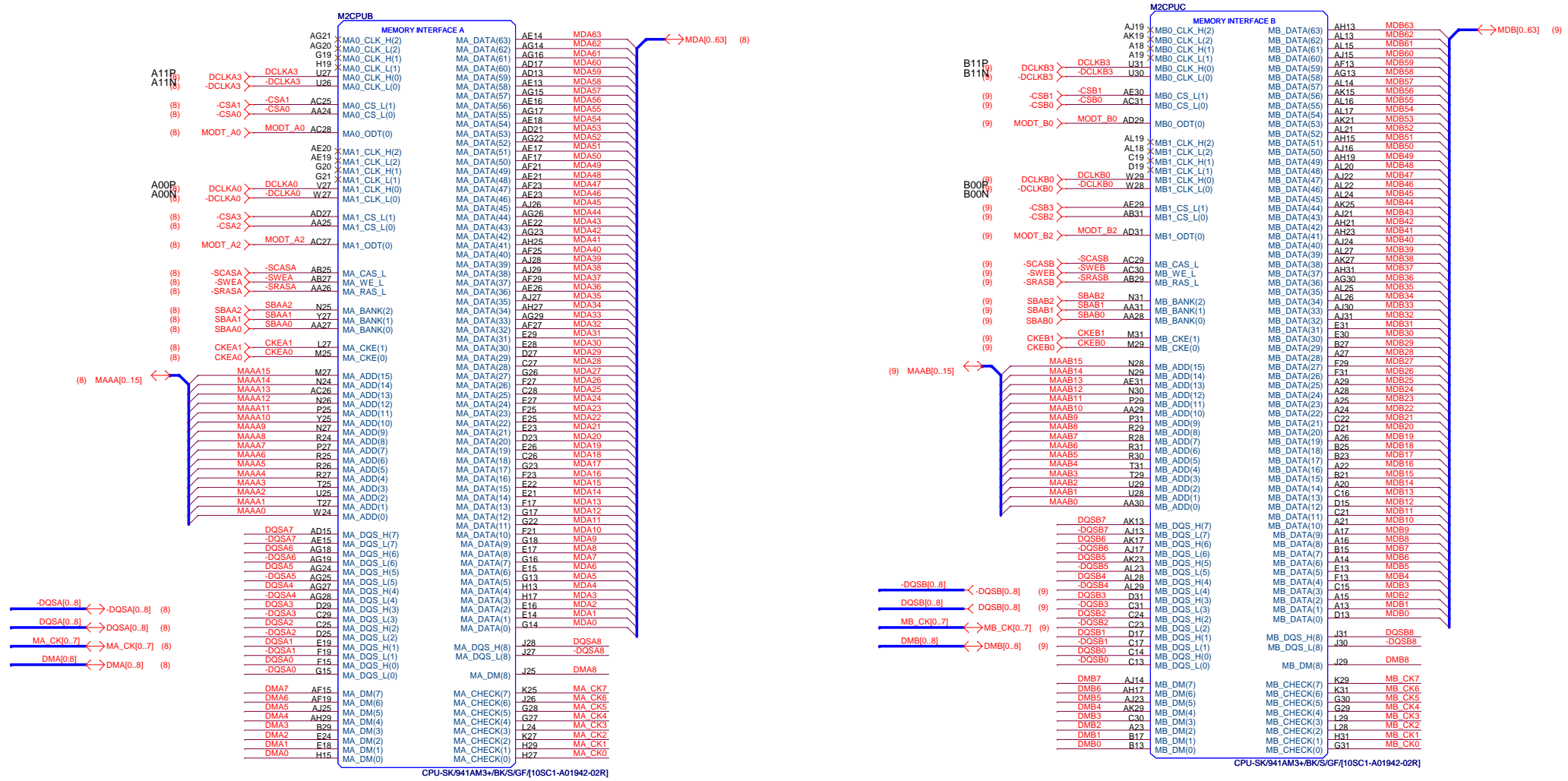
CPU\_VDD\_RUN = VCORE  
 CPU\_VDDA\_RUN = VDDA25  
 VLDT\_RUN = VCC12\_HT  
 CPU\_VDDIO\_SUS = DDR15V  
 CPU\_VDDR = CPU\_VDDR12

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VLDT\_A = VCC12\_HT  
 VLDT\_B = HT12B

M2CPU  
AM3RM/SC/BLMB





**GIGABYTE™**

**CPU DDRIII MEMORY**

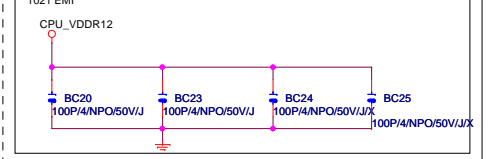
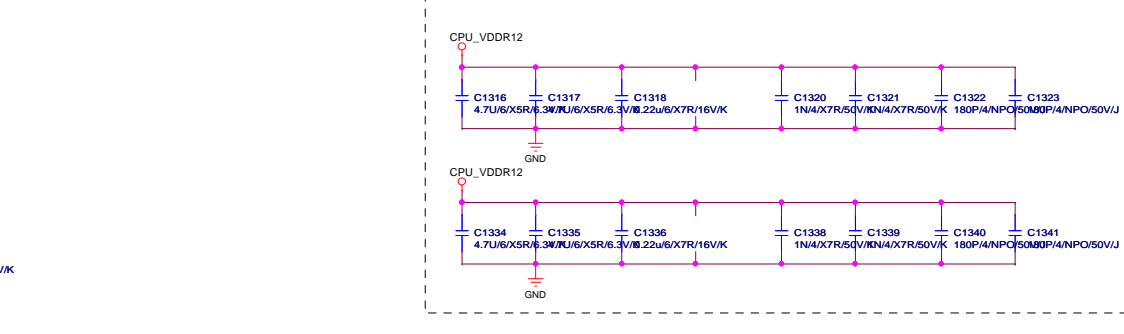
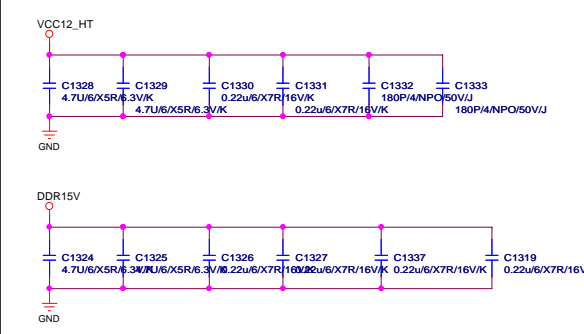
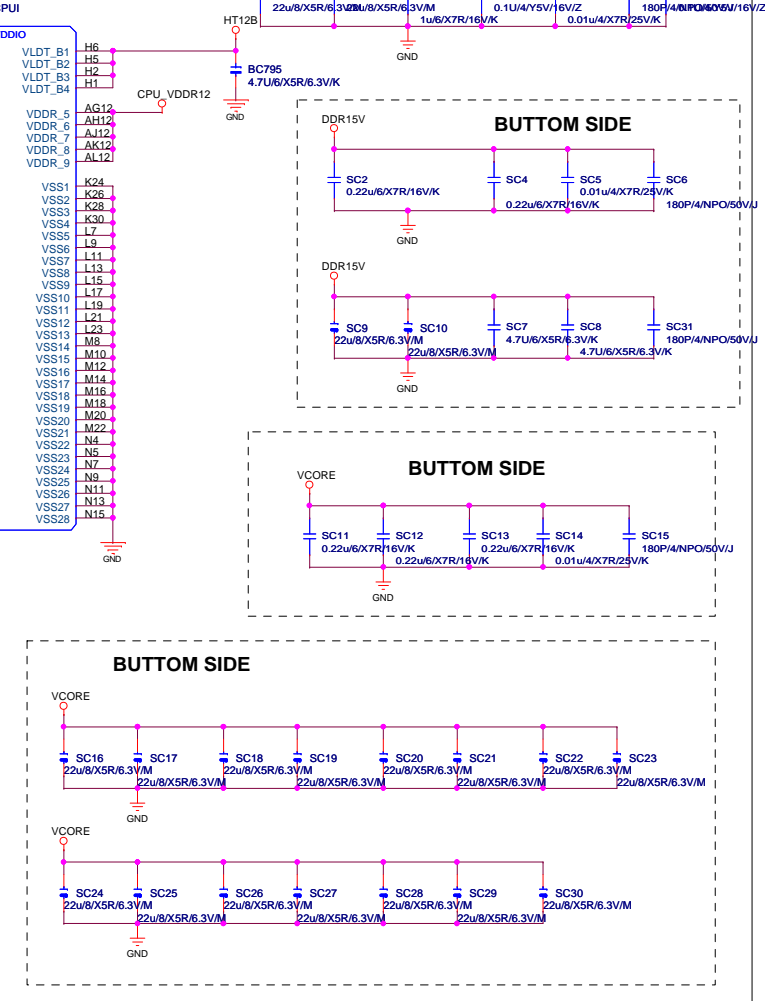
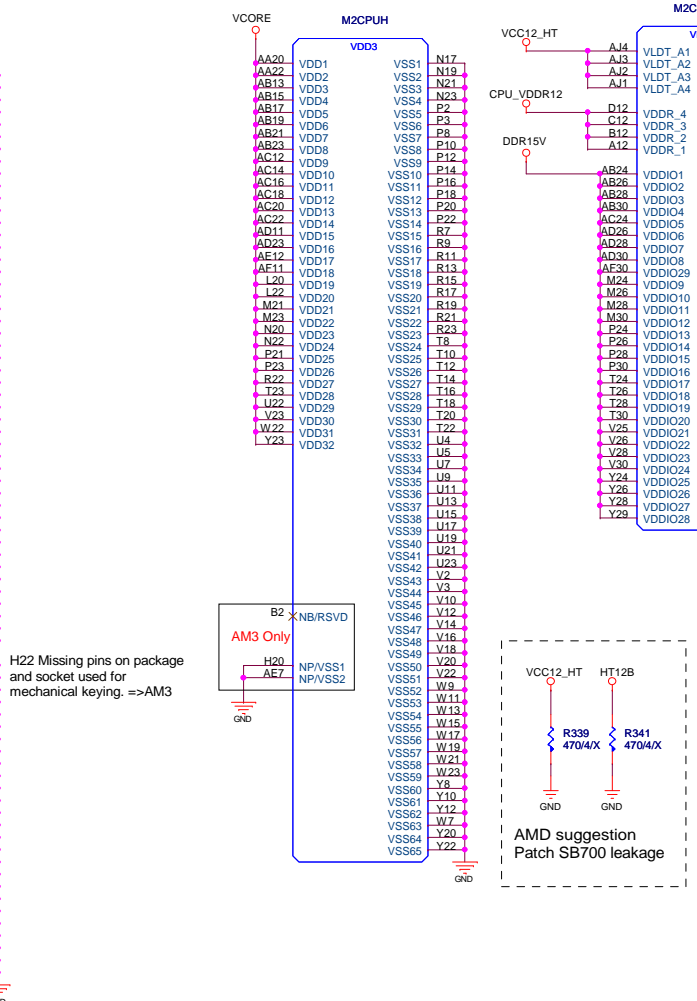
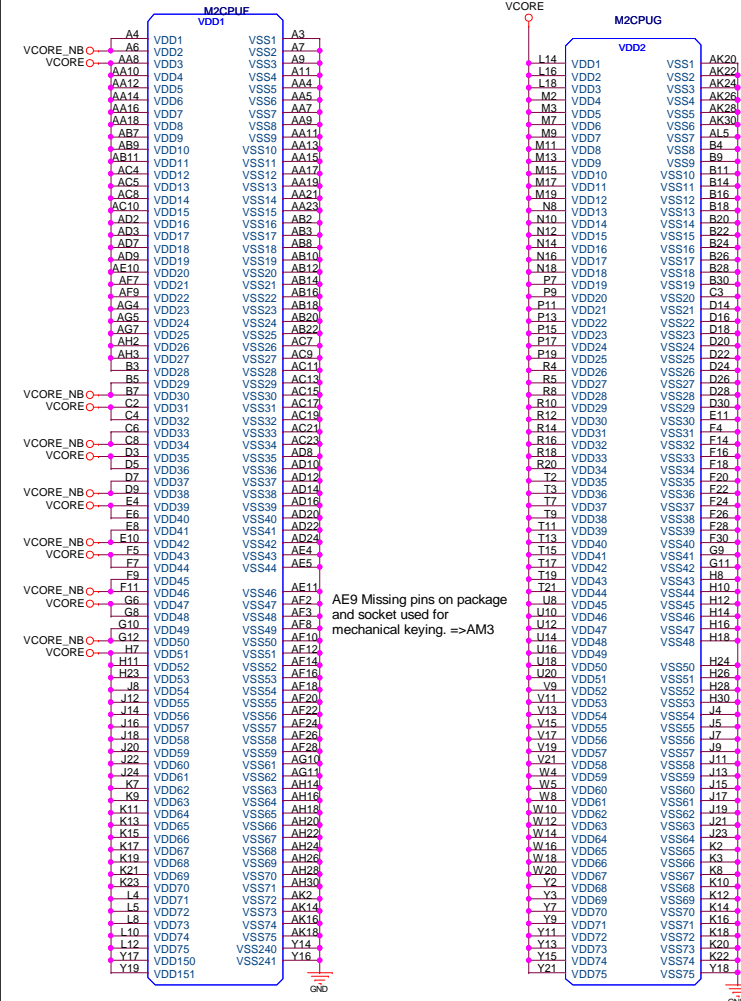
Title

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VLDT\_RUN\_B is connected to the VLDT\_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



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Title: **CPU POWER & GND**

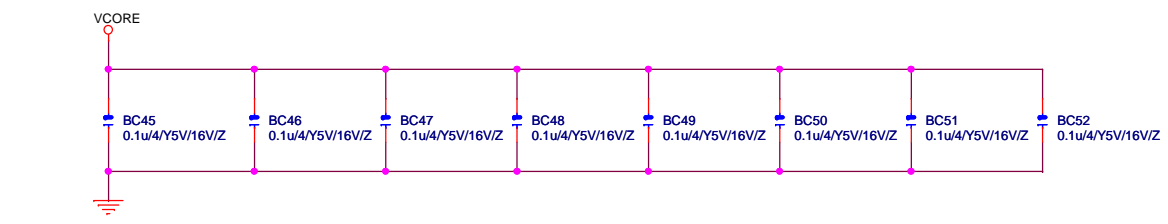
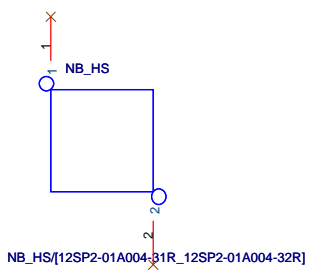
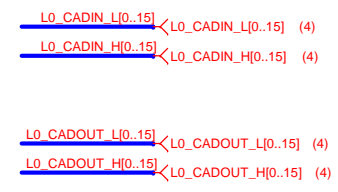
Size: Custom Document Number: **GA-MA770T-UD3** Rev: **3.1**

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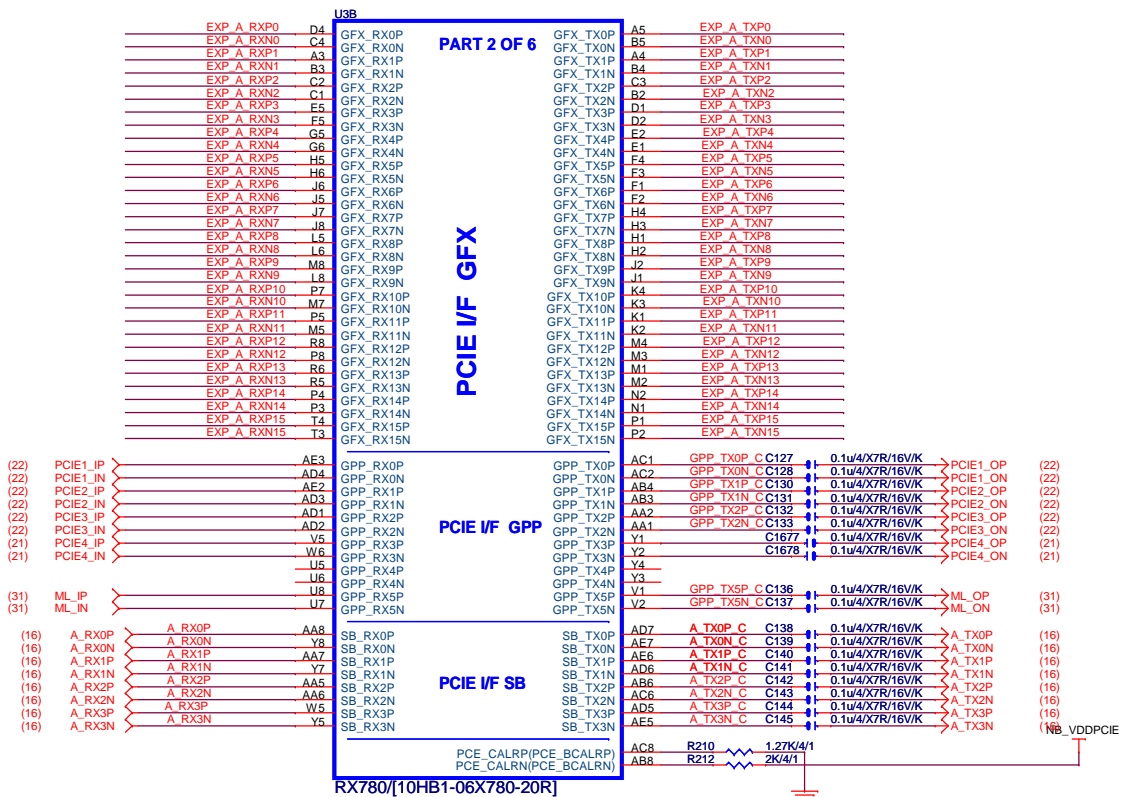


**GIGABYTE™**

Title: **RD780-HT LINK I/F**

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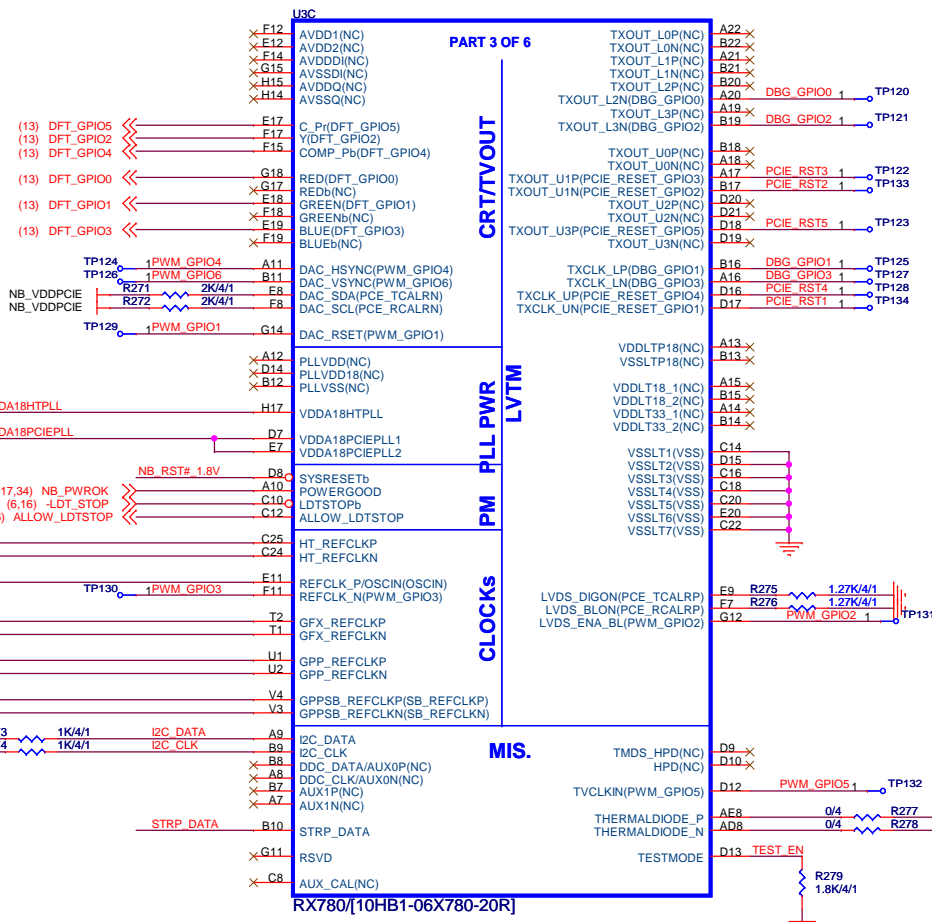
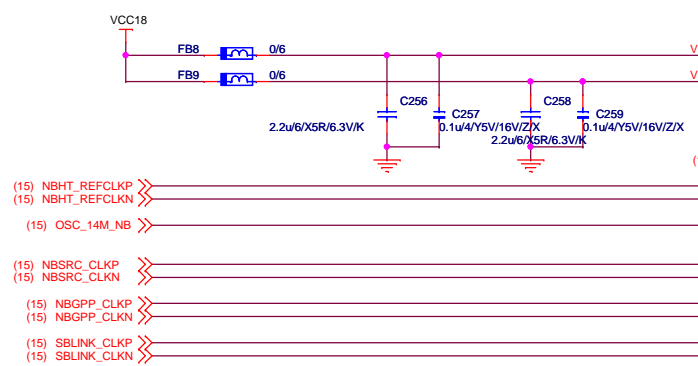
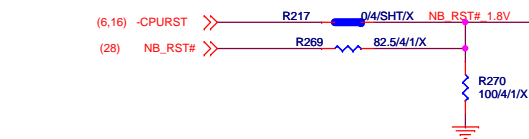


PLACE THESE CAP CLOSE TO CONNECTOR

**GIGABYTE™**

Title: **RD780-PCIE I/F**

Size: Custom	Document Number: <b>GA-MA770T-UD3</b>	Rev: <b>3.1</b>
Date: Thursday, March 17, 2011	Sheet: 11	of 39



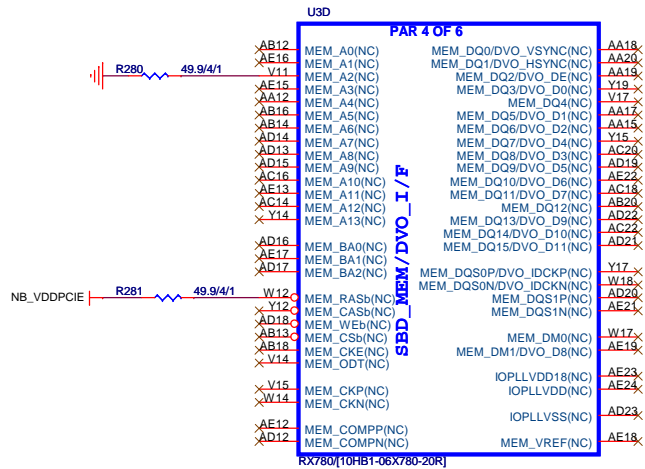
**NOTE: Provide access to STRAP\_DATA and I2C\_CLK is MANDATORY.**  
**DFT\_GPIO1 :**  
**1 : use Hardware Default Values**  
**0 : I2C Master can load strap values from EEPROM**

**GIGABYTE™**

Title: **RD780-SYSTEM I/F**

Size	Document Number	Rev
Custom	<b>GA-MA770T-UD3</b>	<b>3.1</b>

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**DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO.  
 1 : Disable ( Can still be enabled using nbcfg register access)  
 0 : Enable



**DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]**

These pin straps are used to configure PCI-E GPP mode.  
 000 : 00001  
 001 : 00010  
 010 : 01011  
 011 : 00100  
 100 : 01010  
 101 : 01100  
 111 : 01011



**DFT\_GPIO1: LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



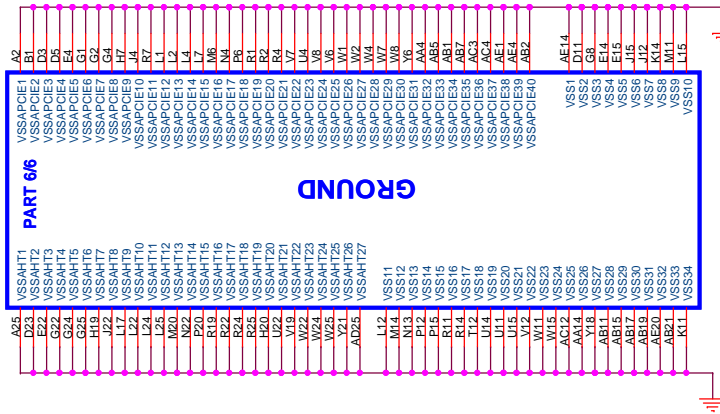
**DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb**

Enables the Test Debug Bus using PCIE bus  
 1 : Disable ( Can still be enabled using nbcfg register access )  
 0 : Enable

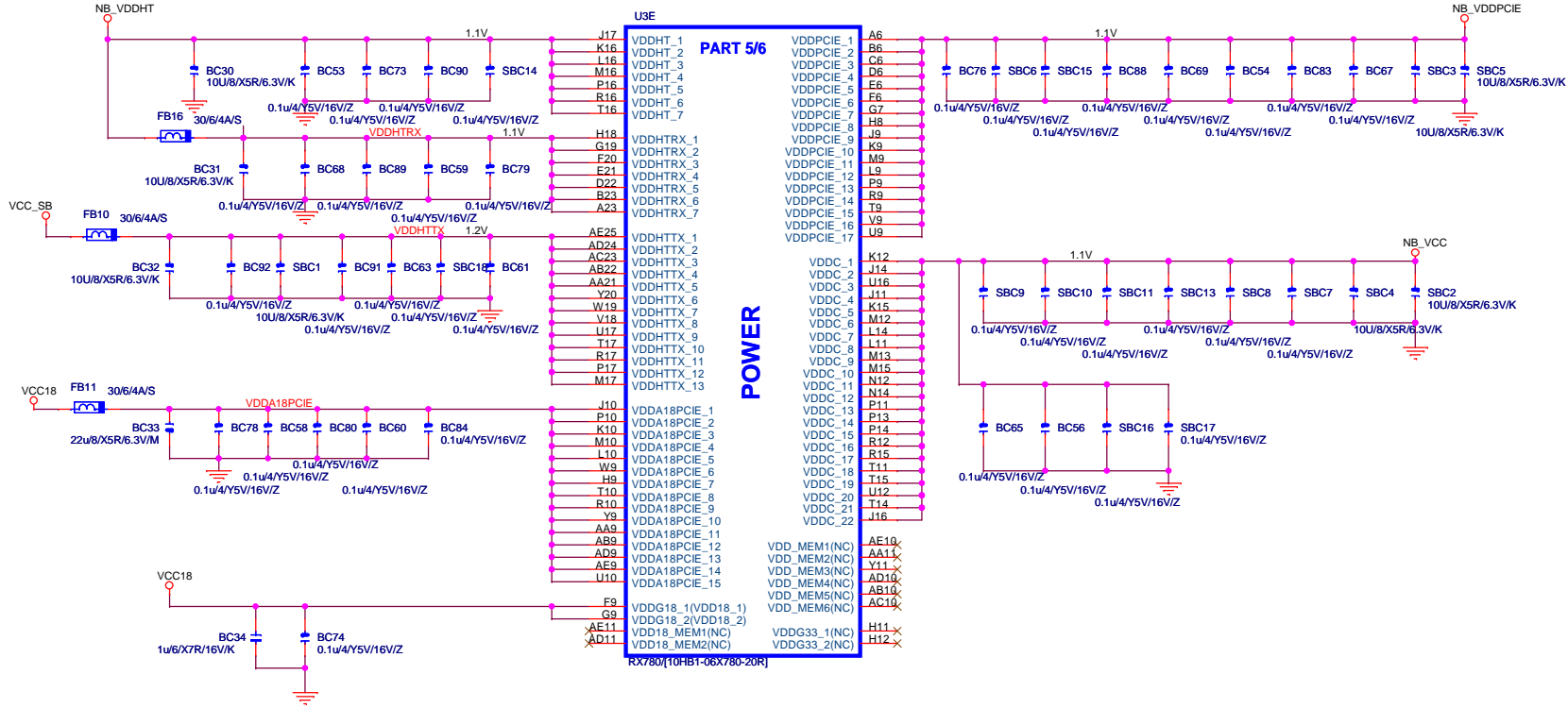
**GIGABYTE™**

Title			RD780 STRAP		
Size	Document Number				Rev
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U3F  
RX780(10HB1-06X780-20R)



Please use 1mm pad size,  
place all ELT test pads  
on bottom side only

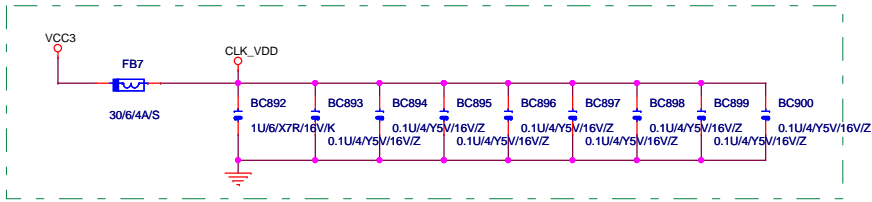


**GIGABYTE™**

Title: **RD780-POWER**

Size: Custom Document Number: **GA-MA770T-UD3** Rev: **3.1**

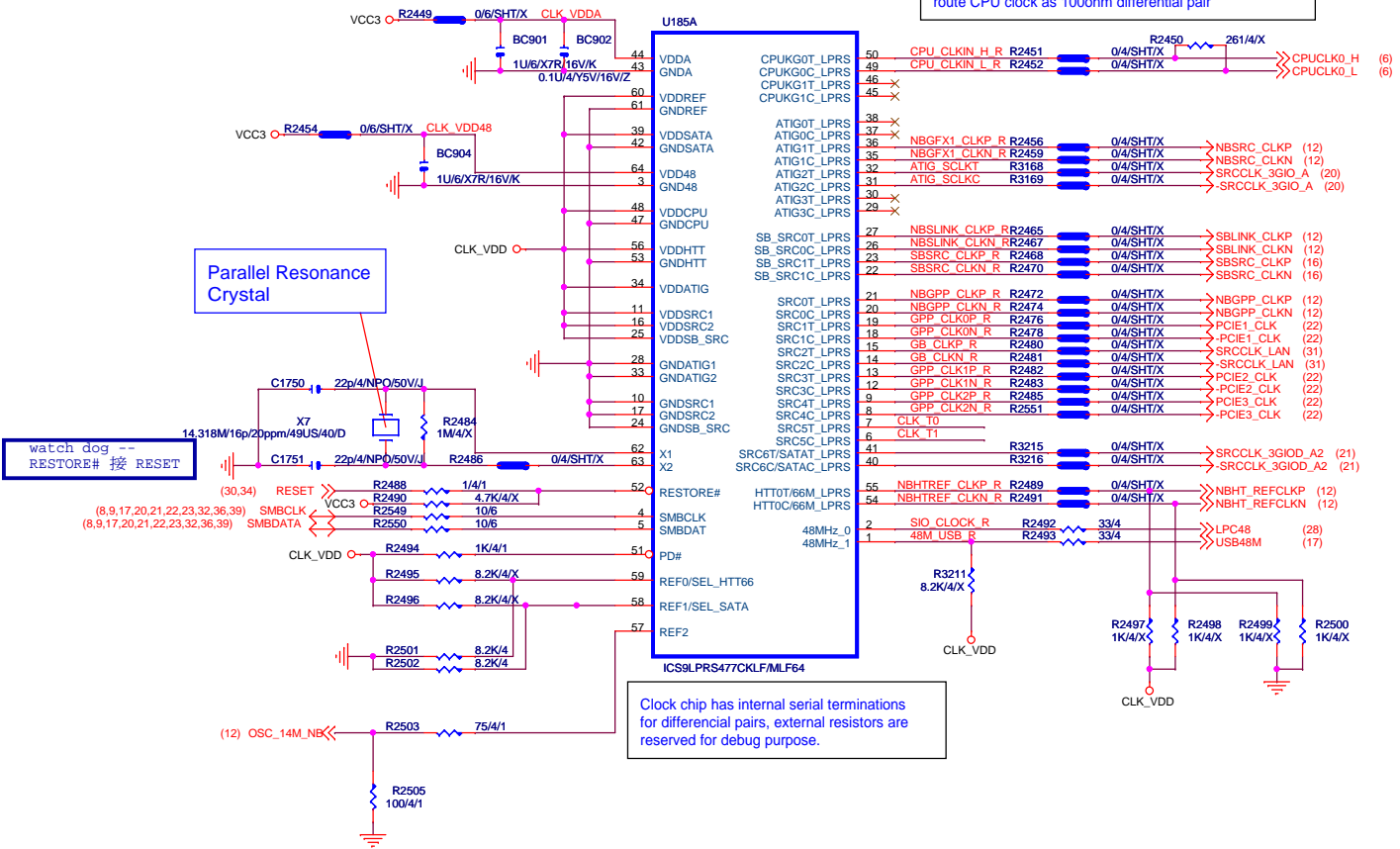
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- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



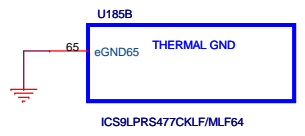
Place R800/801 less than 500 mils away from U800  
 R851 less than 100 mils away from R800/801  
 route CPU clock as 100ohm differential pair



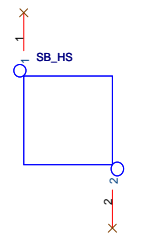
Parallel Resonance Crystal

watch dog -- RESTORE# 接 RESET

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

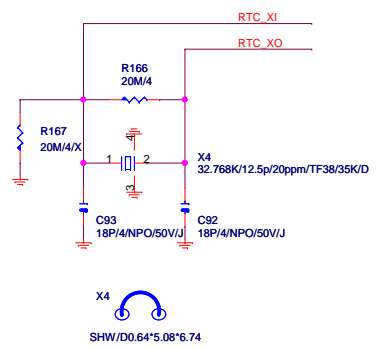


**S.B HEATSINK**

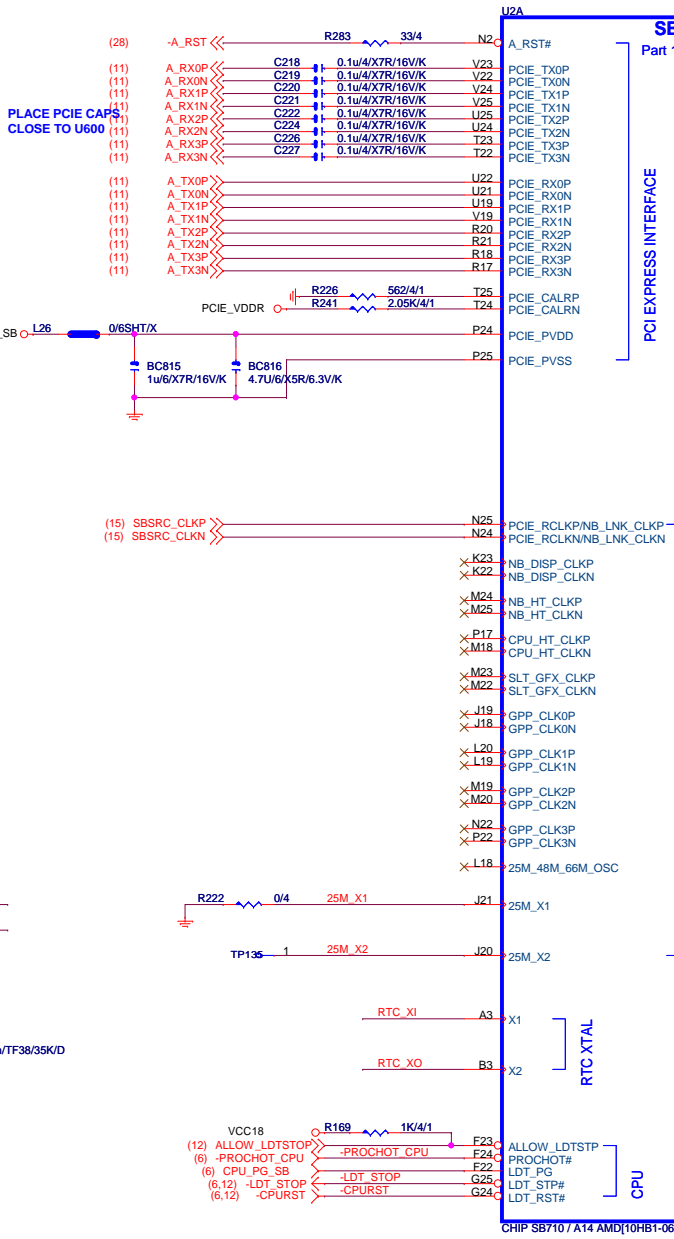


SB\_HS[12SP2-030005-42R\_12SP2-030005-43R]

B



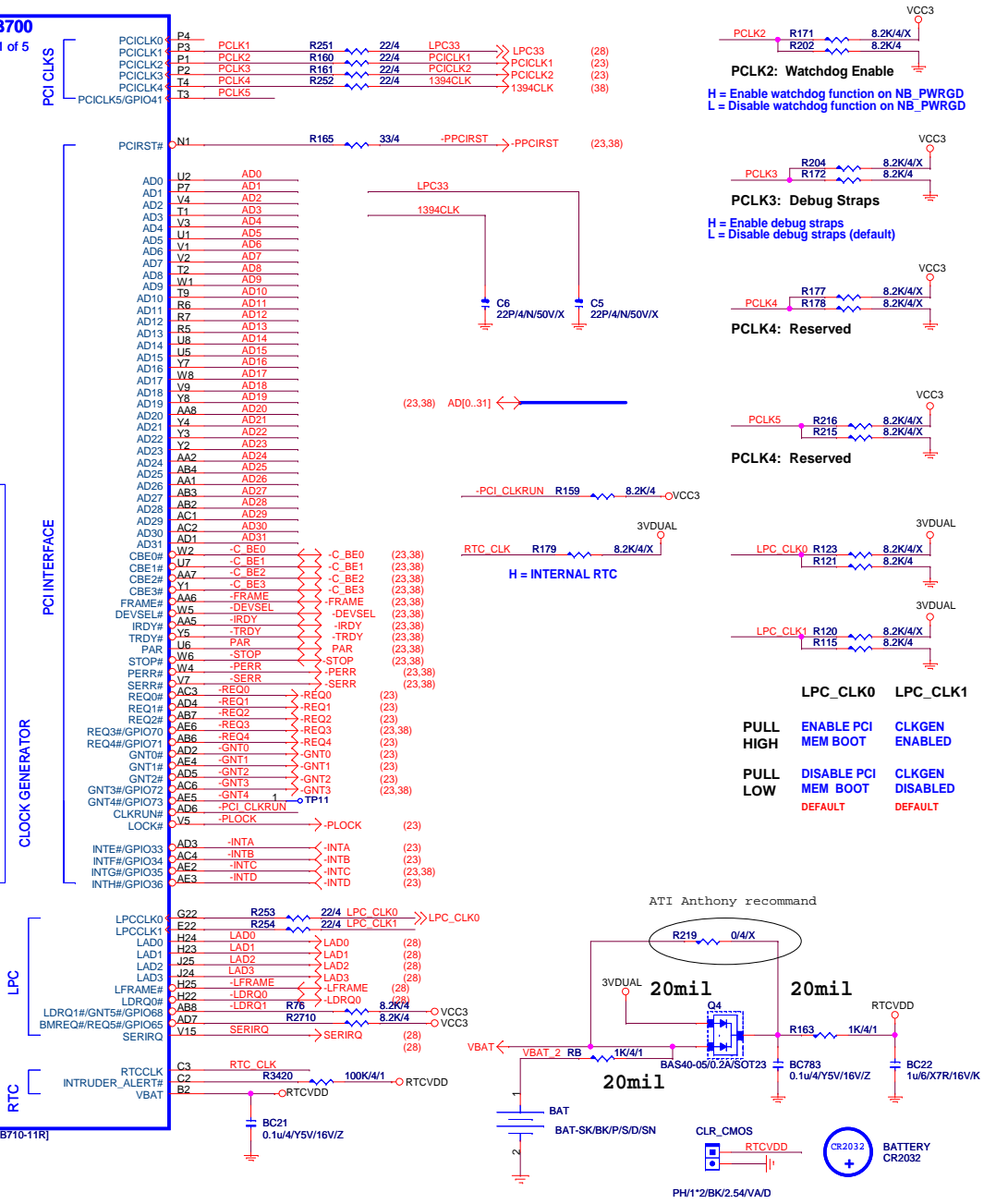
SHW/D0.64\*5.08\*6.74



CHIP SB710/A14 AMD(10HB1-06B710-11R)

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN



**PCLK2: Watchdog Enable**  
 H = Enable watchdog function on NB\_PWRGD  
 L = Disable watchdog function on NB\_PWRGD

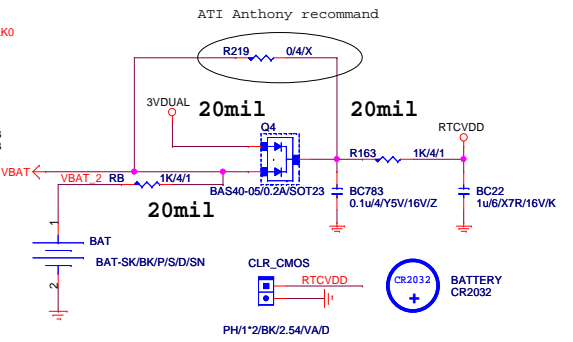
**PCLK3: Debug Straps**  
 H = Enable debug straps  
 L = Disable debug straps (default)

**PCLK4: Reserved**

**PCLK4: Reserved**

**H = INTERNAL RTC**

**LPC\_CLK0**    **LPC\_CLK1**  
 PULL HIGH    ENABLE PCI    CLKGEN ENABLED  
 PULL LOW    DISABLE PCI    CLKGEN DISABLED  
 DEFAULT    DEFAULT    DEFAULT



**GIGABYTE™**

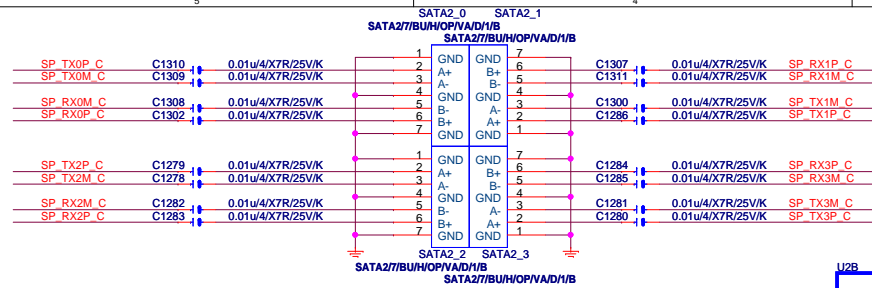
Title: **ATI SB600-PCIW/PCI/CPU/LPC**

Size: Custom	Document Number: <b>GA-MA770T-UD3</b>	Rev: <b>3.1</b>
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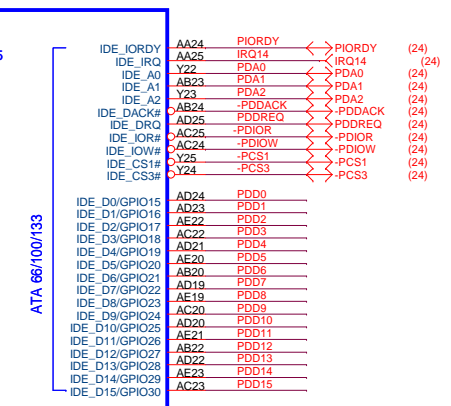
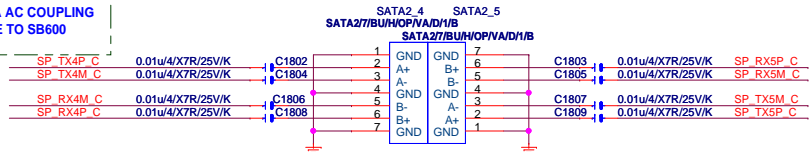
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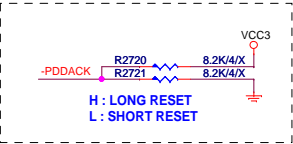
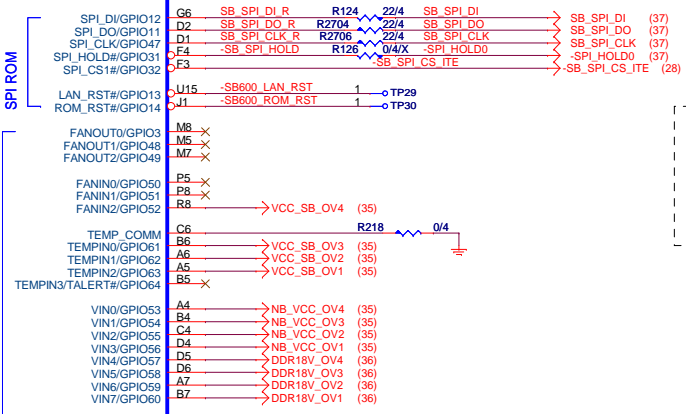
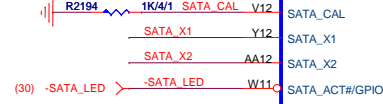
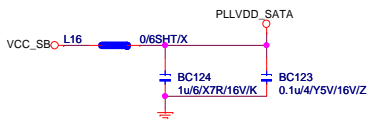
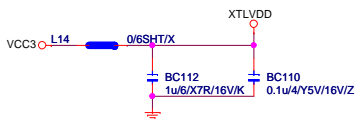
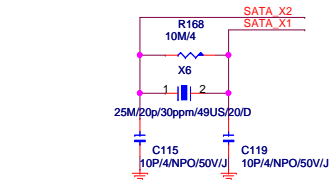




PLACE SATA AC COUPLING CAPS CLOSE TO SB600




NOTE: ROUTE TEMP\_COMM AS A 10MIL TRACE

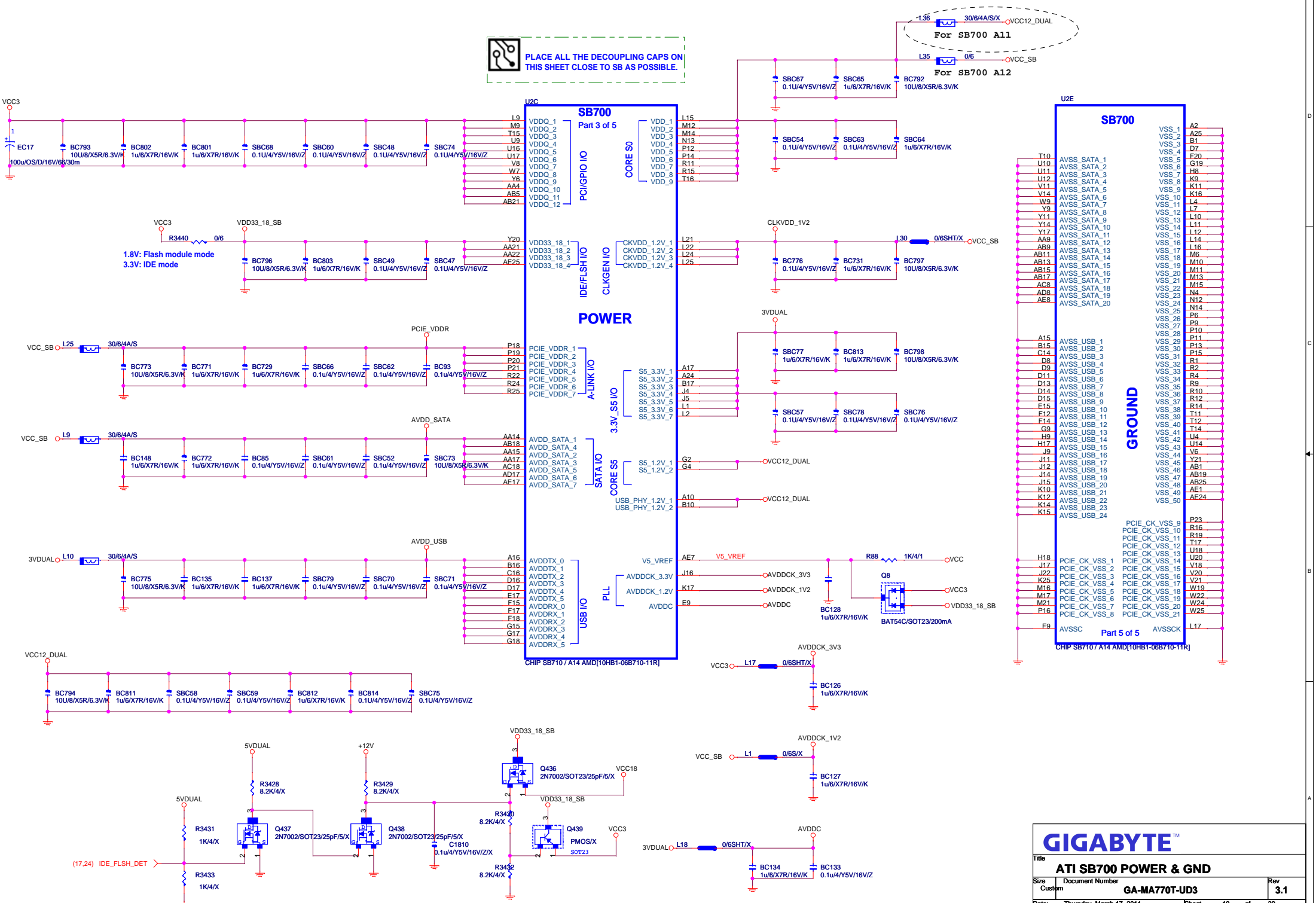


Special NS\_VIA CONNECTS HWM\_AGND TO GND at VIA hole only

CHIP SB710 / A14 AMD[10HB1-06B710-11R]

 **PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.**

**For SB700 A11**  
**For SB700 A12**



**SB700**

T10	AVSS_SATA_1	A2	VSS_1
U11	AVSS_SATA_2	A1	VSS_2
U12	AVSS_SATA_3	B1	VSS_3
U13	AVSS_SATA_4	B2	VSS_4
V11	AVSS_SATA_5	D7	VSS_5
V14	AVSS_SATA_6	F20	VSS_6
V15	AVSS_SATA_7	H8	VSS_7
Y11	AVSS_SATA_8	K9	VSS_8
Y14	AVSS_SATA_9	K11	VSS_9
Y17	AVSS_SATA_10	K16	VSS_10
Y9	AVSS_SATA_11	L4	VSS_11
Y11	AVSS_SATA_12	L7	VSS_12
Y14	AVSS_SATA_13	L10	VSS_13
Y17	AVSS_SATA_14	L11	VSS_14
AB9	AVSS_SATA_15	L12	VSS_15
AB11	AVSS_SATA_16	L16	VSS_16
AB13	AVSS_SATA_17	M6	VSS_17
AB15	AVSS_SATA_18	M10	VSS_18
AB17	AVSS_SATA_19	M11	VSS_19
AB19	AVSS_SATA_20	M13	VSS_20
AD8	AVSS_SATA_1	N4	VSS_21
AE8	AVSS_SATA_2	N12	VSS_22
		N14	VSS_23
		N14	VSS_24
		N14	VSS_25
		N14	VSS_26
		N14	VSS_27
		N14	VSS_28
		N14	VSS_29
		N14	VSS_30
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		N14	VSS_35
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		N14	VSS_95
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		N14	VSS_99
		N14	VSS_100

**GROUND**

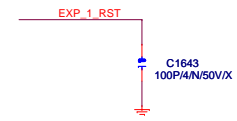
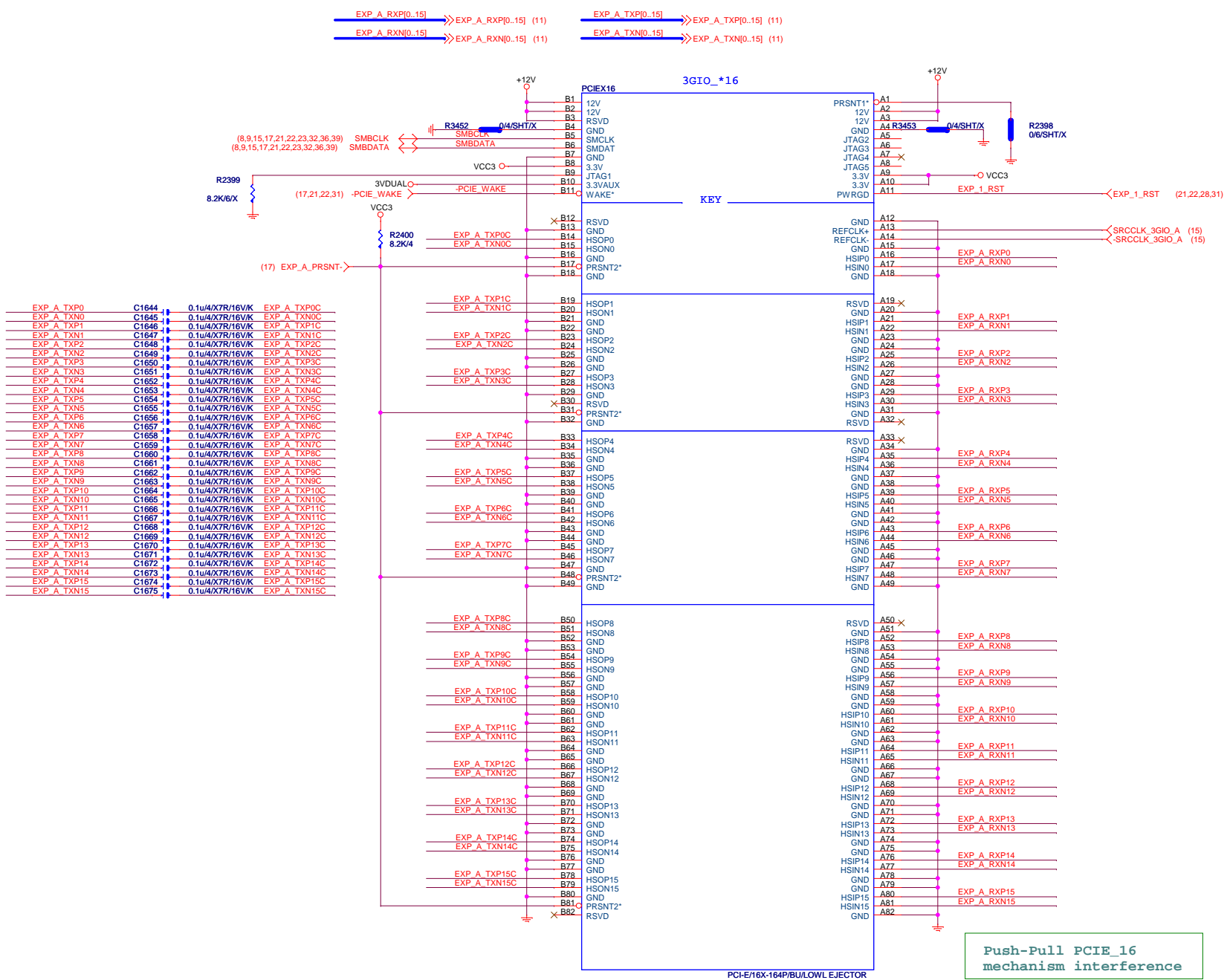
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D8	AVSS_USB_4	T17	PCIE_CK_VSS_12
D9	AVSS_USB_5	U18	PCIE_CK_VSS_13
D11	AVSS_USB_6	V18	PCIE_CK_VSS_14
D13	AVSS_USB_7	V20	PCIE_CK_VSS_15
D14	AVSS_USB_8	W19	PCIE_CK_VSS_16
D15	AVSS_USB_9	W21	PCIE_CK_VSS_17
E15	AVSS_USB_10	W22	PCIE_CK_VSS_18
F12	AVSS_USB_11	W25	PCIE_CK_VSS_19
F14	AVSS_USB_12	W25	PCIE_CK_VSS_20
G9	AVSS_USB_13	W25	PCIE_CK_VSS_21
H9	AVSS_USB_14	W25	PCIE_CK_VSS_22
H17	AVSS_USB_15	W25	PCIE_CK_VSS_23
J9	AVSS_USB_16	W25	PCIE_CK_VSS_24
J11	AVSS_USB_17	W25	PCIE_CK_VSS_25
J12	AVSS_USB_18	W25	PCIE_CK_VSS_26
J14	AVSS_USB_19	W25	PCIE_CK_VSS_27
J15	AVSS_USB_20	W25	PCIE_CK_VSS_28
K10	AVSS_USB_21	W25	PCIE_CK_VSS_29
K12	AVSS_USB_22	W25	PCIE_CK_VSS_30
K14	AVSS_USB_23	W25	PCIE_CK_VSS_31
K15	AVSS_USB_24	W25	PCIE_CK_VSS_32
H18	PCIE_CK_VSS_1	P23	PCIE_CK_VSS_1
J17	PCIE_CK_VSS_2	R16	PCIE_CK_VSS_2
K22	PCIE_CK_VSS_3	R19	PCIE_CK_VSS_3
K25	PCIE_CK_VSS_4	T17	PCIE_CK_VSS_4
M16	PCIE_CK_VSS_5	U18	PCIE_CK_VSS_5
M17	PCIE_CK_VSS_6	V18	PCIE_CK_VSS_6
M21	PCIE_CK_VSS_7	V20	PCIE_CK_VSS_7
M21	PCIE_CK_VSS_8	W19	PCIE_CK_VSS_8
P16	PCIE_CK_VSS_9	W21	PCIE_CK_VSS_9
F9	AVSSCC	W22	PCIE_CK_VSS_10
		W25	PCIE_CK_VSS_11
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CHIP SB710 / A14 AMD[10HB1-06B710-11R]

**GIGABYTE**

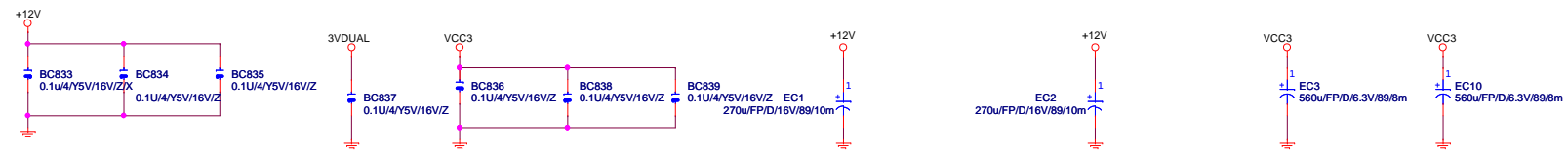
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Size: Custom	Document Number: <b>GA-MA770-UD3</b>	Rev: <b>3.1</b>
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EXP_A_TXP0	C1644	0.1u/4X7R/16VK	EXP_A_TXP0C
EXP_A_TXN0	C1645	0.1u/4X7R/16VK	EXP_A_TXN0C
EXP_A_TXP1	C1646	0.1u/4X7R/16VK	EXP_A_TXP1C
EXP_A_TXN1	C1647	0.1u/4X7R/16VK	EXP_A_TXN1C
EXP_A_TXP2	C1648	0.1u/4X7R/16VK	EXP_A_TXP2C
EXP_A_TXN2	C1649	0.1u/4X7R/16VK	EXP_A_TXN2C
EXP_A_TXP3	C1650	0.1u/4X7R/16VK	EXP_A_TXP3C
EXP_A_TXN3	C1651	0.1u/4X7R/16VK	EXP_A_TXN3C
EXP_A_TXP4	C1652	0.1u/4X7R/16VK	EXP_A_TXP4C
EXP_A_TXN4	C1653	0.1u/4X7R/16VK	EXP_A_TXN4C
EXP_A_TXP5	C1654	0.1u/4X7R/16VK	EXP_A_TXP5C
EXP_A_TXN5	C1655	0.1u/4X7R/16VK	EXP_A_TXN5C
EXP_A_TXP6	C1656	0.1u/4X7R/16VK	EXP_A_TXP6C
EXP_A_TXN6	C1657	0.1u/4X7R/16VK	EXP_A_TXN6C
EXP_A_TXP7	C1658	0.1u/4X7R/16VK	EXP_A_TXP7C
EXP_A_TXN7	C1659	0.1u/4X7R/16VK	EXP_A_TXN7C
EXP_A_TXP8	C1660	0.1u/4X7R/16VK	EXP_A_TXP8C
EXP_A_TXN8	C1661	0.1u/4X7R/16VK	EXP_A_TXN8C
EXP_A_TXP9	C1662	0.1u/4X7R/16VK	EXP_A_TXP9C
EXP_A_TXN9	C1663	0.1u/4X7R/16VK	EXP_A_TXN9C
EXP_A_TXP10	C1664	0.1u/4X7R/16VK	EXP_A_TXP10C
EXP_A_TXN10	C1665	0.1u/4X7R/16VK	EXP_A_TXN10C
EXP_A_TXP11	C1666	0.1u/4X7R/16VK	EXP_A_TXP11C
EXP_A_TXN11	C1667	0.1u/4X7R/16VK	EXP_A_TXN11C
EXP_A_TXP12	C1668	0.1u/4X7R/16VK	EXP_A_TXP12C
EXP_A_TXN12	C1669	0.1u/4X7R/16VK	EXP_A_TXN12C
EXP_A_TXP13	C1670	0.1u/4X7R/16VK	EXP_A_TXP13C
EXP_A_TXN13	C1671	0.1u/4X7R/16VK	EXP_A_TXN13C
EXP_A_TXP14	C1672	0.1u/4X7R/16VK	EXP_A_TXP14C
EXP_A_TXN14	C1673	0.1u/4X7R/16VK	EXP_A_TXN14C
EXP_A_TXP15	C1674	0.1u/4X7R/16VK	EXP_A_TXP15C
EXP_A_TXN15	C1675	0.1u/4X7R/16VK	EXP_A_TXN15C

Push-Pull PCIE\_16 mechanism interference

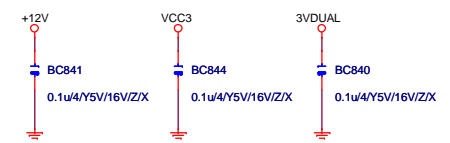
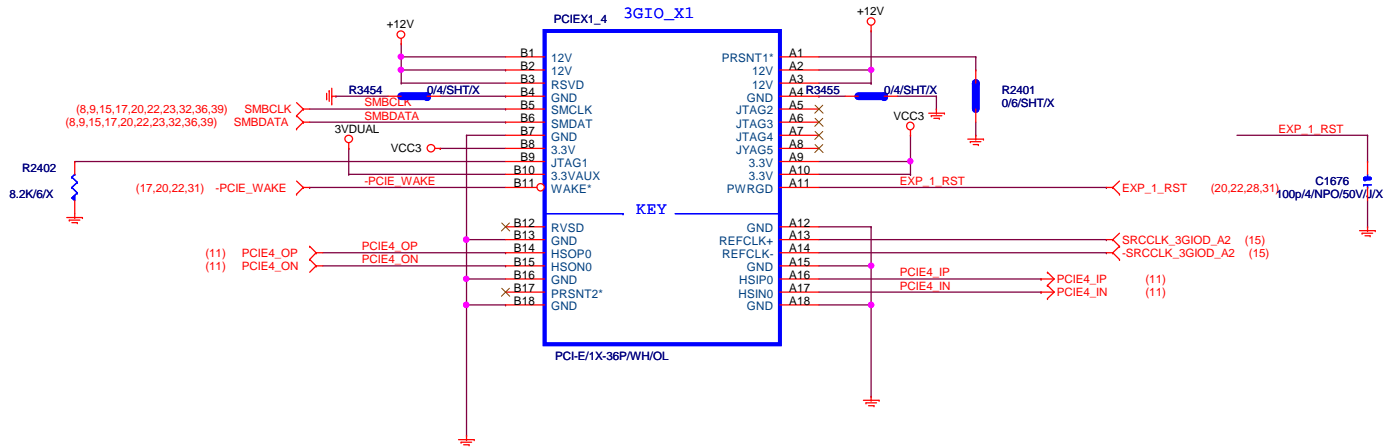


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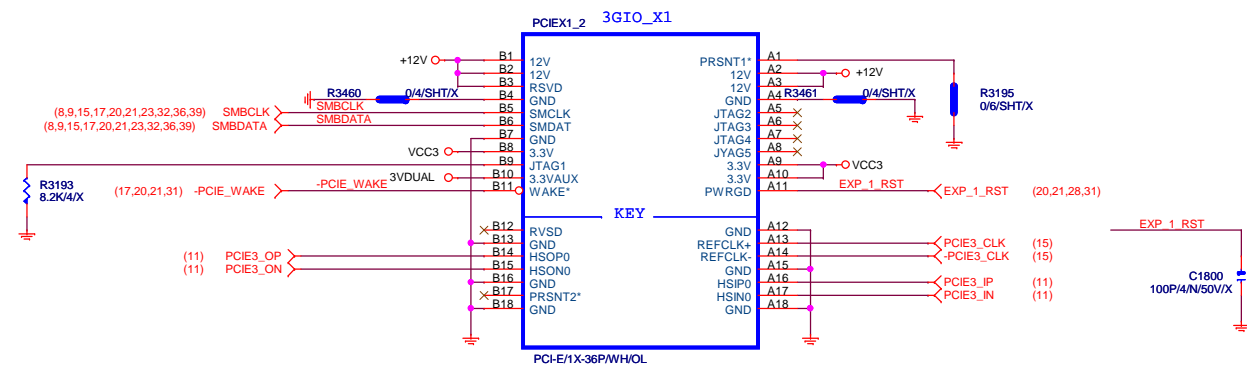
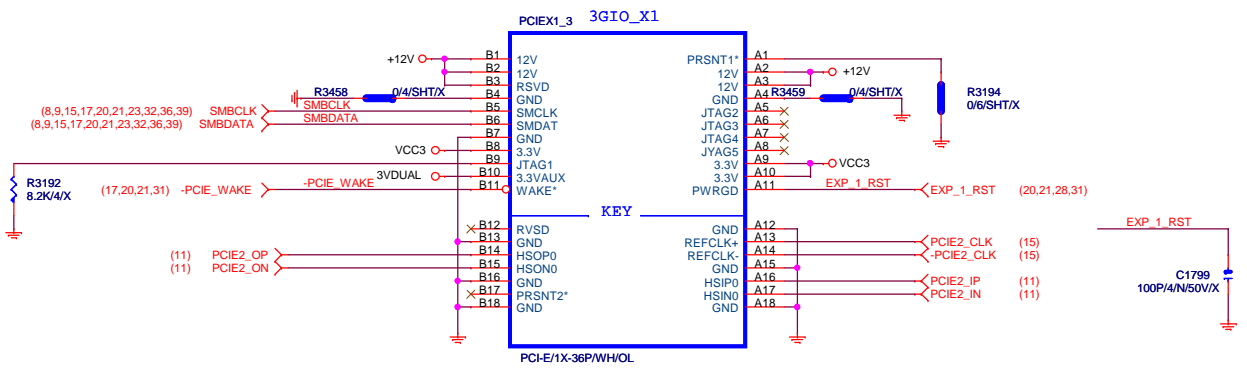
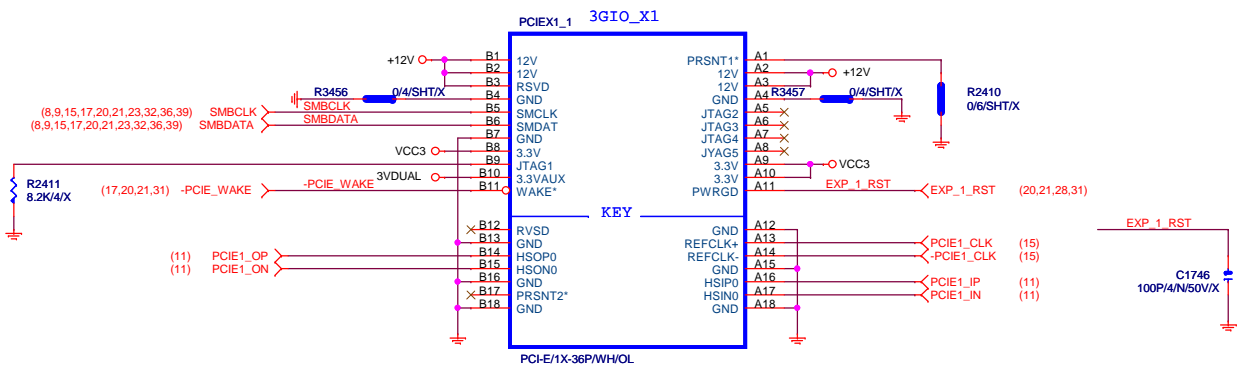
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Size: Custom    Document Number: **GA-MA770T-UD3**    Rev: **3.1**

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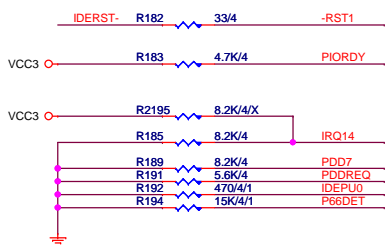
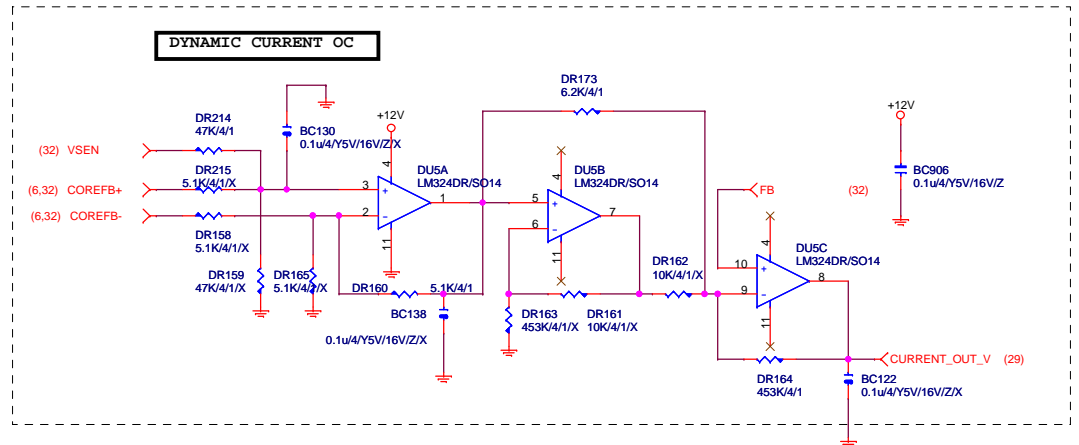
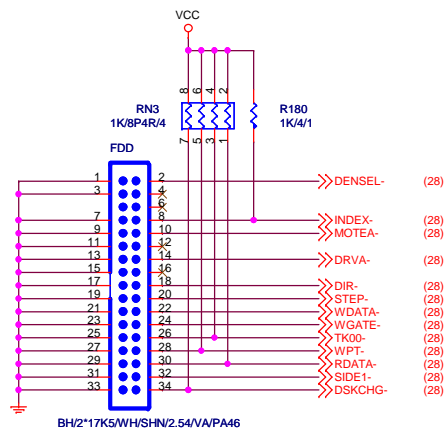


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Size	Document Number	Rev	
Custom	<b>GA-MA770T-UD3</b>	<b>3.1</b>	
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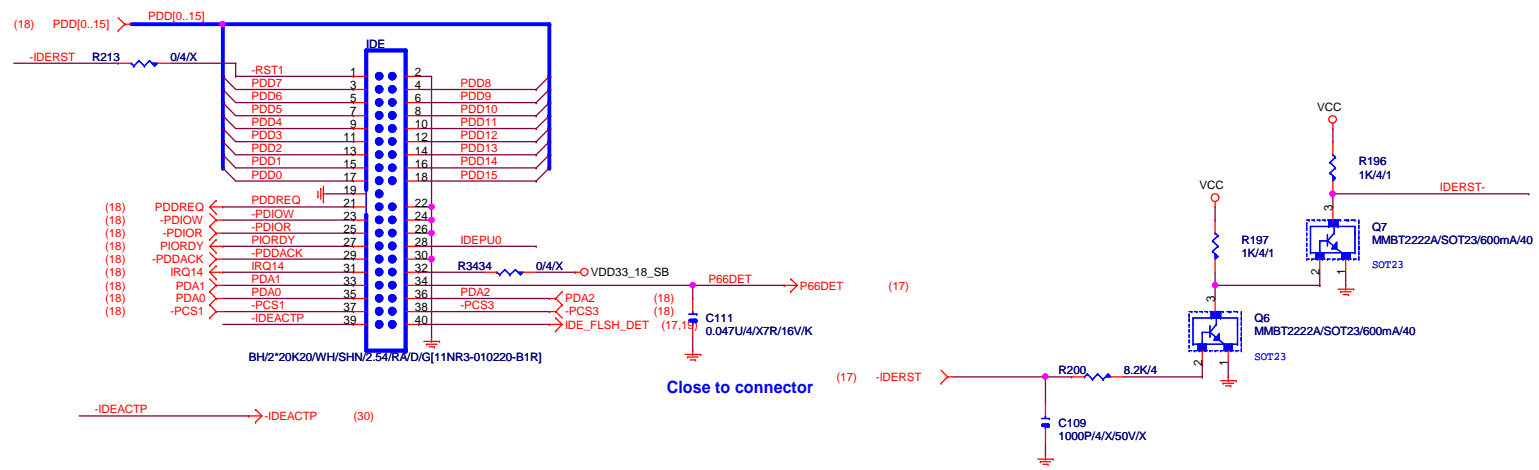


<b>GIGABYTE™</b>		
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Size Custom	Document Number <b>GA-MA770T-UD3</b>	Rev <b>3.1</b>
Date: Thursday, March 17, 2011	Sheet 22	of 39

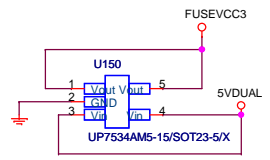
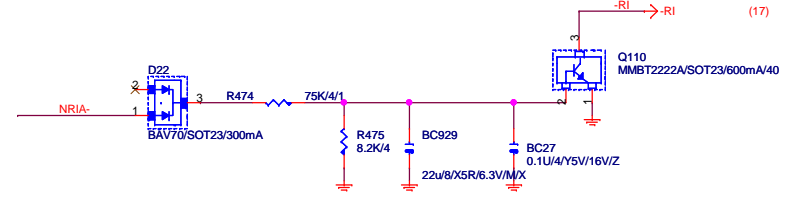
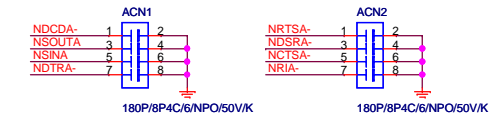
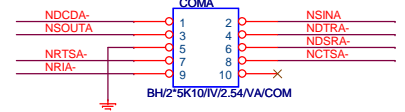
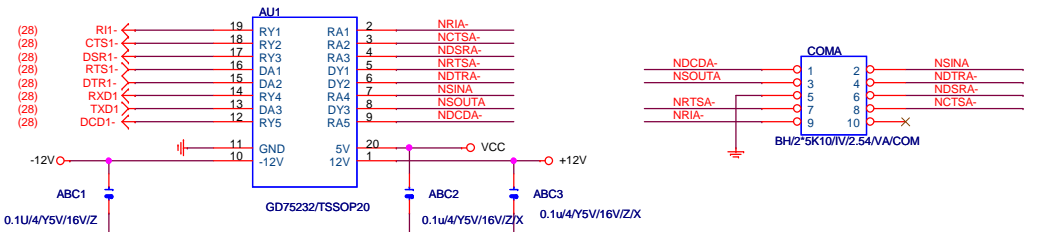




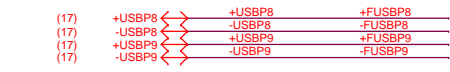
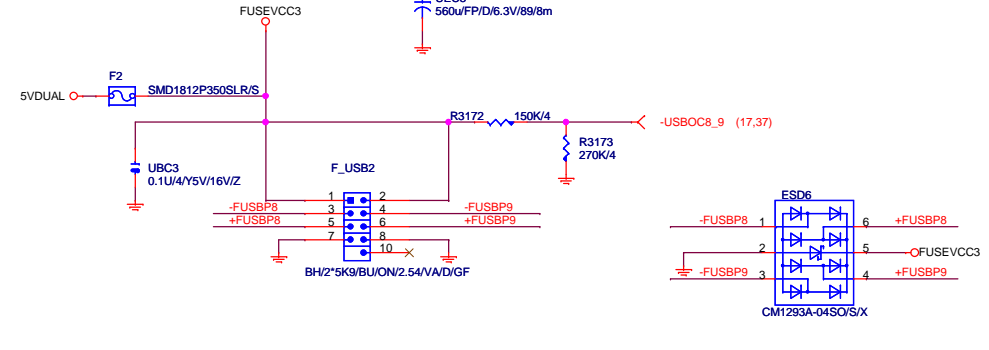
**PRIMARY IDE CONNECTOR**



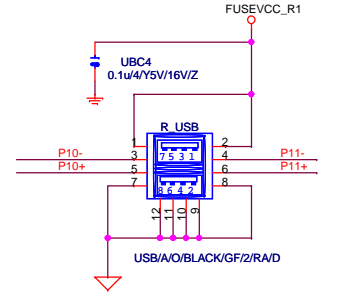
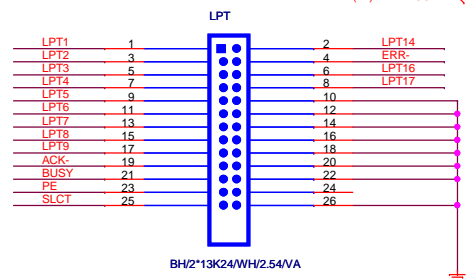
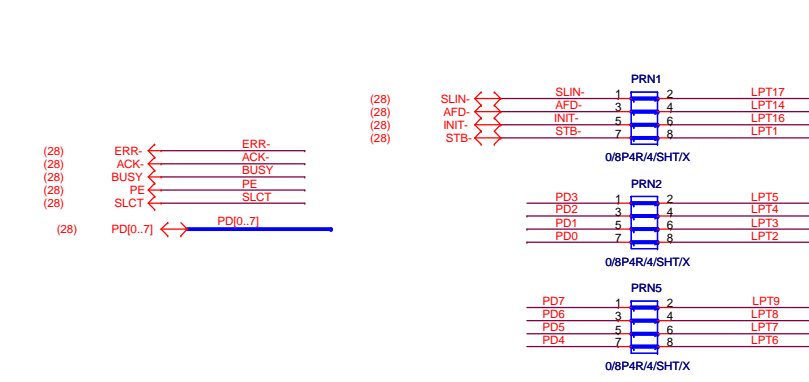
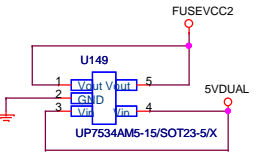
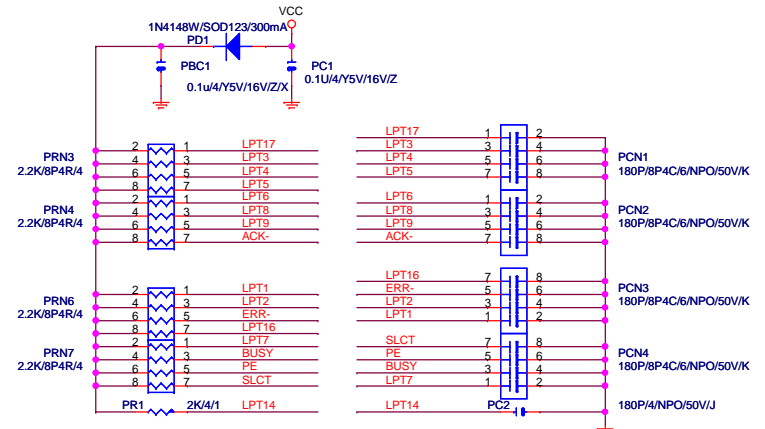
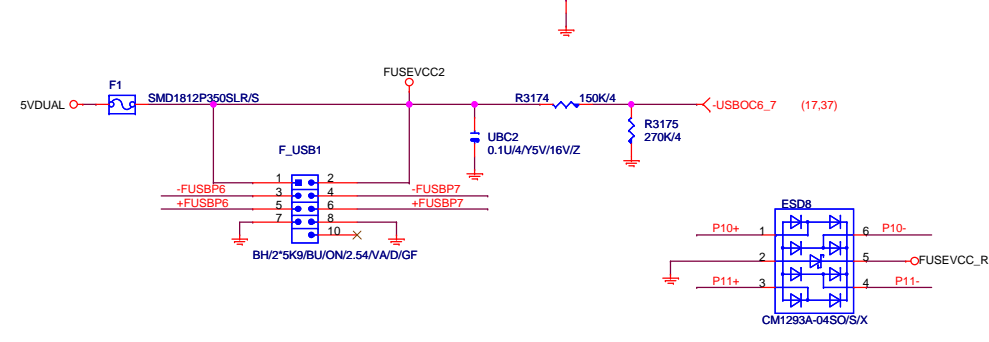




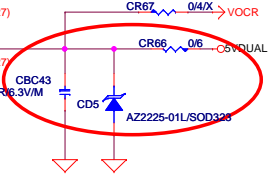
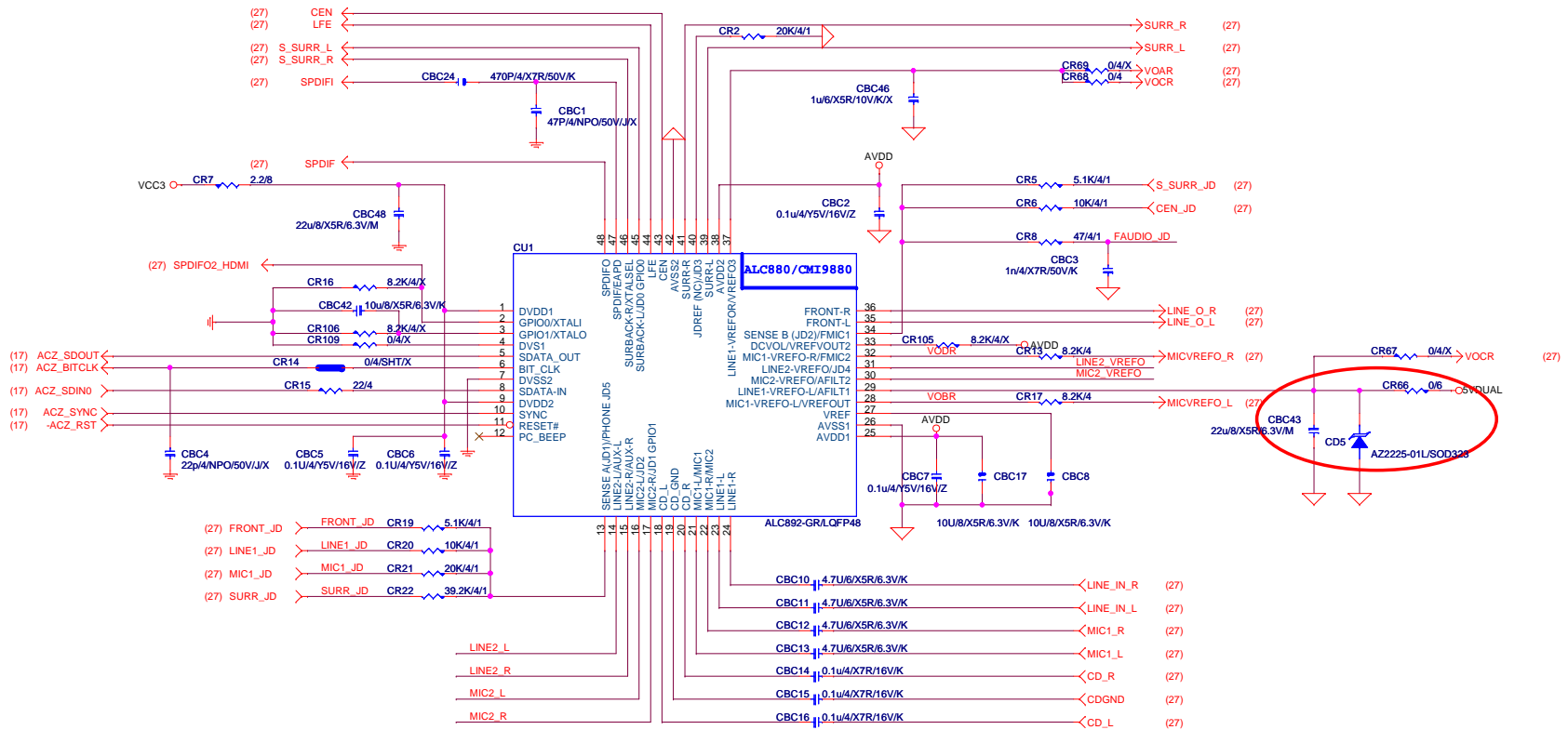
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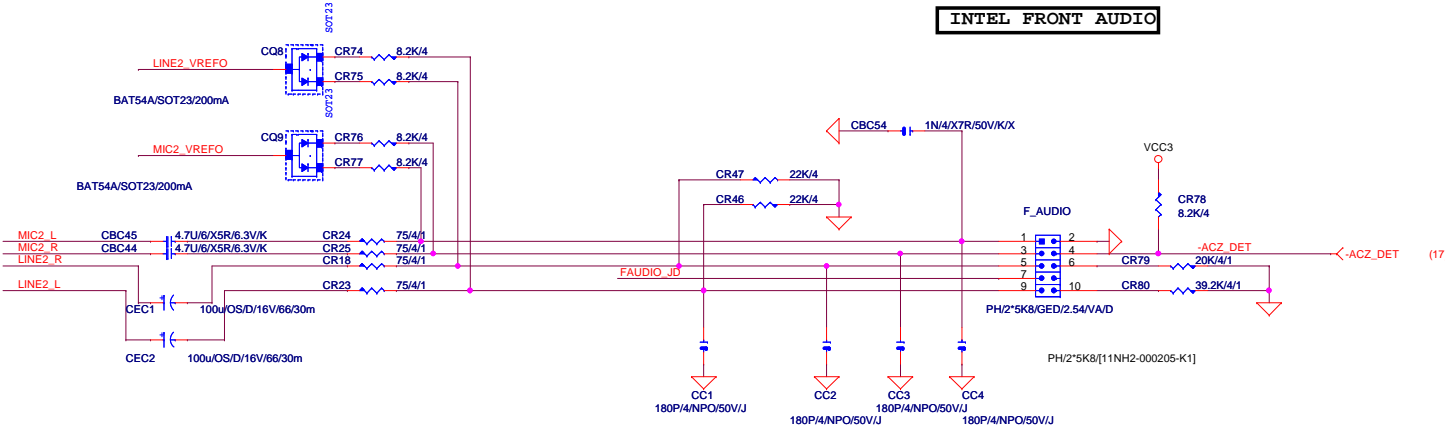
### FRONT SIDE USB



**GIGABYTE**  
**COM/LPT/FUSB**  
 Title: COM/LPT/FUSB  
 Size: Custom  
 Document Number: GA-MA770T-UD3  
 Date: Thursday, March 17, 2011  
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**INTEL FRONT AUDIO**



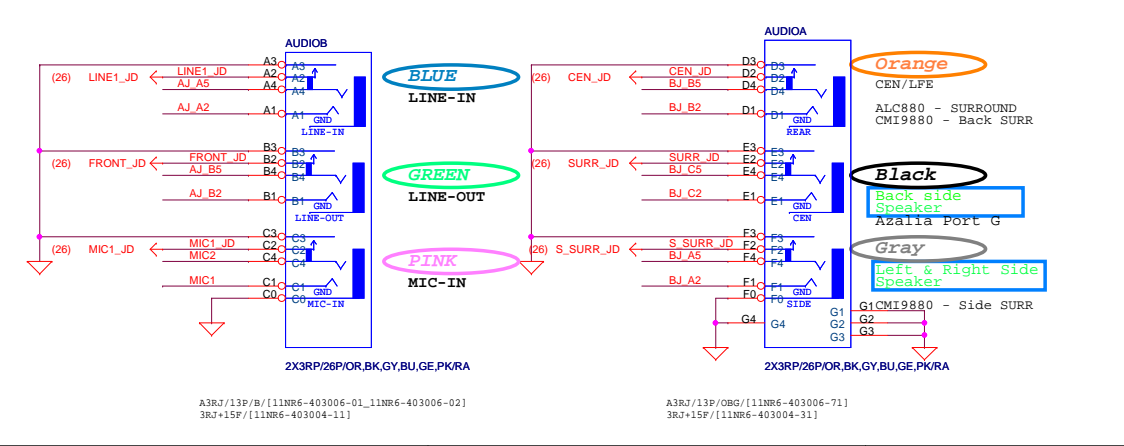
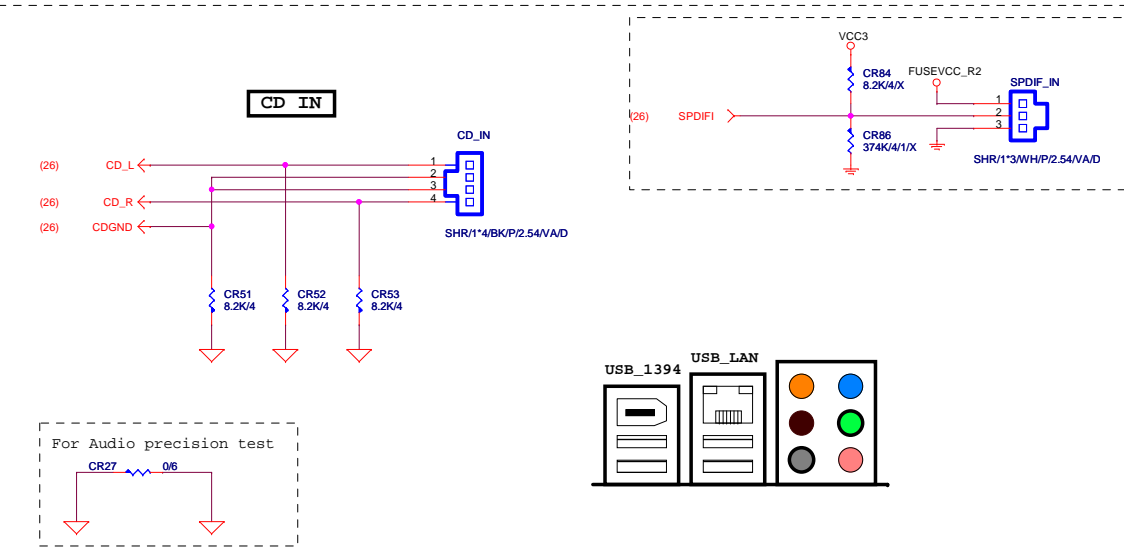
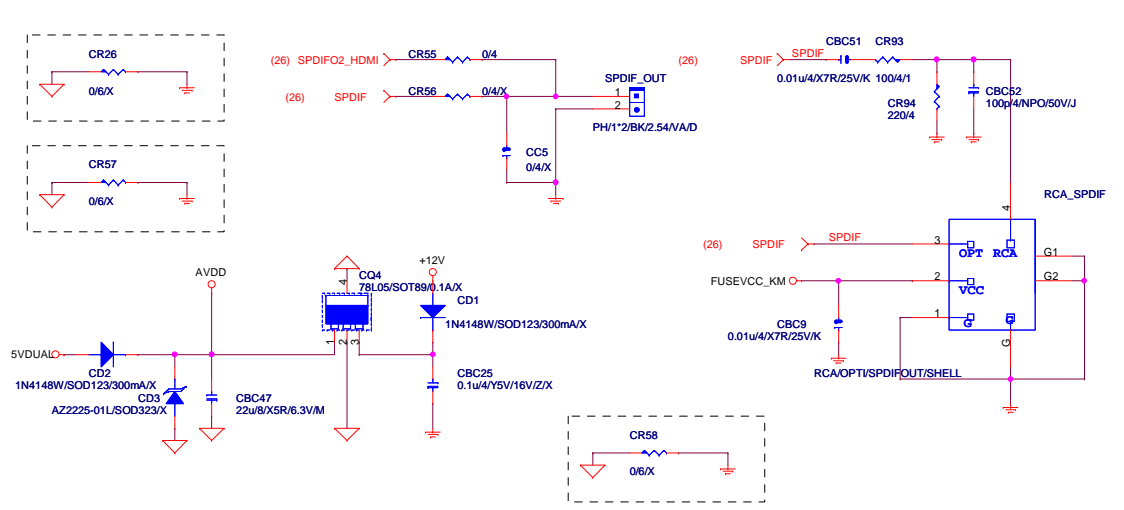
**GIGABYTE™**

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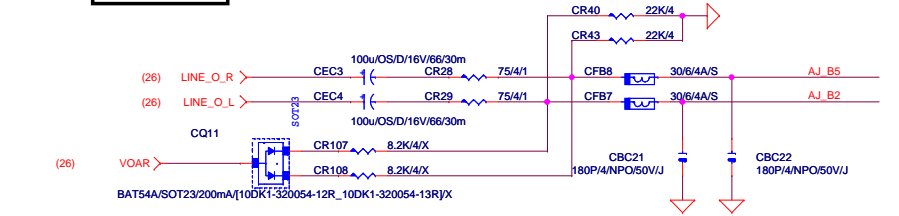
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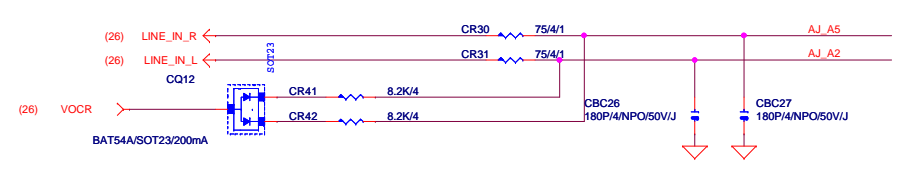
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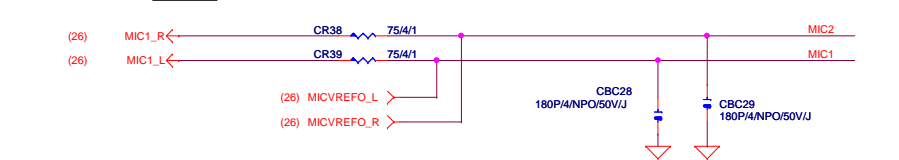
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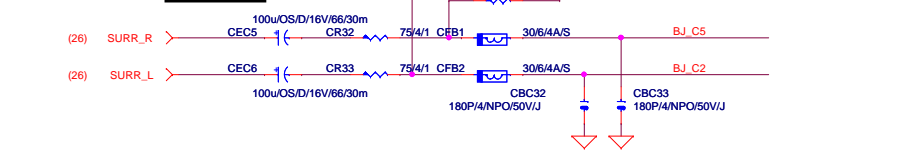
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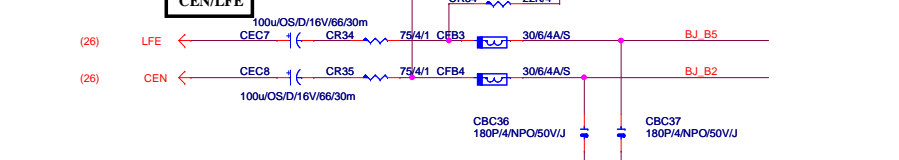
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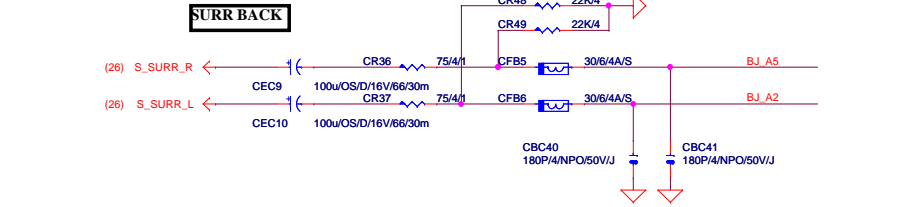
**SURROUND**



**CEN/LFE**



**SURR BACK**



**GIGABYTE™**

Title: **REAR AUDIO JACK**

Size: Document Number **GA-MA770T-UD3** Rev **3.1**

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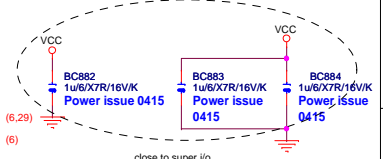
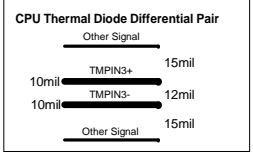
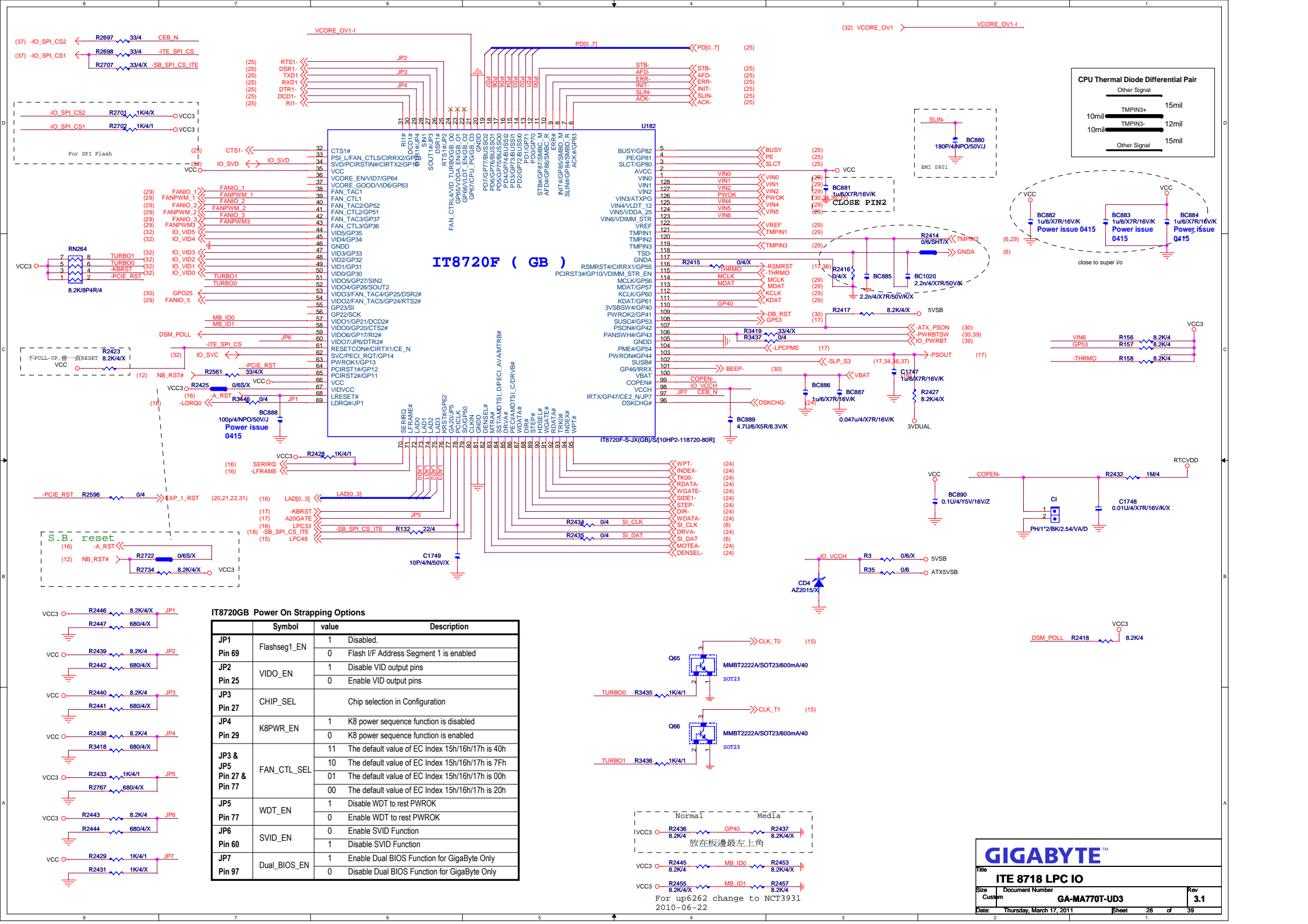
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3R3\*15P/[11NR6-403004-31]

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3R3\*15P/[11NR6-403004-31]

A3R7/13P/0BG/[11NR6-403006-71]  
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A3R7/13P/0BG/[11NR6-403006-71]  
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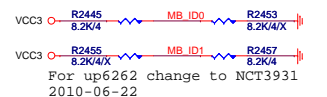
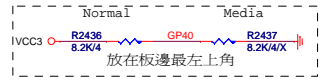
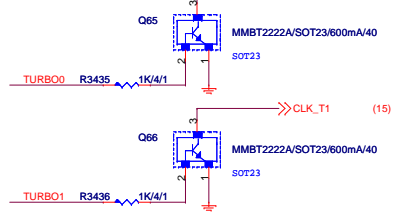
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3R3\*15P/[11NR6-403004-31]



**IT8720F ( GB )**

**IT8720GB Power On Strapping Options**

Symbol	value	Description
JP1	1	Disabled.
Pin 69	Flashseg1_EN	0 Flash I/F Address Segment 1 is enabled
JP2	1	Disable VID output pins
Pin 25	VIDO_EN	0 Enable VID output pins
JP3	CHIP_SEL	Chip selection in Configuration
Pin 27		
JP4	1	K8 power sequence function is disabled
Pin 29	K8PWR_EN	0 K8 power sequence function is enabled
	11	The default value of EC Index 15h/16h/17h is 40h
JP3 & JP5	FAN_CTL_SEL	10 The default value of EC Index 15h/16h/17h is 7Fh
Pin 27 & Pin 77		01 The default value of EC Index 15h/16h/17h is 00h
	00	The default value of EC Index 15h/16h/17h is 20h
JP5	1	Disable WDT to rest PWROK
Pin 77	WDT_EN	0 Enable WDT to rest PWROK
JP6	1	Enable SVID Function
Pin 60	SVID_EN	1 Disable SVID Function
JP7	1	Enable Dual BIOS Function for GigaByte Only
Pin 97	Dual_BIOS_EN	0 Disable Dual BIOS Function for GigaByte Only



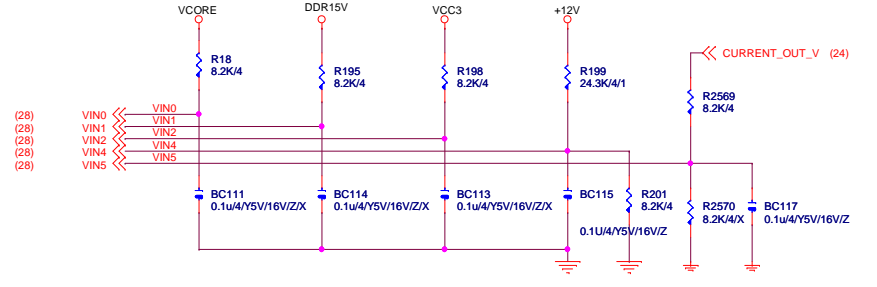
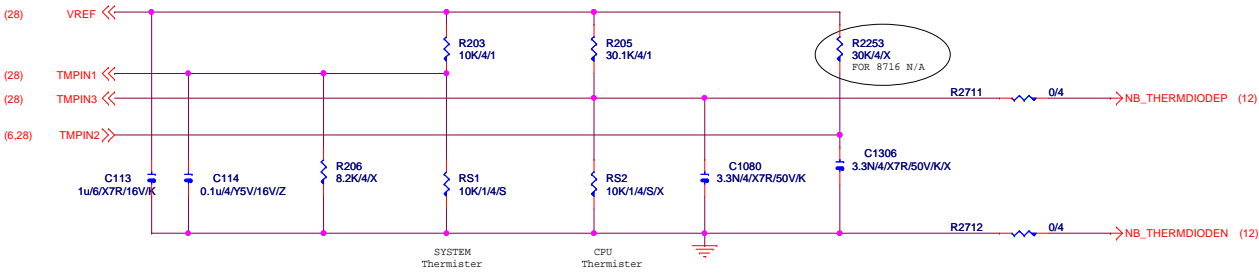
**GIGABYTE™**

File: **ITE 8718 LPC IO**

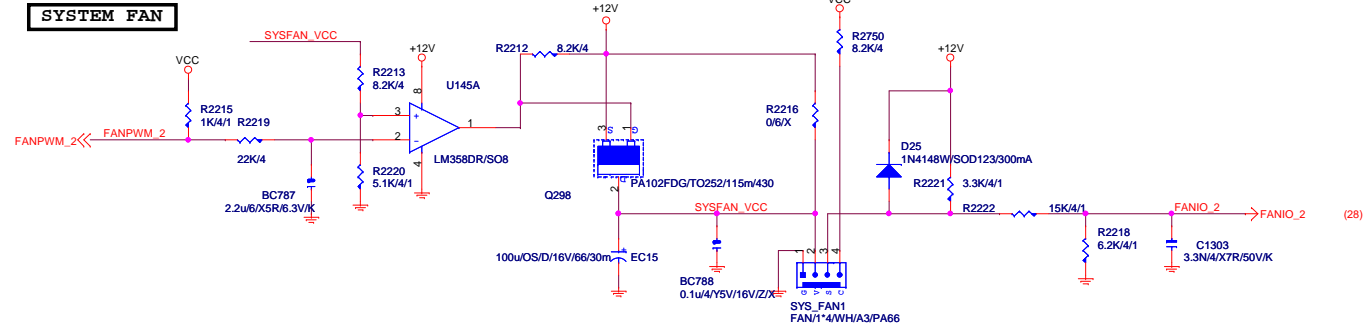
Size: Document Number **GA-MA770T-UD3** Rev: **3.1**

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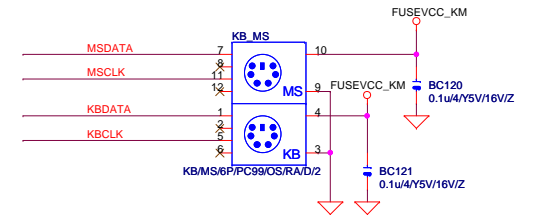
# Hardware Monitor circuits



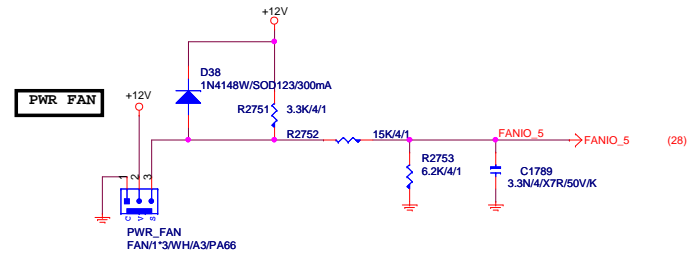
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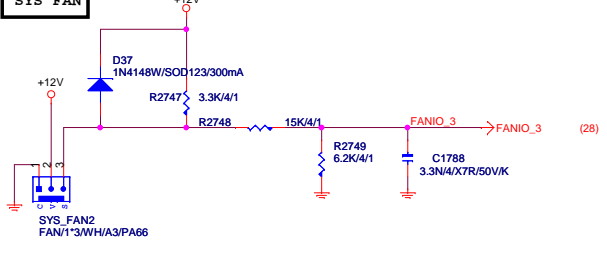
## KB & MS



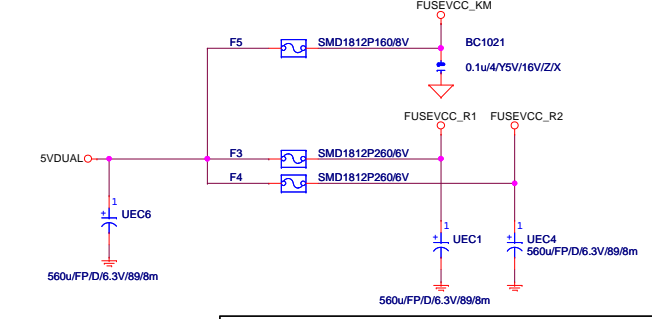
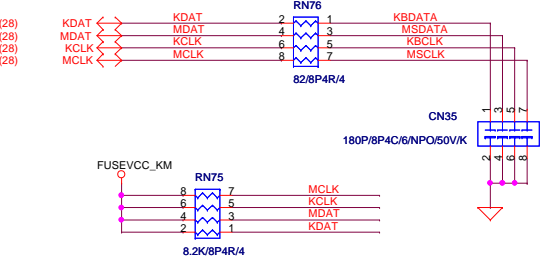
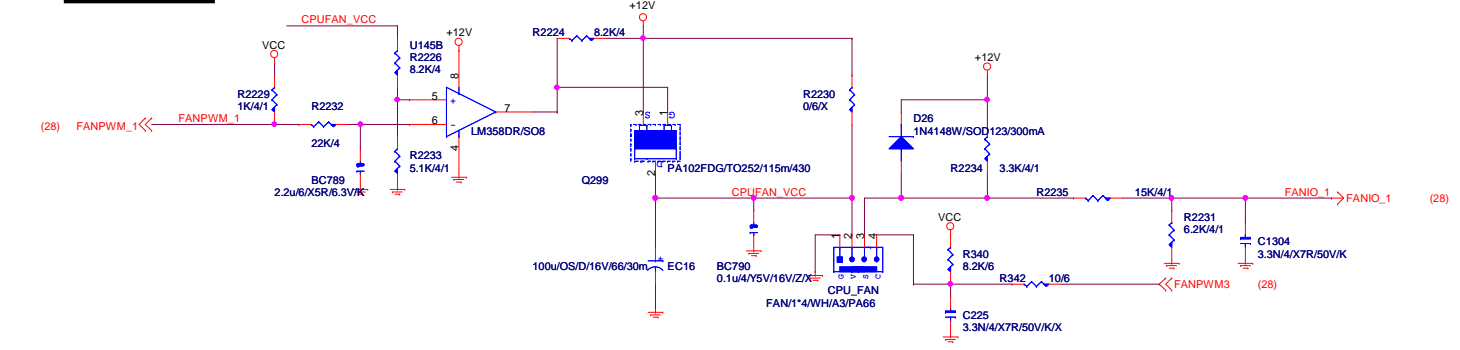
## PWR FAN



## SYS FAN



## CPU FAN

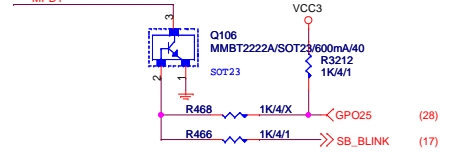
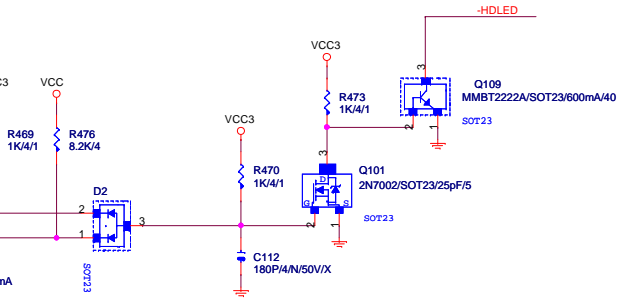
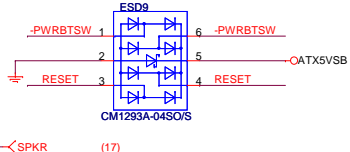
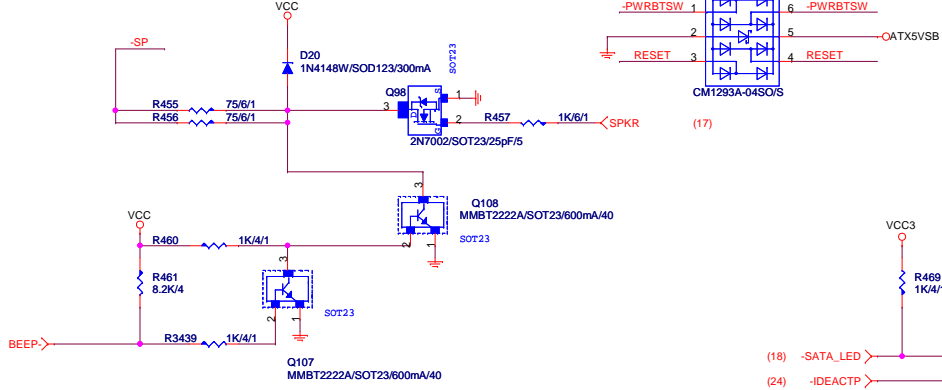
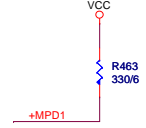
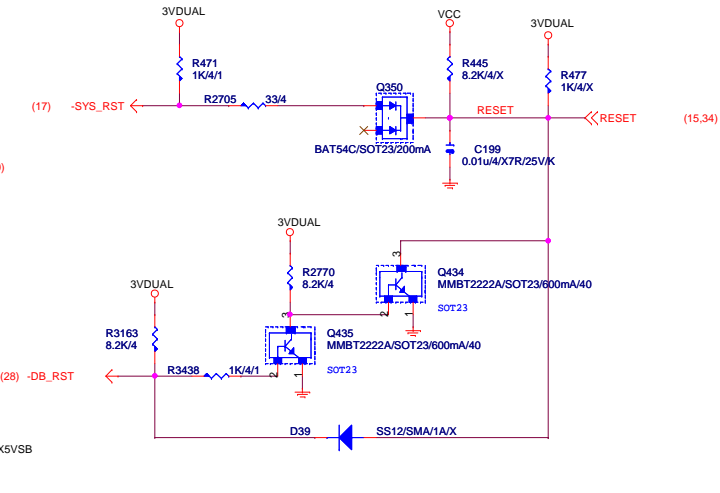
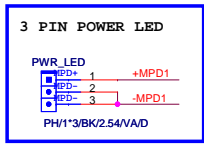
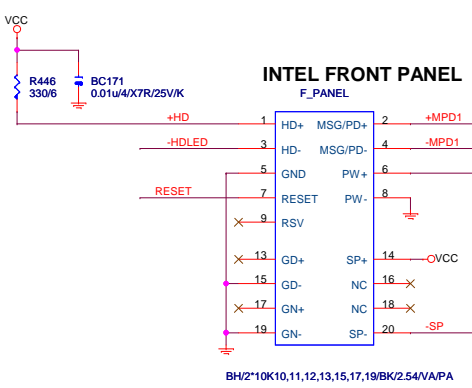


**GIGABYTE**

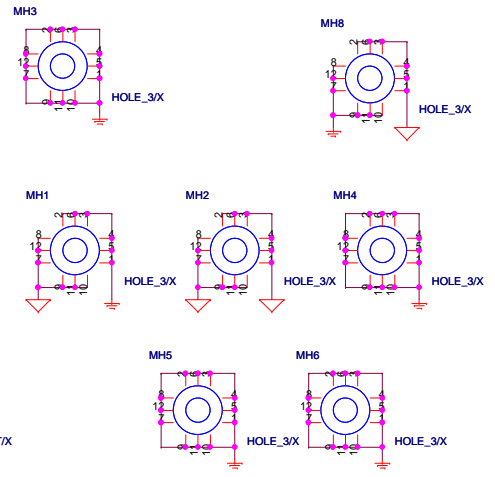
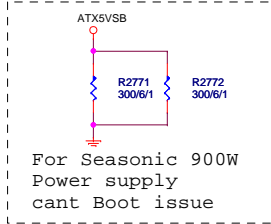
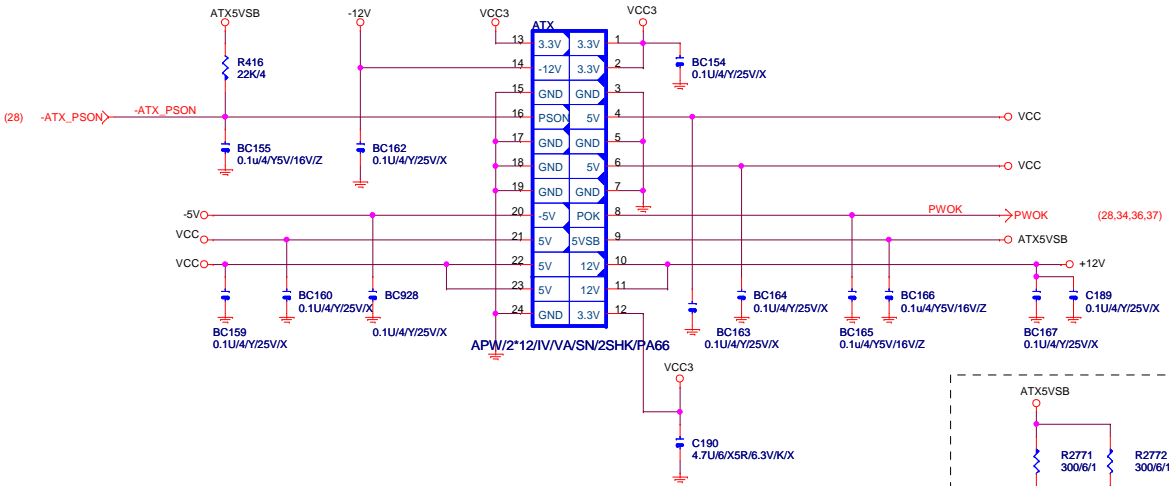
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Size: Custom Document Number: **GA-MA770T-UD3** Rev: **3.1**

Date: Thursday, March 17, 2011 Sheet: 29 of 39



### ATX POWER CONNECTOR



**GIGABYTE™**

Title: **ATX, FRONT PANEL**

Size: Custom

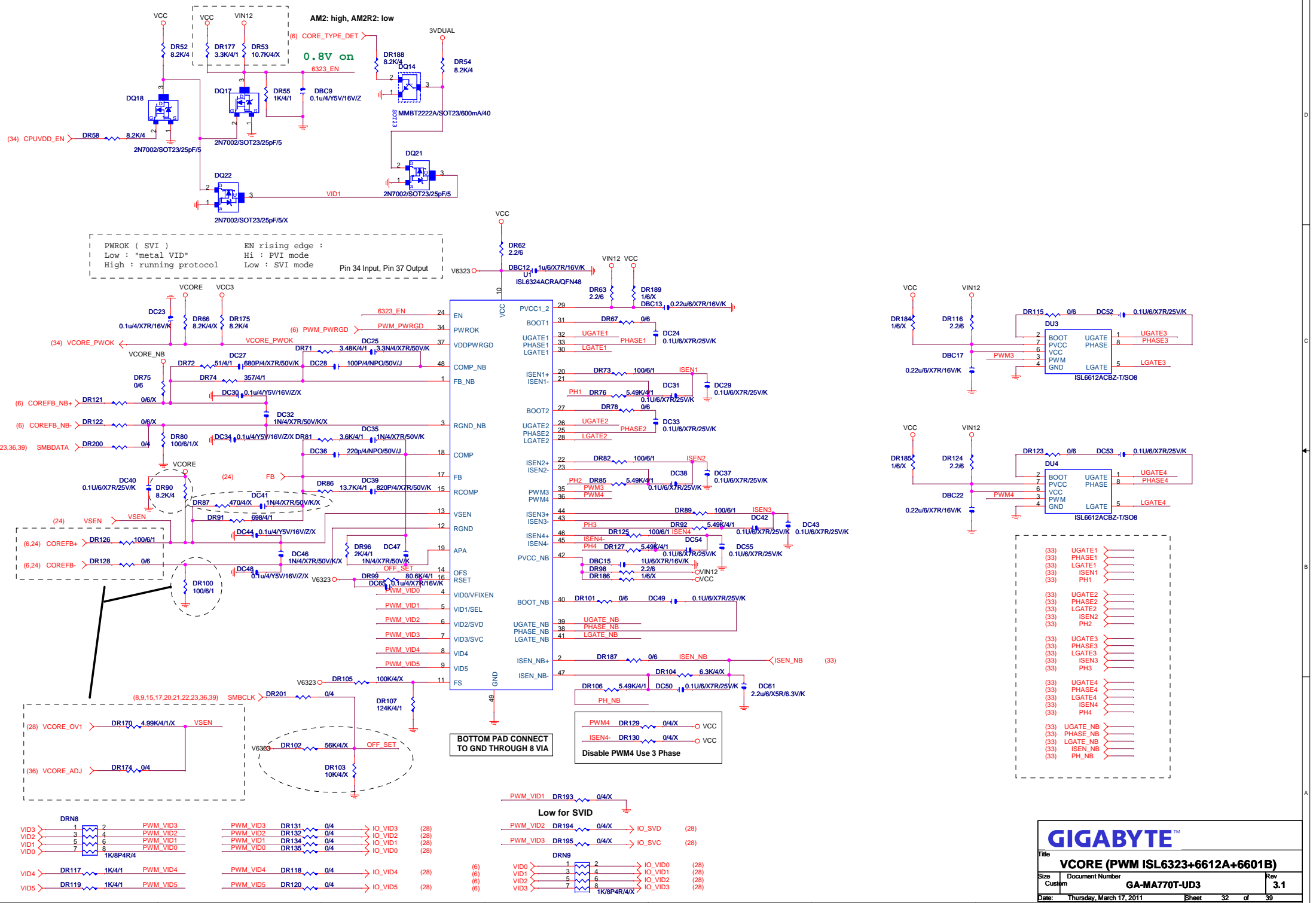
Document Number: **GA-MA770T-UD3**

Date: Thursday, March 17, 2011

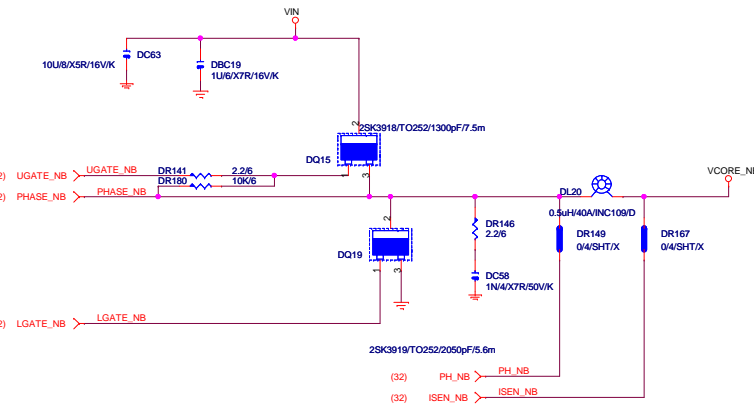
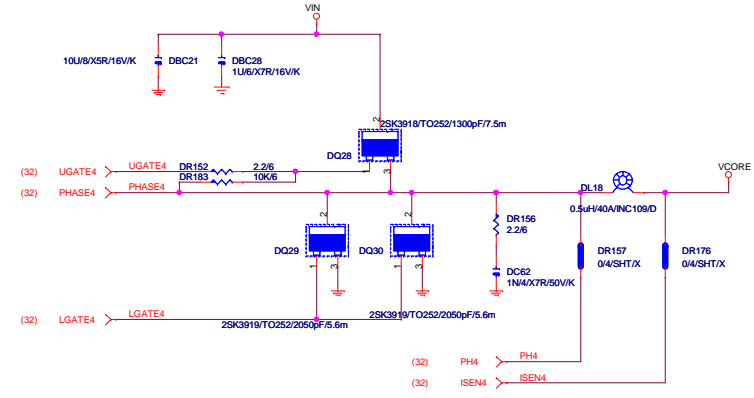
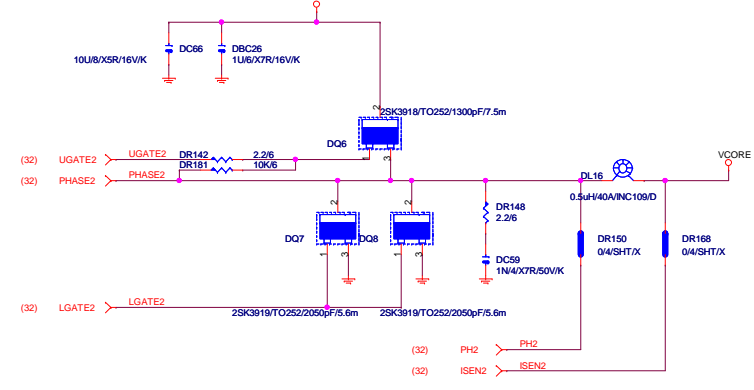
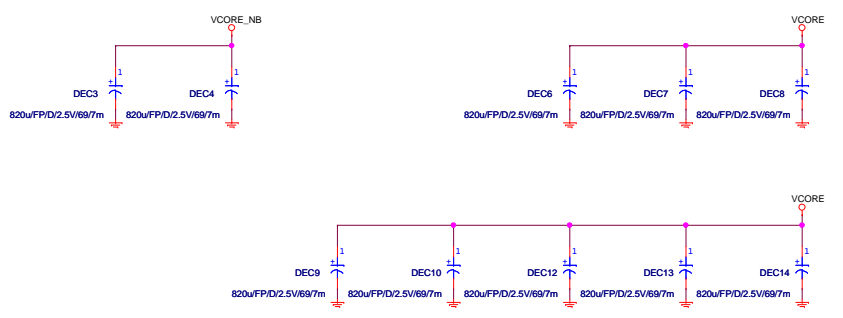
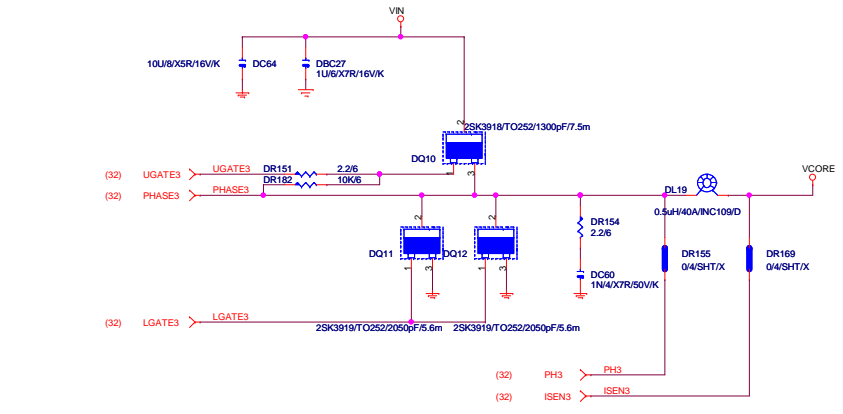
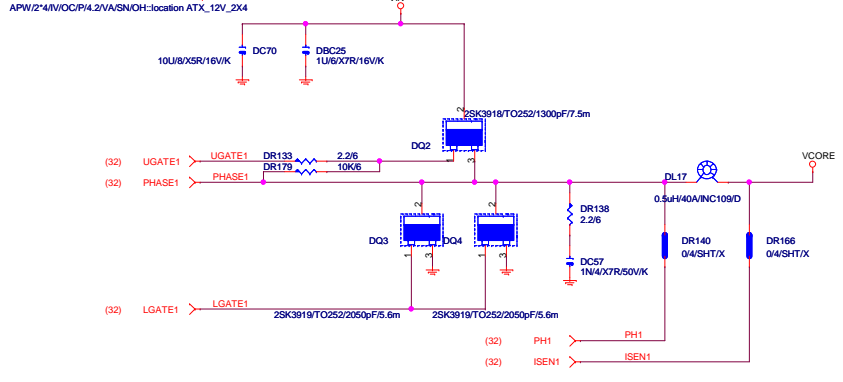
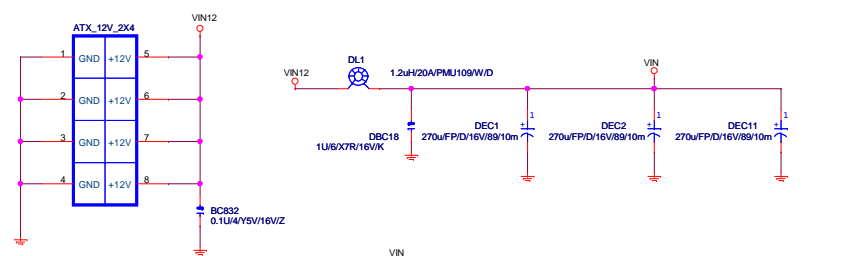
Sheet: 30 of 39

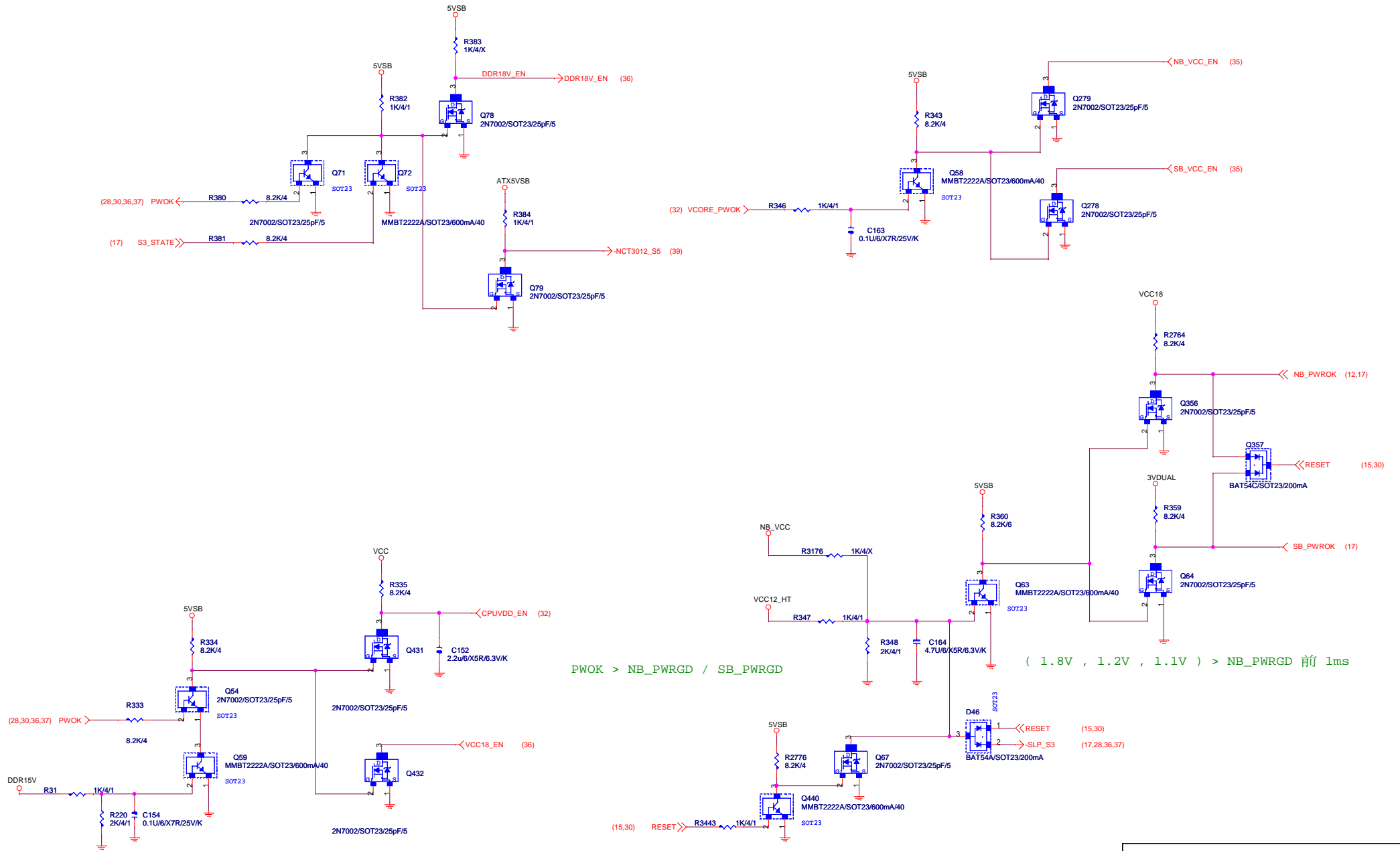
Rev: **3.1**



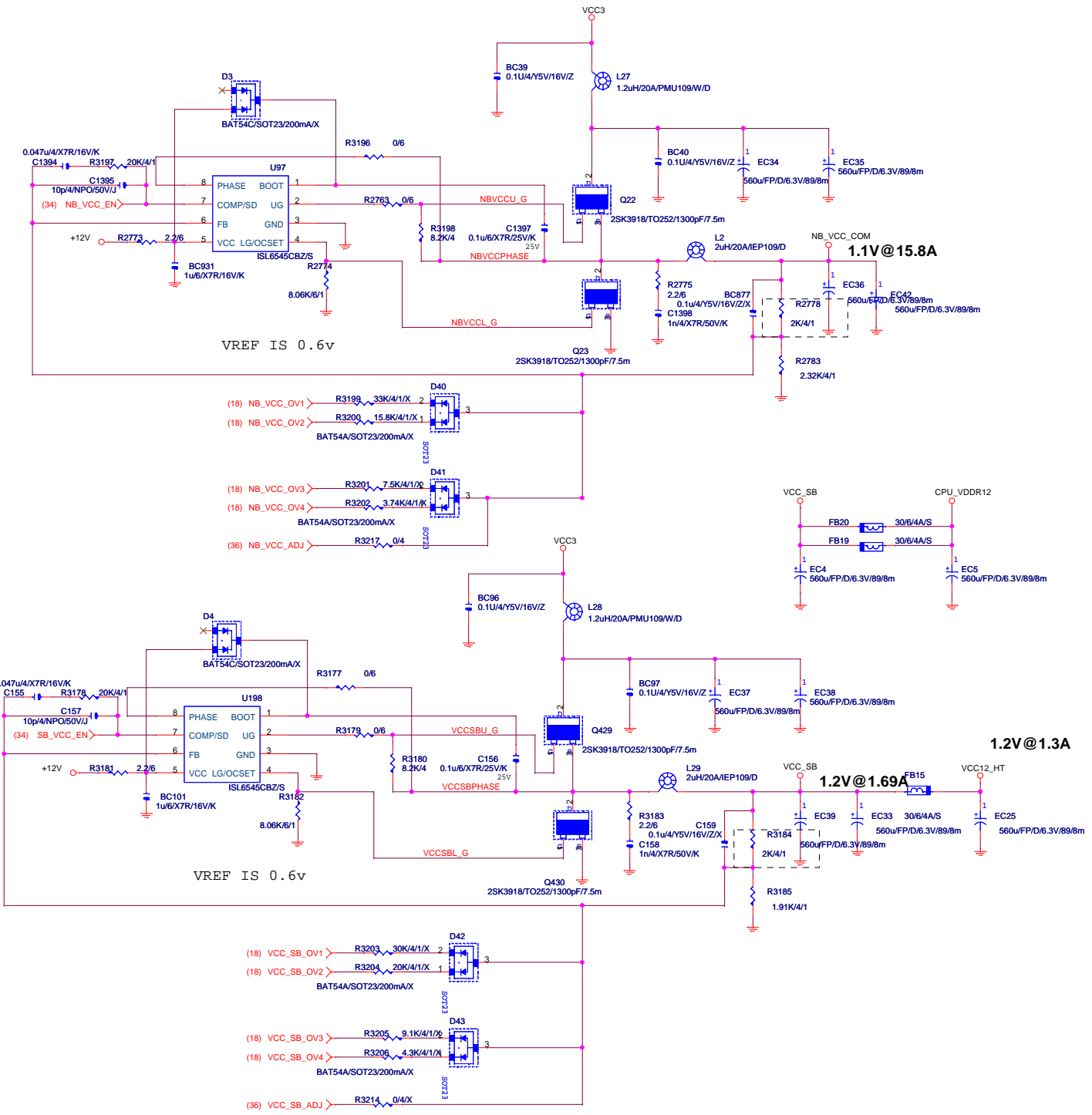








<b>GIGABYTE™</b>		
Title <b>POWER SEQUENCE</b>		
Size Custom	Document Number <b>GA-MA770T-UD3</b>	Rev <b>3.1</b>
Date: Thursday, March 17, 2011	Sheet 34	of 39

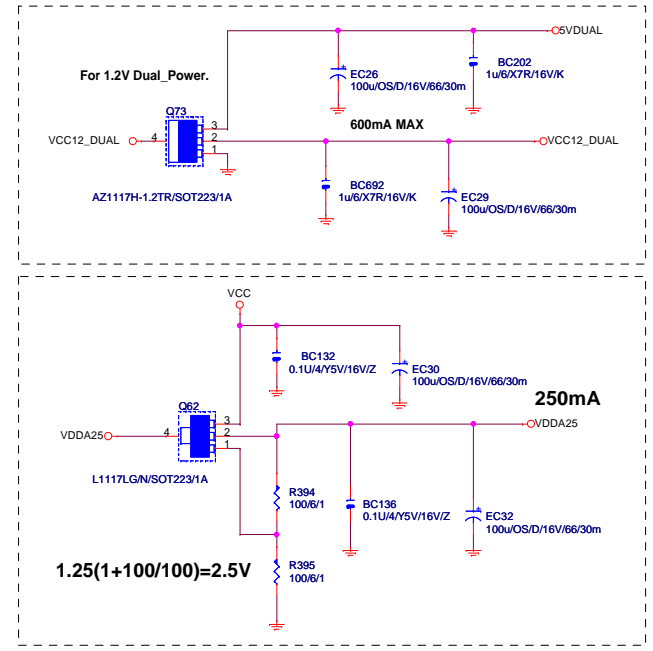
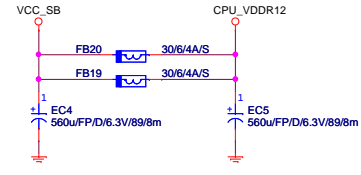
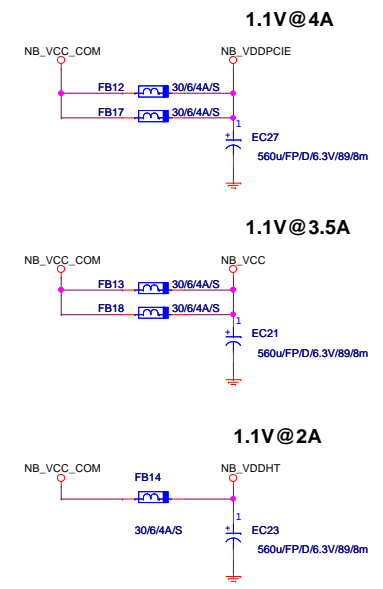


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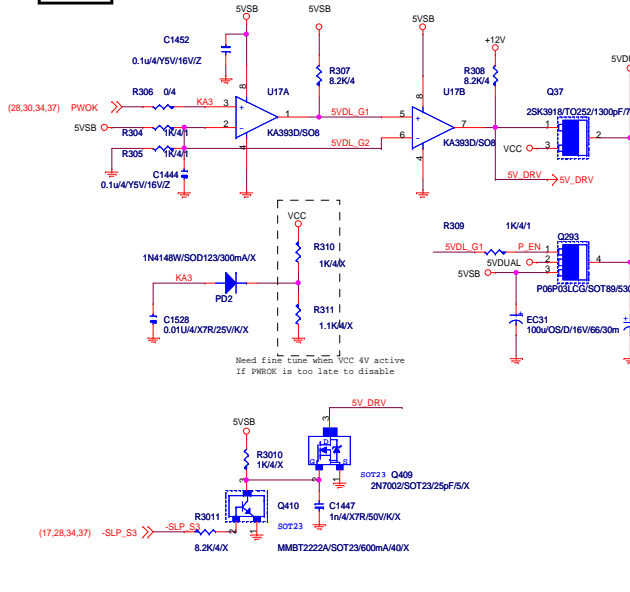
VREF IS 0.6v

- (18) NB\_VCC\_OV1
- (18) NB\_VCC\_OV2
- (18) NB\_VCC\_OV3
- (18) NB\_VCC\_OV4
- (36) NB\_VCC\_ADJ

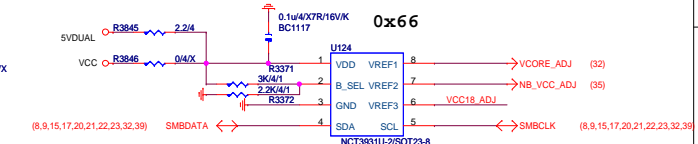
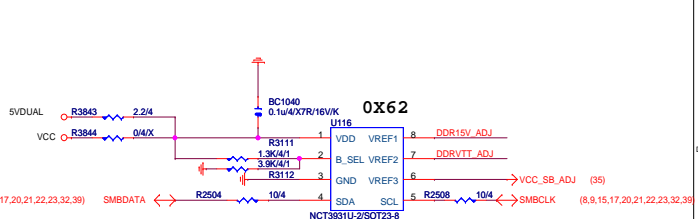
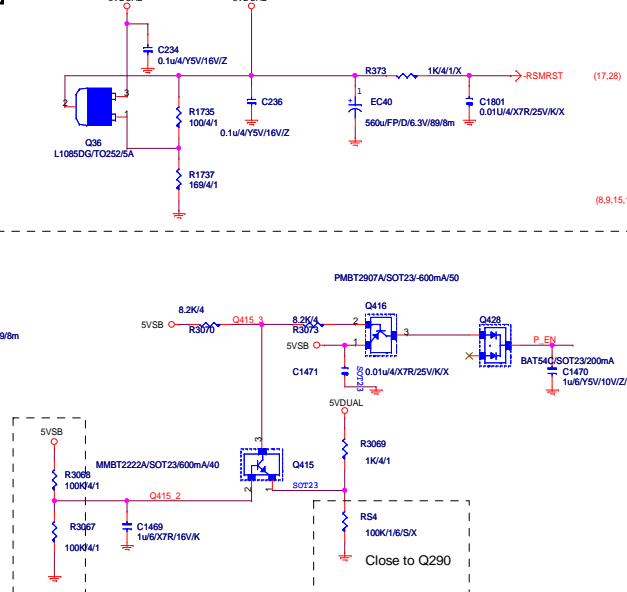
- (18) VCC\_SB\_OV1
- (18) VCC\_SB\_OV2
- (18) VCC\_SB\_OV3
- (18) VCC\_SB\_OV4
- (36) VCC\_SB\_ADJ



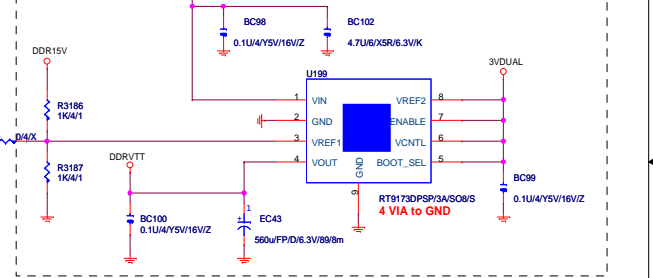
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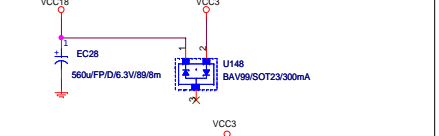
3VDUAL



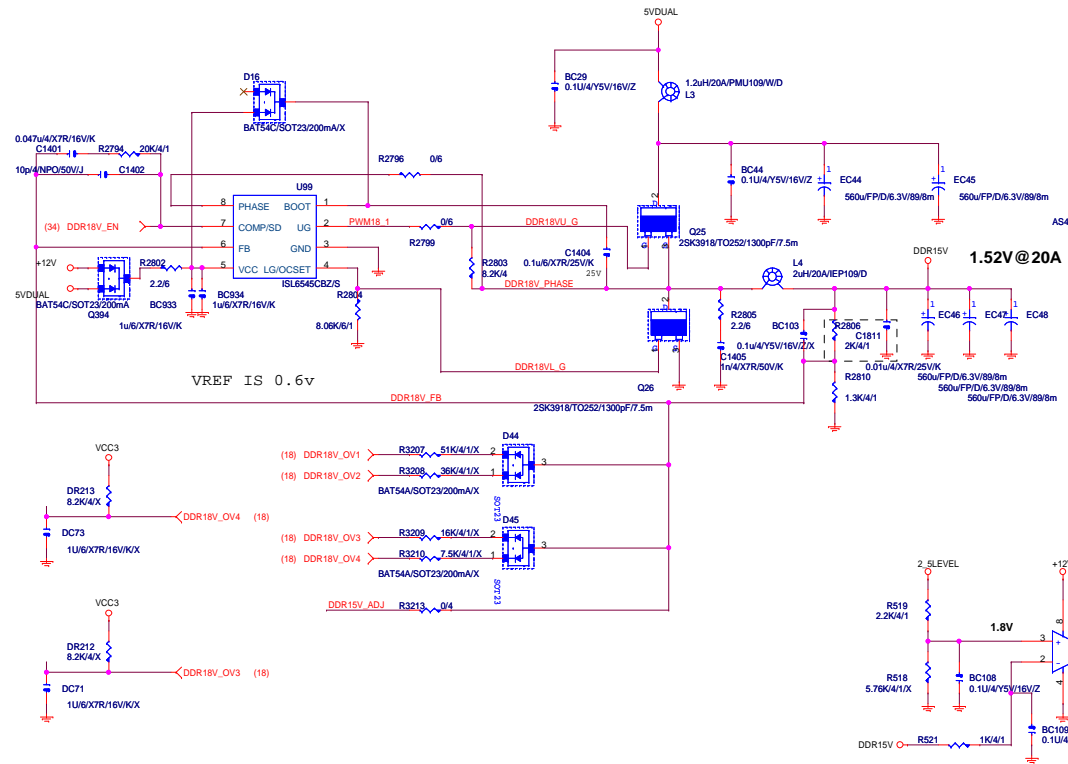
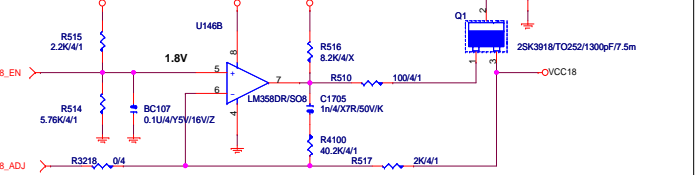
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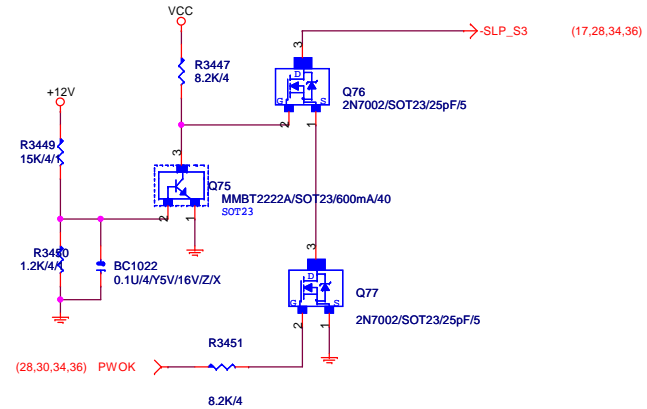
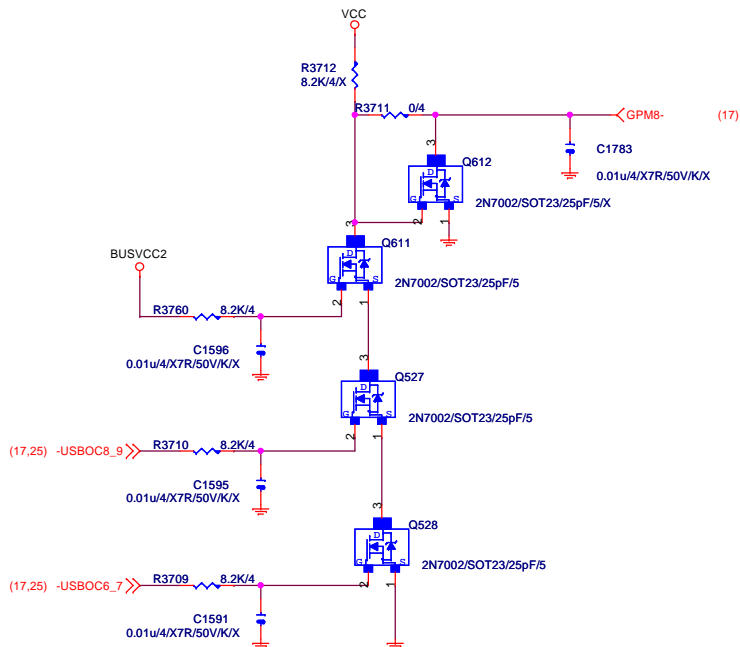
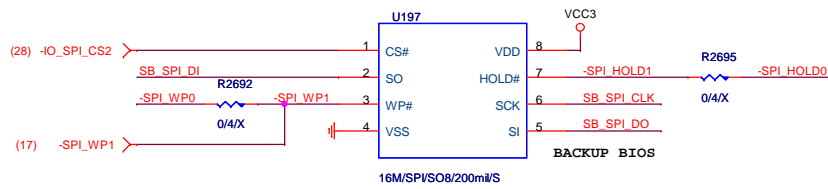
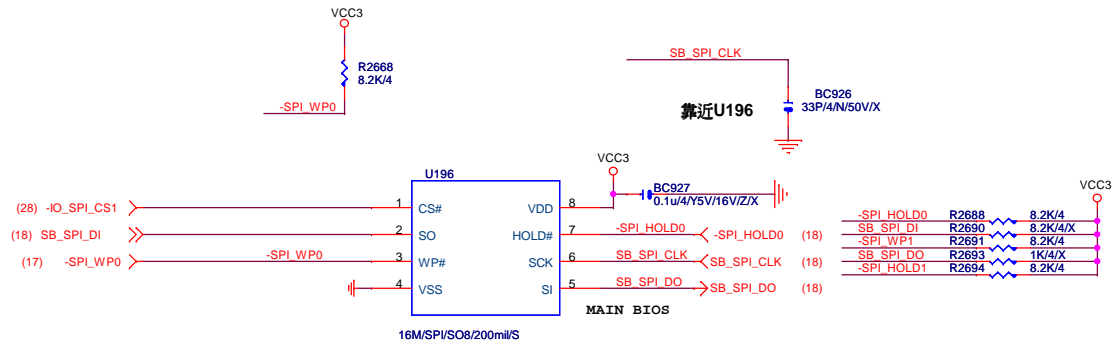


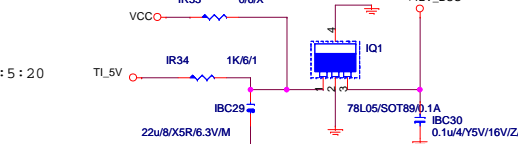
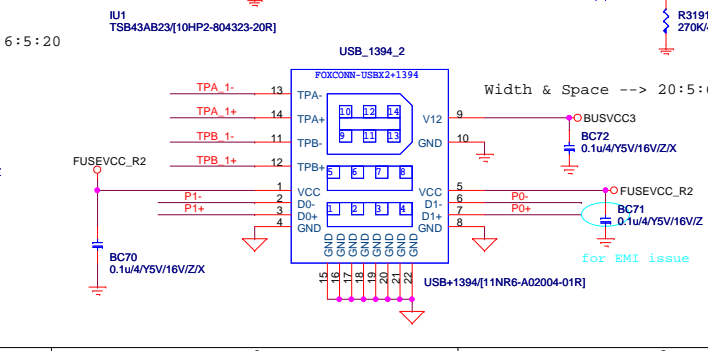
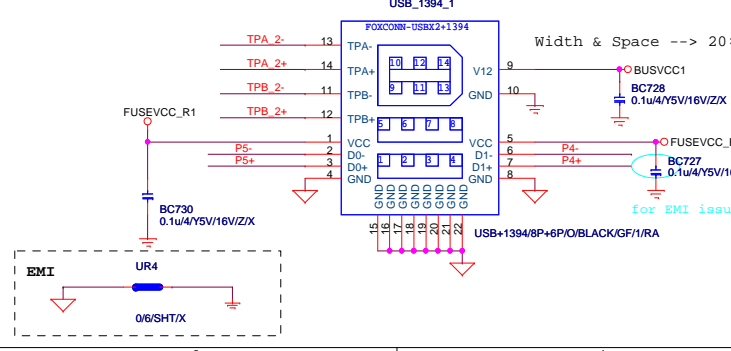
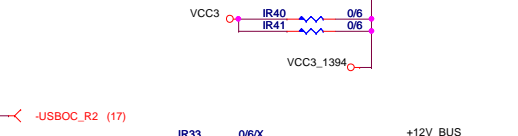
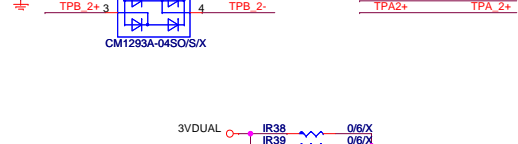
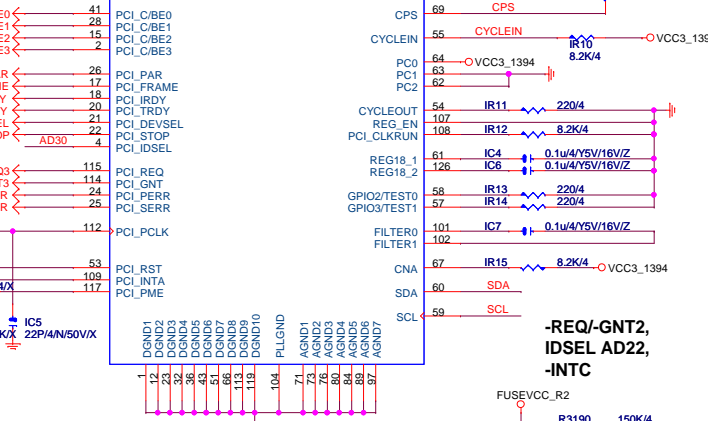
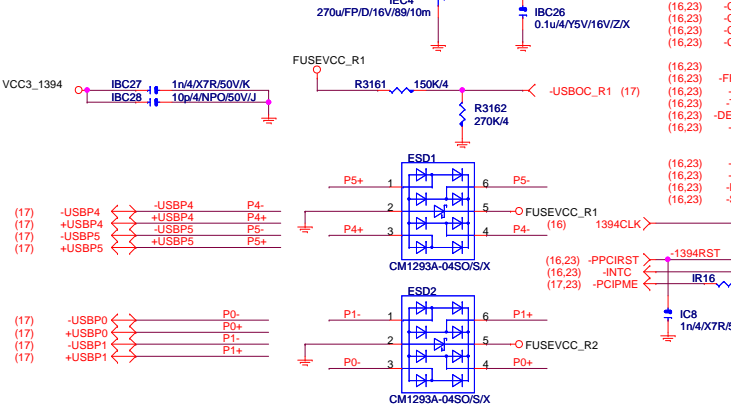
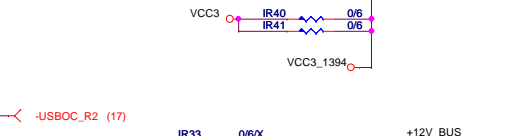
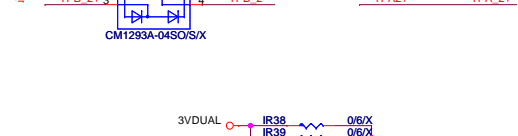
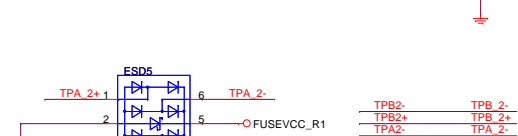
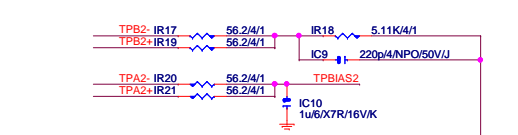
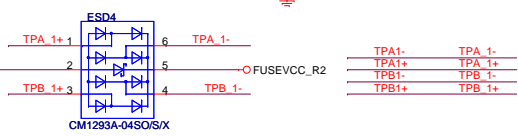
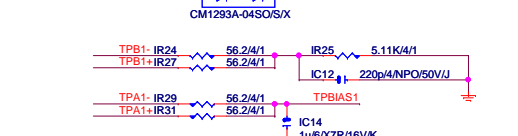
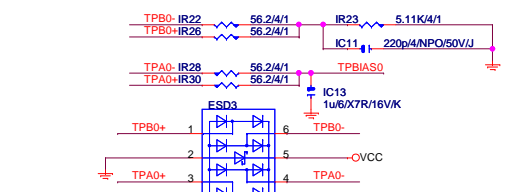
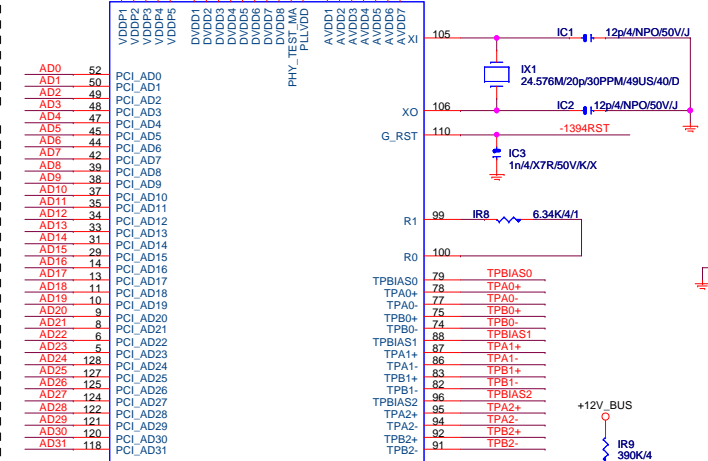
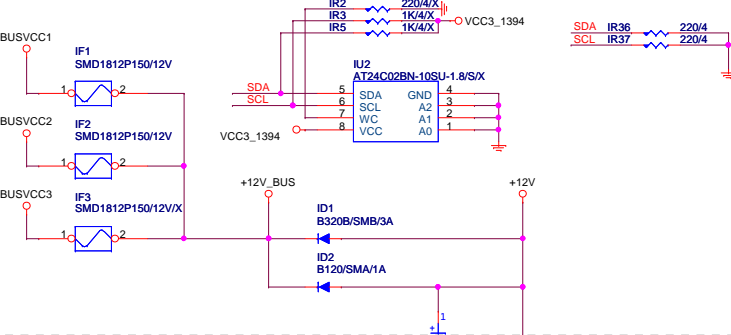
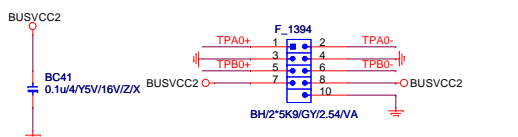
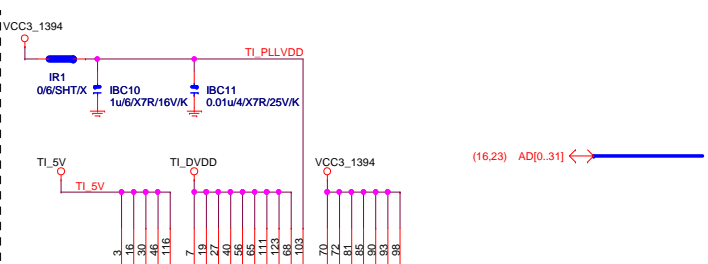
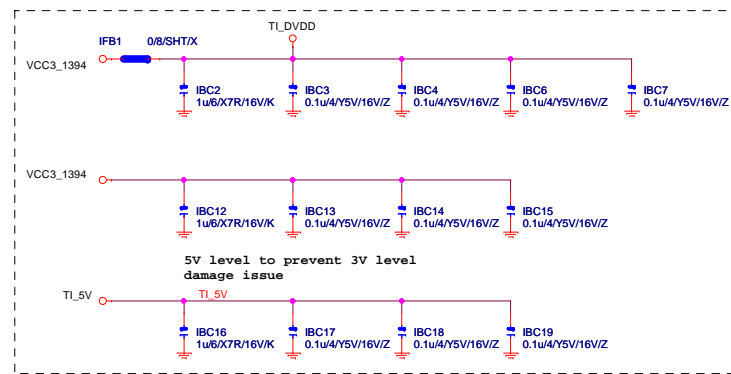
ATI for VCC3/VCC18 power ramp-up 2.1V

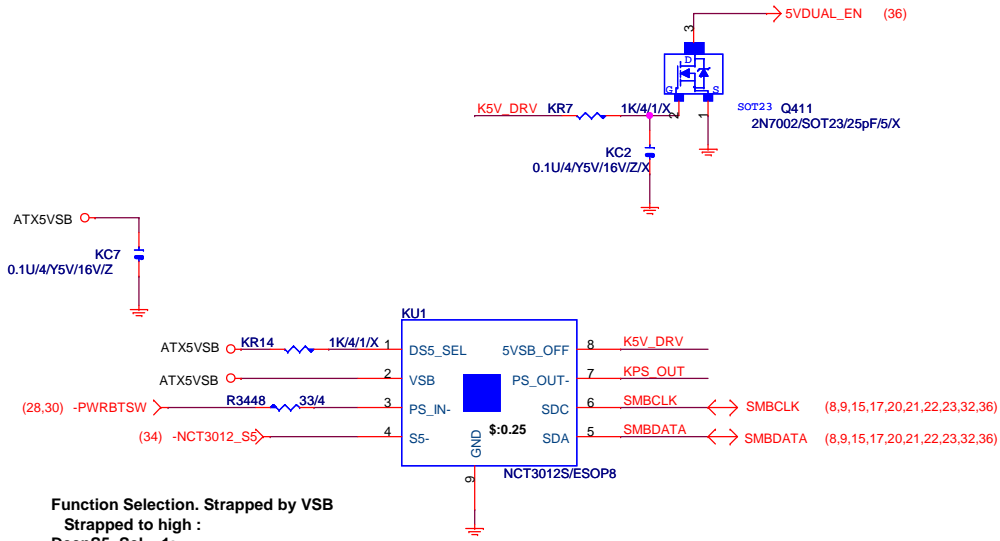


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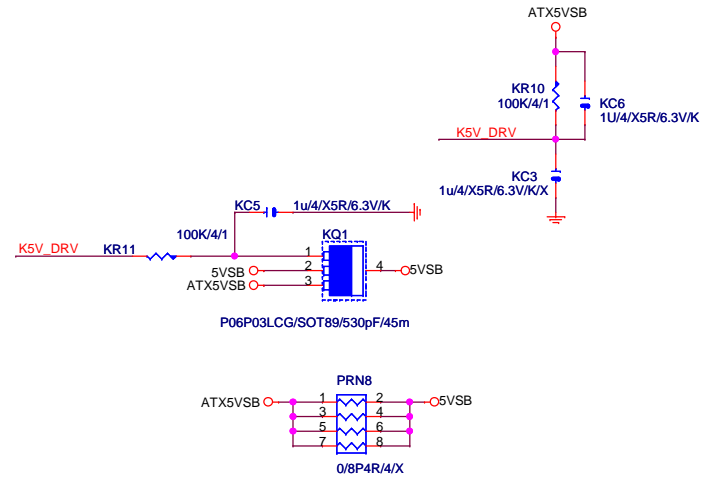
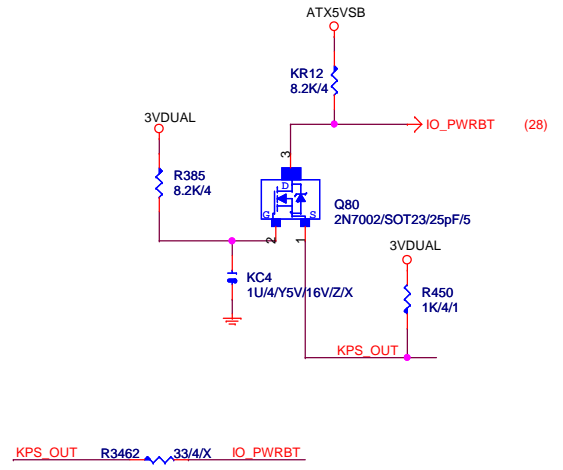








**Function Selection. Strapped by VSB**  
 Strapped to high :  
 DeepS5\_Sel = 1:  
 System will enter the deep S5 state after 6 sec delays when AC power on.  
 Strapped to low : (Default)  
 DeepS5\_Sel = 0:  
 System will not enter the deep S5 state when AC power on. System is in normal ACPI S5 state.



<b>GIGABYTE™</b>		
Title <b>EUP POWER</b>		
Size <b>B</b>	Document Number <b>MA770-ES3</b>	Rev <b>3.1</b>
Date: <b>Thursday, February 10, 2011</b>	Sheet <b>39</b>	of <b>39</b>