

Model Name: P35-DS3 Rev2.01

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	POWER MAP
05	P4 LGA775 A
06	P4 LGA775 B
07	P4 LGA775 C
08	P4 LGA775 D
09	GMCH-BEARLAKE HOST
10	GMCH-BEARLAKE DDRII
11	GMCH-BEARLAKE PCI E, DMI
12	GMCH-BEARLAKE INT VGA
13	GMCH-BEARLAKE GND
14	GMCH-BEARLAKE PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH9 PCI, USB, DMI, LAN
20	ICH9 GPIO, CTRL
21	ICH9 SATA, FAN PWM
22	ICH9 VCC, GND
23	CLOCK GEN CK505
24	PCI EXPRESS*1 ,PCI SLOT 1,2
25	ITE8718/GB,RESET DRIVE
26	COM,LPT
27	BIOS,CI ,HWM,KB/MS

SHEET TITLE

28	AZALIA ALC889A
29	AUDIO JACK
30	VCORE PWM ISL6327
31	DISCRETE POWER
32	ATX POWER
33	JMicron JMB363
34	LAN REALTEK RTL8111B
35	FRONT PANEL ,FUSB ,FDD

Gigabyte Technology

Title		Cover Sheet	
Size	Document Number	Rev	
Custom	P35-DS3	2.01	
Date:	Tuesday, August 14, 2007	Sheet	1 of 35

Circuit or PCB layout change for next version

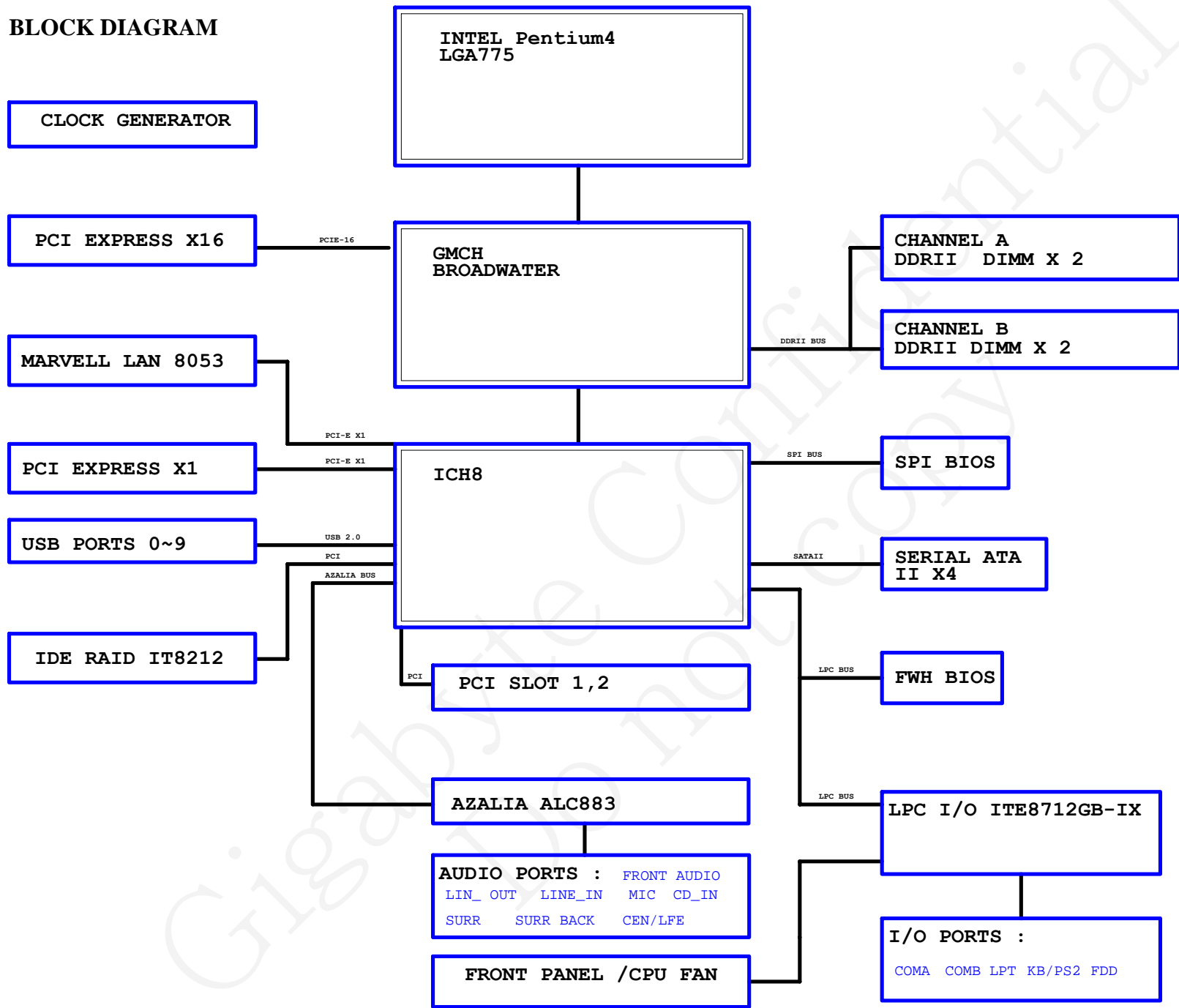
Component value change history

Data	Change Item	Reason
0.1A	EVT release	
0.2A	1. VTT_GMCH Q329 AP40T03 --> 2SK9918	
	2. VCORE CHOKE 0.5uH Footprint Change & 料號修改	
	3. IOUT DR100 100K --> 20K	
	4. PCB 智恩 REMOVE	
	5. PWM5, PWM6 阻值修改	
	6. CHOKE FOOTPRINT MODIFY	
	7. ADD COAXIAL:11NR6-501004-83R	
	8. REMOVE VGA , CHANGE TO COM	
	9. REMOVE HDMI_AC	
	10. PWM MOSFET MODIFY	
0.2B	1. BC115, BC729 2.2u/6/Y5V/10V/Z --> 2.2u/6/Y5V/6.3V/Z	
	2. ADD 8P4R(0402) 8.2K : 10RN3-048201-16R	
	3. ITE8718 REV.EX --> GX	
	4. U55只保留RT9199,其餘移除	
	5. VCC1_25 CAP 560uF --> 820uF	
1.0A	1. U55 ADD 替料 10GL2-206137-01R	
	2. UPDATE GMCH/A2 料號	
	3. ISL6545 OCP CHANGE R2007, R2009 15K/4 --> 8.2K/4	
	4. AP40T03H --> NEC3918	
	5. ALC889 PIN40 CR2 20K/4/1 --> 20K/4/0.1	
	6. VCORE MOSFET ADD VENDOR:INFINEO	
	7. RCA REMOVE 11NR6-501004-83R	
	8. 5VDUAL PROTECT R2057 390K/4 --> 150K/4	
1.0B	1. 增加包材	
	2. N/B CHANGE 新料號	
	3. MODIFY VCORE LOAD LINE RISISTOR	
	4. Q36 替料移除10GL6-501084-07R/09R	
	5. DU2, U50, U52 替料移除10TA1-200324-05R	
	6 -RSMRST C1329 0.1u/6 --> 0.01u/6	
	7. -PWRBTWS ADD 限流電阻 R2077=33/4	

DATE	Change Item	Reason
0.1	EVT release	
0.2	1. CHOKE 0.5uH 1.2uH 2uH Footprint Change	
	2. BSEL166_4 GP46 --> GP41	
	3. DDR18V_OV1~OV3 ITE8718 --> ICH9 GPIO	
	4. ADD CPU GTLREF_UV0~UV1 GPIO CONTROL	
1.0	1. Remove All 0 ohm	
	2. OS-CON CAP 底下的零件要移除 (AUDIO)	
	3. DL15 FOOTPRINT CHANGE "CHOKE08U-15A_1P-2"	
	4. LGA775 FOOTPRINT CHANGE "LGA775-39"	
	5. SB_HEATSINI --> SB_HEATSINK	
	6. BEARLAKE機種PCB要導入文字面	
	7. 5VDUAL PROTECT ADD D18	
1.01	1.北橋 HEATSINK 擋住 MODEL 文字面	
	2. DL9~DL14 "CHOKE05U-30A-1PQ-1" --> "CHOKE05U-30A-1PQ-2"	
	3. -PWRBTWS ADD 限流電阻 R2077=33/4	
1.02	1. 移除"Ultra Durable 2"	
	2. ADD NB_HEATSINK 外框	
	3. 文字面修改 DDRII 800/1066 (OC)--> DDRII 800/1066	
2.8	1. JMB363 CHANGE TO E-SATA	
	2. F_USB2,3 --> R_USB2,3	
	3. ADD OP+MOSFET補償線路	
	4. R.G.B & HDMI REMOVE	
	5. LPT CHANGE TO CONNECT 2*13K24	
	6. CHECNGE CONNECT FOR SPDIF I & SPDIF_O	
	7. RTL8111B & RTL8111C CO-LAYOUT	
2.81	1. JMB363 E-SATA --> ICH9R PORT4_5 E-SATA	2. RCA_SPDIF FOOTPRINT UPDATE
BOM		3. NB_HEATSINK 改 4上2下
P35-DS3R-10C	1. CPU GTLREF0~3 RATIO 0.67 --> 0.63 2. REMOVE VIN_CAP DBC3 1u/8	4. OP+MOSFET 補償線路修改
10D	1. EC176 560uF --> 820uF For VCC1_05 Shake	2.0
10E	1. REMOVE R2038 8.2K/4	1. JMB363 & ICH9R還原成REV1.02 2. 後齒改8個USB
1.02		3. RTL8111C CO-LAYOUT UPDATE
10G	1. PCB REV1.01 --> REV1.02	2.01 螺絲孔修改
10H	1. C1388 1u/6/Y5V/10V/Z --> 1u/6/X5R/10V/K (STR Fail on high temp.)	
2.8		
2.8A	1. PCB REV1.02 --> REV2.8	
28B	1. N/B HEATSINK 改成 I2SP2-040007-2*R 2. REMOVE R2078, R2079, R2080 20K/4/1 3. REMOVE C1427, C1428, C1429 1N/4/X7R/50V/K	
28C	1. PCB REV2.8 --> REV2.81	
20A	1. PCB REV2.0 --> 2.01 (螺絲孔修改) 2. 包材CHECK	
20A-DB	1. 包材修改	

Gigabyte Technology		
Title BOM & PCB MODIFY HISTORY		
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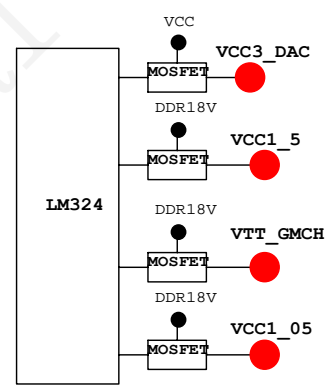
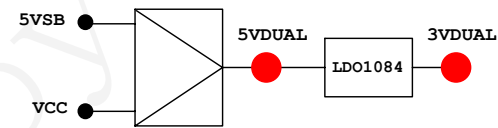
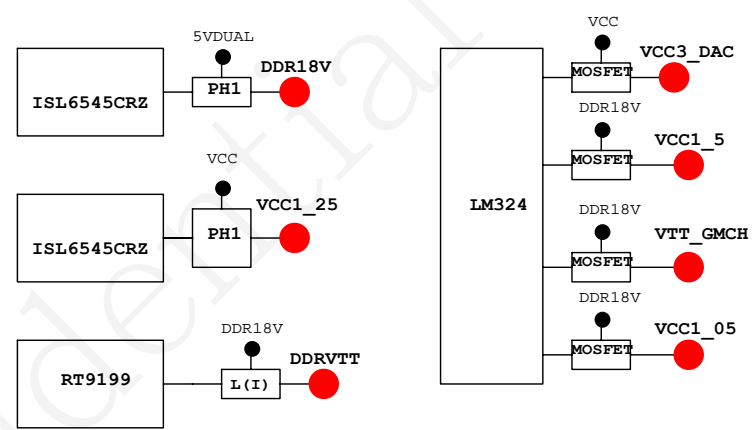
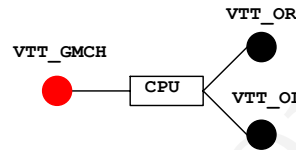
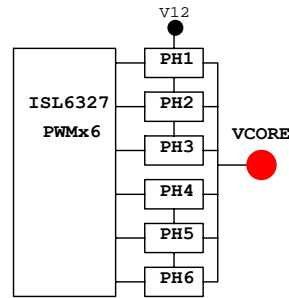
BLOCK DIAGRAM



ICH8 GPIO LIST TABLE

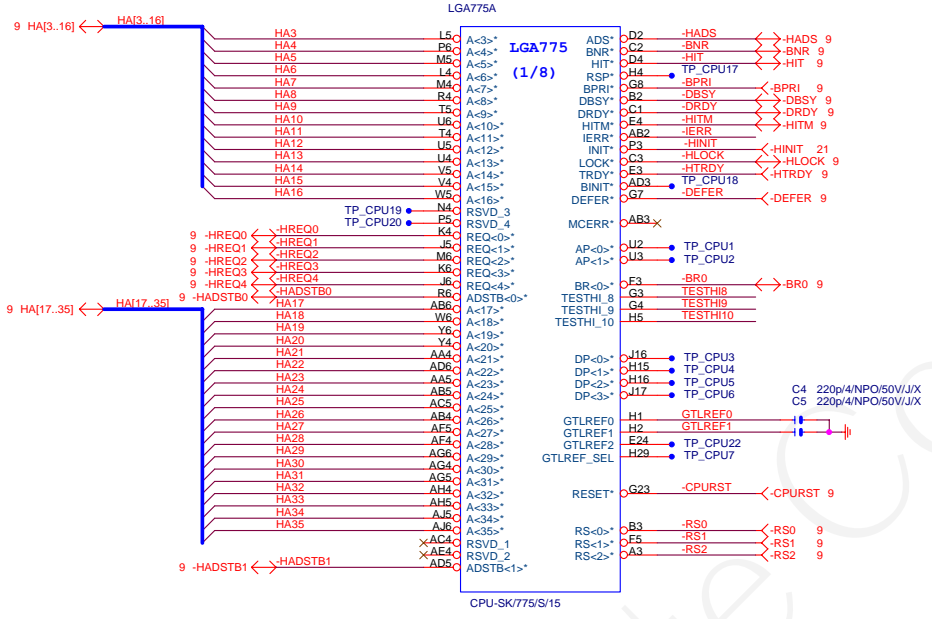
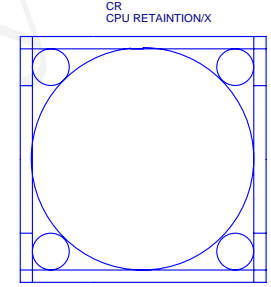
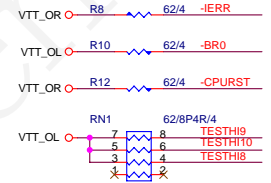
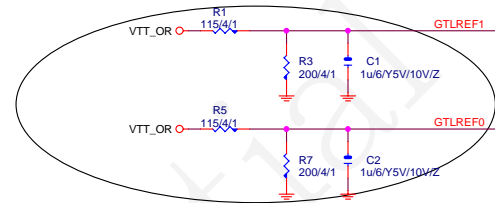
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8 (DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE (STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2 (STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27 (EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED (EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:6 PHASE PWM--ISL6327CRZ

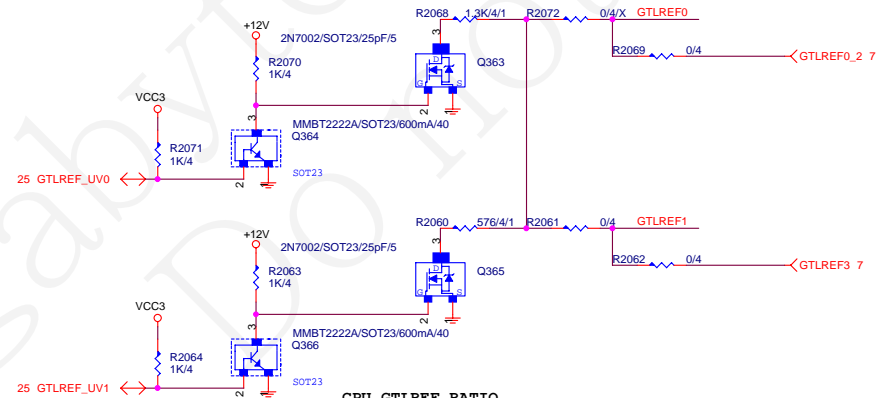
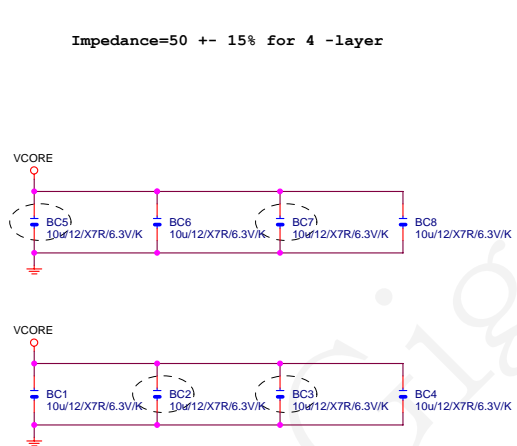


Gigabyte Technology			
Title			
TABLE LIST			
Size	Document Number	Rev	
B	P35-DS3	2.0	
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HA/REQ: 4/11 50+-15%
ADSTB: 4/14 50+-15%



Impedance=50 +- 15% for 4 -layer



CPU GTLREF RATIO

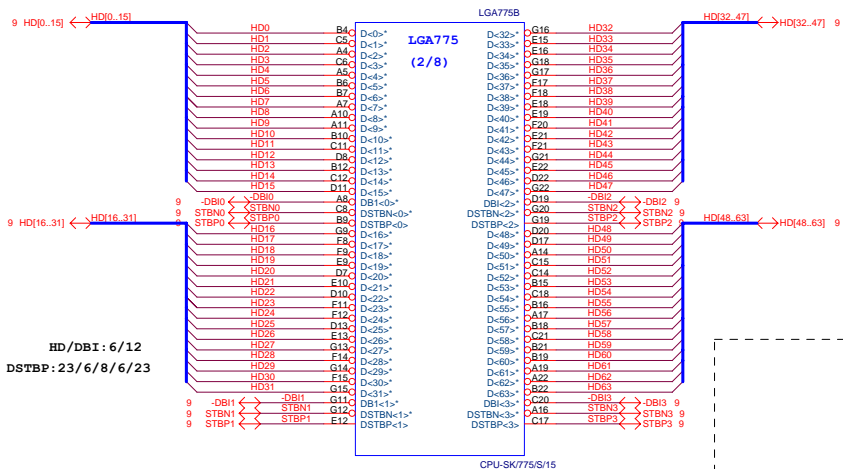
GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615

Gigabyte Technology

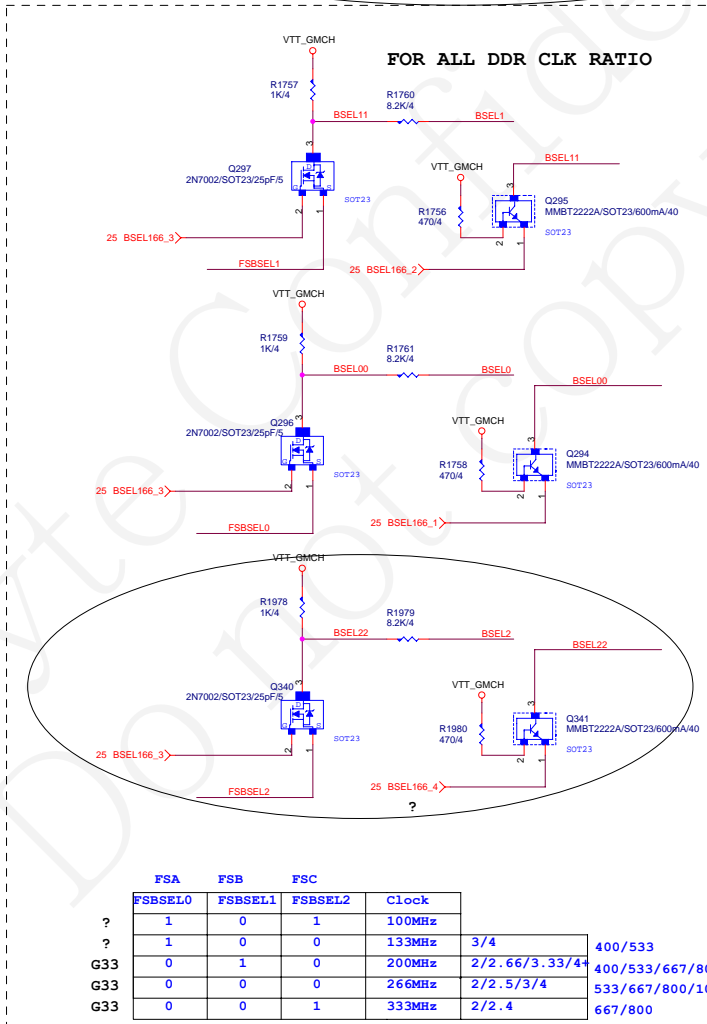
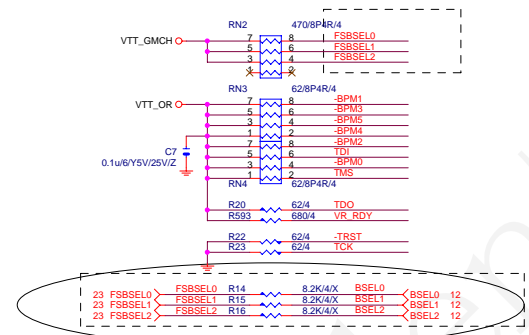
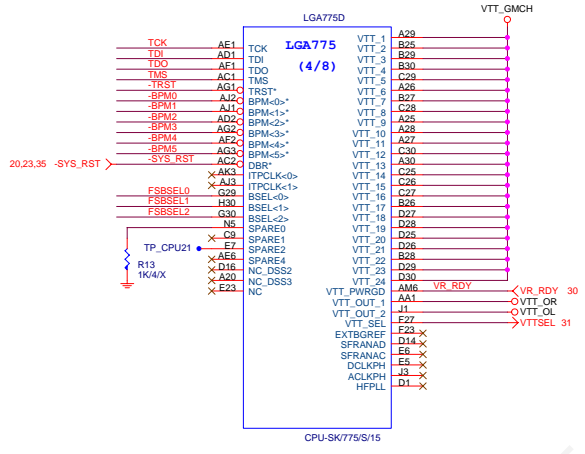
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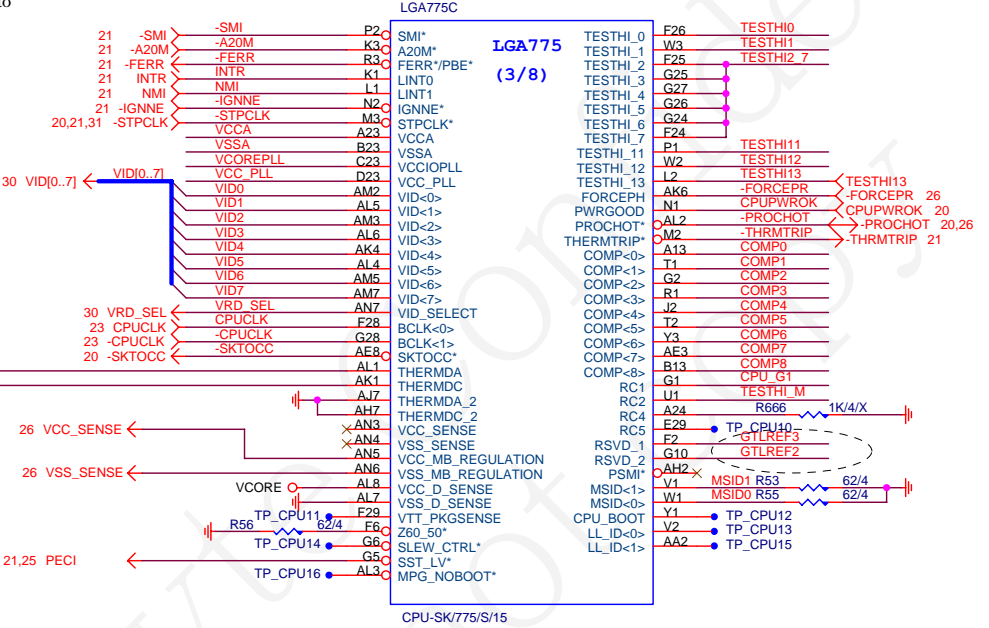
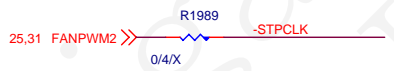
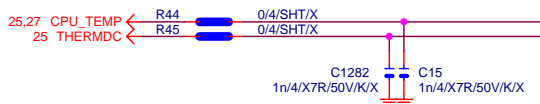
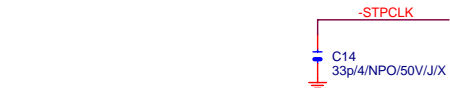
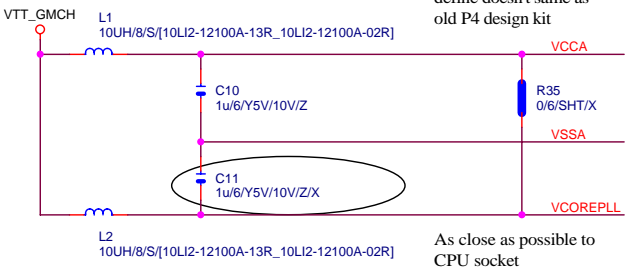
Size: Document Number P35-DS3 Rev 2.01

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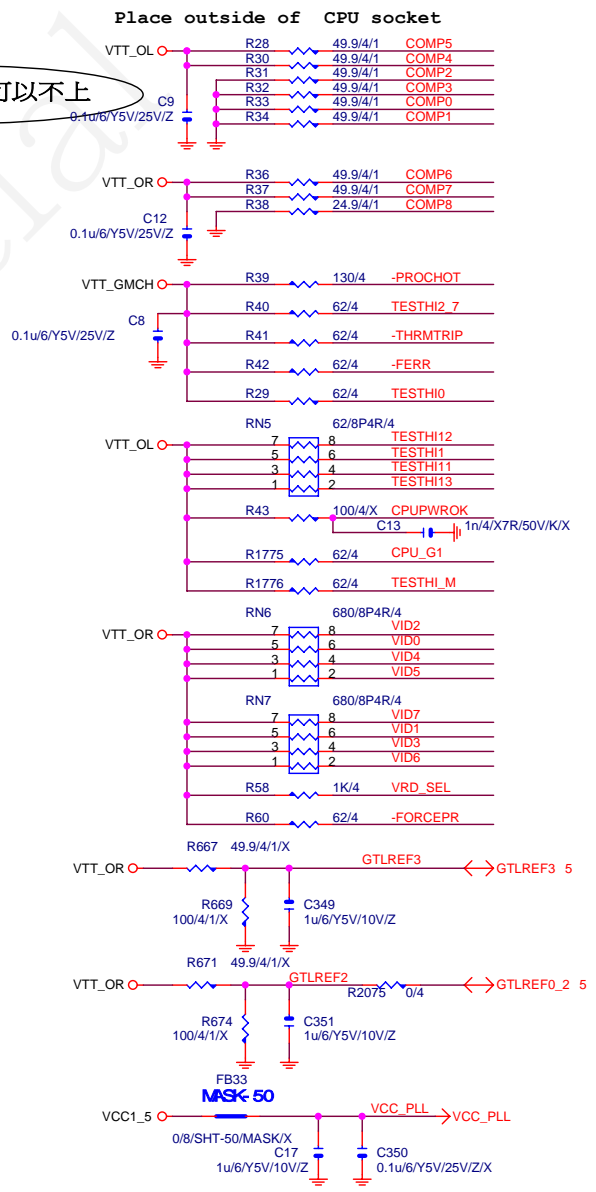


HD/DBI: 6/12
DSTBP: 23/6/8/6/23



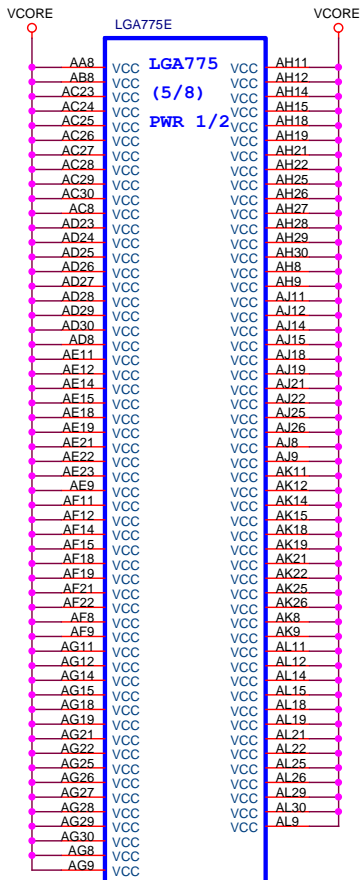


COMP4~7 可以不上

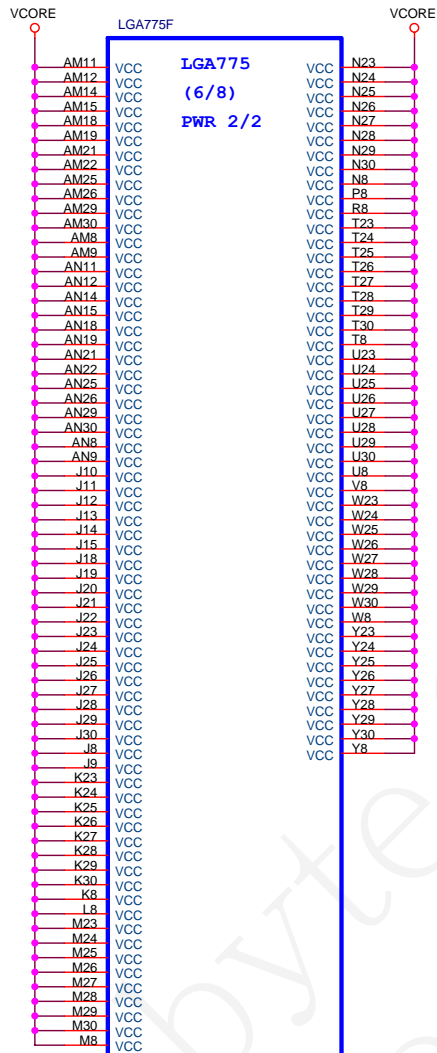


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Title P4_LGA775-C		
Size B	Document Number P35-DS3	Rev 2.0
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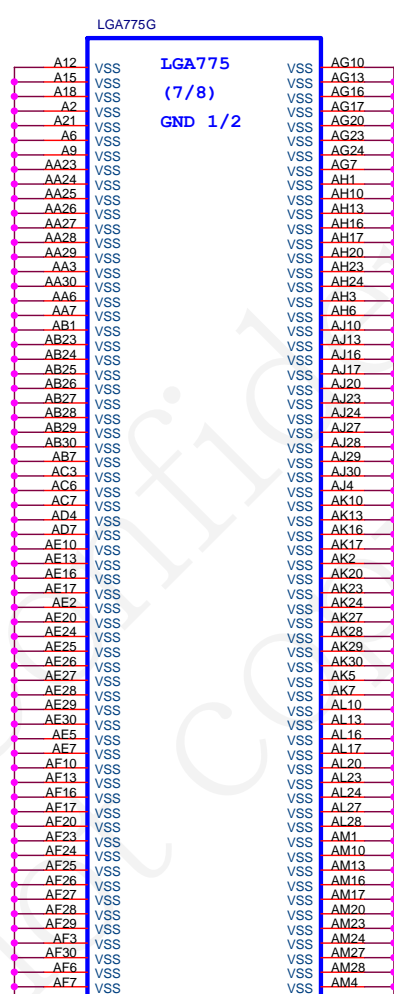
PECI: Platform Environment Control Interface



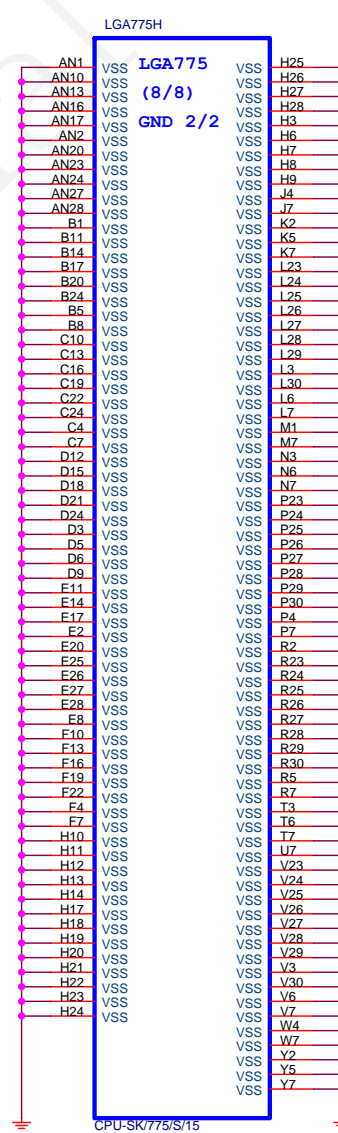
CPU-SK/775/S/15



CPU-SK/775/S/15



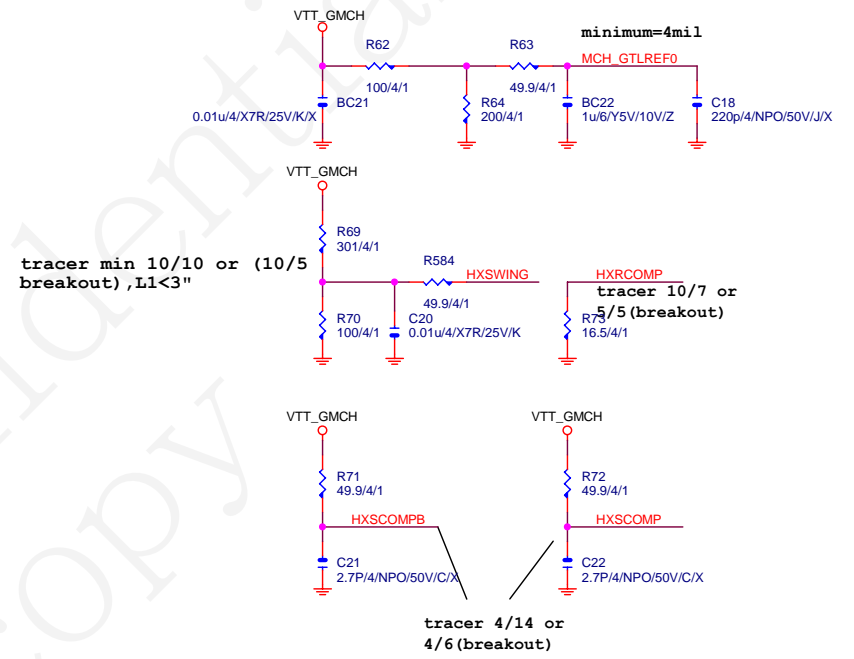
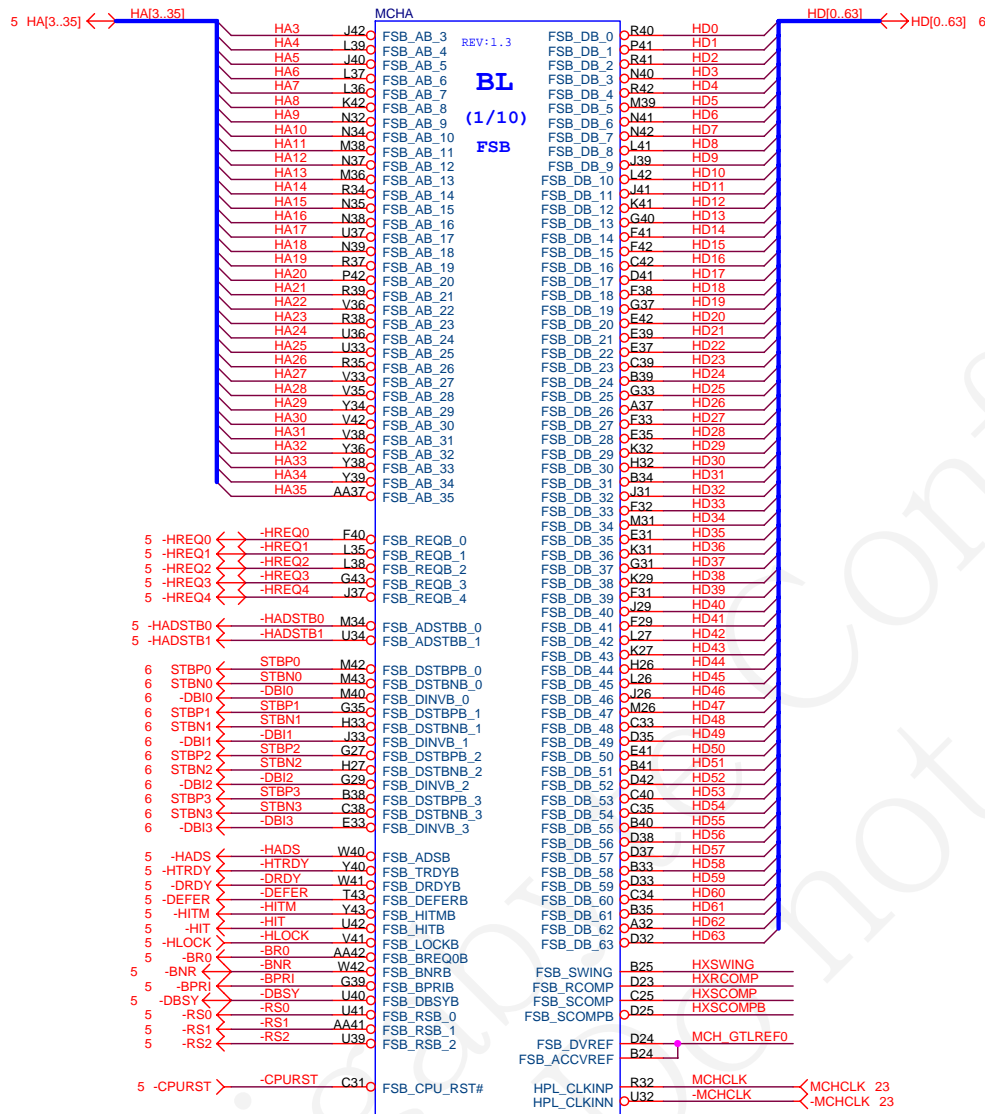
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CPU-SK/775/S/15

Gigabyte Technology

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Size	Document Number	P35-DS3	
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Gigabyte Technology		
Title GMCH-HOST		
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MCHB

REV:1.3
BL
(2/10)
DDR_A

Table of pin assignments for MCHB, including DDR_A, DDR_B, and various control signals like SWEA, SCSA, SBAA, CSAA, CKEA, MDT, DCLK, and AR.

6.5/5/6.5 Length max=5.0"
MCH die to DIMM0/1 pin =6" max
FOR channel A

LE82BLP-A2/BGA1226

DDR INTERFACE

MCHC

REV:1.3
BL
(3/10)
DDR_B

Table of pin assignments for MCHC, including DDR_B, DDR_C, and various control signals like SWEA, SCSA, SBAB, CSAB, CKEB, MDT, DCLK, and AR.

6.5/5/6.5 Length max=5.0"
MCH die to DIMM2/3 pin =7" max
FOR channel B

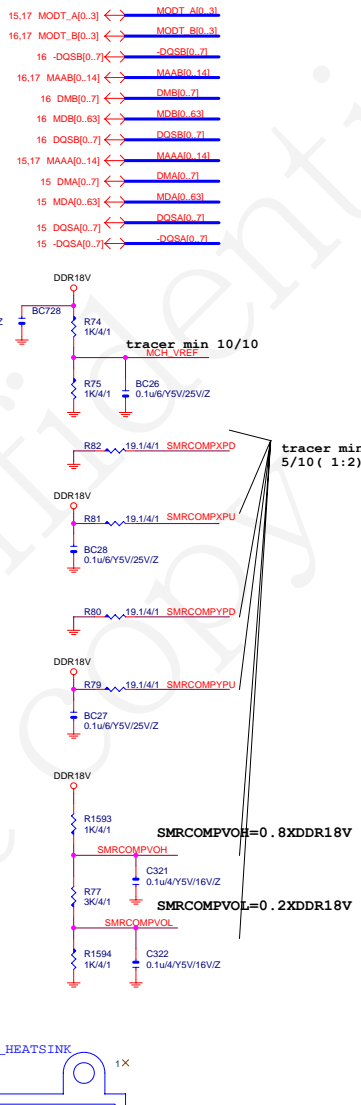
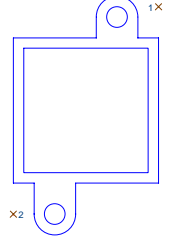
LE82BLP-A2/BGA1226

MCHD

REV:1.3
BL
(4/10)
DDR_C

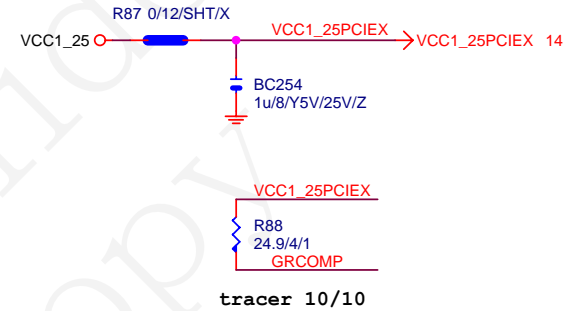
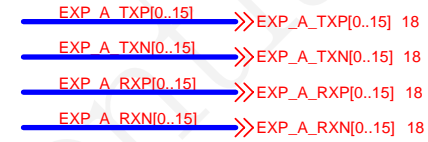
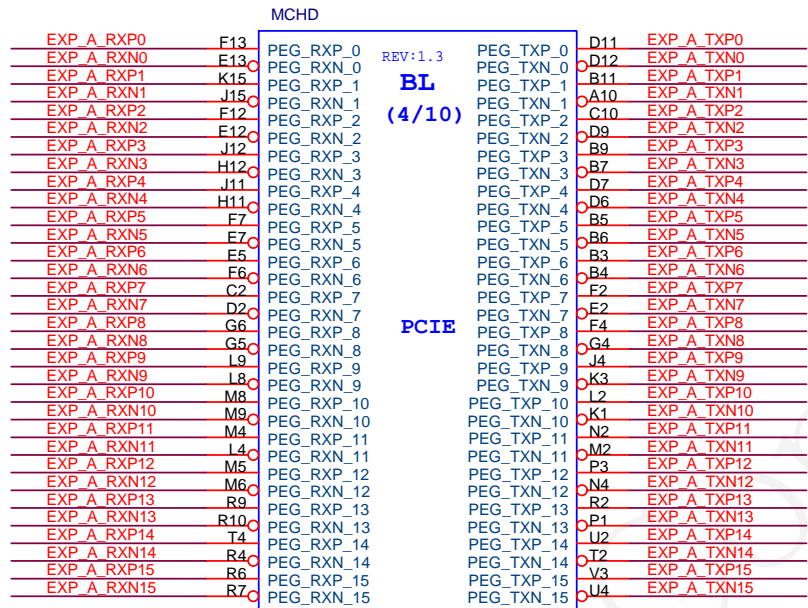
Table of pin assignments for MCHD, including DDR_C, DDR_D, and various control signals like SWEA, SCSA, SBAA, CSAA, CKEA, MDT, DCLK, and AR.

NB_HEATSINK(12SP2-040007-21R_12SP2-040007-22R_12SP2-040007-23R)

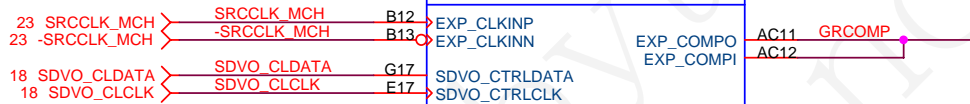
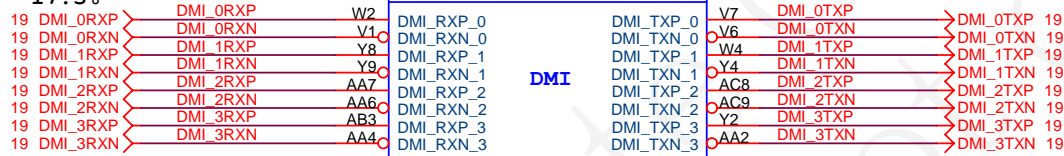


Gigabyte Technology logo and title block containing: Title: GMCH-DDRII, Document Number: P35-DS3, Date: Tuesday, August 14, 2007, Sheet: 10 of 35, Rev: 2.0

PCIE16:15/4/8/4/15
Impedance=95 +/- 17.5%



DMI:12/4/8/4/12
Impedance=95 +/- 17.5%



LE82BLP-A2/BGA1226

Gigabyte Technology		
Title: GMCH-PCI E & DMI		
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MCHG

REV:1.3

BL
(7/10)
GND

BC37	VSS_1	VSS_181	AE24
BC32	VSS_2	VSS_182	AE22
BC28	VSS_3	VSS_183	AE20
BC24	VSS_4	VSS_184	AE4
BC10	VSS_5	VSS_185	AE3
BC5	VSS_6	VSS_186	AE2
BB7	VSS_7	VSS_187	AD42
AY4	VSS_8	VSS_188	AD39
AW43	VSS_9	VSS_189	AD37
AW41	VSS_10	VSS_190	AD35
AV37	VSS_11	VSS_191	AD33
AV35	VSS_12	VSS_192	AD25
AV27	VSS_13	VSS_193	AD23
AV23	VSS_14	VSS_194	AD21
AV21	VSS_15	VSS_195	AD19
AV17	VSS_16	VSS_196	AC38
AV11	VSS_17	VSS_197	AC35
AV9	VSS_18	VSS_198	AC24
AV7	VSS_19	VSS_199	AC22
AV2	VSS_20	VSS_200	AC20
AU42	VSS_21	VSS_201	AC10
AU38	VSS_22	VSS_202	AC7
AU32	VSS_23	VSS_203	AC5
AU24	VSS_24	VSS_204	AB43
AU20	VSS_25	VSS_205	AB25
AU16	VSS_26	VSS_206	AB23
AU4	VSS_27	VSS_207	AB21
AT31	VSS_28	VSS_208	AB19
AT29	VSS_29	VSS_209	AB2
AT15	VSS_30	VSS_210	AB1
AT13	VSS_31	VSS_211	AA38
AT12	VSS_32	VSS_212	AA35
AR38	VSS_33	VSS_213	AA24
AR33	VSS_34	VSS_214	AA22
AR32	VSS_35	VSS_215	AA20
AR27	VSS_36	VSS_216	JA8
AR26	VSS_37	VSS_217	JA5
AR23	VSS_38	VSS_218	Y42
AR21	VSS_39	VSS_219	Y37
AR20	VSS_40	VSS_220	Y35
AR17	VSS_41	VSS_221	Y33
AR9	VSS_42	VSS_222	Y25
AR6	VSS_43	VSS_223	Y23
AP43	VSS_44	VSS_224	Y21
AP24	VSS_45	VSS_225	Y19
AP18	VSS_46	VSS_226	Y10
AP1	VSS_47	VSS_227	Y7
AN38	VSS_48	VSS_228	G38
AN31	VSS_49	VSS_229	G32
AN29	VSS_50	VSS_230	G21
AN24	VSS_51	VSS_231	G13
AN23	VSS_52	VSS_232	G12
AN20	VSS_53	VSS_233	G11
AN13	VSS_54	VSS_234	G9
AN12	VSS_55	VSS_235	G7
AN11	VSS_56	VSS_236	G1
AN4	VSS_57	VSS_237	F37
AM42	VSS_58	VSS_238	F35
AM40	VSS_59	VSS_239	F27
AM36	VSS_60	VSS_240	F21
AM33	VSS_61	VSS_241	F18
AM29	VSS_62	VSS_242	F15
AM24	VSS_63	VSS_243	F3
AM23	VSS_64	VSS_244	E43
AM20	VSS_65	VSS_245	E32
AM11	VSS_66	VSS_246	E24
AM9	VSS_67	VSS_247	E21
AM7	VSS_68	VSS_248	E11
AM4	VSS_69	VSS_249	E9
AL36	VSS_70	VSS_250	E8
AL33	VSS_71	VSS_251	E7
AL31	VSS_72	VSS_252	E3
AK43	VSS_73	VSS_253	E38
AJ39	VSS_74	VSS_254	U35
AJ36	VSS_75	VSS_255	U8
AJ33	VSS_76	VSS_256	U7
AJ32	VSS_77	VSS_257	U5
AH42	VSS_78	VSS_258	T42
AG37	VSS_79	VSS_259	T1
AG34	VSS_80	VSS_260	R36
AF43	VSS_81	VSS_261	R33
AF37	VSS_82	VSS_262	R31
AF36	VSS_83	VSS_263	R11
AF10	VSS_84	VSS_264	R8
AF9	VSS_85	VSS_265	R5
AF8	VSS_86	VSS_266	R3
AF7	VSS_87	VSS_267	C26
AF6	VSS_88	VSS_268	C11
AF5	VSS_89	VSS_269	C8
	VSS_90	VSS_270	C5

LE82BLP-A2/BGA1226

MCHH

REV:1.3

BL
(8/10)
GND

N5	VSS_91	VSS_271	B10
M37	VSS_92	VSS_272	A39
M35	VSS_93	VSS_273	A34
M33	VSS_94	VSS_274	A26
M27	VSS_95	VSS_275	A18
M21	VSS_96	VSS_276	A12
M20	VSS_97	VSS_277	A7
M17	VSS_98	VSS_278	BC41
M15	VSS_99	VSS_279	BC3
M10	VSS_100	VSS_280	BA1
M7	VSS_101	VSS_281	AY40
M1	VSS_102	VSS_282	AF23
L40	VSS_103	VSS_283	AF21
L33	VSS_104	VSS_284	AF19
L32	VSS_105	VSS_285	AE18
L31	VSS_106	VSS_286	AC18
L29	VSS_107	VSS_287	AA18
L24	VSS_108	VSS_288	V29
L20	VSS_109	VSS_289	U29
L11	VSS_110	VSS_290	U27
L7	VSS_111	VSS_291	R21
L5	VSS_112	VSS_292	E1
L3	VSS_113	VSS_293	C43
K43	VSS_114	VSS_294	C1
K26	VSS_115	VSS_295	A41
K21	VSS_116	VSS_296	A5
K18	VSS_117	VSS_297	A3
K13	VSS_118	VSS_298	
K12	VSS_119		V30
K2	VSS_120		
J38	VSS_121		
J35	VSS_122		
J32	VSS_123		
J27	VSS_124		
J21	VSS_125		
J9	VSS_126		
J7	VSS_127		
J5	VSS_128		
H31	VSS_129		
H29	VSS_130		
H21	VSS_131		
H20	VSS_132		
H17	VSS_133		
H15	VSS_134		
H13	VSS_135		
G42	VSS_136		
G38	VSS_137		
G32	VSS_138		
G21	VSS_139		
G13	VSS_140		
G12	VSS_141		
G11	VSS_142		
G9	VSS_143		
G7	VSS_144		
G1	VSS_145		
F37	VSS_146		
F35	VSS_147		
F27	VSS_148		
F21	VSS_149		
F18	VSS_150		
F15	VSS_151		
F3	VSS_152		
E43	VSS_153		
E32	VSS_154		
E24	VSS_155		
E21	VSS_156		
E11	VSS_157		
E9	VSS_158		
E8	VSS_159		
E7	VSS_160		
E3	VSS_161		
E38	VSS_162		
U35	VSS_163		
U8	VSS_164		
U7	VSS_165		
U5	VSS_166		
T42	VSS_167		
T1	VSS_168		
R36	VSS_169		
R33	VSS_170		
R31	VSS_171		
R11	VSS_172		
R8	VSS_173		
R5	VSS_174		
R3	VSS_175		
C26	VSS_176		
C11	VSS_177		
C8	VSS_178		
C5	VSS_179		
C4	VSS_180????		
B37			
B32			
B31			
B26			
B23			
B22			
B19			
B14			
N7			
M11			

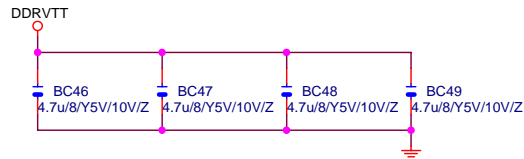
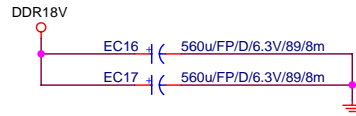
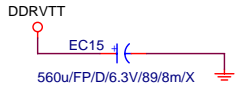
LE82BLP-A2/BGA1226

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Title		
GMCH-GND		
Size	Document Number	Rev
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Date:	Tuesday, August 14, 2007	Sheet 13 of 35

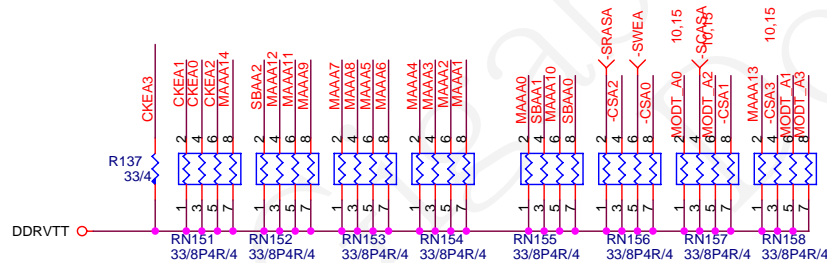
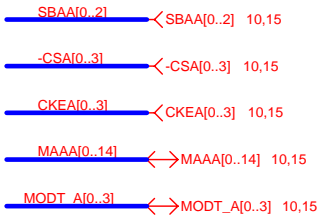
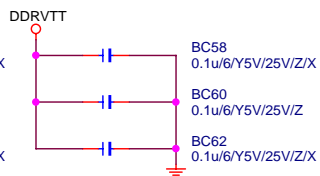
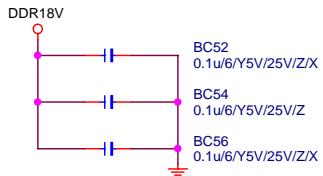
DDR TERMINATION CHANNEL A

DDRVTT Decouple



DDR18V Decouple

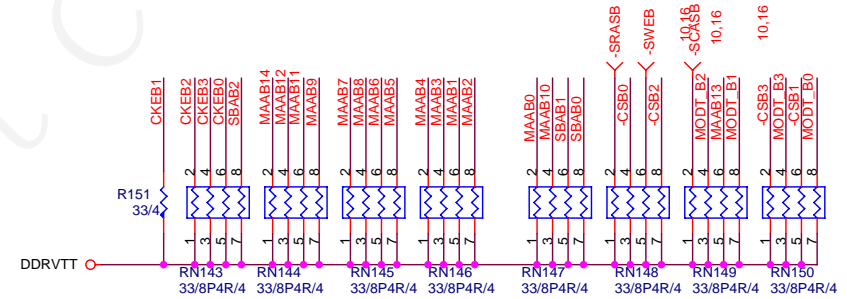
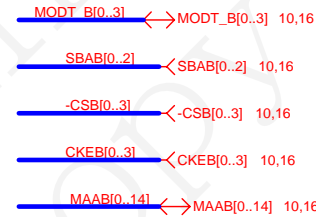
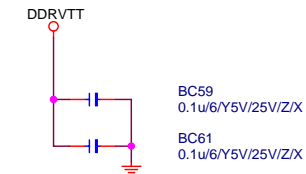
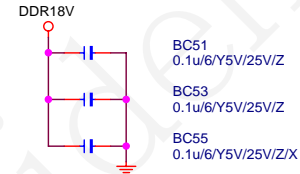
DDRVTT Decouple



DDR TERMINATION CHANNEL B

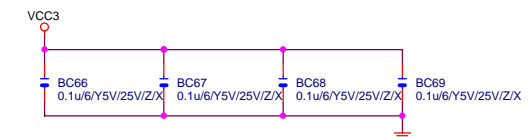
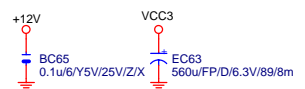
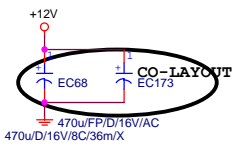
DDR18V Decouple

DDRVTT Decouple



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Title		
DDRII TERMINATOR		
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PCIE16:15/4/8/4/15

EXP_A_TXP[0..15] >>> EXP_A_TXP[0..15] 11
 EXP_A_TXN[0..15] >>> EXP_A_TXN[0..15] 11

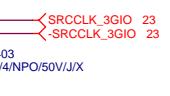
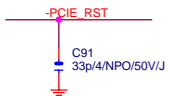
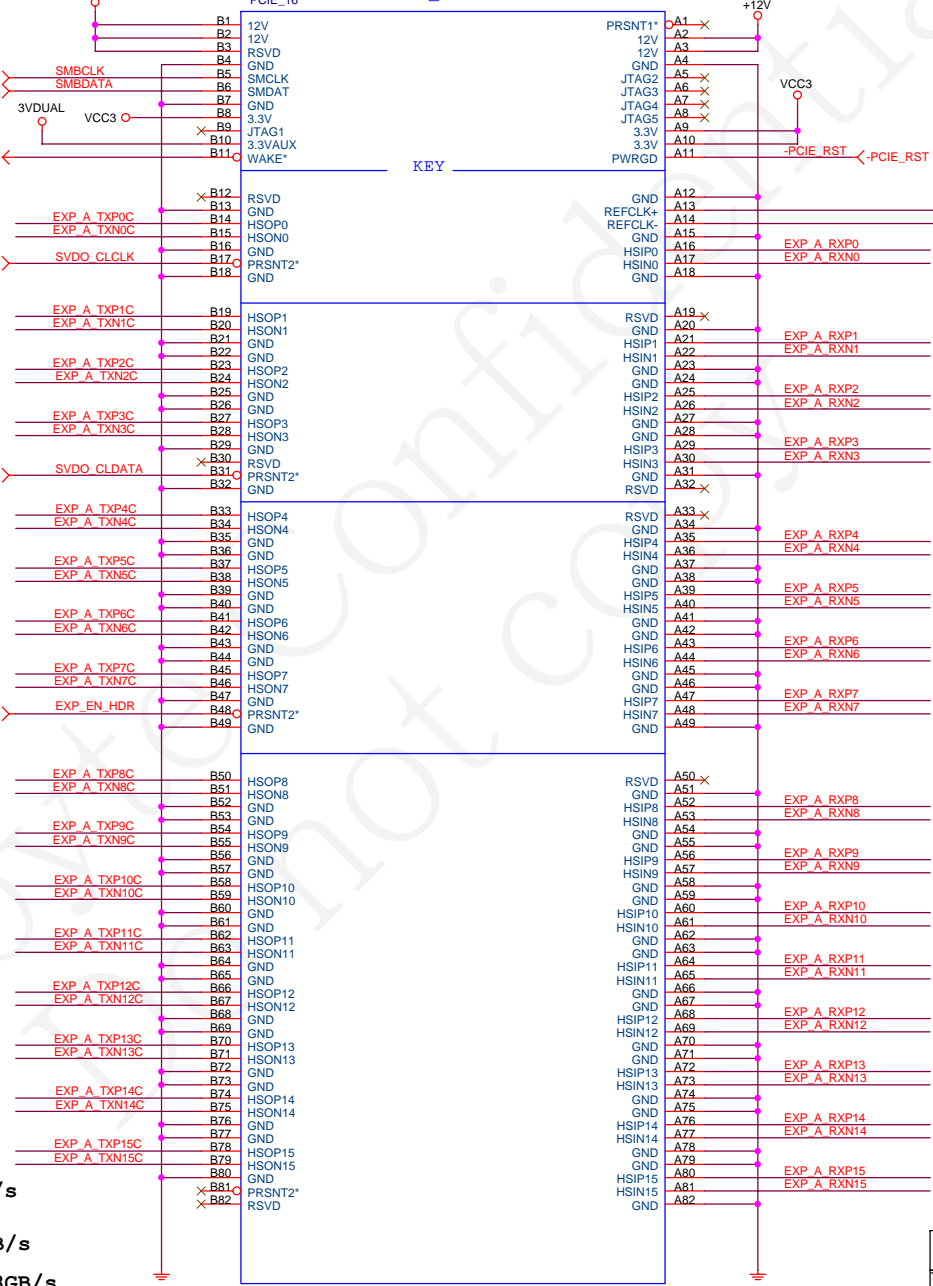
EXP_A_TXP0	C92	0.1u4/Y5V/16V/Z	EXP_A_TXP0C
EXP_A_TXN0	C93	0.1u4/Y5V/16V/Z	EXP_A_TXN0C
EXP_A_TXP1	C94	0.1u4/Y5V/16V/Z	EXP_A_TXP1C
EXP_A_TXN1	C95	0.1u4/Y5V/16V/Z	EXP_A_TXN1C
EXP_A_TXP2	C96	0.1u4/Y5V/16V/Z	EXP_A_TXP2C
EXP_A_TXN2	C97	0.1u4/Y5V/16V/Z	EXP_A_TXN2C
EXP_A_TXP3	C98	0.1u4/Y5V/16V/Z	EXP_A_TXP3C
EXP_A_TXN3	C99	0.1u4/Y5V/16V/Z	EXP_A_TXN3C
EXP_A_TXP4	C100	0.1u4/Y5V/16V/Z	EXP_A_TXP4C
EXP_A_TXN4	C101	0.1u4/Y5V/16V/Z	EXP_A_TXN4C
EXP_A_TXP5	C102	0.1u4/Y5V/16V/Z	EXP_A_TXP5C
EXP_A_TXN5	C103	0.1u4/Y5V/16V/Z	EXP_A_TXN5C
EXP_A_TXP6	C104	0.1u4/Y5V/16V/Z	EXP_A_TXP6C
EXP_A_TXN6	C105	0.1u4/Y5V/16V/Z	EXP_A_TXN6C
EXP_A_TXP7	C106	0.1u4/Y5V/16V/Z	EXP_A_TXP7C
EXP_A_TXN7	C107	0.1u4/Y5V/16V/Z	EXP_A_TXN7C
EXP_A_TXP8	C108	0.1u4/Y5V/16V/Z	EXP_A_TXP8C
EXP_A_TXN8	C109	0.1u4/Y5V/16V/Z	EXP_A_TXN8C
EXP_A_TXP9	C110	0.1u4/Y5V/16V/Z	EXP_A_TXP9C
EXP_A_TXN9	C111	0.1u4/Y5V/16V/Z	EXP_A_TXN9C
EXP_A_TXP10	C112	0.1u4/Y5V/16V/Z	EXP_A_TXP10C
EXP_A_TXN10	C113	0.1u4/Y5V/16V/Z	EXP_A_TXN10C
EXP_A_TXP11	C114	0.1u4/Y5V/16V/Z	EXP_A_TXP11C
EXP_A_TXN11	C115	0.1u4/Y5V/16V/Z	EXP_A_TXN11C
EXP_A_TXP12	C116	0.1u4/Y5V/16V/Z	EXP_A_TXP12C
EXP_A_TXN12	C117	0.1u4/Y5V/16V/Z	EXP_A_TXN12C
EXP_A_TXP13	C118	0.1u4/Y5V/16V/Z	EXP_A_TXP13C
EXP_A_TXN13	C119	0.1u4/Y5V/16V/Z	EXP_A_TXN13C
EXP_A_TXP14	C120	0.1u4/Y5V/16V/Z	EXP_A_TXP14C
EXP_A_TXN14	C121	0.1u4/Y5V/16V/Z	EXP_A_TXN14C
EXP_A_TXP15	C122	0.1u4/Y5V/16V/Z	EXP_A_TXP15C
EXP_A_TXN15	C123	0.1u4/Y5V/16V/Z	EXP_A_TXN15C

11 SDVO_CLK >>> SVDO_CLK

11 SDVO_CLDATA >>> SVDO_CLDATA

12 EXP_EN_HDR >>> EXP_EN_HDR

PCIESLOT-164DN-2 3GIO_*16



EXP_A_RXP[0..15] >>> EXP_A_RXP[0..15] 11
 EXP_A_RXN[0..15] >>> EXP_A_RXN[0..15] 11

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1 (單向) BANDWIDTH=2.5GHZ*(8b/10b)=2Gb/s=250MB/s

PCE-E X1 (雙向) BANDWIDTH=2.5GHZ*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16 (單向) BANDWIDTH=2.5GHZ*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16 (雙向) BANDWIDTH=2.5GHZ*(8b/10b)X16X2=64Gb/s=8GB/s

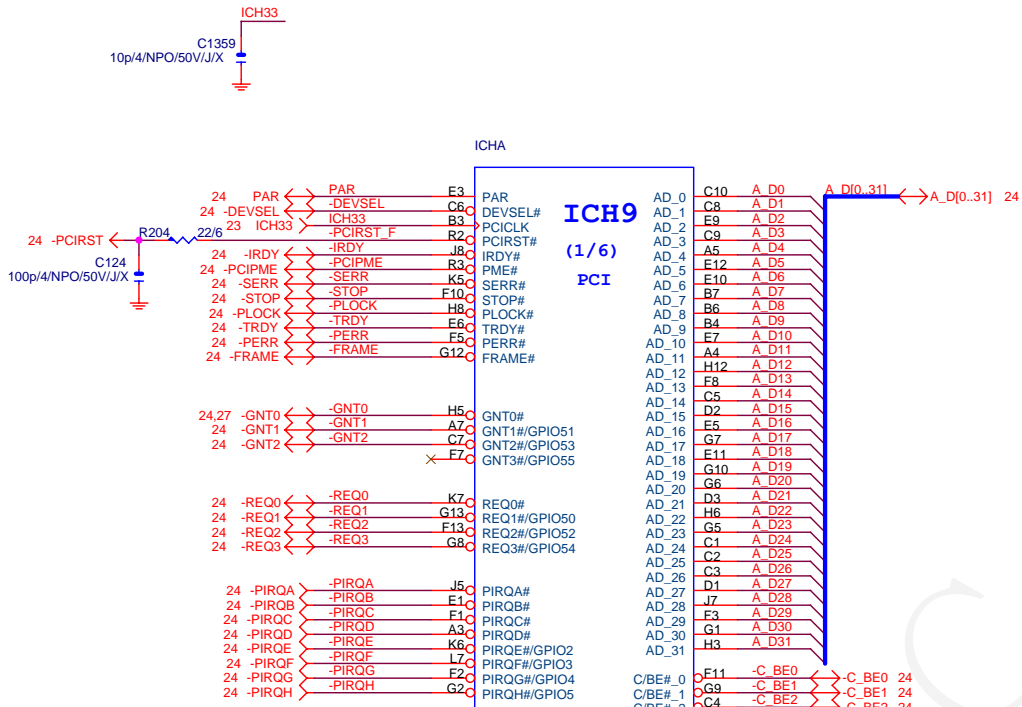
PCI-E REV:2.0--> 5GHZ

PCI-E/16X-164P/BU-297C/RIGHT PUSH

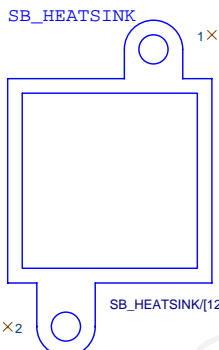
Gigabyte Technology

PCI EXPRESS * 16

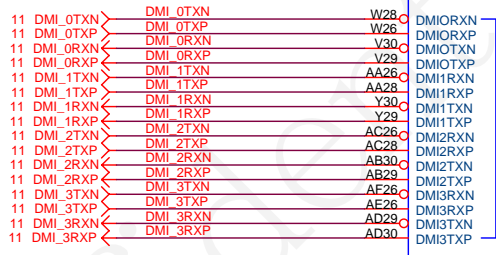
Title		P35-DS3		Rev	2.01
Size	Document Number	P35-DS3			
Custom					
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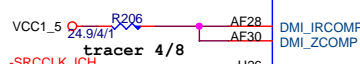
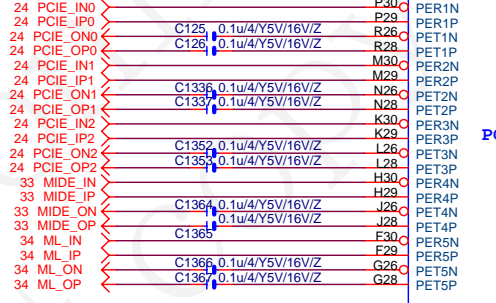
NH82801IB-A2/BGA676/[10HB1-038280-90R]



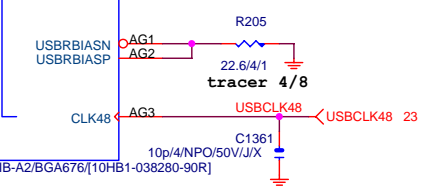
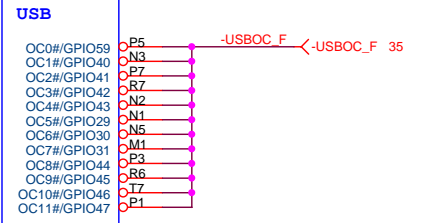
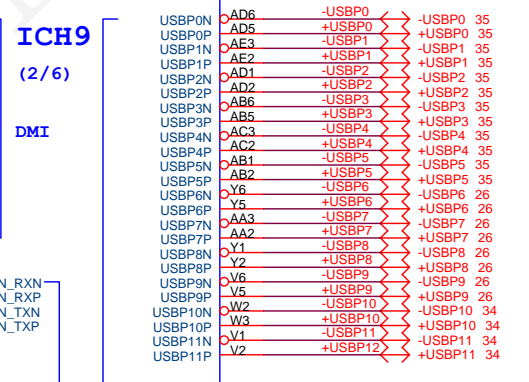
DMI:12/4/8/4/12
Impedance=95 +- 17.5%



PCIE X1 :15/4/8/4/15
Impedance=95 +- 17.5%



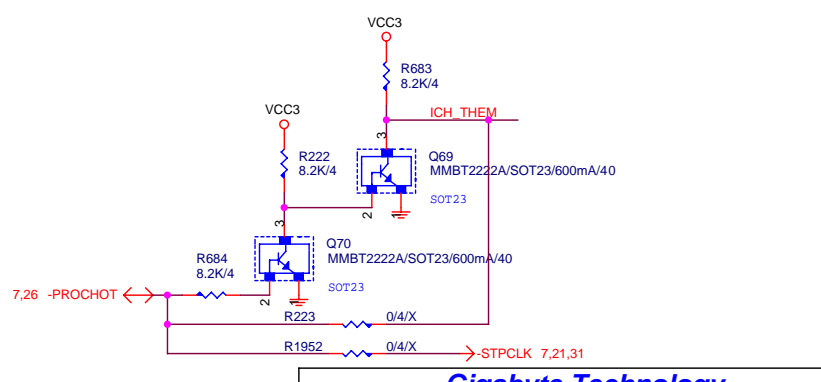
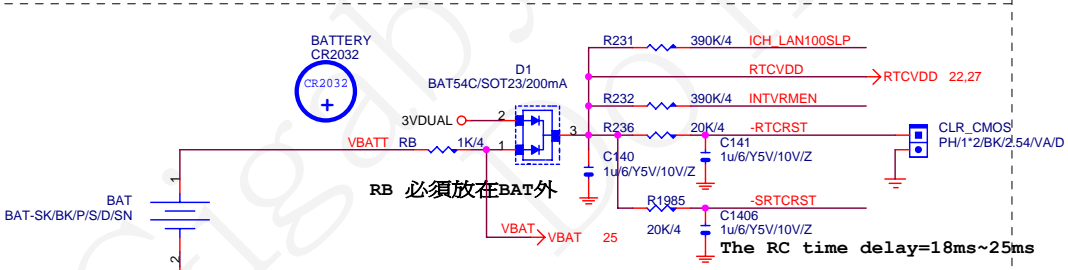
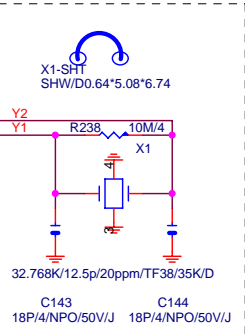
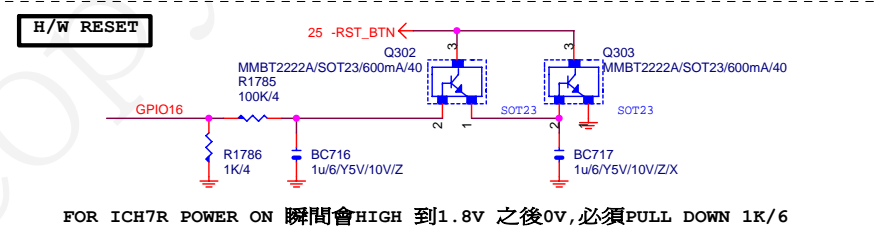
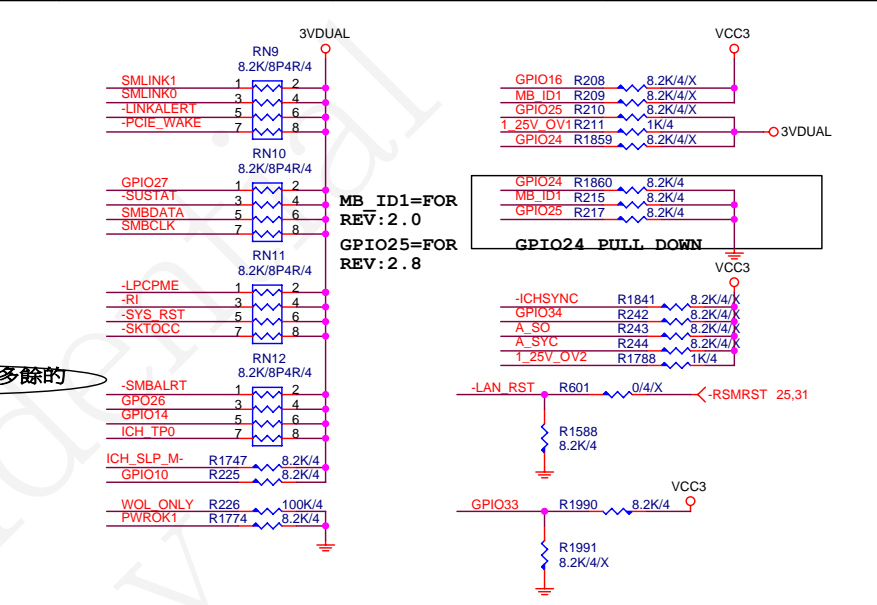
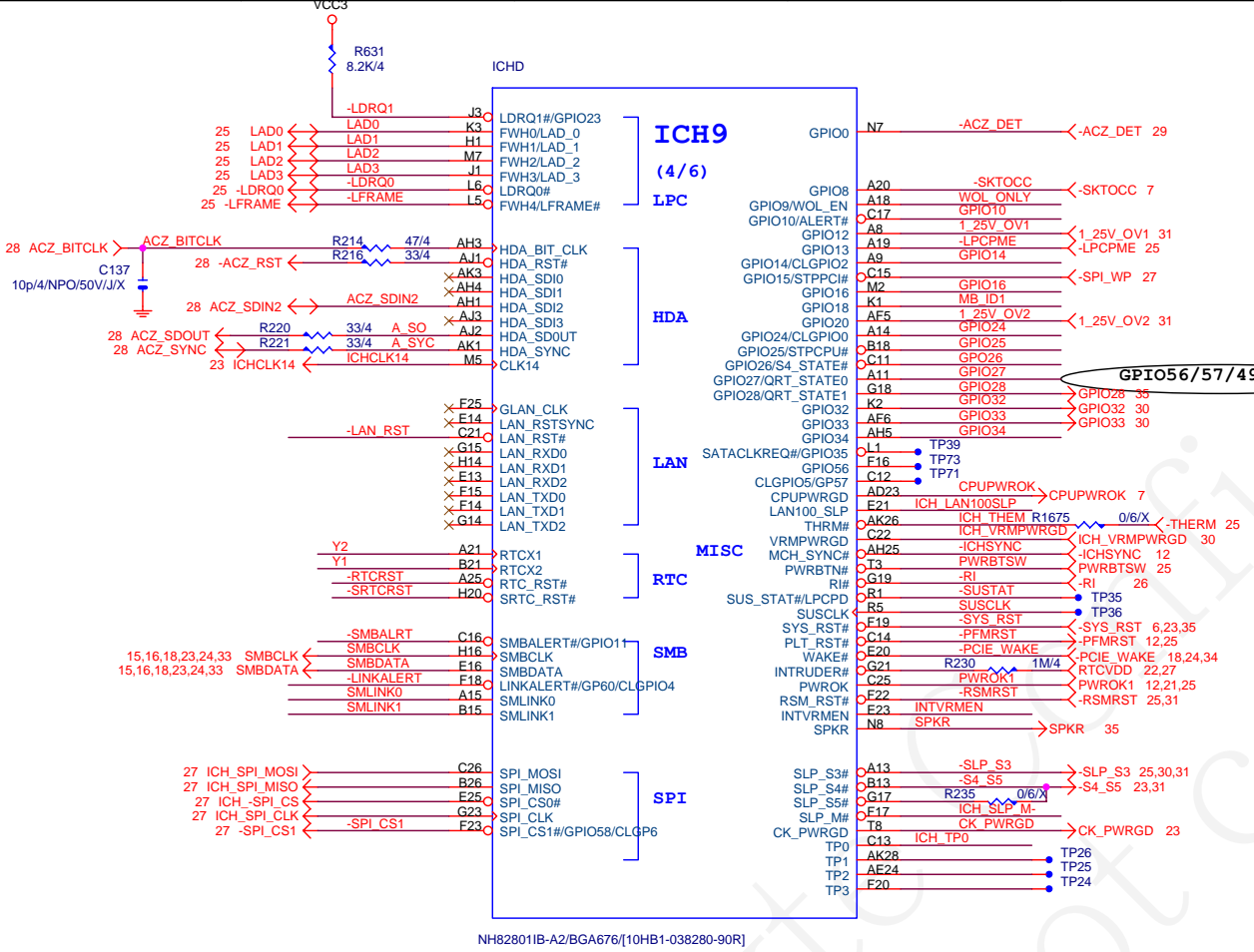
ICHB
USB:15/4.5/7.5/4.5/15
Impedance=90+- 15%



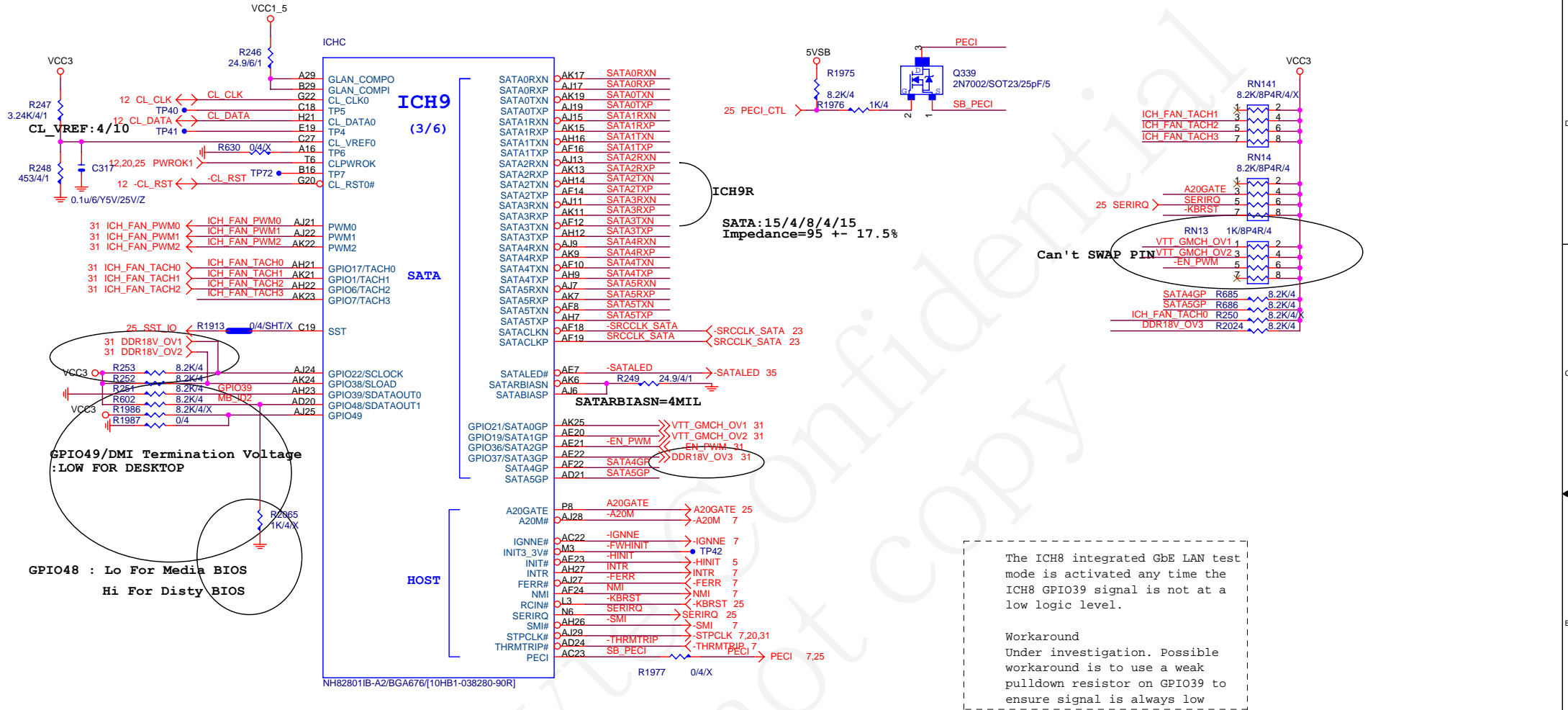
NH82801IB-A2/BGA676/[10HB1-038280-90R]

Gigabyte Technology

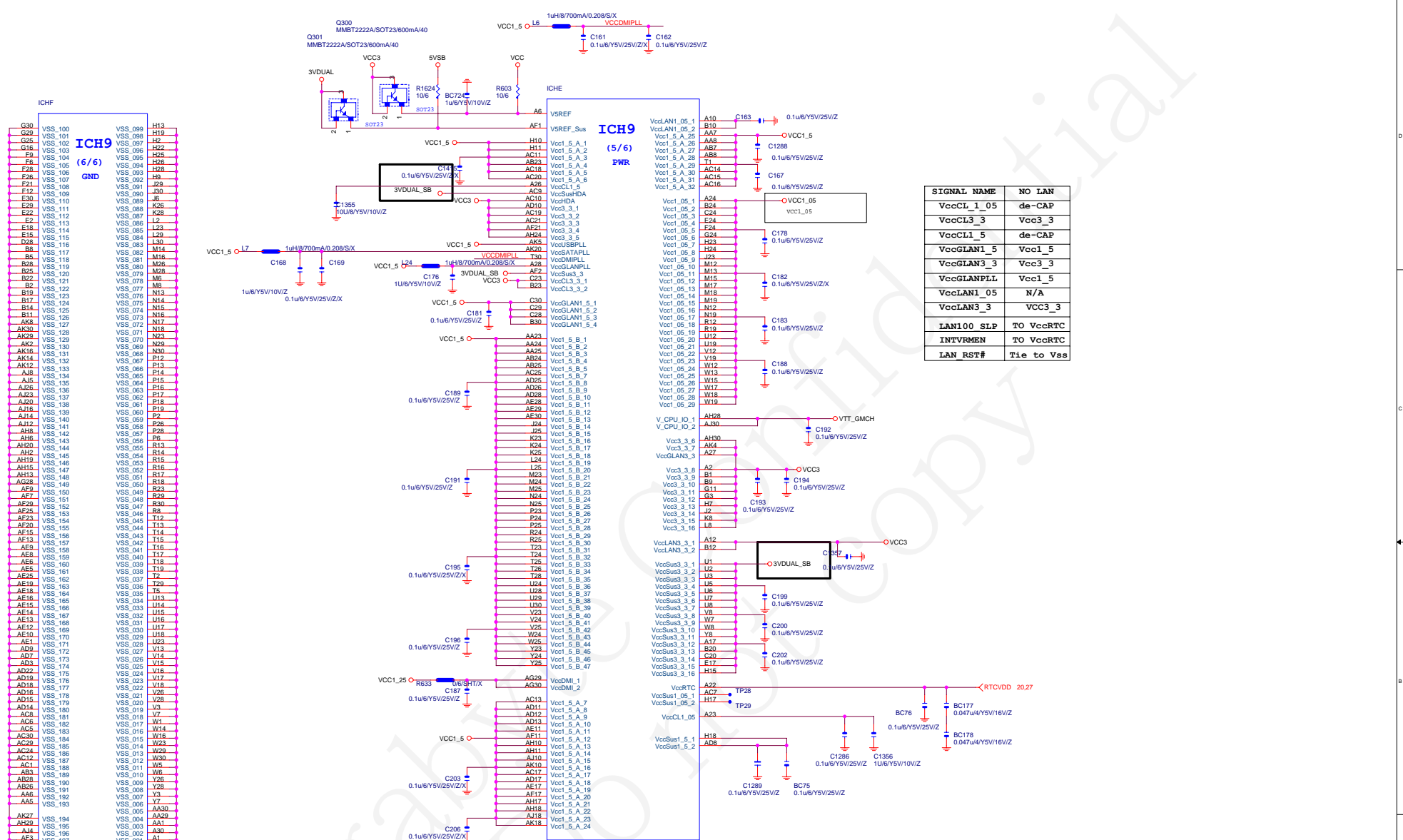
Title		
ICH9-PCI, DMI, LAN, USB		
Size	Document Number	Rev
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Title: ICH9 GPIO, CTRL			
Size: B	Document Number: P35-DS3	Rev: 2.0	
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ICH9- SATA, FAN CTRL			
Size B	Document Number	P35-DS3	
Date:	Tuesday, August 14, 2007	Sheet	21 of 35
			Rev 2.0



IC#	Pin	Signal
G30	VSS_100	ICH9
G29	VSS_101	ICH9
G25	VSS_102	ICH9
G16	VSS_103	ICH9
F9	VSS_104	ICH9
F8	VSS_105	ICH9
F28	VSS_106	ICH9
F27	VSS_107	ICH9
F21	VSS_108	ICH9
F12	VSS_109	ICH9
E30	VSS_110	ICH9
E22	VSS_111	ICH9
E18	VSS_112	ICH9
E2	VSS_113	ICH9
E15	VSS_114	ICH9
D28	VSS_115	ICH9
D8	VSS_116	ICH9
B8	VSS_117	ICH9
B5	VSS_118	ICH9
B28	VSS_119	ICH9
B25	VSS_120	ICH9
B22	VSS_121	ICH9
B2	VSS_122	ICH9
B19	VSS_123	ICH9
B17	VSS_124	ICH9
B14	VSS_125	ICH9
B11	VSS_126	ICH9
B5	VSS_127	ICH9
AK8	VSS_128	ICH9
AK30	VSS_129	ICH9
AK29	VSS_130	ICH9
AK2	VSS_131	ICH9
AK16	VSS_132	ICH9
AK14	VSS_133	ICH9
AK12	VSS_134	ICH9
A48	VSS_135	ICH9
A35	VSS_136	ICH9
A28	VSS_137	ICH9
A23	VSS_138	ICH9
A20	VSS_139	ICH9
A16	VSS_140	ICH9
A14	VSS_141	ICH9
A12	VSS_142	ICH9
A8	VSS_143	ICH9
A6	VSS_144	ICH9
A4	VSS_145	ICH9
A2	VSS_146	ICH9
AH9	VSS_147	ICH9
AH3	VSS_148	ICH9
AG28	VSS_149	ICH9
AF7	VSS_150	ICH9
AF5	VSS_151	ICH9
AF23	VSS_152	ICH9
AF5	VSS_153	ICH9
AF15	VSS_154	ICH9
AF13	VSS_155	ICH9
AE9	VSS_156	ICH9
AE8	VSS_157	ICH9
AE8	VSS_158	ICH9
AE5	VSS_159	ICH9
AE5	VSS_160	ICH9
AE19	VSS_161	ICH9
AE16	VSS_162	ICH9
AE15	VSS_163	ICH9
AE14	VSS_164	ICH9
AE13	VSS_165	ICH9
AE12	VSS_166	ICH9
AE10	VSS_167	ICH9
AD9	VSS_168	ICH9
AD7	VSS_169	ICH9
AD3	VSS_170	ICH9
AD2	VSS_171	ICH9
AD16	VSS_172	ICH9
AD15	VSS_173	ICH9
AD15	VSS_174	ICH9
AD15	VSS_175	ICH9
AD16	VSS_176	ICH9
AD16	VSS_177	ICH9
AD15	VSS_178	ICH9
AD15	VSS_179	ICH9
AC8	VSS_180	ICH9
AC6	VSS_181	ICH9
AC6	VSS_182	ICH9
AC5	VSS_183	ICH9
AC4	VSS_184	ICH9
AC24	VSS_185	ICH9
AC12	VSS_186	ICH9
AC1	VSS_187	ICH9
AB3	VSS_188	ICH9
AB28	VSS_189	ICH9
AB26	VSS_190	ICH9
AA6	VSS_191	ICH9
AA5	VSS_192	ICH9
AA5	VSS_193	ICH9
AK27	VSS_194	ICH9
AH29	VSS_195	ICH9
A4	VSS_196	ICH9
AE3	VSS_197	ICH9
B27	VSS_198	ICH9

SIGNAL_NAME	NO LAN
VccCL1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3_3
LAN100_SLP	TO VccRTC
INTVRMEN	TO VccRTC
LAN_RST#	Tie to Vss

NH62801B-A2/BGA676(10HBI-038280-90R)

NH62801B-A2/BGA676(10HBI-038280-90R)

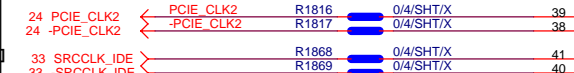
50歐母: [18/4/10/4/18]



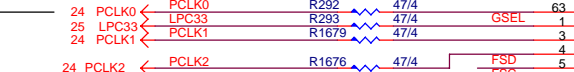
50歐母: [18/4/10/4/18]



50歐母: [18/4/10/4/18]



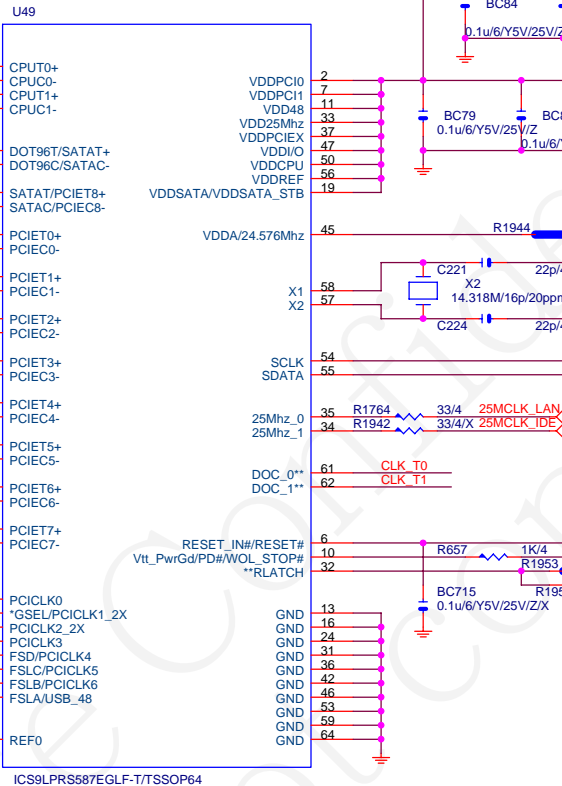
50歐母: [4/10]



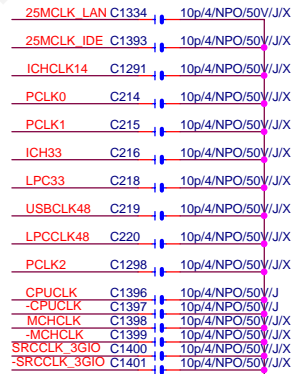
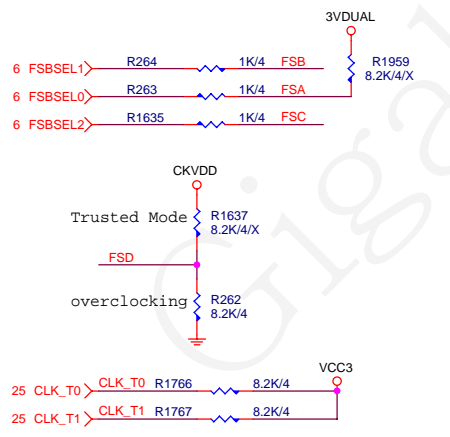
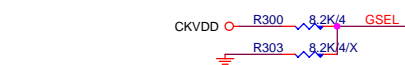
50歐母: [4/10]



50歐母: [4/10]



GSEL=1,96Mhz from 14/15,SATACLK from 17/18
GSEL=0,SATACLK from 14/15,PCIECLK from 17/18



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CK505 CLK GEN

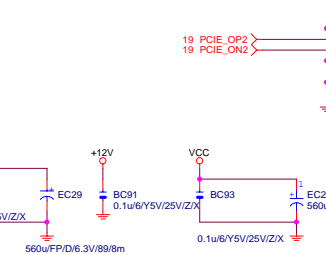
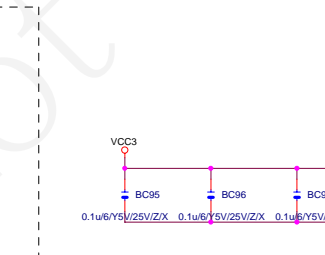
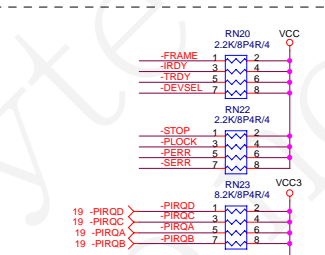
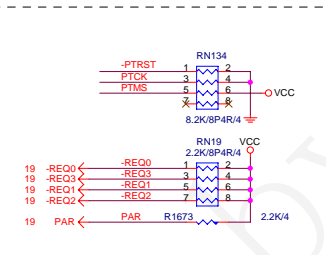
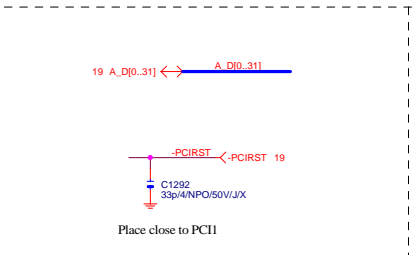
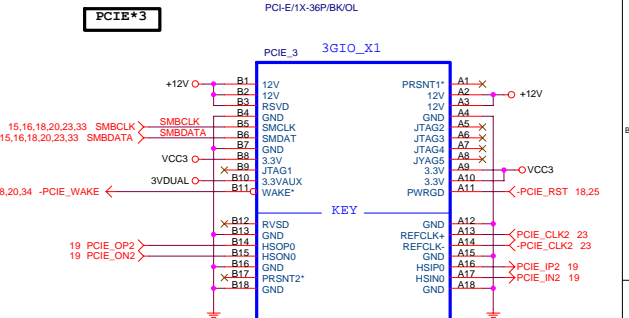
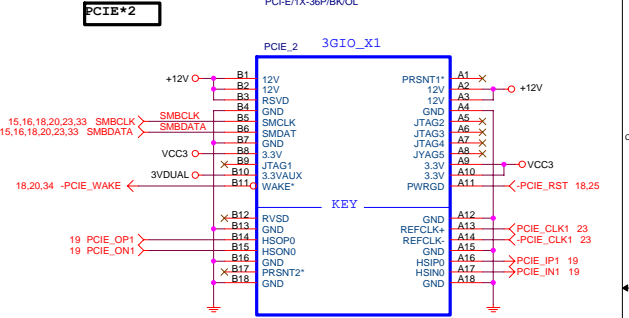
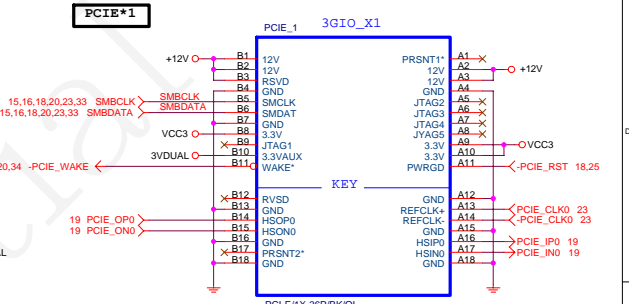
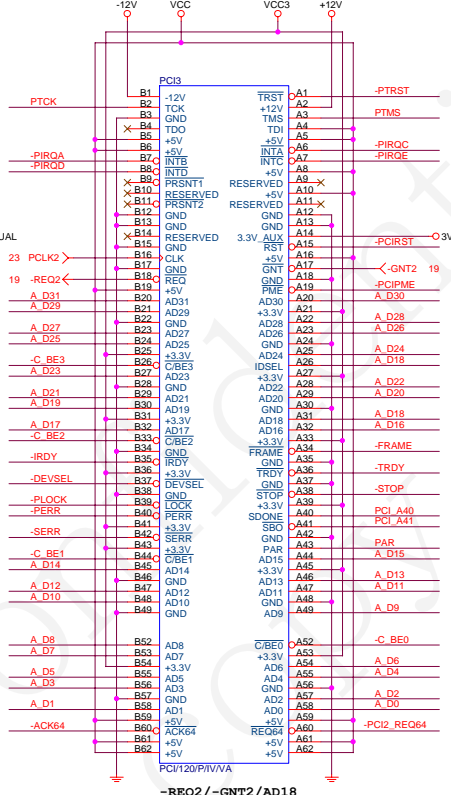
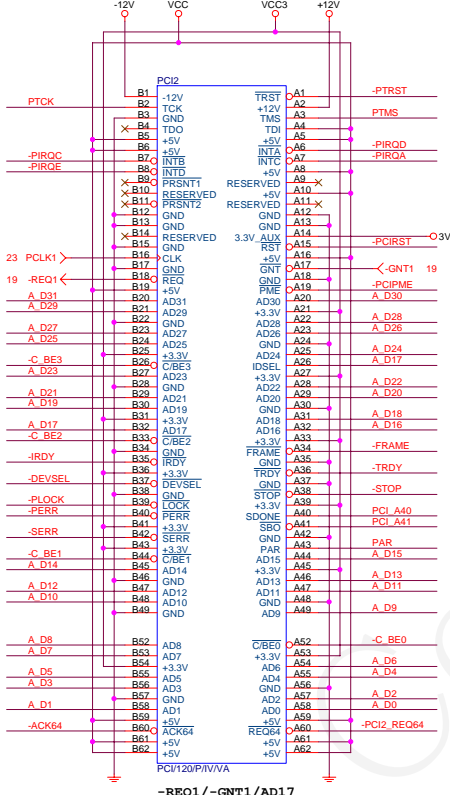
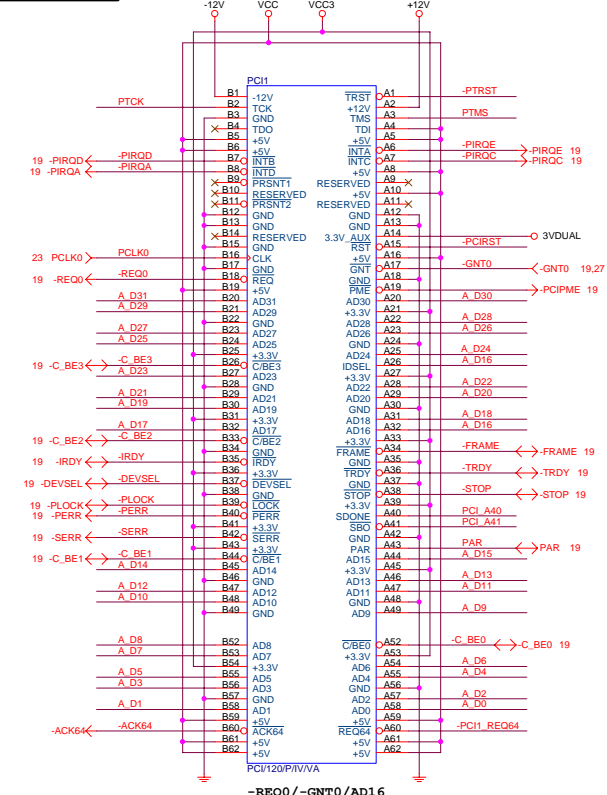
P35-DS3

Title: CK505 CLK GEN

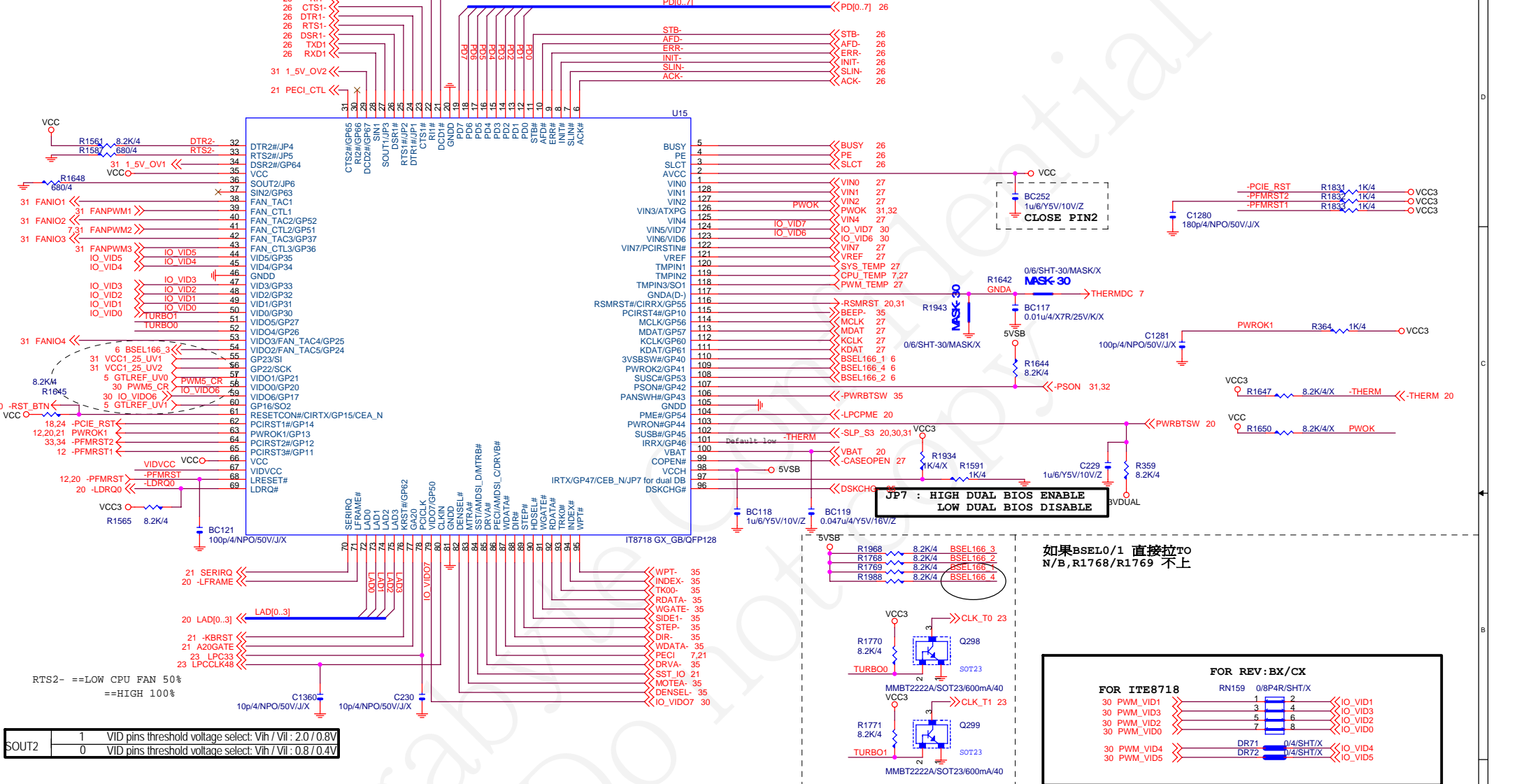
Size: Custom Document Number: P35-DS3 Rev: 2.01

Date: Tuesday, August 14, 2007 Sheet: 23 of 35

PCI1,2 SLOT

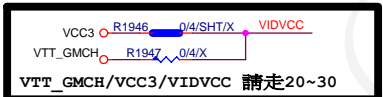


IT8712F LPC I/O



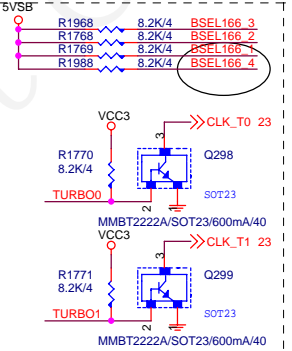
SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V

1.2V or 3.3V tolerance select.
 1.2V OUTPUT 接 VTT_GMCH
 3.3V OUTPUT 接 3.3V
 LPCPD# = VIDVCC



**JP7 : HIGH DUAL BIOS ENABLE
 LOW DUAL BIOS DISABLE**

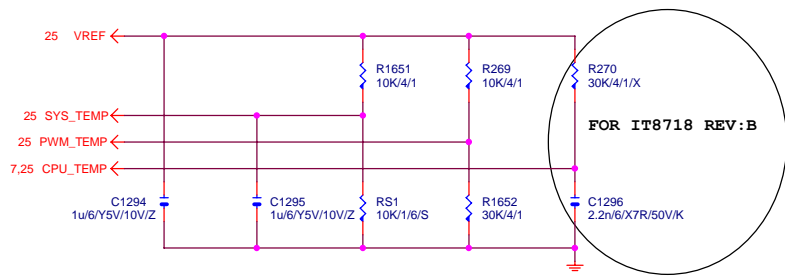
如果BSEL0/1 直接拉到
 N/B, R1768/R1769 不上



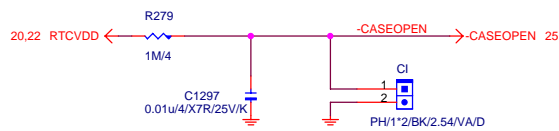
FOR REV: BX/CX

FOR ITE8718	RN159	0/8P4R/SHT/X	1	2	<< IO_VID1
			3	4	<< IO_VID3
			5	6	<< IO_VID2
			7	8	<< IO_VID0
	DR71	0/4/SHT/X			<< IO_VID4
	DR72	0/4/SHT/X			<< IO_VID5

TEMP H/W MONITOR

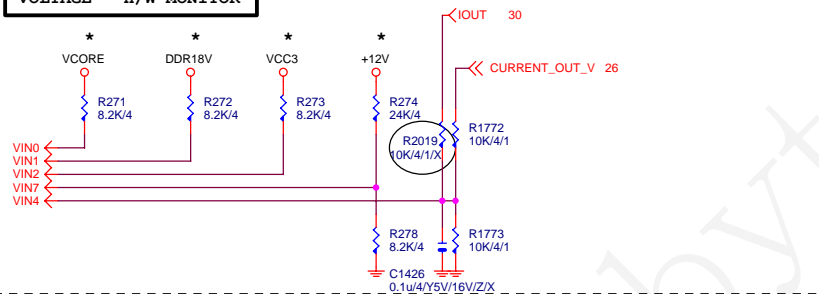


CASE OPEN

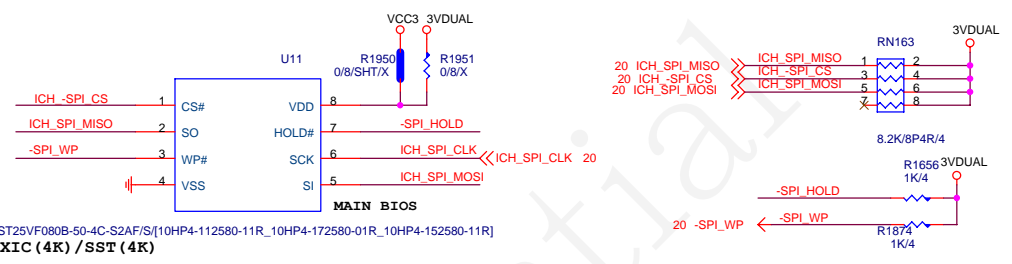
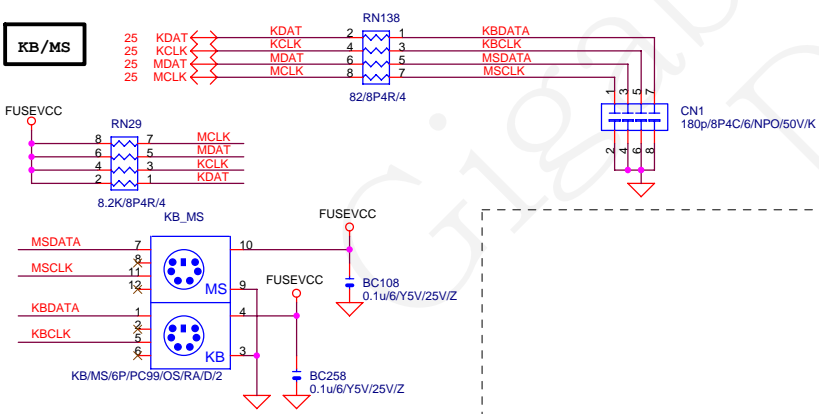


Case Open Circuits

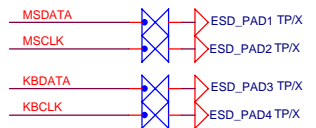
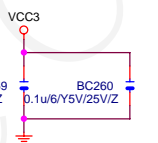
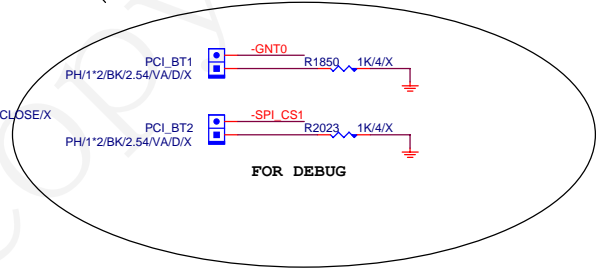
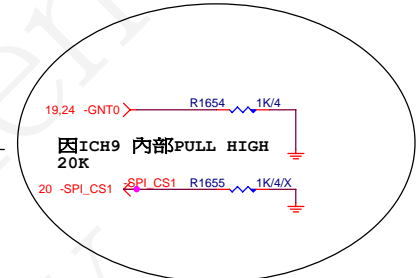
VOLTAGE-- H/W MONITOR



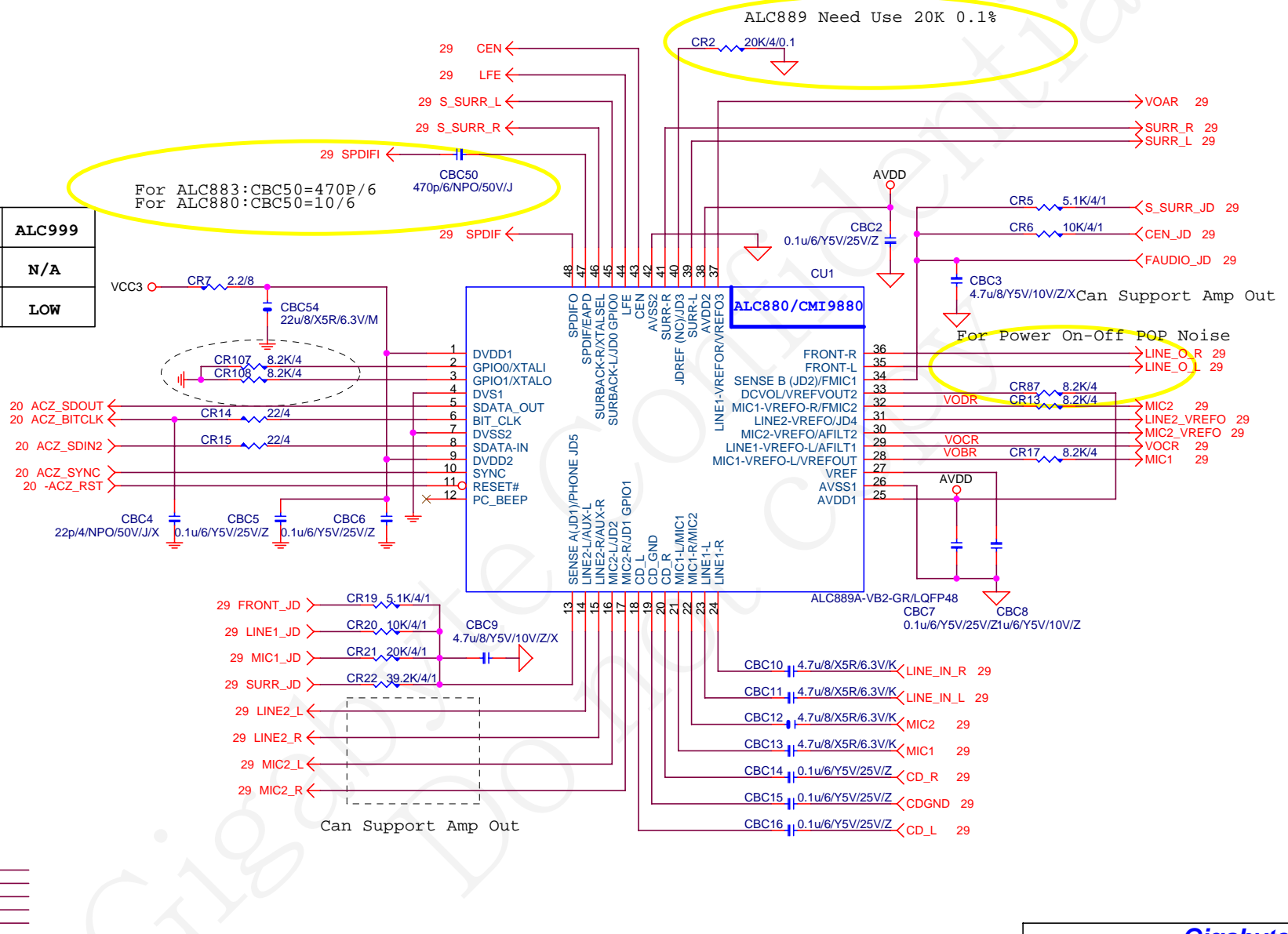
KB/MS



BOOT DEVICE	GNT0	CS1
SPI	0	1
PCI	1	0
FWH	1	1



	ALC889A	ALC999
GPI00	LOW	N/A
GPI01	LOW	LOW



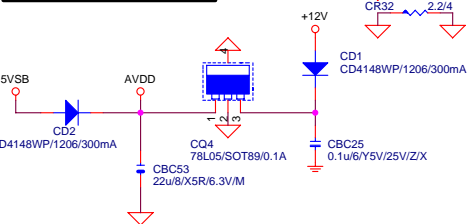
- 20 ACZ_SDOUT <
- 20 ACZ_SYNC <
- 20 -ACZ_RST <
- 20 ACZ_BITCLK <
- 20 ACZ_SDIN2 <

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ALC889A

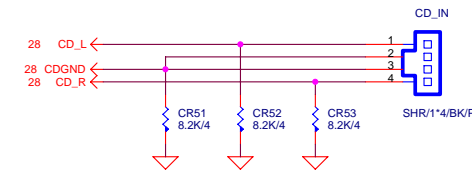
Title		ALC889A	
Size Custom	Document Number	P35-DS3	
		Rev	2.01
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CODEC POWER/EMI PAD



CO-LAYOUT

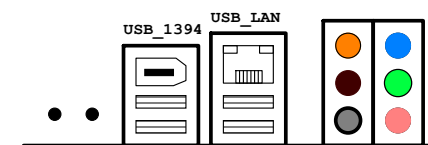
CD IN



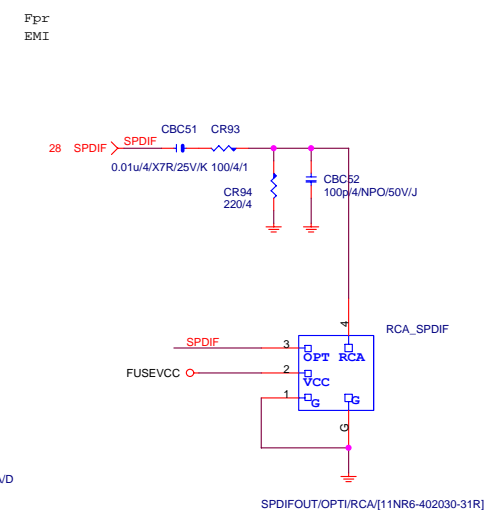
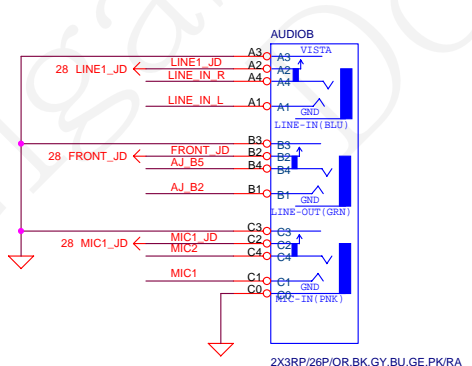
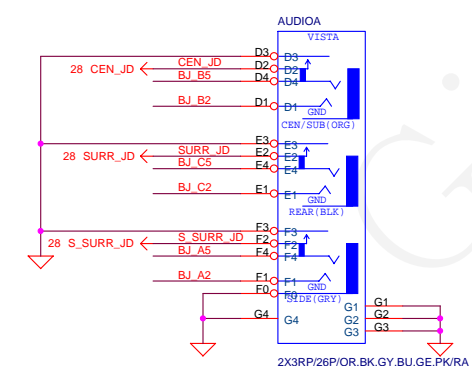
SPDIF



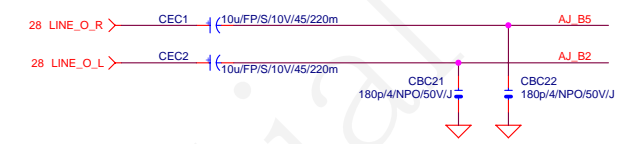
AZALIA JACK



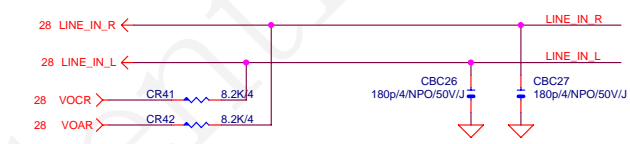
3RP/26P/OR, BK, GY, BU, GE, PK/RA/D/1/B
VISTA 規範: REAR-->BLK, CEN/SUB-->ORG



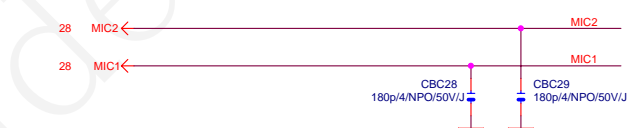
LINE-OUT



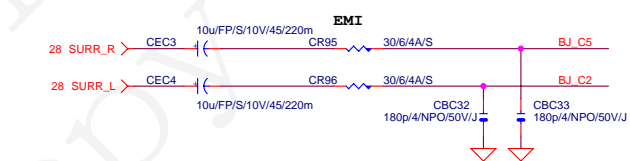
LINE-IN



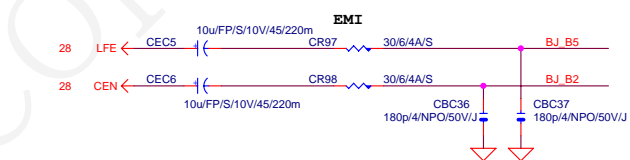
MIC-IN



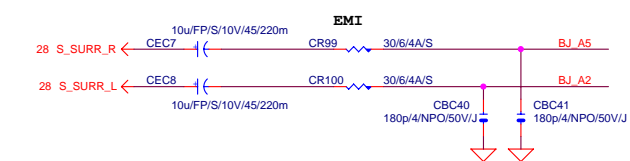
SURROUND



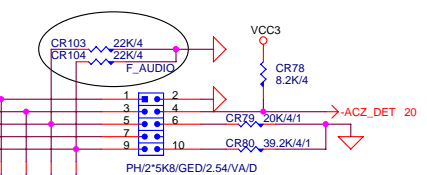
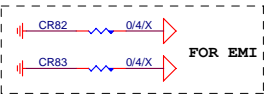
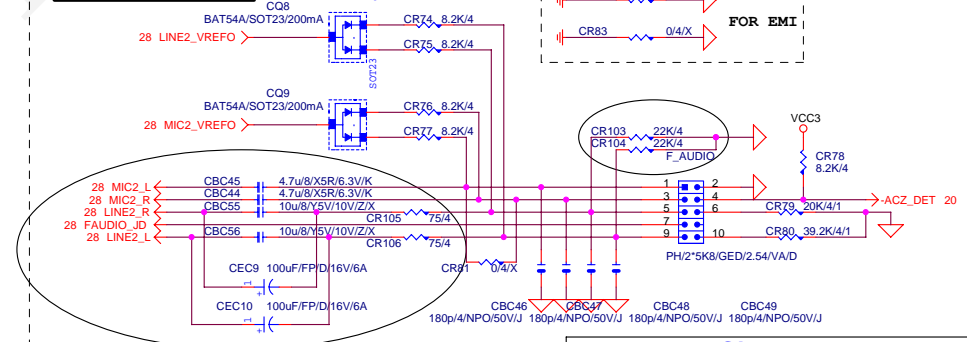
CEN/LFE



SURR BACK

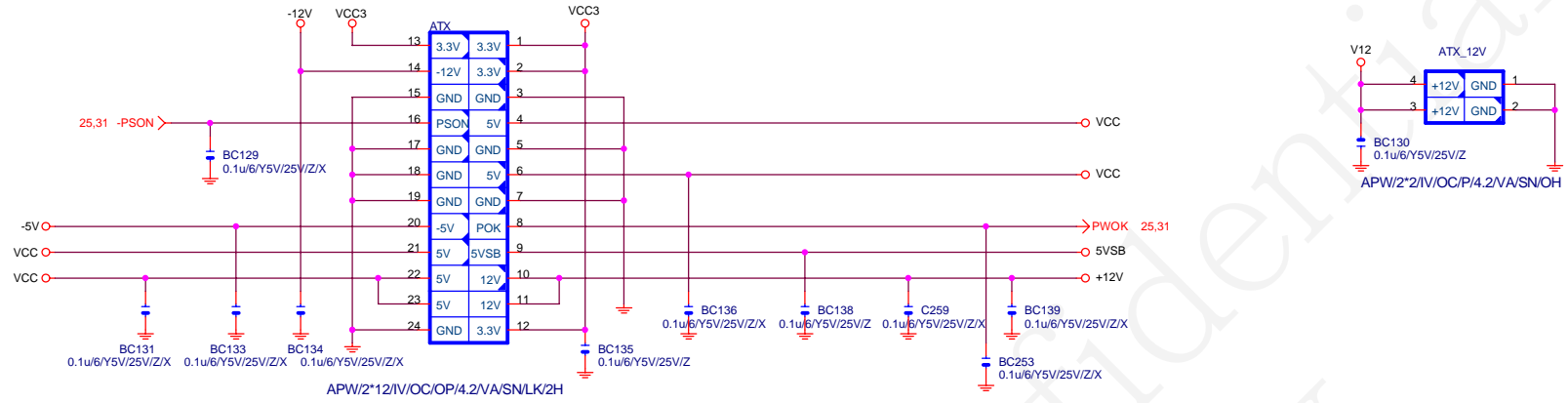


AZALIA FRONT PANEL

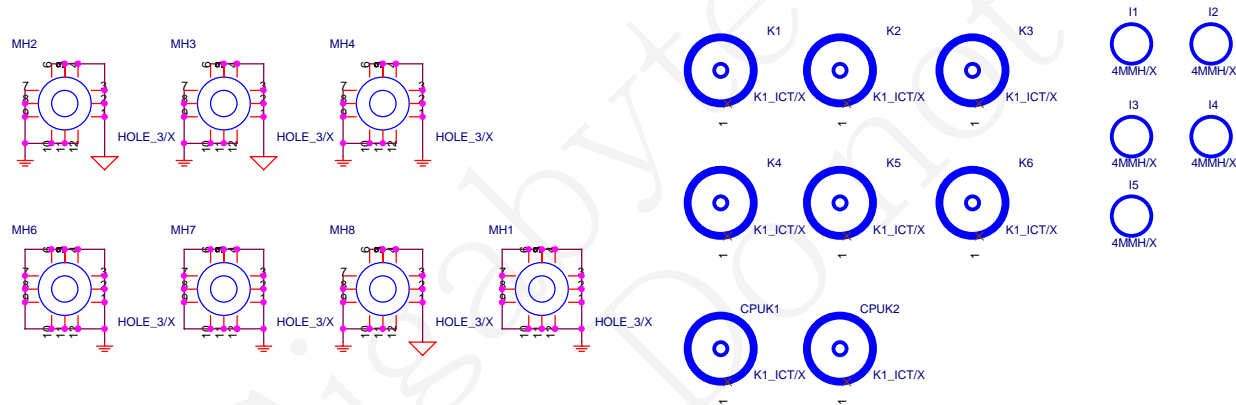


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AUDIO JACK		
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		2.01
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ATX POWER CONNECTOR

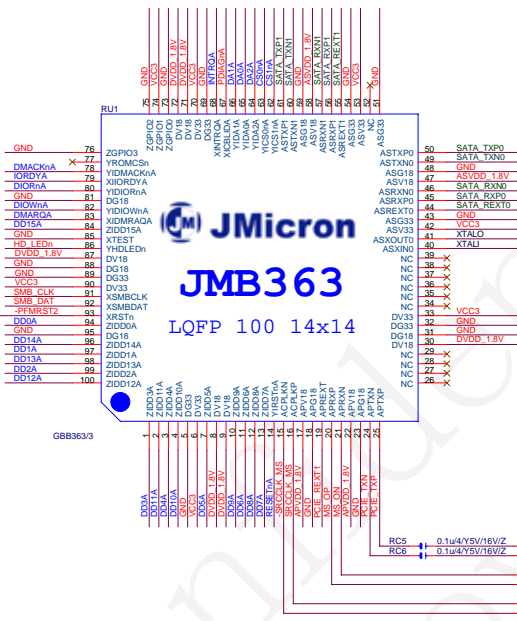
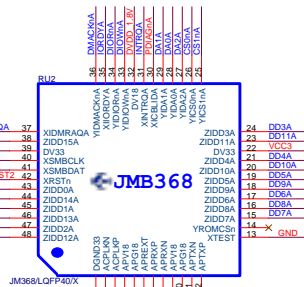
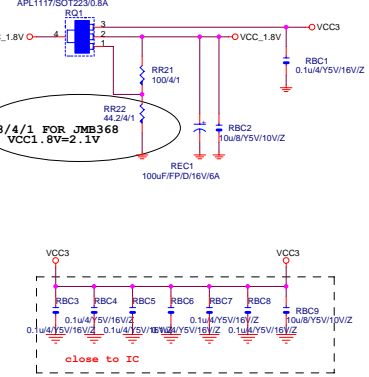


HOLE_3-2--->有鉛



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Title		
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	2	1

3.3V to 1.8V Voltage Regulator



PH_D07	DD7A
PH_D08	DD8A
PH_D09	DD9A

PH_D05	DD5A
PH_D04	DD4A
PH_D010	DD10A
PH_D011	DD11A

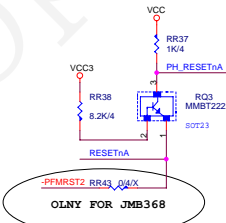
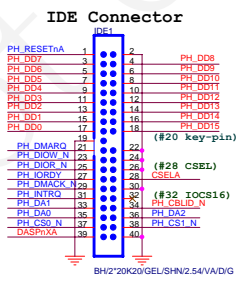
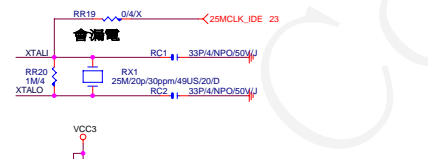
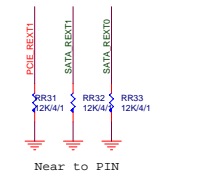
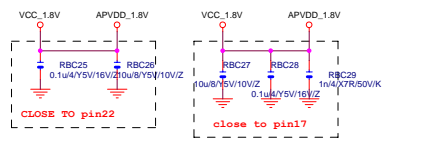
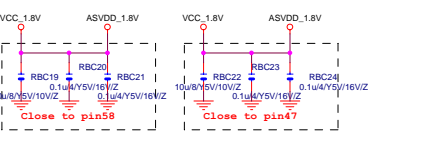
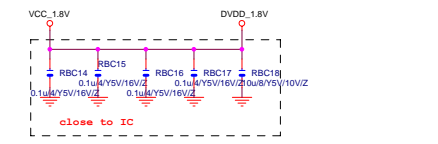
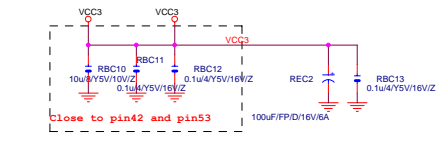
PH_D03	DD3A
PH_DD12	DD12A
PH_DD13	DD13A

PH_DD1	DD1A
PH_DD0	DD0A
PH_DD14	DD14A
PH_DD15	DD15A

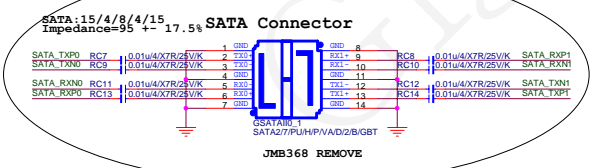
PH_DI0W_N	DI0WnA
PH_DI0R_N	DI0RnA

PH_DMACK_N	DMACKnA
PH_DA1	DA1A
PH_DA0	DA0A
PH_CS0_N	CS0nA
PH_DA2	DA2A
PH_CS1_N	CS1nA

PH_I0RDY	I0RDYA
PH_DMARGO	DMARGO
PH_INTR0	INTR0A
PH_CBLID_N	PDIA0nA



SATA Connector usb:90 规格: [15/4.5/7.5/4.5/15]



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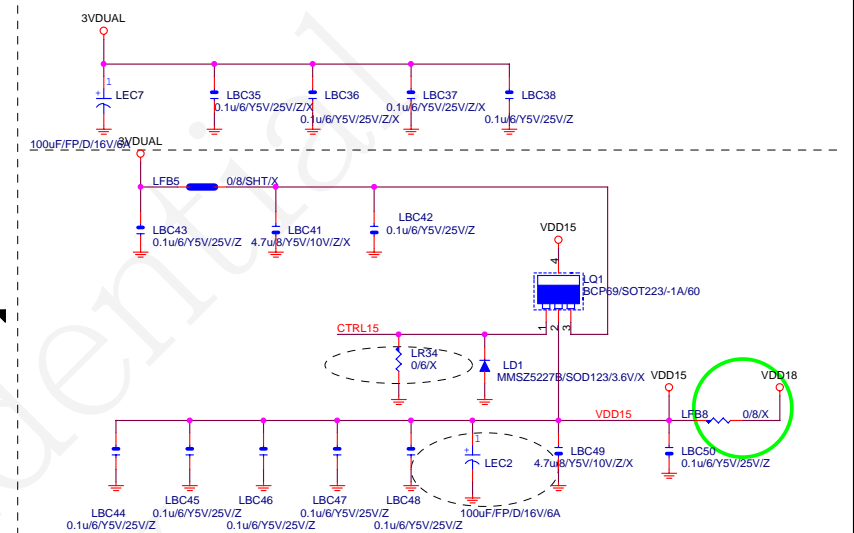
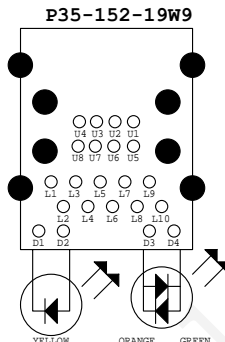
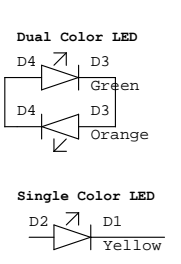
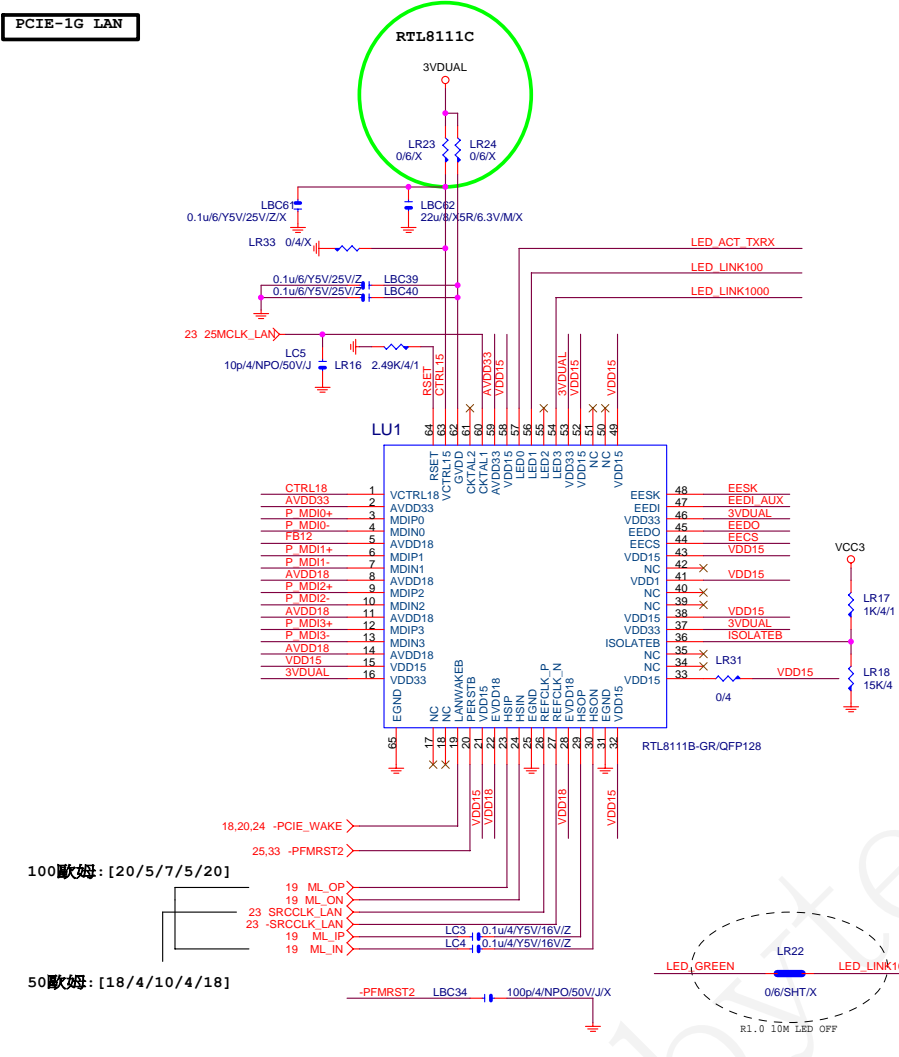
JMR363

Title: _____

Size: _____ Document Number: **P35-DS3** Rev: **2.01**

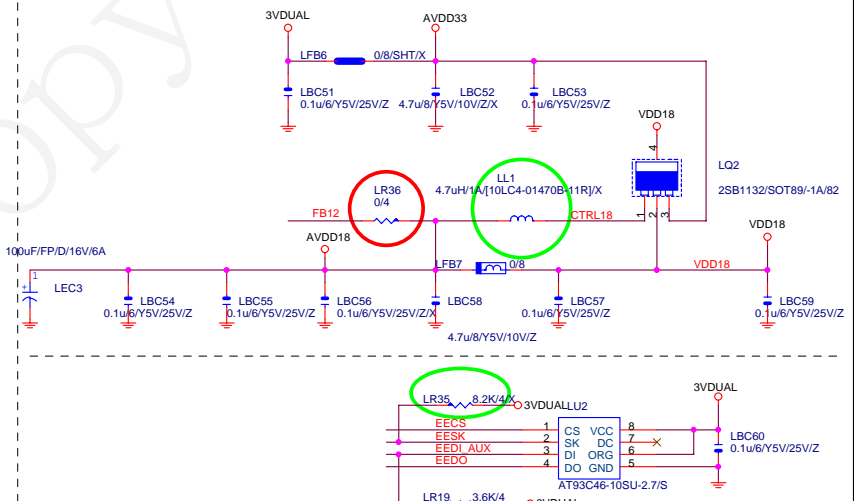
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PCIE-1G LAN

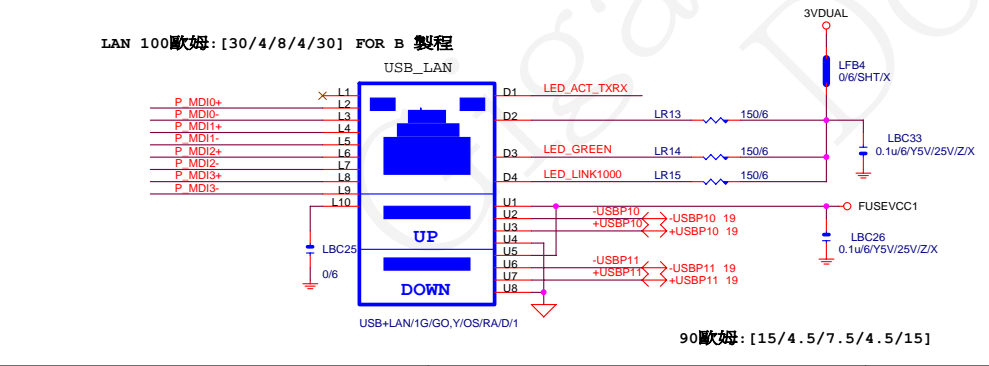


Power domain chart

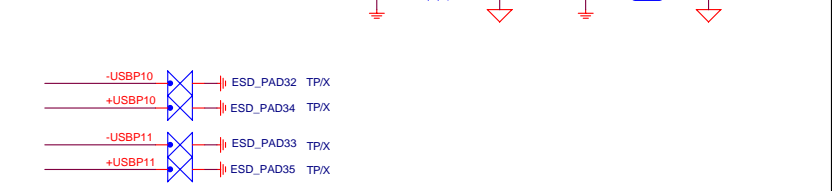
	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V



USB LAN CONNECTOR



USB LAN

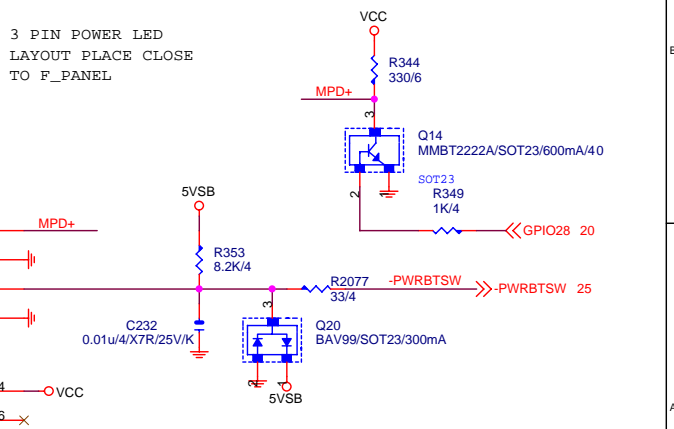
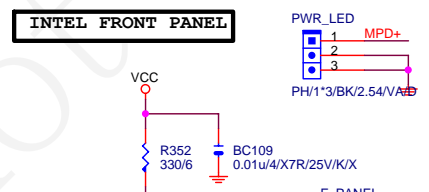
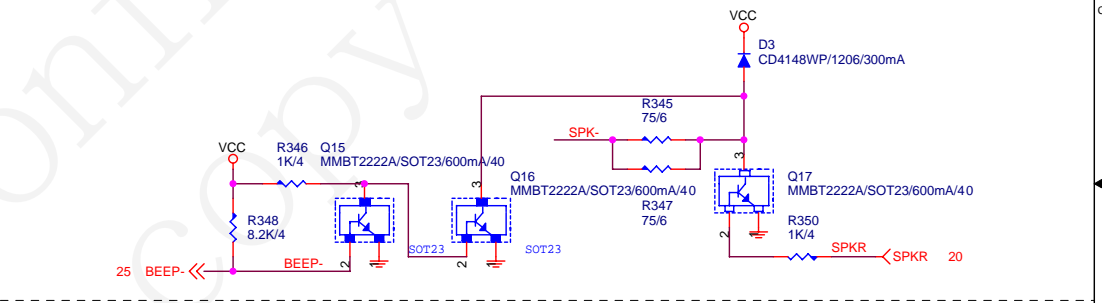
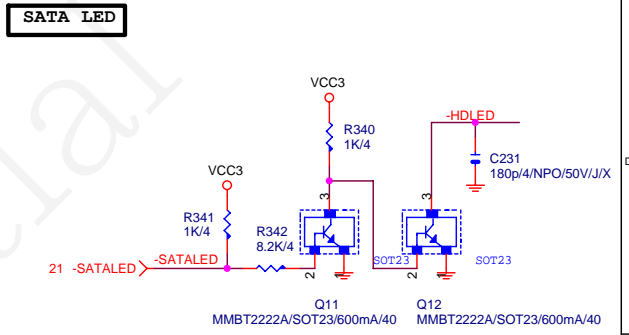
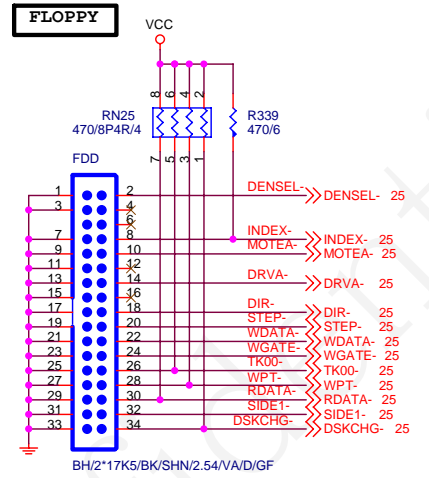
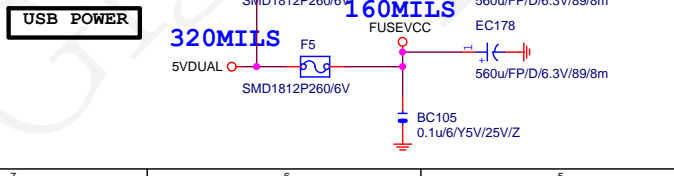
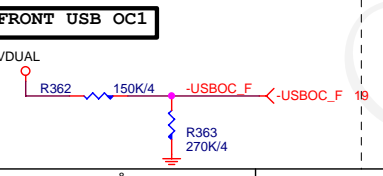
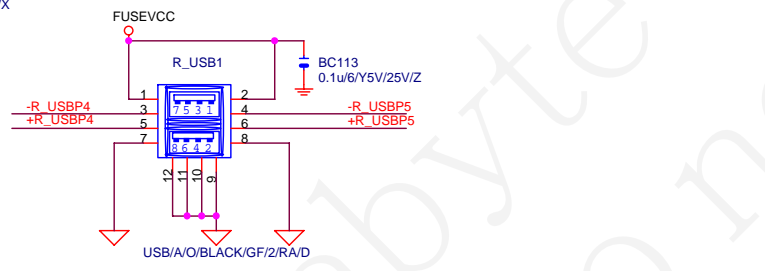
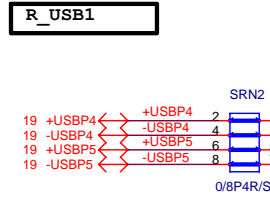
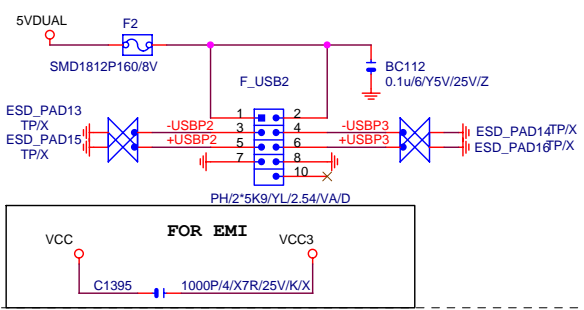
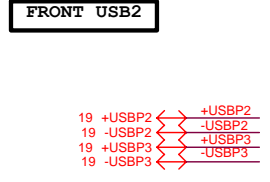
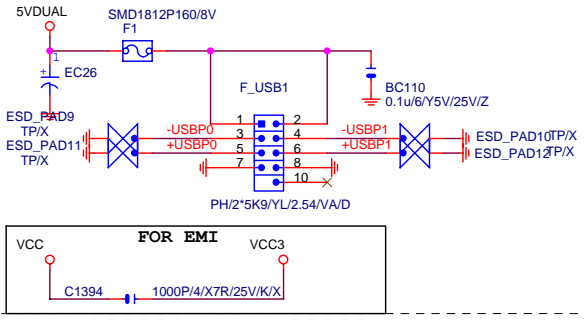
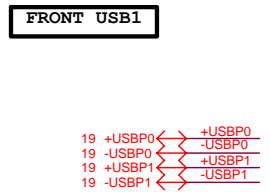


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