First International Computer,Inc

Protable Computer Group HW Department

Board name : Mother Board Schematic

Project : LM7R

Version : 0.1

Initial Date : March 1 , 2005

1. Schematic Page Description :
2. PCI & IRQ & DMA Description :
3. Block Diagram :
4. Nat name Description :
5. Board Stack up Description :
6. Schematic modify Item and History :
7. power on & off & S3 Sequence :
8. Layout Guideline :
9. switch setting

Manager Sign by:

Drawing by : AHARRY_HUANG

Total confirm by: CC_TSAO

LAN Circuit check by:

Audio Circuit check by:

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 1 of 56

1. Schematic Page Description :

LM7 Schematic Ver : 0.1

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI(Wireless LAN)
AD23	CardBus

PCIINT	CHIP
IRQA	MiniPCI/NB
IRQB	MiniPCI/CardBus
IRQC	MiniPCI
IRQD	

BUSMASTER

REQ	CHIP
REQ0 / GNT0	MiniPCI
REQ1 / GNT1	CardBus
REQ2 / GNT2	Mini PCI(Wireless LAN)
REQ3 / GNT3	
REQ4 / GNT4	

IRQ Channel	Desciption	
IRQ0	System timer	
IRQ1	Keyboard	
IRQ2	(Casacde)	
IRQ3	LAN / MODEM	
IRQ4	~~Serial Port~~	
IRQ5	AUDIO / VGA / USB	
IRQ6	~~FLOPPY DISK~~	
IRQ7	~~LPT~~	
IRQ8	RTC	
IRQ9	ACPI	
IRQ10	FIR (Disable by default)	(MODEM/LAN)
IRQ11	Cardbus	
IRQ12	PS/2 mouse	
IRQ13	FPU	
IRQ14	HDD	
IRQ15	CDROM	

DMA Channel	Device	
DMA0	FIR (disable by default)	(MODEM / LAN)
DMA1	~~ECP~~	
DMA2	~~FLOPPY DISK~~	
DMA3	AUDIO	
DMA4	(Cascade)	
DMA5	Unused	
DMA6	Unused	
DMA7	Unused	

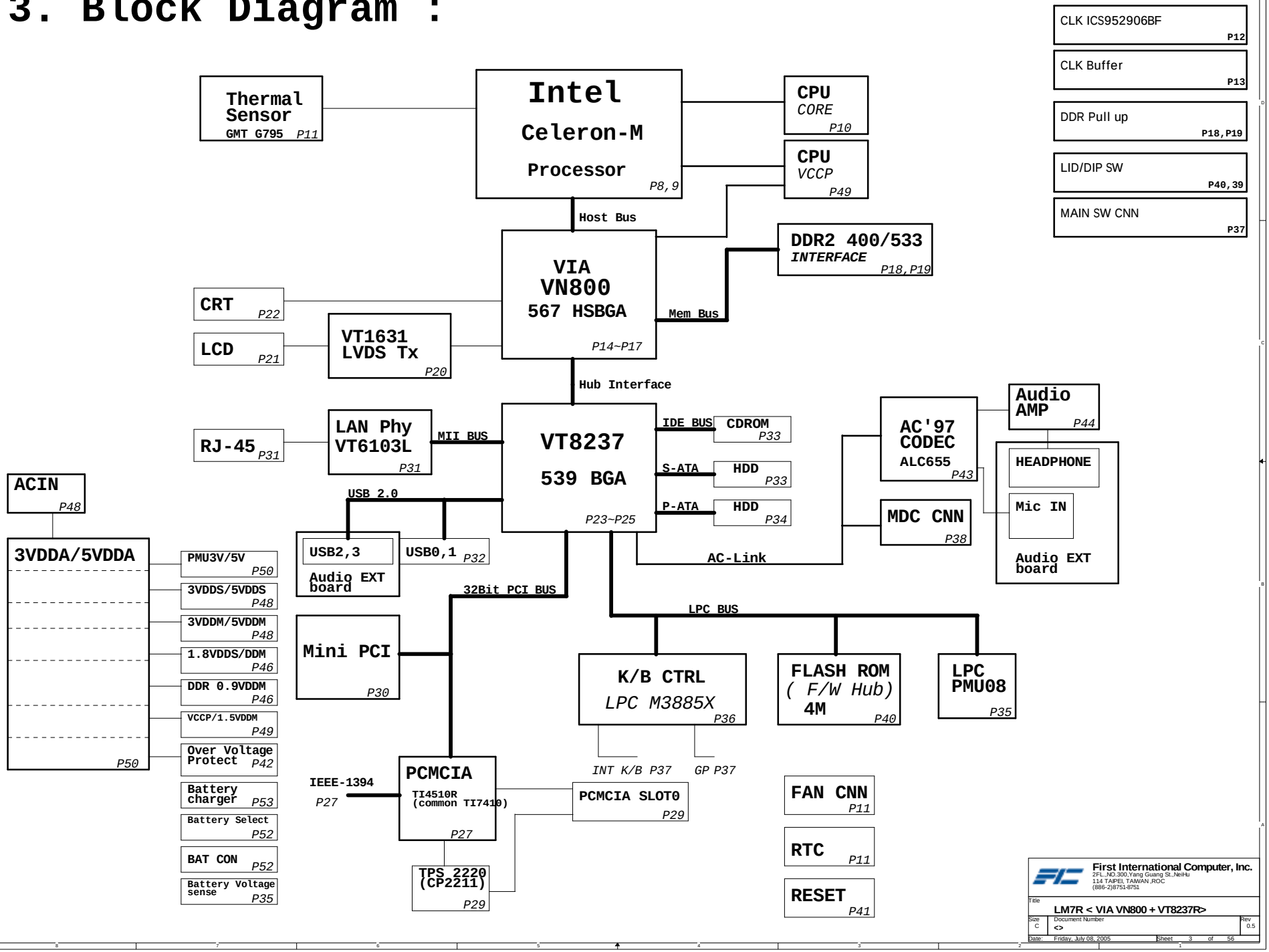
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 2 of 56

3. Block Diagram :



4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
3VDDS	3.3V power rail
5VDDS	5.0V power rail
3VDDM	3.3V switched power rail
5VDDM	5.0V switched power rail
Vcore_CPU	Core Voltage for CPU
VCCP	1.05V for AGTL+ Termination Voltage
1.8VDDM	1.8V for CPU PLL Voltage
DDR_0.9VDDM	0.9V DDR Termination Voltage
1.5VDDM	1.5V switched power rail
1.5VDDS	1.5V power rail
1.5VDDA	1.5V always on power rail
2.5VDDS	2.5V power rail for DDR

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal

Signal Conditioning

_D_	=	Damped (by a resistor)
_Q_	=	Isolated (by a Q-switch)
_L_	=	Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Power Plane
Layer 3		Stripline Layer(AGTL,CLOCK,DDR)
Layer 4		Stripline Layer(Analog,LVDS,other)
Layer 5		Ground Plane
Layer 6		Solder Side,Microstrip signal Layer

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 4 of 56

6.Schematic modify Item and History :

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

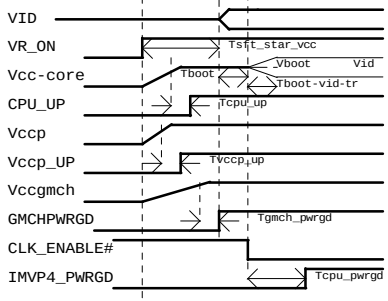
Title
LM7R < VIA VN800 + VT8237R>

Size	Document Number	Rev
C	<>	0.5

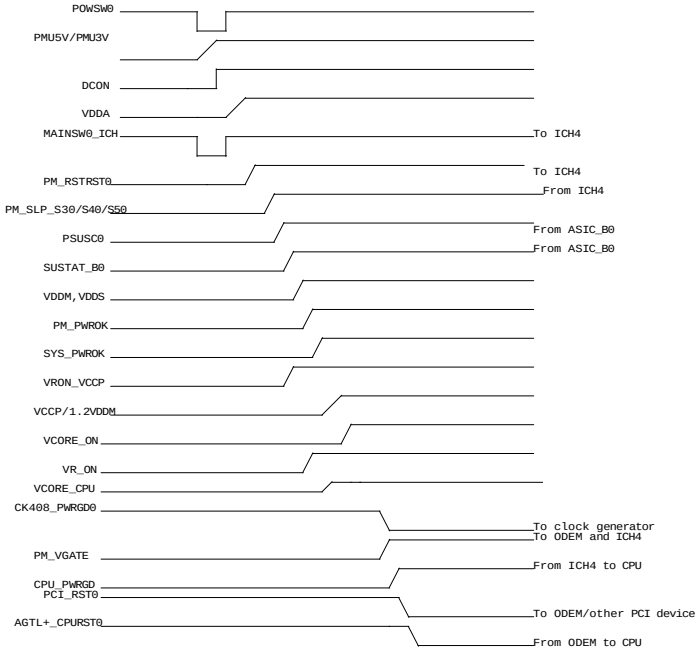
Date: Friday, July 08, 2005 Sheet 5 of 56

7. power on & off & S3 Sequence :

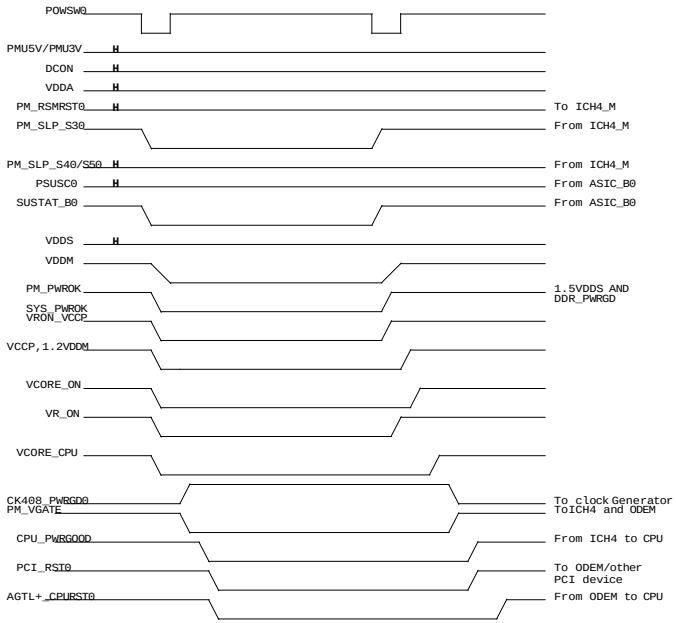
Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



S3 SUSPEND AND RESUME TIMING



First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 6 of 56

8. Layout Guideline :

Montara-GM DDR Layout Guidelines

Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length

DDR Signal Groups

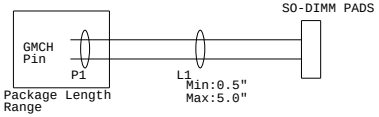
Group	Signal Name
Clocks	SCK[5:0] SCK#[5:0]
Data	SDQ[71:0] SDQS[8:0] SDM[8:0]
Control	SCKE[3:0] SCS#[3:0]
Command	SMA[12,6,3:0] SBA[1:0] SRAS# SCAS# SWE#
CPC	SMA[5,4,2,1] SMAB[5,4,2,1]
Feedback	RCVENOUT# RCVENIN#

Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock - 1.0"	Clock + 0.5"
Command to Clock	Clock - 1.0"	Clock + 2.0"
CPC to Clock	Clock - 1.0"	Clock + 0.5"
Strobe to Clock	Clock - 1.0"	Clock + 0.5"
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

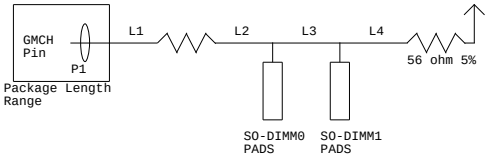
CLOCKS	LENGTH	TRACE / SPACE	NOTES
HCLKCPU[1..0] HCLKNB[1..0] HCLKITP[1..0]	2" ~ 8"	5 / 20 mils (5 mil space between + & -)	1.Differentials pairs with the same length (within 10 mil) 2.CPU & NB trace mismatch within 450 mil
66MCLK_ICH 66MCLK_GMCH AGPCLK_ATI	4.5" ~ 9.0 " MAX : 8.5"	5 / 20 mils	* 66MCLK_ICH & AGPCLK_GMCH AGPCLK_ATI Length mismatch within 100 mils
PCLKICH PCLKCB PCLK1394 PCLKUSB20 PCLKOP PCLKFWH PCLKSIO PCLKLAN	4.5"~9.0"	5 / 20 mils	1.Making PCI length with minimum various 2.Max skew = 1ns
14MCLK_SIO 14MCLK_ICH 14MCLK_AC97	4.5"~9.0"	5 / 10 mils	
48MCLK_ICH 48MCLK_CB	3.5" ~ 12.5"	5 / 20 mils	

Clock Signals Topologies and Routing Guidelines



7 mil trace, 4 mil pair space
Clock length tolerenve within the pair : +/- 10 mil
Clock to Clock Length Matching : +/- 25 mils
Minimum Pair to Pair Spacing : 20 mils
Minimum Spacing to other Signals : 20 mils

Data Signals Topologies and Routing Guidelines

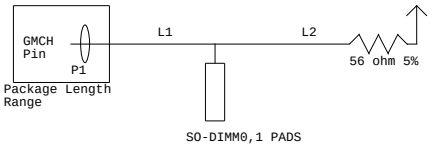


Minimun Spacing to Trace Width Ratio, SDQ/SDM : 2 to 1
SDQS : 3 to1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 3.75"
L2 : Max 0.75"
L3 : Min 0.25" , Max 1.0"
L4 : Max 1.0 "
Length Matching : SDQS to SCK/SCK#
SDQS , SODIMM0 P1+L1+L2
SDQS , SODIMM1 P1+L1+L2+L3
Min : Clock - 1.0" , Max : Clock + 0.5"
SDQ/SDM to SDQS : +/- 25 mils

SDQ/SDM to SDQS Mapping

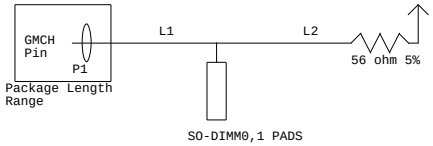
Signal	Mask	Relative To	Mismatching
SDQ[7..0]	SDM[0]	SDQS[0]	+/- 25 mil
SDQ[15..8]	SDM[1]	SDQS[1]	+/- 25 mil
SDQ[23..16]	SDM[2]	SDQS[2]	+/- 25 mil
SDQ[31..24]	SDM[3]	SDQS[3]	+/- 25 mil
SDQ[39..32]	SDM[4]	SDQS[4]	+/- 25 mil
SDQ[56..40]	SDM[5]	SDQS[5]	+/- 25 mil
SDQ[55..48]	SDM[6]	SDQS[6]	+/- 25 mil
SDQ[63..56]	SDM[7]	SDQS[7]	+/- 25 mil
SDQ[71..64]	SDM[8]	SDQS[8]	+/- 25 mil

Control Signals Topologies and Routing Guidelines



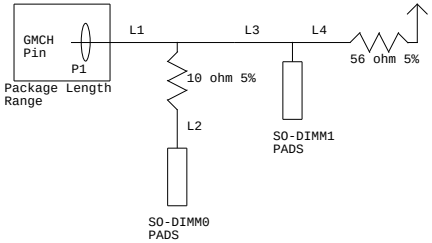
Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CTRL(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

CPC Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CPC(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

Command Signals Topologies and Routing Guidelines



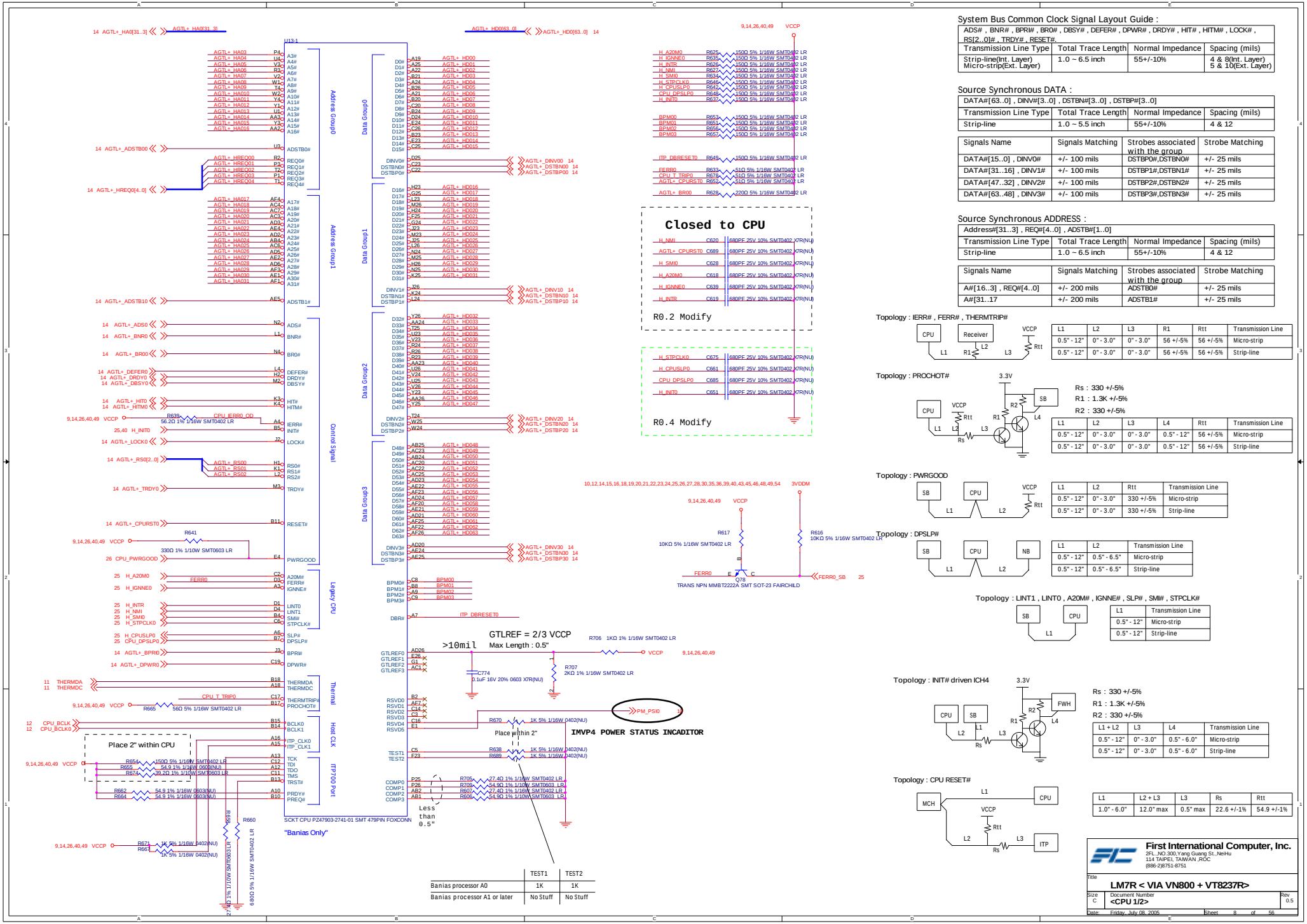
Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 4.0"
L2 : Max 1.0"
L3 : Max 2.0"
L2+L3 : Max 3.0"
L4 : Max 1.0"
Length Matching : CMD to SCK/SCK#
CMD , SODIMM0 P1+L1+L2
CMD , SODIMM1 P1+L1+L3
Min : Clock - 1.0" , Max : Clock + 2.0"

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: **LM7R < VIA VN800 + VT8237R>**

Size: C | Document Number: <> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 7 of 56



System Bus Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer) Micro-strip(Ext. Layer)	1.0 ~ 6.5 inch	55+/-10%	4 & 8(Int. Layer) 5 & 10(Ext. Layer)

Source Synchronous DATA :

DATA#[63..0] , DINV#[3..0] , DSTBN#[3..0] , DSTBP#[3..0]

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line	1.0 ~ 5.5 inch	55+/-10%	4 & 12

Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

Source Synchronous ADDRESS :

Address#[31..3] , REQ#[4..0] , ADSTB#[1..0]

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line	1.0 ~ 6.5 inch	55+/-10%	4 & 12

Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 25 mils
A#[31..17	+/- 200 mils	ADSTB1#	+/- 25 mils

Topology : IERR# , FERR# , THERMTRIP#

L1	L2	L3	R1	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	0" - 3.0"	56 +/-5%	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	0" - 3.0"	56 +/-5%	56 +/-5%	Strip-line

Topology : PROCHOT#

Rs : 330 +/-5%
R1 : 1.3K +/-5%
R2 : 330 +/-5%

L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	0" - 3.0"	0.5" - 12"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	0" - 3.0"	0.5" - 12"	56 +/-5%	Strip-line

Topology : PWRGOOD

L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	330 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	330 +/-5%	Strip-line

Topology : DPSL#

L1	L2	Transmission Line
0.5" - 12"	0.5" - 6.5"	Micro-strip
0.5" - 12"	0.5" - 6.5"	Strip-line

Topology : LINT1 , LINT0 , A20M# , IGNNE# , SLP# , SMI# , STPCLK#

L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : INIT# driven ICH4

Rs : 330 +/-5%
R1 : 1.3K +/-5%
R2 : 330 +/-5%

L1 + L2	L3	L4	Transmission Line
0.5" - 12"	0" - 3.0"	0.5" - 6.0"	Micro-strip
0.5" - 12"	0" - 3.0"	0.5" - 6.0"	Strip-line

Topology : CPU RESET#

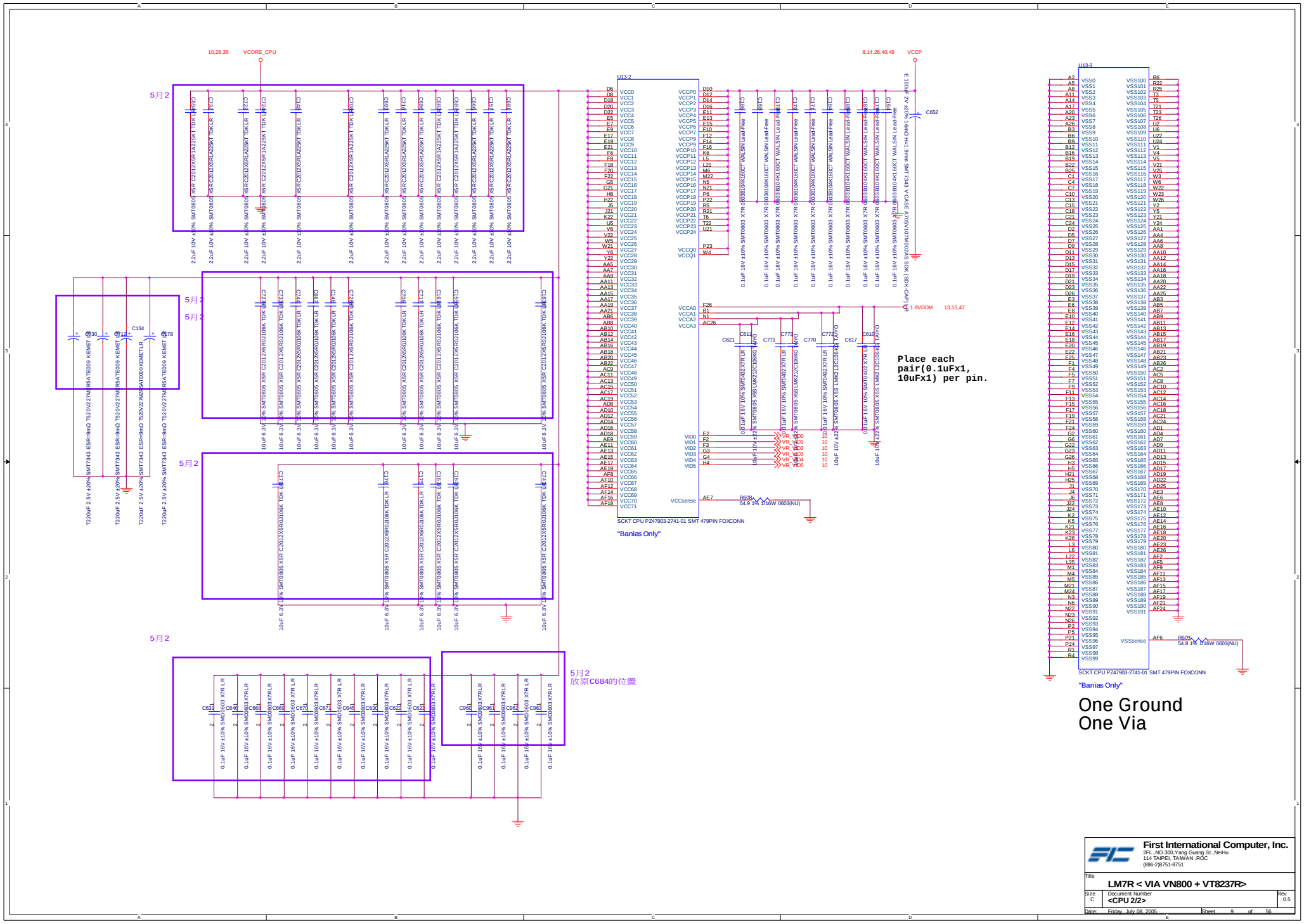
L1	L2 + L3	L3	Rs	Rtt
1.0" - 6.0"	12.0" max	0.5" max	22.6 +/-1%	54.9 +/-1%

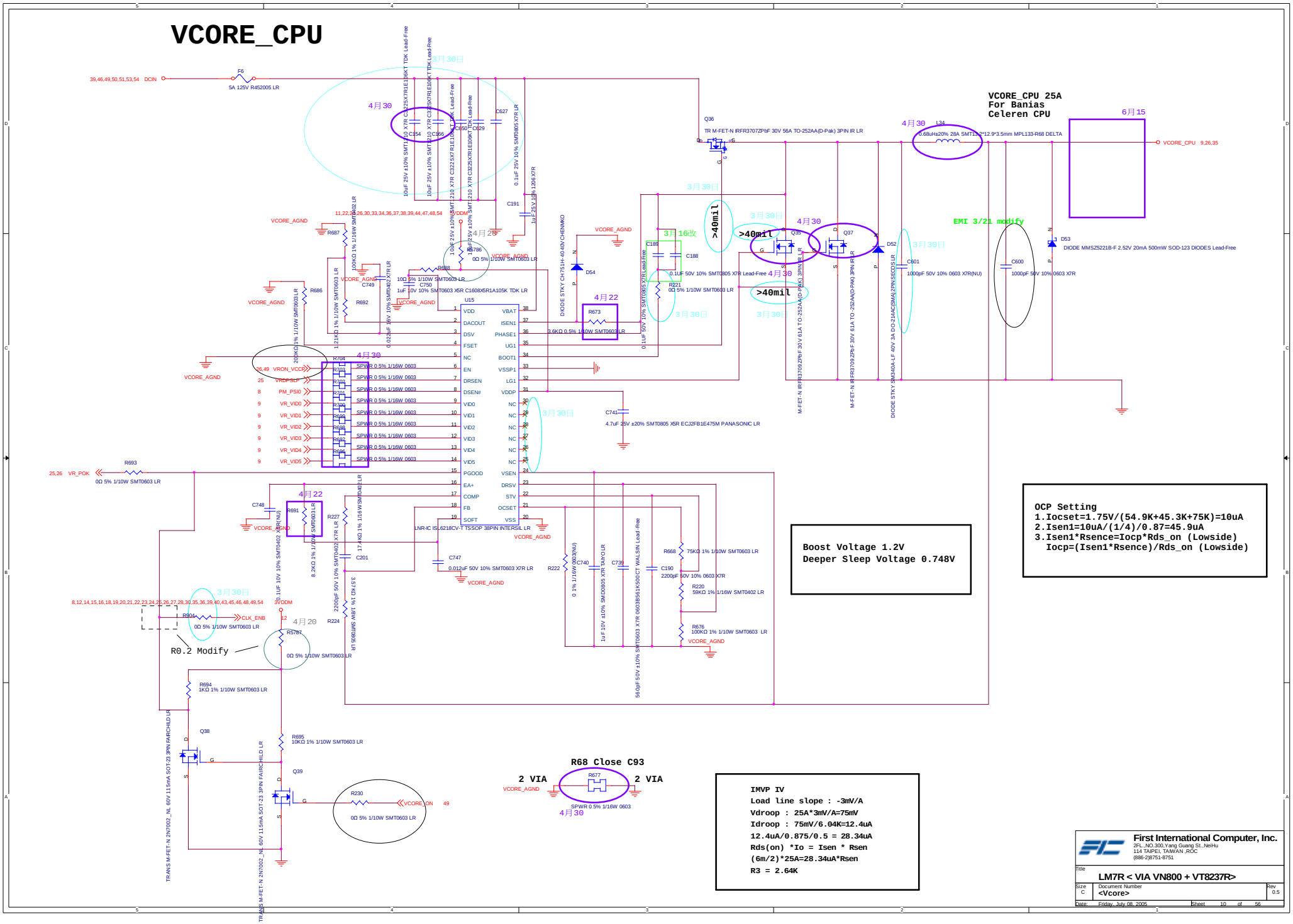
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

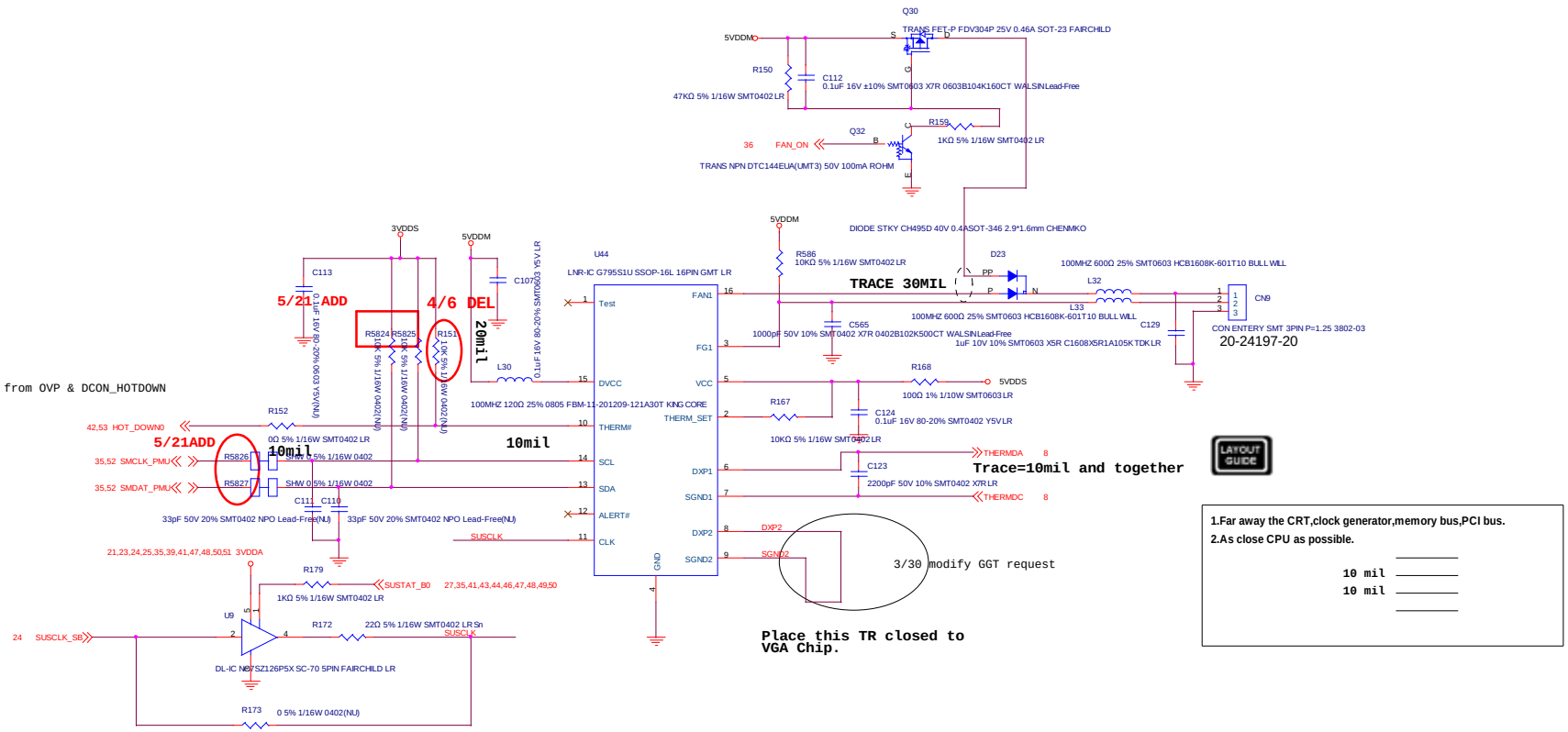
Size: C | Document Number: <CPU 1/2> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 8 of 56

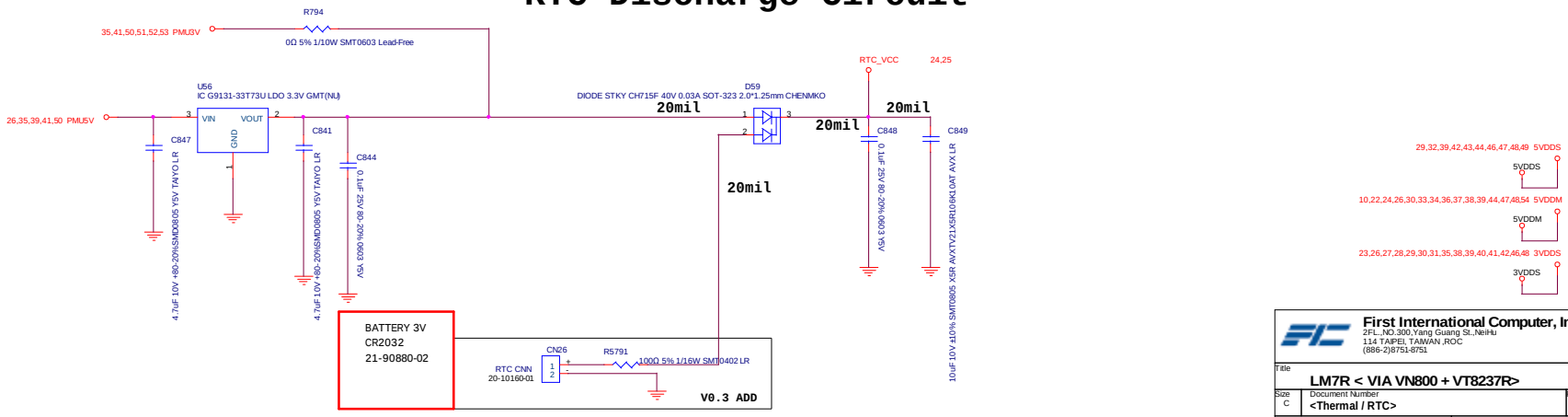




THERMAL SENSOR

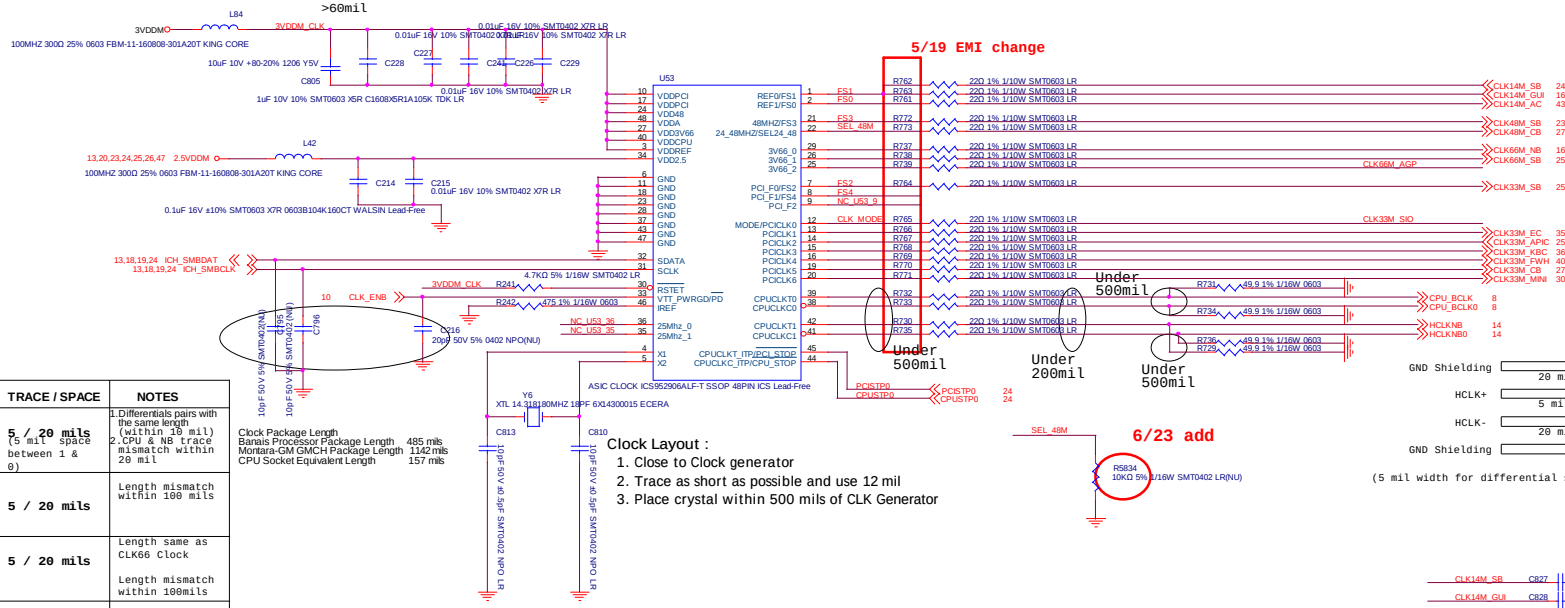


RTC Discharge Circuit



Title	LM7R < VIA VN800 + VT8237R>
Size	C
Document Number	<Thermal / RTC>
Rev	0.5
Date:	Friday, July 08, 2005
Sheet	11 of 56

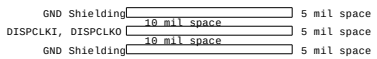
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

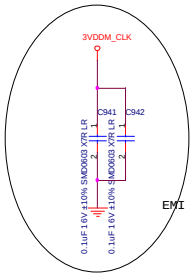


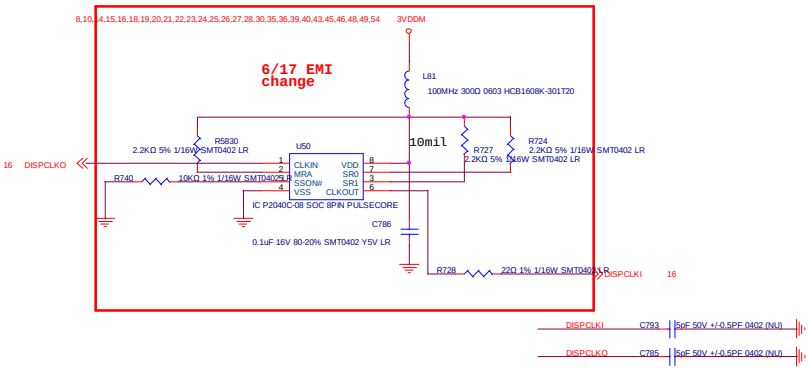
Clock Latout Guideline

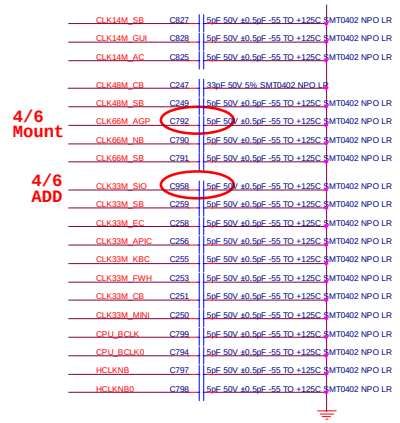
	CLOCKS	LENGTH	TRACE / SPACE	NOTES
HOST Clock	CPU_BCLK[1..0] MCH_BCLK[1..0] ITP_BCLK[1..0]	2" ~ 8 "	5 / 20 mils (5 mil space between 1 & 0)	1.Differentials pairs with the same length (within 10 mil) 2.CPU & NB trace mismatch within 20 mil
CLK66 Clock	CLK_ICH66 CLK_MCH66 CLK_AGP	4.5" ~ 9.0 " MAX : 8.5"	5 / 20 mils	Length mismatch within 100 mils
CLK33 Clock	CLK_ICHPCI CLK_SIOPCI CLK_FWHPCI	4.5" ~ 9.0 "	5 / 20 mils	Length same as CLK66 Clock Length mismatch within 100mils
PCI Clock	CLK_MINIPCI CLK_1394PCI CLK_PMU08PCI CLK_CBPCI	4.5"~9.0"	5 / 20 mils	1.Making PCI length with minimum various 2. Length Require CLK33-2.5" 3. Length mismatch +/- 2.0"
CLK14 Clock	CLK_SIO14 CLK_ICH14 CLK_TV14	2.0"~9.0"	5 / 20 mils	1. Length mismatch +/- 500 mils
	CLK_ICH48 CLK_MCH48	3.5" ~ 12.5"	5 / 20 mils	

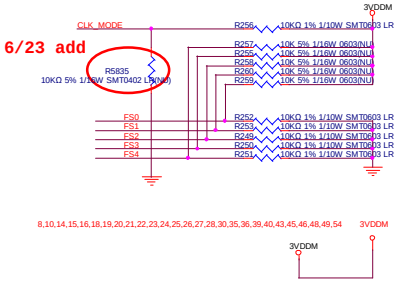
FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI	REF
0	0	0	0	0	100.00M	66.67M	33.33M	14.318M
0	0	0	0	1	200.00M	66.67M	33.33M	14.318M
0	0	0	1	0	133.33M	66.67M	33.33M	14.318M
0	0	0	1	1	166.67M	66.67M	33.33M	14.318M
0	0	1	0	1	400.00M	66.67M	33.33M	14.318M







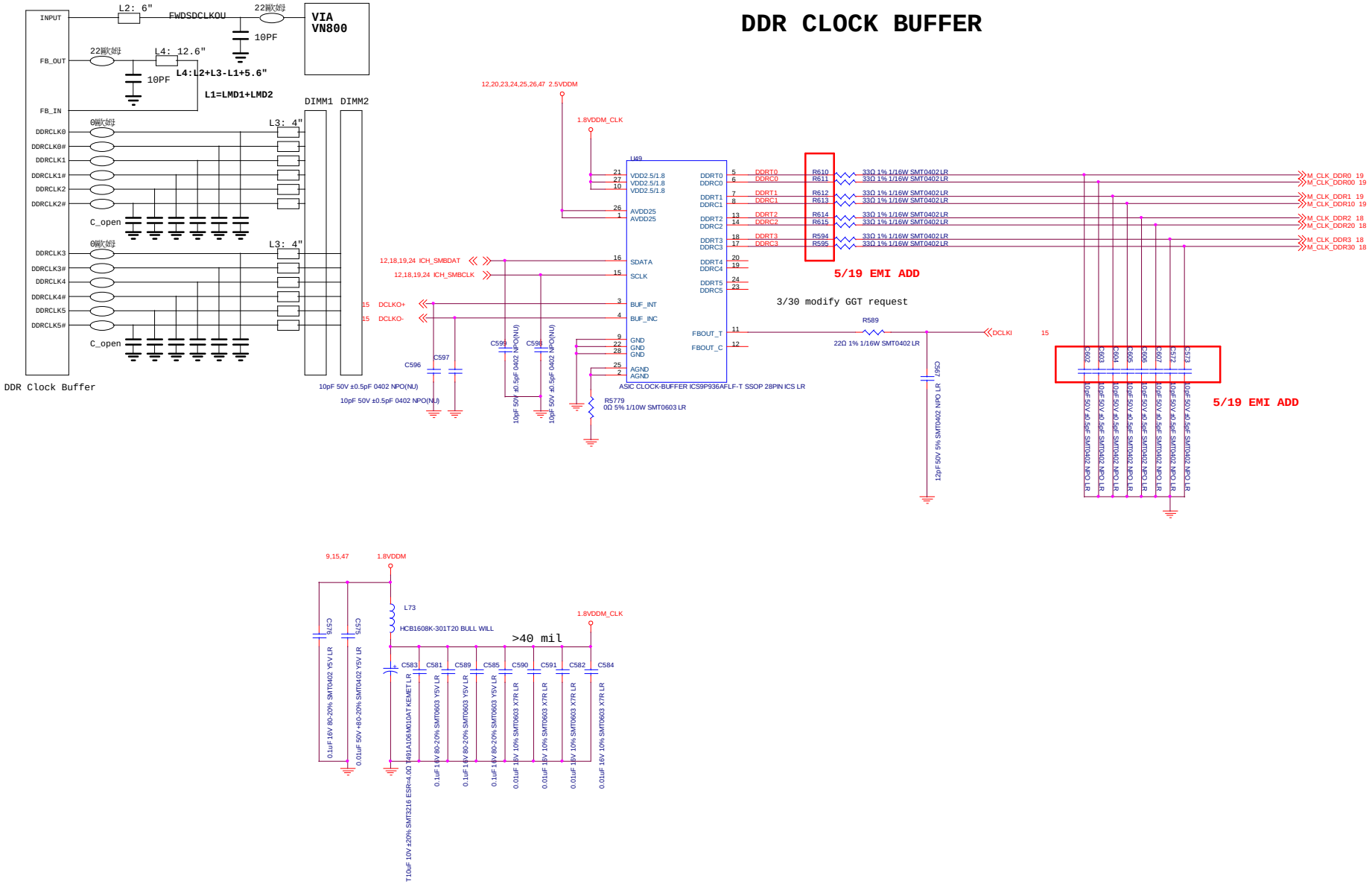




Title	LM7R < VIA VN800 + VT8237R>
Size	C
Document Number	<Clock-Gen>
Rev	0.5
Date:	Friday, July 08, 2005
Sheet	12 of 56

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

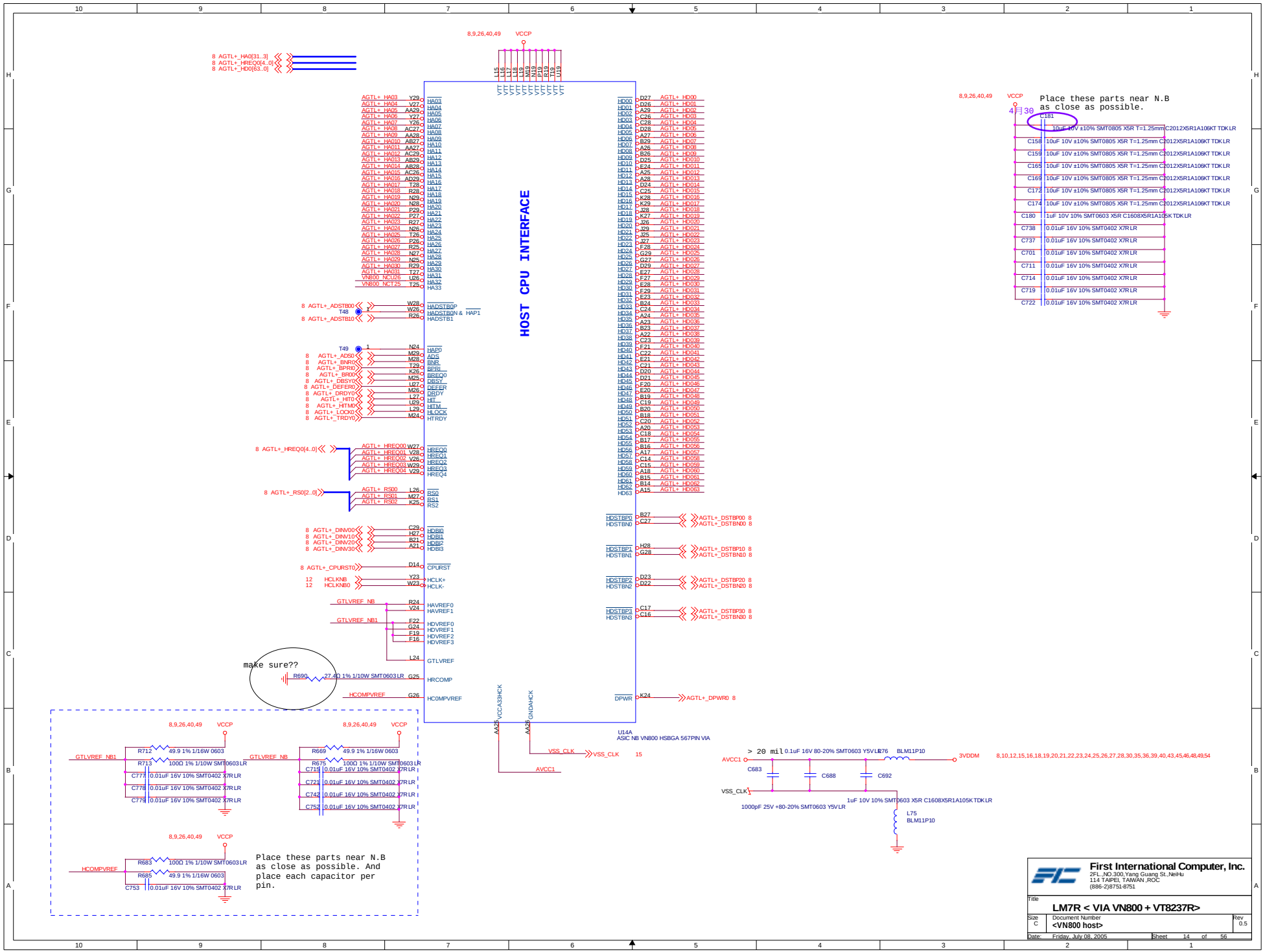
DDR CLOCK BUFFER

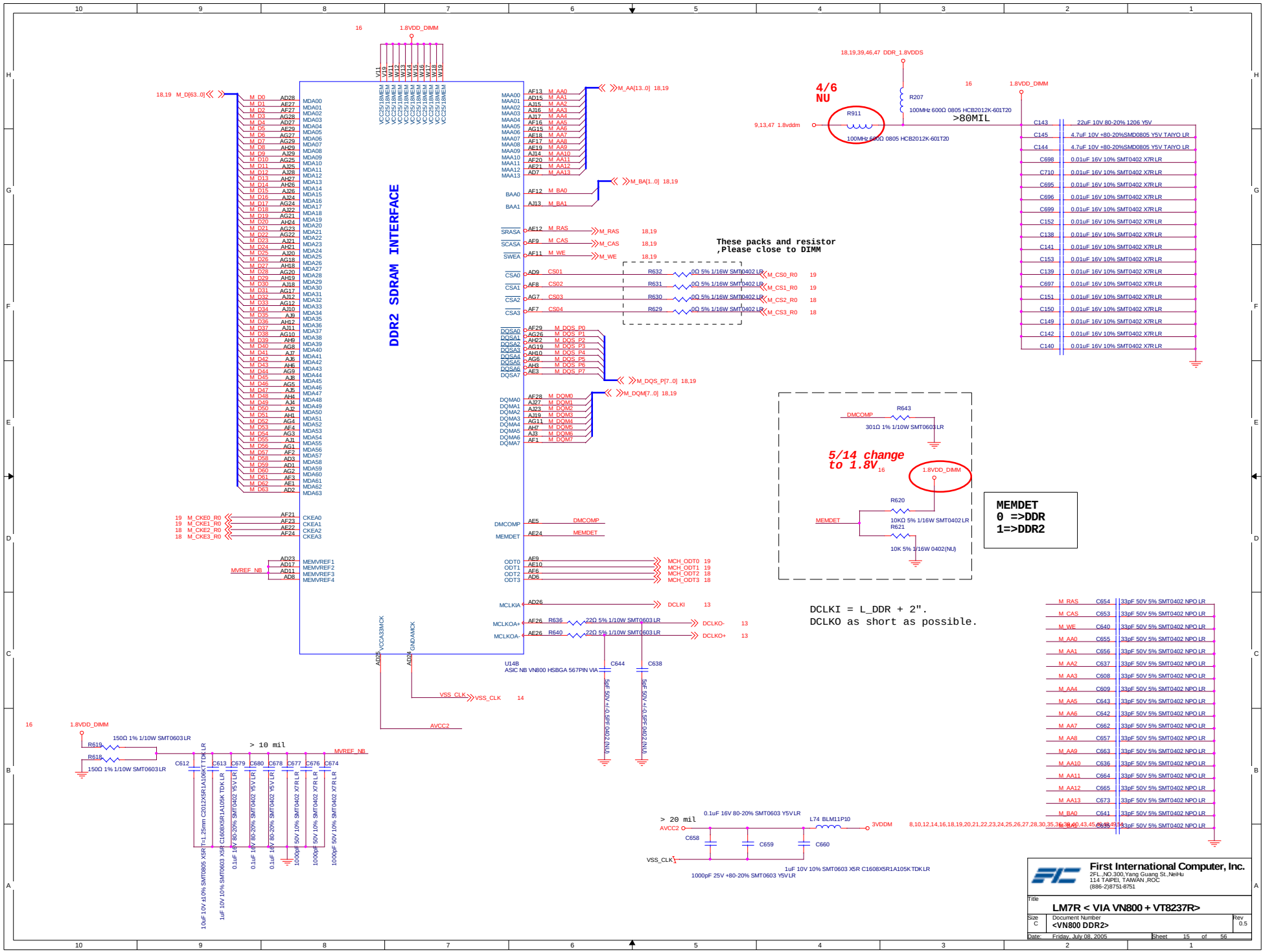


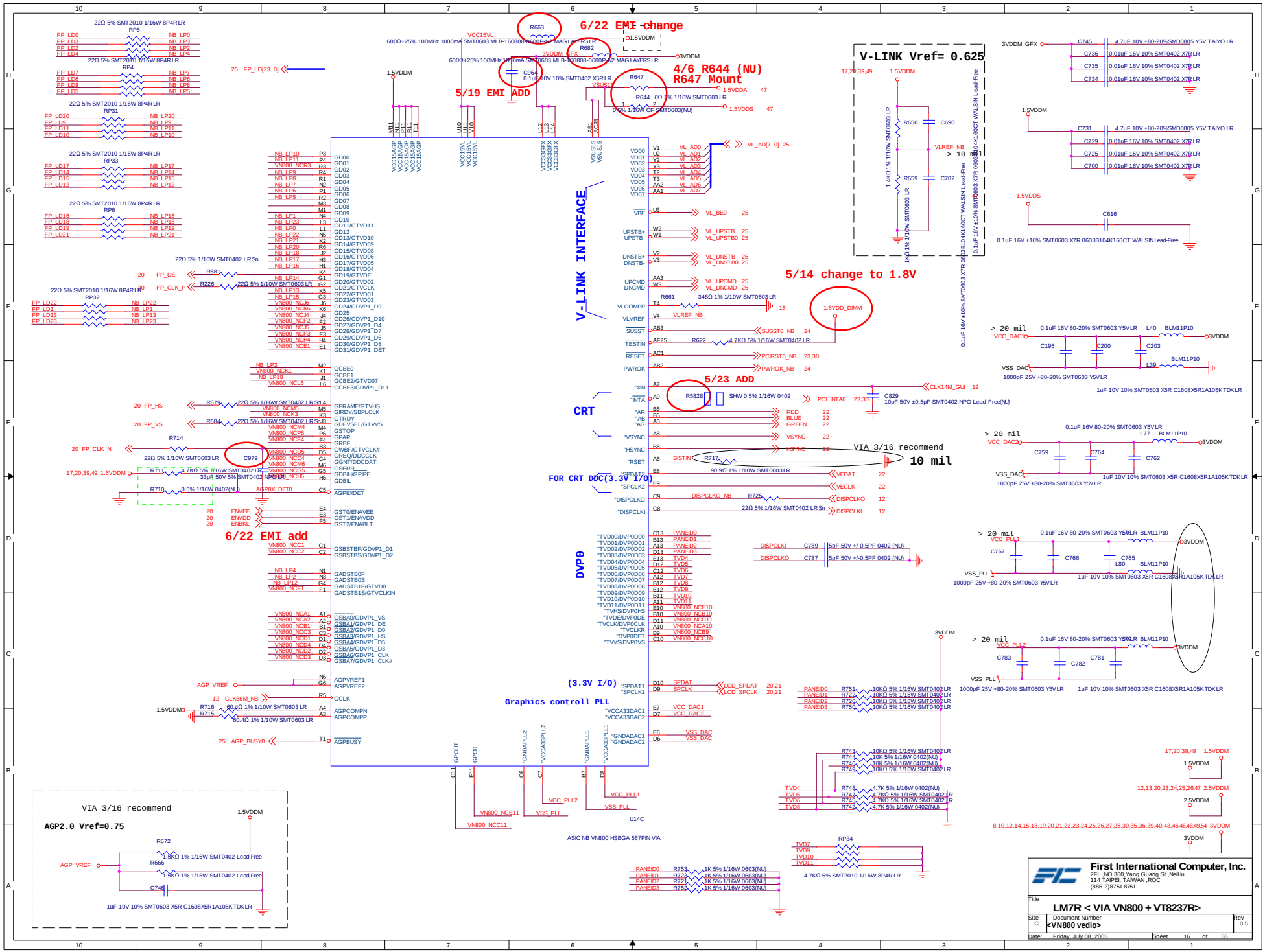
PDF created with pdfFactory trial version www.pdffactory.com

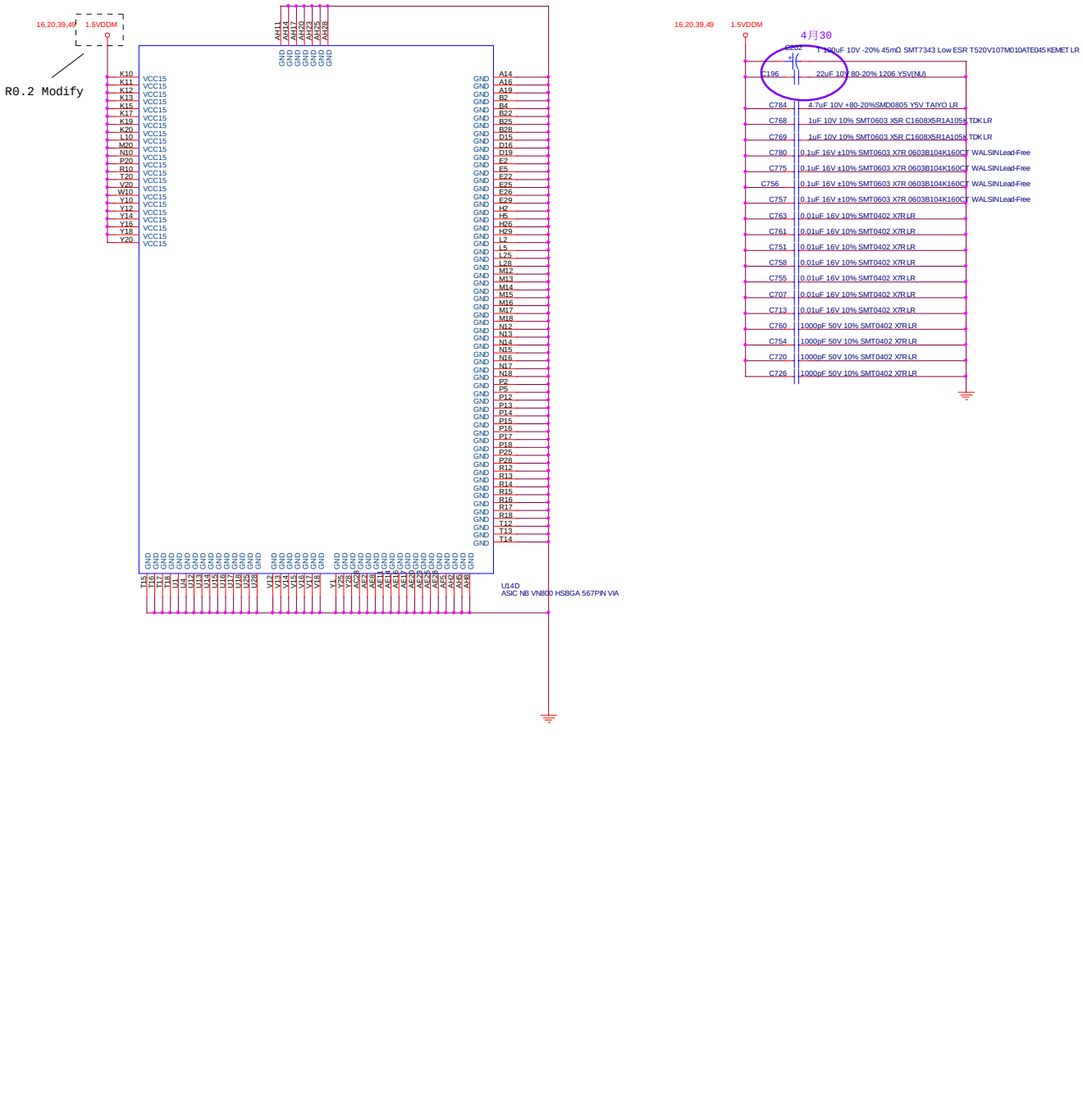
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title	LM7R < VIA VN800 + VT8237R>	
Size: C	Document Number: <clock buffer>	Rev: 0.5
Date: Friday, July 08, 2005	Sheet 13 of 56	

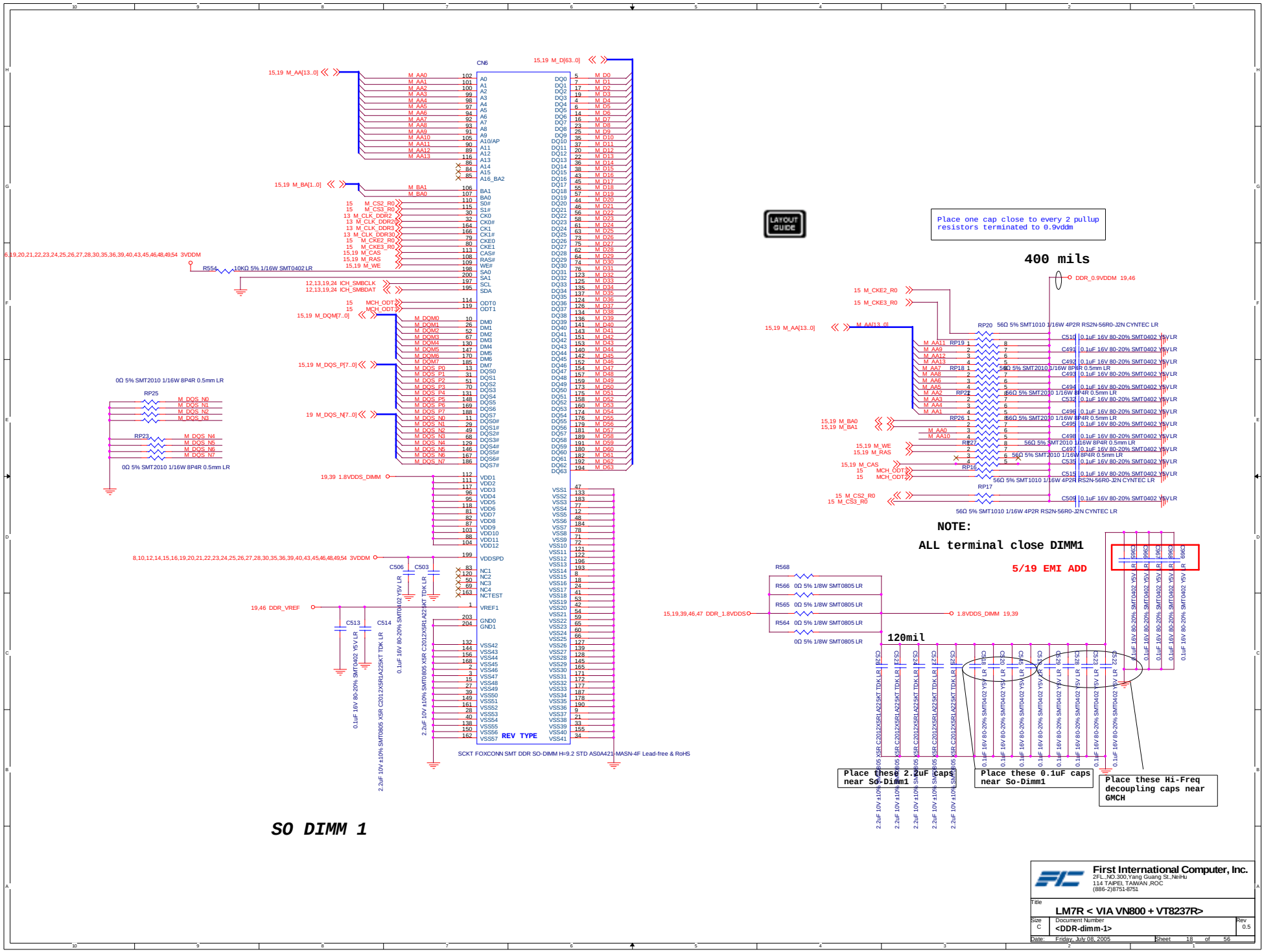


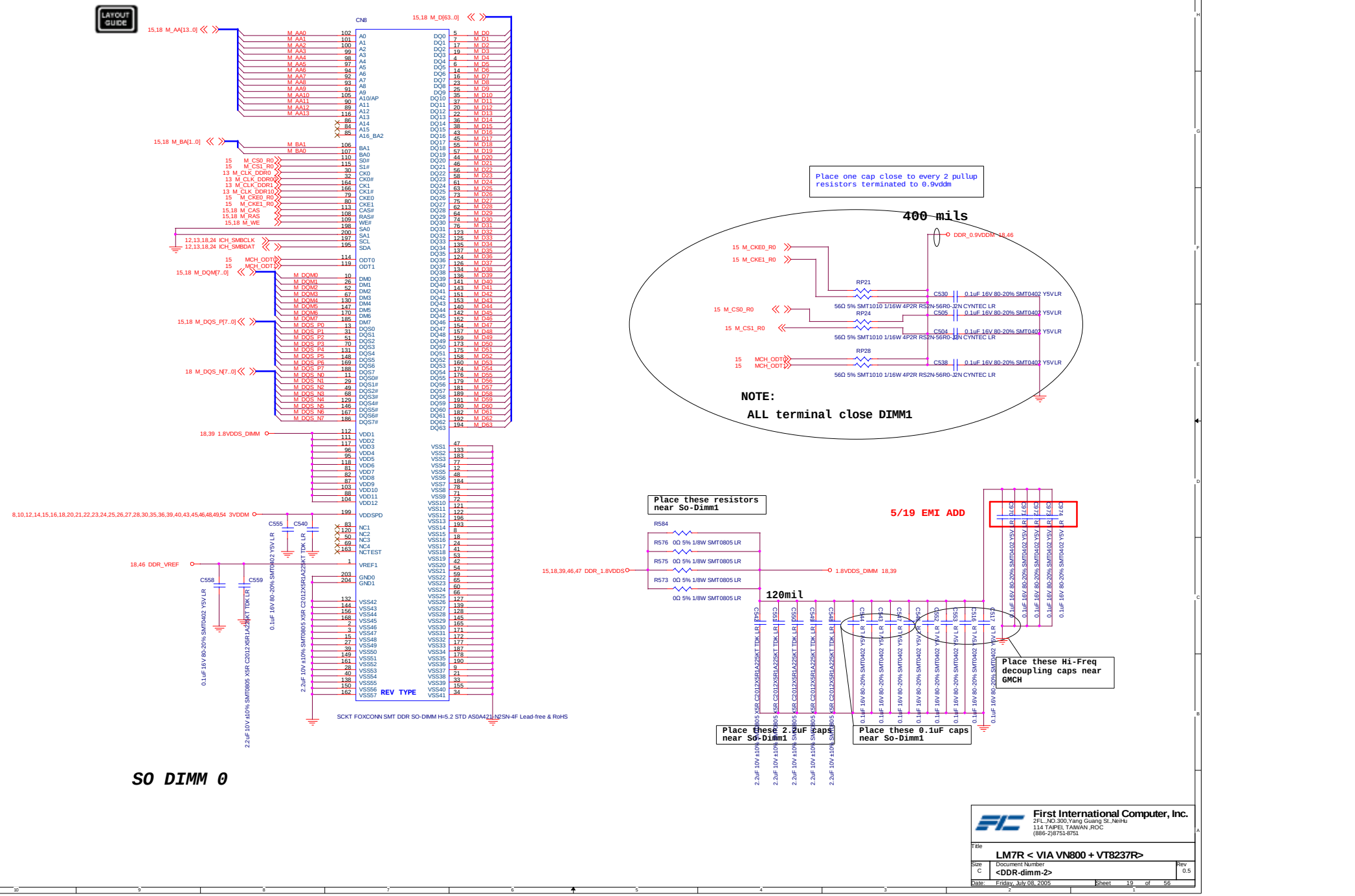


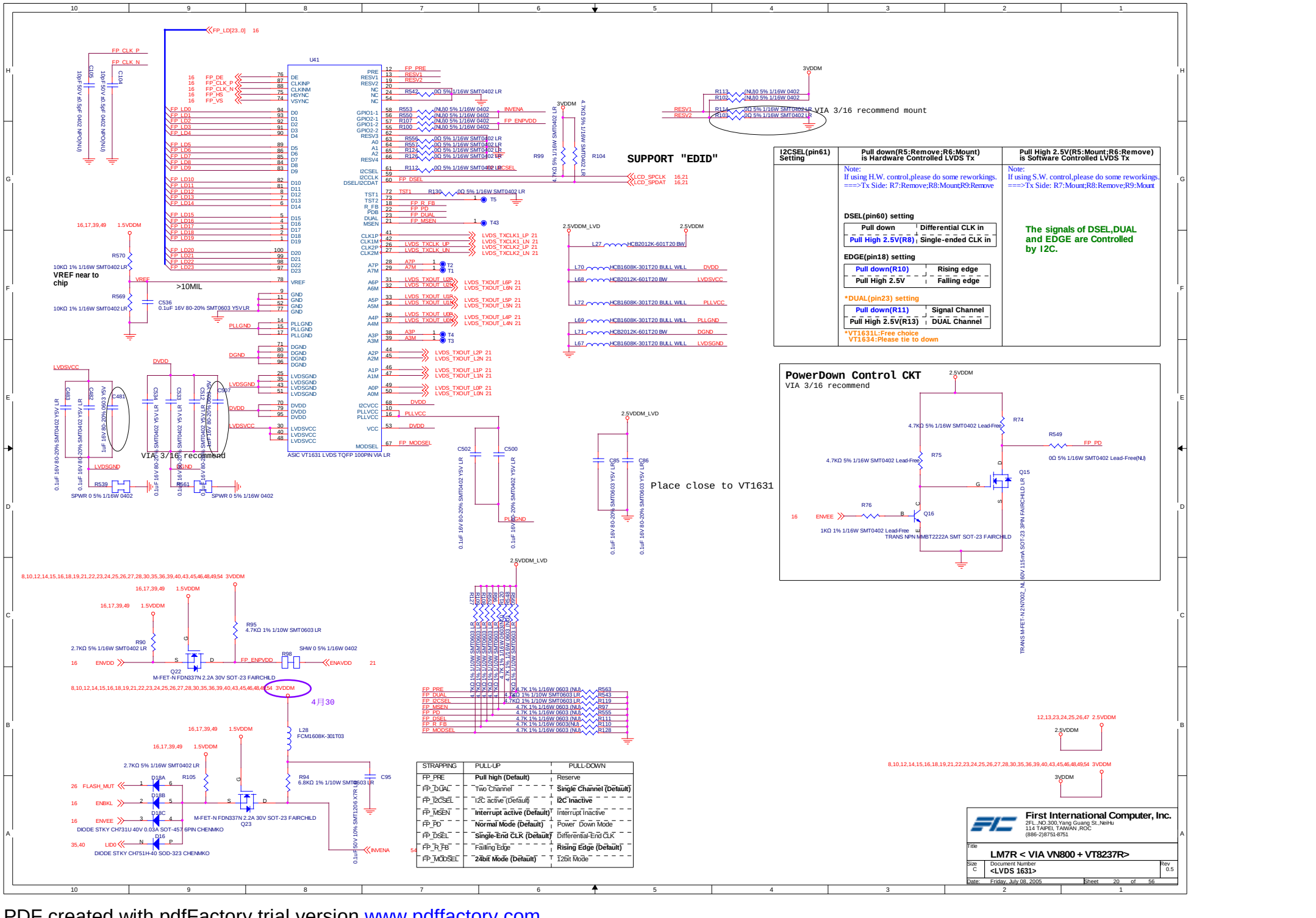


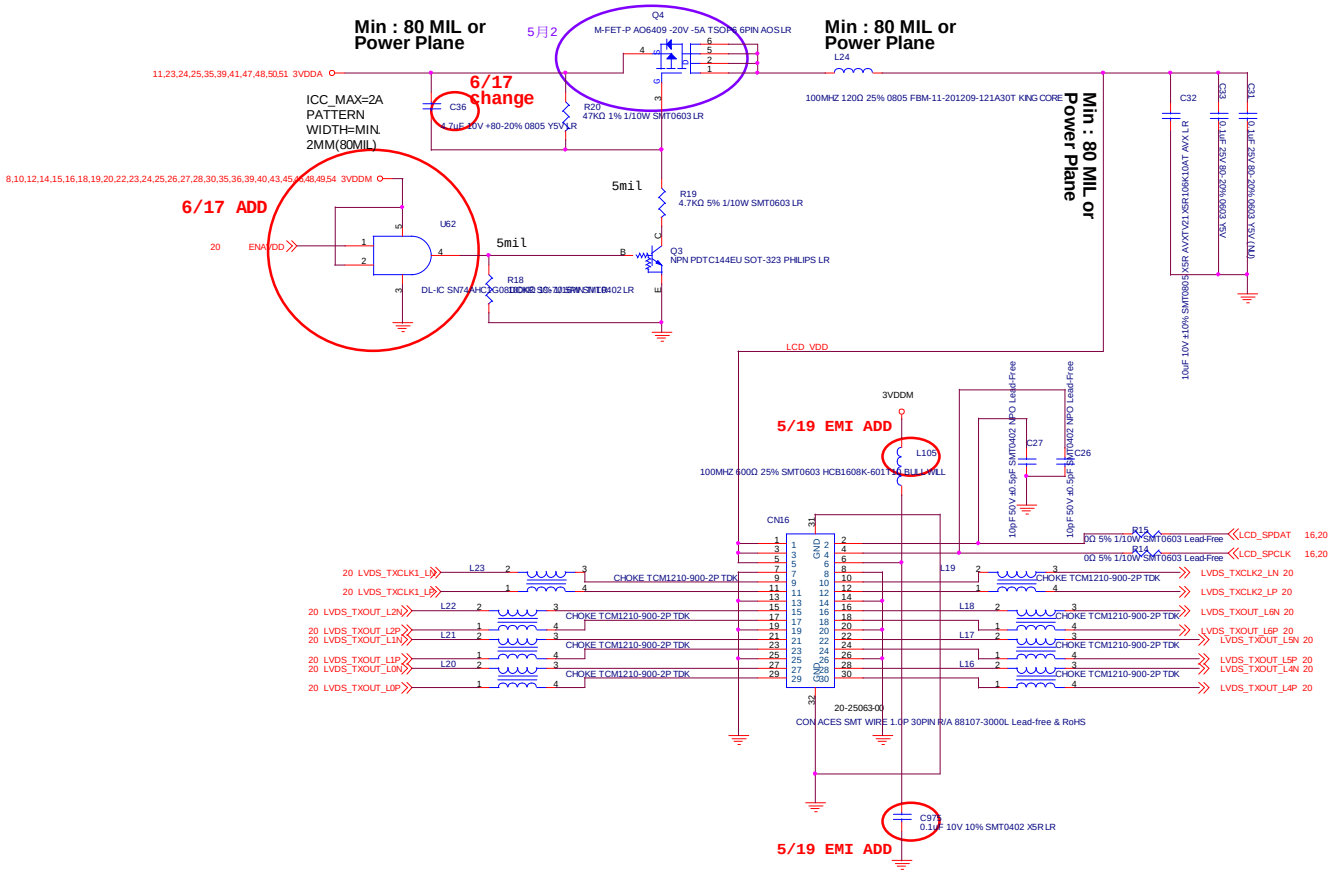


First International Computer, Inc.	2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751
Title	LM7R < VIA VN800 + VT8237R>
Size C	Document Number <VN800 power>
Rev	0.5
Date: Friday, July 08, 2005	Sheet 17 of 56









LVDS Interface

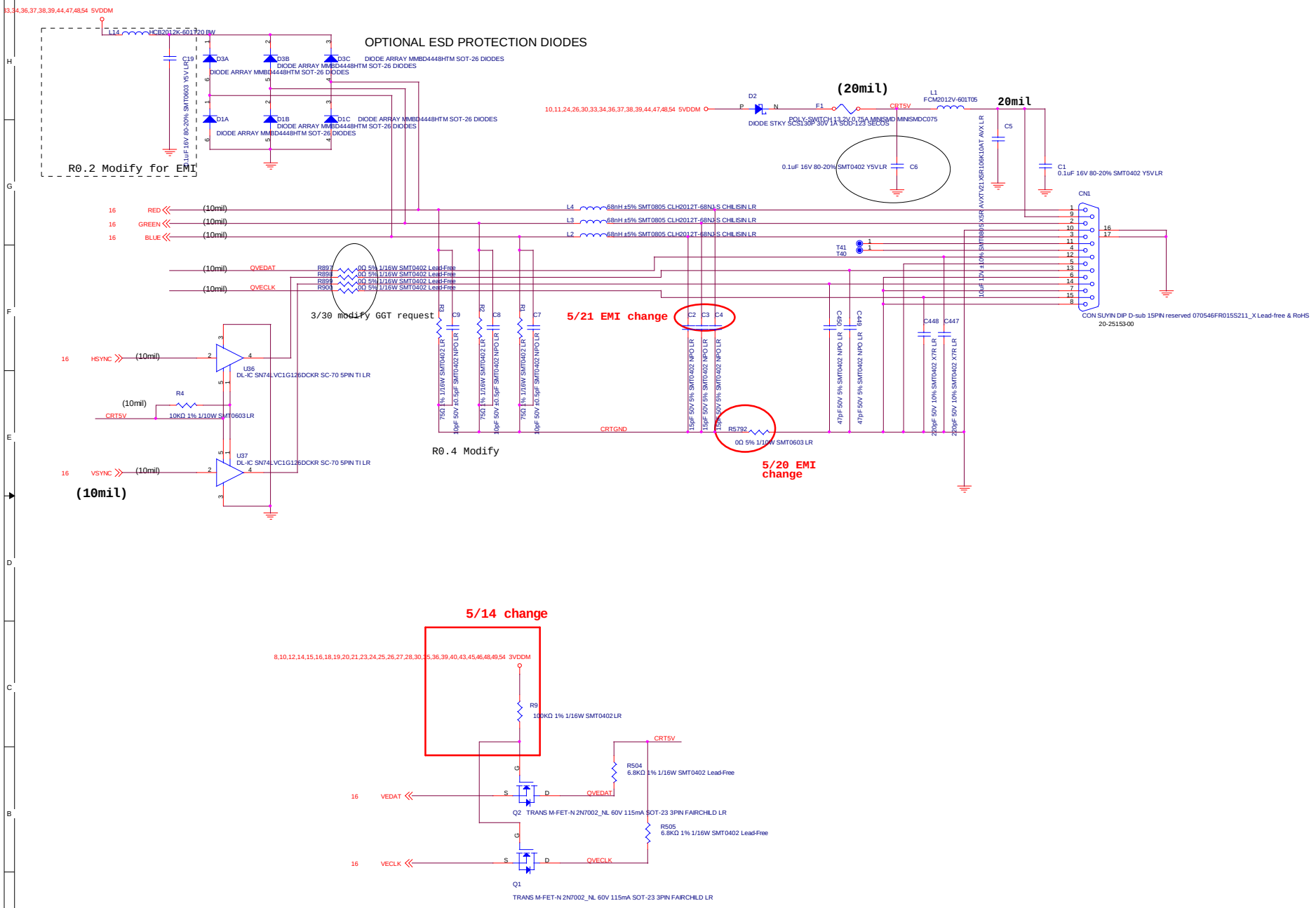
Signal	LENGTH	TRACE	SPACE	TRACE MUTCHING	Impedance	Note
LVDS	10" Cable MAX 16"	4 mils (stripline) 6 mils (microstrip)	20 mils 7 mils (edge to edge) 20 mils (pair to pair) 20 mils (to non LVDS signal)	+/-20 mils (data to clock) +/-20 mils (with a clock pair) X +/-20 mils (clock to clock)	100 ohms +/-15%	Breakout region from NB should be less than 500 mils

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

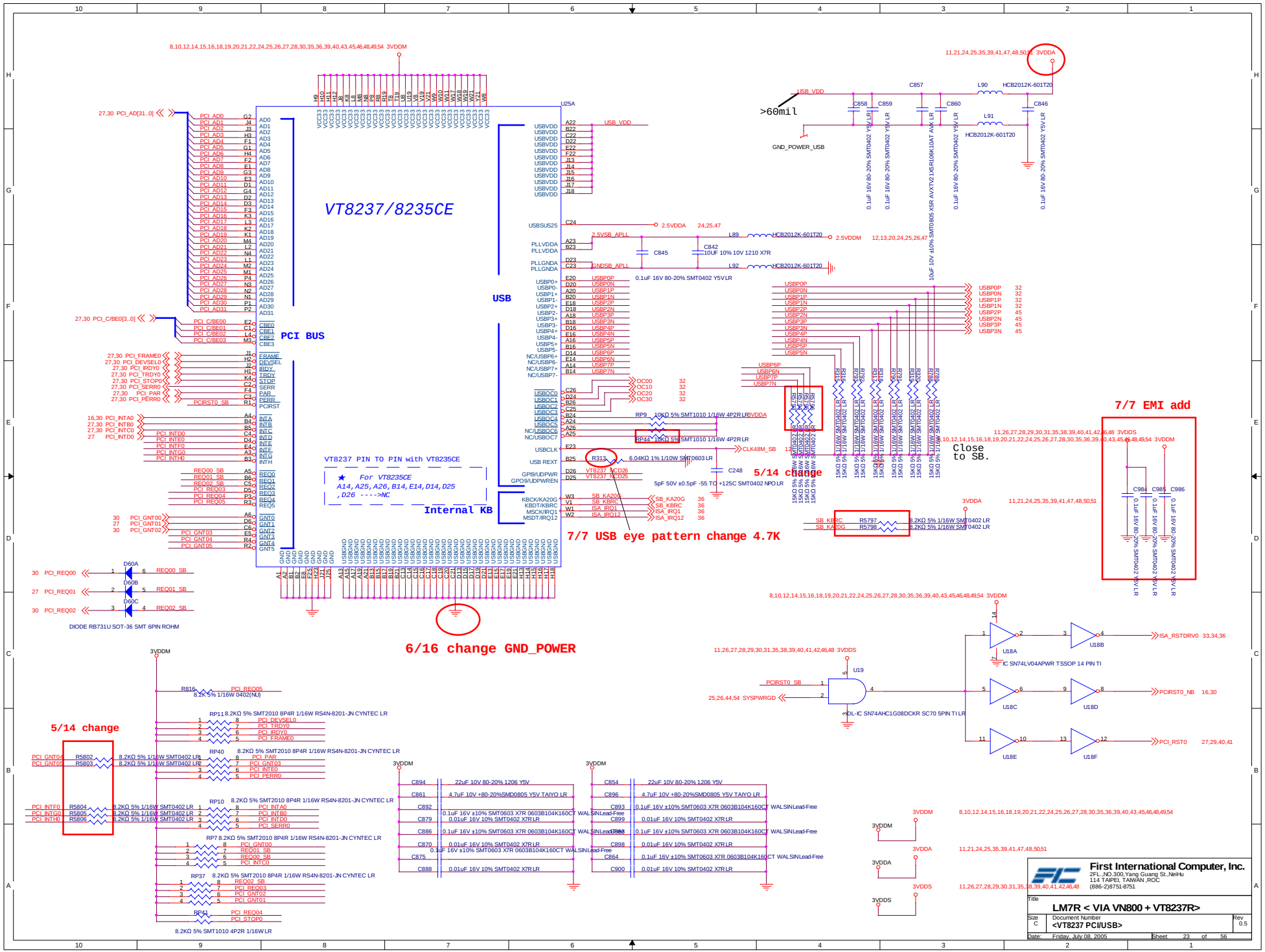
Title: LM7R < VIA VN800 + VT8237R>

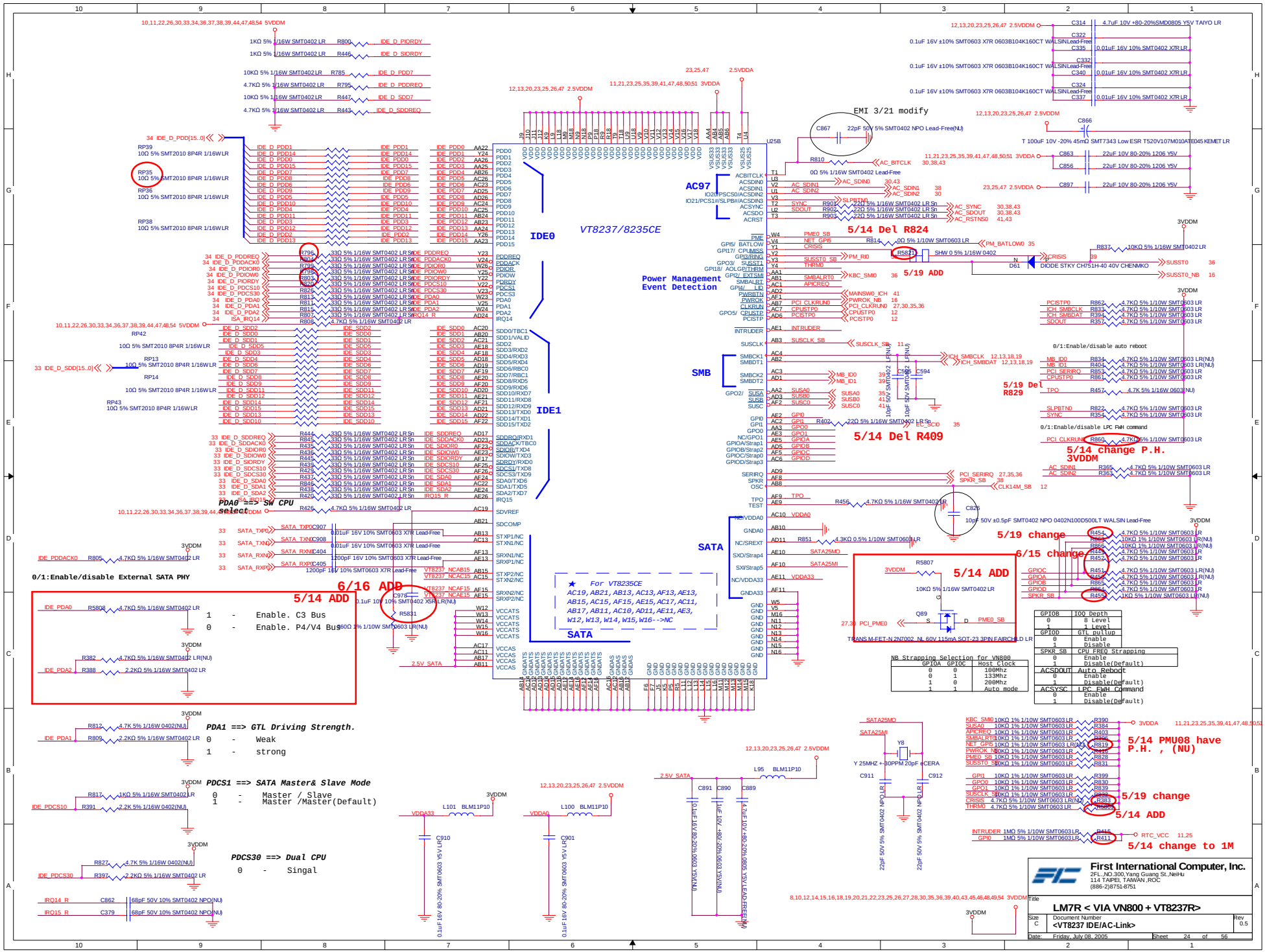
Size: C | Document Number: <LCD connecter> | Rev: 0.5

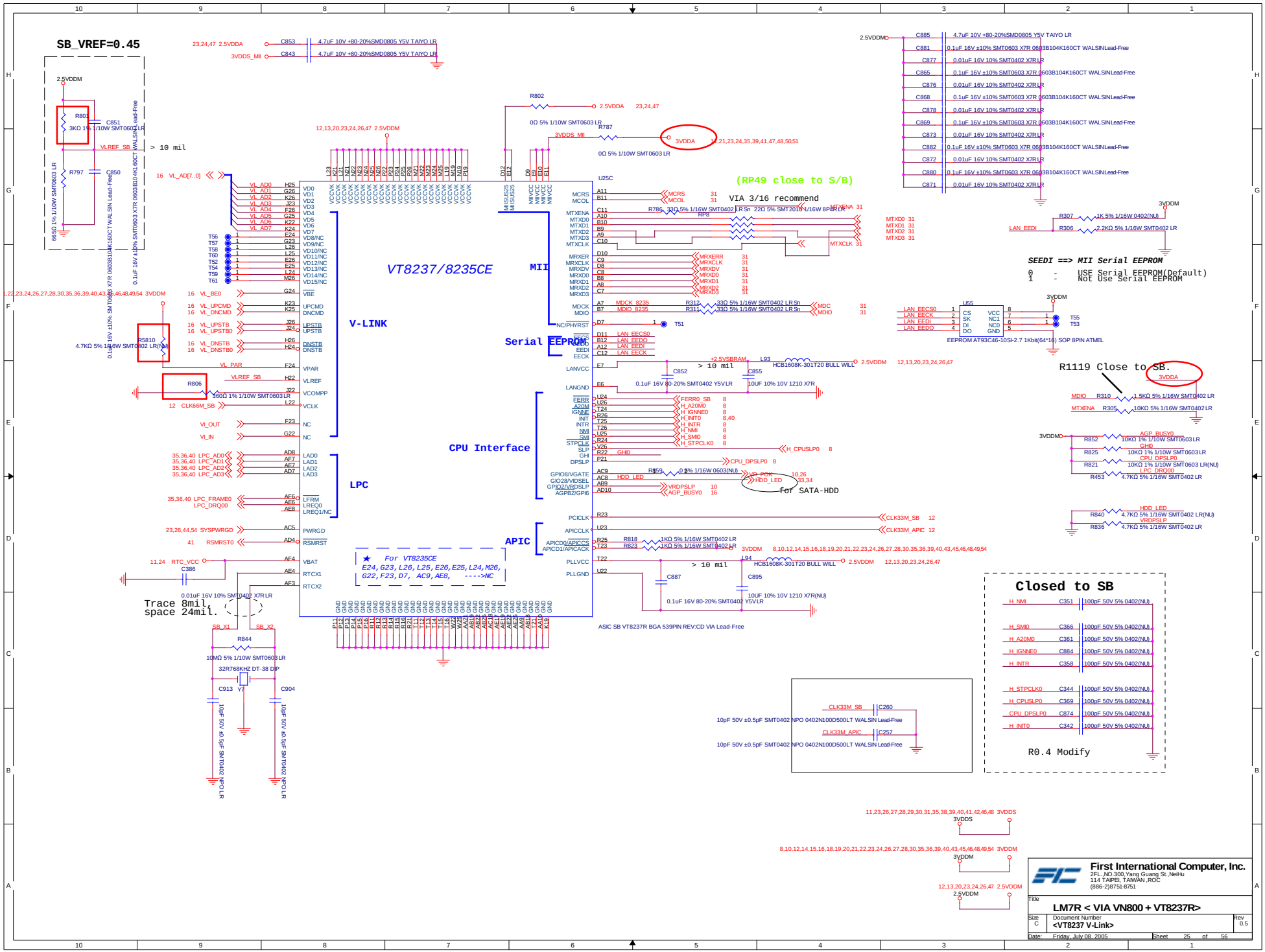
Date: Friday, July 08, 2005 | Sheet 21 of 56



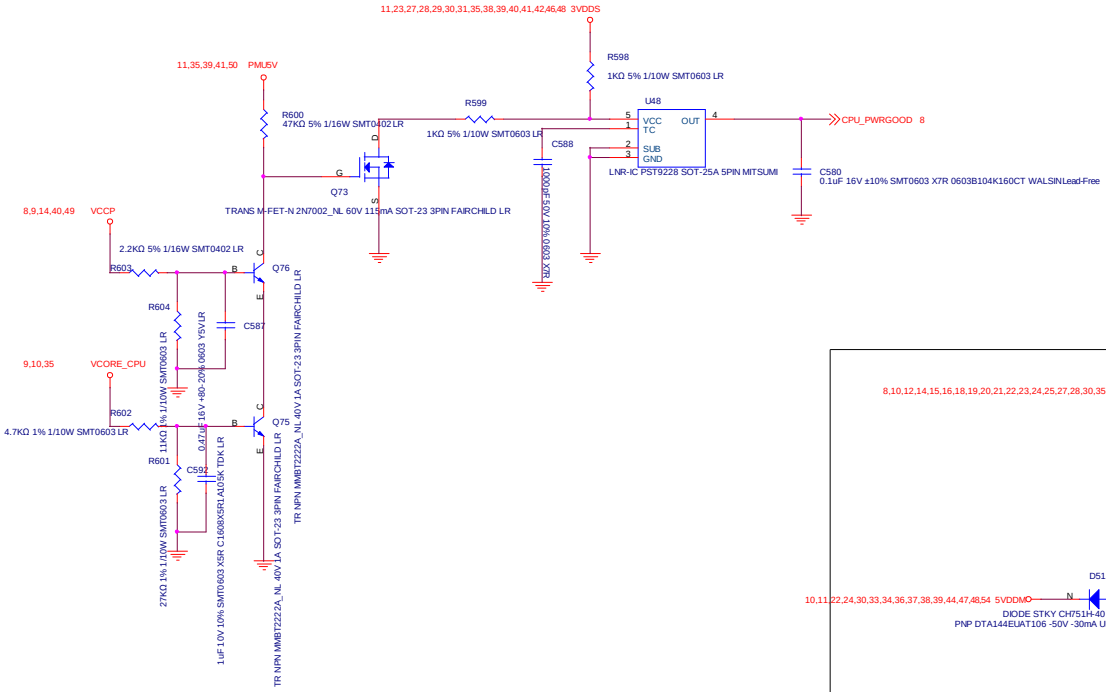
Company	First International Computer, Inc.
Address	2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC
Phone	(886-2)8751-8751
Title	LM7R < VIA VN800 + VT8237R>
Size	C
Document Number	<CRT connector>
Rev	0.5
Date	Friday, July 08, 2005
Sheet	22 of 56



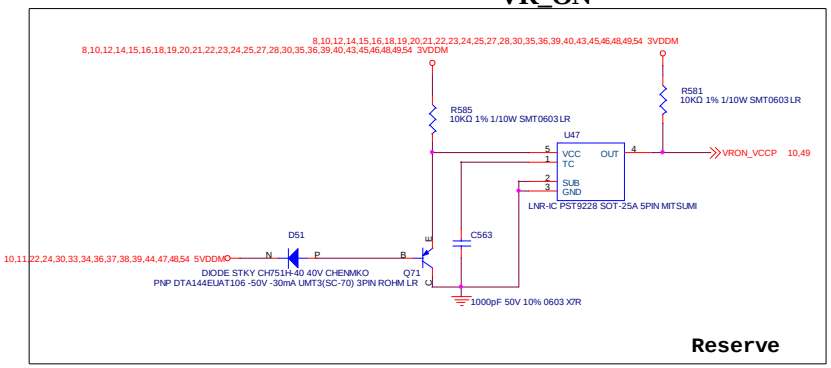




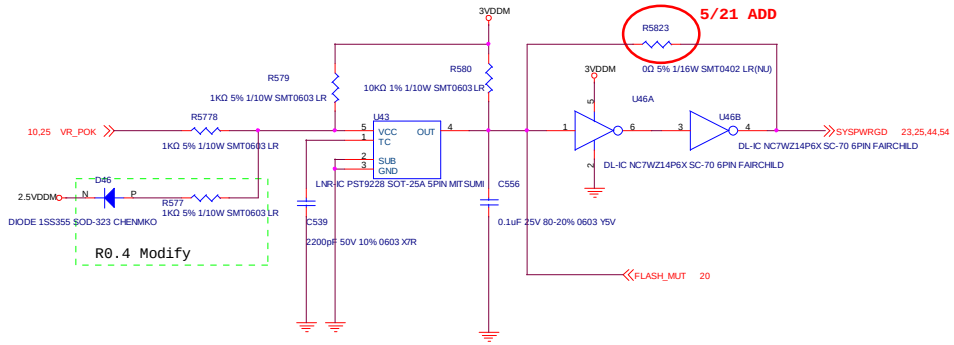
CPU POWER OK CIRCUIT

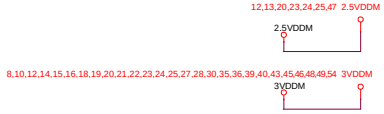


VR_ON



SYSTEM POWER OK CIRCUIT



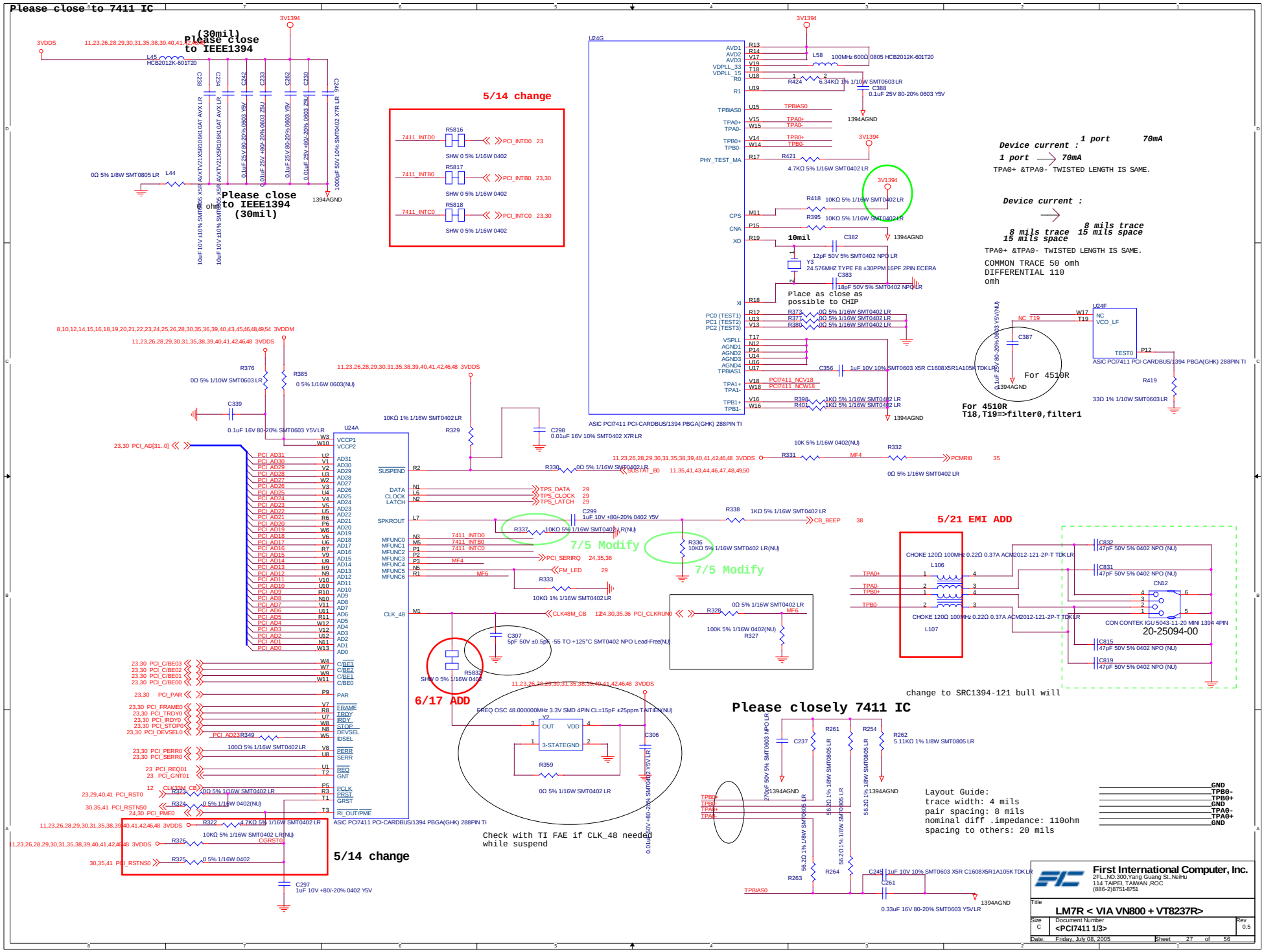


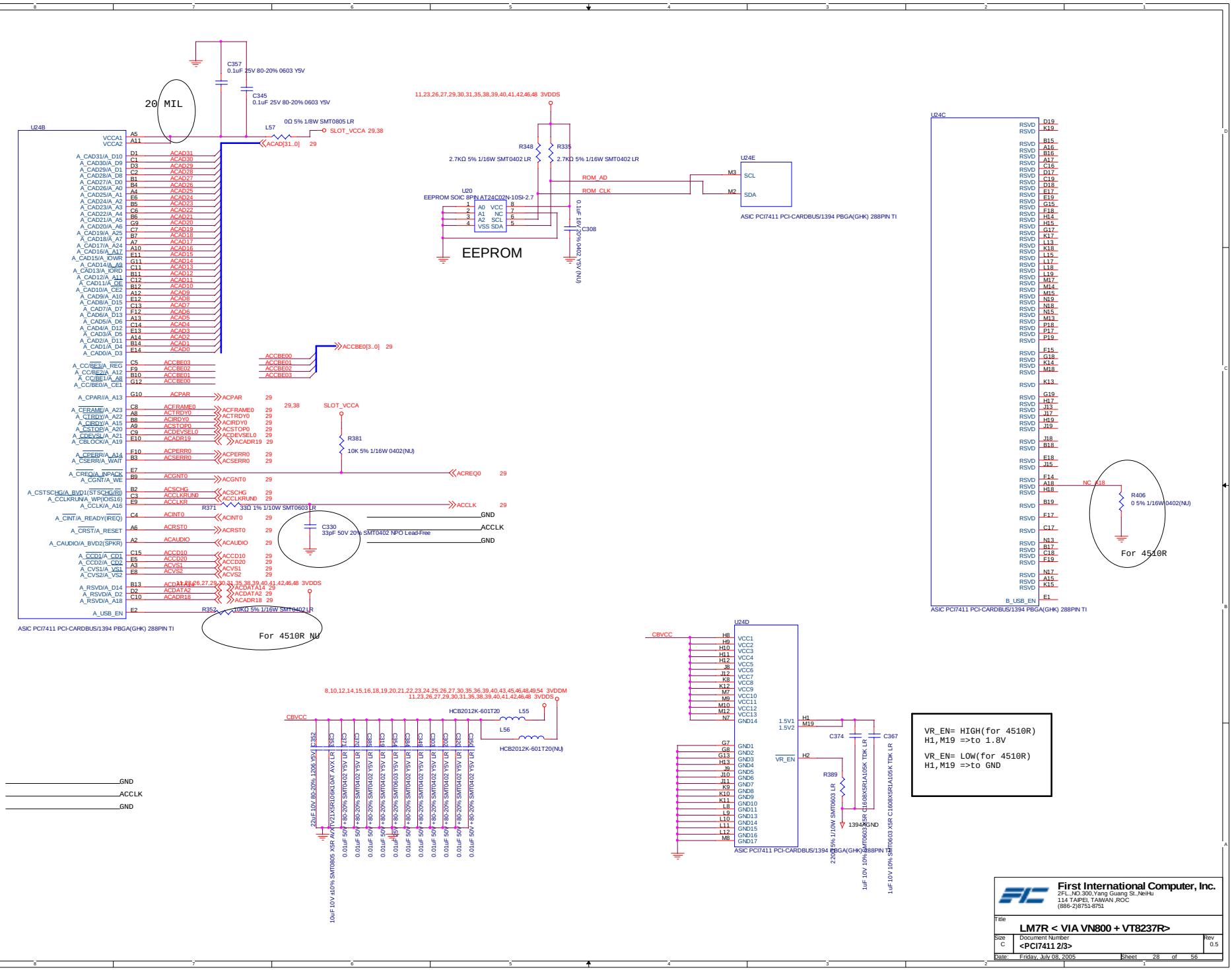
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

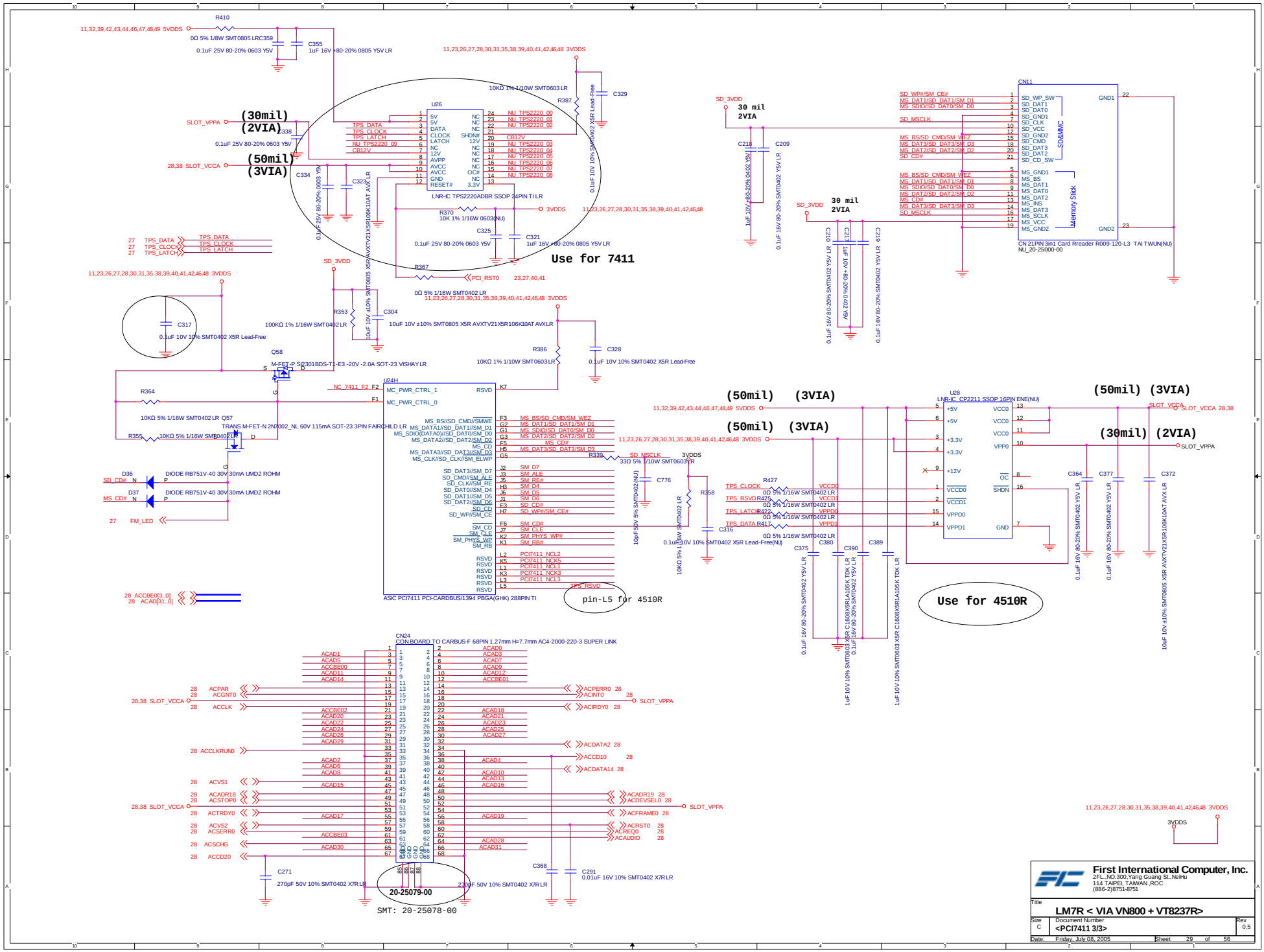
Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <POWER Good> | Rev: 0.5

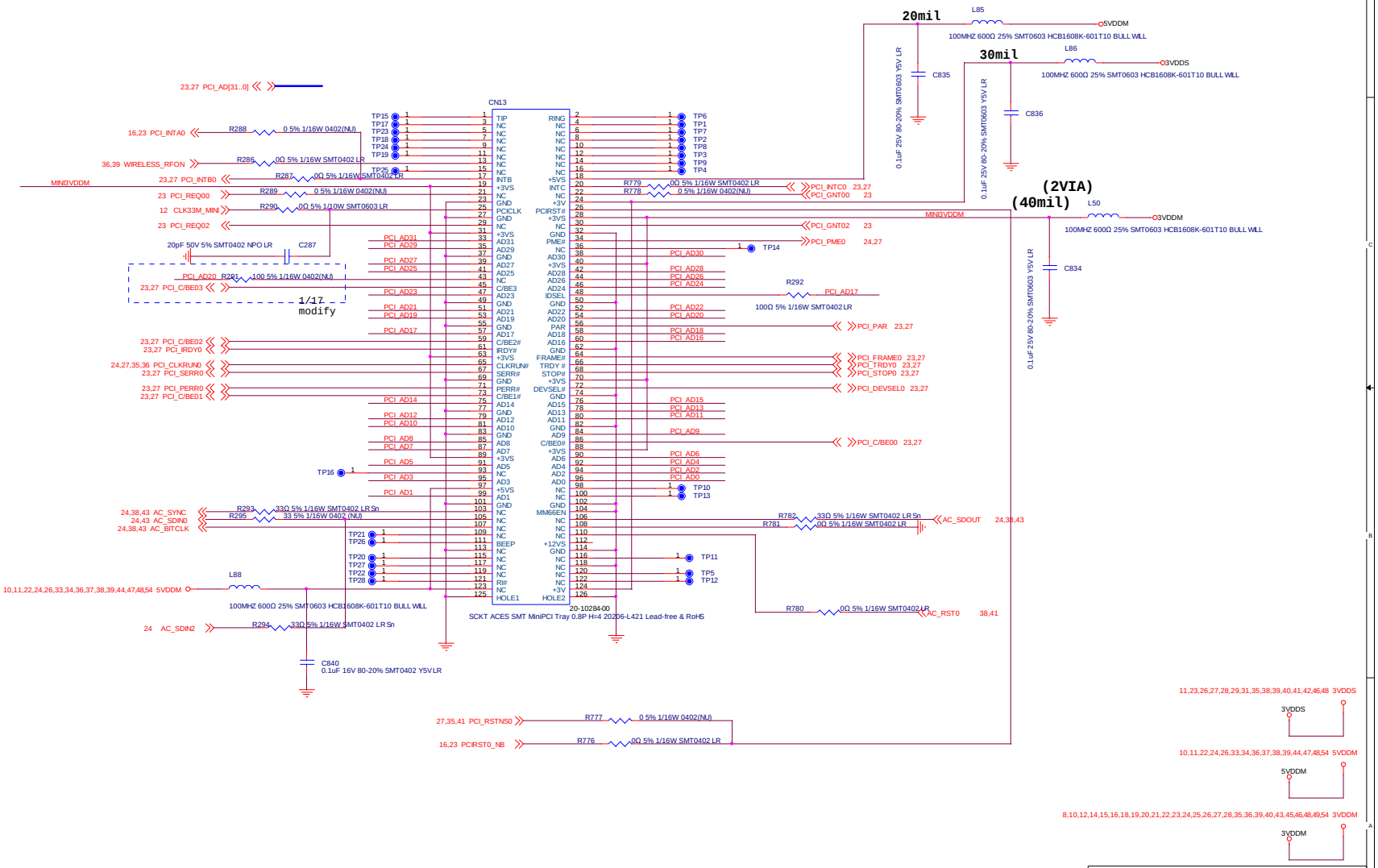
Date: Friday, July 08, 2005 | Sheet 26 of 56





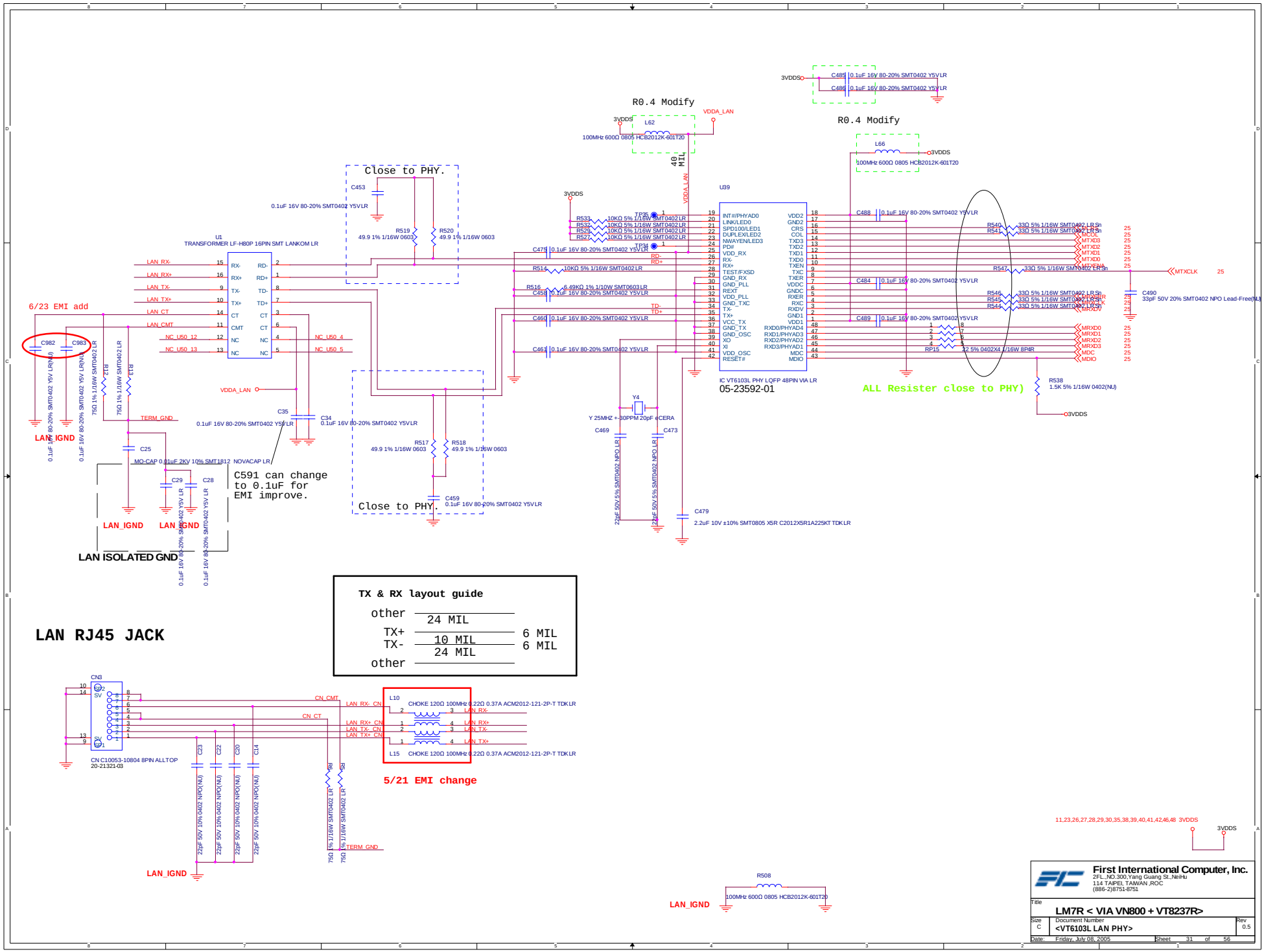


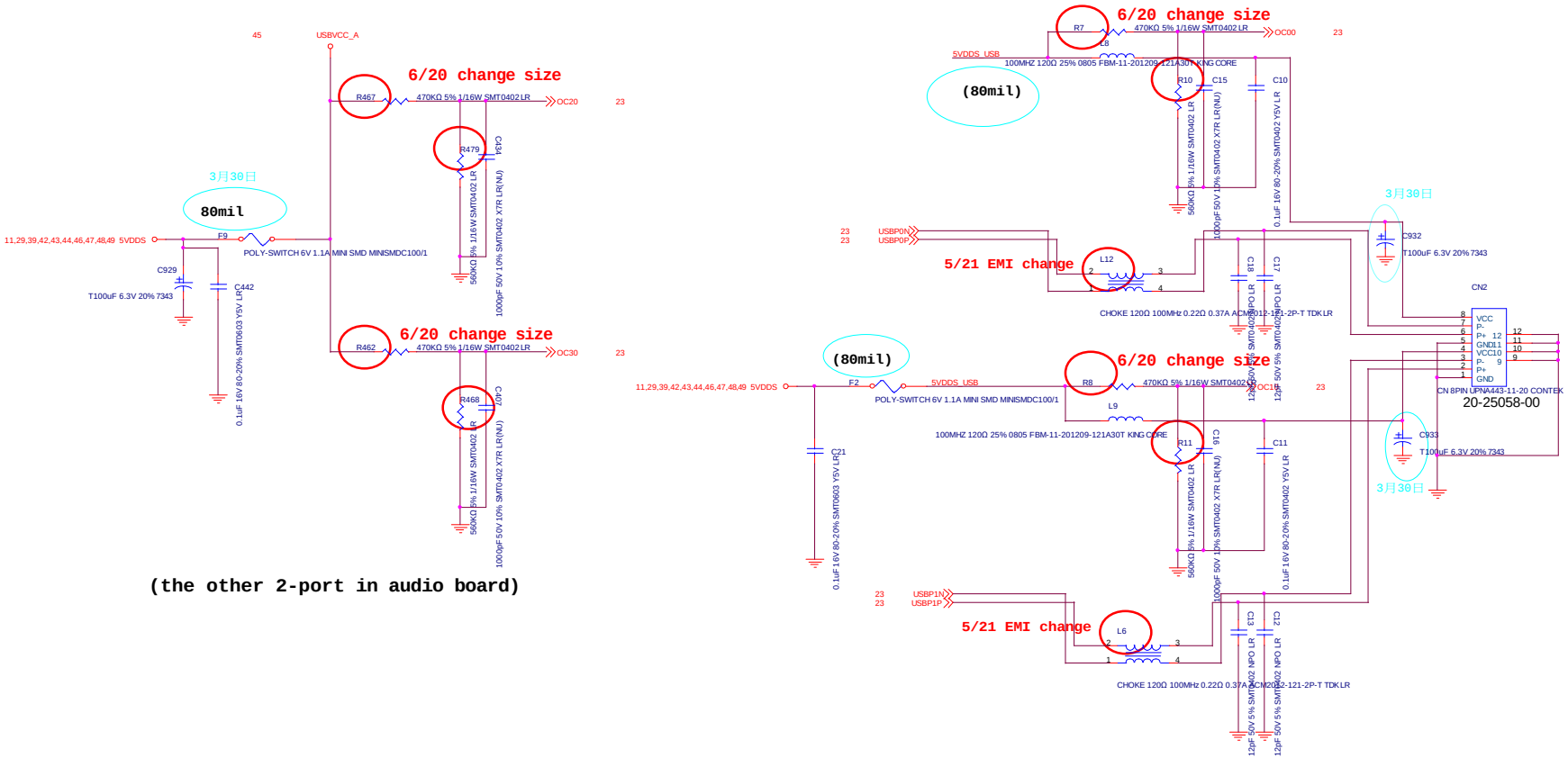
TYPE III MODEM / LAN CONNECTOR



First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title	LM7R < VIA VN800 + VT8237R>	
Size: C	Document Number: <Mini-PCI>	Rev: 0.5
Date: Friday, July 08, 2005	Sheet 30 of 56	





(the other 2-port in audio board)

First International Computer, Inc.	2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751
Title	LM7R < VIA VN800 + VT8237R>
Size: C	Document Number: <USB CNN>
Rev: 0.5	
Date: Friday, July 08, 2005	Sheet 32 of 56

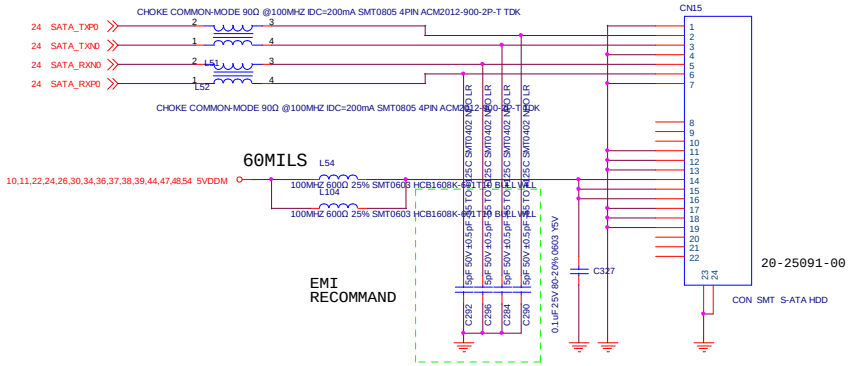
SATA Layout Note:

MS or SL:

* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.

NOTE

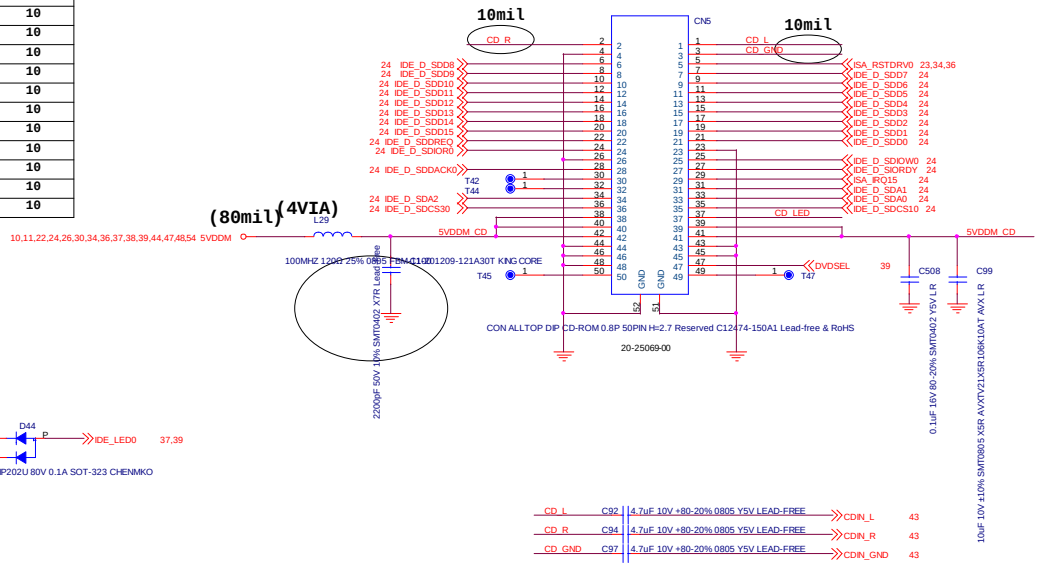
SATA differential stripline 20:5:6:5:20
SATA differential mircostripline 20:6:6:6:20
請包GROUND

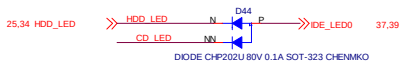


IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

CDROM CNN





First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

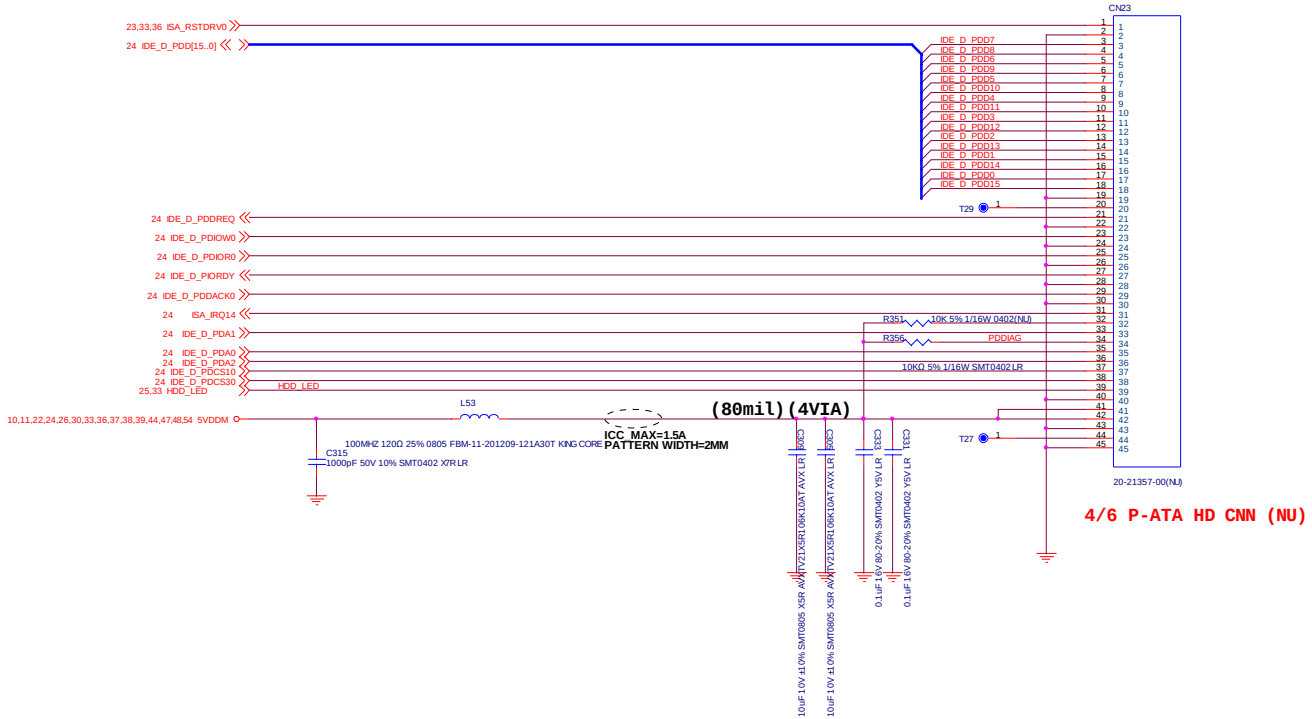
Size: C | Document Number: <IDE connector> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 33 of 56

IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

PATA-HDD SWITCH CNN(option)

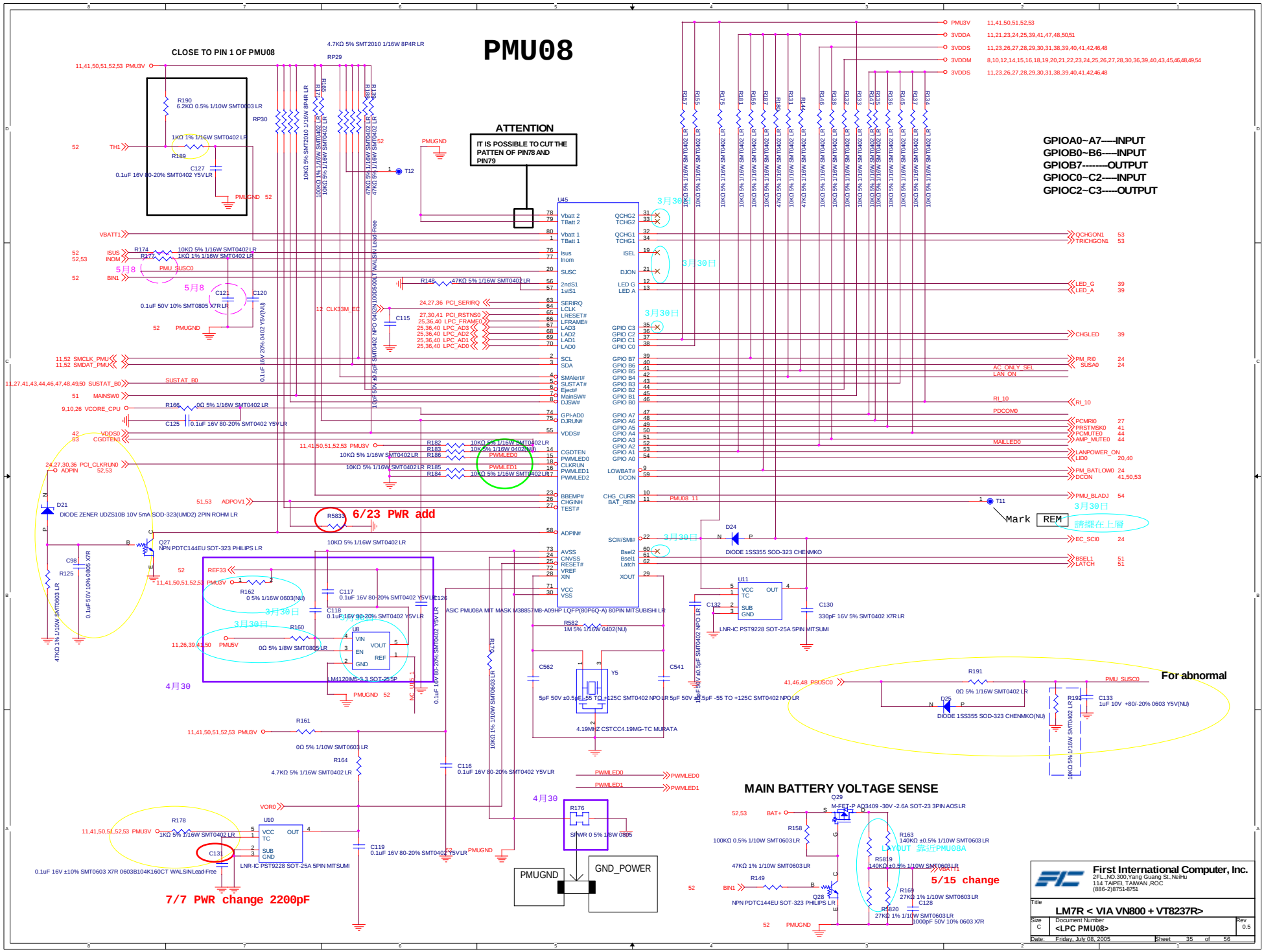


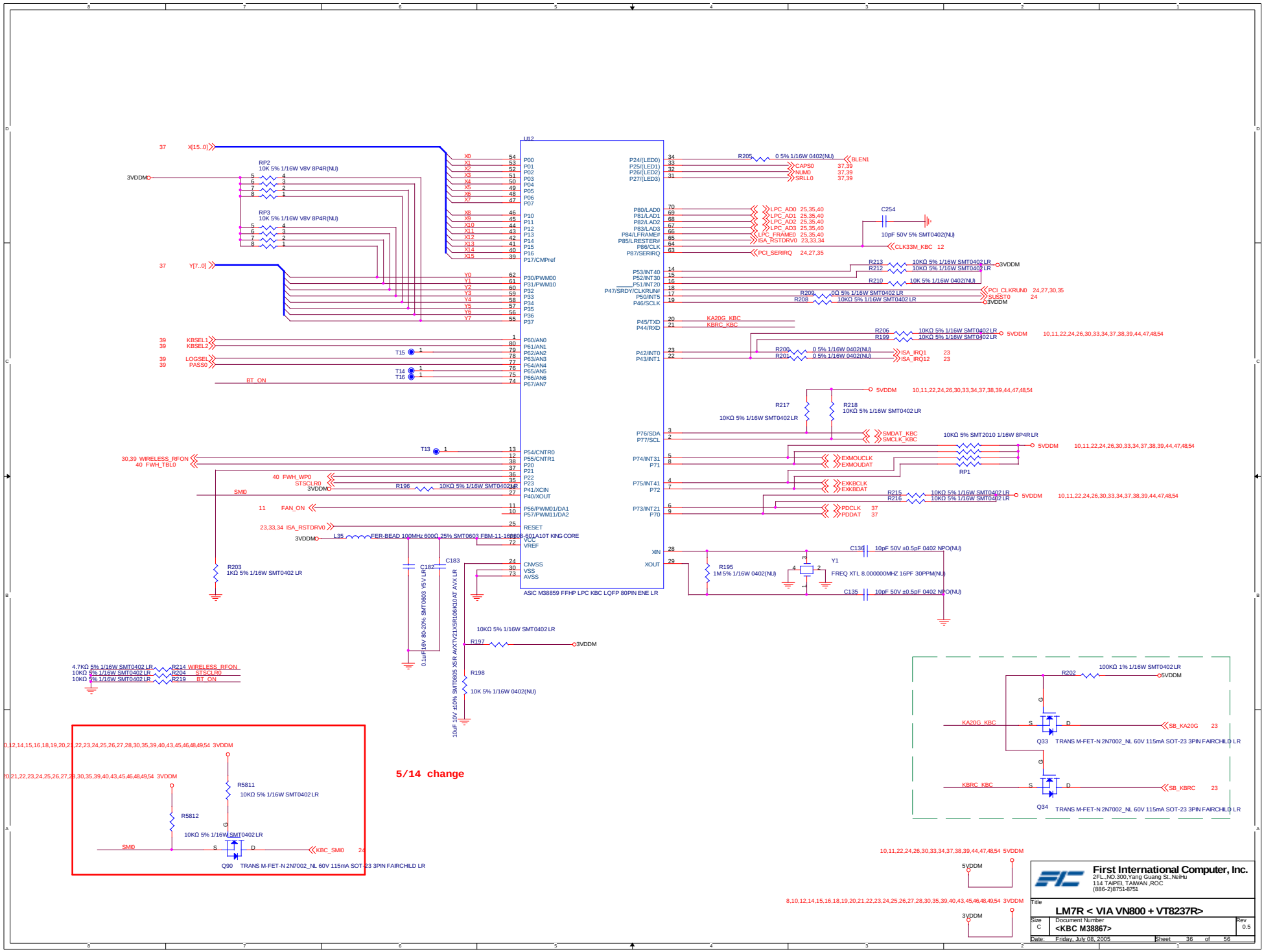
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

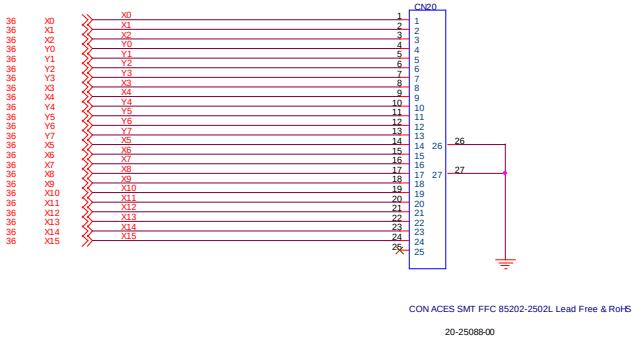
Size: C | Document Number: <PATA-FPC-CNN> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 34 of 56

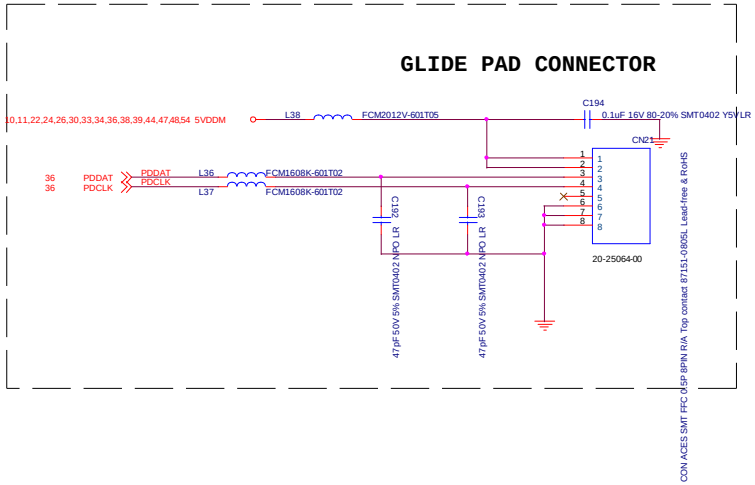


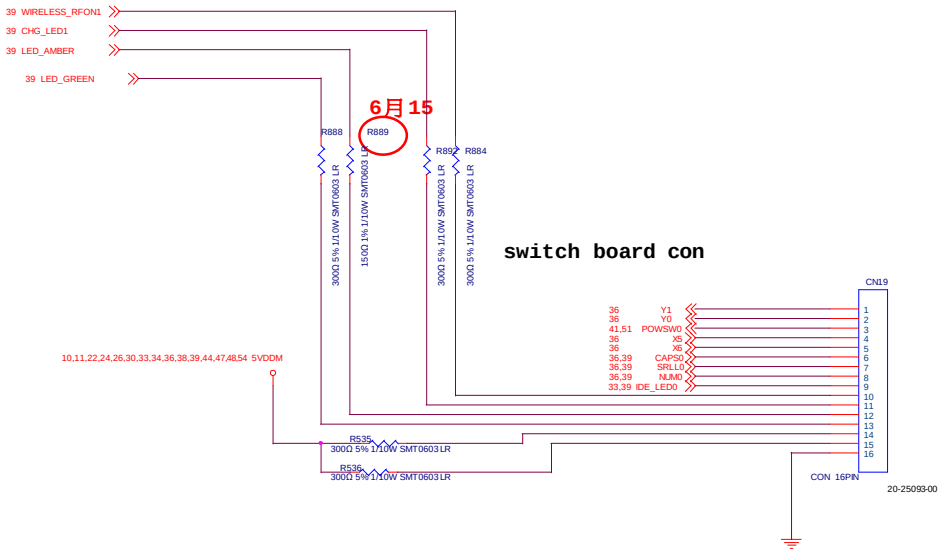


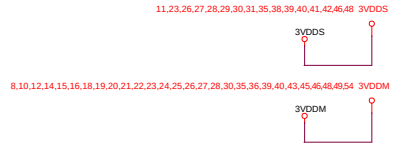
INT KB CNN



GLIDE PAD CONNECTOR







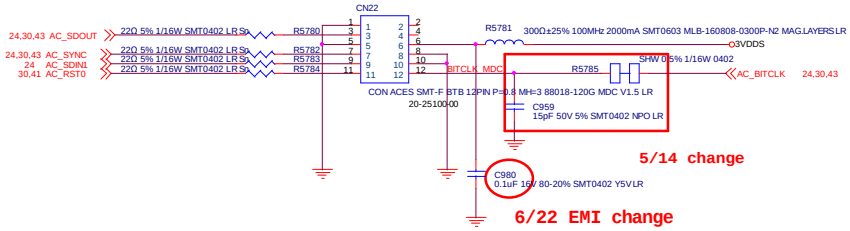
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

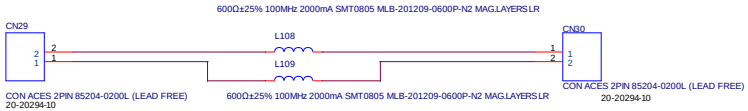
Title: LM7R < VIA VN800 + VT8237R>

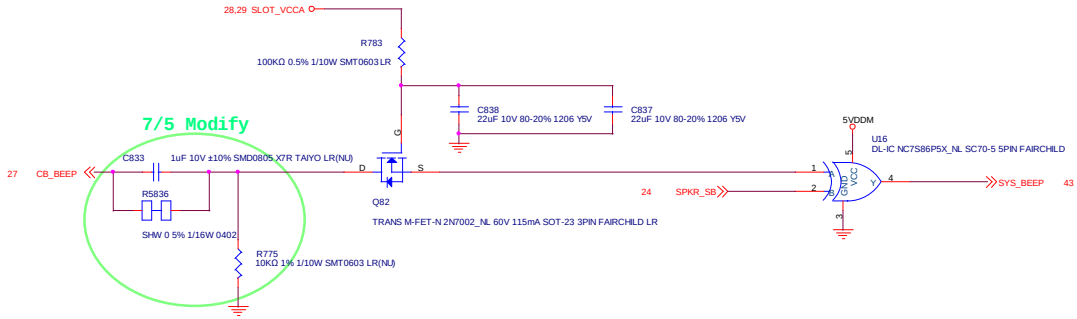
Size: C | Document Number: <INT K/B /GP/SW CNN> | Rev: 0.5

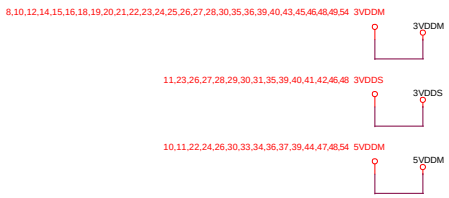
Date: Friday, July 08, 2005 | Sheet 37 of 56

MDC 1.5 CNN





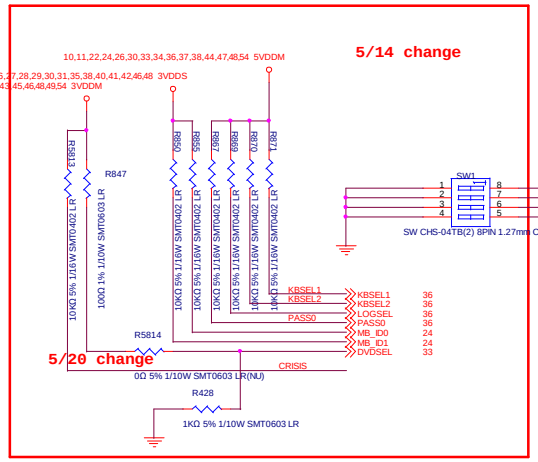


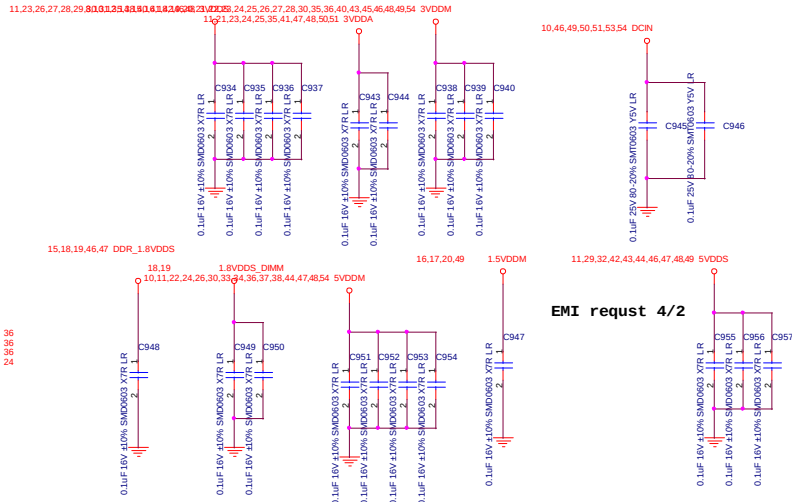


First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

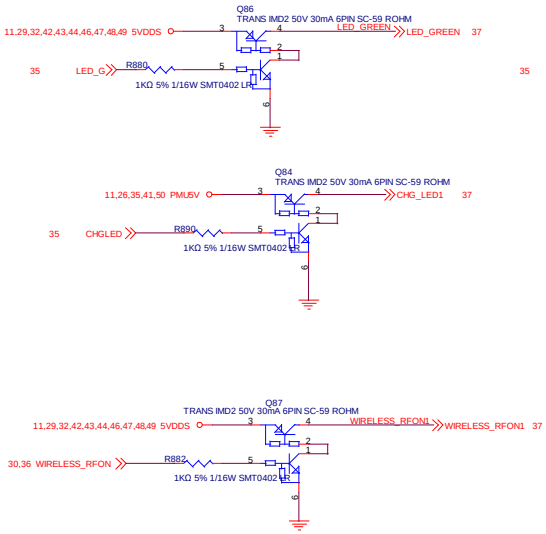
Title	LM7R < VIA VN800 + VT8237R>	
Size C	Document Number <MDC CNN>	Rev 0.5
Date: Friday, July 08, 2005	Sheet 38 of 56	

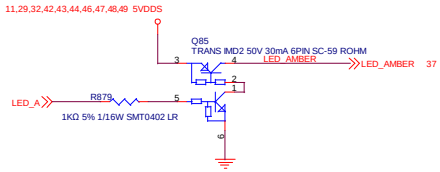
DIP SWITCH





LED indicator control logic





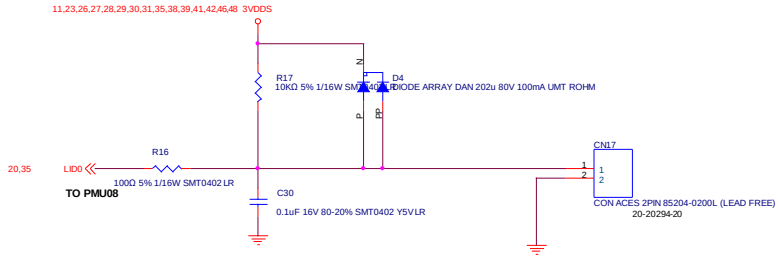
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

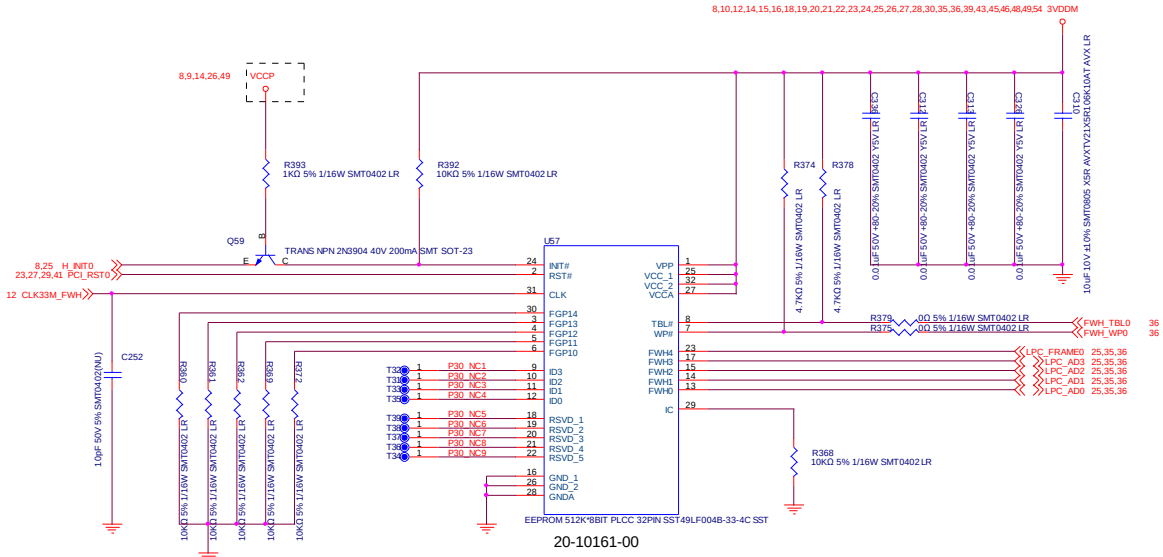
Size: C | Document Number: <DIP SW/ LED> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 39 of 56

LID Switch



4M FLASH ROM



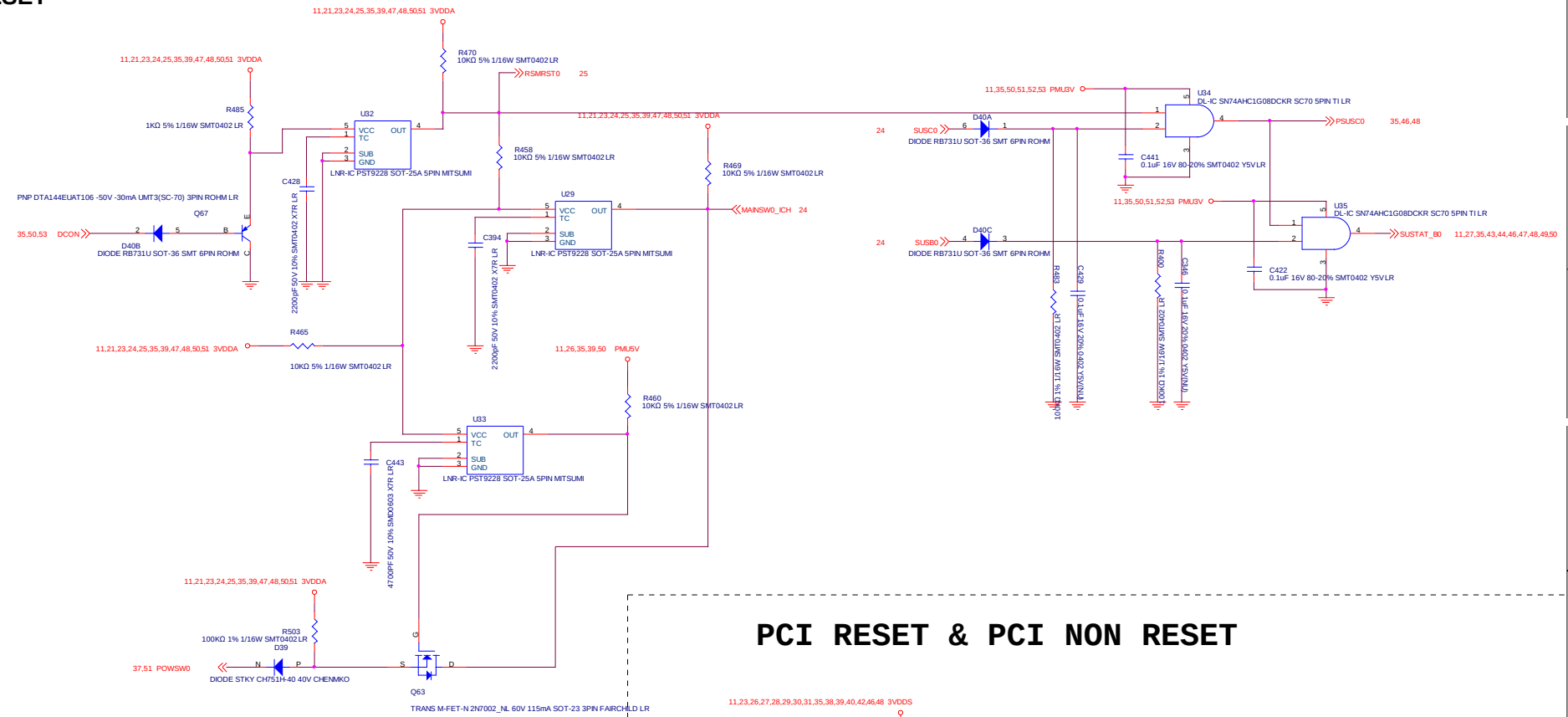
20-10161-00

20-10161-00 SOCKET

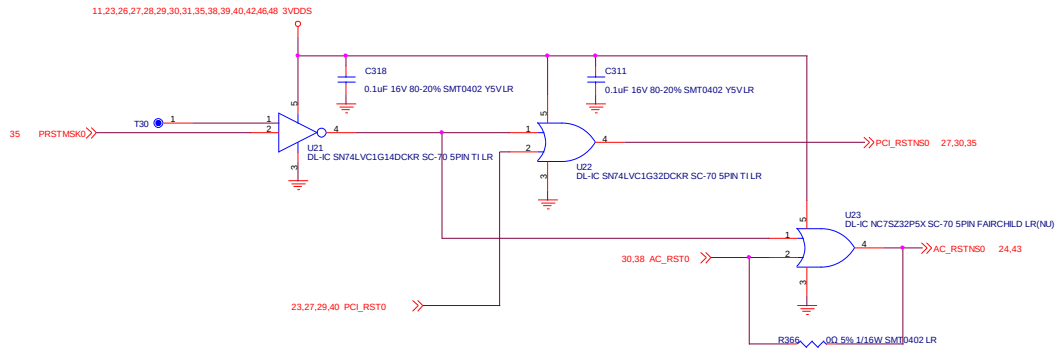
03-10119-15 Atmel Flash

First International Computer, Inc.	2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751
Title	LM7R < VIA VN800 + VT8237R>
Size: C	Document Number: <LID SW/ BIOS>
Rev: 0.5	
Date: Friday, July 08, 2005	Sheet 40 of 56

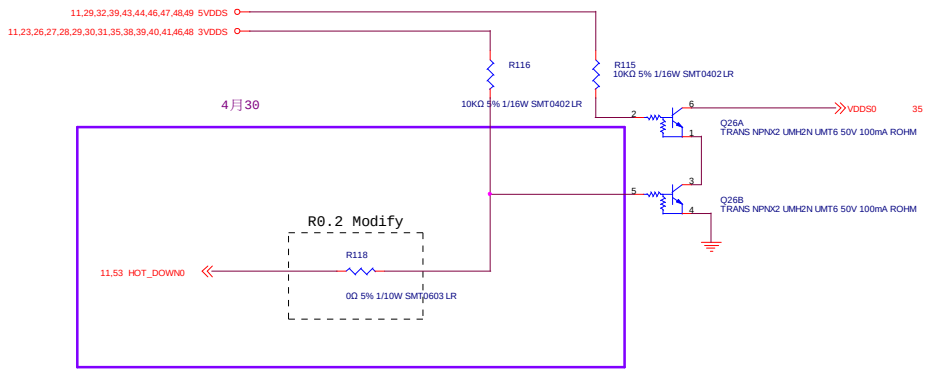
RESUME RESET

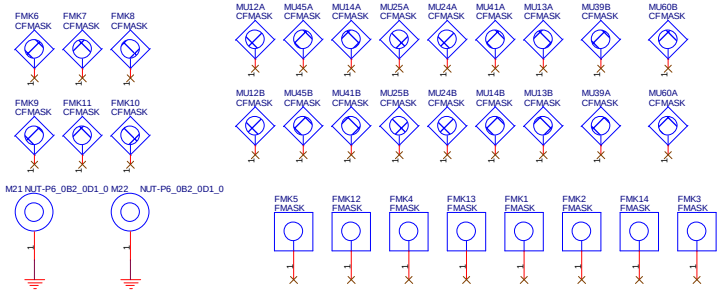


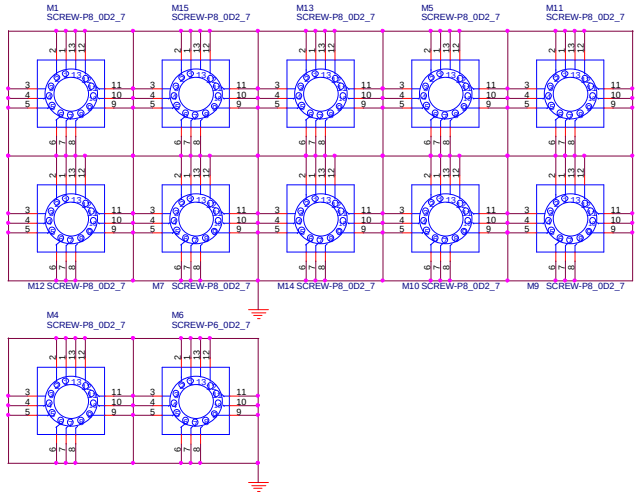
PCI RESET & PCI NON RESET



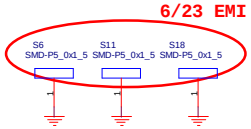
First International Computer, Inc.	2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751
Title	LM7R < VIA VN800 + VT8237R>
Size: C	Document Number: <Reset Circuit>
Rev: 0.5	
Date: Friday, July 08, 2005	Sheet 41 of 56

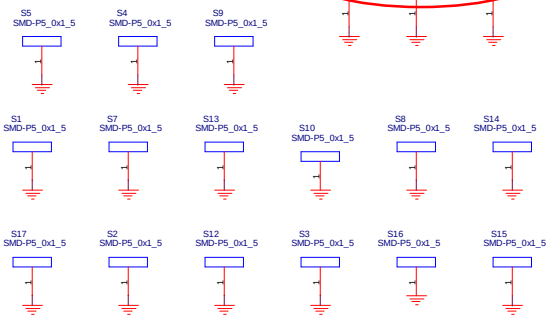


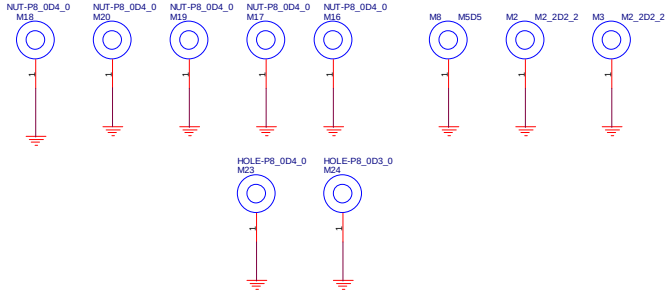




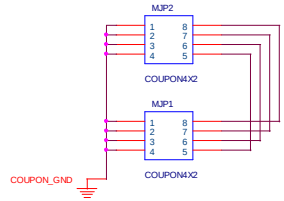
6/23 EMI change







COUPON4X2

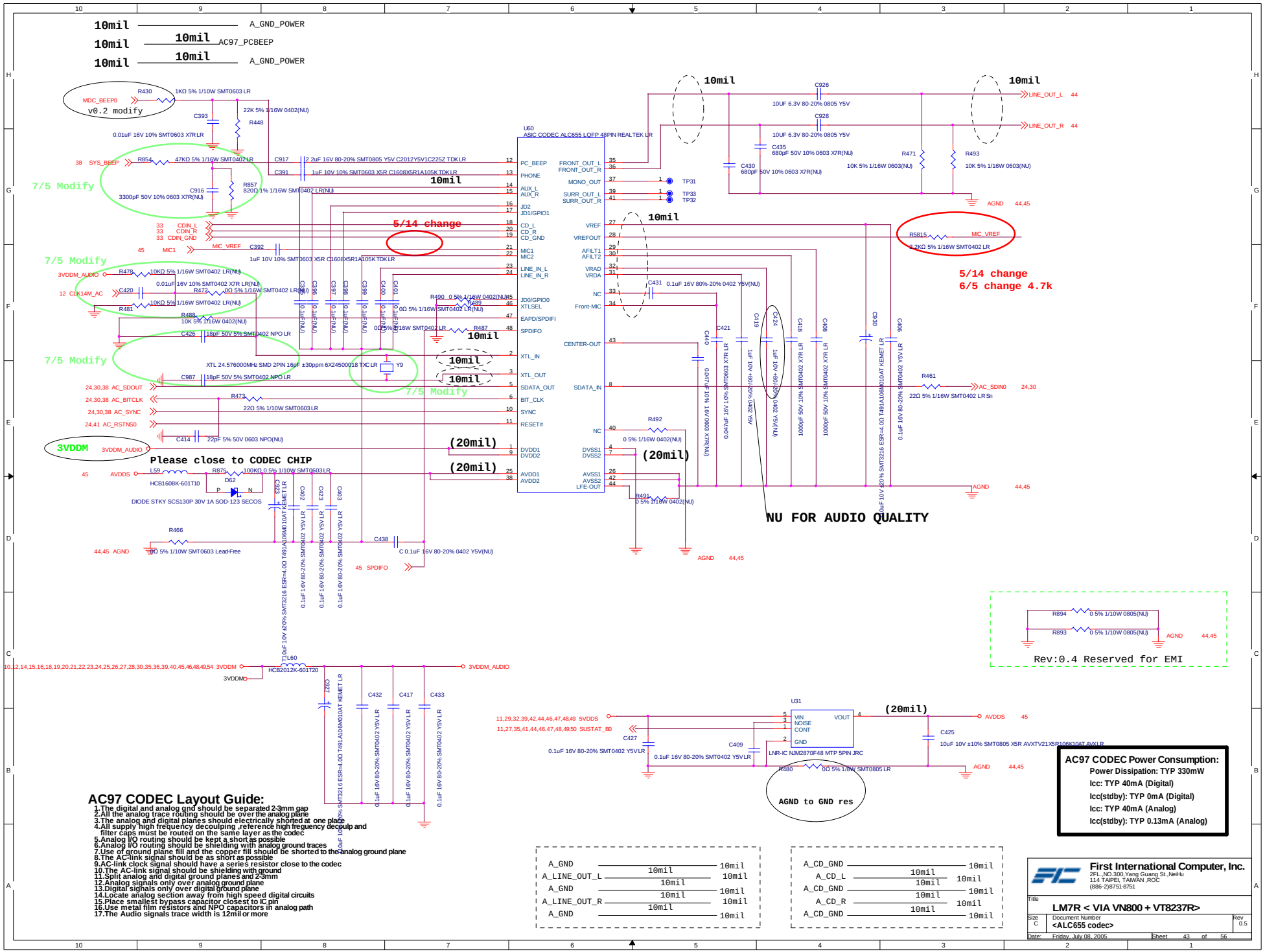


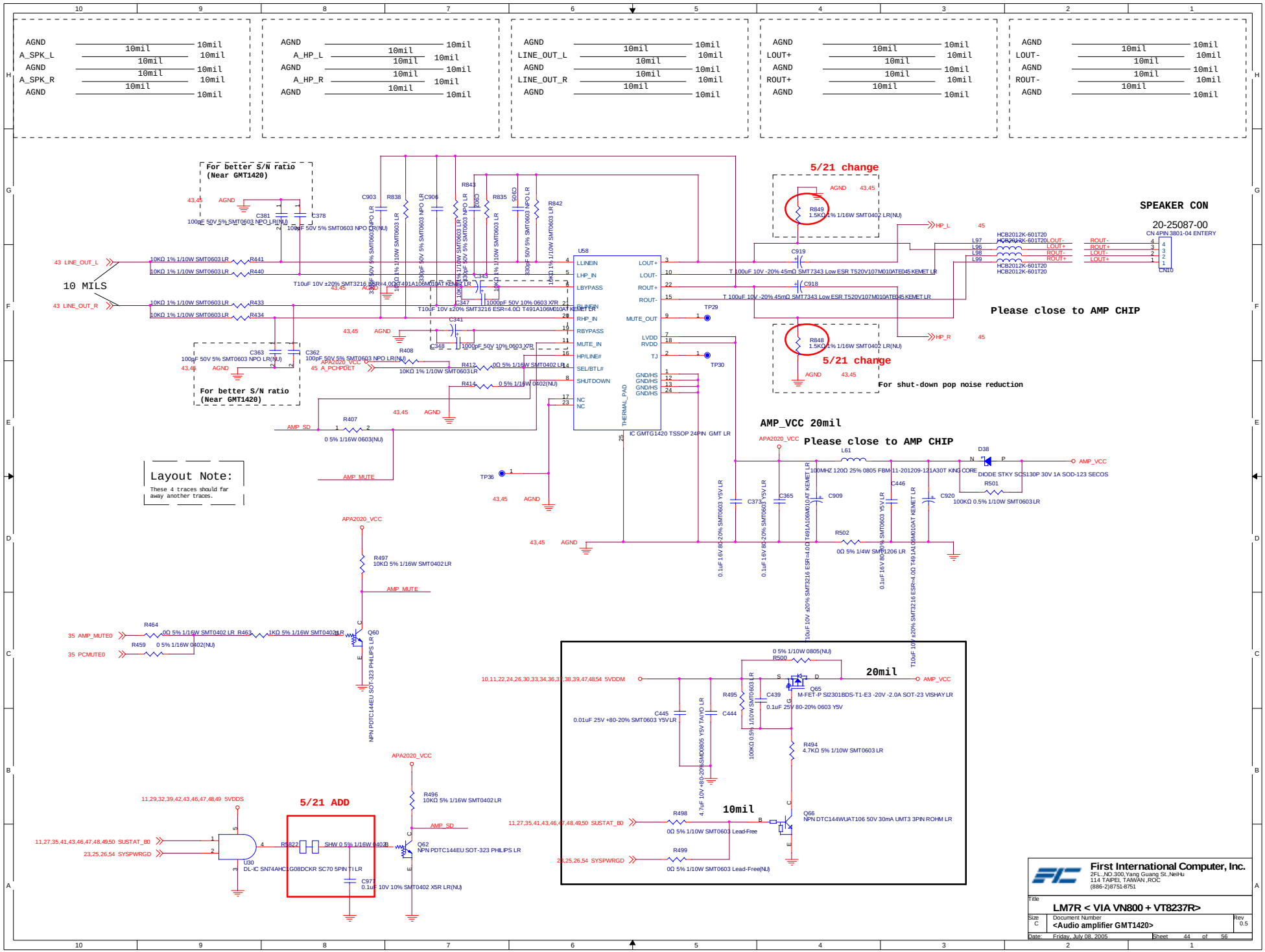
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

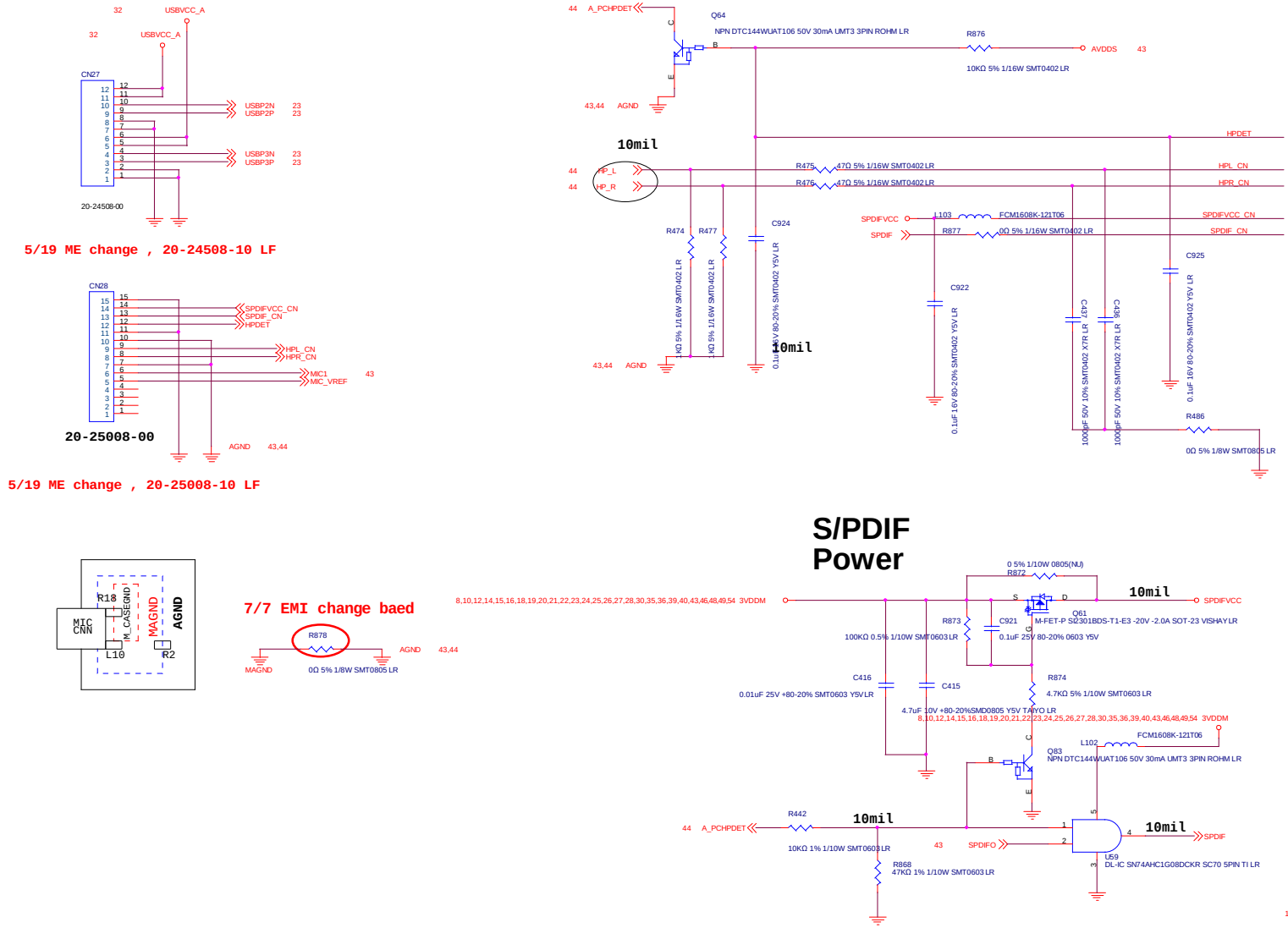
Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <OVP CKT> | Rev: 0.5

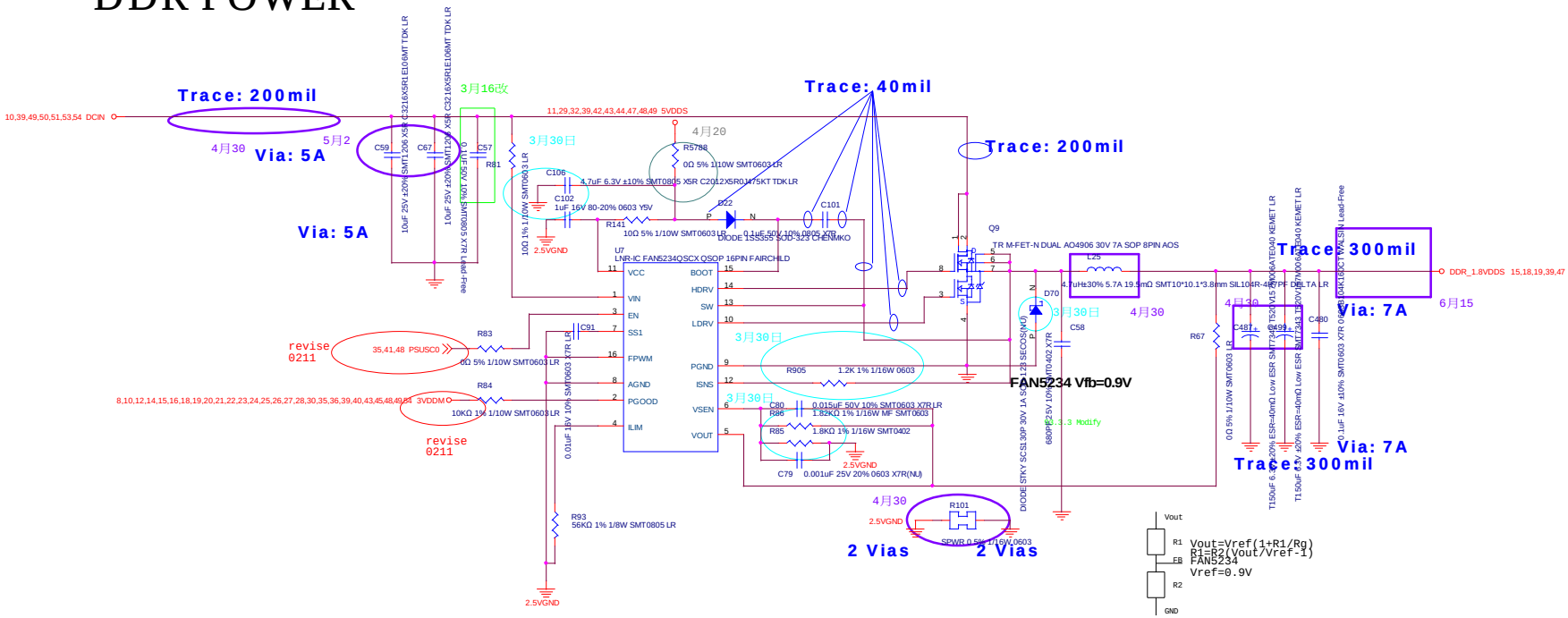
Date: Friday, July 08, 2005 | Sheet 42 of 56

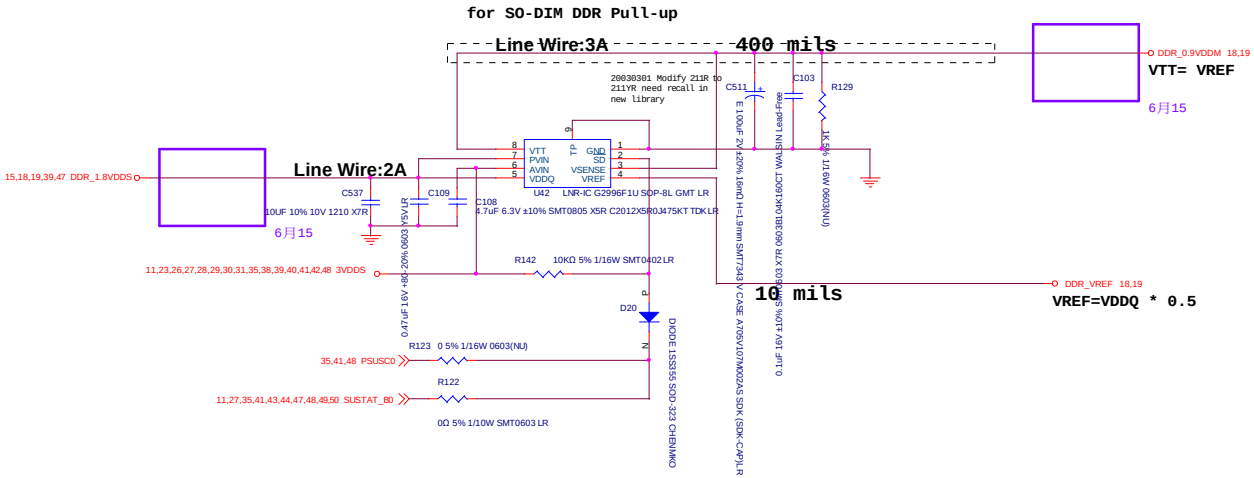






DDR POWER





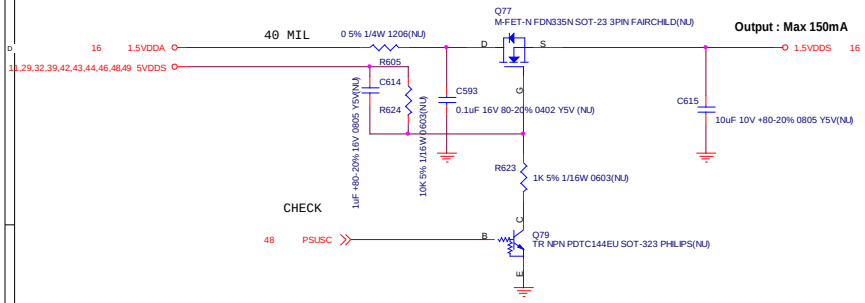
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

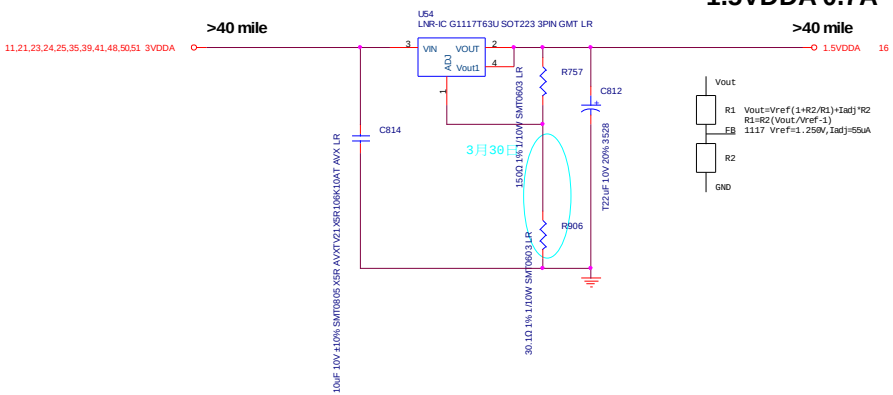
Size: C | Document Number: <DDR2 POWER> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 46 of 56

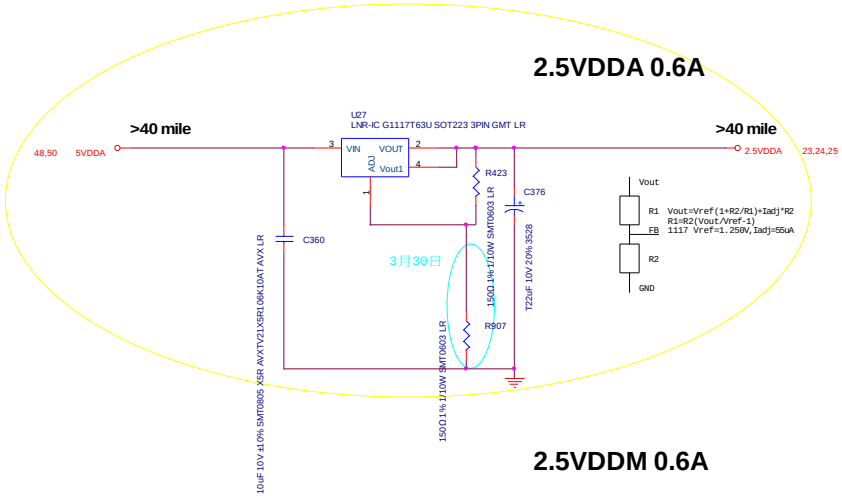
1.5VDDS 0.2A



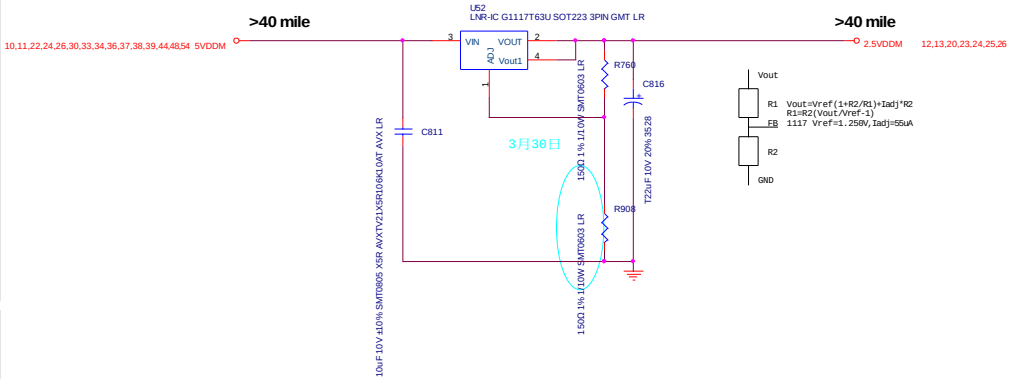
1.5VDDA 0.7A



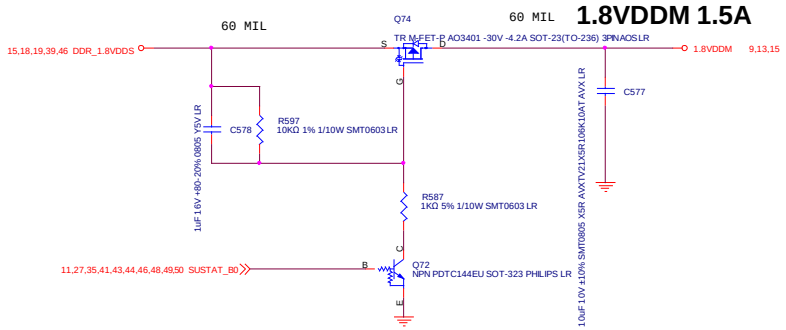
2.5VDDA 0.6A



2.5VDDM 0.6A



1.8VDDM 1.5A



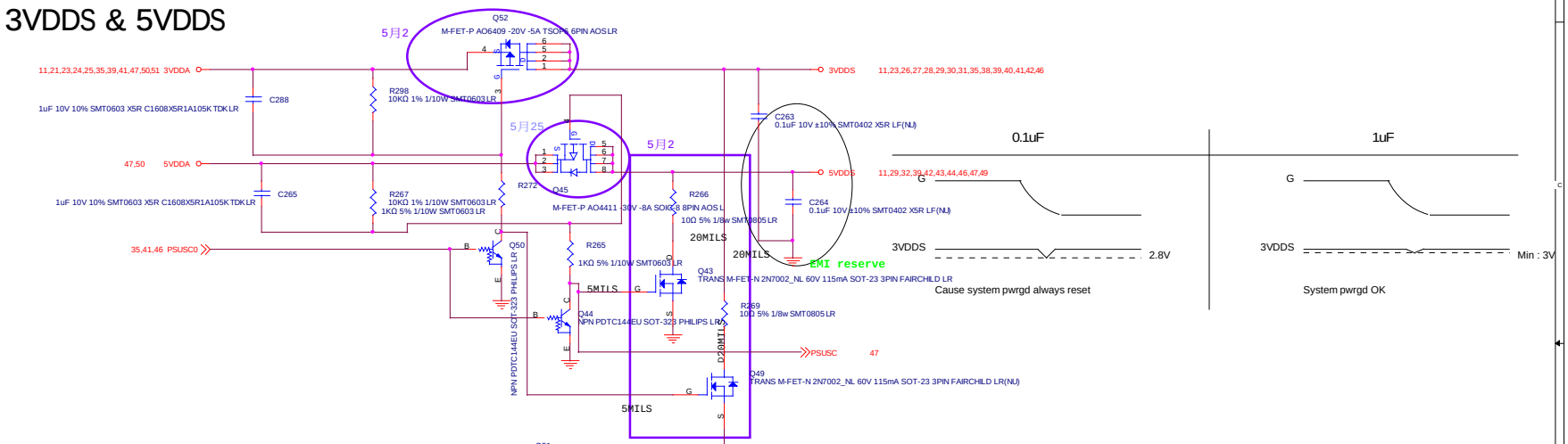
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

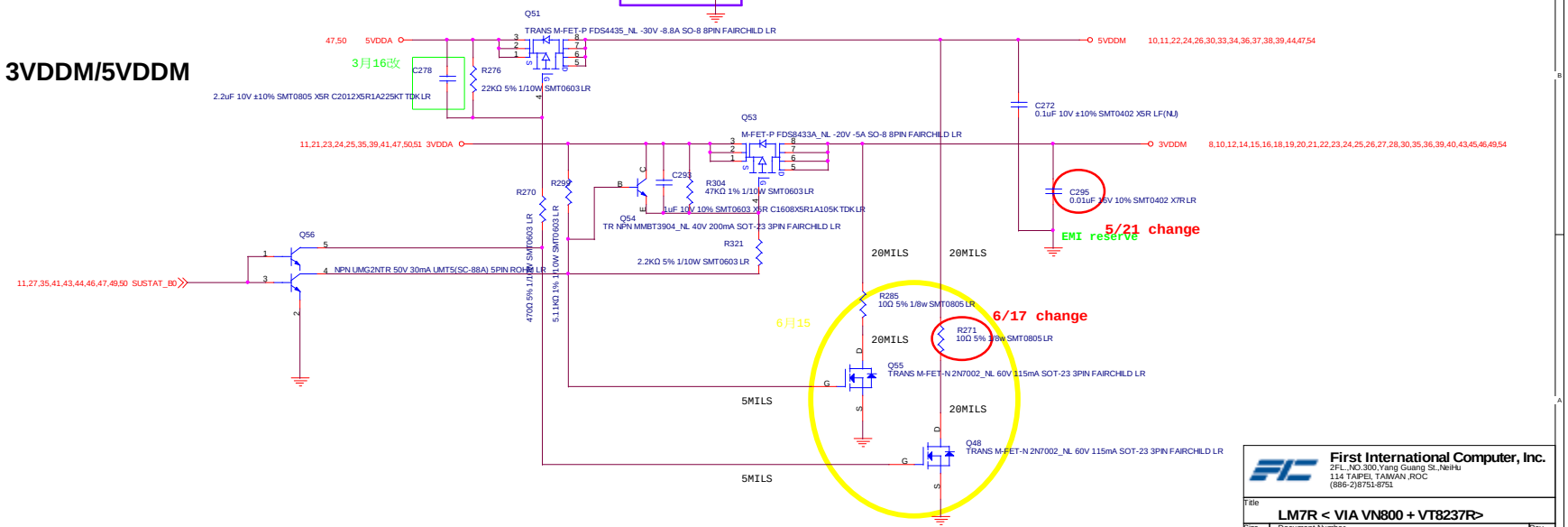
Size: C | Document Number: <1.5V / 2.5V /1.8V> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 47 of 56

3VDDS & 5VDDS



3VDDM/5VDDM



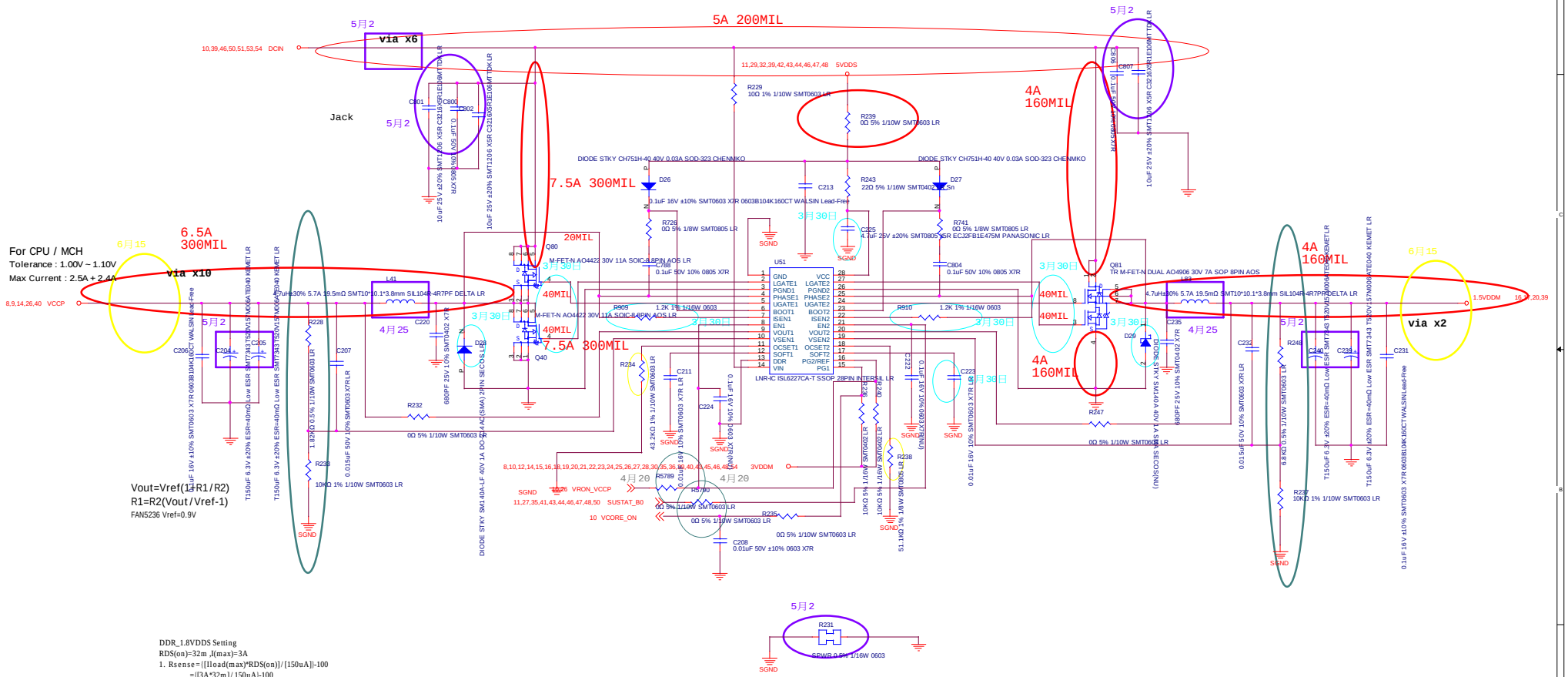
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title: LM7R < VIA VN800 + VT8237R>

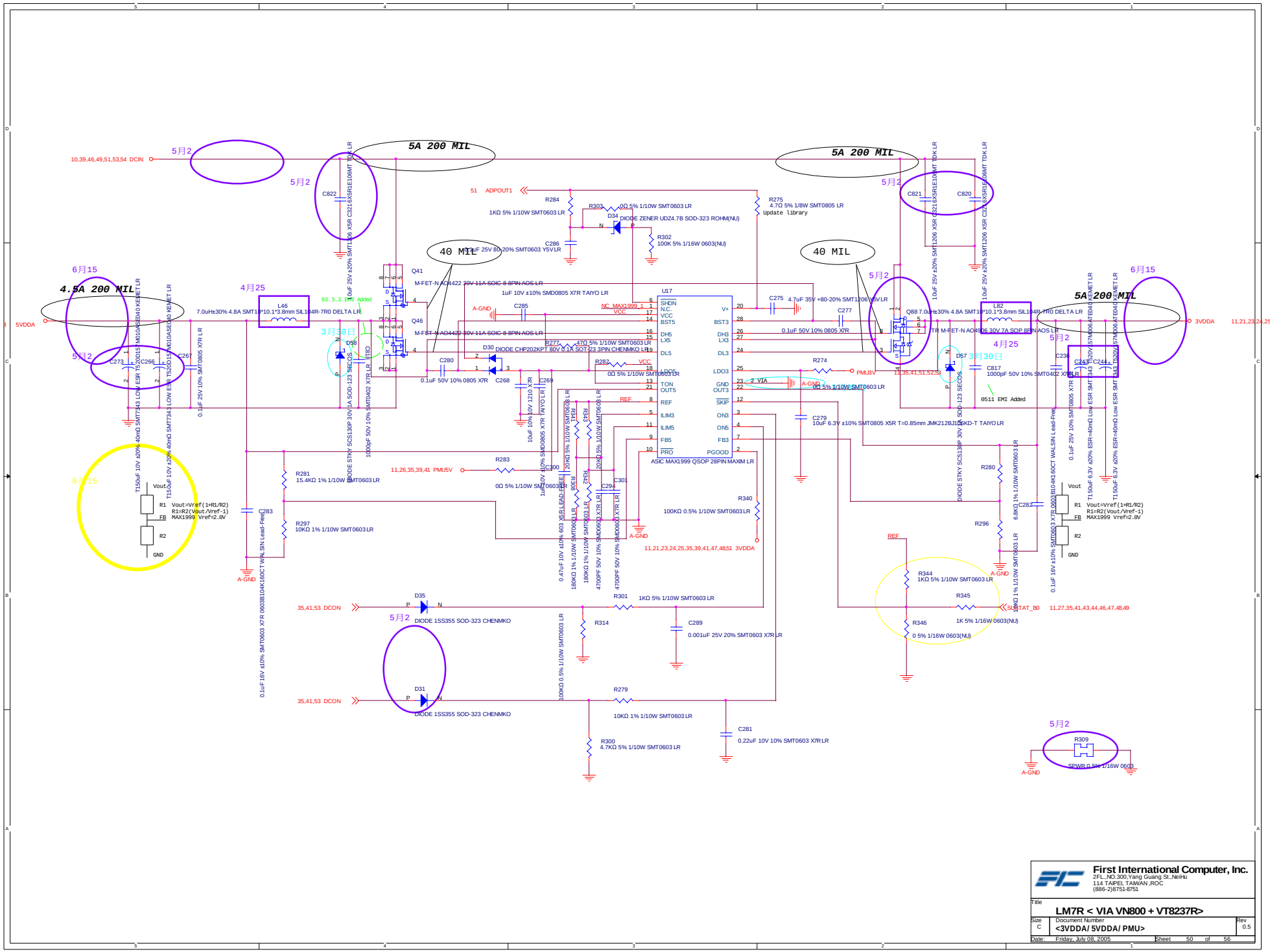
Size: C | Document Number: <POWER 3/5 VDDS/VDDM> | Rev: 0.5

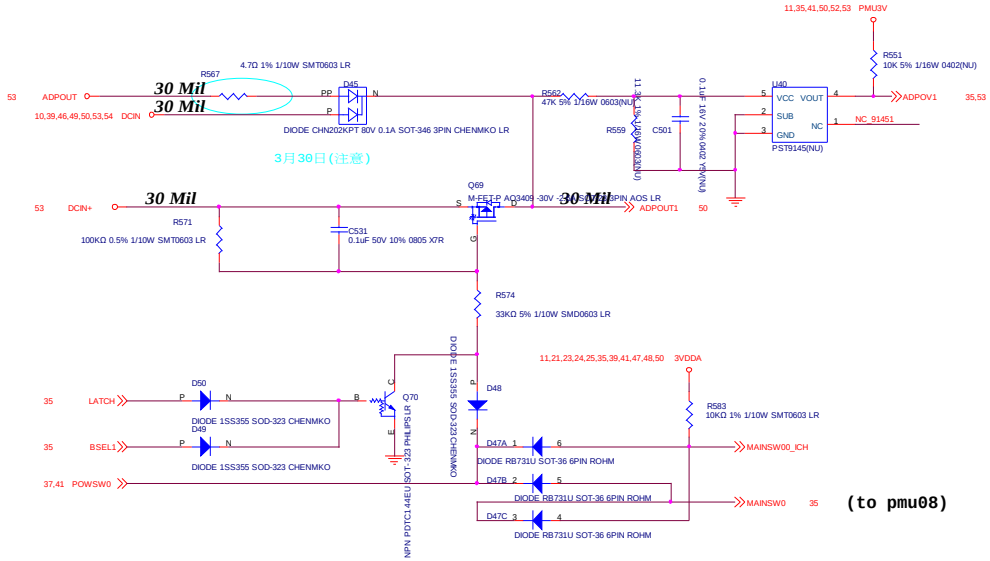
Date: Friday, July 08, 2005 | Sheet 48 of 56

VCCP ,VORE_GMCH

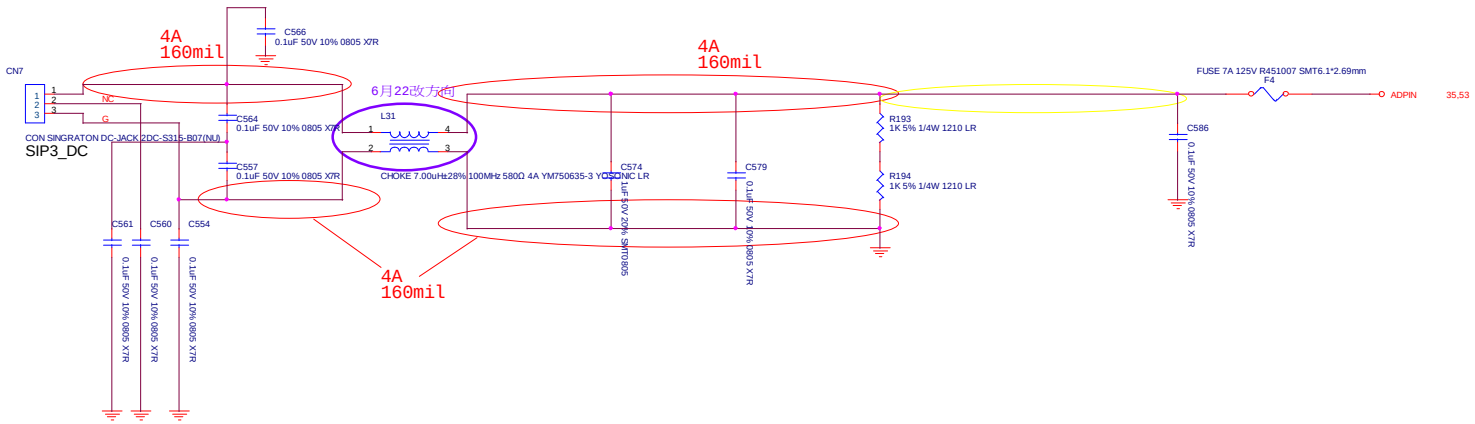


First International Computer, Inc.		
2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751		
Title	LM7R < VIA VN800 + VT8237R>	
Size C	Document Number <VCCP & 1.5VDDM>	Rev 0.5
Date: Friday, July 08, 2005	Sheet 49 of 56	

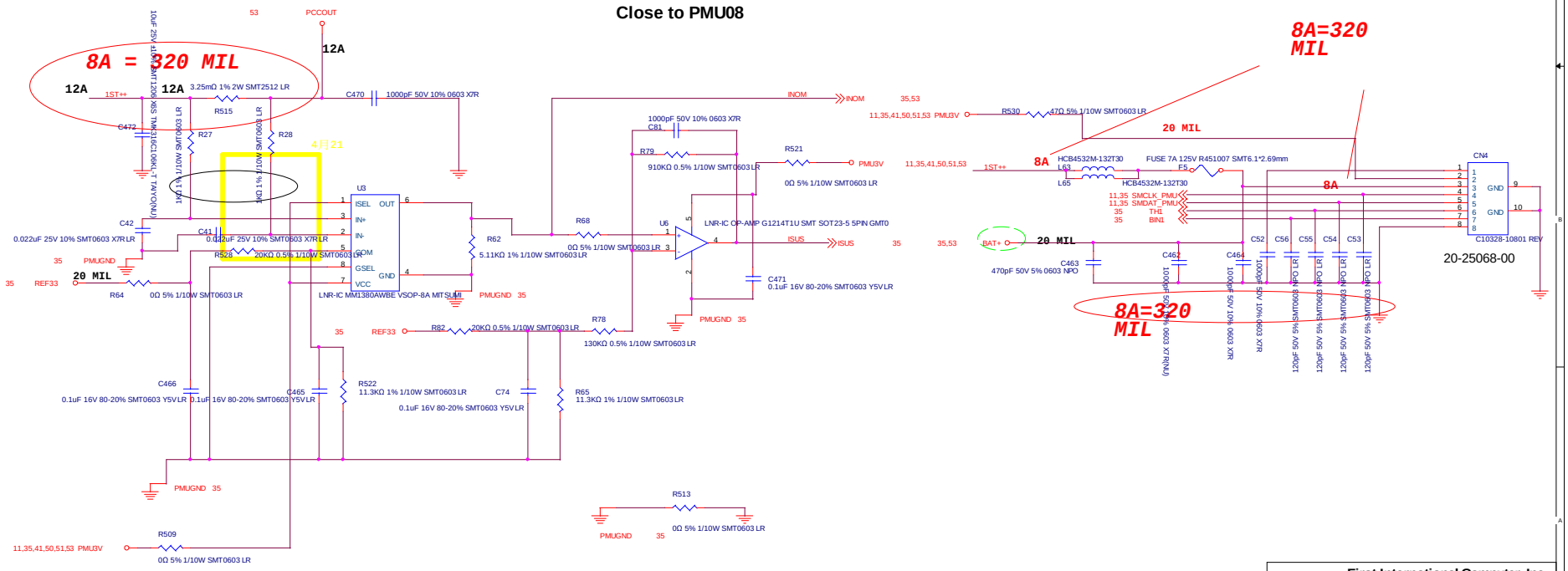




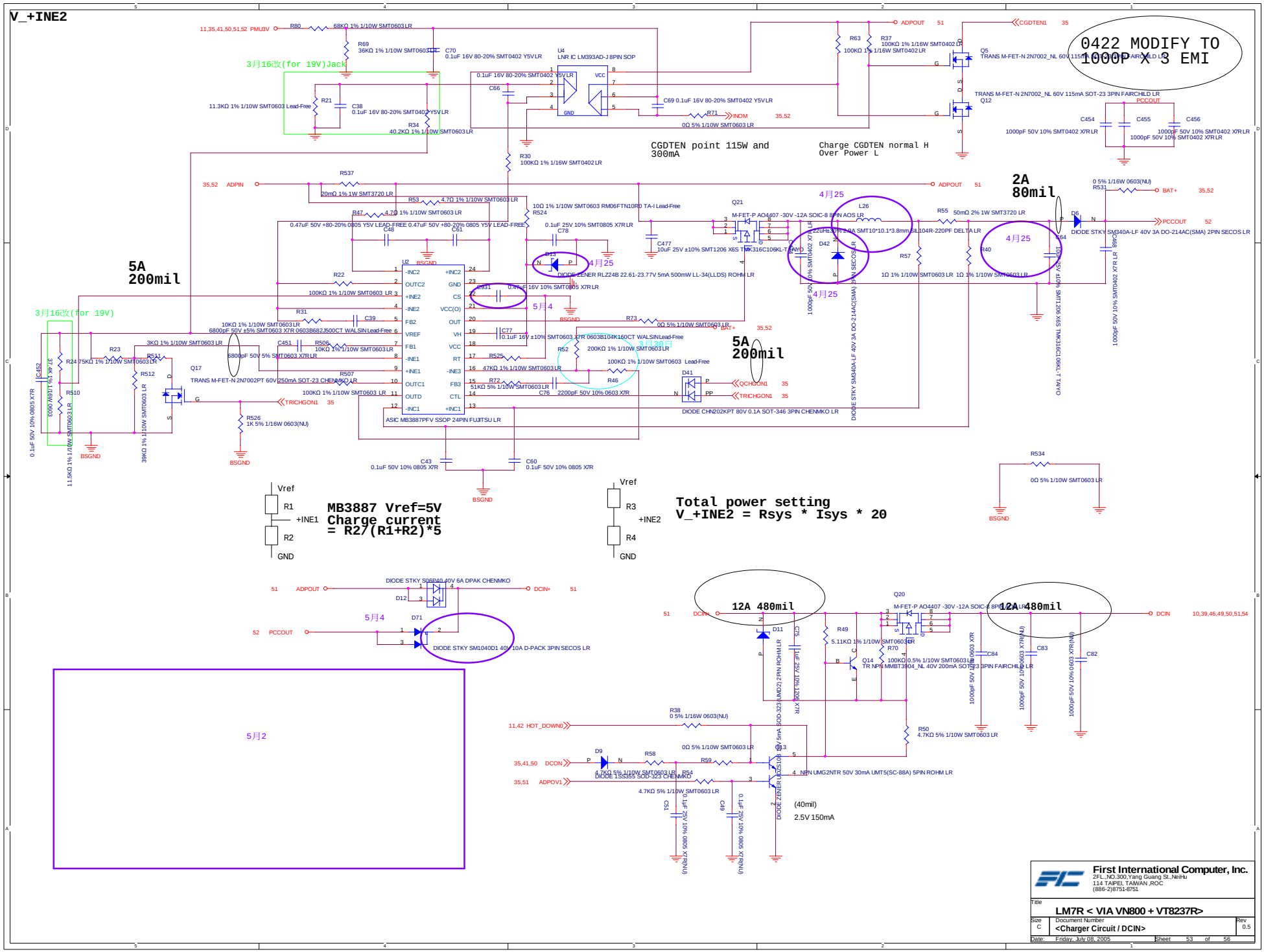
First International Computer, Inc.	2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751
Title	LM7R < VIA VN800 + VT8237R>
Size C	Document Number <power-on switch control> Rev 0.5
Date: Friday, July 08, 2005	Sheet 51 of 56



CHR BATTERY IN

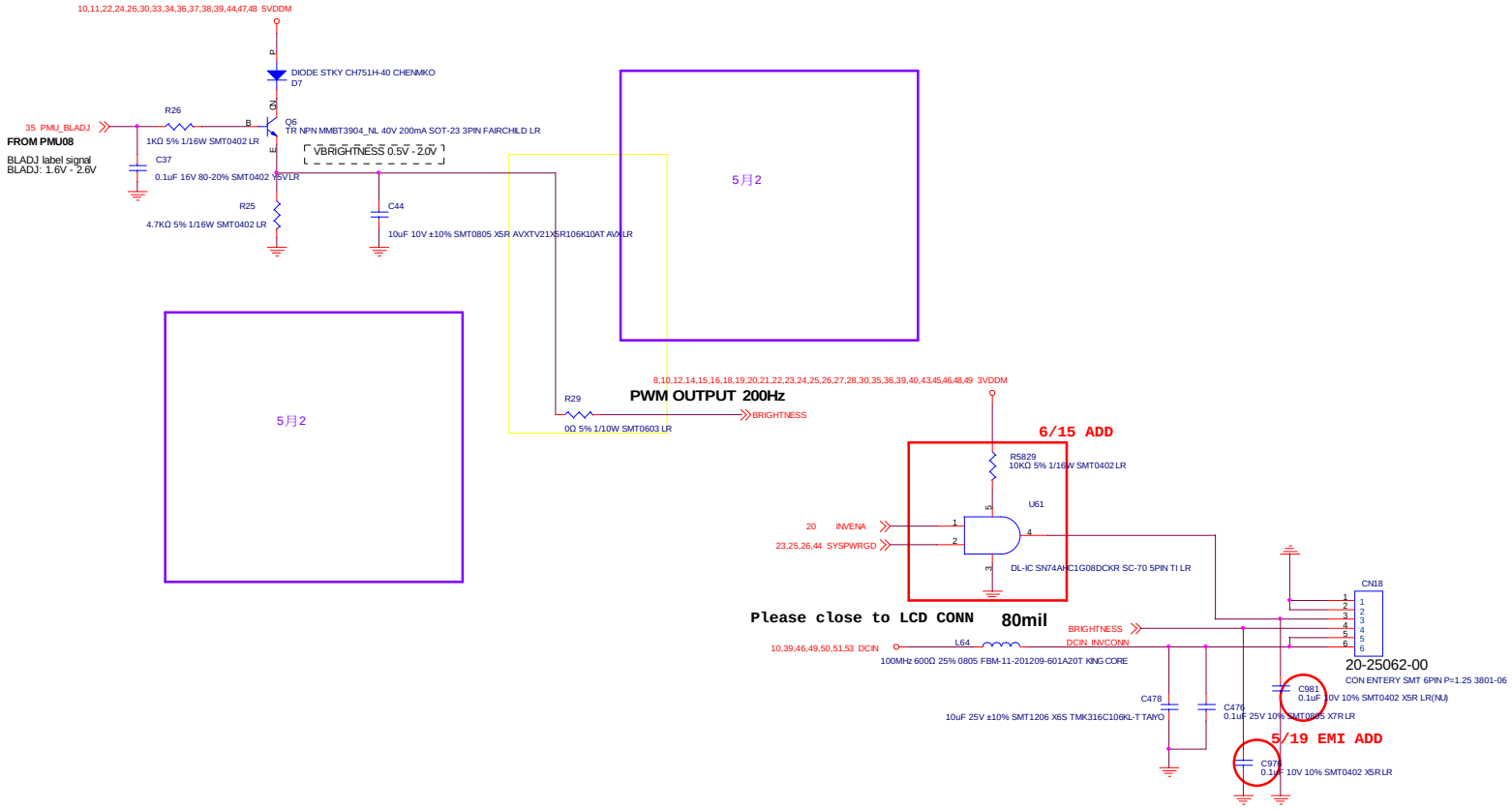


First International Computer, Inc.		
2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751		
Title	LM7R < VIA VN800 + VT8237R>	
Size: C	Document Number: <AC-IN / Battery CNN>	Rev: 0.5
Date: Friday, July 08, 2005	Sheet 52 of 56	



Inverter Control

LCD brightness control



First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

Title	LM7R < VIA VN800 + VT8237R>	
Size: C	Document Number: <Inverter>	Rev: 0.5
Date: Friday, July 08, 2005	Sheet 54 of 56