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G43M01_uATX (Version: 0A)

CPU: Intel Conroe, Wolfdale, Yorkfield processors in LGA775 Package.

System Chipset:

North Bridge ... G43
South Bridge ... ICH10R

Main Memory:

Dual Channel / DDR-II * 2 (Maximum to 8GB)

On Board Device:

Clock Generator ... ICS9LPRS919HKLF-T
Super I/O ... IT8720F
HDA Codec ... ALC888S
BIOS ... SPI Flash ROM

Expansion Slots:

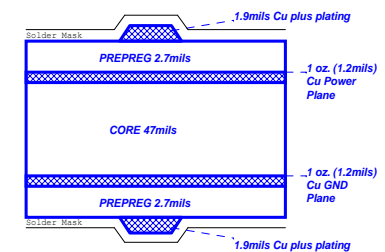
PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT * 1
PCI SLOT * 2

PWM Controller:

Controller ...ISL6334 (3Phase)

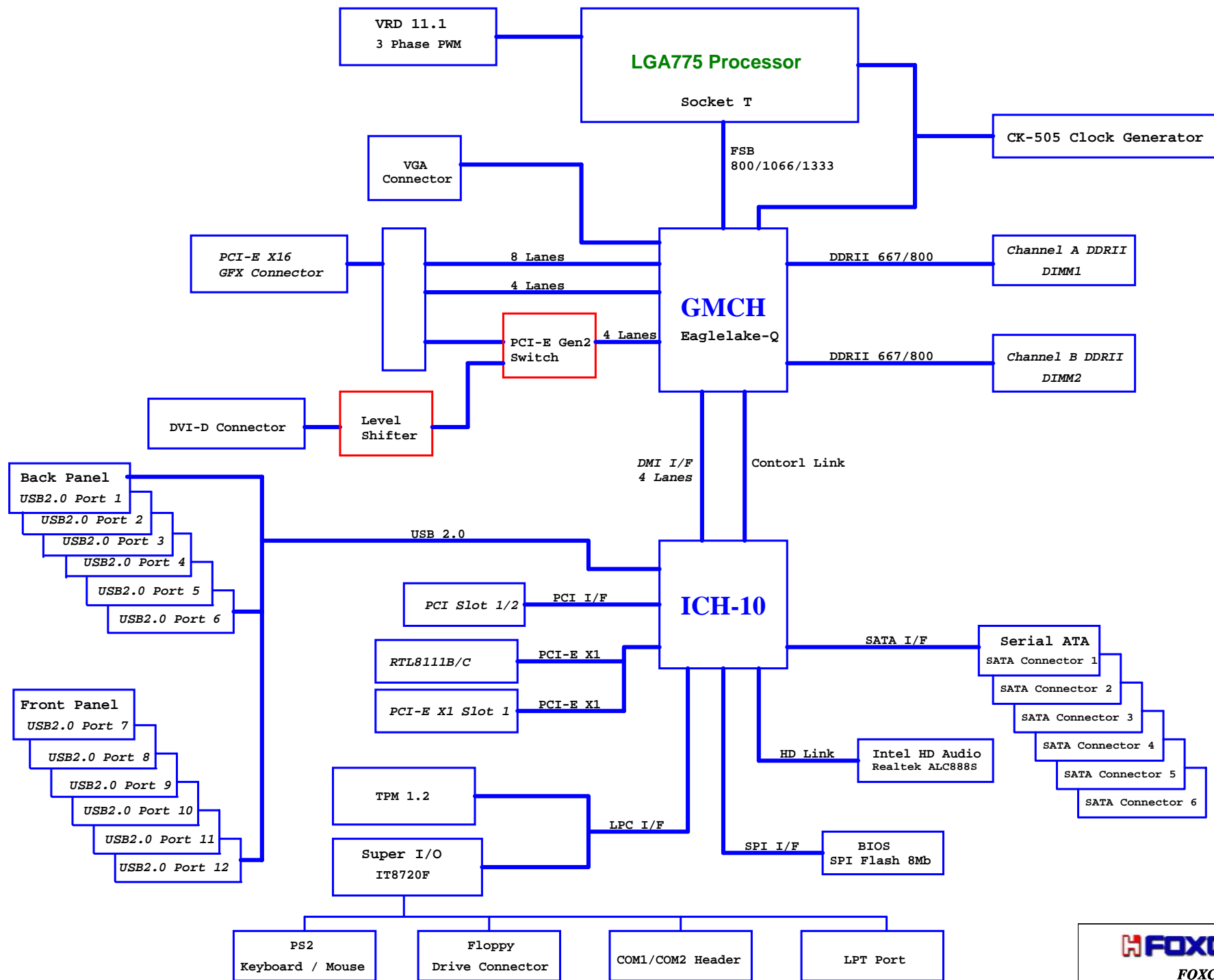
Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
DMI - 95ohm : 15/4/8/4/15

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FOXCONN PCEG		
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14.318MHz

CPU

CPU 200/266/333 MHz Diff Pair

MCH 200/266/333 MHz Diff Pair

PCI Express 100 MHz Diff Pair

PCI Express x16 Gfx

DOT 96 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

USB/SIO 48 MHz

ICH 33 MHz

REF 14 MHz

PCI 33 MHz

PCI Slot 1
PCI Slot 2

TPM 33 MHz

TPM 1.2

SIO 33 MHz

SATA 100 MHz Diff Pair

PCI Express 100 Mhz Diff Pair

GMCH
Eaglelake

DDR II 2 Slots 6 Diff CLKs

Channel A DDR II
DIMM1

DDR II 667/800

Channel B DDR II
DIMM2

DDR II 667/800

CK-505

PCI Express 100 Mhz Diff Pair

PCI Express x1 Slot 1

RTL8111B/C

32.768KHz

Azalia Bit Clock

HD Audio

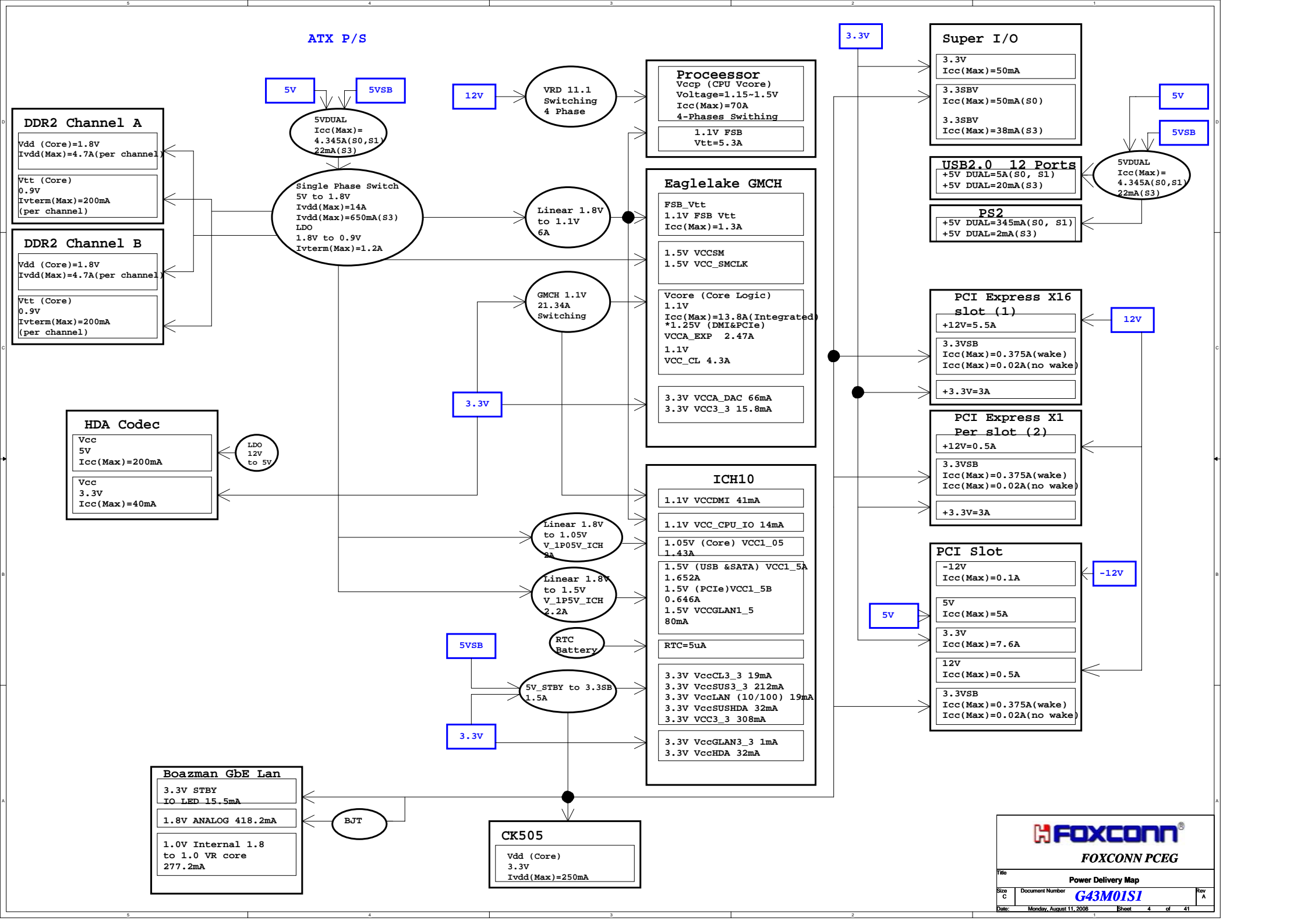
Super I/O



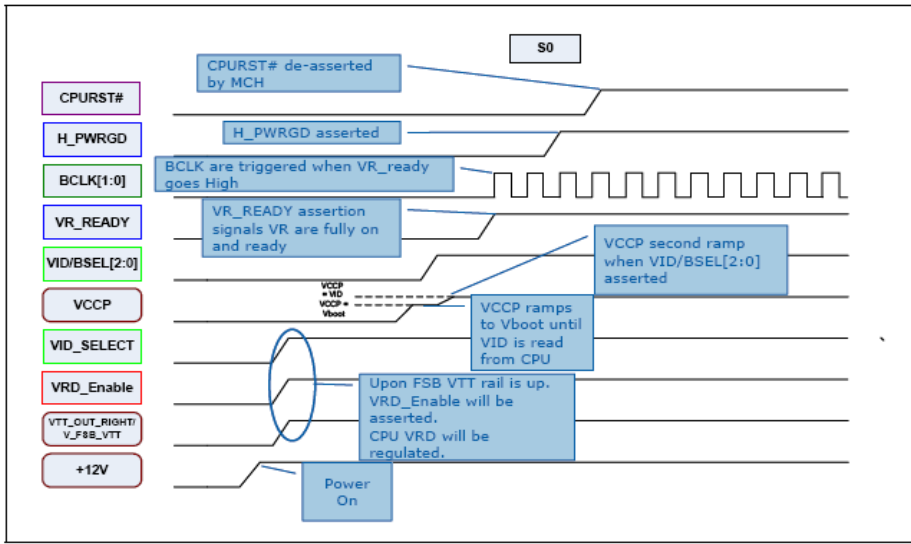
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Title		
Clock Distribution		
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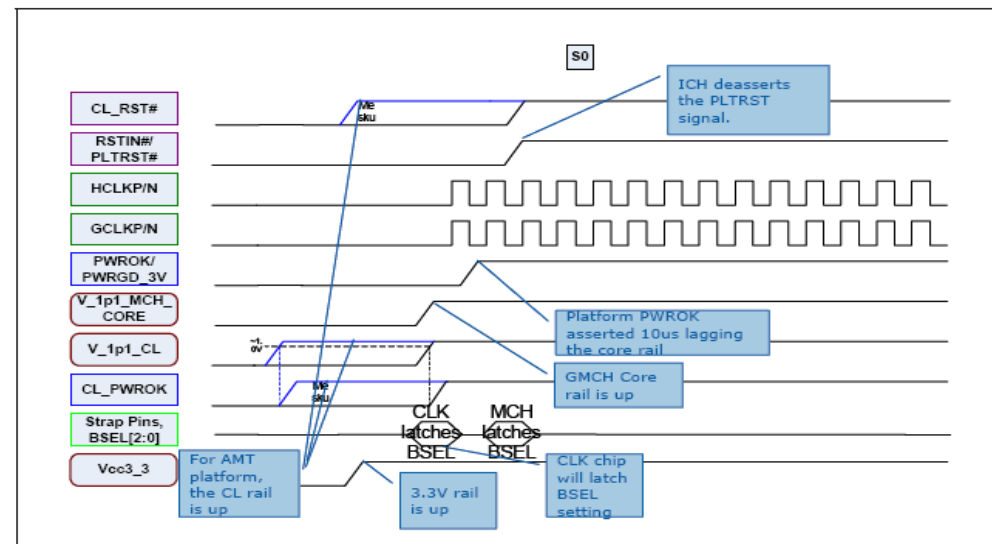
ATX P/S



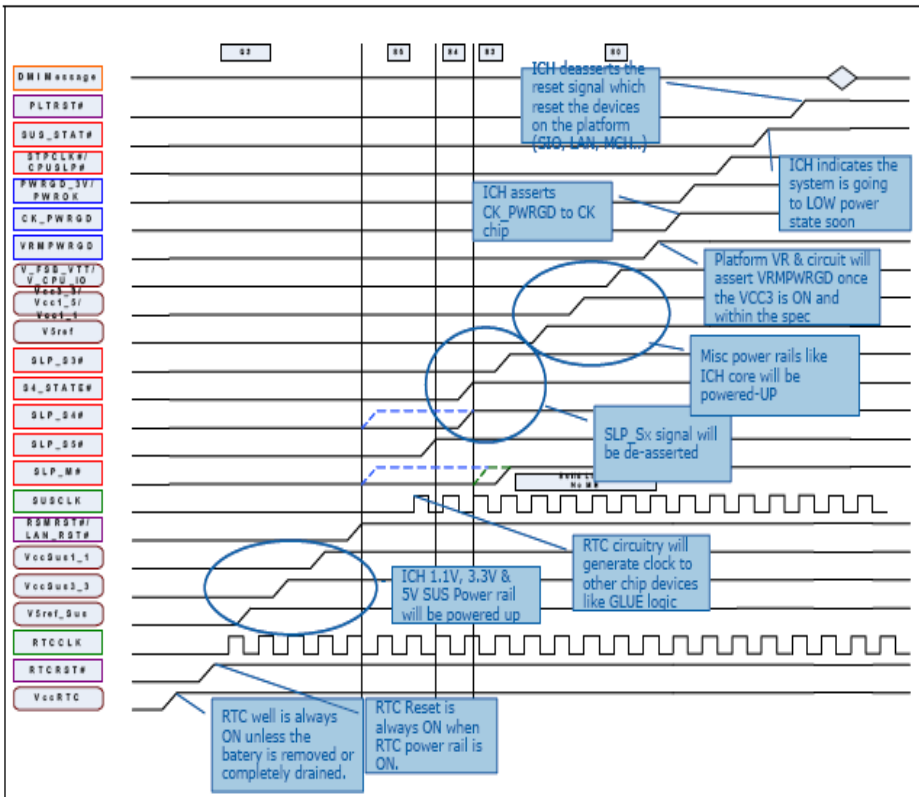
Intel® Eaglelake Platform Sequencing:- CPU VR Sequencing Diagram



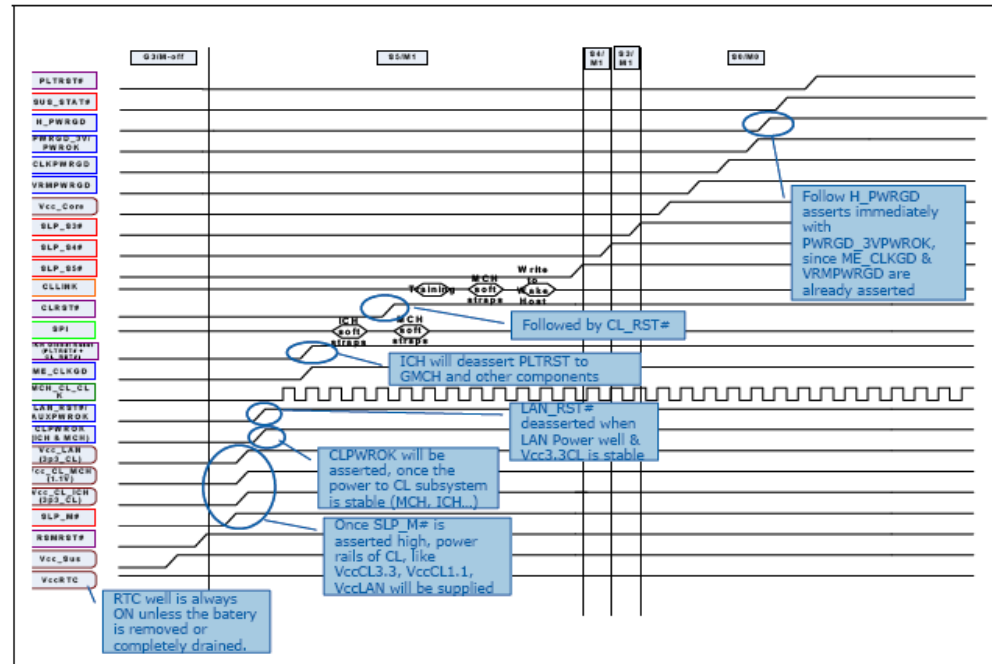
Intel® Eaglelake Platform Sequencing:- GMCH Sequencing Diagram



Intel® Eaglelake Platform Sequencing:- ICH10 Sequencing Diagram



ME Platform Sequencing Diagram

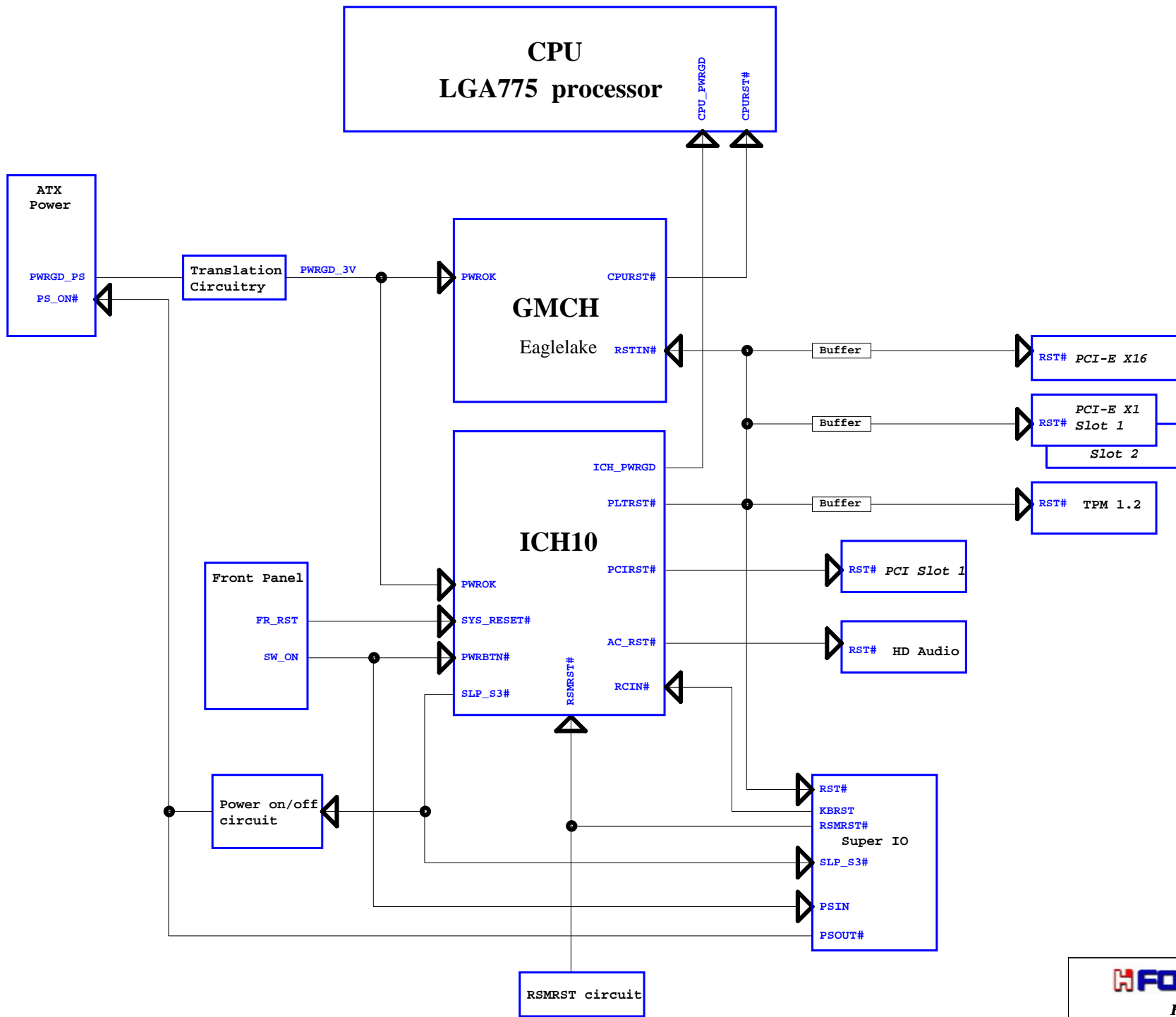


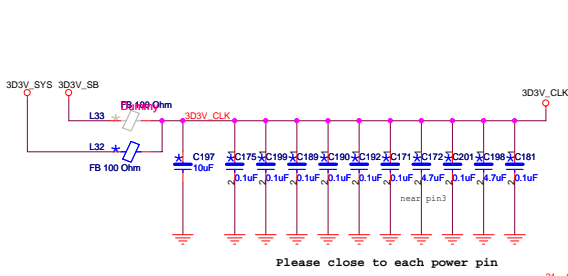
FOXCONN
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Title: Platform Sequence

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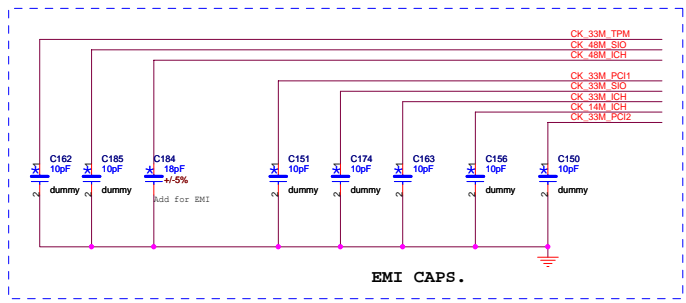
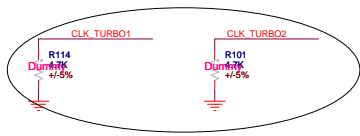
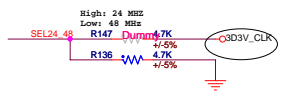


SEL_STOP: latched input to select pin functionality
 1 = Selects pin 41/42 to be PCI_STOP#/CPU_STOP#
 0 = Selects pin 41/42 to be PCIeX outputs

check value???

PCI-E x1 (Slot1)
 PCI-E Micron 368

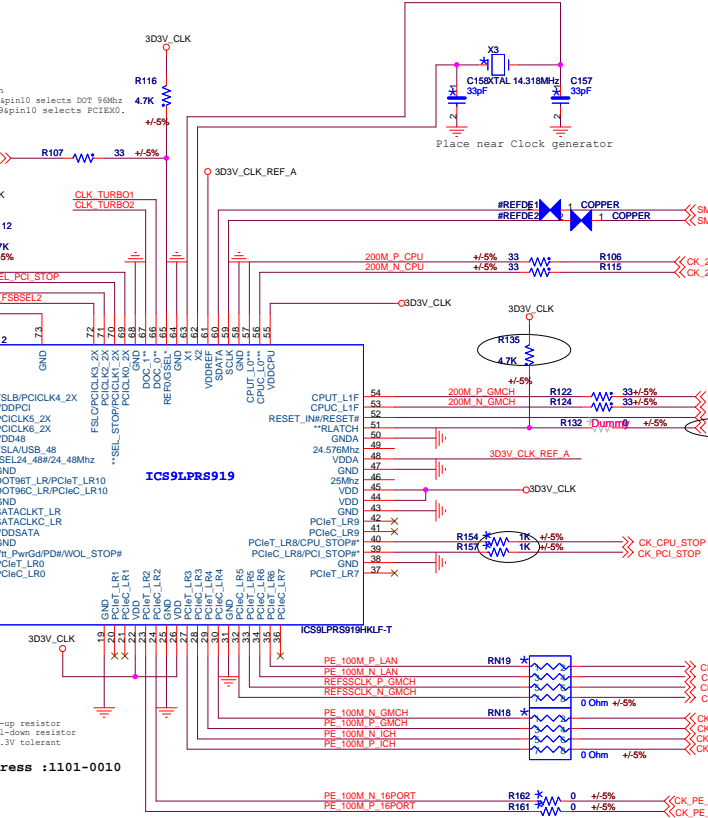
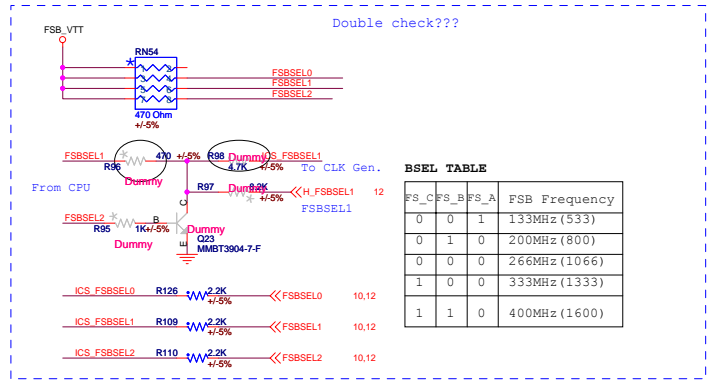
PCI-E x16 Slot



*Internal pull-up resistors
 *Internal pull-down resistor
 RESET pin is 3.3V tolerant

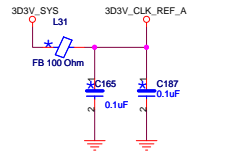
SMBus Address :1101-0010

Double check???

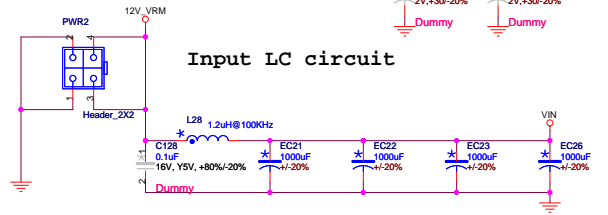
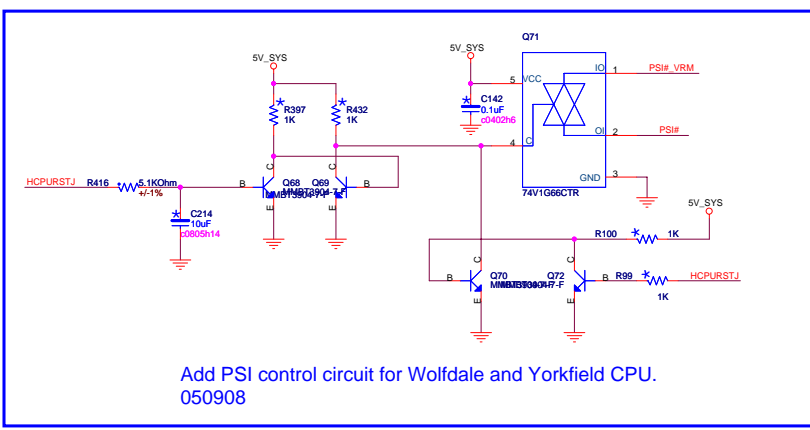
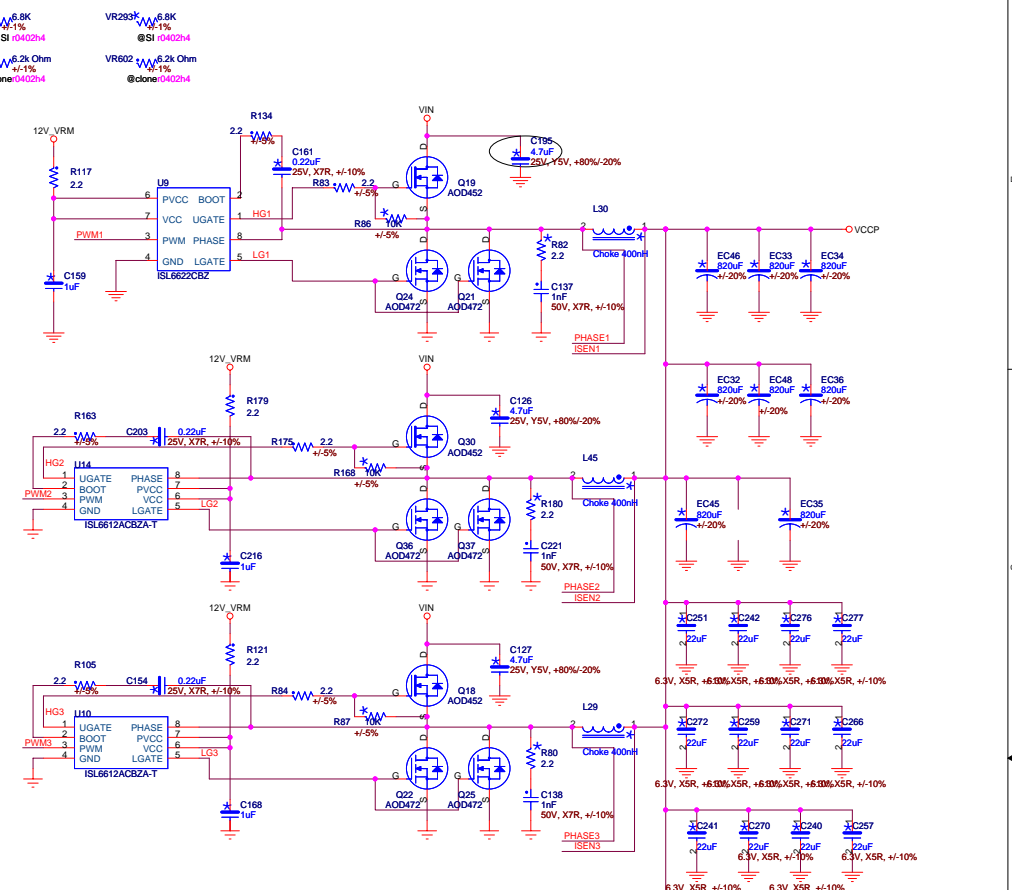
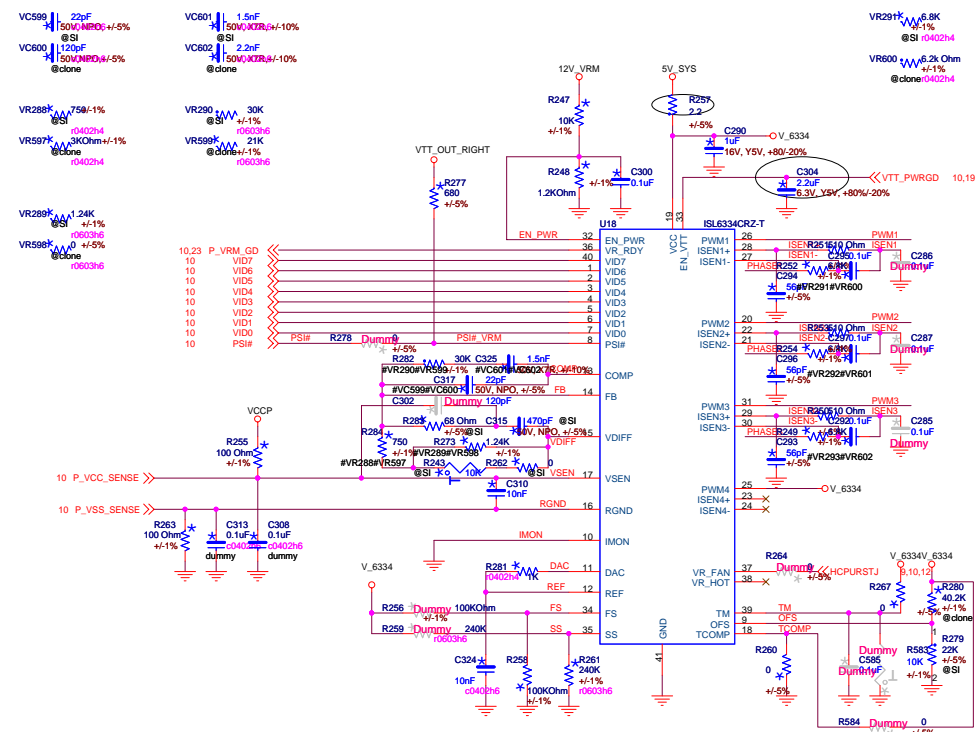


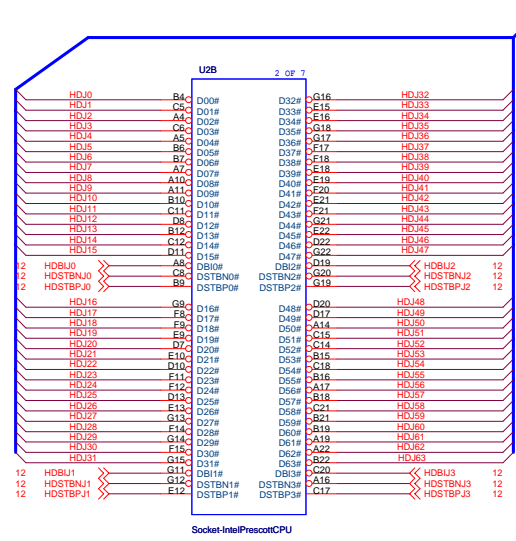
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 #REFDE2 COPPER

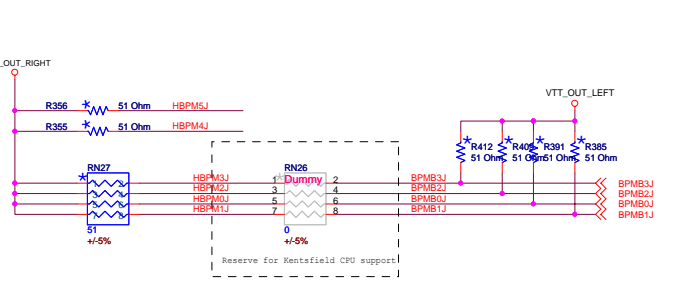
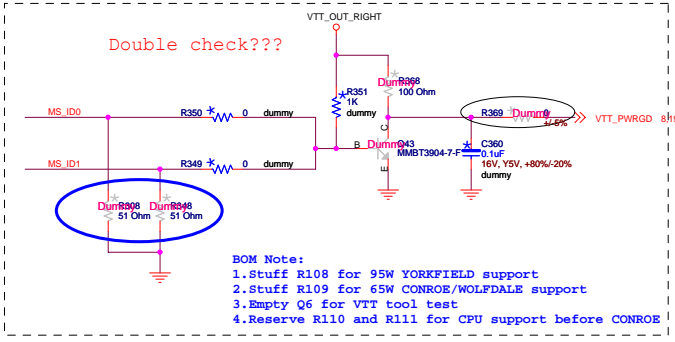
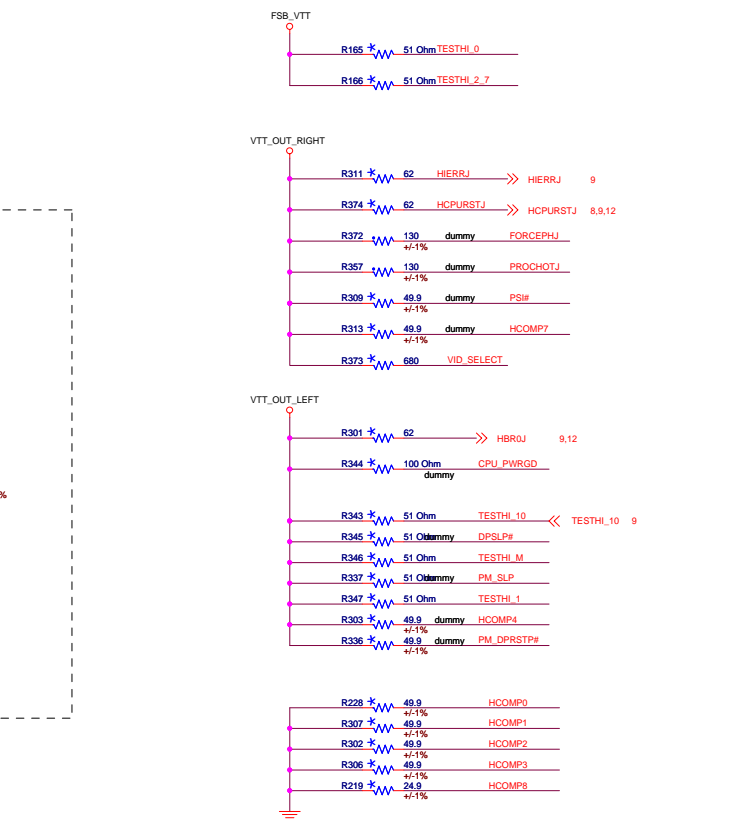
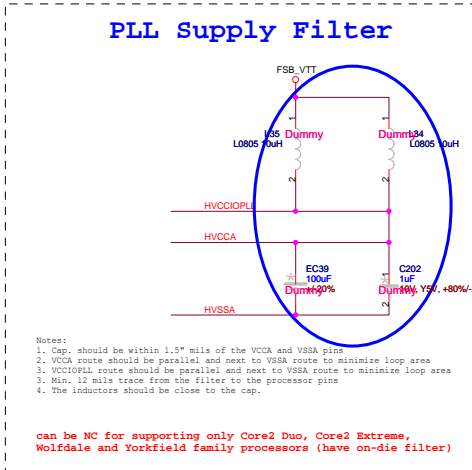
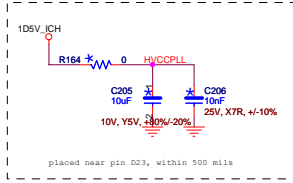
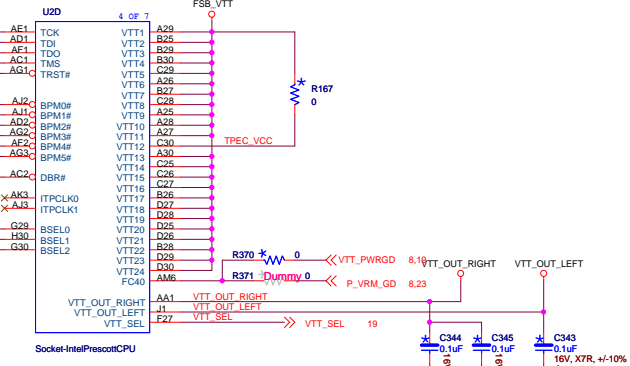
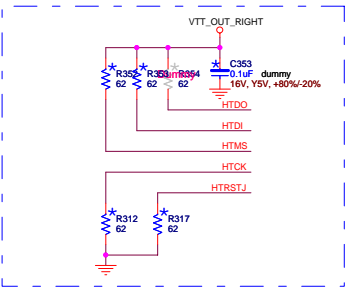
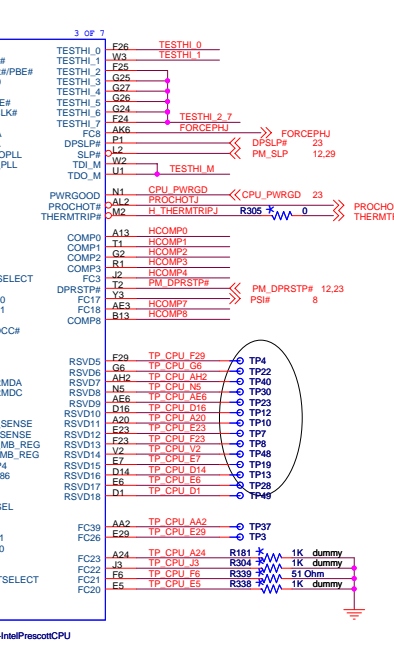
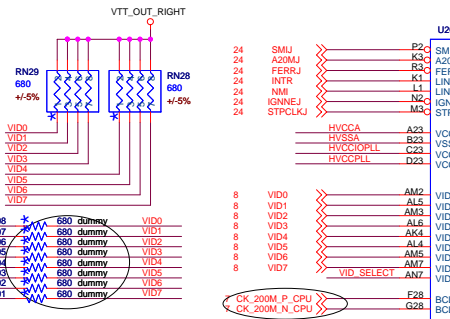
Close to pin 48, 61



FOXCONN PCEG







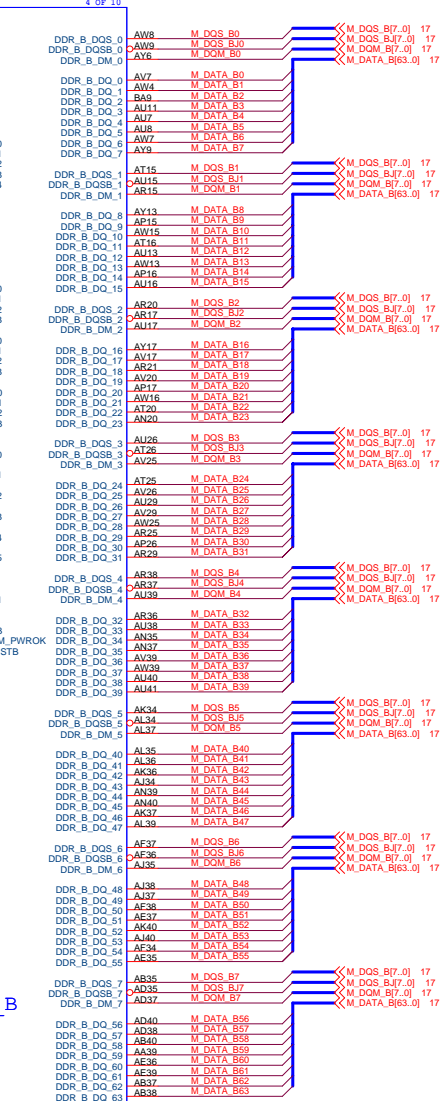
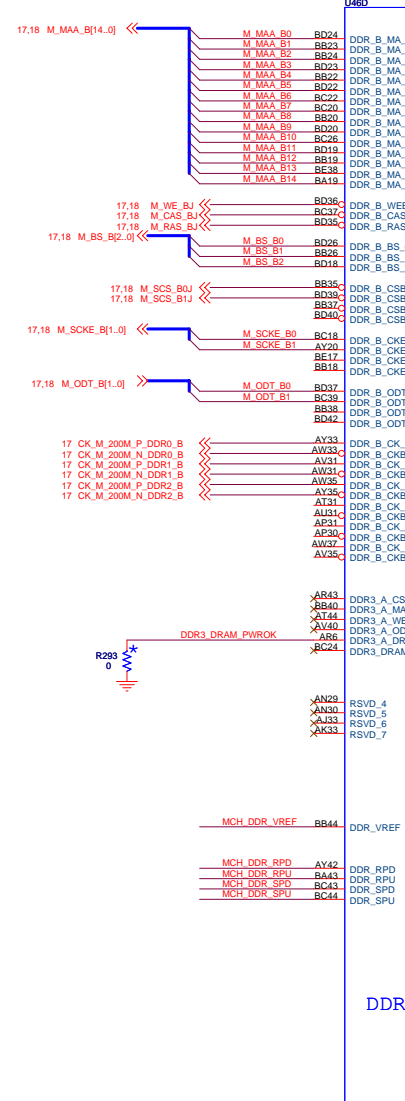
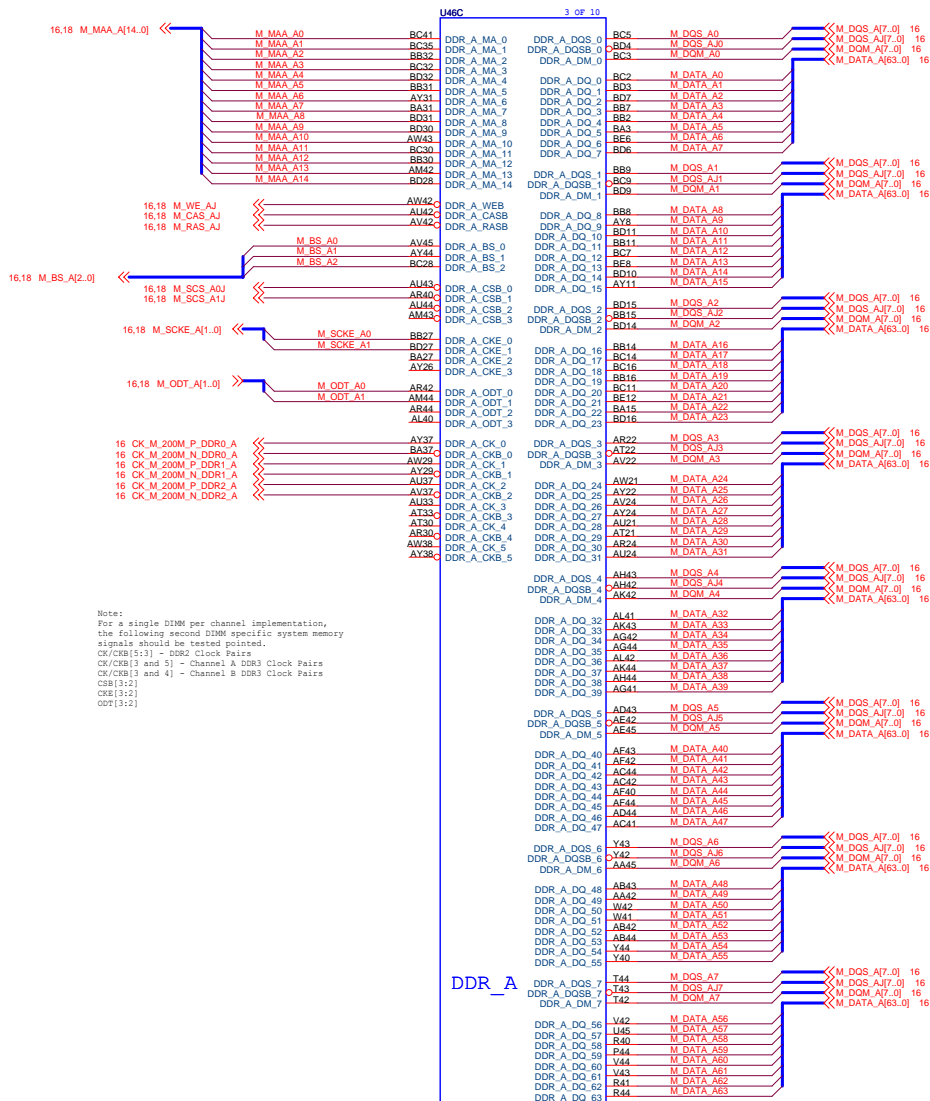
VCCP		UZE		3 OF 7		VCCP	
AG22	VCCP1	VCCP93	AK12				
K29	VCCP2	VCCP94	AF22				
AM26	VCCP3	VCCP95	T29				
AE12	VCCP5	VCCP96	AM14				
VCCP6	VCCP97	VCCP97	AM25				
AE11	VCCP98	VCCP98	AH19				
W23	VCCP99	VCCP99	AE9				
W24	VCCP100	VCCP100	AH29				
W25	VCCP101	VCCP101	AH27				
T25	VCCP102	VCCP102	AG28				
W28	VCCP103	VCCP103	VCCP191	VSS47			
AL18	VCCP104	VCCP104	AG28	VSS48			
AC25	VCCP105	VCCP105	AL26	VSS49			
W30	VCCP106	VCCP106	AM12	VCCP192	VSS50		
V30	VCCP107	VCCP107	T28	VCCP193	VSS51		
AN14	VCCP108	VCCP108	W28	VCCP194	VSS52		
AD28	VCCP109	VCCP109	J25	VCCP195	VSS53		
V26	VCCP110	VCCP110	J27	VCCP196	VSS54		
AC29	VCCP111	VCCP111	AG19	VCCP197	VSS55		
VCCP18	VCCP112	VCCP112	AL9	VCCP198	VSS56		
VCCP19	VCCP113	VCCP113	AG25	VCCP199	VSS57		
VCCP20	VCCP114	VCCP114	AF21	VCCP200	VSS58		
AC27	VCCP115	VCCP115	AK14	VCCP201	VSS59		
J23	VCCP116	VCCP116	AD30	VCCP202	VSS60		
U24	VCCP117	VCCP117	AF21	VCCP203	VSS61		
AM18	VCCP118	VCCP118	AH30	VCCP204	VSS62		
AM19	VCCP119	VCCP119	AK14	VCCP205	VSS63		
AB8	VCCP120	VCCP120	J9	VCCP206	VSS64		
AC26	VCCP121	VCCP121	M27	VCCP207	VSS65		
J8	VCCP122	VCCP122	AF14	VCCP208	VSS66		
T28	VCCP123	VCCP123	J30	VCCP209	VSS67		
T30	VCCP124	VCCP124	AG18	VCCP210	VSS68		
AM9	VCCP125	VCCP125	W27	VCCP211	VSS69		
AF15	VCCP126	VCCP126	AG8	VCCP212	VSS70		
AC8	VCCP127	VCCP127	AN8	VCCP213	VSS71		
AE14	VCCP128	VCCP128	AH14	VCCP214	VSS72		
W29	VCCP129	VCCP129	AD29	VCCP215	VSS73		
U29	VCCP130	VCCP130	W8	VCCP216	VSS74		
AC24	VCCP131	VCCP131	AH8	VCCP217	VSS75		
AC23	VCCP132	VCCP132	N24	VCCP218	VSS76		
AN26	VCCP133	VCCP133	AN22	VCCP219	VSS77		
AN25	VCCP134	VCCP134	J14	VCCP220	VSS78		
AN11	VCCP135	VCCP135	AK11	VCCP221	VSS79		
AN18	VCCP136	VCCP136	AF19	VCCP222	VSS80		
Y27	VCCP137	VCCP137	N8	VCCP223	VSS81		
AD24	VCCP138	VCCP138	AF12	VCCP224	VSS82		
AE23	VCCP139	VCCP139	M28	VCCP225	VSS83		
AE22	VCCP140	VCCP140	AK9	VCCP226	VSS84		
AN19	VCCP141	VCCP141					
V8	VCCP142	VCCP142					
AE21	VCCP143	VCCP143					
AM30	VCCP144	VCCP144					
AE19	VCCP145	VCCP145					
AC30	VCCP146	VCCP146					
AE15	VCCP147	VCCP147					
N30	VCCP148	VCCP148					
K27	VCCP149	VCCP149					
M24	VCCP150	VCCP150					
AN21	VCCP151	VCCP151					
T8	VCCP152	VCCP152					
AC28	VCCP153	VCCP153					
N25	VCCP154	VCCP154					
AE18	VCCP155	VCCP155					
W26	VCCP156	VCCP156					
AD26	VCCP157	VCCP157					
M8	VCCP158	VCCP158					
AD26	VCCP159	VCCP159					
AJ26	VCCP160	VCCP160					
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U25	VCCP165	VCCP165					
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M23	VCCP169	VCCP169					
AG29	VCCP170	VCCP170					
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L8	VCCP175	VCCP175					
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AD8	VCCP177	VCCP177					
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AH28	VCCP179	VCCP179					
AH21	VCCP180	VCCP180					
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	VCCP183	VCCP183					
	VCCP184	VCCP184					

Socket-IntelPrescottCPU

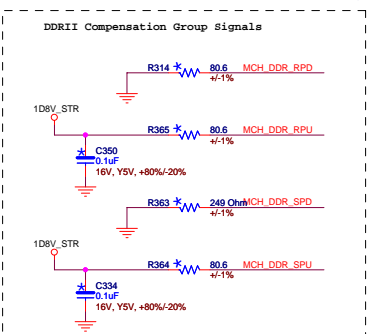
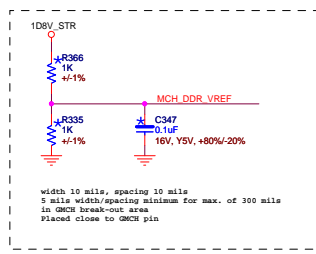
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		AF9	VCCP185	VSS41	AL23		
		AH11	VCCP186	VSS42	AL20		
		AJ14	VCCP187	VSS43	L25		
		AH19	VCCP188	VSS44	J7		
		AH29	VCCP189	VSS45	AE29		
		AH27	VCCP190	VSS46	AE9		
		AG28	VCCP191	VSS47	K5		
		AL26	VCCP192	VSS48	AE29		
		AM12	VCCP193	VSS49	AE30		
		T28	VCCP194	VSS50	AN20		
		W28	VCCP195	VSS51	AE10		
		J13	VCCP196	VSS52	AE24		
		T28	VCCP197	VSS53	AM4		
		W28	VCCP198	VSS54	AK23		
		J25	VCCP199	VSS55	H9		
		J27	VCCP200	VSS56	H13		
		AG19	VCCP201	VSS57	AC7		
		AL9	VCCP202	VSS58	AC5		
		AG25	VCCP203	VSS59	AH6		
		AF21	VCCP204	VSS60	AM16		
		AK14	VCCP205	VSS61	P25		
		J9	VCCP206	VSS62	W4		
		M27	VCCP207	VSS63	P25		
		AF14	VCCP208	VSS64	AE25		
		J30	VCCP209	VSS65	P23		
		AG18	VCCP210	VSS66	AG13		
		W27	VCCP211	VSS67	AG16		
		AG8	VCCP212	VSS68	AG17		
		AN8	VCCP213	VSS69	F19		
		AD29	VCCP214	VSS70	AH13		
		W8	VCCP215	VSS71	C7		
		AH8	VCCP216	VSS72	Y2		
		N24	VCCP217	VSS73	L30		
		AN22	VCCP218	VSS74	L29		
		J14	VCCP219	VSS75	D15		
		AK11	VCCP220	VSS76	AL27		
		AF19	VCCP221	VSS77	AH20		
		N8	VCCP222	VSS78	Y7		
		AF12	VCCP223	VSS79	AE5		
		M28	VCCP224	VSS80	AE23		
		AK9	VCCP225	VSS81	AE3		
			VCCP226	VSS82	AE3		
				VSS83	AE5		
				VSS84	AE6		
				VSS85	AE6		
				VSS86	AE7		
				VSS87	AE7		
				VSS88	AE8		
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				VSS120	AE9		
				VSS121	AE9		
				VSS122	AE9		
				VSS123	AE9		
				VSS124	AE9		
				VSS125	AE9		

Socket-IntelPrescottCPU

VCCP		U2G		7 OF 7		VCCP	
		H22	VSS126	VSS201	AE10		
		H21	VSS127	VSS202	AE13		
		H20	VSS128	VSS203	H6		
		H19	VSS129	VSS204	A18		
		H18	VSS130	VSS205	A2		
		H17	VSS131	VSS206	E2		
		H16	VSS132	VSS207	C4		
		H15	VSS133	VSS208	H3		
		H14	VSS134	VSS209	AE5		
		H13	VSS135	VSS210	DE		
		H12	VSS136	VSS211	AE6		
		H11	VSS137	VSS212	A3		
		H10	VSS138	VSS213	B1		
		H9	VSS139	VSS214	H5		
		H8	VSS140	VSS215	B8		
		H7	VSS141	VSS216	A4		
		H6	VSS142	VSS217	AH1		
		H5	VSS143	VSS218	V7		
		H4	VSS144	VSS219	C13		
		H3	VSS145	VSS220	AK24		
		H2	VSS146	VSS221	AB30		
		H1	VSS147	VSS222	L6		
			VSS148	VSS223	L7		
			VSS149	VSS224	AB29		
			VSS150	VSS225	M1		
			VSS151	VSS226	E8		
			VSS152	VSS227	AG20		
			VSS153	VSS228	AN17		
			VSS154	VSS229	AB27		
			VSS155	VSS230	AB26		
			VSS156	VSS231	AN16		
			VSS157	VSS232	AN16		
			VSS158	VSS233	AM		
			VSS159	VSS234	AB25		
			VSS160	VSS235	AB24		
			VSS161	VSS236	AB23		
			VSS162	VSS237	N5		
			VSS163	VSS238	AA30		
			VSS164	VSS239	AG10		
			VSS165	VSS240	AE13		
			VSS166	VSS241	H28		
			VSS167	VSS242	F7		
			VSS168	VSS243	AE29		
			VSS169	VSS244	AE27		
			VSS170	VSS245	AE25		
			VSS171	VSS246	AN28		
			VSS172	VSS247	AN27		
			VSS173	VSS248	AE24		



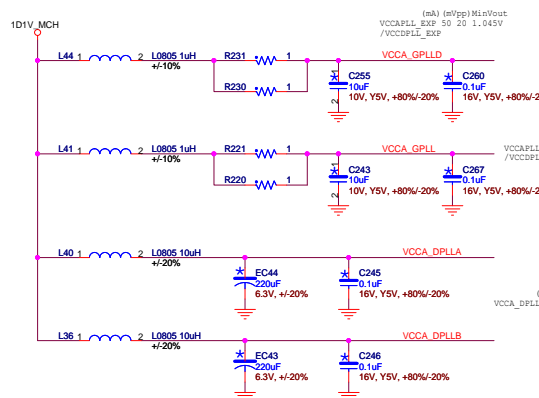
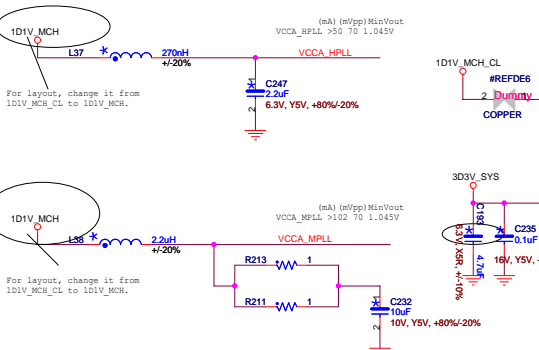
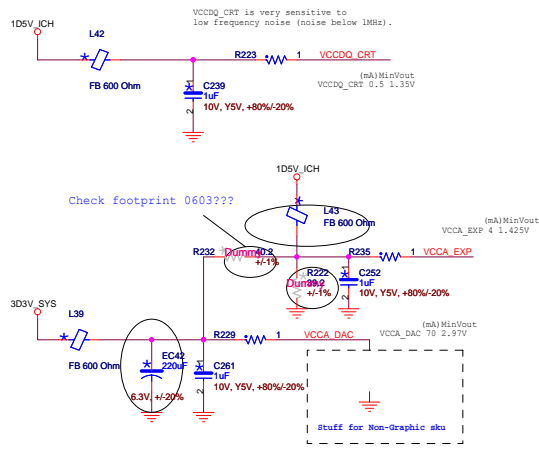
Note:
 For a single DIMM per channel implementation,
 the following second DIMM specific system memory
 signals should be tested/pinpointed:
 CR/CBR[3:1] - DDR2 Clock Pairs
 CV/CBV[3 and 5] - Channel A DDR3 Clock Pairs
 CW/CBW[3 and 4] - Channel B DDR3 Clock Pairs
 CSB[3:2]
 CSV[3:2]
 CDT[3:2]



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Title: **Eaglelake-GMCH-2**

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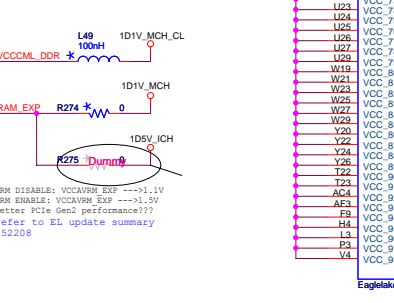
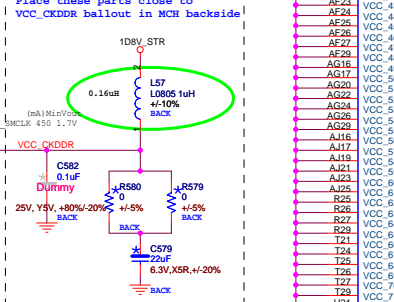


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AA32	VCC_CL_1	AK21	VCC_CL_42
AA33	VCC_CL_2	AK22	VCC_CL_43
AB32	VCC_CL_3	AK23	VCC_CL_44
AB33	VCC_CL_4	AK24	VCC_CL_45
AD32	VCC_CL_5	AK25	VCC_CL_46
AD33	VCC_CL_6	AK26	VCC_CL_47
AE32	VCC_CL_7	AK27	VCC_CL_48
AE33	VCC_CL_8	AK28	VCC_CL_49
AF32	VCC_CL_9	AK29	VCC_CL_50
AF33	VCC_CL_10	AK30	VCC_CL_51
AL32	VCC_CL_11	AL1	VCC_CL_52
AL33	VCC_CL_12	AL10	VCC_CL_53
AM15	VCC_CL_13	AL11	VCC_CL_54
AM16	VCC_CL_14	AL12	VCC_CL_55
AM17	VCC_CL_15	AL13	VCC_CL_56
AM20	VCC_CL_16	AL14	VCC_CL_57
AM21	VCC_CL_17	AL15	VCC_CL_58
AM22	VCC_CL_18	AL16	VCC_CL_59
AM24	VCC_CL_19	AL17	VCC_CL_60
AM25	VCC_CL_20	AL18	VCC_CL_61
AM26	VCC_CL_21	AL19	VCC_CL_62
AM29	VCC_CL_22	AL20	VCC_CL_63
Y32	VCC_CL_23	AL21	VCC_CL_64
Y33	VCC_CL_24	AL22	VCC_CL_65
AP1	VCC_CL_25	AL23	VCC_CL_66
AP2	VCC_CL_26	AL24	VCC_CL_67
AP3	VCC_CL_27	AL25	VCC_CL_68
AA31	VCC_CL_28	AL26	VCC_CL_69
AB31	VCC_CL_29	AL27	VCC_CL_70
AC31	VCC_CL_30	AL28	VCC_CL_71
AD31	VCC_CL_31	AL29	VCC_CL_72
AE31	VCC_CL_32	AL30	VCC_CL_73
AF31	VCC_CL_33	AL31	VCC_CL_74
AG30	VCC_CL_34	AL32	VCC_CL_75
AG31	VCC_CL_35	AL33	VCC_CL_76
AI30	VCC_CL_36	AM3	VCC_CL_77
AJ31	VCC_CL_37	AM4	VCC_CL_78
AK16	VCC_CL_38	AA16	VCC_CL_79
AK17	VCC_CL_39	AA17	VCC_CL_80
AK18	VCC_CL_40	AA18	VCC_CL_81
AK19	VCC_CL_41	AA19	VCC_CL_82
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		AA21	VCC_CL_84
		AA22	VCC_CL_85

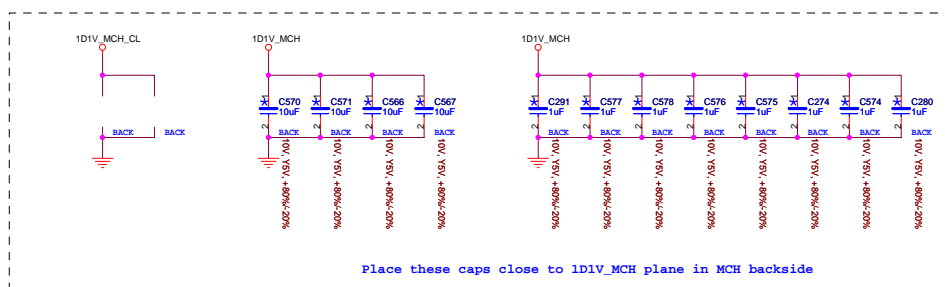
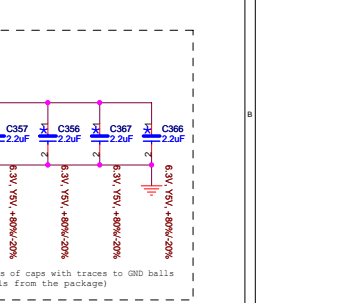
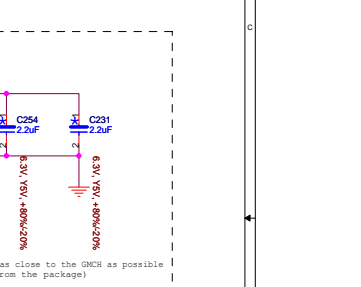
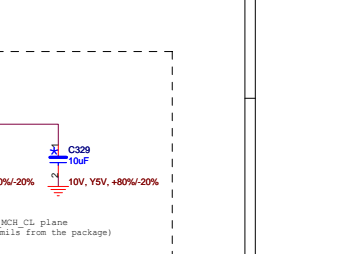
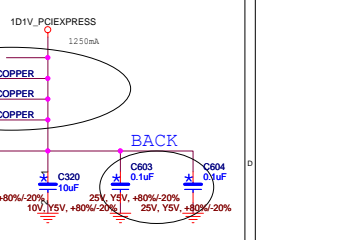
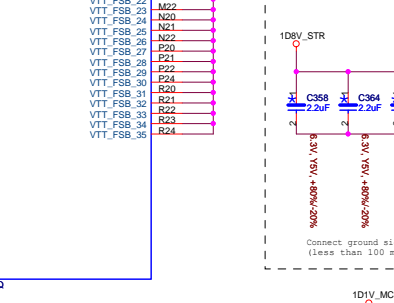
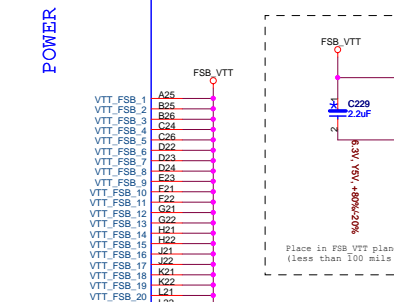
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AA23	VCC_4	AA17	VCC_EXP_4
AA24	VCC_5	AA18	VCC_EXP_5
AA25	VCC_6	AA19	VCC_EXP_6
AA26	VCC_7	AA20	VCC_EXP_7
AA27	VCC_8	AA21	VCC_EXP_8
AA28	VCC_9	AA22	VCC_EXP_9
AA29	VCC_10	AA23	VCC_EXP_10
AA30	VCC_11	AA24	VCC_EXP_11
AA31	VCC_12	AA25	VCC_EXP_12
AA32	VCC_13	AA26	VCC_EXP_13
AA33	VCC_14	AA27	VCC_EXP_14
AA34	VCC_15	AA28	VCC_EXP_15
AA35	VCC_16	AA29	VCC_EXP_16
AA36	VCC_17	AA30	VCC_EXP_17
AA37	VCC_18	AA31	VCC_EXP_18
AA38	VCC_19	AA32	VCC_EXP_19
AA39	VCC_20	AA33	VCC_EXP_20
AA40	VCC_21	AA34	VCC_EXP_21
AA41	VCC_22	AA35	VCC_EXP_22
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AA43	VCC_24	AA37	VCC_EXP_24
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AA46	VCC_27	AA40	VCC_EXP_27
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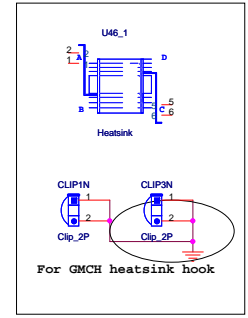
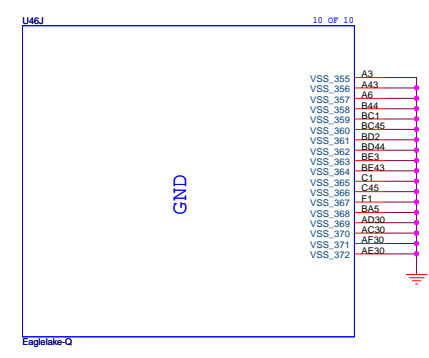
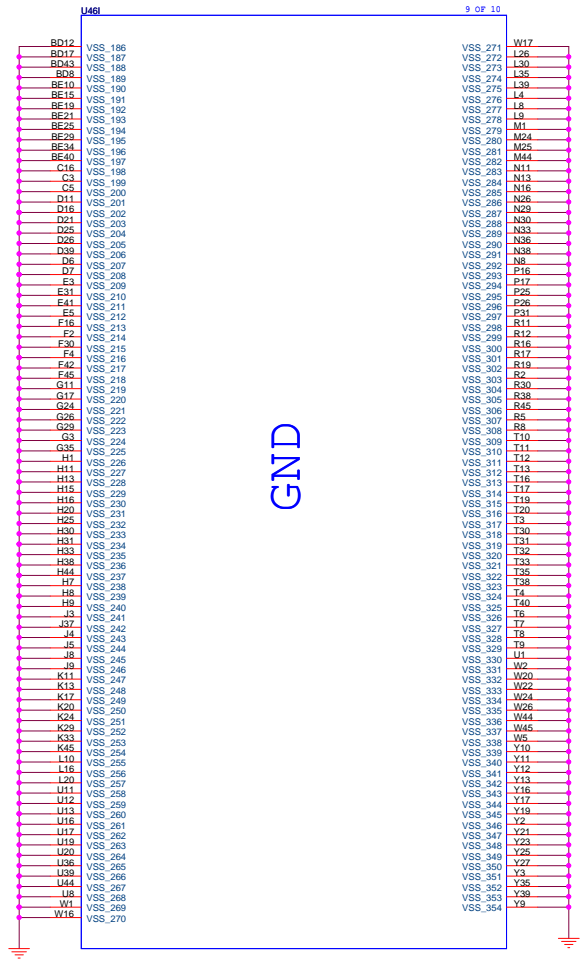
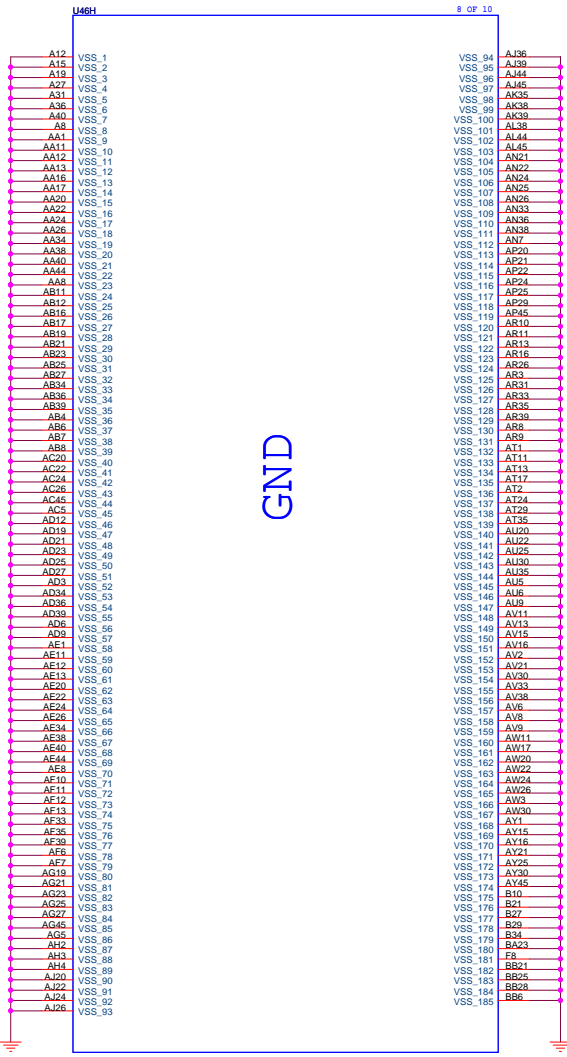
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AA23	VCC_4	AA17	VCC_EXP_4
AA24	VCC_5	AA18	VCC_EXP_5
AA25	VCC_6	AA19	VCC_EXP_6
AA26	VCC_7	AA20	VCC_EXP_7
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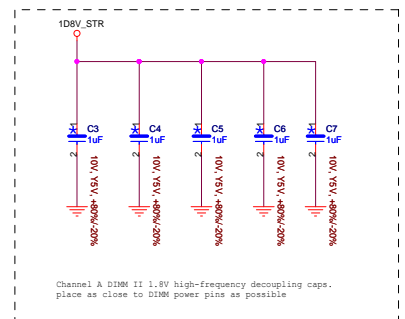
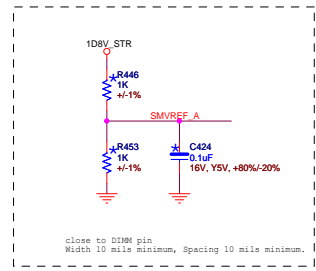
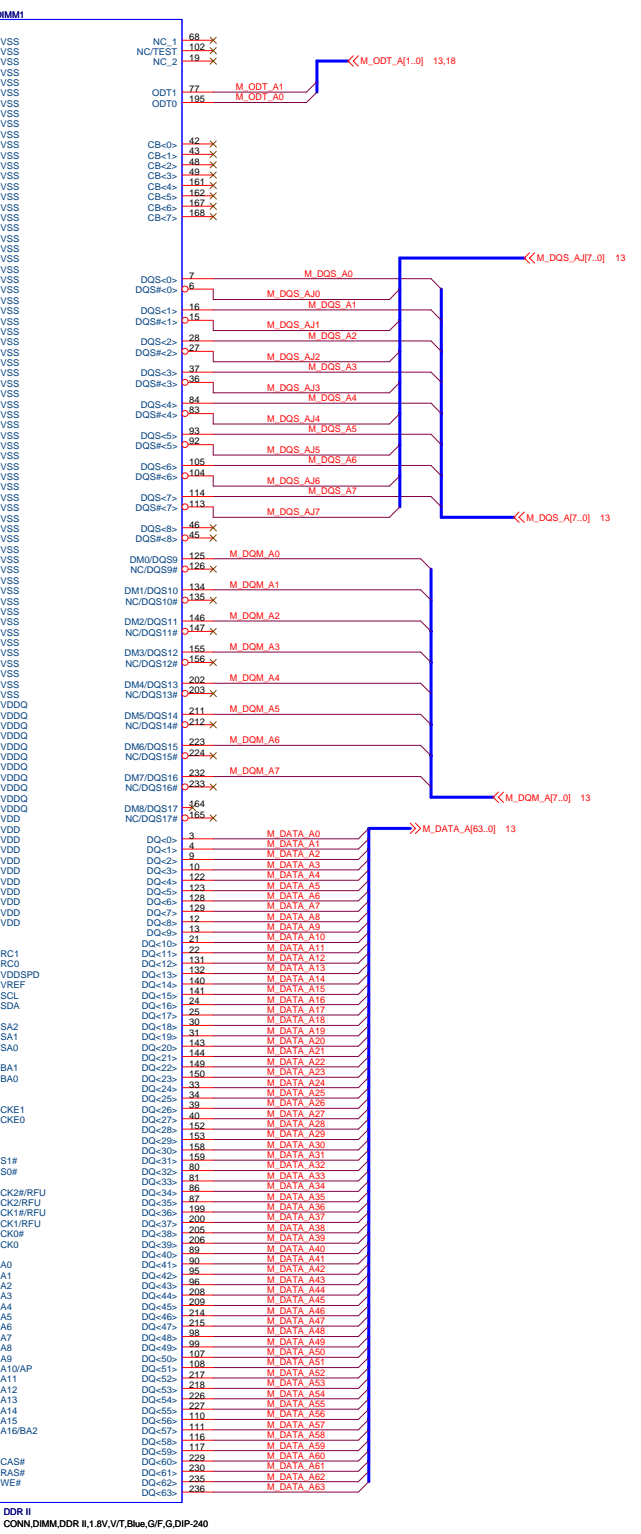
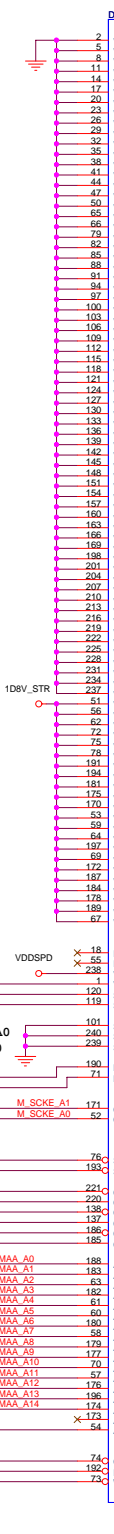
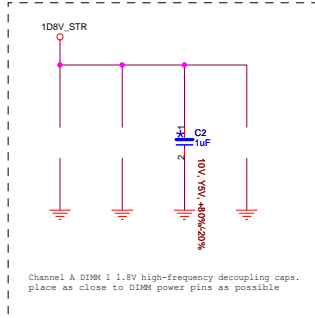
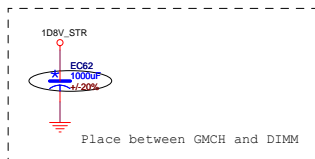
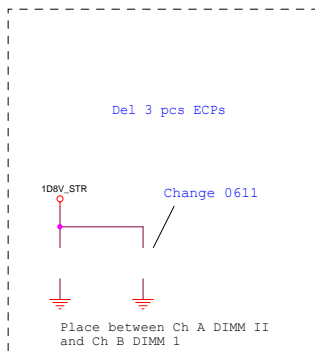
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 Size: C Document Number: G43M01S1 Rev: A
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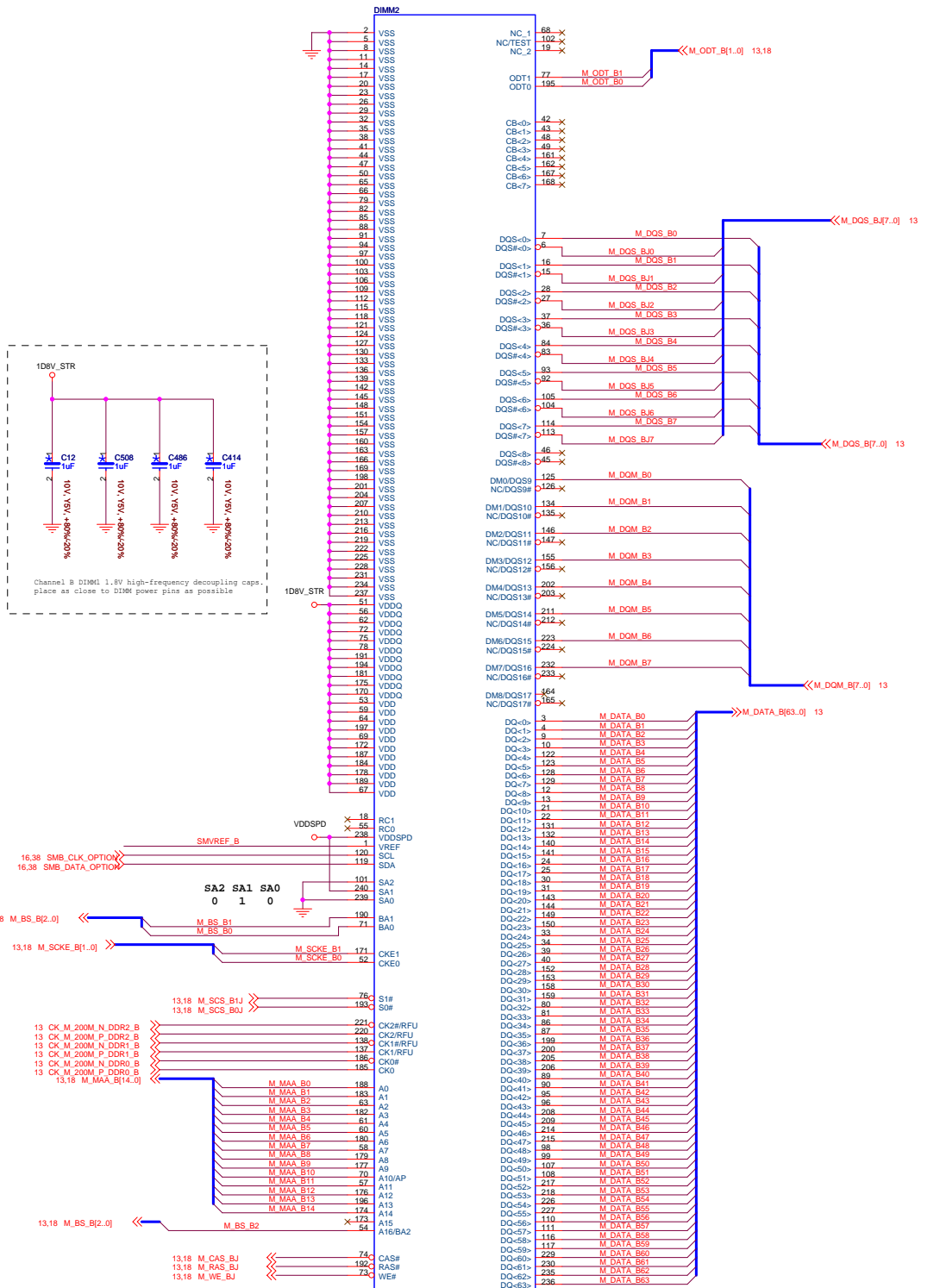
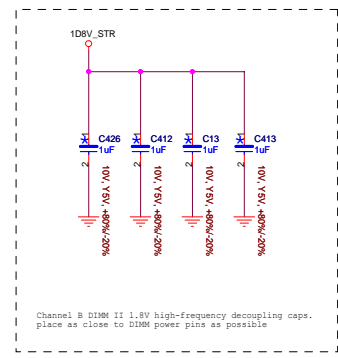
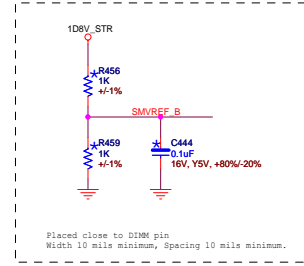
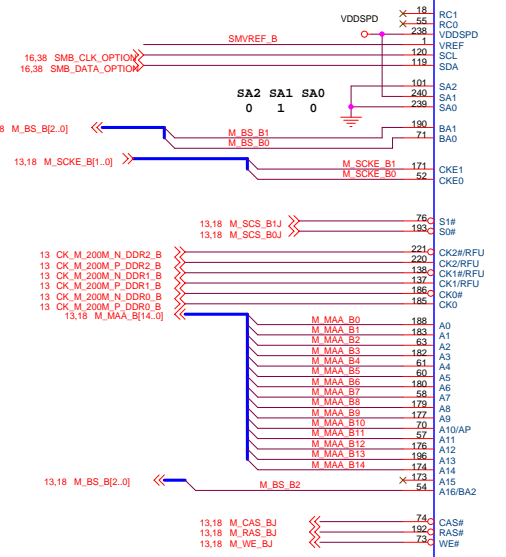
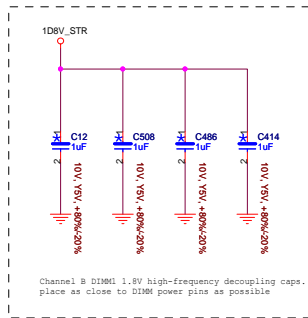
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Title: DDR3 Channel A DIMM 1, 2

Size C: Document Number: **G43M01S1**

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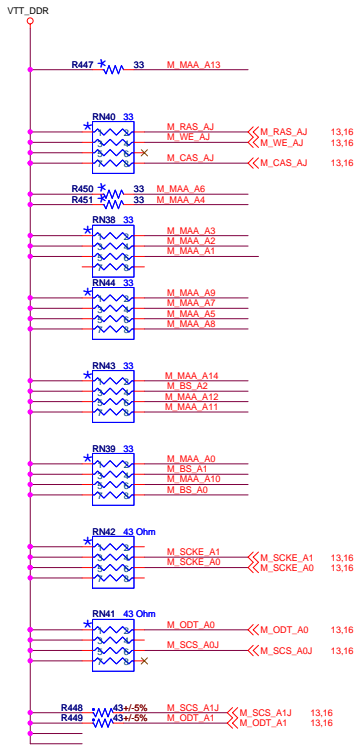
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Size C Document Number **G43M01S1** Rev A

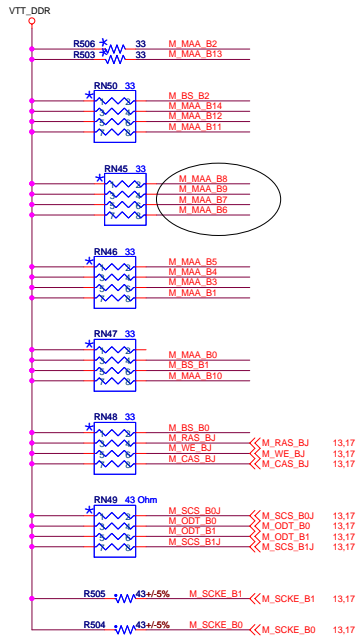
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 <<M_BS_A[2..0] 13,16
 <<M_MAA_A[14..0] 13,16

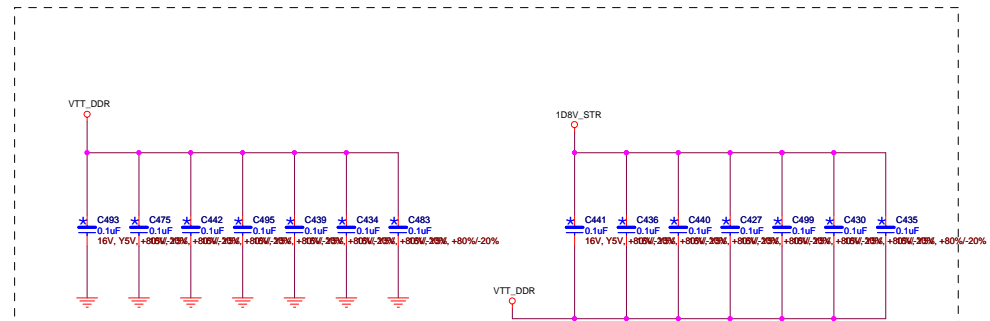
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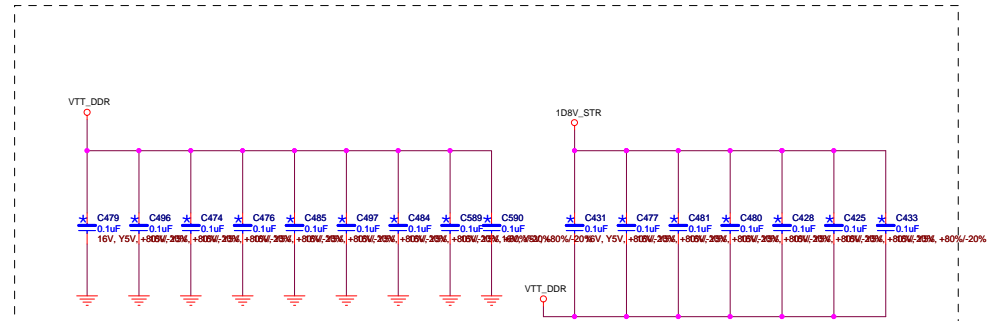
Channel A VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



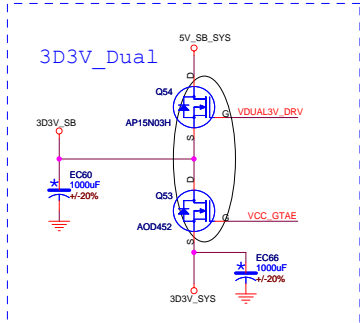
Channel B VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



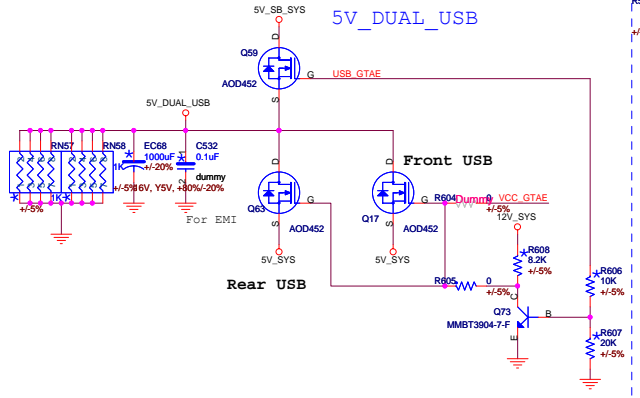
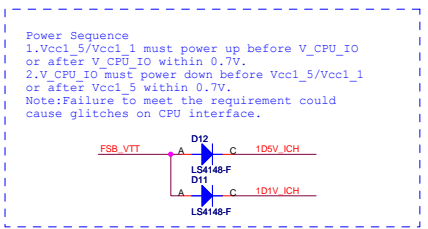
Channel A VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible



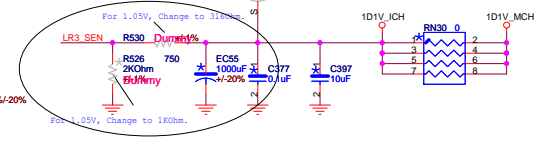
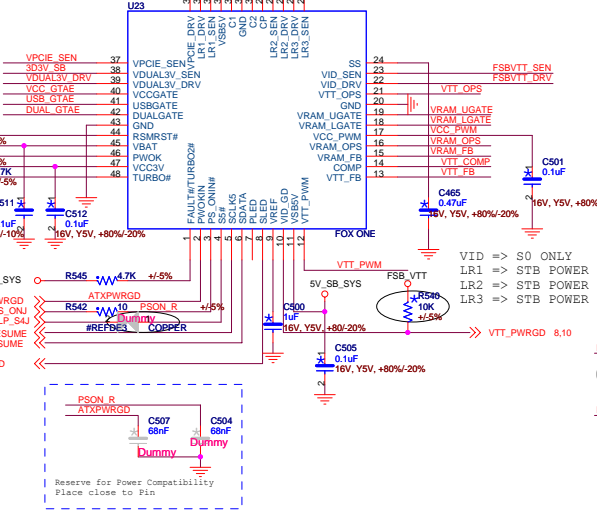
Channel B VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

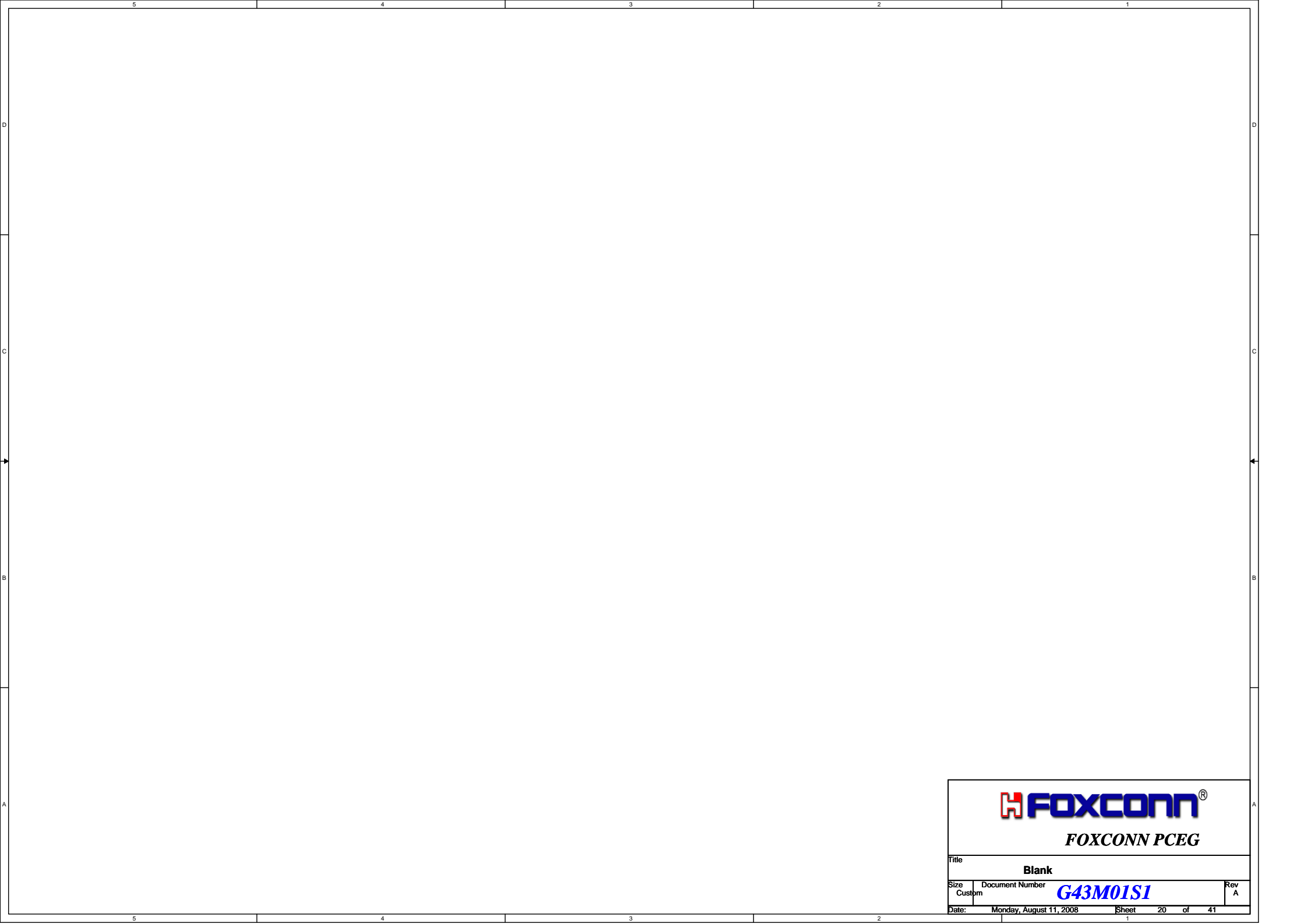


Note:
Over voltage regulator summary:
1. LRPCIE: can set the reference voltage by software.
A: Vref: 0.68V~0.96V /16 steps (Turbo2, Turbo1+2)
B: Vref: 0.74V~1.04V /16 steps (Turbo2, Turbo1+others)
2. LR3: can set the reference voltage by software.
Vref: 0.74V~1.04V /16 steps
3. PWRVRAM_P90VTT:
Vref: 0.74V~1.04V /16 steps



Del SLP_5# control method
For VTT Power OCP





5

4

3

2

1

D

D

C

C

B

B

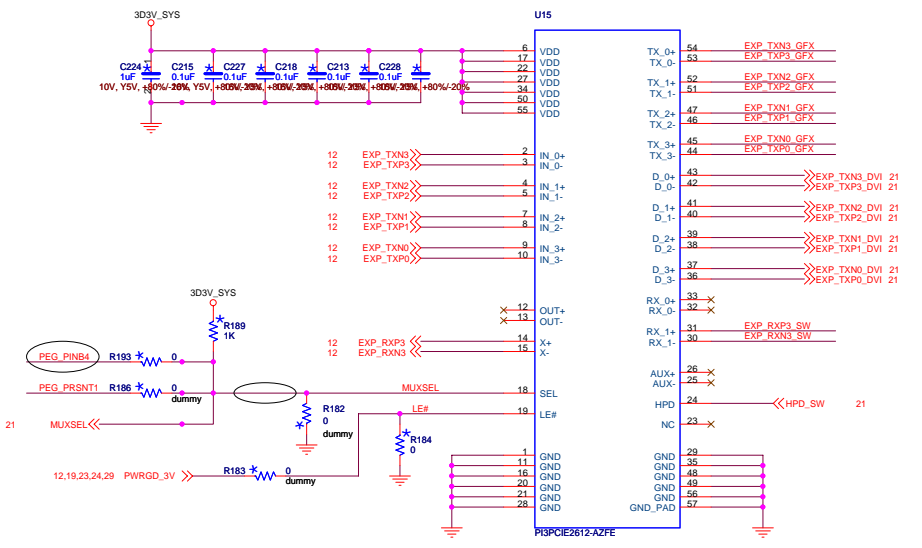
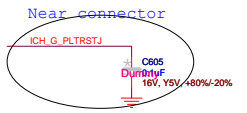
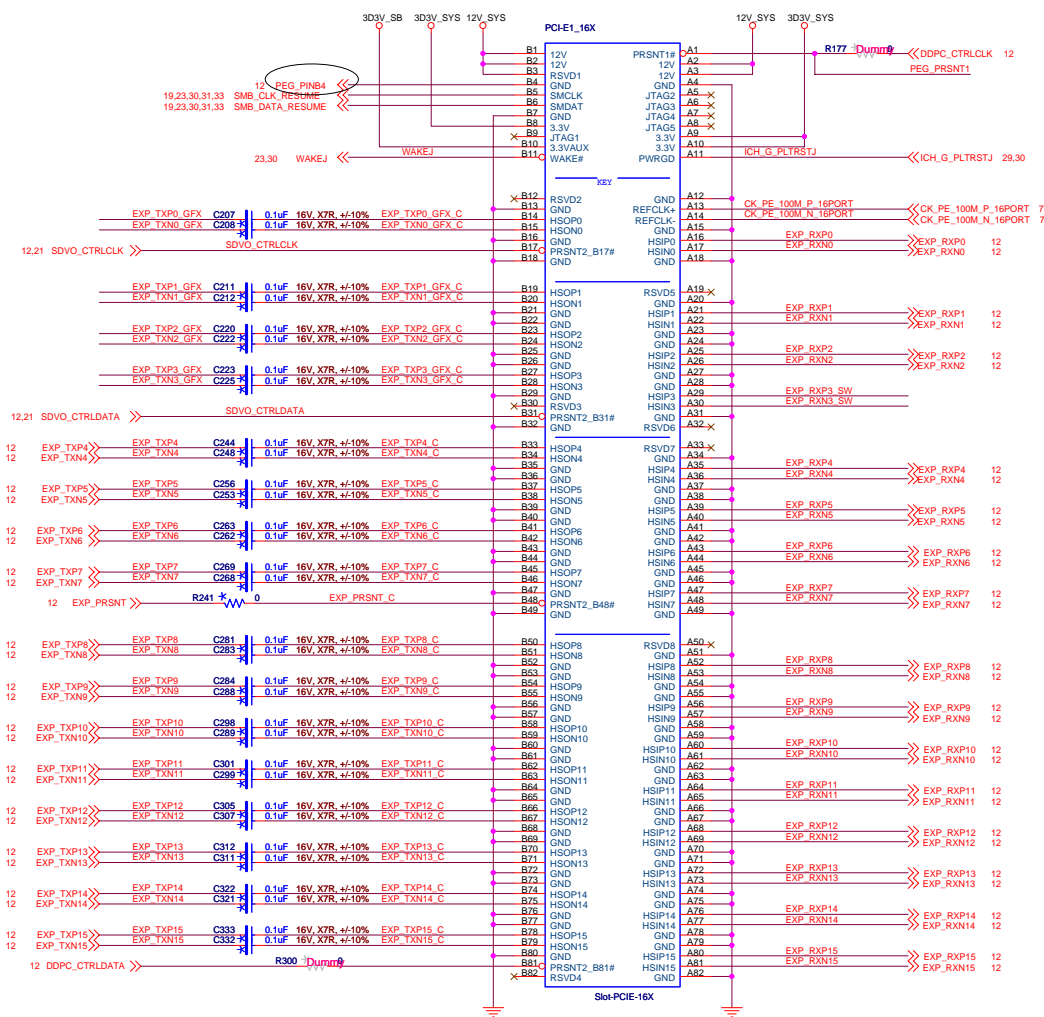
A

A

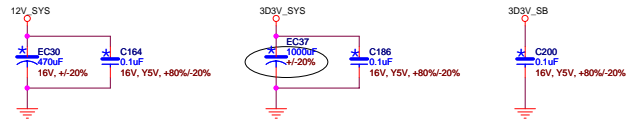


FOXCONN PCEG

Title			
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Size	Document Number	Rev	
Custom	G43M01S1	A	
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Change to another part.
050608

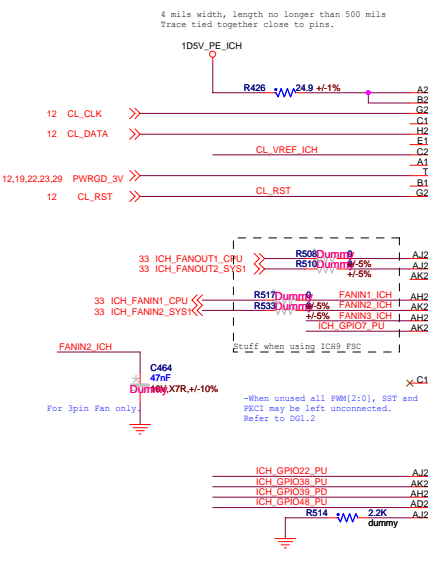
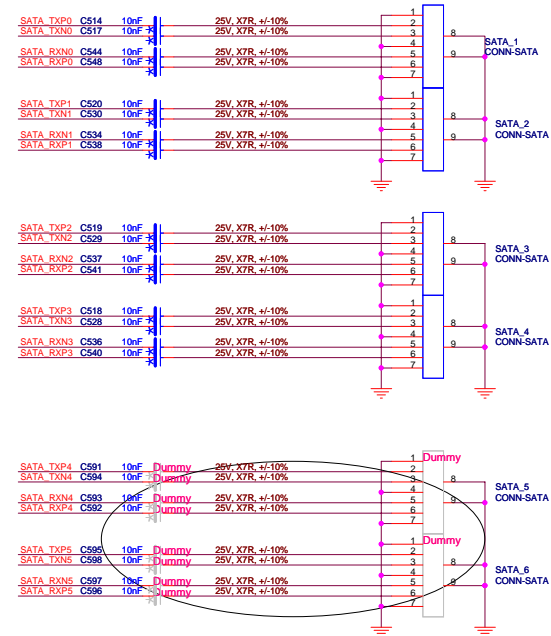
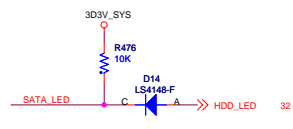


FOXCONN
FOXCONN PCEG

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Size	Document Number	G43M01S1	
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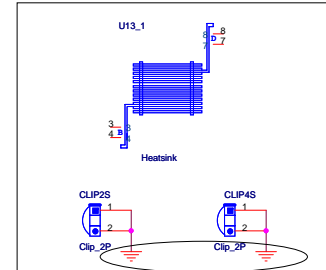
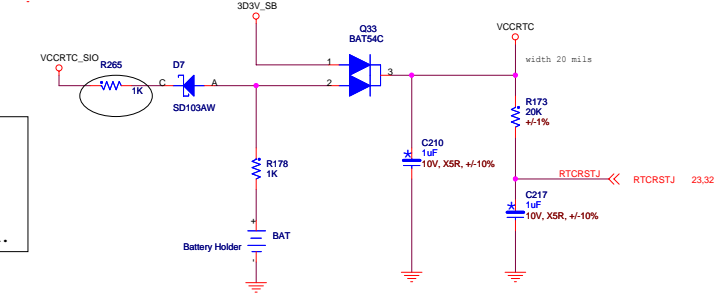
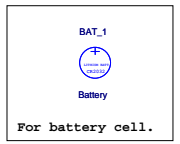
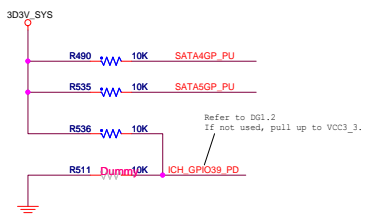
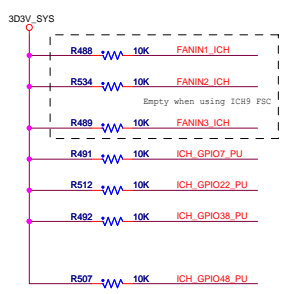
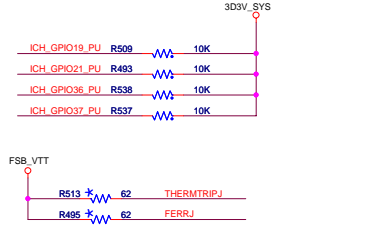
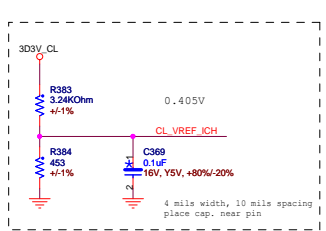
ICH10

SATA0RXN	AK17	SATA_RXN0	
SATA0RXP	AJ17	SATA_RXP0	
SATA0TXN	AK19	SATA_TXN0	
SATA0TXP	AJ19	SATA_TXP0	
SATA1RXN	AJ15	SATA_RXN1	
SATA1RXP	AK15	SATA_RXP1	
SATA1TXN	AH16	SATA_TXN1	
SATA1TXP	AE16	SATA_TXP1	
SATA2RXN	AJ13	SATA_RXN2	
SATA2RXP	AK13	SATA_RXP2	
SATA2TXN	AH14	SATA_TXN2	
SATA2TXP	AE14	SATA_TXP2	
SATA3RXN	AJ11	SATA_RXN3	
SATA3RXP	AK11	SATA_RXP3	
SATA3TXN	AE12	SATA_TXN3	
SATA3TXP	AH12	SATA_TXP3	
SATA4RXN	AJ9	SATA_RXN4	
SATA4RXP	AK9	SATA_RXP4	
SATA4TXN	AE10	SATA_TXN4	
SATA4TXP	AH9	SATA_TXP4	
SATA5RXN	AK7	SATA_RXN5	
SATA5RXP	AE7	SATA_RXP5	
SATA5TXN	AH7	SATA_TXN5	
SATA5TXP	AE18	SATA_TXP5	
SATA6RXN	AK18	CK SATA 100M N_ICH	CK SATA_100M_N_ICH 7
SATA6RXP	AE18	CK SATA 100M P_ICH	CK SATA_100M_P_ICH 7
SATA6TXN	AK19		
SATA6TXP	AE19		
SATA6CLKN			
SATA6CLKP			
SATALEDB	AE7	SATA_LED	
SATARBASN	AK6	SATARBASN_ICH	R484 24.9 +/-1%
SATARBASP	AJ6		
GP21 SATA0GP	AK25	ICH_GPIO21_PU	
GP19 SATA1GP	AE20	ICH_GPIO19_PU	
GP36 SATA2GP	AE21	ICH_GPIO36_PU	
GP37 SATA3GP	AE22	ICH_GPIO37_PU	
SATA4GP	AD22	SATA4GP_PU	
SATA5GP	AD21	SATA5GP_PU	
A20GATE	P8	A20GATE	29
A20M	AJ28	A20MJ	10
IGNNEB	AC22	IGNNEJ	10
INT3_3VB	M3		
INTR	AH27	INTR	9
FERRL	AF27	FERRJ	10
NMI	L3	NMI	10
RCINB	NG	KBRSTJ	29
SERIR0	NG	SERIRJ	29,34
SMID	AJ29	SMIJ	10
STPCLKB	AD24	STPCLKJ	10
THRMTRIPB	AD24	THRMTRIPJ	10
PECI	AC23	R488 Dummy	10,29



3 OF 6

For SEC spec change for EV2 stage



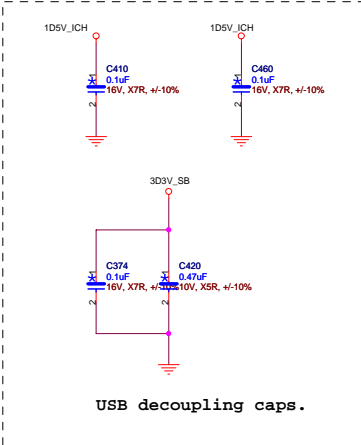
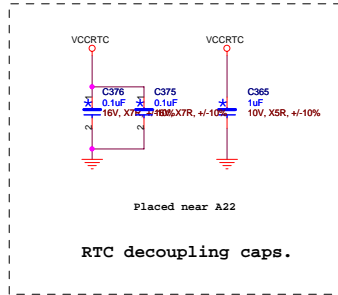
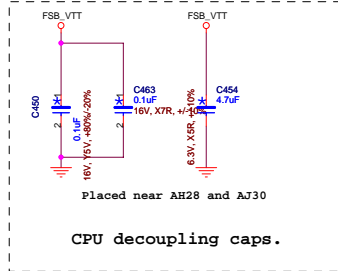
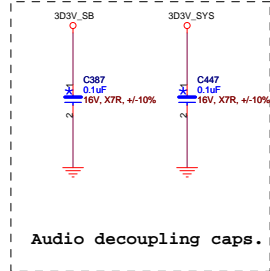
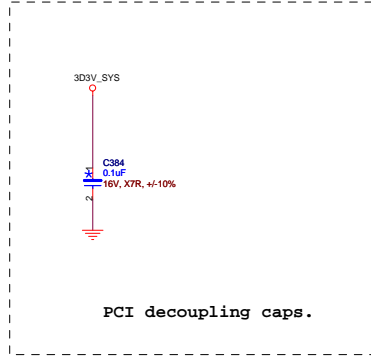
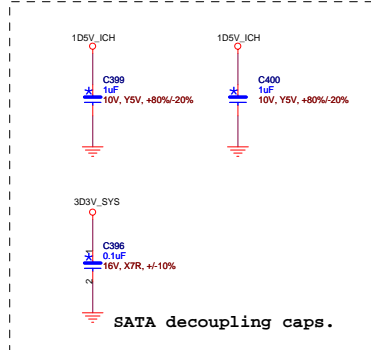
FOXCONN
FOXCONN PCEG

Title: ICH10 -2
Size: C Document Number: G43M01S1
Date: Monday, August 11, 2008 Sheet: 24 of 41

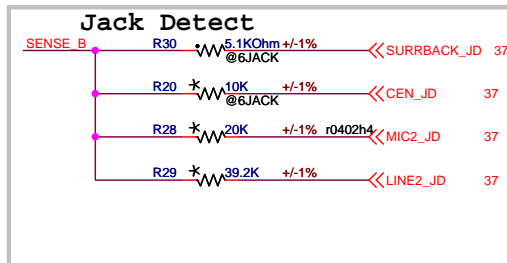
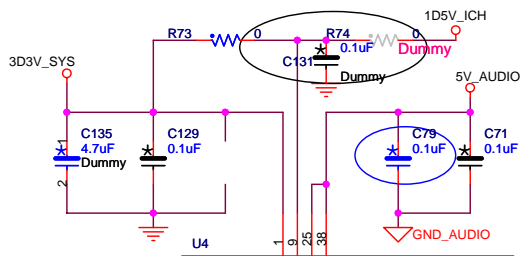
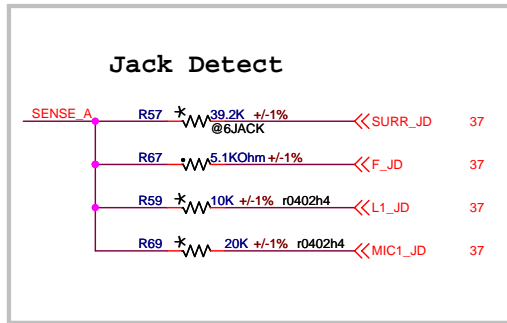
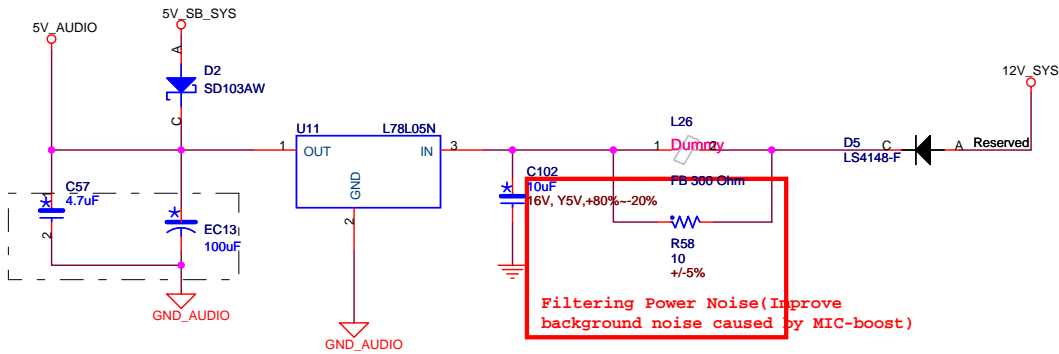
ICH10

G30	VSS_100	H13
G29	VSS_101	H19
G25	VSS_102	H2
G16	VSS_103	H22
F9	VSS_104	H25
F6	VSS_105	H26
F28	VSS_106	H28
F26	VSS_107	H5
F21	VSS_108	J29
E30	VSS_109	K30
E29	VSS_110	K26
E22	VSS_111	K28
E2	VSS_112	K28
E18	VSS_113	L23
E15	VSS_114	L20
D28	VSS_115	L20
D8	VSS_116	L30
B8	VSS_117	M14
B5	VSS_118	M16
B28	VSS_119	M28
B25	VSS_120	M28
B2	VSS_121	M6
B19	VSS_122	M6
B17	VSS_123	M13
B14	VSS_124	M14
B11	VSS_125	M15
AK9	VSS_126	M16
AK30	VSS_127	M18
AK29	VSS_128	M29
AK16	VSS_130	N30
AK12	VSS_131	N23
AK14	VSS_132	P13
AJ8	VSS_133	P14
AJ6	VSS_134	P15
AJ5	VSS_135	P16
AJ23	VSS_136	P17
AJ20	VSS_138	P18
AJ16	VSS_139	P19
AJ14	VSS_140	P2
AJ12	VSS_141	P28
AH8	VSS_142	P6
AH6	VSS_143	P6
AH20	VSS_144	R14
AH2	VSS_145	R14
AH19	VSS_146	R15
AH15	VSS_147	R16
AH13	VSS_148	R17
AG28	VSS_149	R18
AF9	VSS_150	R23
AF7	VSS_151	R29
AF29	VSS_152	R30
AF26	VSS_153	R8
AF23	VSS_154	T12
AF20	VSS_155	T13
AF15	VSS_156	T14
AF13	VSS_157	T15
AE9	VSS_158	T16
AE8	VSS_159	T17
AE6	VSS_160	T18
AE5	VSS_161	T19
AE25	VSS_162	T2
AE19	VSS_163	T29
AE18	VSS_164	T5
AE16	VSS_165	L13
AE15	VSS_166	L14
AE14	VSS_167	L15
AE13	VSS_168	L16
AE12	VSS_169	L17
AE10	VSS_170	L18
AE1	VSS_171	L23
AD9	VSS_172	L13
AD7	VSS_173	V14
AD3	VSS_174	V15
AD22	VSS_175	V16
AD18	VSS_176	V18
AD19	VSS_177	V17
AD16	VSS_178	V26
AD15	VSS_179	V28
AD14	VSS_180	V3
AC8	VSS_181	V7
AC6	VSS_182	W1
AC5	VSS_183	W14
AC30	VSS_184	W16
AC29	VSS_185	W23
AC24	VSS_186	W29
AC12	VSS_187	W30
AC1	VSS_188	W5
AB3	VSS_189	W6
AB28	VSS_190	Y26
AB26	VSS_191	Y28
AA6	VSS_192	Y3
AA5	VSS_193	Y7
AA27	VSS_194	AA30
AA29	VSS_195	AA29
AA4	VSS_196	AA1
AF3	VSS_197	AA0
B27	VSS_198	A1

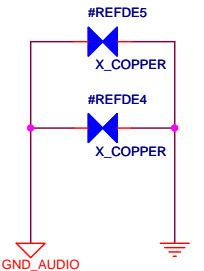
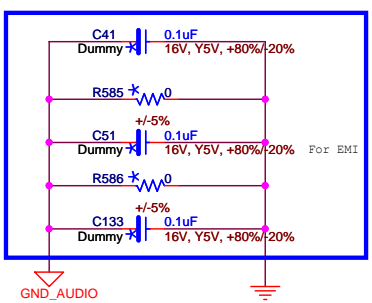
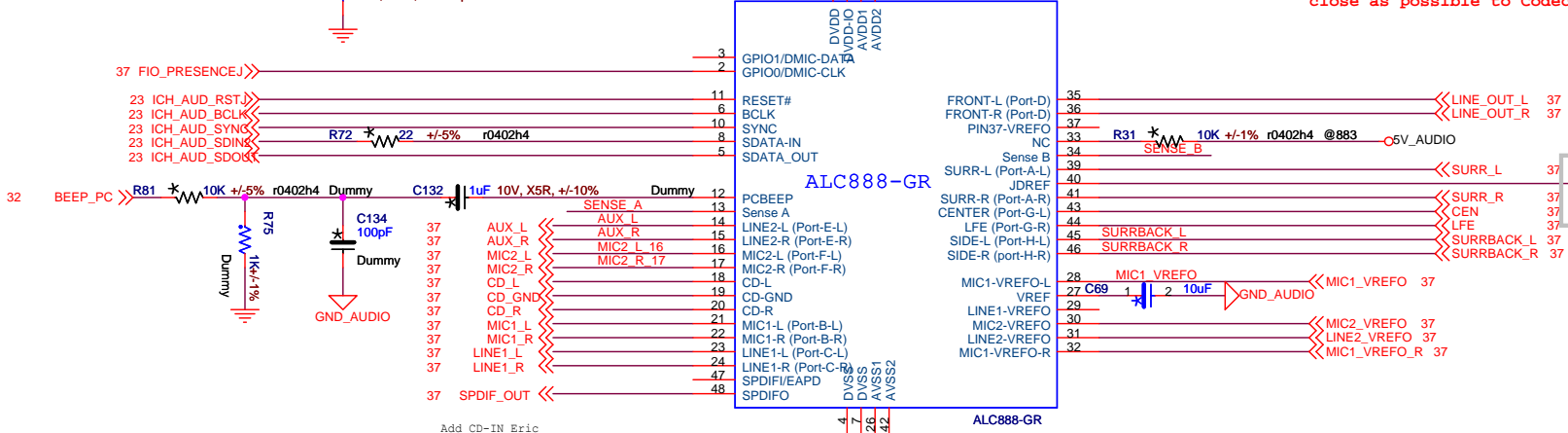
6 OF 6



Del PLTRST# and PCIRST# buffer
Use SIO PCIRST# buffer



All of JD resistors should be placed as close as possible to Codec.

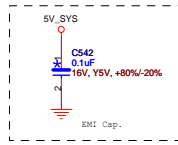
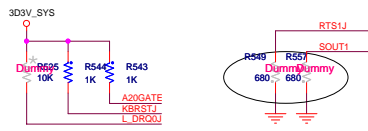


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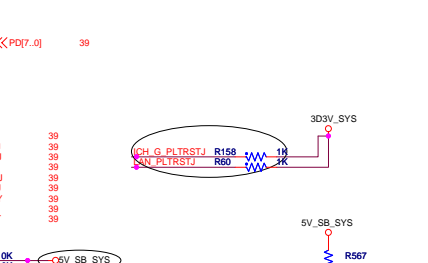
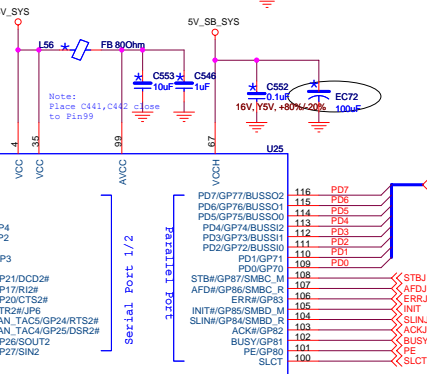
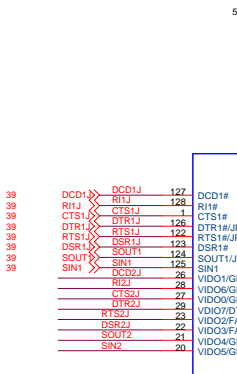
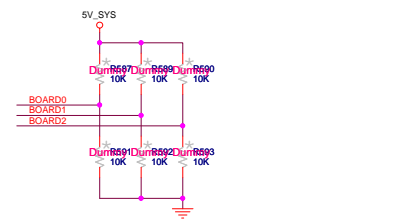
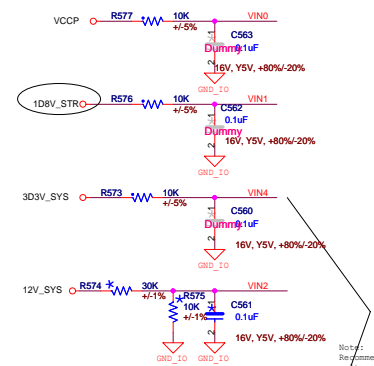
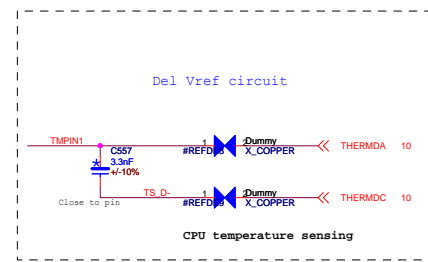
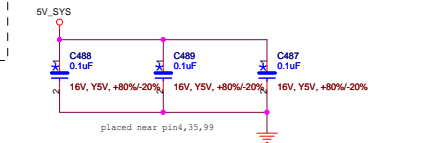
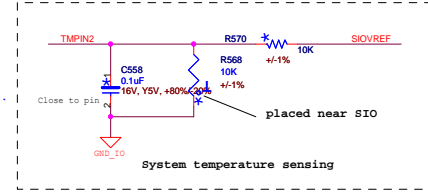
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Size	Document Number	G43M01S1			Rev
Custom					A
Date:	Monday, August 11, 2008	Sheet	28	of	41

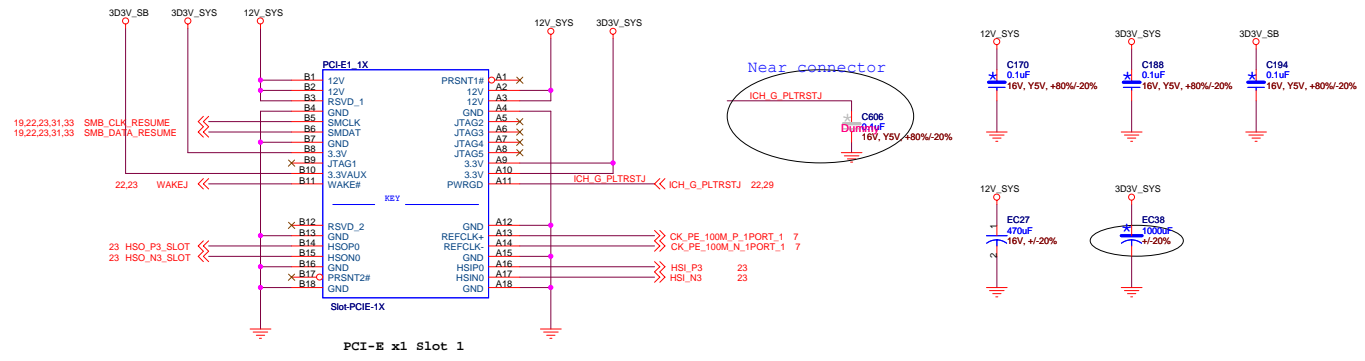
If without use these pins, Please pull-up to VCC.
Don't let it floating

- 1.Pin 30:RESETCON#
- 2.Pin 95:VIN3/ATXPG
- 3.Pin 71:SUSB#
- 4..Power On Strapping Options pin
- 5.Please don't remove the pull-up resistor (R108) of pin38/LDRQ#.
- 6.Please don't remove any components in the VINk circuits and the FANk control circuits.
- 7.Please don't change the sequence of VINO-VIN6.
- 8.If without use these pins,please pull-up to VCC, Don't let it floating ,pin 30,pin 38,pin 46, pin 95,pin 122,pin 124,pin 126.

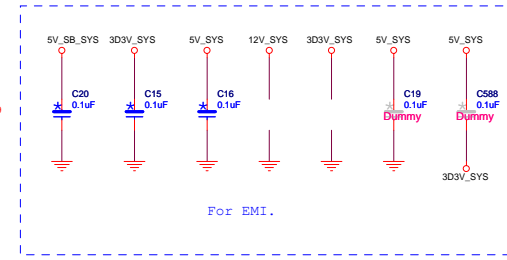
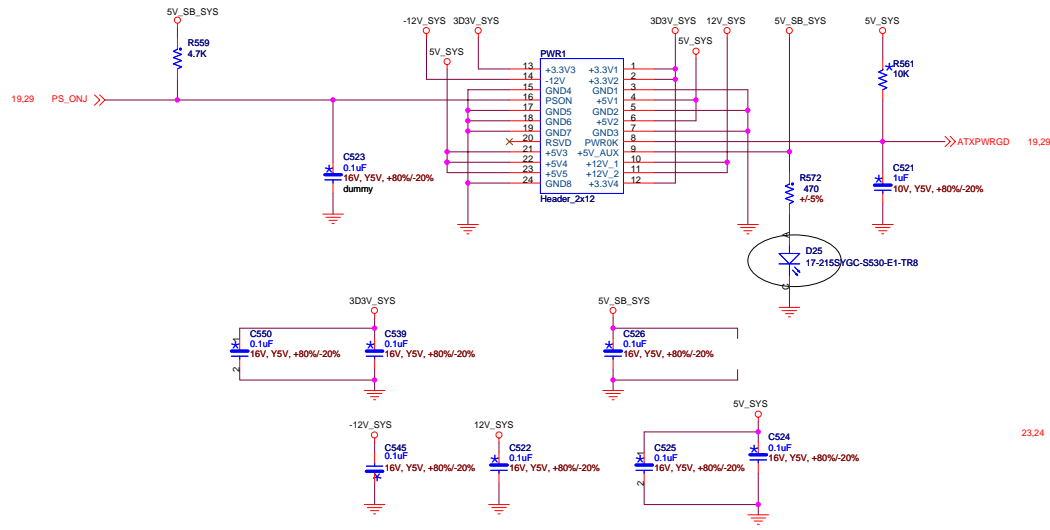


For the temperature sensor circuits,
1)Please don't remove the 1uF capacitor(C4) between Vref and AGND.
2)Place the thermal diode close to IT8720F.
3)Keep the trace away from +12V, fast data bus, and CRTs.
4)Recommended trace widths and spacings are 12 mils.
5)Isolate AGND and DGND.



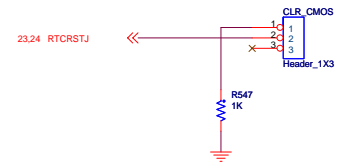


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PCI Express x1 Slot		
Size	Document Number	Rev
C	G43M01S1	A
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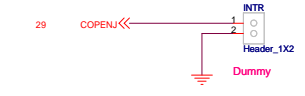


Clear CMOS

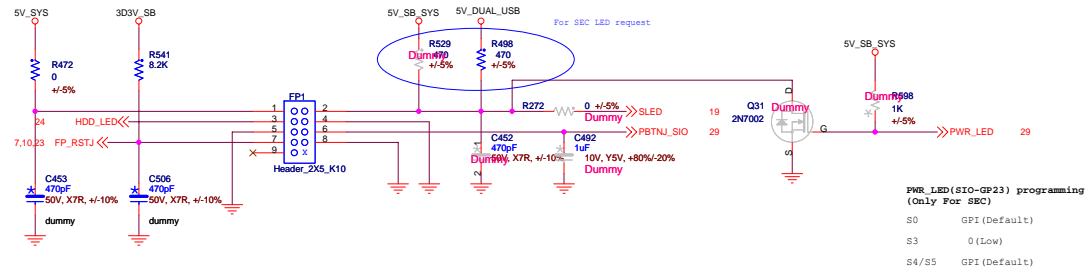
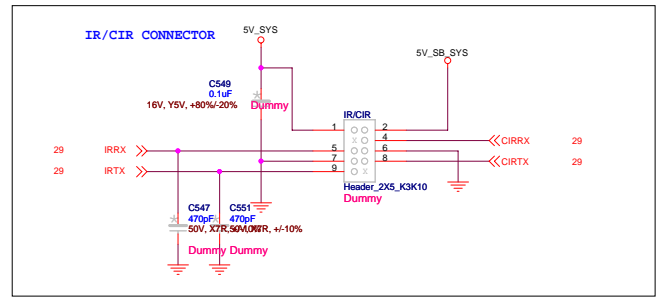
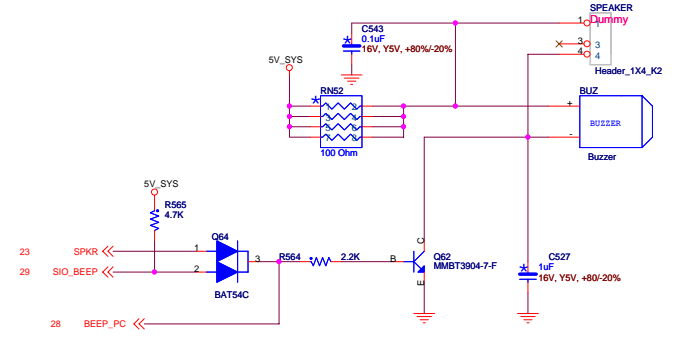
CLR_CMOS	CMOS
Clear	(1-2)
Normal	(2-3)



Chassis Intruder Header



SPEAKER HEADER



PWR_LED (SIO-GP23) programming
(Only For SEC)

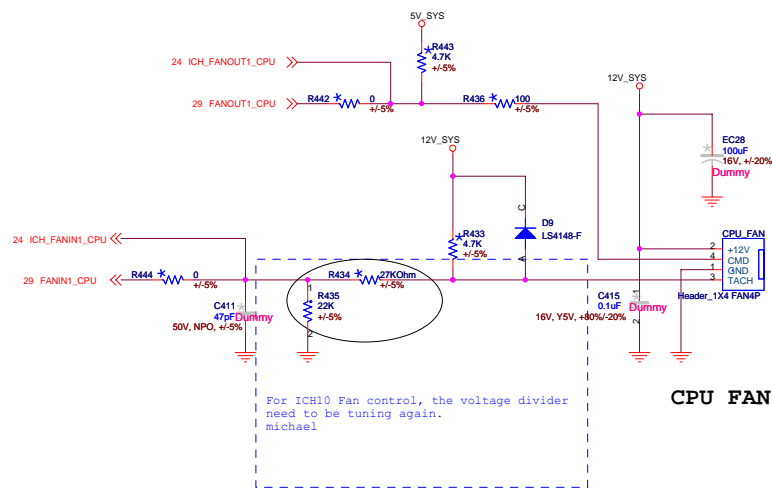
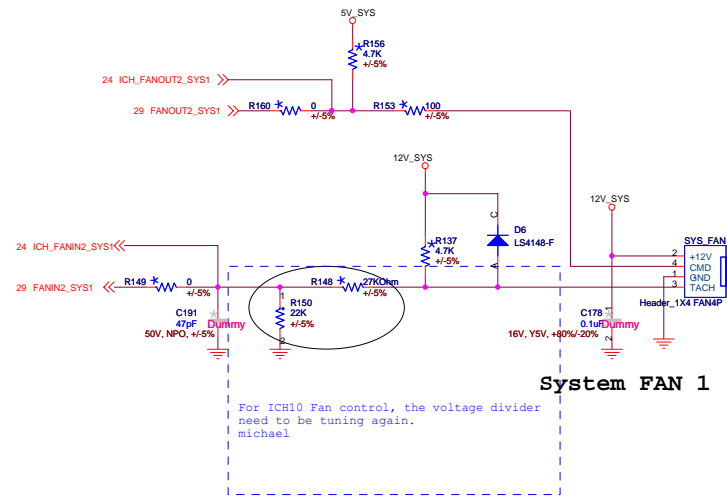
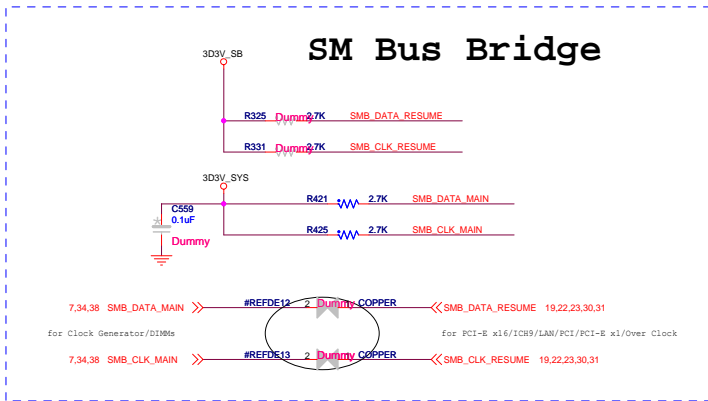
S0 GPI (Default)
S3 0 (Low)
S4/S5 GPI (Default)

FOXCONN
FOXCONN PCEG

Title: **ATX, FP, MISC Connector**

Size C Document Number: **G43M01S1** Rev A

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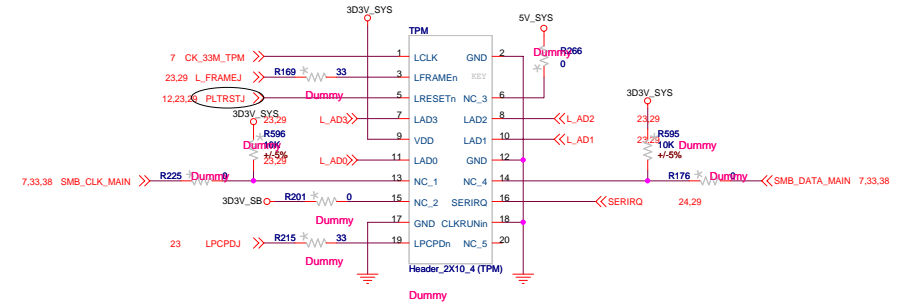


4-pin FAN Header Definition
 pin1. GND
 pin2. +12V
 pin3. Sense
 pin4. Control

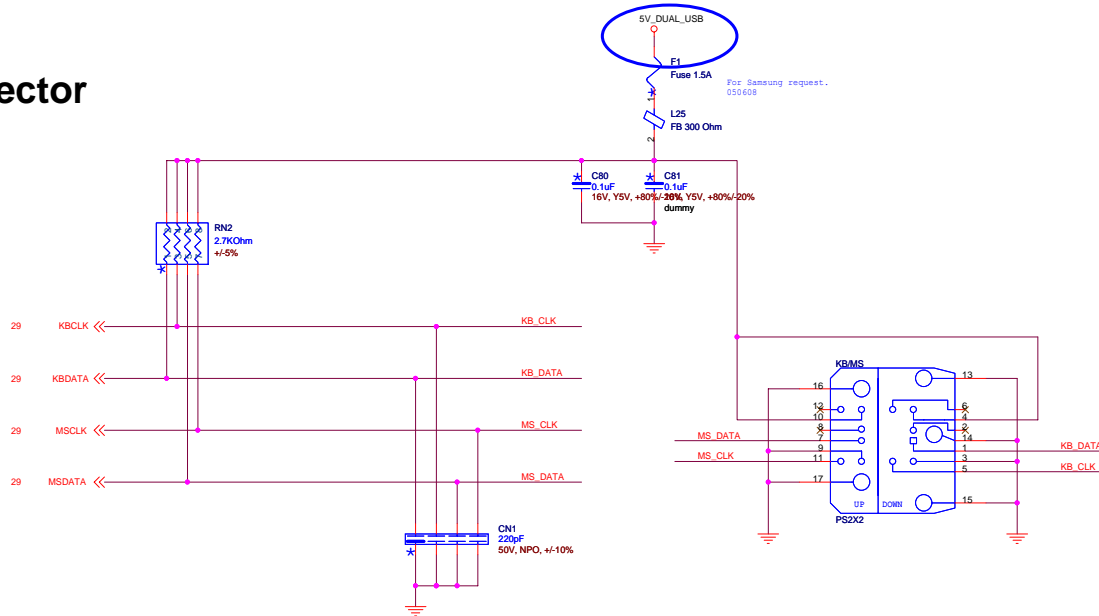
Peak fan current draw: 1.5A
 Average fan current draw: 1.1A
 Fan start-up current draw: 2.2A
 Fan start-up current draw maximum duration: 1.0 second
 Fan header voltage: 12V +/- 10%

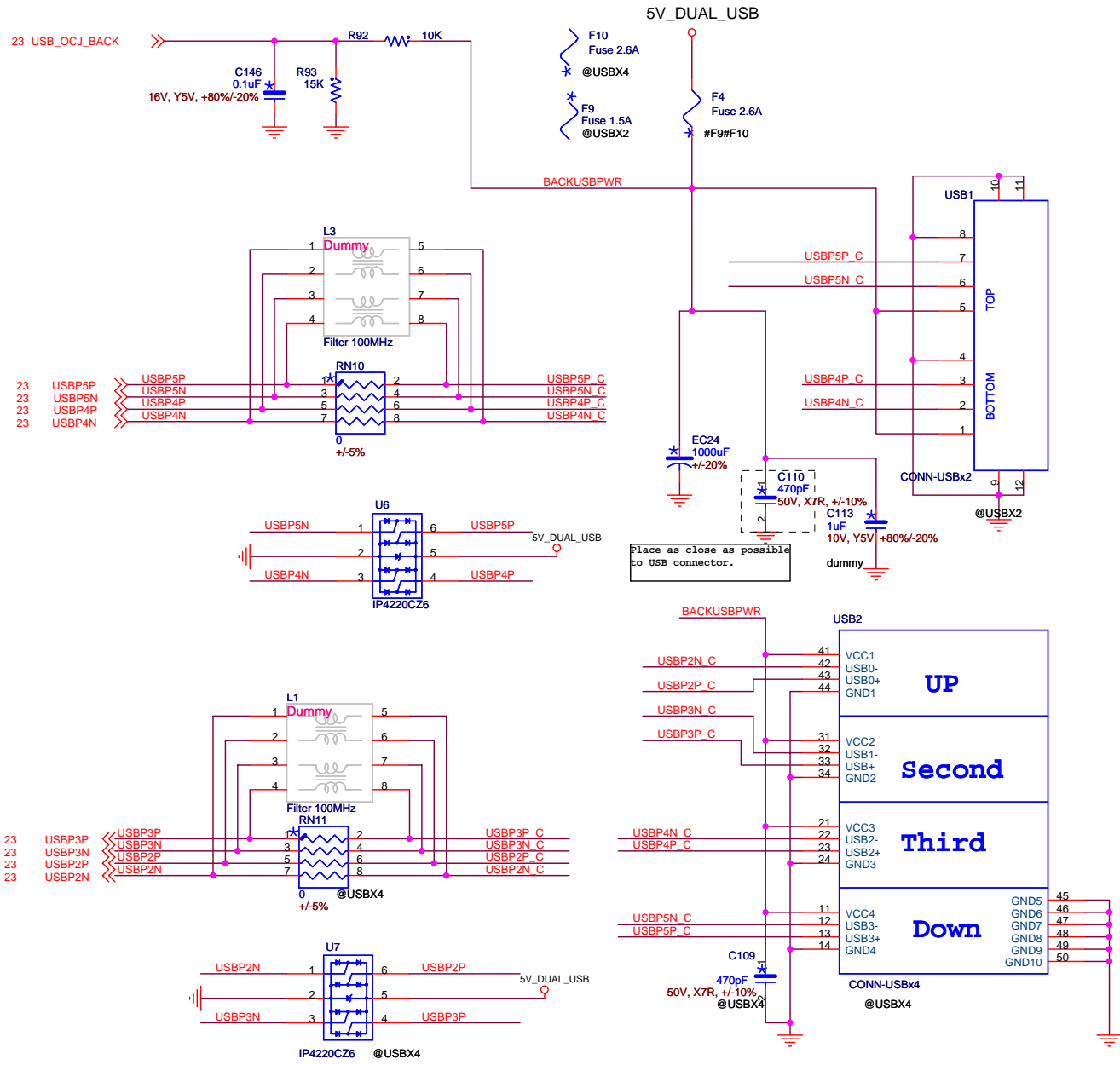
Del XDP Connector


TPM Connector



KB / MS Connector



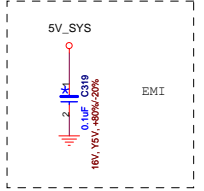
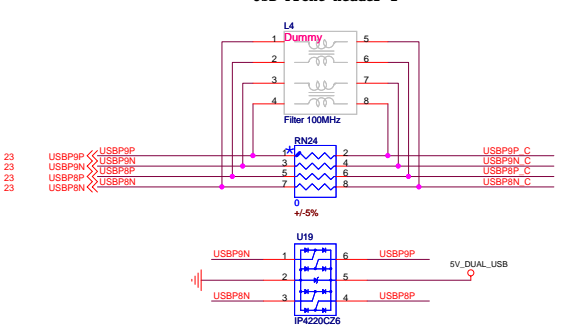
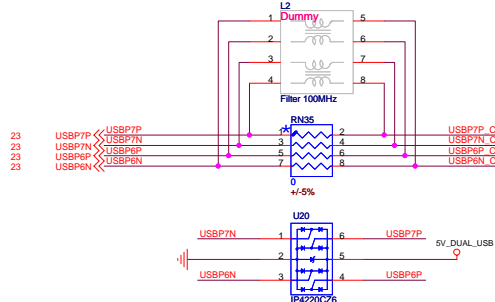
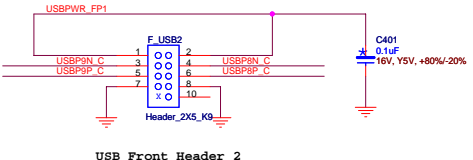
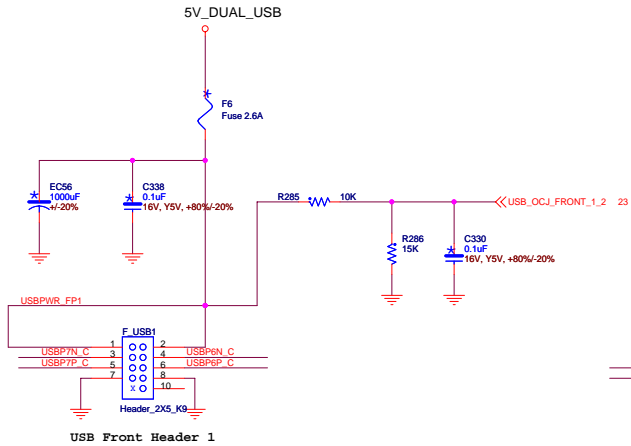
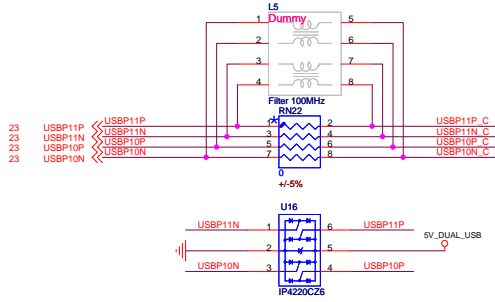
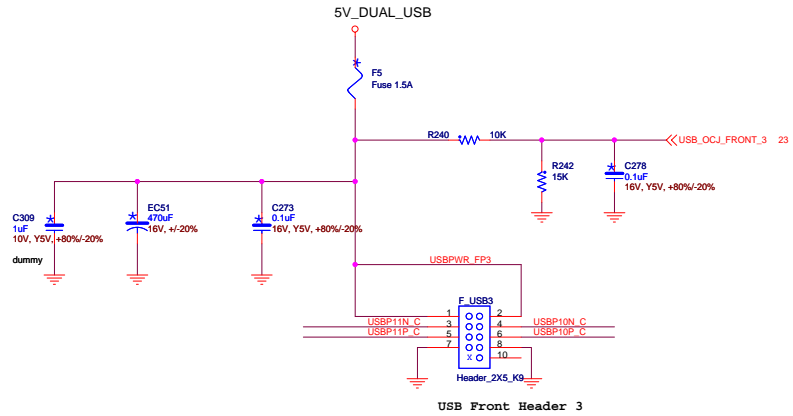




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Title		
LAN / USB Connectors		
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Del F_USB header 4

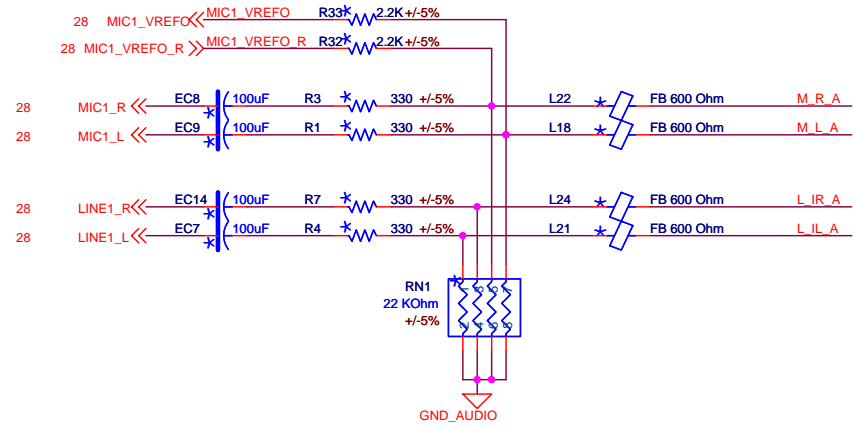


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Title: **Front USB Connector**

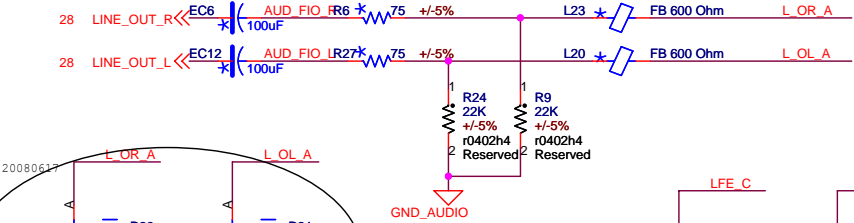
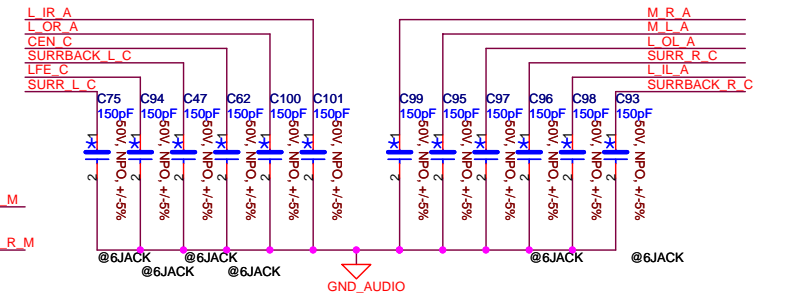
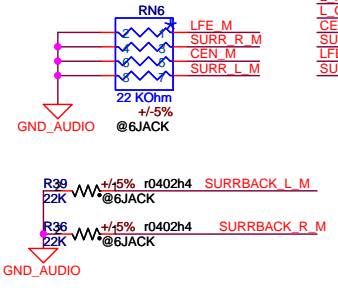
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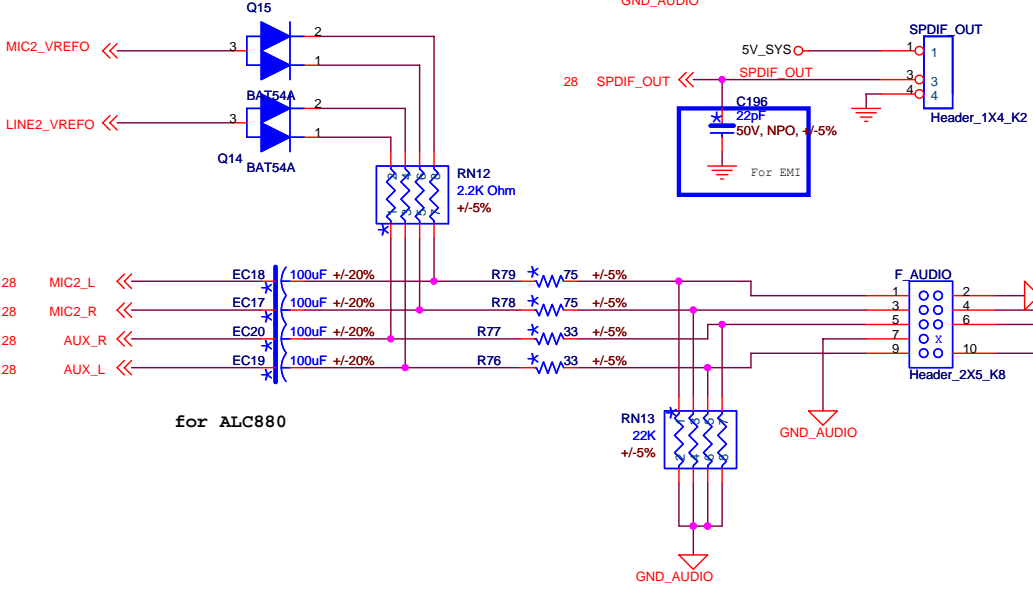
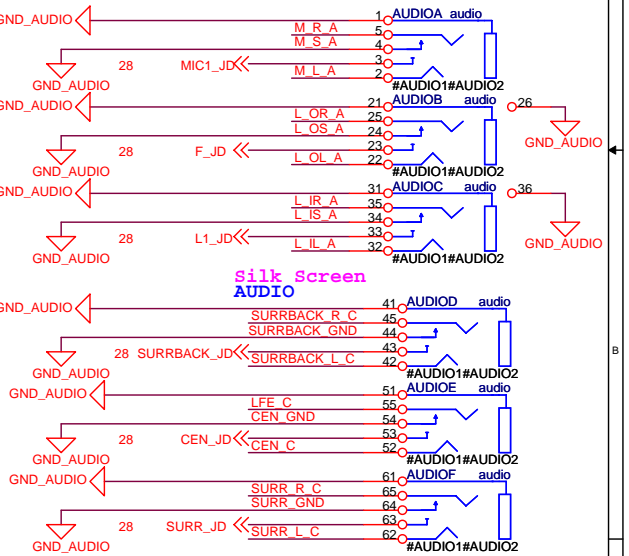
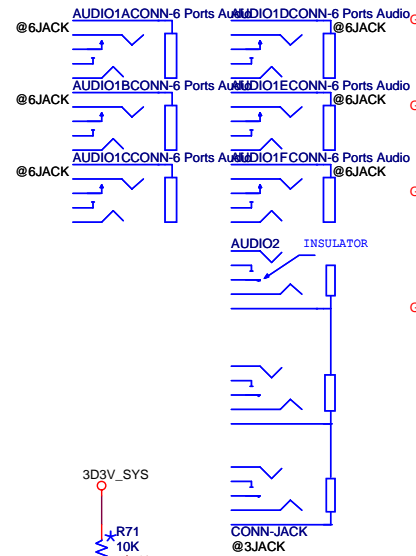
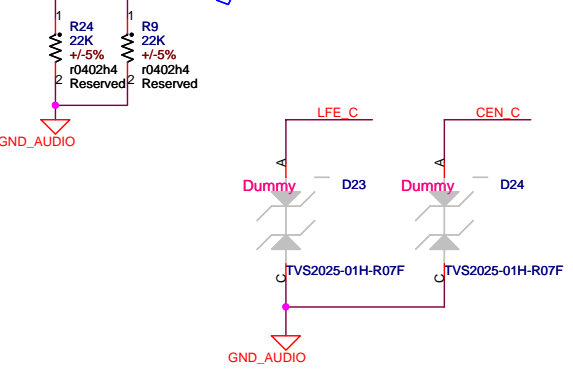
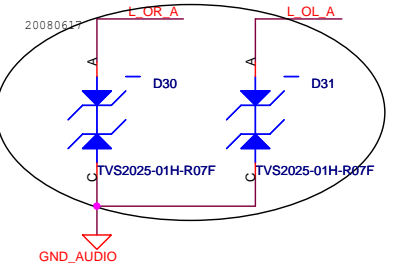


**AUDIO
MIC-IN**

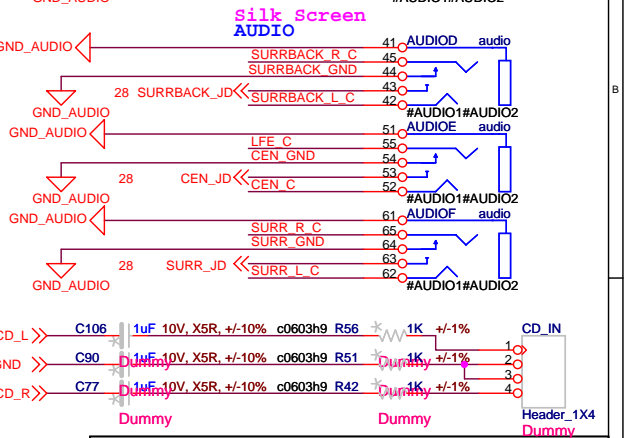
**AUDIO
LINE-IN**



**AUDIO
Front_OUT**



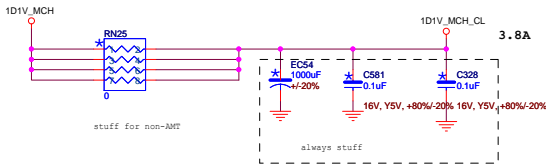
for ALC880



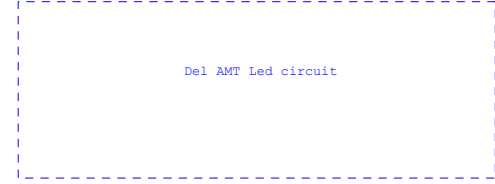
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HDA Audio Port			
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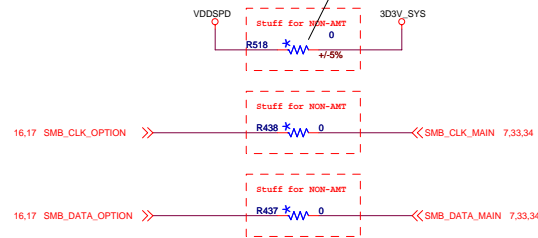
Del 1.1V MCH CL circuit
(1D8V_STR to 1D1V_MCH_CL)



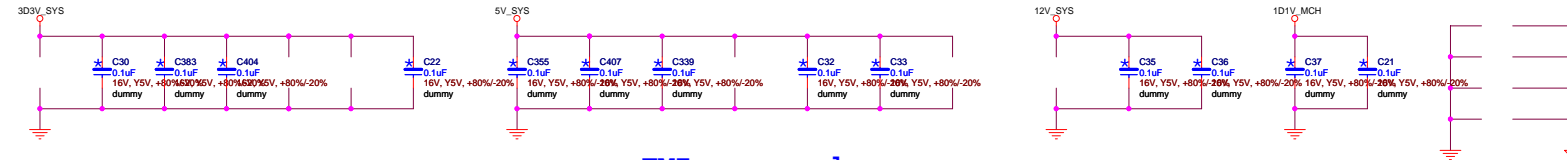
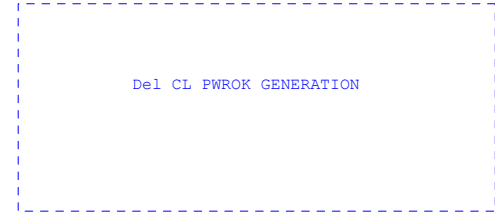
Del AMT Led circuit



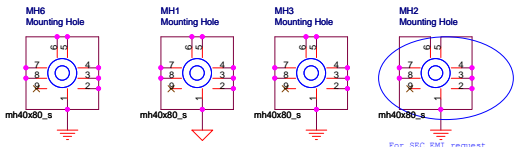
Change footprint to 0603



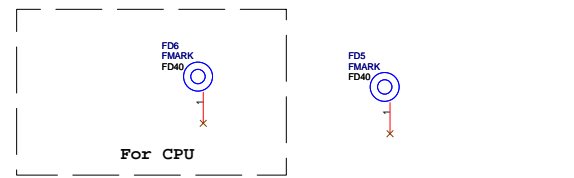
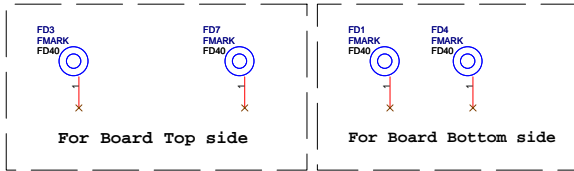
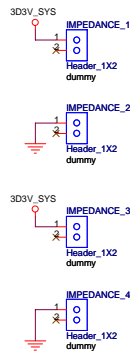
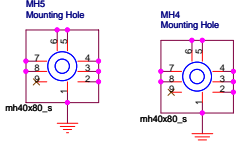
Del CL PWROK GENERATION



EMI reserved



MH footprint update to mh4x80_s for SEC only. 052208




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ICH10 GPIO Summary

Name	Power Well	Type	Description
GPIO0	3.3V	I/O	FP_AUD_DETECT
GPIO1	3.3V	I/O	TACH_1
GPIO2	5V	I/OD	PIRQE#
GPIO3	5V	I/OD	PIRQF#
GPIO4	5V	I/OD	PIRQG#
GPIO5	5V	I/OD	PIRQH#
GPIO6	3.3V	I/O	TACH_2
GPIO7	3.3V	I/O	TACH_3
GPIO8	3.3V_SB	I/O	Unused(pull-up)
GPIO9	3.3V_SB	I/O	WOL_ONLY
GPIO10	3.3V_SB	I/O	Unused(pull-up)
GPIO11	3.3V_SB	I/O	SMBALERT#
GPIO12	3.3V_SB	I/O	LAN_DISABLE#
GPIO13	3.3V_SB	I/O	L_PME#
GPIO14	3.3V_SB	I/O	Unused(pull-up)
GPIO15	3.3V_SB	I/O	CK_PCI_STOP
GPIO16	3.3V	I/O	Unused(NC)
GPIO17	3.3V	I/O	TACH_0
GPIO18	3.3V	I/O	Unused(NC)
GPIO19	3.3V	I/O	SATA_1GP
GPIO20	3.3V	I/O	Unused(NC)
GPIO21	3.3V	I/O	SATA_0GP
GPIO22	3.3V	I/O	Unused(pull-up)
GPIO23	3.3V	I/O	LDRQ1#
GPIO24	3.3V_SB	I/O	AMT_LED
GPIO25	3.3V_SB	I/O	CK_CPU_STOP
GPIO26	3.3V_SB	I/O	S4_STATE#
GPIO27	3.3V_SB	I/O	QRT_STATE0
GPIO28	3.3V_SB	I/O	QRT_STATE1
GPIO29	3.3V_SB	I/O	USB_OC3_FRONT#
GPIO30	3.3V_SB	I/O	USB_OC4_FRONT#
GPIO31	3.3V_SB	I/O	USB_OC4_FRONT#
GPIO32	3.3V	I/O	Unused(NC)
GPIO33	3.3V	I/O	MFG
GPIO34	3.3V	I/O	Unused(NC)
GPIO35	3.3V	I/O	Unused(NC)
GPIO36	3.3V	I/O	SATA_2GP
GPIO37	3.3V	I/O	SATA_3GP
GPIO38	3.3V	I/O	Unused(pull-up)
GPIO39	3.3V	I/O	Unused(pull-down)
GPIO40	3.3V_SB	I/O	USB_OC1_FRONT#
GPIO41	3.3V_SB	I/O	USB_OC2_FRONT#
GPIO42	3.3V_SB	I/O	USB_OC2_FRONT#
GPIO43	3.3V_SB	I/O	USB_OC3_FRONT#
GPIO44	3.3V_SB	N/A	USB_OC_BACK#
GPIO45	3.3V_SB	N/A	USB_OC_BACK#
GPIO46	3.3V_SB	N/A	USB_OC_BACK_LAN#
GPIO47	3.3V_SB	N/A	USB_OC_BACK_LAN#
GPIO48	3.3V	I/O	Unused(pull-up)
GPIO49	3.3V	I/O	DMF_STRAP(pull-down)
GPIO50	5.5V	I/O	REQ_1#
GPIO51	3.3V	I/O	Unused(NC)
GPIO52	5.5V	I/O	REQ_2#
GPIO53	3.3V	I/O	Unused(NC)
GPIO54	5.5V	I/O	REQ_3#
GPIO55	3.3V	I/O	Unused(NC)
GPIO56	3.3V_SB	I/O	Unused(pull-up)
GPIO57	3.3V_SB	I/O	Unused(pull-up)
GPIO58	3.3V_SB	I/O	Unused(pull-up)
GPIO59	3.3V_SB	I/O	USB_OC1_FRONT#
GPIO60	3.3V_SB	I/O	Unused(pull-up)

PCI Routing Summary

	PCI1				
INTAJ	F				
INTBJ	G				
INTCJ	H				
INTDJ	E				
INTEJ					
INTFJ					
INTGJ					
INTHJ					
REG#/GNT#	0				
IDSEL	16				



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Title: **GPIO / IRQ / IDSEL Map**

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Change history

FAB-B change

Date: May 9, 2008

1. PG 07: Change R154, R157 from 33 Ohm to 1K Ohm
2. PG 08: Add PSI control circuit for Wolfdale and Yorkfield CPU
3. PG 10: Add R310 51 Ohm, dummy L34, L35, EC39, R308, R348
4. PG 12: Dummy R185
5. PG 19: Reserve EC73, EC74; Connect VBAT pin of U23 to VCCRTC.
6. PG 29: Dummy R549, R566, RN51
7. PG 32: Add Q67, R597, R598 with 2N3904, 1KOhm, 1KOhm repectively
8. PG 34: Change KB/MS Power from 5V_SB_SYS to 5V_Dual_USB
9. PG 39: Add RN23, RN26 from 2.7KOhm

EV2 to PV1 change

Date: June 17, 2008

1. PG 09: Dummy R390,R388,C372,R342,R375,R376,C361,R341,Reserve R439,R440,R431,R422,R427,R428,R430,R423,R411,R377,R340,Q44,Q45,Q46,Q47, Change R439 from 10K Ohm to 1K Ohm
2. PG 19: Add D32,R602,R601(dummy) Change R477 from 21K Ohm to 20K Ohm,Change R268 from 24.9K Ohm to 15K Ohm
3. PG 25: Change R460 from 10 Ohm to 100 Ohm
4. PG 37: Add D30,D31
5. PG 39: Add Q32,Q35,Q65,Q67

PV1 to PV2 change

Date: July 10, 2008

1. PG 14: Add C603,C604
2. PG 19: Reserve D32,R551,Add R208,C14,R604,R605,R606,R607,R608,Q73,Change C465 from 0.22uF Ohm to 0.47uF
3. PG 23: Add R415
4. PG 29: Add R597(dummy),Reserve R558

PV2 to PR change

Date: July 23, 2008

1. PG 32: Change C527 from 0.1uF to 1uF



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File		
History		
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