FIRST RESET SIGNAL ON LAPTOP MOTHERBOARD

By Adie Dkhaz on Sunday, March 8, 2015 at 8:00pm

RSMRST#
When the Power,Bios,Ec are OK, the RSMRST# will go Hi. In the other word,this pin go Low only when the systemreset.If BIOSdata is error,RSMRST# won't go HI.
When SIO(EC) get +V_RTC
thecrystal will work.

1. **RTC have to be oscillating(32.768KHz).**
2. **RTCRST# have to be high.**
3. **RSMRST# have to be inactive (high).**
4. **PWRBTN# have a trigger.**
5. **LOW_BAT# have to be inactive (high).**

If true, thenEC will recieve SLP_S3# / SLP_S5 from ICH/PCH, in the old ICH or some deferent circuirity SLP_S3 and SLP_S5 will generate directly from ICH,or both EC and PCH having this signal also.
When All+V?S/+V? powers are ready, PWR_GOOD will tie to high to turn on CPU powers(+VCCP and +VCC_CORE).

SB/PCH Power good--->SB/PCH pwr_btn--->PCH RUN
SUSB## from PCH toSIO pullup the signal SLP_S3# The signal is usedto shut power off /on through logic gate transistor or IC

SUSC# from PCH toSIO pullup the signal SLP_S5# The signal is usedto shut power off /on through logic gate transistor or IC

ICH/SB,MCH & CPU
IMVP_PWRGD => CLK_ENABLE# => RESET_OUT#=> ICH_PWRGD => PLTRST# => PCI_RST=> H_PWRGOOD

CPU generate the first cycle to read the BIOS code
CPU bus DMI LPC SPI
CPU ===> GMCH===> ICH===>SIO ===> BIOS

CPU MASTER POWER

VR_ON Enable--->+VCCORE 08VS to 1,5VS
Memory +VTT and +V1.5VS (DDR3) is ok, the PGOOD VTT_PWRGD pull high to CPU
First nd ICH will tie H_PWRGD to high ,then NB will tieCPURST# to reset CPU.

Crystal clock Oscilator CLOCK SUMMARY

(1) 32.768KHz to SIO Required +V_RTC and to ICH(chipset) also Required +V_RTC
(2) 49.152MHz to (audio controller) Required +V3S
(3) 27MHz : to Graphicchip (video controller)Required +V3S
(4) 14.318MHz : X1 to (clock Generator) Required +V3S

Make sure crystal is oscillating for EC(SIO),SB/ICH/PCH and VGA or it will no post

Clock Generator
Elementary required
1) Power : +V3S
(2) Crystal : 14.318MHz
(3) Control : PCISTOP# , CPUSTOP#_ is HI
When +VCC_CORE is ready, CLKEN#will go high to enable clock-Generator and turn all clock.
PCI_STOP# and CPU_STOP# must beat high otherwise some clocks will be turned off.

Clock out -->SIO(EC)-->PCH/SB-->NB-->CPU

LPC_Frame-->SB output signal is high

Note High signal can be identified by measuring 3.3V available