2012 EU ALSA Training
F1A75, A55 Series

GRMA Brain_HUNG

F1A75&A55 Series – Agenda

- AMD Fusion Platform Structure
- Critical Power Flow
- Clock Distribution
- Power Sequence
- Repairing Experience Sharing (00)
- Repairing Experience Sharing (all dots)
- Fusion Platform Complement

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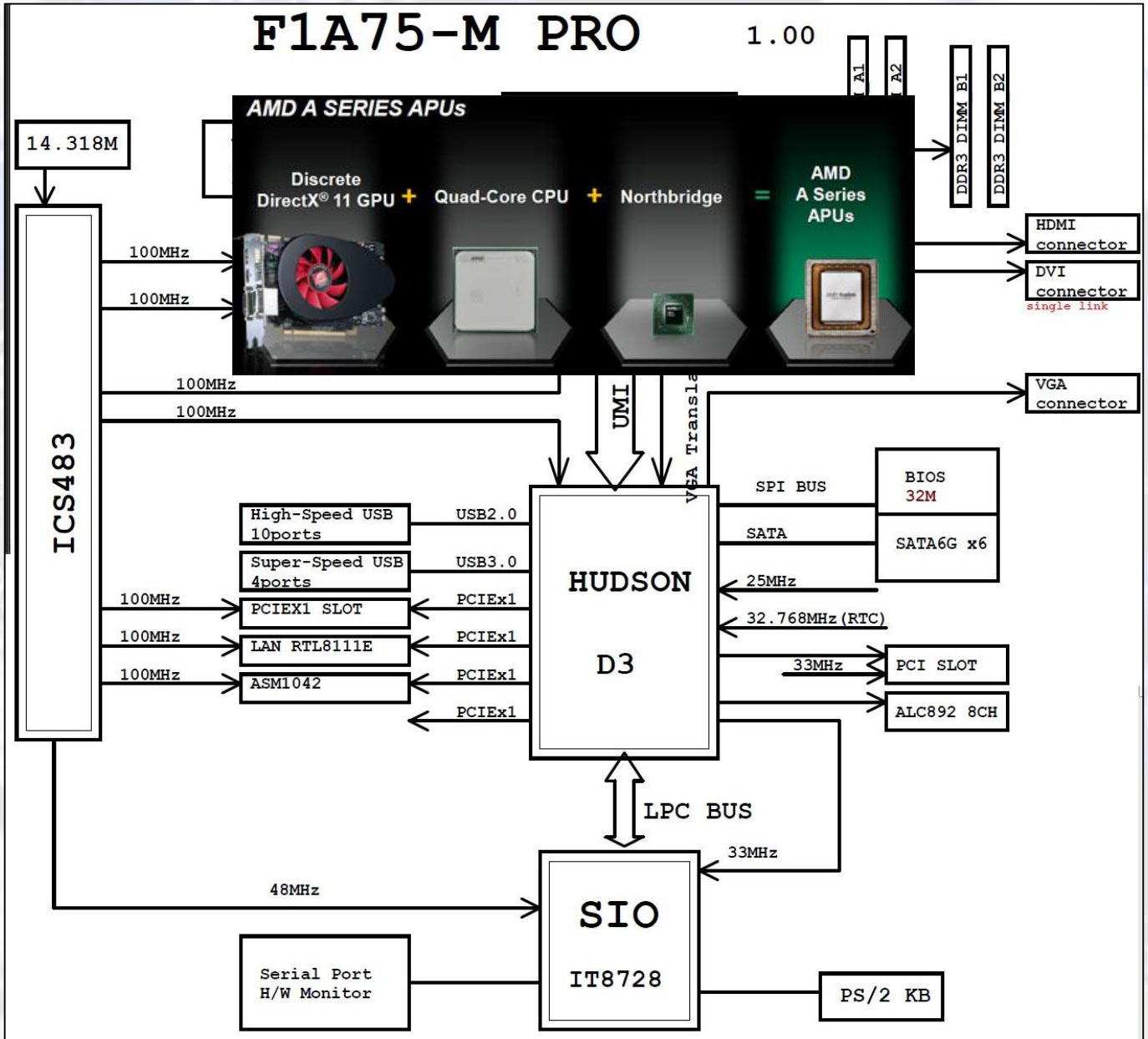
AMD Fusion Platform Structure



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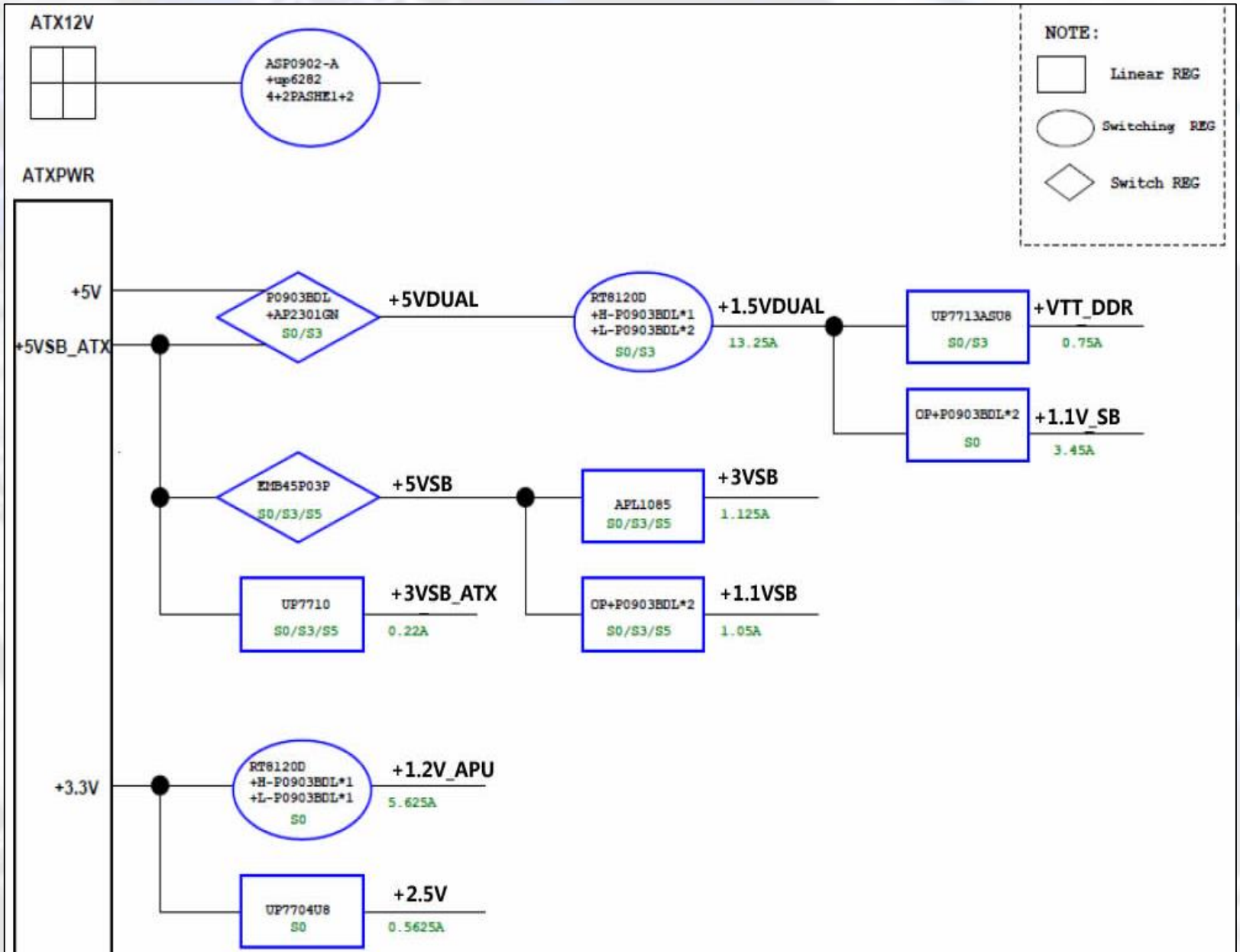
F1A75&A55 Power Flow



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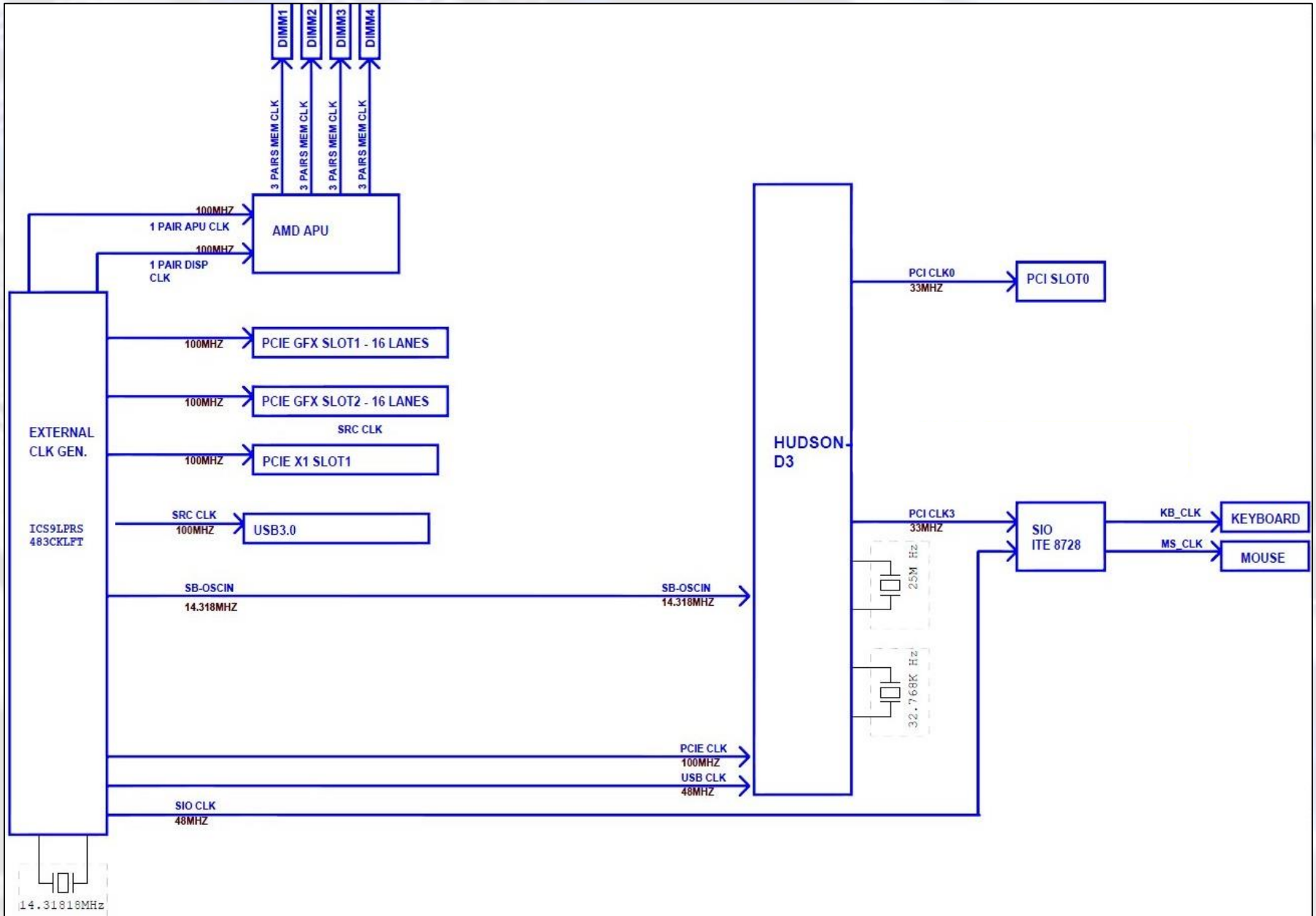
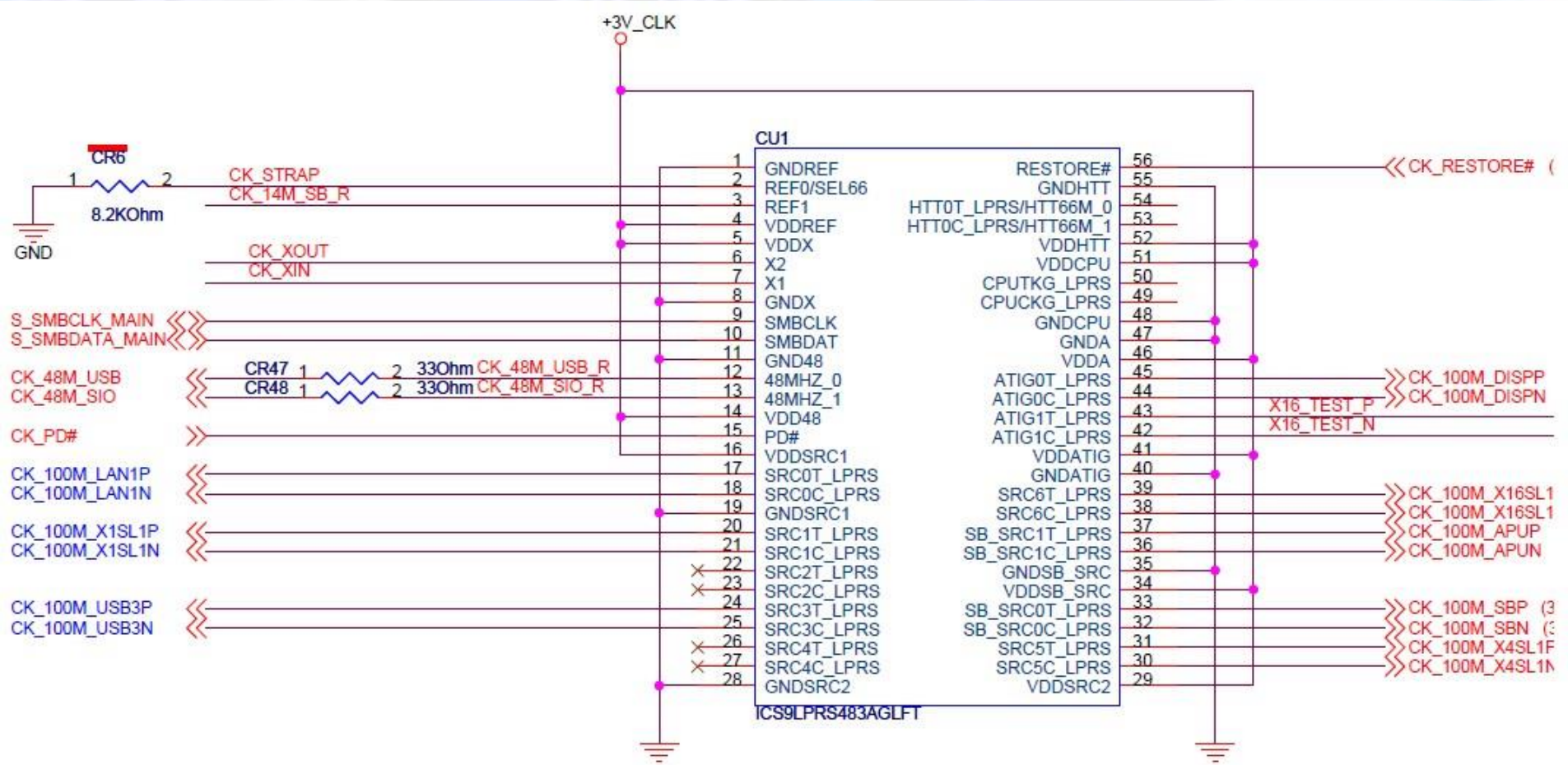
Frequency Distribution (F1A75-M)



Frequency Distribution (F1A75-M)



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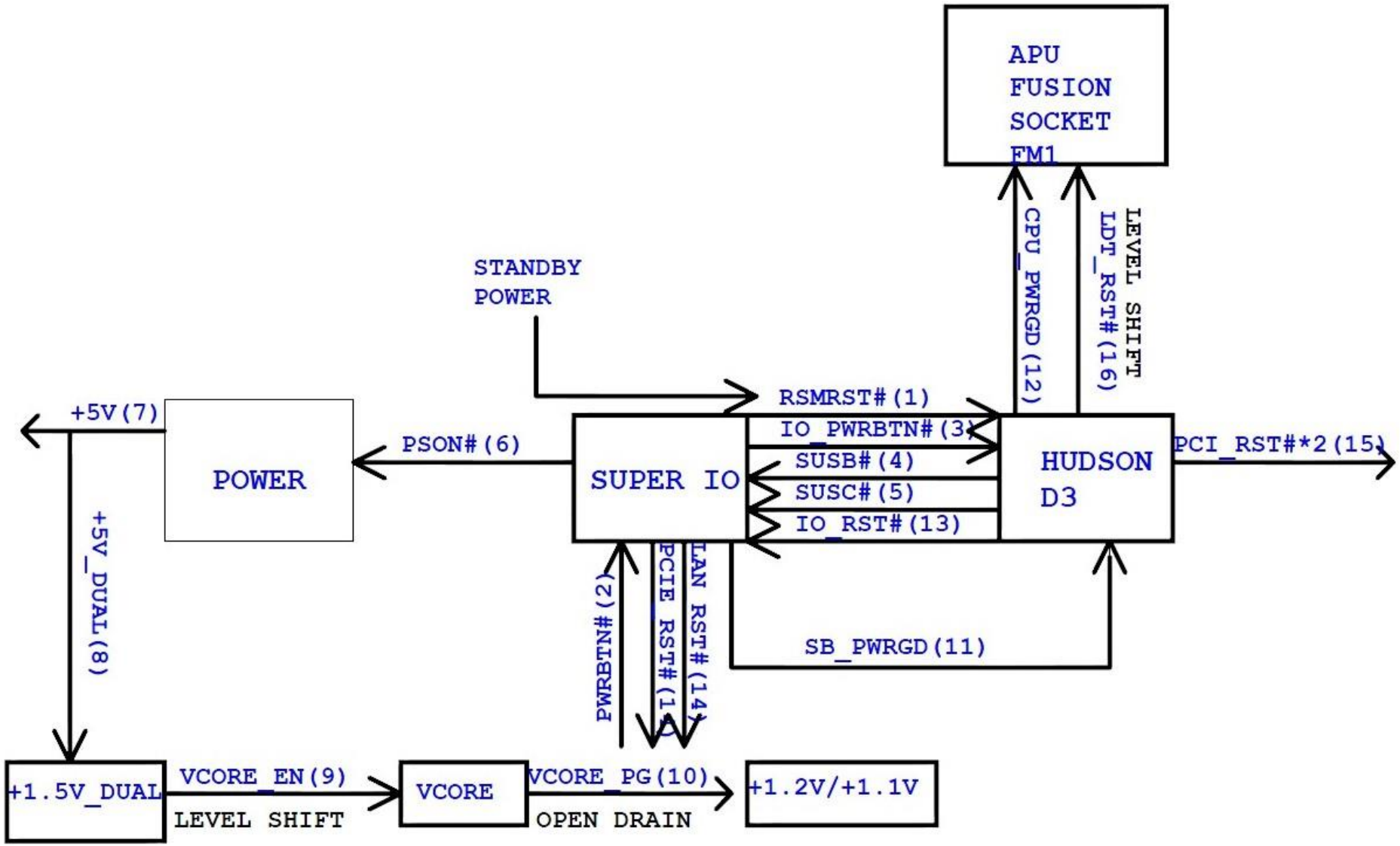
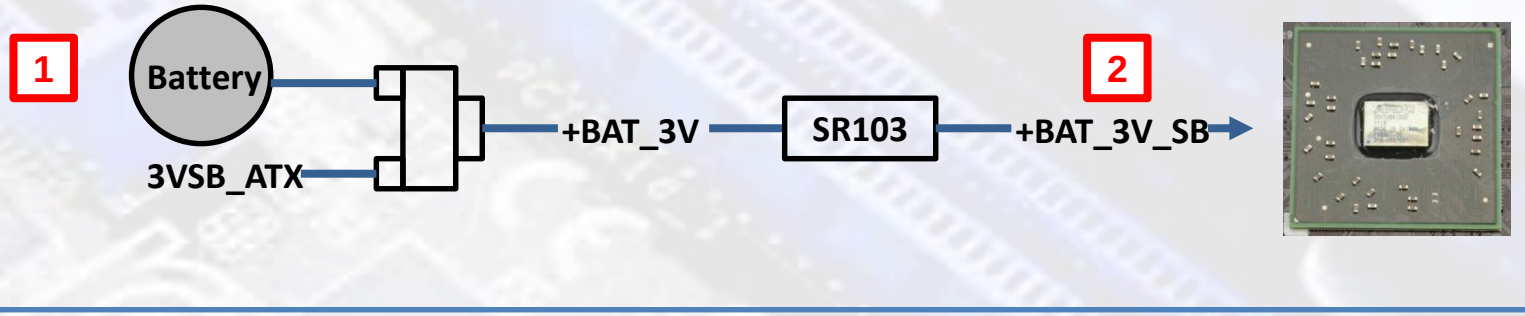
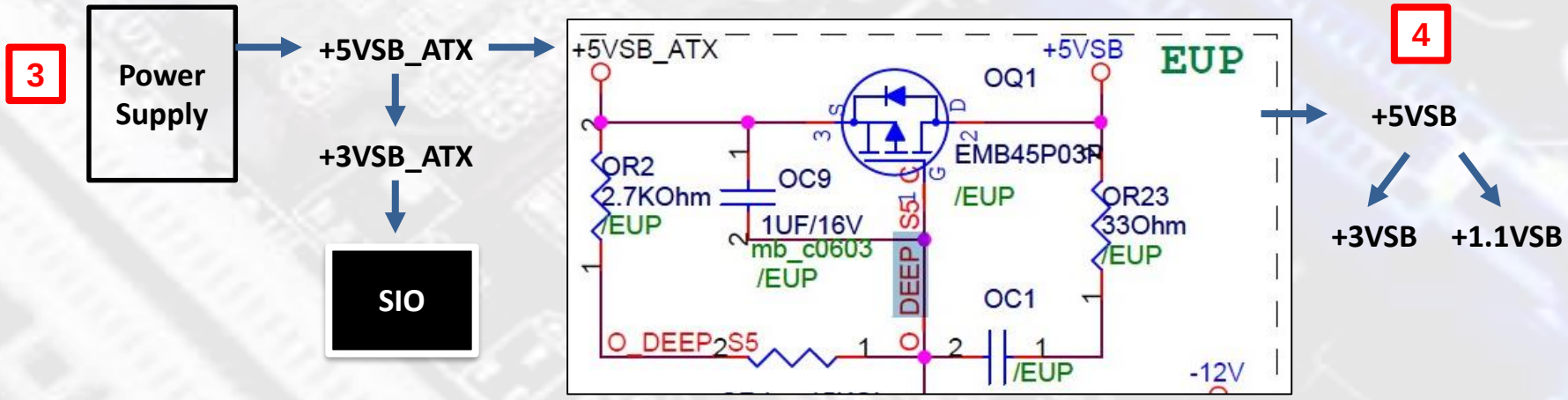
Power Sequence

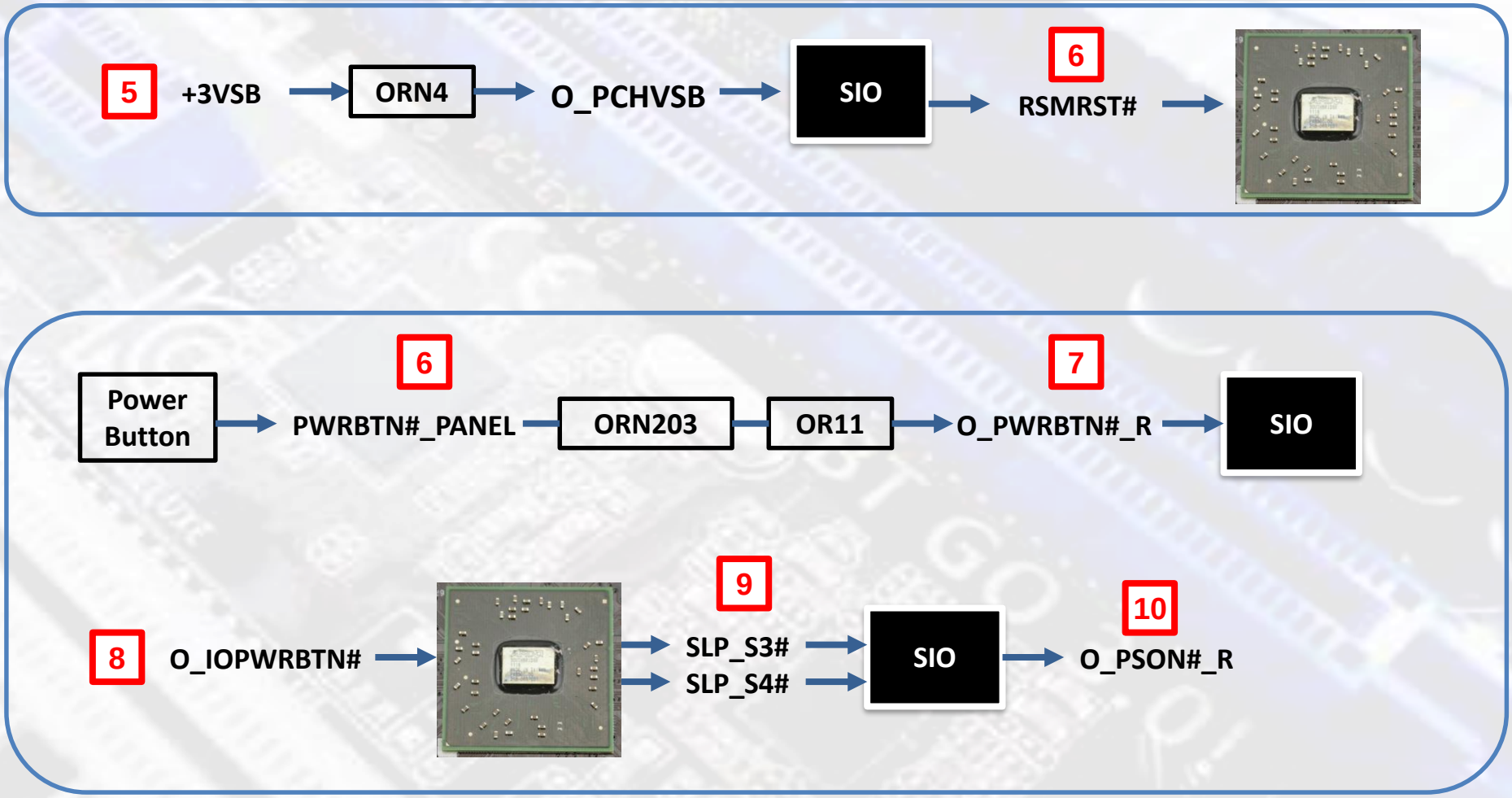


Power Sequence (F1A75-M)



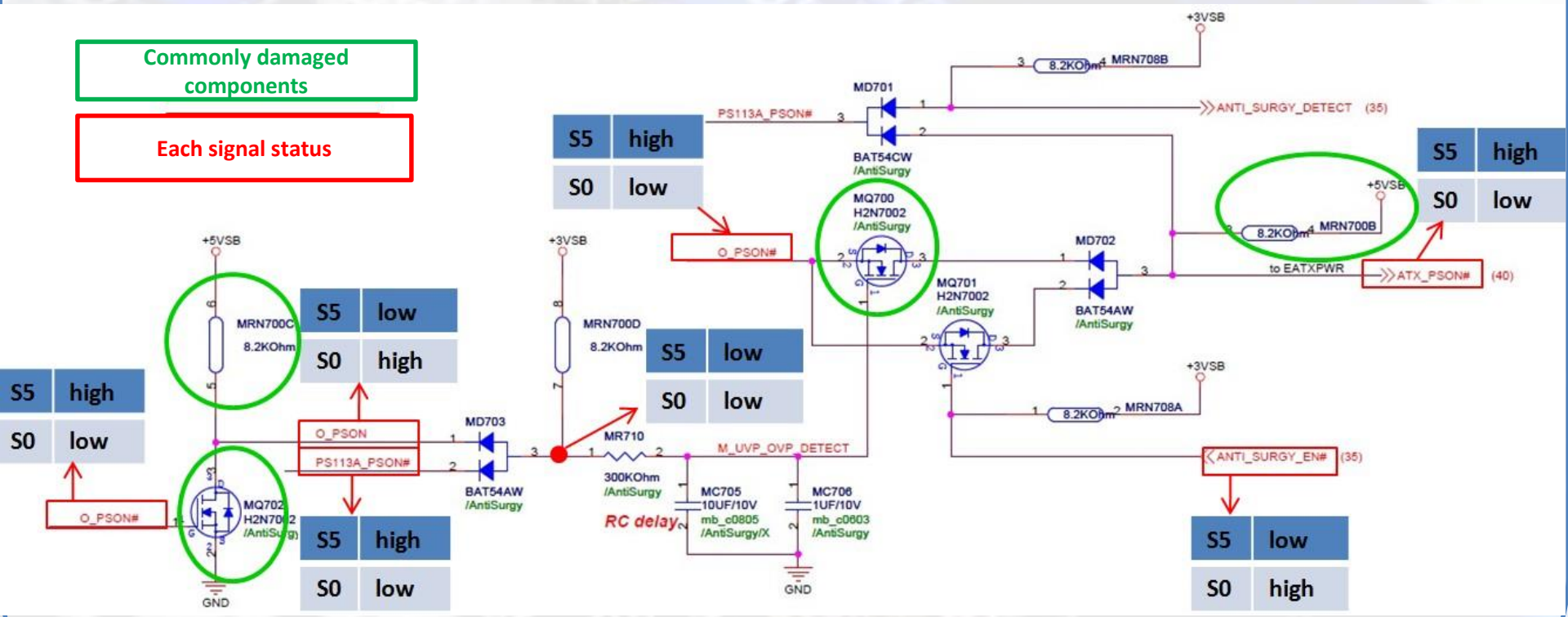


Power Sequence (F1A75-M)



Power Sequence (F1A75-M)

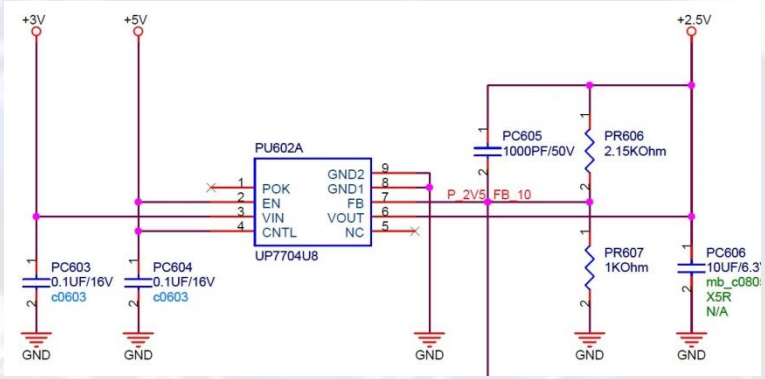
SIO → O_PSON#_R → OR13 → O_PSON#



Power Sequence (F1A75-M)

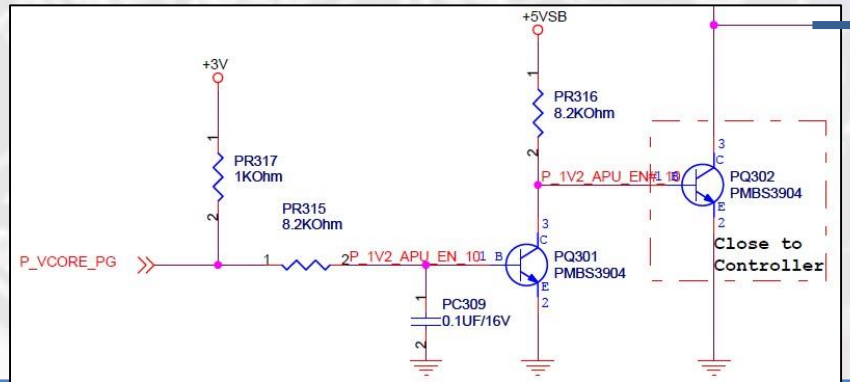
9 ATX_PSON# → Power Supply → 10 3V, 5V, 12V → MB Circuit → DUAL POWER / Chipset POWER / Others POWER

3V → MB Circuit → +2.5VDDA



11 +1.5VDUAL → MB Circuit → 12 P_VCORE_EN → VCORE IC → VCORE

13 VCORE IC → VCORE_PG

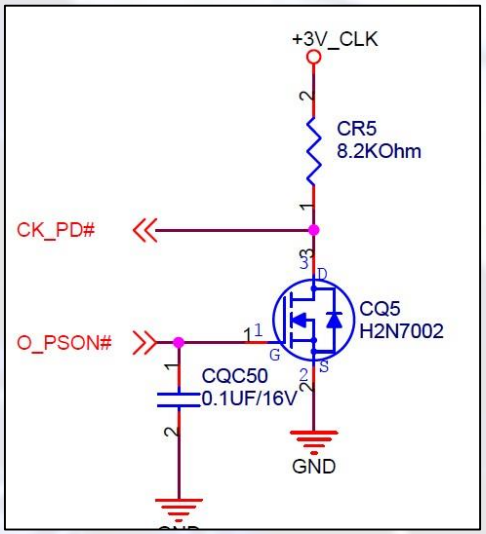


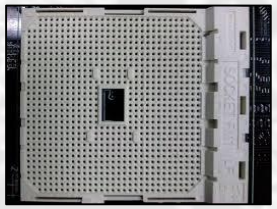
MB Circuit → 14 +1.2V_APU

Power Sequence (F1A75-M)

After PSON# →

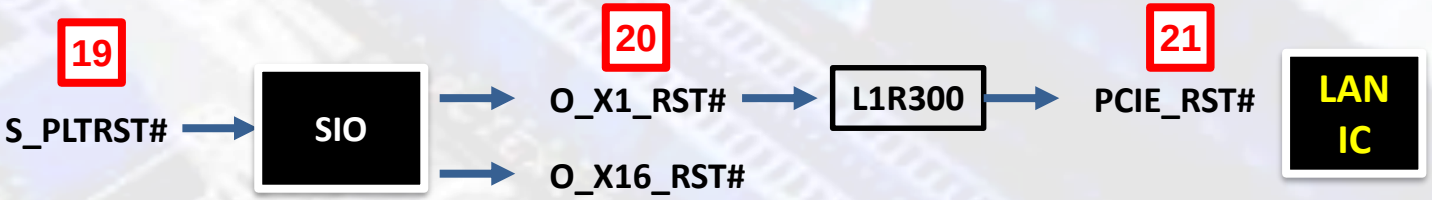
15 SIO → O_PWROK_SB

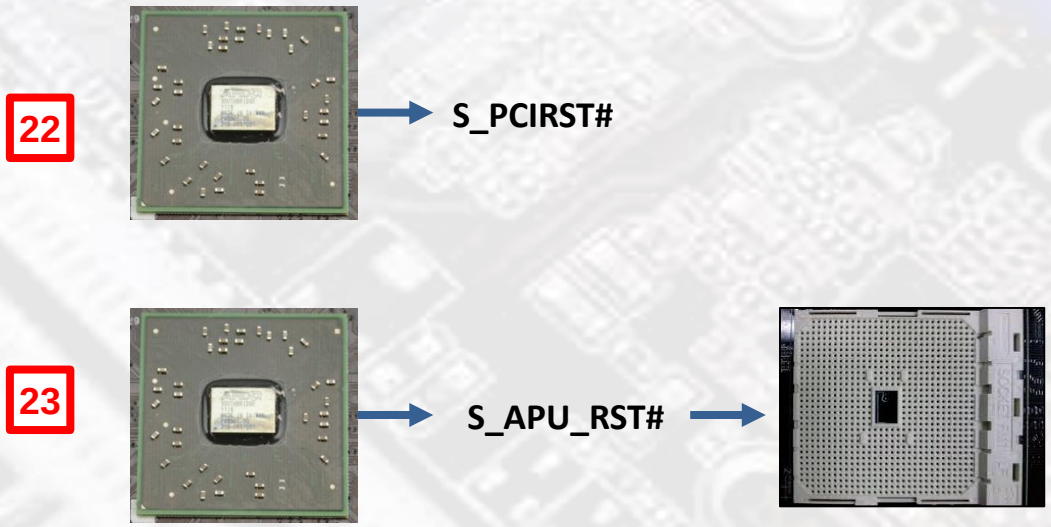


16  → S_APU_PWROK →  → 17 SVID → VCORE IC

18  → S_A_RST#_R → SR2 → 19 S_PLTRST# → SIO

Power Sequence (F1A75-M)





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- **Repairing Experience Sharing (00)**
- Repairing Experience Sharing (all dots)
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Repairing Experience Sharing (00)

◆ F1A55-M LE: 00

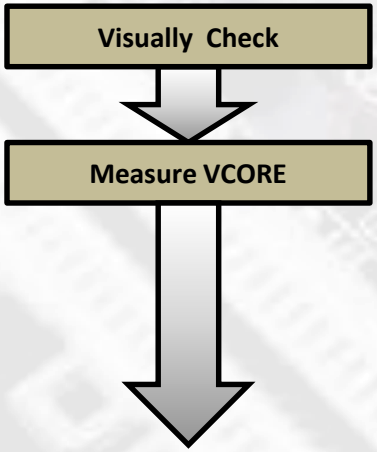
MB Type	L1 Problem Description	Needed materials situation	L2 Problem Description	Signal	Position Number
F1A55-M LE	00	SU1			

The Initial Problem Analysis:

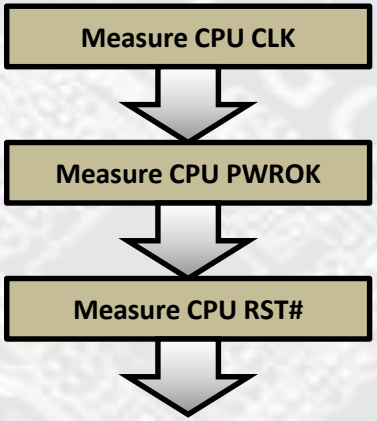
1 : Visually check MB slot for damage. Check front and back of the board for line breaks.

2: Check SX1 if it has 32.768KHZ,POU601 PIN:2 3VSB, OU2 PIN:4 3VSB_ATX。

3: After plugging in power supply and power on, the debug card shows 00



1.+1.5V_DUAL PL511 PIN2
2.VCORE 1.1V PL141 PIN2
3.VDDNB 1.1V PL221 PIN2
4.+1.2V_APU PL311 PIN1
5.+2.5V_VDDA HR19 PIN2



1.CK_100M_APUN,CK_100M_APUP
2.CK_100M_DISPP, CK_100M_DISPN

S_APU_PWROK 1.5V HQ2 PIN3

S_APU_RST# 1.5V , SU3 PIN1
(Trigger RSTCON# and S_APU_RST# can be reset)
All CPU condition are all normal so it can consider as “00”

Repairing Experience Sharing (00)

1.+3VSB
2.+3V SL4 PIN1
3.+3V_BAT_SB SC18 PIN1
4.+1.1VSB PQ902 PIN3
5.+1.1V_SB
6.S_1.1VSB_PLL_CLK SL5 PIN
7.+1.1VSB_USB3 SL9 PIN2
8.S_3V_PLL_CLK SL4 PIN2
9.S_3V_PLL_PCIE SL1 PIN2
10.S_3V_PLL_SATA SL2 PIN2
11.S_3V_PLL_VGA SL10 PIN2
12.S_3VSB_PLL_USB SL6 PIN2
11.S_3VSB_PLL_USB3 SL12 PIN2

1.25MHz SX2
2.S_CK_14M_SB SR37 PIN2
3.CK_100M_SBP,
CK_100M_SBN SC22,SC23 PIN1
4.CK_48M_USB SC27 PIN1

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Repairing Experience Sharing (all dots)

◆ F1A55-M LE: ALL DOTS

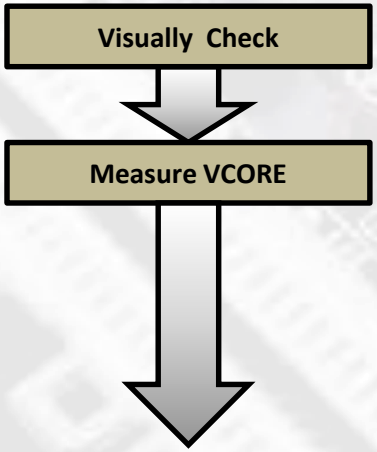
MB Type	L1 Problem Description	Needed materials situation	L2 Problem Description	Signal	Position Number
F1A55-M LE	All dots			S_APU_PWROK	HRN3

The Initial Problem Analysis:

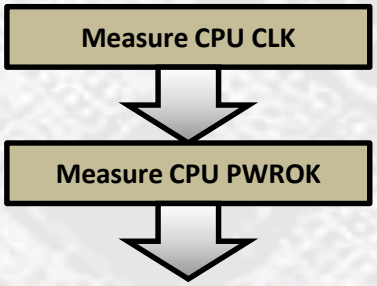
1 : Visually check MB slot for damage. Check front and back of the board for line breaks.

2: Check SX1 if it has 32.768KHZ,POU601 PIN:2 3VSB, OU2 PIN:4 3VSB_ATX。

3: After plugging in power supply and power on, the debug card shows all dots



1.+1.5V_DUAL PL511 PIN2
2.VCORE 1.1V PL141 PIN2
3.VDDNB 1.1V PL221 PIN2
4.+1.2V_APU PL311 PIN1
5.+2.5V_VDDA HR19 PIN2



1.CK_100M_APUN,CK_100M_APUP
2.CK_100M_DISPP, CK_100M_DISPN

S_APU_PWROK 1.5V HQ2 PIN3 has no power

Repairing Experience Sharing (all dots)

CLK Check

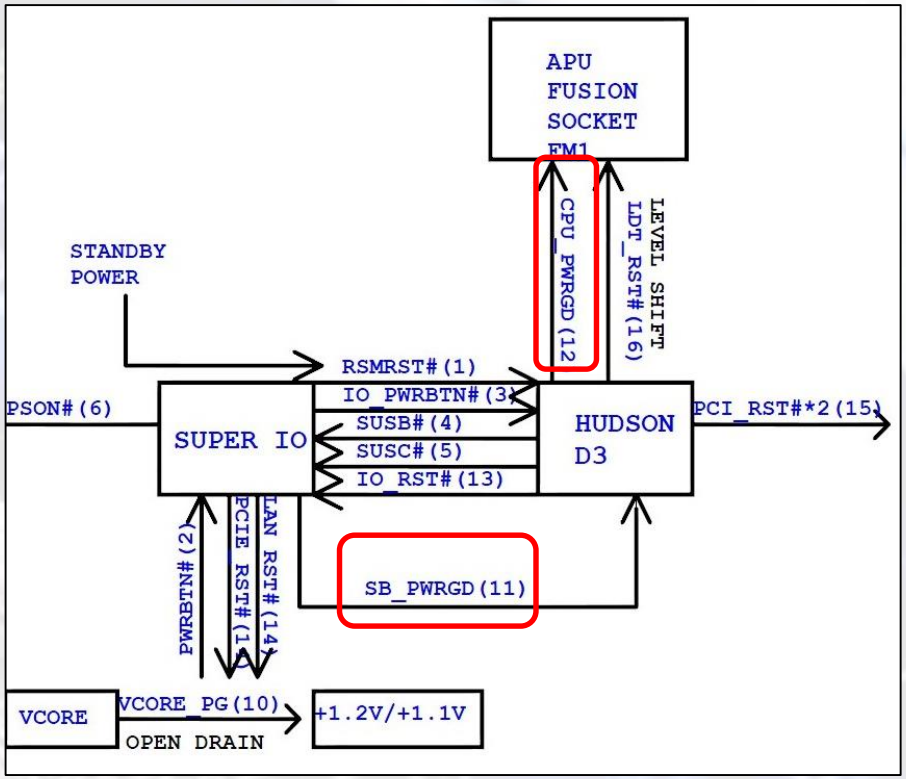
1.CK_100M_SBN
2.CK_100M_SBP
3.CK_14M_SB
4.CK_48M_SIO

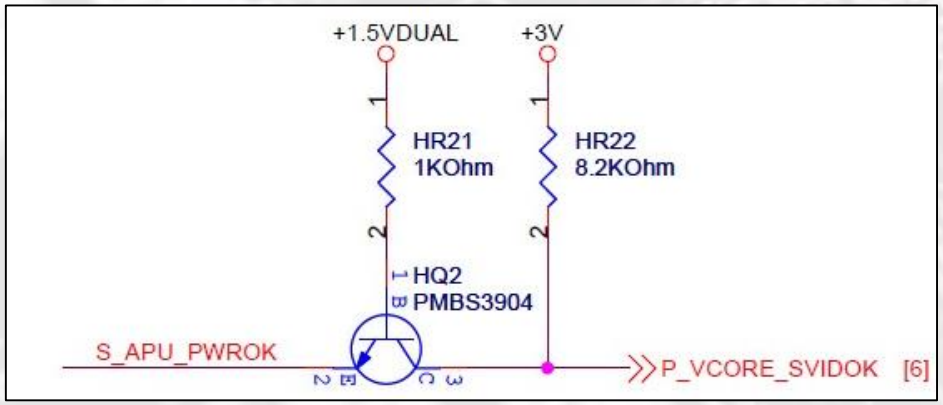
Measure PWROK Signals

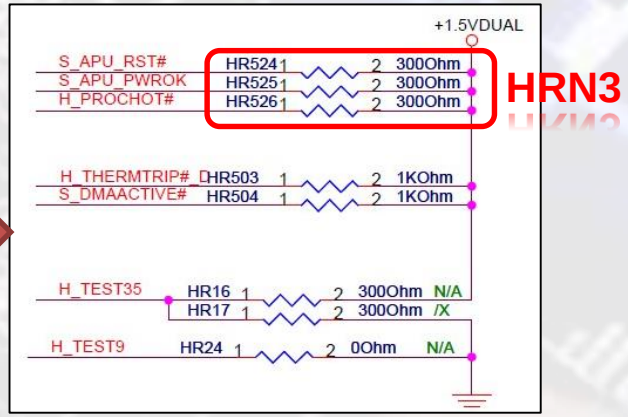
O_PWROK_SB is normal

Measure HQ2

PIN1 has 1.5V
Try to replace HRN3 to solve this problem.







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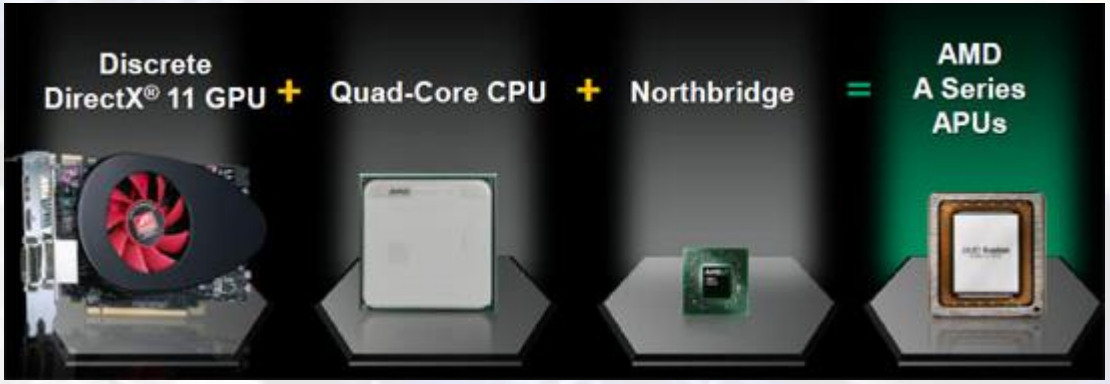
AMD Fusion Complement

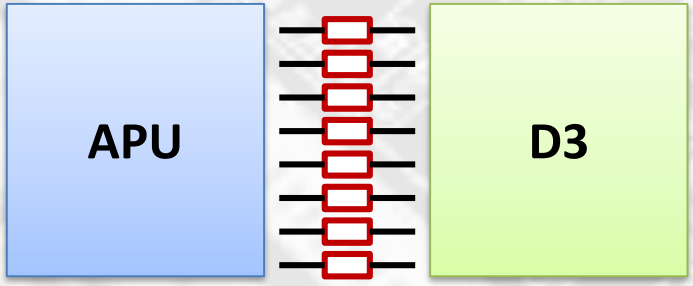
“APU” (short for Accelerated Processing Unit) technology.

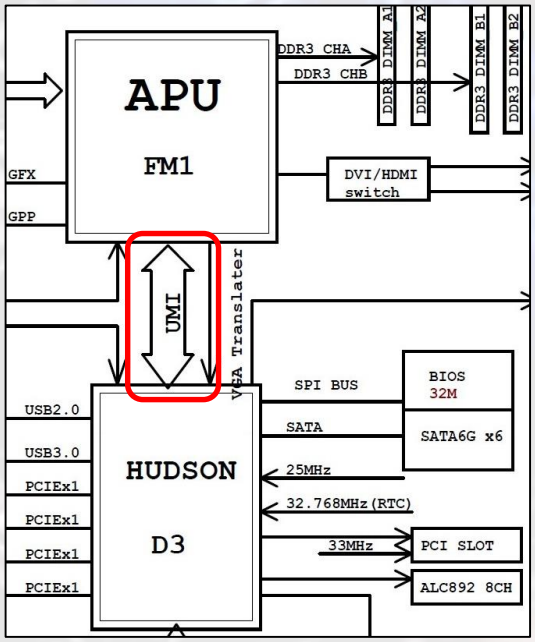
The short version of this is that AMD basically mashed together a high performance CPU and a high performance GPU into one tiny, fast, energy sipping chip.



UMI: Unified Media Interface

In FM1 structure, it’s for communication bus between D3 and APU.





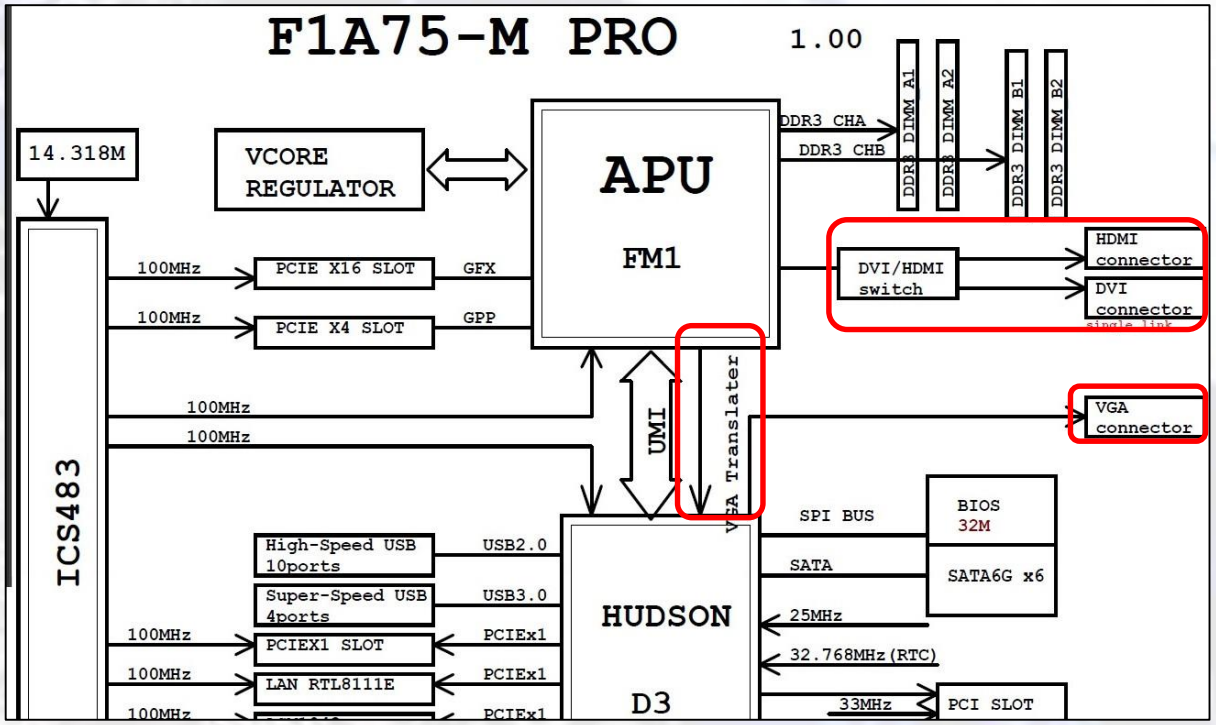
AMD Fusion Platform Structure

A. DVI Interface (Digital):

Connected with CPU and controlled by CPU directly.

A. VGA Interface (Analogy):

Connected with SB and through “VGA Translator Bus” to communicate with CPU and controlled by CPU.



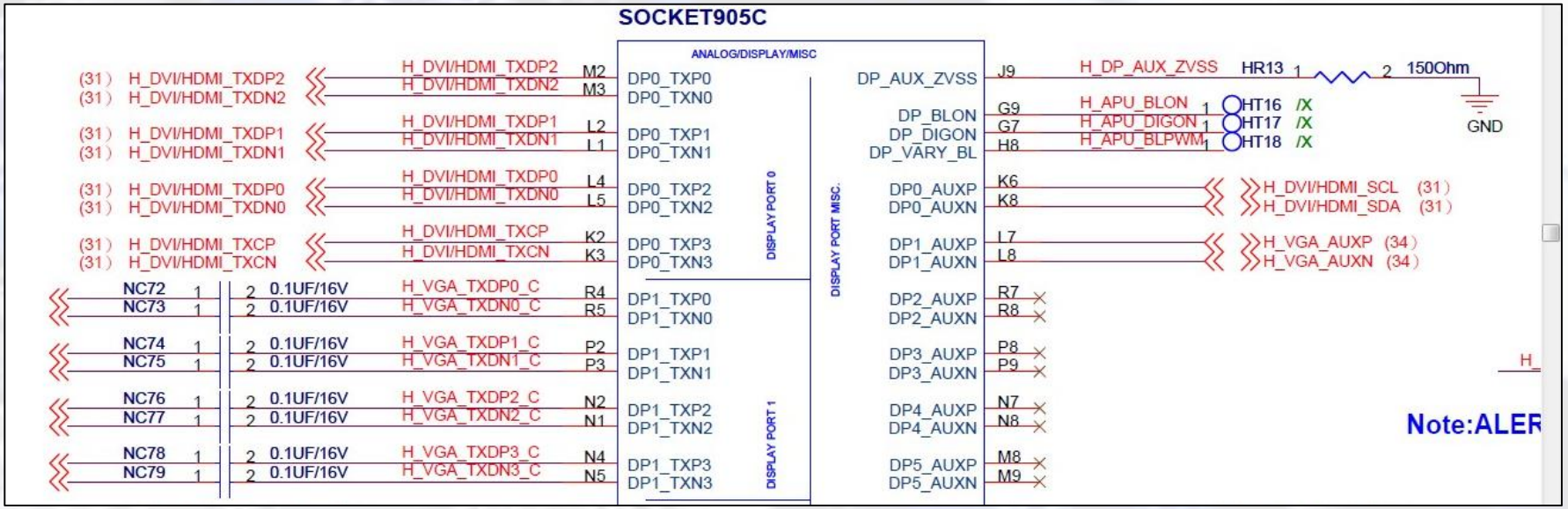
H_VGA_TXN[0:3], H_VGA_TXP[0:3] connected with SB side, the ground impedance is 942；

H_VGA_TXN_C[0:3], H_VGA_TXP_C[0:3] connected with CPU side

S_VGA_AUXN, connected with SB side, the ground impedance is 552

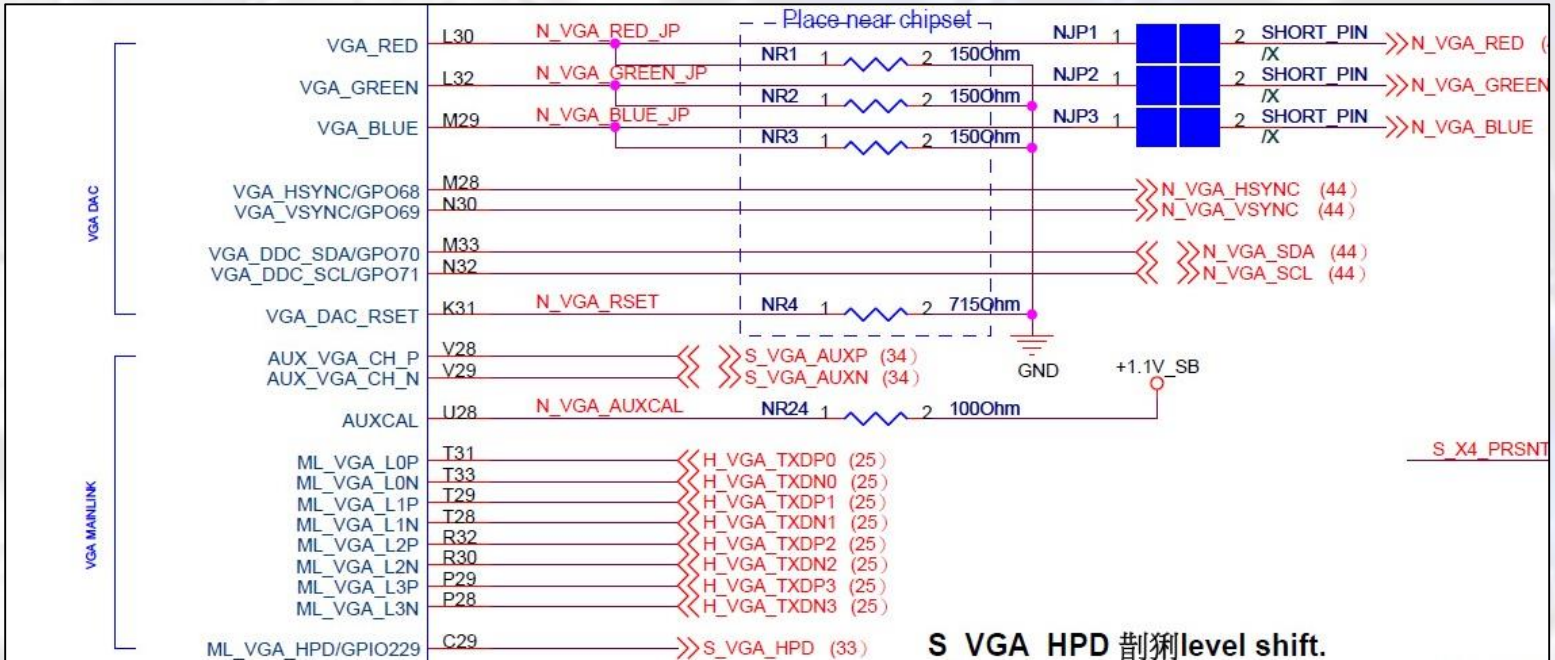
S_VGA_HPD the ground impedance is 816。

AMD For DVI/HDMI & VGA



CPU

D3



Thank You!