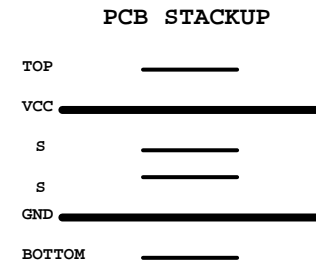
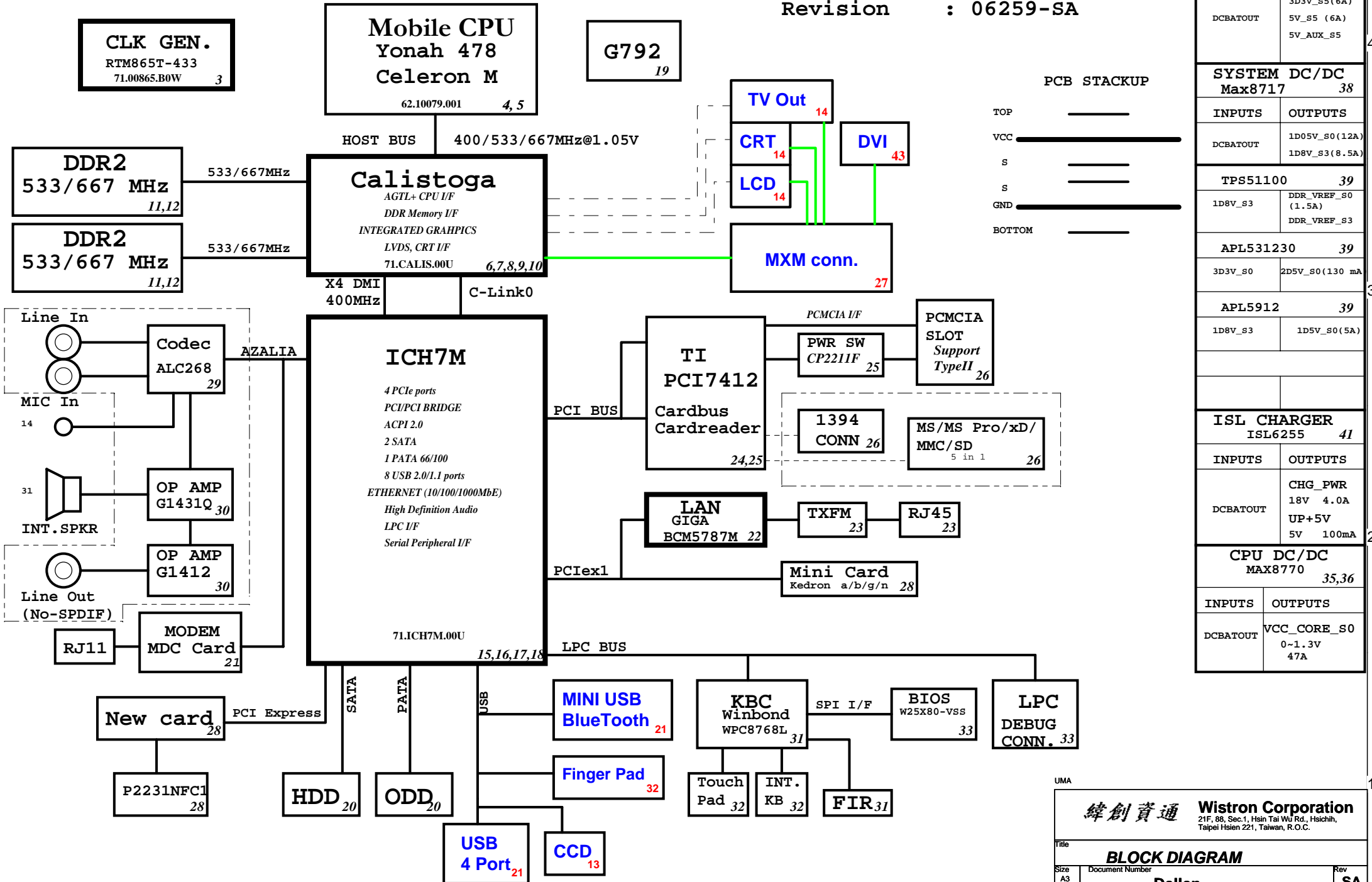


Dellen Block Diagram

Project code: 91.4V401.001
 PCB P/N : 48.4T307.0SA
 Revision : 06259-SA



SYSTEM DC/DC MAX8744 37	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 (6A) 5V_S5 (6A) 5V_AUX_S5
SYSTEM DC/DC Max8717 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 (1.2A) 1D8V_S3 (8.5A)
TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL531230 39	
3D3V_S0	2D5V_S0 (130 mA)
APL5912 39	
1D8V_S3	1D5V_S0 (5A)
ISL CHARGER ISL6255 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **Dellen** Rev: SA

Date: Tuesday, January 16, 2007 Sheet 1 of 43

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GP017, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0]	ICH7 internal 20K pull-ups
LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/GPIO17#, GNT4#/GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

page 17

PCI Routing

	IDSEL	INT	REQ	GNT
TI7412	AD22	G: CARDBUS B: 1394 F: Flash Media G: SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	FingerPad
5	BlueTooth
6	CCD
7	NewCard

Calistoga Strapping Signals and Configuration

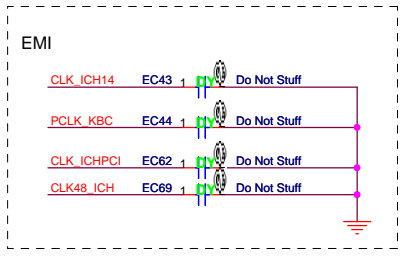
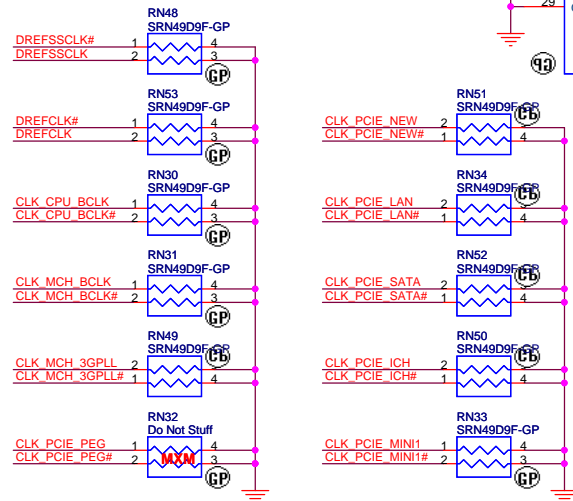
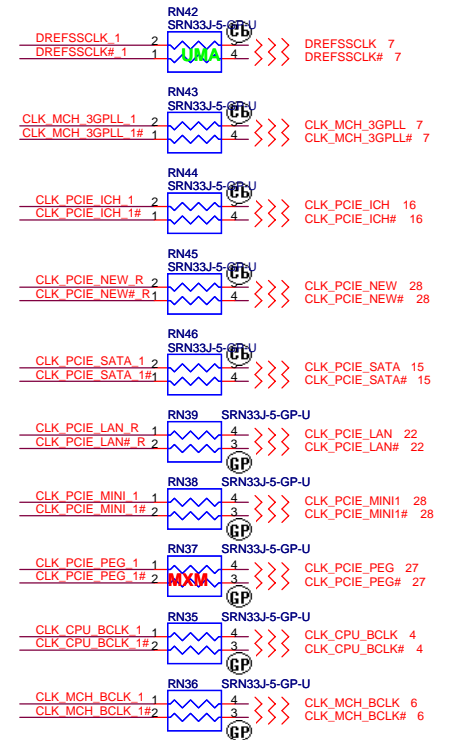
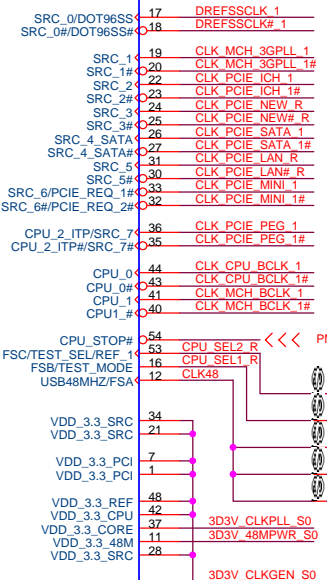
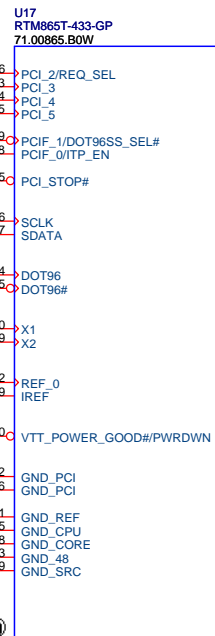
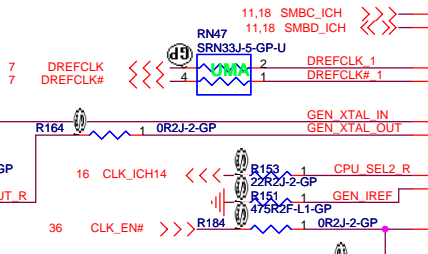
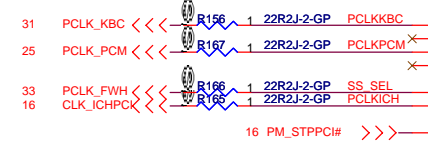
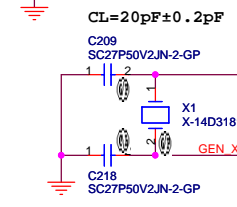
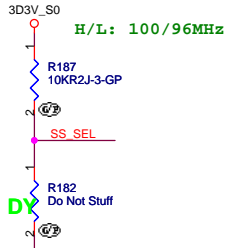
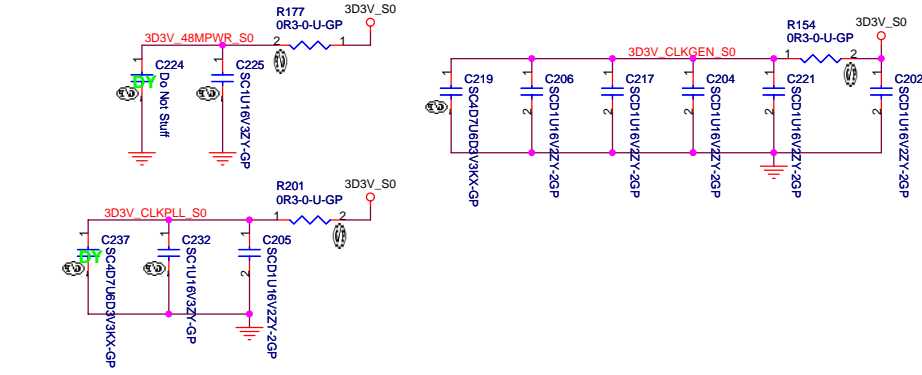
EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes, 15->0, 14->1 ect... 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 = Reverse Lane, 4->0, 3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWROK in signal.

UMA

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Reference			
Size A3	Document Number	Dellen	
Date: Tuesday, January 16, 2007	Sheet 2	of	43
			SA



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	333M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

UMA

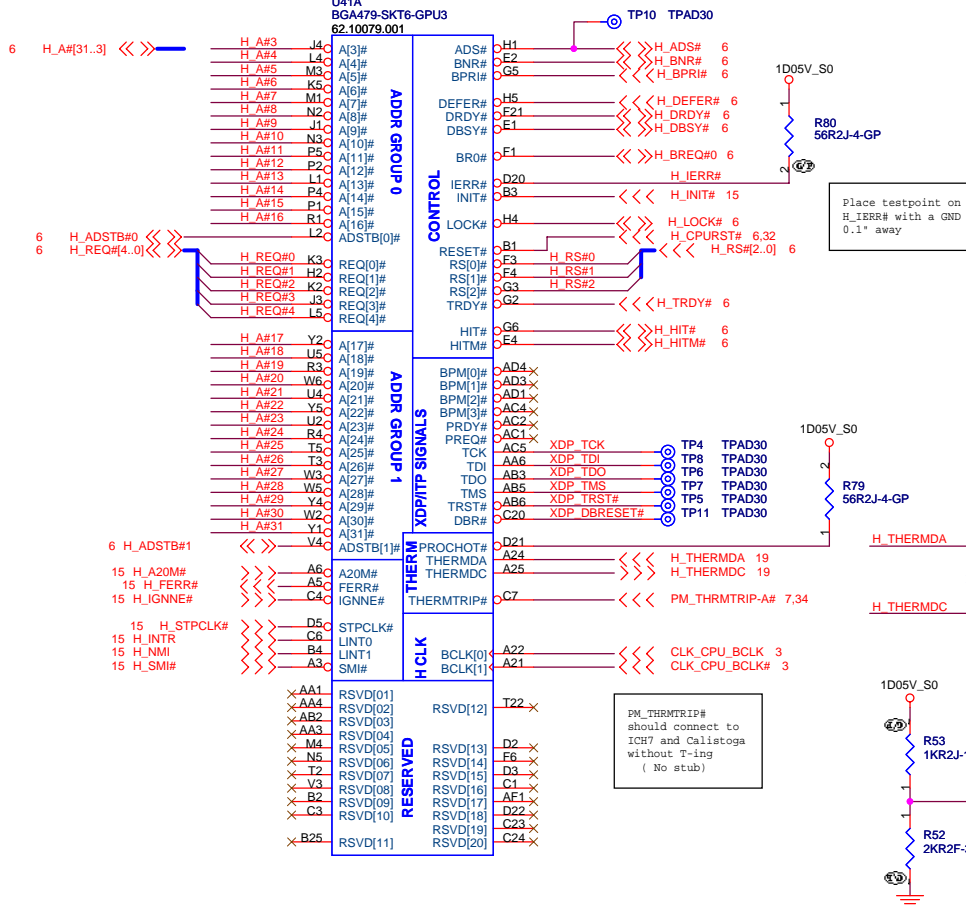
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Title: **Clock Generator RTM865T-433**

Size: A3 Document Number: **Dellen** Rev: SA

Date: Tuesday, January 16, 2007 Sheet 3 of 43

2nd source: 62.10053.401



<<>> H_DINV#[3..0] 6

<<>> H_DSTBN#[3..0] 6

<<>> H_DSTBP#[3..0] 6

<<>> H_D#[63..0] 6

6 H_DSTBN#0 <<>>

6 H_DSTBP#0 <<>>

6 H_DINV#0 <<>>

6 H_DSTBN#1 <<>>

6 H_DSTBP#1 <<>>

6 H_DINV#1 <<>>

3,7 CPU_SEL0 <<>>

3,7 CPU_SEL1 <<>>

3,7 CPU_SEL2 <<>>

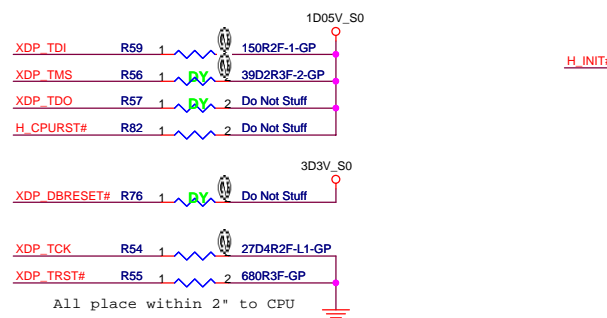
15 H_DPRSLP# 15,36 <<>>

15 H_DPWPR# 6 <<>>

15,32,34 H_PWRGD <<>>

6,15 H_CPUSLP# <<>>

36 PSI# <<>>

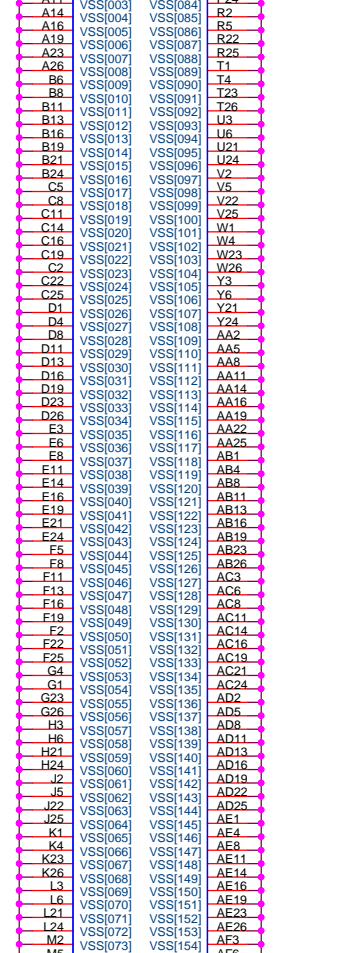
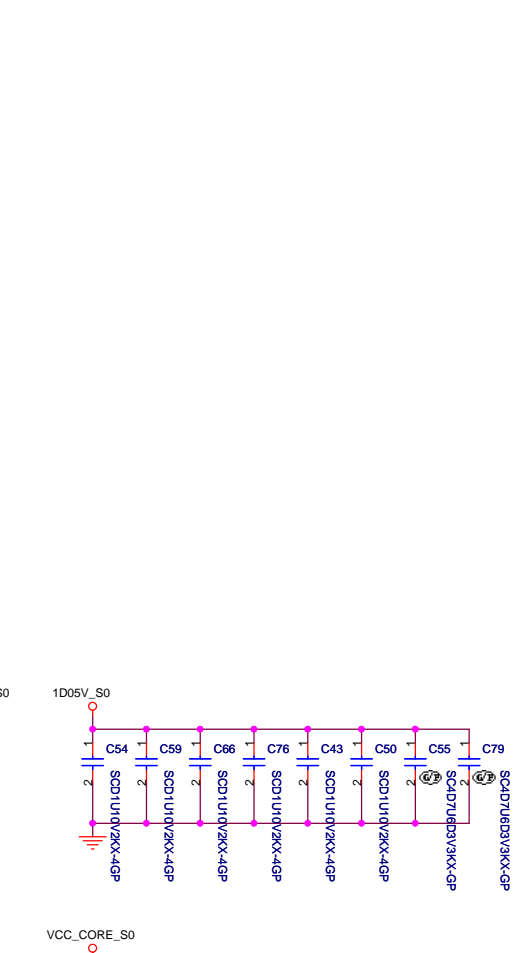
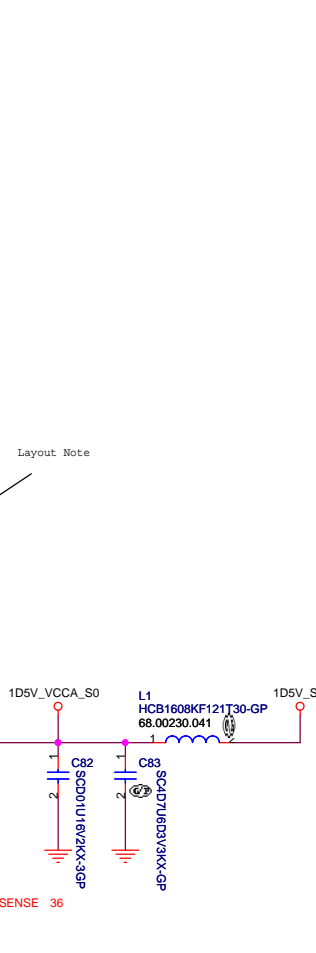
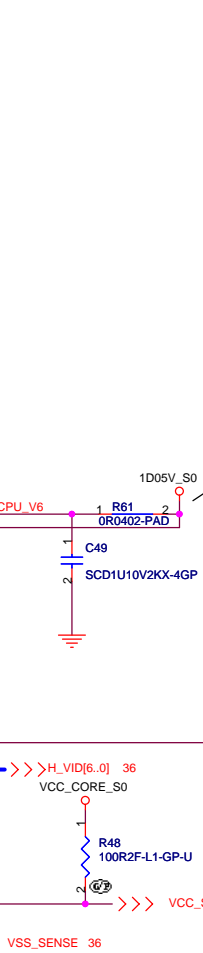
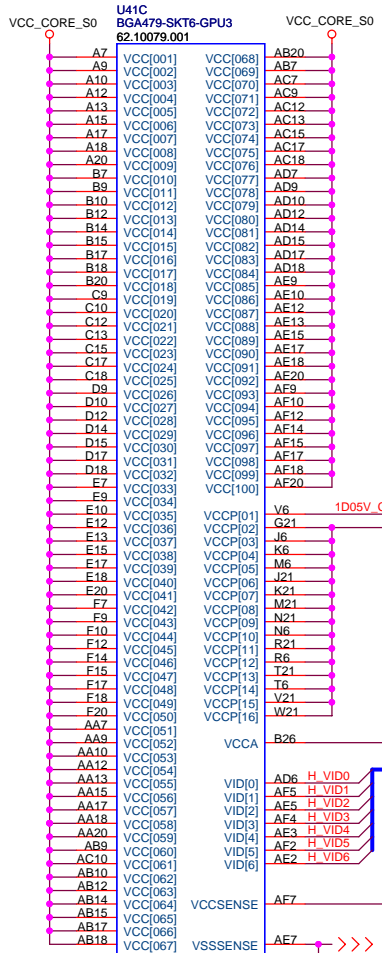


Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

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Title			CPU (1 of 2)		
Size	Document Number		Rev		
A3			SA		
Date:	Tuesday, January 16, 2007	Sheet	4	of	43

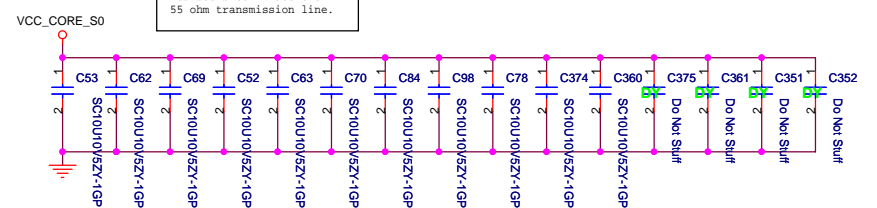


U41D
BGA479-SKT6-GPU3
62.10079.001

A4	VSS[001]	VSS[082]	P6
A6	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
A26	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE14
K26	VSS[068]	VSS[149]	AE16
L3	VSS[069]	VSS[150]	AE19
L6	VSS[070]	VSS[151]	AE23
L21	VSS[071]	VSS[152]	AE26
L24	VSS[072]	VSS[153]	AF1
M2	VSS[073]	VSS[154]	AF11
M5	VSS[074]	VSS[155]	AF13
M22	VSS[075]	VSS[156]	AF16
M25	VSS[076]	VSS[157]	AF19
N1	VSS[077]	VSS[158]	AF21
N4	VSS[078]	VSS[159]	AF24
N23	VSS[079]	VSS[160]	
N26	VSS[080]	VSS[161]	
P3	VSS[081]	VSS[162]	

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

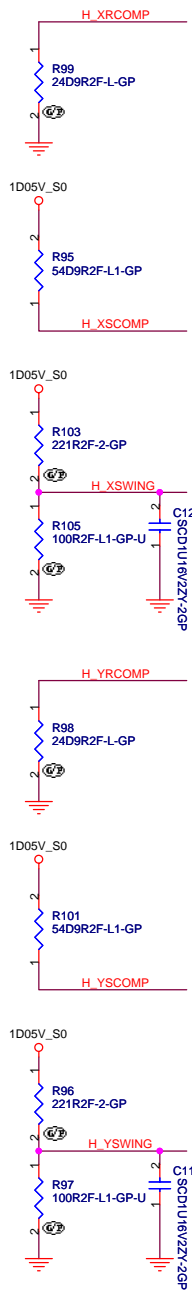


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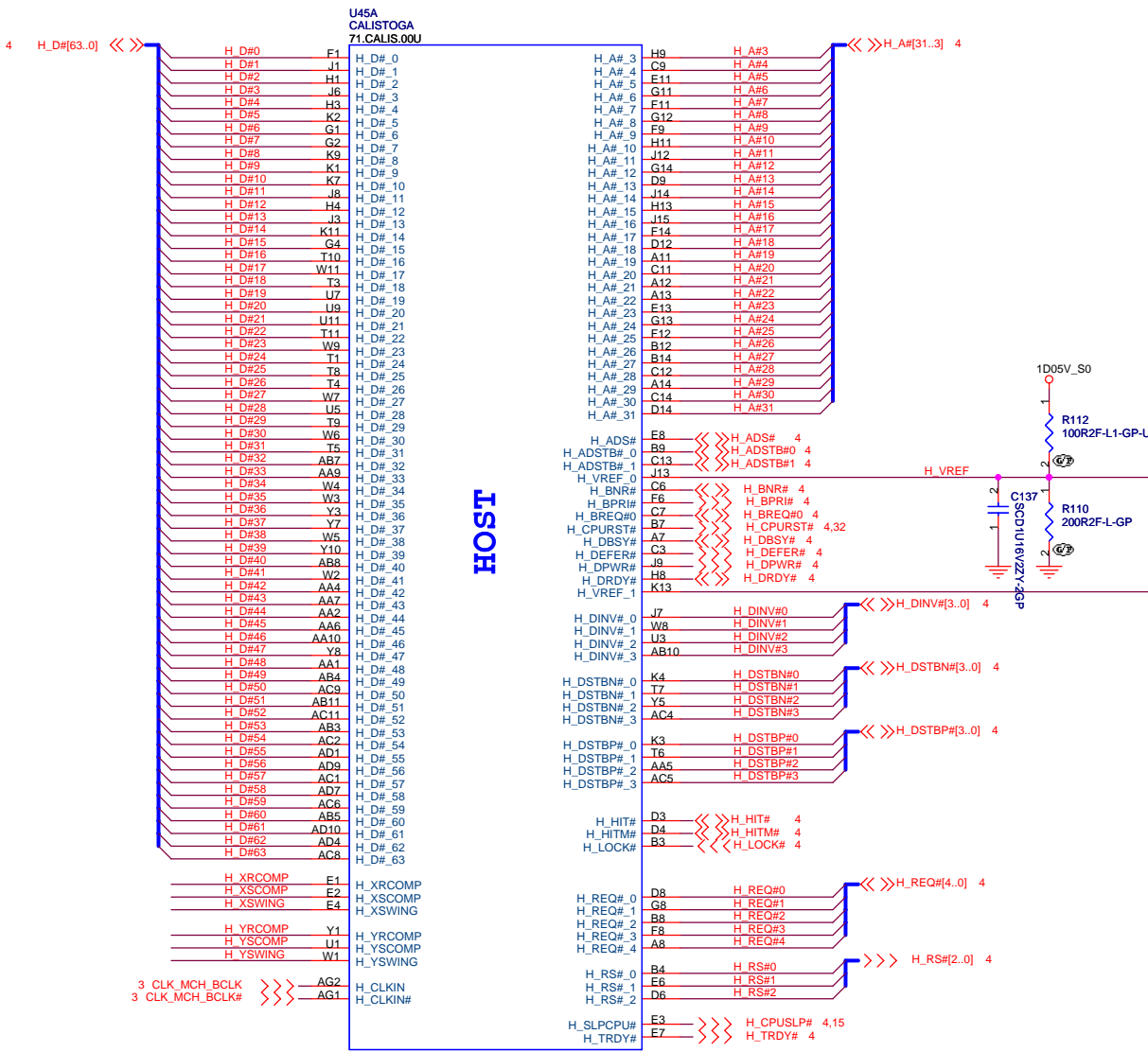
Title: CPU (2 of 2)

Size: A3 Document Number: Delllen Rev: SA

Date: Tuesday, January 16, 2007 Sheet 5 of 43



Place them near to the chip (< 0.5")



HOST

DIS : KI.94501.006
 UMA : 943GML P/N is 71.00943.M01

UMA

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Title: **GMCH (1 of 5)**

Size: A3 Document Number: **Dellen** Rev: SA

Date: Tuesday, January 16, 2007 Sheet 6 of 43

U45D
CALISTOGA
71.CALIS.00U

11 M_A_DQ[63.0] <<<	M A DQ0	AJ35	SA_DQ0
	M A DQ1	AJ34	SA_DQ1
	M A DQ2	AM31	SA_DQ2
	M A DQ3	AM33	SA_DQ3
	M A DQ4	AJ36	SA_DQ4
	M A DQ5	AJ32	SA_DQ5
	M A DQ6	AK35	SA_DQ6
	M A DQ7	AH31	SA_DQ7
	M A DQ8	AN35	SA_DQ8
	M A DQ9	AP33	SA_DQ9
	M A DQ10	AR31	SA_DQ10
	M A DQ11	AP31	SA_DQ11
	M A DQ12	AN38	SA_DQ12
	M A DQ13	AM36	SA_DQ13
	M A DQ14	AM34	SA_DQ14
	M A DQ15	AN33	SA_DQ15
	M A DQ16	AK26	SA_DQ16
	M A DQ17	AL27	SA_DQ17
	M A DQ18	AM26	SA_DQ18
	M A DQ19	AN28	SA_DQ19
	M A DQ20	AK28	SA_DQ20
	M A DQ21	AL28	SA_DQ21
	M A DQ22	AM24	SA_DQ22
	M A DQ23	AP26	SA_DQ23
	M A DQ24	AP23	SA_DQ24
	M A DQ25	AL22	SA_DQ25
	M A DQ26	AP21	SA_DQ26
	M A DQ27	AN20	SA_DQ27
	M A DQ28	AL23	SA_DQ28
	M A DQ29	AP24	SA_DQ29
	M A DQ30	AP20	SA_DQ30
	M A DQ31	AT21	SA_DQ31
	M A DQ32	AR12	SA_DQ32
	M A DQ33	AR14	SA_DQ33
	M A DQ34	AP13	SA_DQ34
	M A DQ35	AP12	SA_DQ35
	M A DQ36	AT13	SA_DQ36
	M A DQ37	AT12	SA_DQ37
	M A DQ38	AL14	SA_DQ38
	M A DQ39	AL12	SA_DQ39
	M A DQ40	AK9	SA_DQ40
	M A DQ41	AN7	SA_DQ41
	M A DQ42	AK8	SA_DQ42
	M A DQ43	AK7	SA_DQ43
	M A DQ44	AF9	SA_DQ44
	M A DQ45	AN9	SA_DQ45
	M A DQ46	AT5	SA_DQ46
	M A DQ47	AL5	SA_DQ47
	M A DQ48	AY2	SA_DQ48
	M A DQ49	AW2	SA_DQ49
	M A DQ50	AP1	SA_DQ50
	M A DQ51	AN2	SA_DQ51
	M A DQ52	AV2	SA_DQ52
	M A DQ53	AT3	SA_DQ53
	M A DQ54	AN1	SA_DQ54
	M A DQ55	AL2	SA_DQ55
	M A DQ56	AG7	SA_DQ56
	M A DQ57	AF9	SA_DQ57
	M A DQ58	AG4	SA_DQ58
	M A DQ59	AF6	SA_DQ59
	M A DQ60	AG9	SA_DQ60
	M A DQ61	AH6	SA_DQ61
	M A DQ62	AF4	SA_DQ62
	M A DQ63	AF8	SA_DQ63

DDR SYSTEM MEMORY A

SA_BS_0	AU12	M A BS#0 11,12
SA_BS_1	AV14	M A BS#1 11,12
SA_BS_2	BA20	M A BS#2 11,12
SA_BS_2	AY13	M A CAS# 11,12
SA_DM_0	AJ35	M A DM0
SA_DM_1	AM35	M A DM1
SA_DM_2	AL26	M A DM2
SA_DM_3	AN22	M A DM3
SA_DM_4	AM14	M A DM4
SA_DM_5	AL9	M A DM5
SA_DM_6	AR3	M A DM6
SA_DM_7	AH4	M A DM7
SA_DQS_0	AK33	M A DQS0
SA_DQS_1	AT33	M A DQS1
SA_DQS_2	AN28	M A DQS2
SA_DQS_3	AM22	M A DQS3
SA_DQS_4	AN12	M A DQS4
SA_DQS_5	AN9	M A DQS5
SA_DQS_6	AP3	M A DQS6
SA_DQS_7	AG5	M A DQS7
SA_DQS#_0	AK32	M A DQS#0
SA_DQS#_1	AU33	M A DQS#1
SA_DQS#_2	AN27	M A DQS#2
SA_DQS#_3	AM21	M A DQS#3
SA_DQS#_4	AM12	M A DQS#4
SA_DQS#_5	AL8	M A DQS#5
SA_DQS#_6	AN3	M A DQS#6
SA_DQS#_7	AH5	M A DQS#7
SA_MA_0	AY16	M A A0
SA_MA_1	AU14	M A A1
SA_MA_2	AW16	M A A2
SA_MA_3	BA16	M A A3
SA_MA_4	BA17	M A A4
SA_MA_5	AU16	M A A5
SA_MA_6	AV17	M A A6
SA_MA_7	AU17	M A A7
SA_MA_8	AW17	M A A8
SA_MA_9	AT16	M A A9
SA_MA_10	AU13	M A A10
SA_MA_11	AT17	M A A11
SA_MA_12	AV20	M A A12
SA_MA_13	AV12	M A A13
SA_RAS#	AW14	M A RAS# 11,12
SA_RCVENIN#	AK23	SA RCVENIN#
SA_RCVENOUT#	AK24	SA RCVENOUT#
SA_WE#	AY14	M A WE# 11,12

Place Test PAD Near to Chip
as could as possible

11 M_B_DQ[63.0] <<<

U45E
CALISTOGA
71.CALIS.00U

M B DQ0	AK39	SB_DQ0
M B DQ1	AJ37	SB_DQ1
M B DQ2	AP35	SB_DQ2
M B DQ3	AR41	SB_DQ3
M B DQ4	AJ38	SB_DQ4
M B DQ5	AK38	SB_DQ5
M B DQ6	AN41	SB_DQ6
M B DQ7	AP41	SB_DQ7
M B DQ8	AV41	SB_DQ8
M B DQ9	AT40	SB_DQ9
M B DQ10	AU38	SB_DQ10
M B DQ11	AV38	SB_DQ11
M B DQ12	AP38	SB_DQ12
M B DQ13	AR40	SB_DQ13
M B DQ14	AW38	SB_DQ14
M B DQ15	AY38	SB_DQ15
M B DQ16	BA38	SB_DQ16
M B DQ17	AV36	SB_DQ17
M B DQ18	AR36	SB_DQ18
M B DQ19	AP36	SB_DQ19
M B DQ20	BA36	SB_DQ20
M B DQ21	AU36	SB_DQ21
M B DQ22	AP35	SB_DQ22
M B DQ23	AP34	SB_DQ23
M B DQ24	AV33	SB_DQ24
M B DQ25	BA33	SB_DQ25
M B DQ26	AT31	SB_DQ26
M B DQ27	AU29	SB_DQ27
M B DQ28	AU31	SB_DQ28
M B DQ29	AW31	SB_DQ29
M B DQ30	AV29	SB_DQ30
M B DQ31	AW29	SB_DQ31
M B DQ32	AM19	SB_DQ32
M B DQ33	AL19	SB_DQ33
M B DQ34	AP14	SB_DQ34
M B DQ35	AN14	SB_DQ35
M B DQ36	AN17	SB_DQ36
M B DQ37	AM16	SB_DQ37
M B DQ38	AP15	SB_DQ38
M B DQ39	AL15	SB_DQ39
M B DQ40	AJ11	SB_DQ40
M B DQ41	AH10	SB_DQ41
M B DQ42	AJ9	SB_DQ42
M B DQ43	AN10	SB_DQ43
M B DQ44	AK13	SB_DQ44
M B DQ45	AH11	SB_DQ45
M B DQ46	AK10	SB_DQ46
M B DQ47	AJ8	SB_DQ47
M B DQ48	BA10	SB_DQ48
M B DQ49	AW10	SB_DQ49
M B DQ50	BA4	SB_DQ50
M B DQ51	AW4	SB_DQ51
M B DQ52	AY10	SB_DQ52
M B DQ53	AY9	SB_DQ53
M B DQ54	AV9	SB_DQ54
M B DQ55	AV4	SB_DQ55
M B DQ56	AV4	SB_DQ56
M B DQ57	AR5	SB_DQ57
M B DQ58	AK4	SB_DQ58
M B DQ59	AK3	SB_DQ59
M B DQ60	AT4	SB_DQ60
M B DQ61	AK5	SB_DQ61
M B DQ62	AJ5	SB_DQ62
M B DQ63	AJ3	SB_DQ63

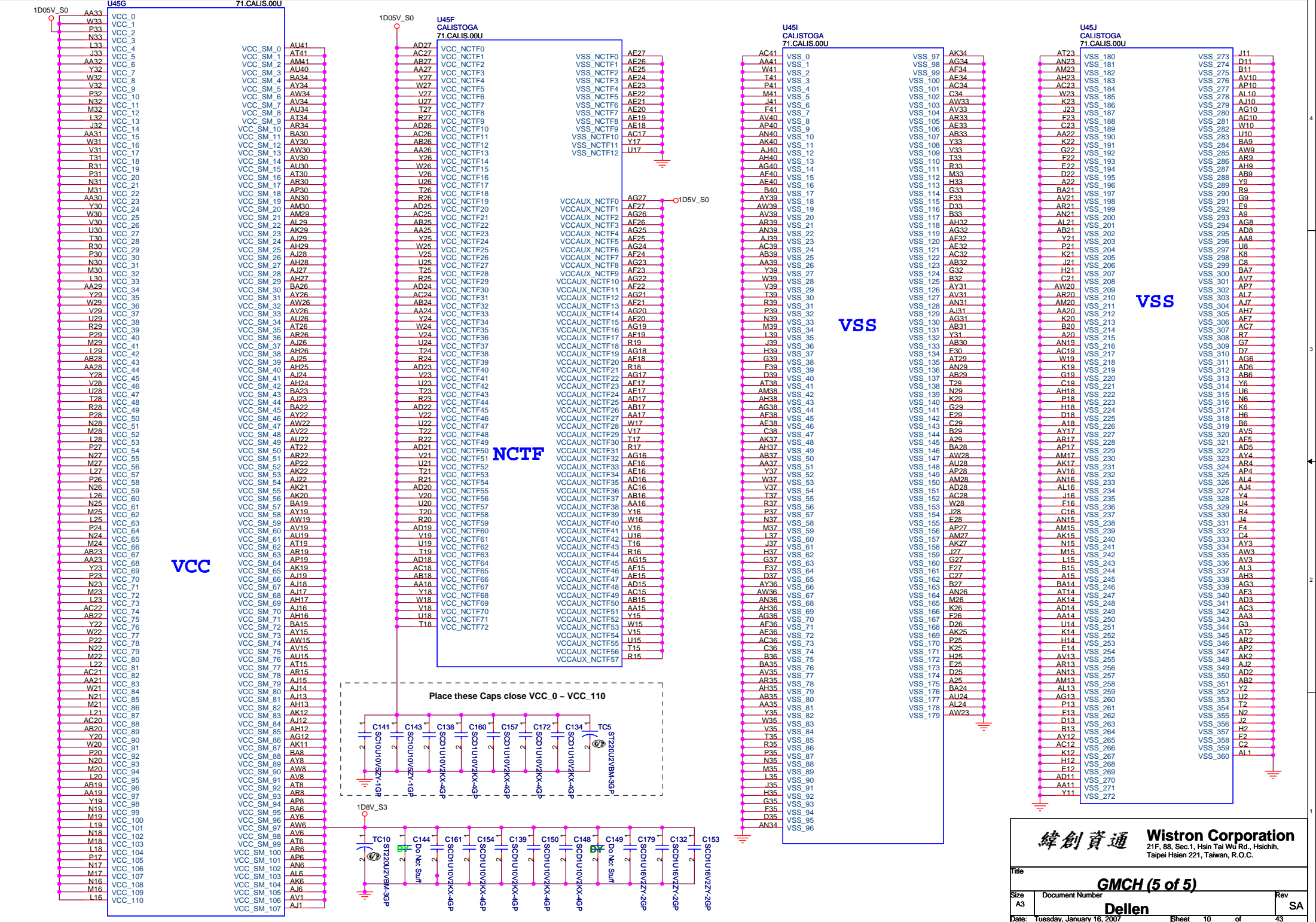
DDR SYSTEM MEMORY B

SB_BS_0	AT24	M B BS#0 11,12
SB_BS_1	AV23	M B BS#1 11,12
SB_BS_2	AY28	M B BS#2 11,12
SB_CAS#	AR24	M B CAS# 11,12
SB_DM_0	AK36	M B DM0
SB_DM_1	AR38	M B DM1
SB_DM_2	AT36	M B DM2
SB_DM_3	BA31	M B DM3
SB_DM_4	AL17	M B DM4
SB_DM_5	AH8	M B DM5
SB_DM_6	BA5	M B DM6
SB_DM_7	AN4	M B DM7
SB_DQS_0	AM39	M B DQS0
SB_DQS_1	AT39	M B DQS1
SB_DQS_2	AU35	M B DQS2
SB_DQS_3	AR29	M B DQS3
SB_DQS_4	AR16	M B DQS4
SB_DQS_5	AR10	M B DQS5
SB_DQS_6	AR7	M B DQS6
SB_DQS_7	AN6	M B DQS7
SB_DQS#_0	AM40	M B DQS#0
SB_DQS#_1	AU39	M B DQS#1
SB_DQS#_2	AT35	M B DQS#2
SB_DQS#_3	AP29	M B DQS#3
SB_DQS#_4	AP16	M B DQS#4
SB_DQS#_5	AT10	M B DQS#5
SB_DQS#_6	AT7	M B DQS#6
SB_DQS#_7	AP5	M B DQS#7
SB_MA_0	AY23	M B A0
SB_MA_1	AW24	M B A1
SB_MA_2	AY24	M B A2
SB_MA_3	AR28	M B A3
SB_MA_4	AT27	M B A4
SB_MA_5	AT28	M B A5
SB_MA_6	AU27	M B A6
SB_MA_7	AV28	M B A7
SB_MA_8	AV27	M B A8
SB_MA_9	AW27	M B A9
SB_MA_10	AW24	M B A10
SB_MA_11	BA27	M B A11
SB_MA_12	AY27	M B A12
SB_MA_13	AR23	M B A13
SB_RAS#	AU23	M B RAS# 11,12
SB_RCVENIN#	AK18	SB RCVENIN#
SB_RCVENOUT#	AK18	SB RCVENOUT#
SB_WE#	AR27	M B WE# 11,12

Place Test PAD Near to Chip
as could as possible

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VCC

NCTF

VSS

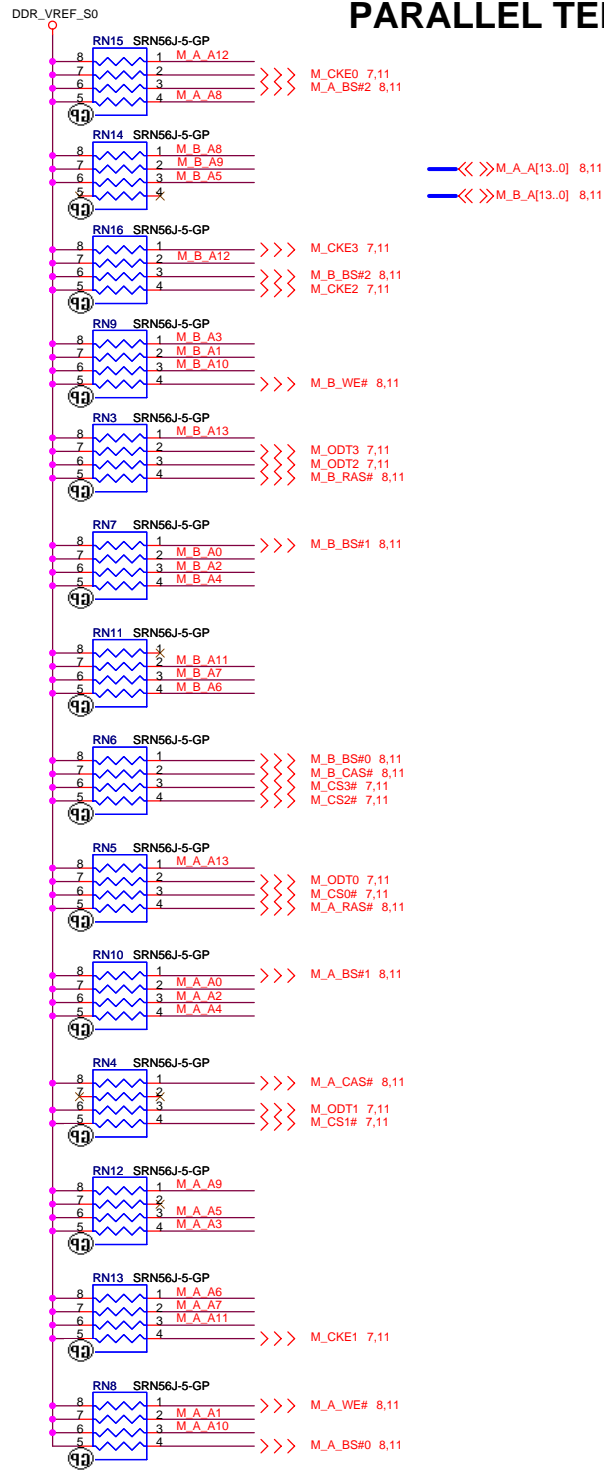
VSS

Place these Caps close VCC_0 - VCC_110

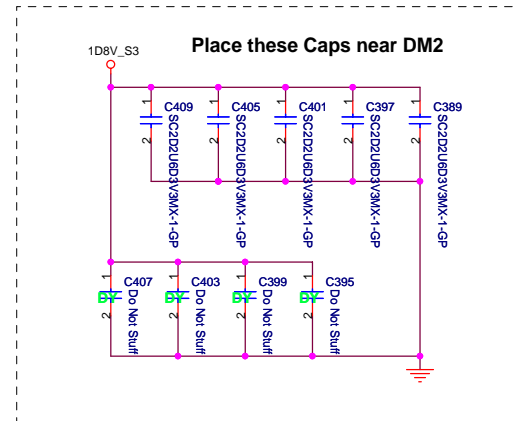
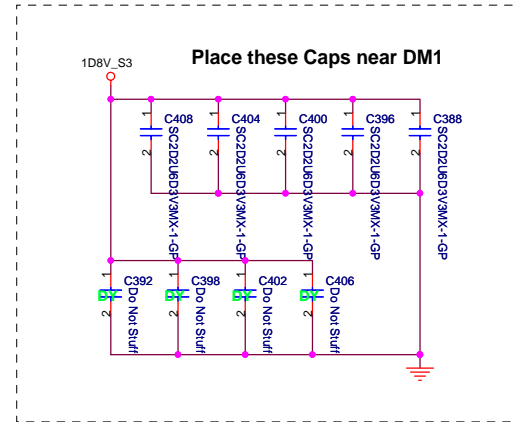
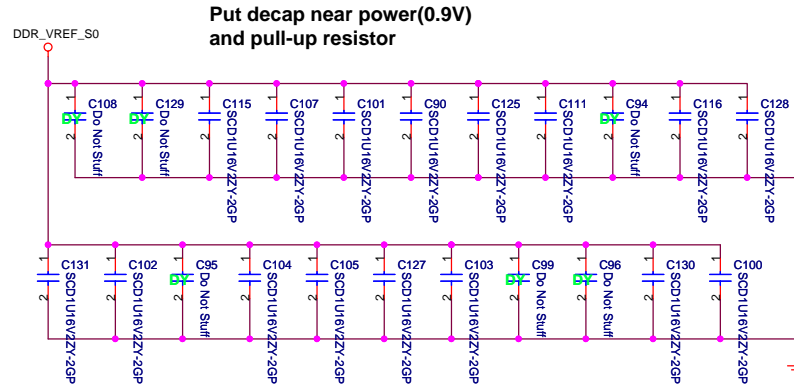
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Title			GMCH (5 of 5)		
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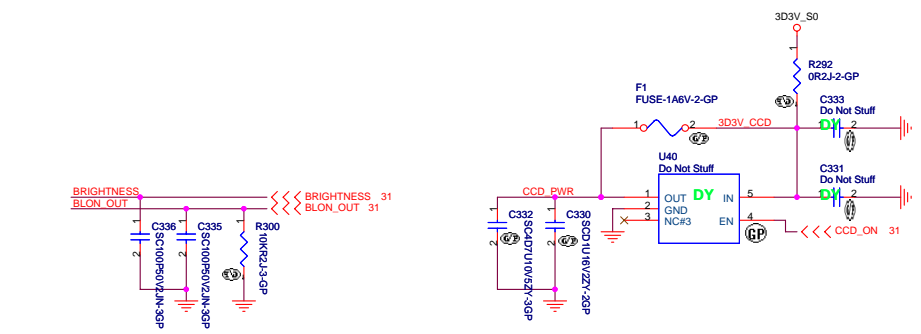
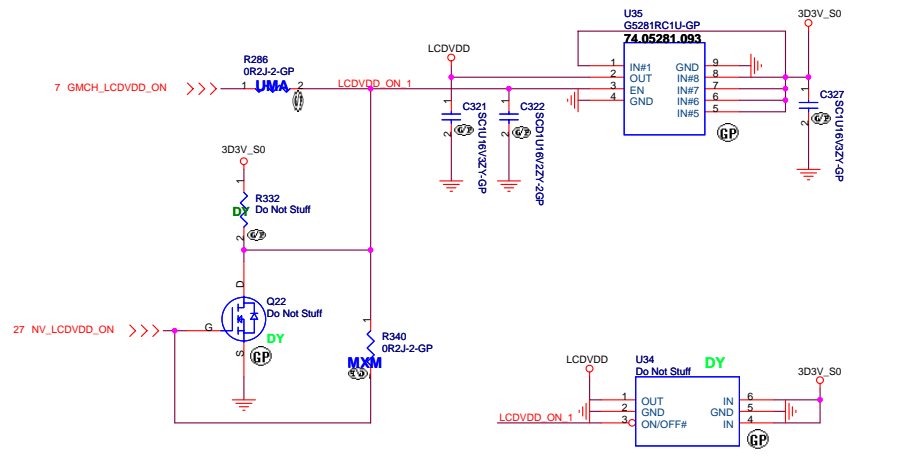
PARALLEL TERMINATION



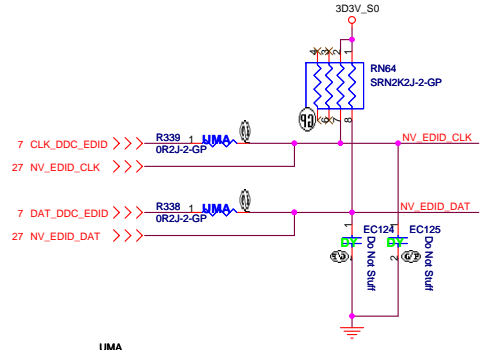
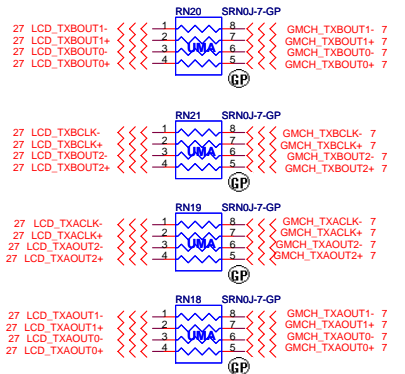
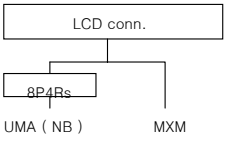
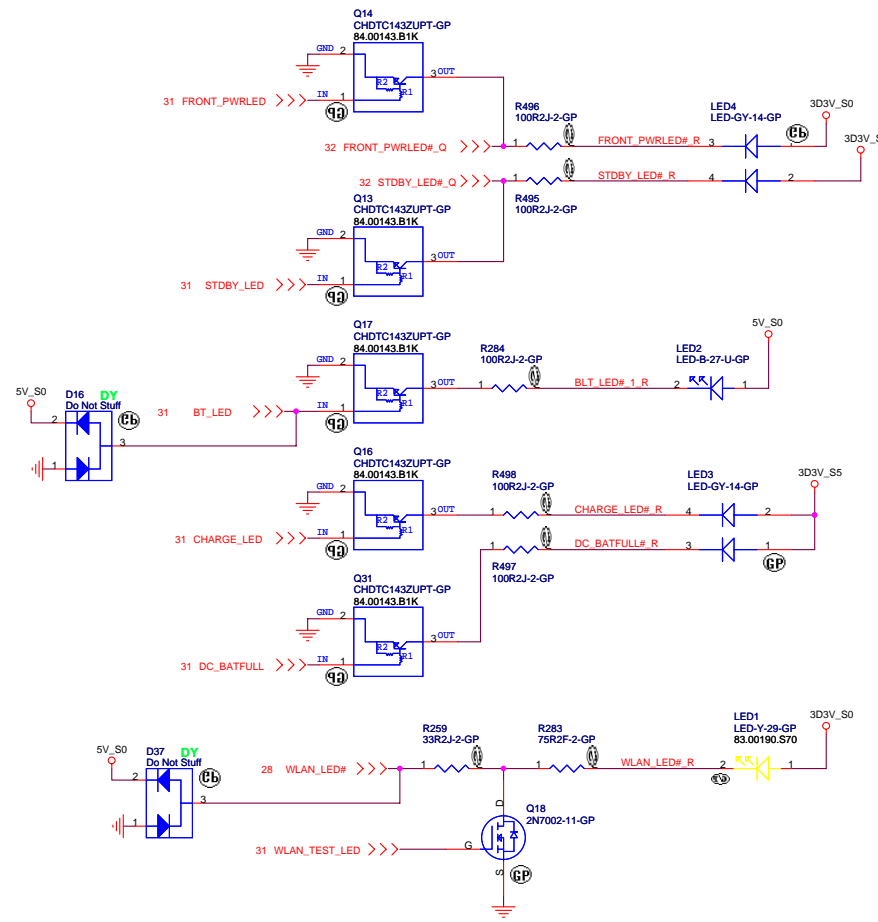
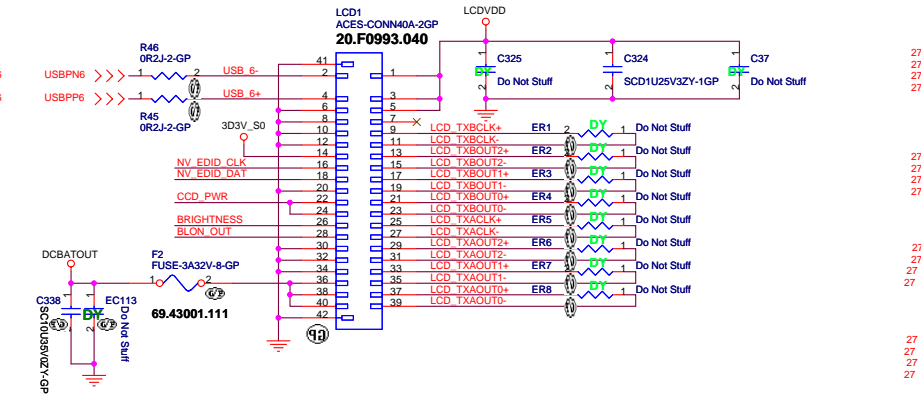
Decoupling Capacitor



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DDR2 Termination Resistor			
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LCD / Inverter conn.



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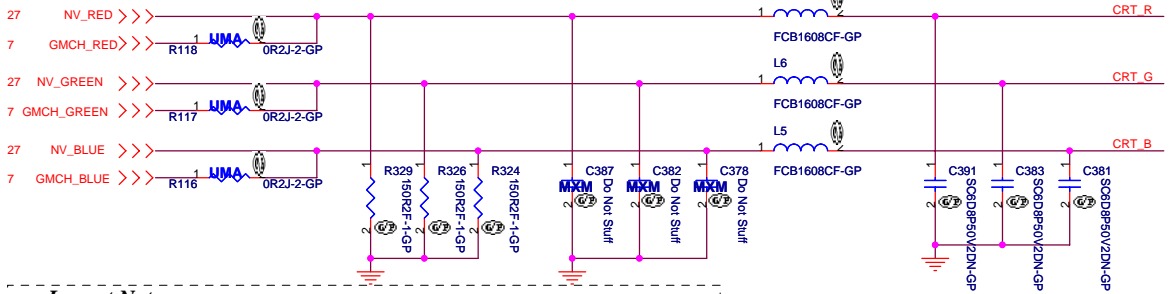
File: **LCD CONN & LED**

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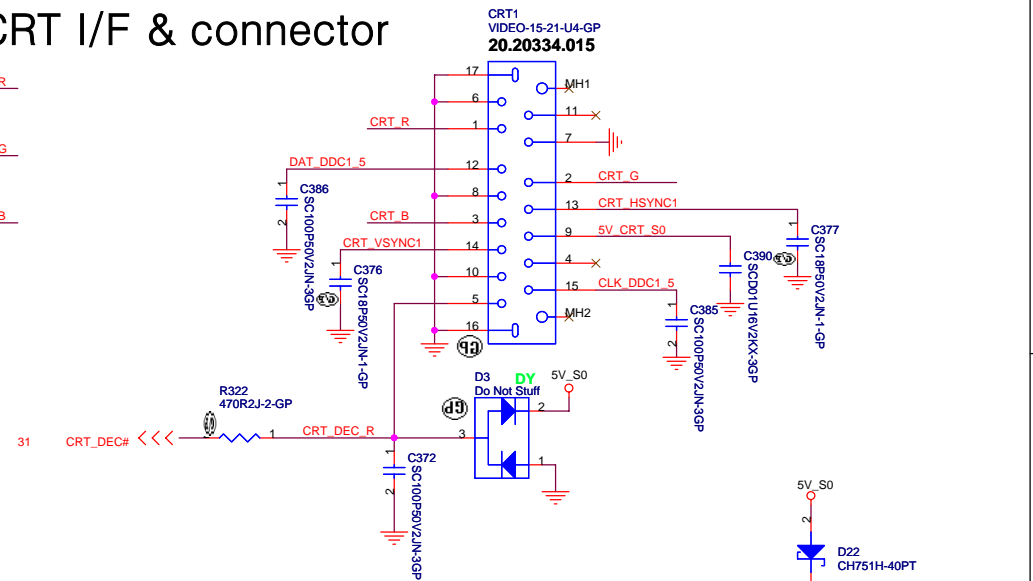
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

CRT I/F & connector

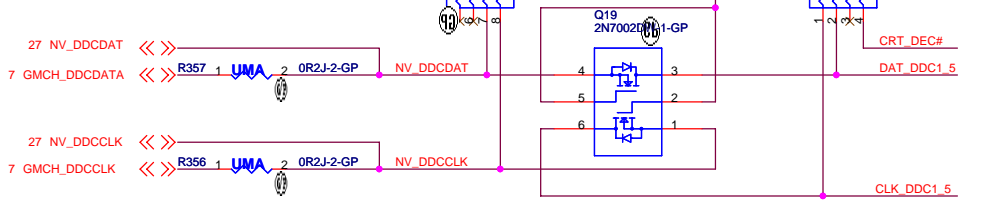
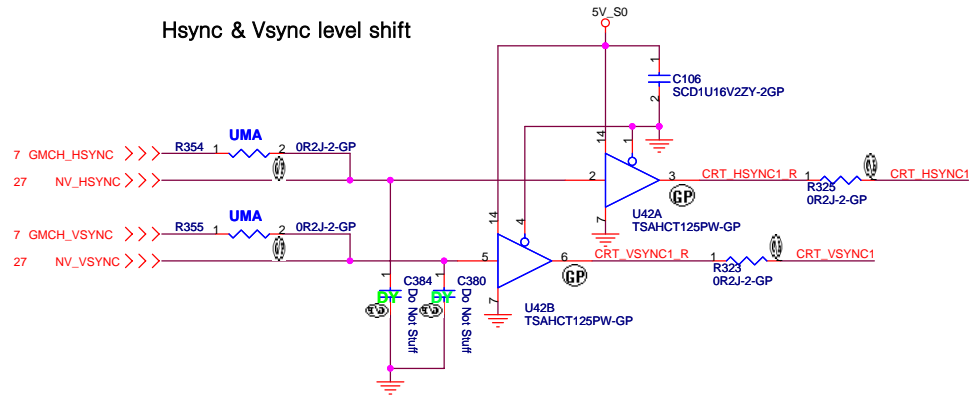


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

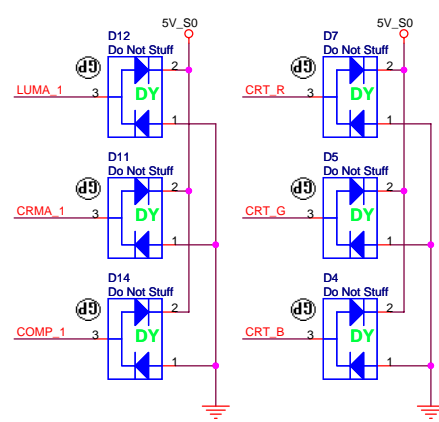
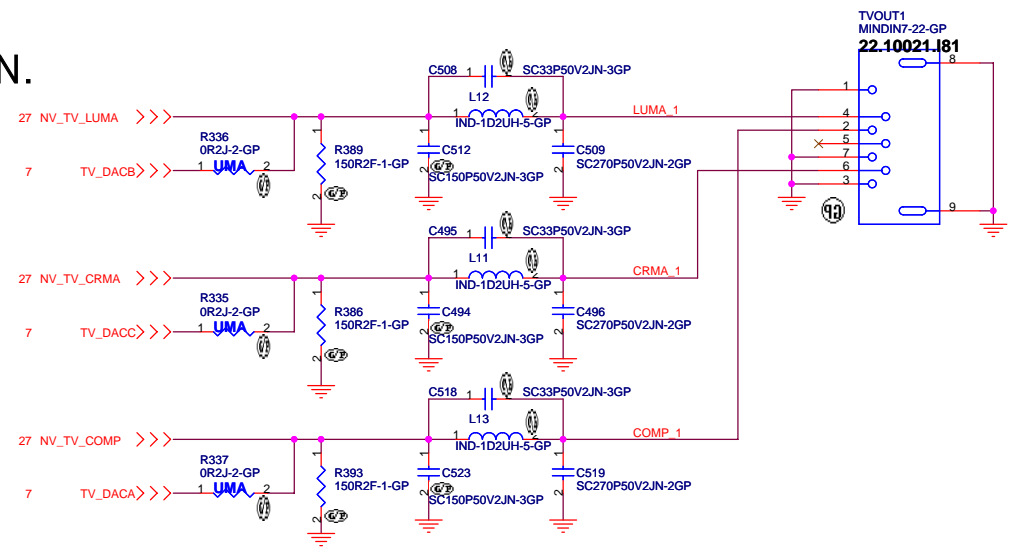


DDC_CLK & DATA level shift

Hsync & Vsync level shift



TV CONN.

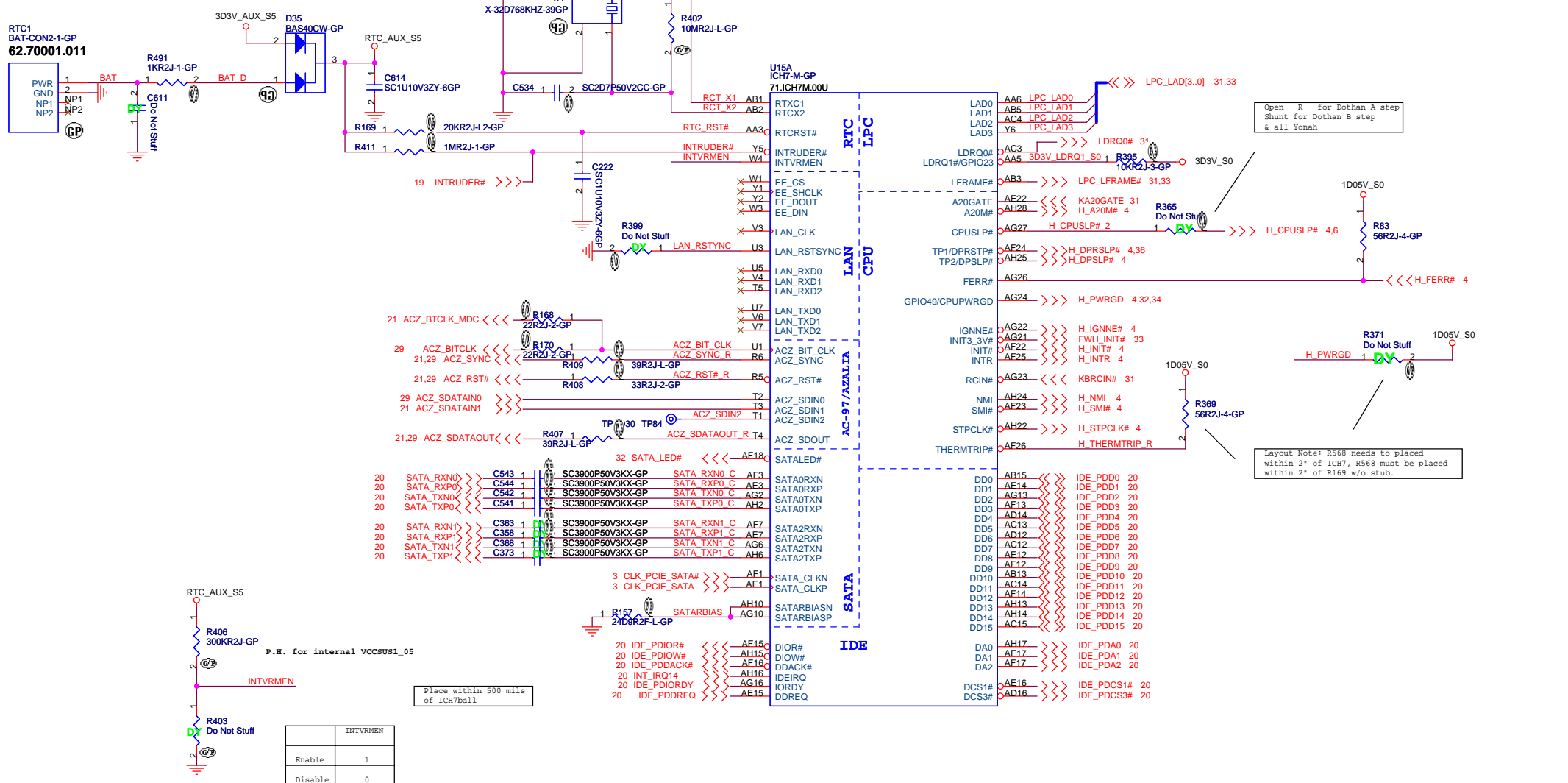


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RTC circuit

RTC1
BAT-CON2-1-GP
62.70001.011



Place within 500 mils of ICH7ball

	INTRVMEN
Enable	1
Disable	0

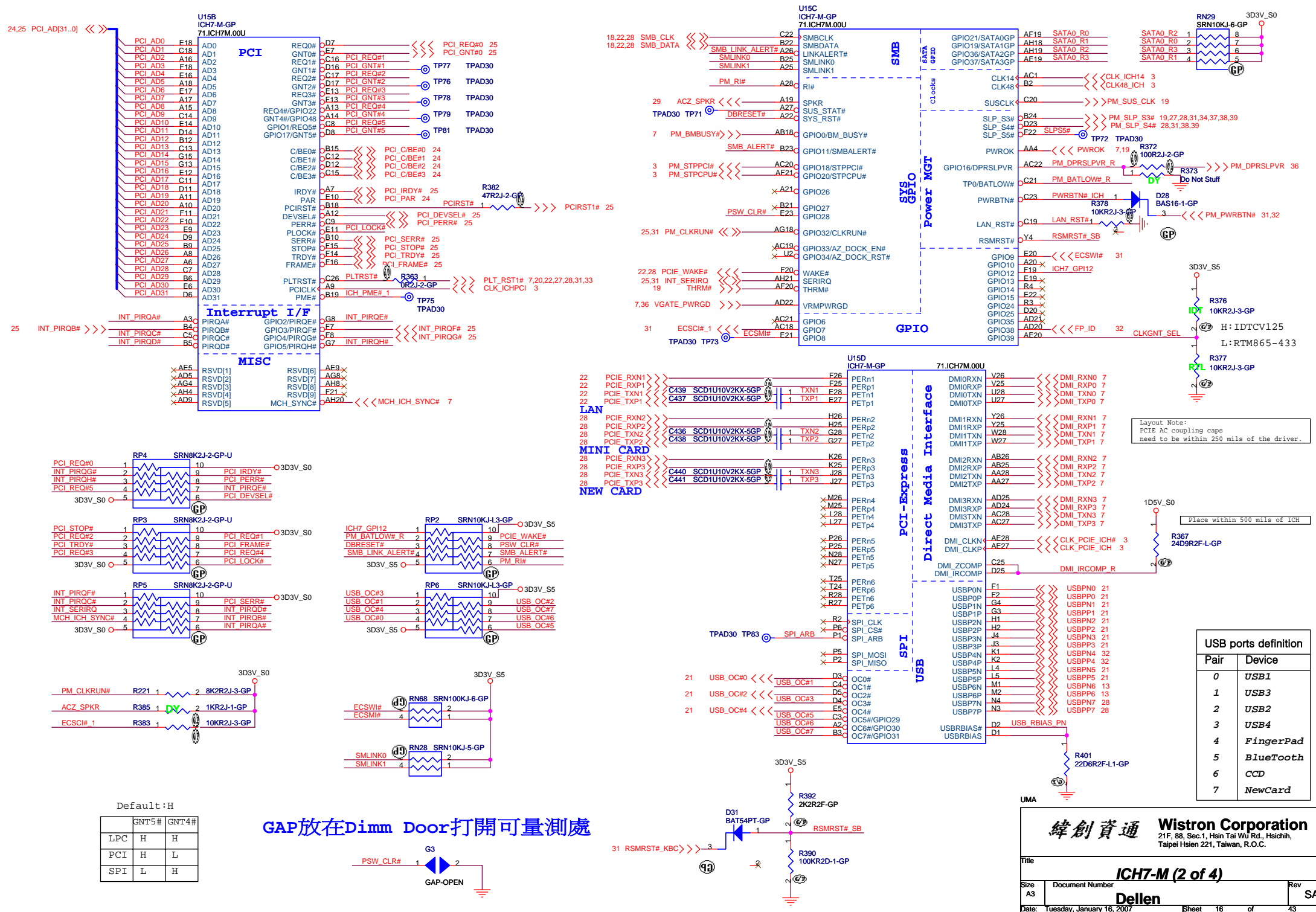
Placement Note:
Distance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

Open R for Dothan A step
Shunt for Dothan B step
& all Yonah

Layout Note: R568 needs to be placed
within 2" of ICH7, R568 must be placed
within 2" of R169 w/o stub.

UMA

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Title ICH7-M (1 of 4)	
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Layout Note:
PCIe AC coupling caps
need to be within 250 mils of the driver.

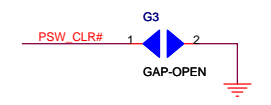
Place within 500 mils of ICH

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	FingerPad
5	BlueTooth
6	CCD
7	NewCard

GAP放在Dimm Door打開可量測處

Default:H

	GNT5#	GNT4#
LPC	H	H
PCI	H	L
SPI	L	H

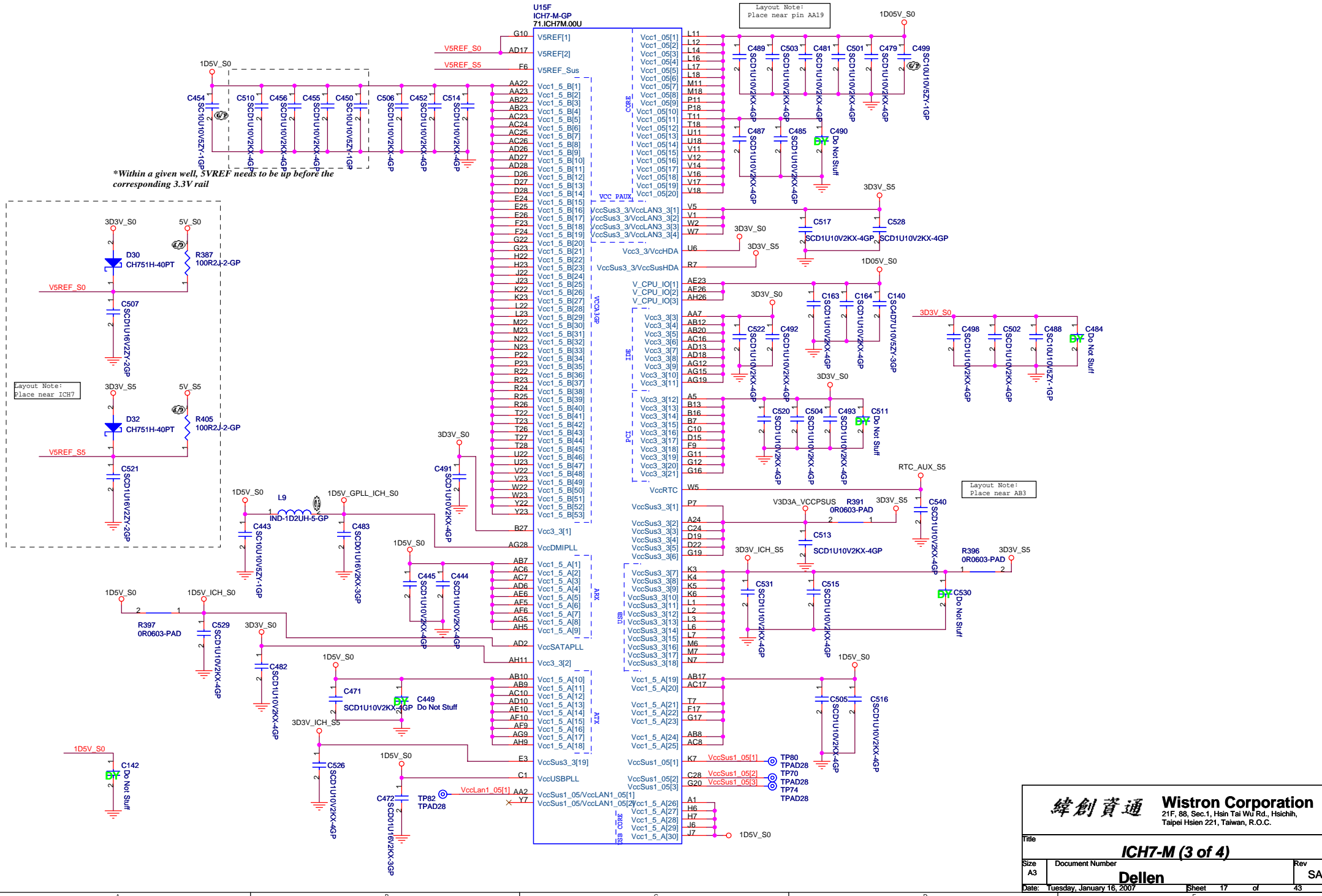


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File: **ICH7-M (2 of 4)**

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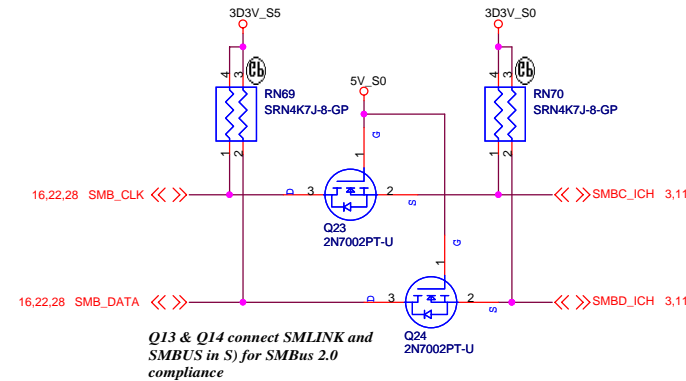
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail



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<p>Title</p> <p>ICH7-M (3 of 4)</p>	<p>Document Number</p> <p>Dellen</p>	<p>Rev</p> <p>SA</p>
<p>Date</p> <p>Tuesday, January 16, 2007</p>	<p>Sheet</p> <p>17 of 43</p>	<p>Page</p> <p>17 of 43</p>

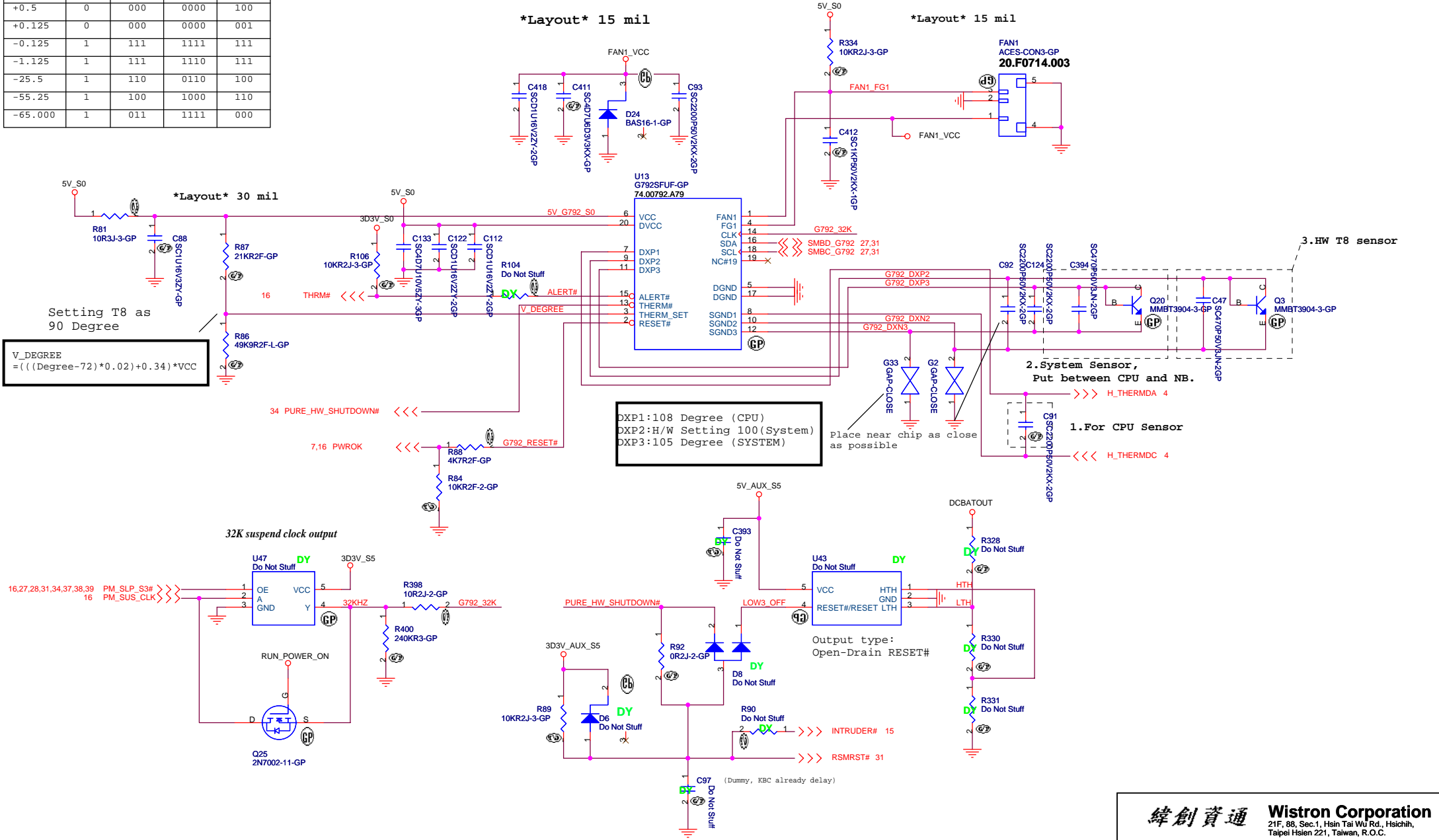
U15E ICH7-M-GP 71.ICH7M.00U		
A4	VSS[1]	VSS[98]
A23	VSS[2]	VSS[99]
B1	VSS[3]	VSS[100]
B8	VSS[4]	VSS[101]
B11	VSS[5]	VSS[102]
B14	VSS[6]	VSS[103]
B17	VSS[7]	VSS[104]
B20	VSS[8]	VSS[105]
B26	VSS[9]	VSS[106]
B29	VSS[10]	VSS[107]
C2	VSS[11]	VSS[108]
C6	VSS[12]	VSS[109]
C27	VSS[13]	VSS[110]
D10	VSS[14]	VSS[111]
D13	VSS[15]	VSS[112]
D18	VSS[16]	VSS[113]
D21	VSS[17]	VSS[114]
D24	VSS[18]	VSS[115]
E1	VSS[19]	VSS[116]
E2	VSS[20]	VSS[117]
E4	VSS[21]	VSS[118]
F8	VSS[22]	VSS[119]
E15	VSS[23]	VSS[120]
F3	VSS[24]	VSS[121]
F4	VSS[25]	VSS[122]
F5	VSS[26]	VSS[123]
F12	VSS[27]	VSS[124]
F27	VSS[28]	VSS[125]
F28	VSS[29]	VSS[126]
G1	VSS[30]	VSS[127]
G2	VSS[31]	VSS[128]
G5	VSS[32]	VSS[129]
G6	VSS[33]	VSS[130]
G9	VSS[34]	VSS[131]
G14	VSS[35]	VSS[132]
G18	VSS[36]	VSS[133]
G21	VSS[37]	VSS[134]
G24	VSS[38]	VSS[135]
G25	VSS[39]	VSS[136]
G26	VSS[40]	VSS[137]
H3	VSS[41]	VSS[138]
H4	VSS[42]	VSS[139]
H5	VSS[43]	VSS[140]
H24	VSS[44]	VSS[141]
H27	VSS[45]	VSS[142]
H28	VSS[46]	VSS[143]
J1	VSS[47]	VSS[144]
J2	VSS[48]	VSS[145]
J5	VSS[49]	VSS[146]
J24	VSS[50]	VSS[147]
J25	VSS[51]	VSS[148]
J26	VSS[52]	VSS[149]
K24	VSS[53]	VSS[150]
K27	VSS[54]	VSS[151]
K28	VSS[55]	VSS[152]
L13	VSS[56]	VSS[153]
L15	VSS[57]	VSS[154]
L24	VSS[58]	VSS[155]
L25	VSS[59]	VSS[156]
L26	VSS[60]	VSS[157]
M3	VSS[61]	VSS[158]
M4	VSS[62]	VSS[159]
M5	VSS[63]	VSS[160]
M12	VSS[64]	VSS[161]
M13	VSS[65]	VSS[162]
M14	VSS[66]	VSS[163]
M15	VSS[67]	VSS[164]
M16	VSS[68]	VSS[165]
M17	VSS[69]	VSS[166]
M24	VSS[70]	VSS[167]
M27	VSS[71]	VSS[168]
M28	VSS[72]	VSS[169]
N1	VSS[73]	VSS[170]
N2	VSS[74]	VSS[171]
N5	VSS[75]	VSS[172]
N6	VSS[76]	VSS[173]
N11	VSS[77]	VSS[174]
N12	VSS[78]	VSS[175]
N13	VSS[79]	VSS[176]
N14	VSS[80]	VSS[177]
N15	VSS[81]	VSS[178]
N16	VSS[82]	VSS[179]
N17	VSS[83]	VSS[180]
N18	VSS[84]	VSS[181]
N24	VSS[85]	VSS[182]
N25	VSS[86]	VSS[183]
N26	VSS[87]	VSS[184]
P3	VSS[88]	VSS[185]
P4	VSS[89]	VSS[186]
P12	VSS[90]	VSS[187]
P13	VSS[91]	VSS[188]
P14	VSS[92]	VSS[189]
P15	VSS[93]	VSS[190]
P16	VSS[94]	VSS[191]
P17	VSS[95]	VSS[192]
P24	VSS[96]	VSS[193]
P27	VSS[97]	VSS[194]

SMBUS



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TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



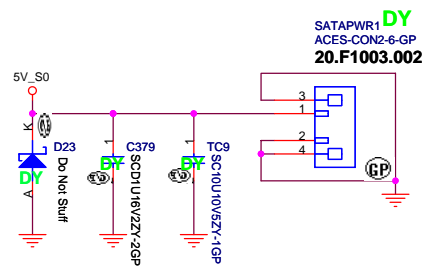
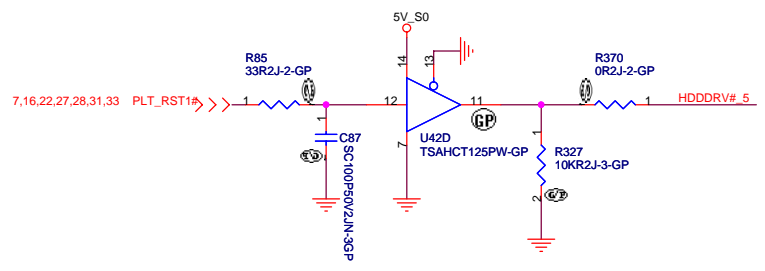
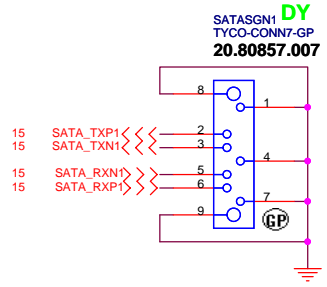
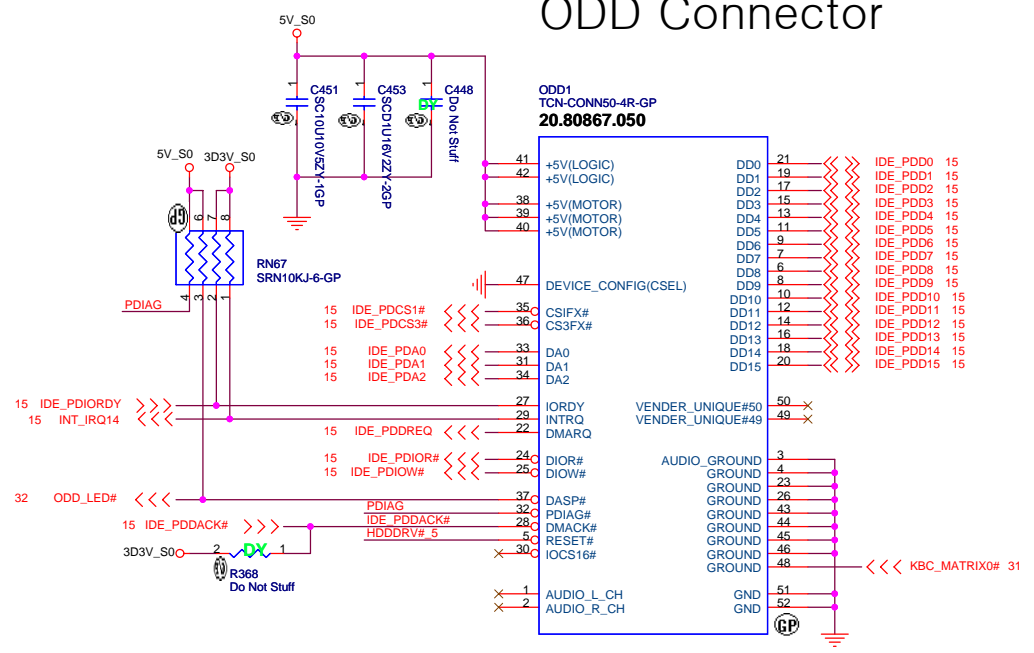
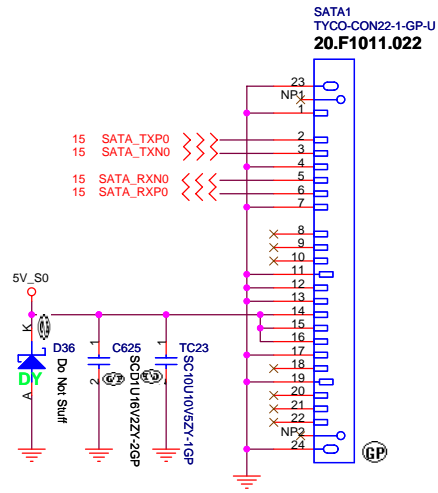
Setting T8 as 90 Degree

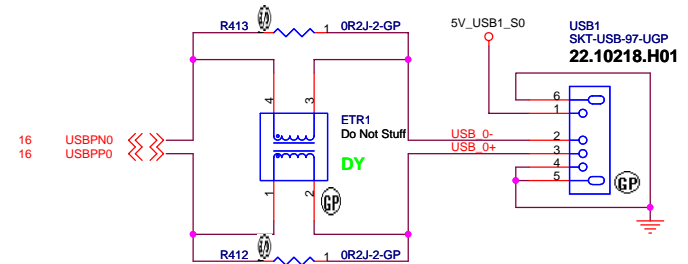
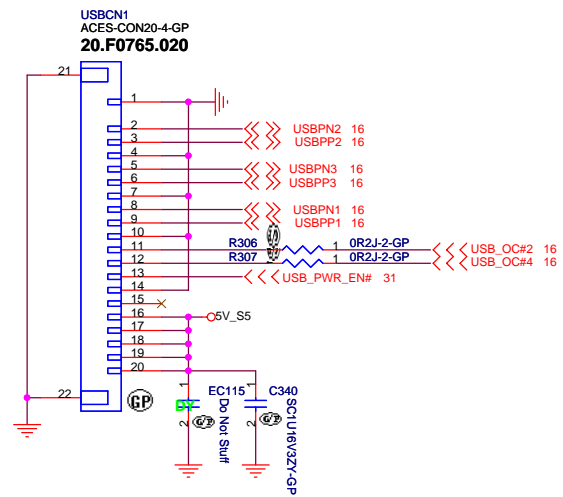
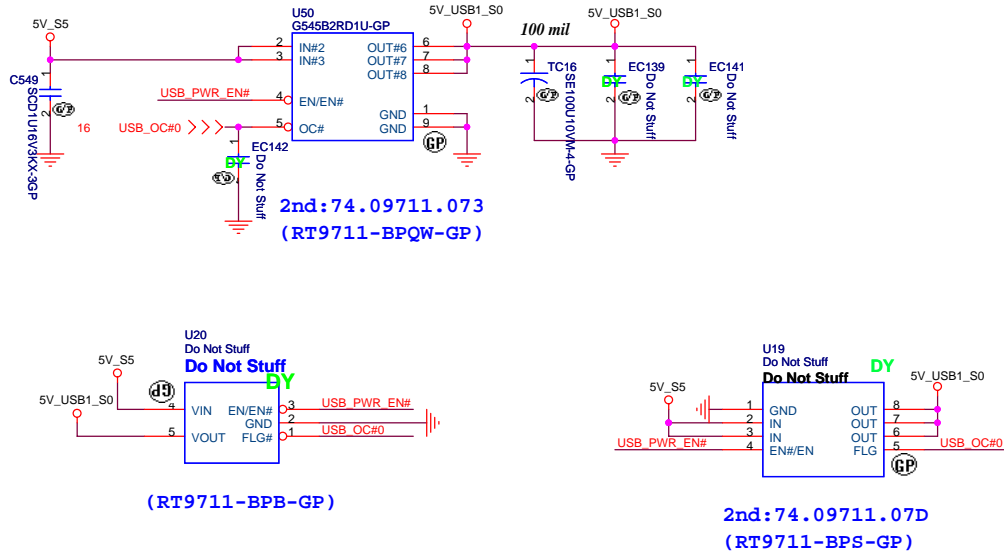
$$V_DEGREE = (((Degree-72)*0.02)+0.34)*VCC$$

DXP1:108 Degree (CPU)
 DXP2:H/W Setting 100(System)
 DXP3:105 Degree (SYSTEM)

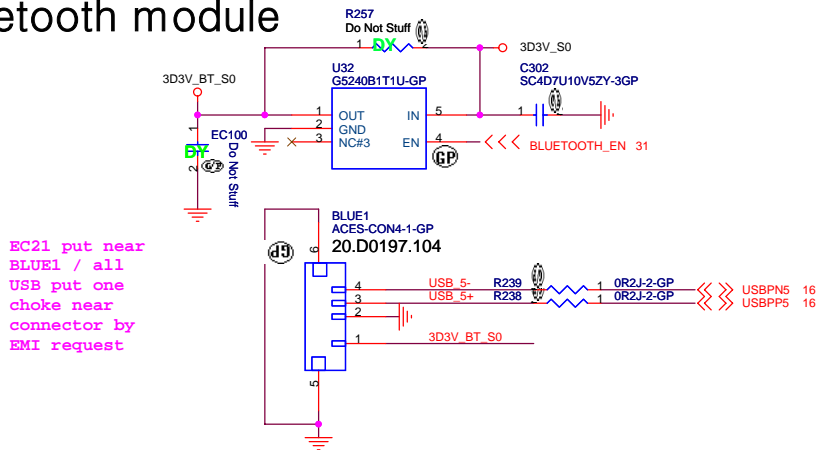
SATA HD Connector

ODD Connector

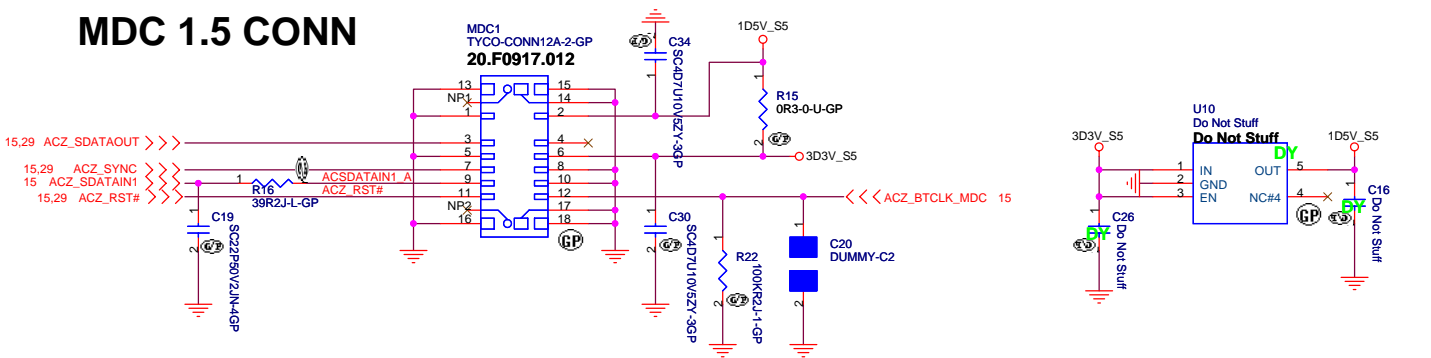


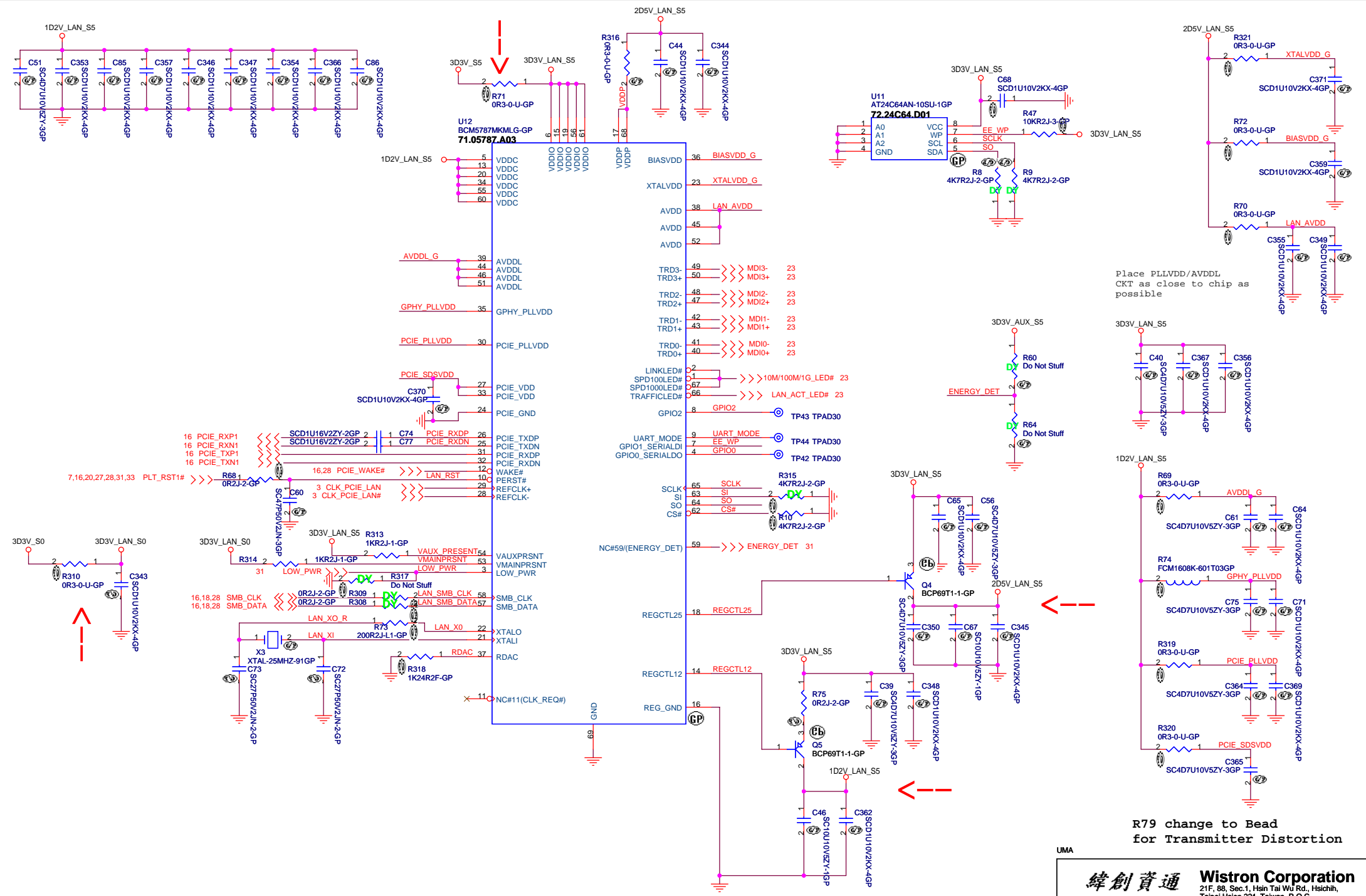


Bluetooth module



MDC 1.5 CONN





Place PLLVDD/AVDDL CKT as close to chip as possible

R79 change to Bead for Transmitter Distortion

UMA

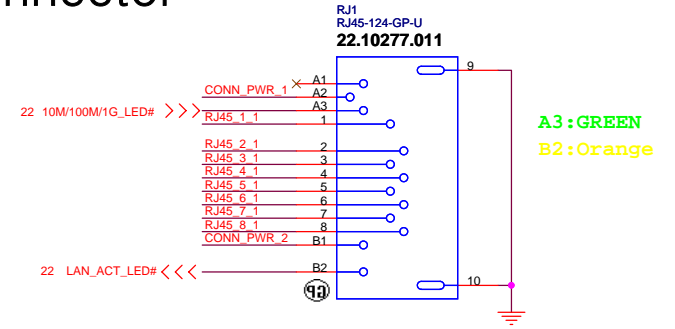
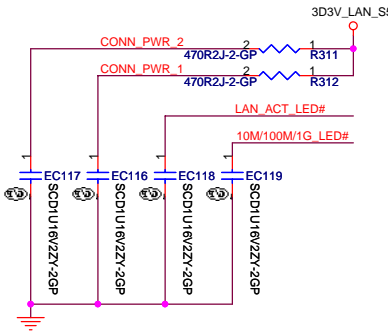
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BCM5787MKMLG**

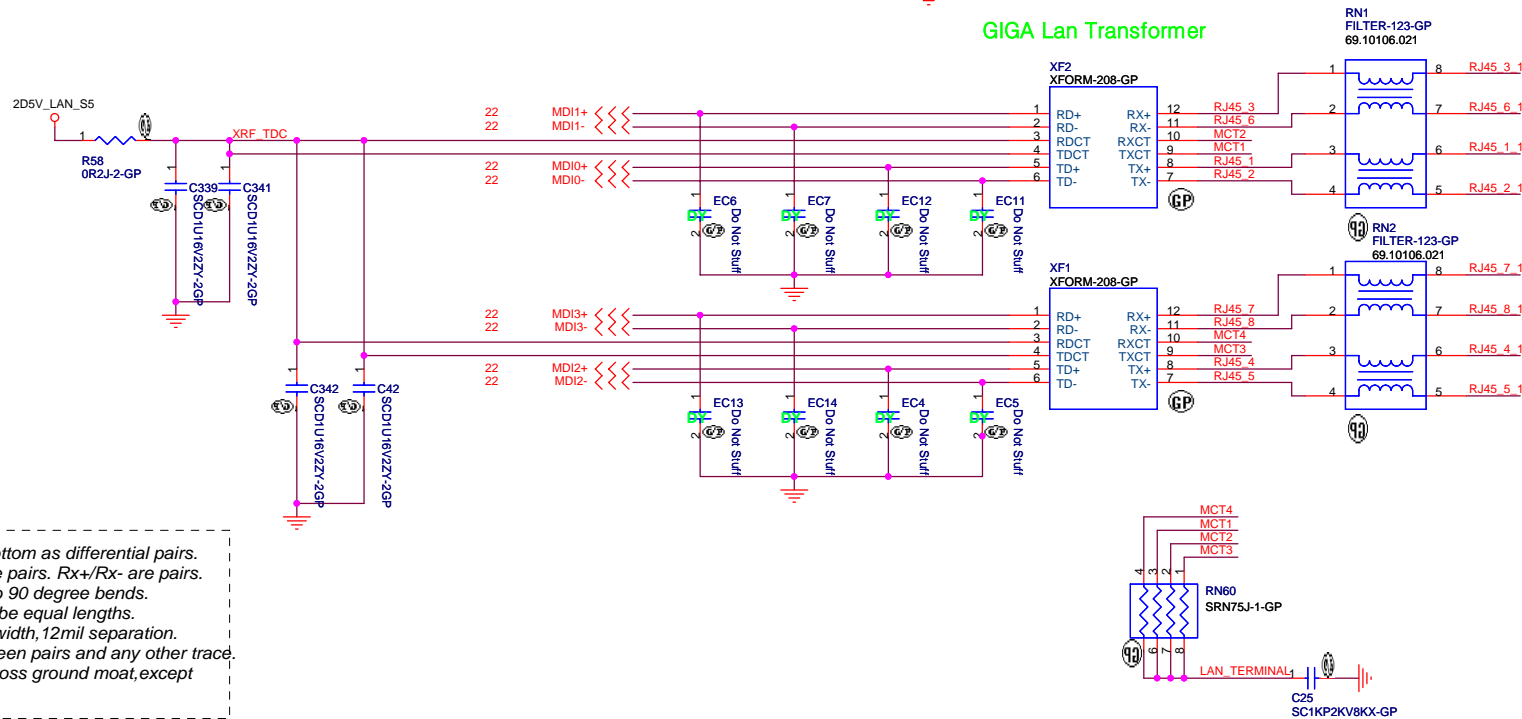
Size: A3	Document Number: Dellen	Rev: SA
Date: Tuesday, January 16, 2007		Sheet 22 of 43

LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



GIGA Lan Transformer



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

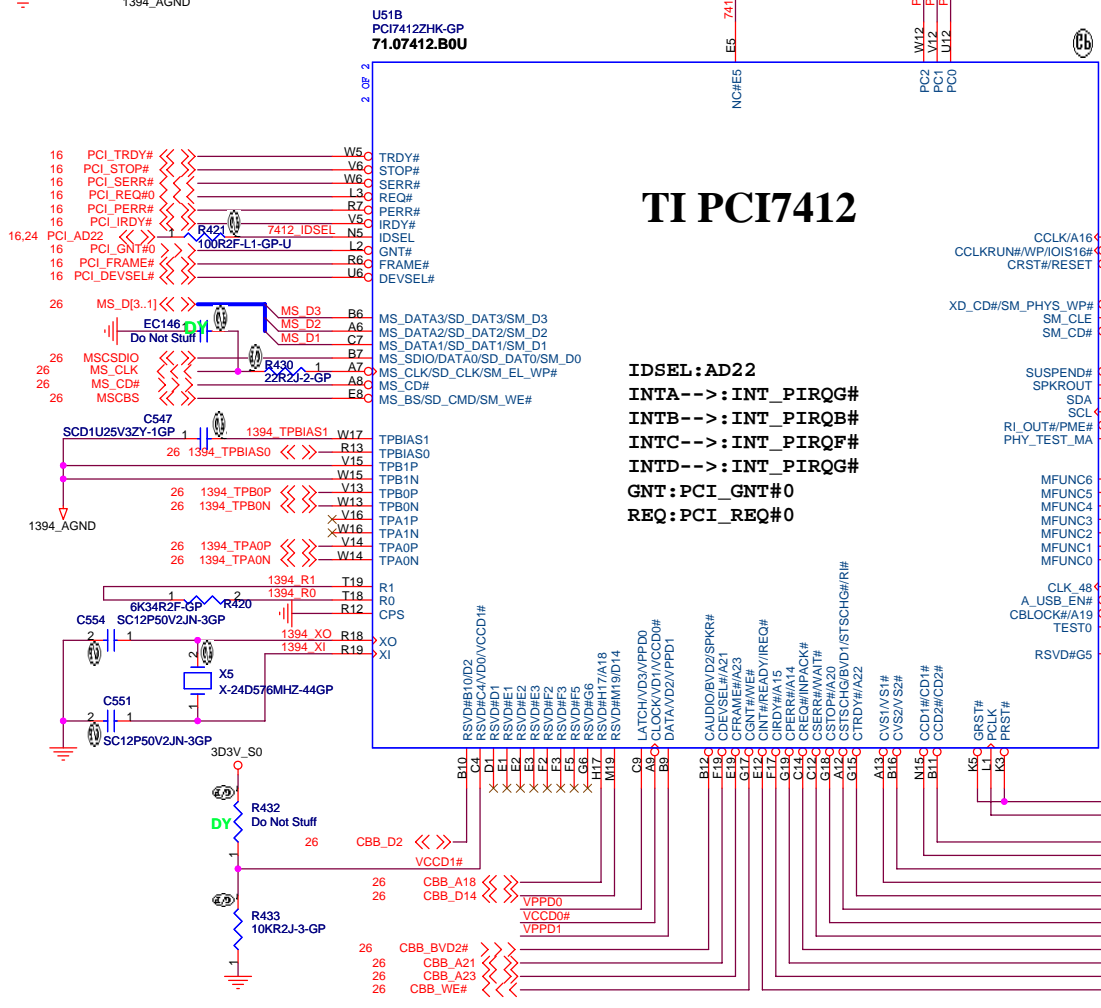
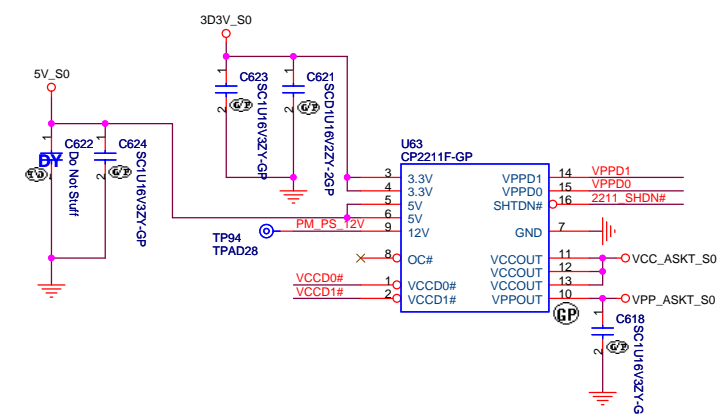
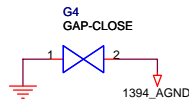
UMA

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Title: **LAN Connector**

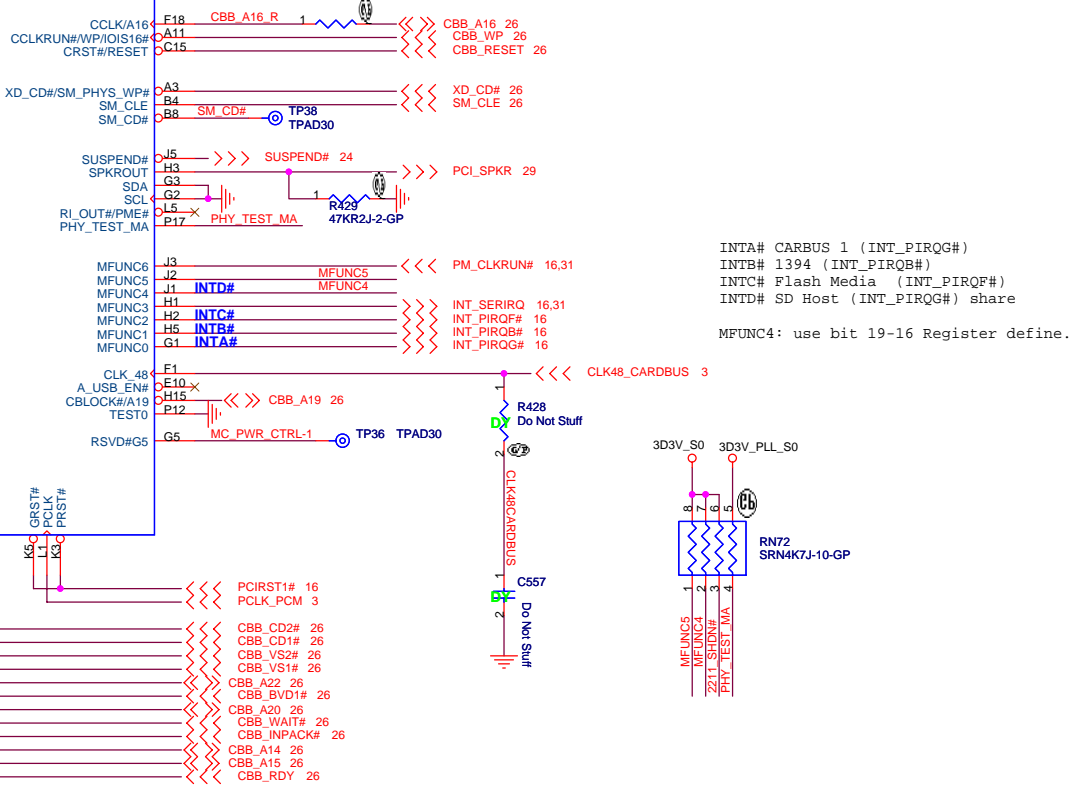
Size A3 Document Number: **Dellen** Rev: **SA**

Date: Tuesday, January 16, 2007 Sheet 23 of 43



TI PCI7412

IDSEL: AD22
INTA---: INT_PIRQ#
INTB---: INT_PIRQ#
INTC---: INT_PIRQ#
INTD---: INT_PIRQ#
GNT: PCI_GNT#0
REQ: PCI_REQ#0



INTA# CARBUS 1 (INT_PIRQ#)
INTB# 1394 (INT_PIRQ#)
INTC# Flash Media (INT_PIRQ#)
INTD# SD Host (INT_PIRQ#) share
MFUNC4: use bit 19-16 Register define.

UMA

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Title: **TI PCI7412 (2 of 2)**

Size: A3 Document Number: Dellén Rev: SA

Date: Tuesday, January 16, 2007 Sheet 25 of 43

PCMCIA Socket

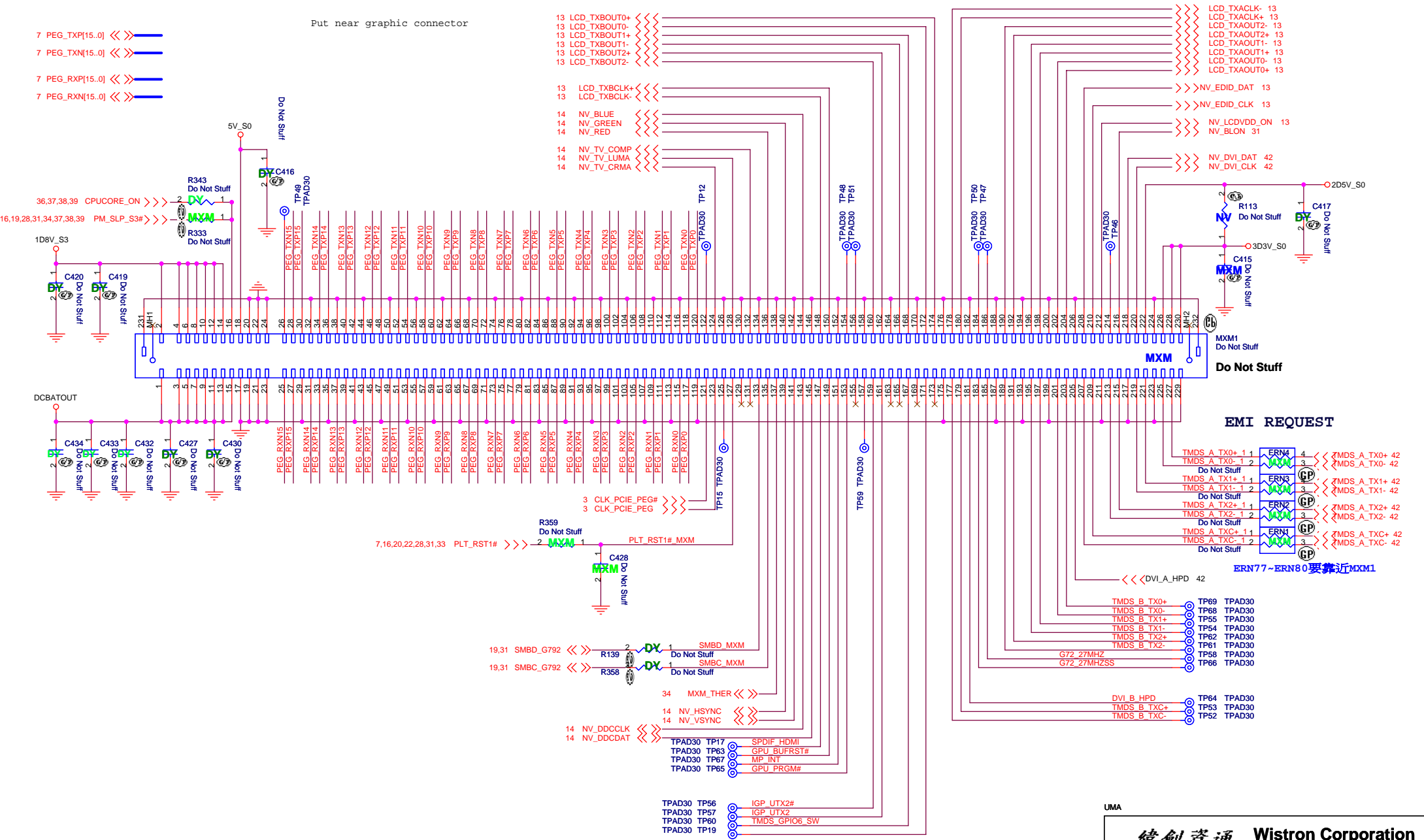
CN1
CARDBUS66P-23GP
62.10024.851

Cardbus I/F

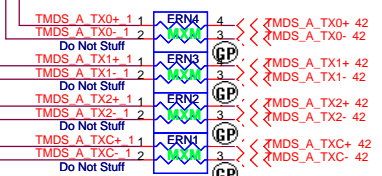
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- CBB_WE# 25
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- CBB_D625 672
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- CBB_D628 675
- CBB_D629 676
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- CBB_D763 810
- CBB_D764 811
- CBB_D765 812
- CBB_D766 813
- CBB_D767 814
- CBB_D768 815
- CBB_D769 816
- CBB_D770 817
- CBB_D771 818
- CBB_D7

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector



EMI REQUEST

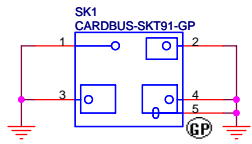


ERN7~ERN8要靠近MXM1

UMA

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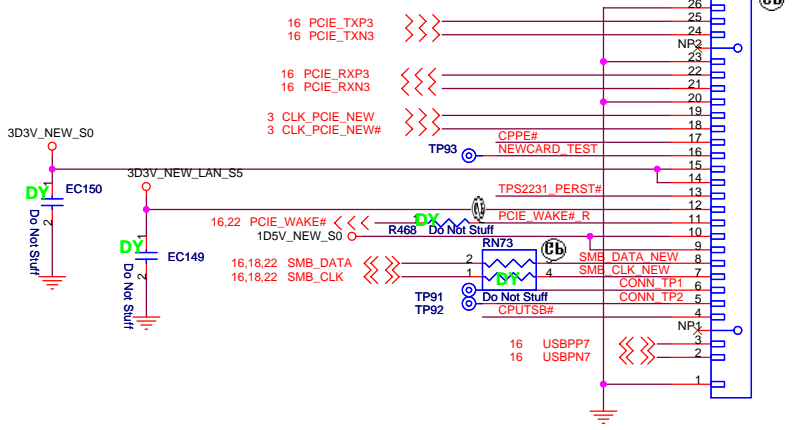
Title Graphic MXM CONN		
Size A3	Document Number Dellen	Rev SA
Date: Tuesday, January 16, 2007	Sheet 27	of 43



NEWCARD Connector

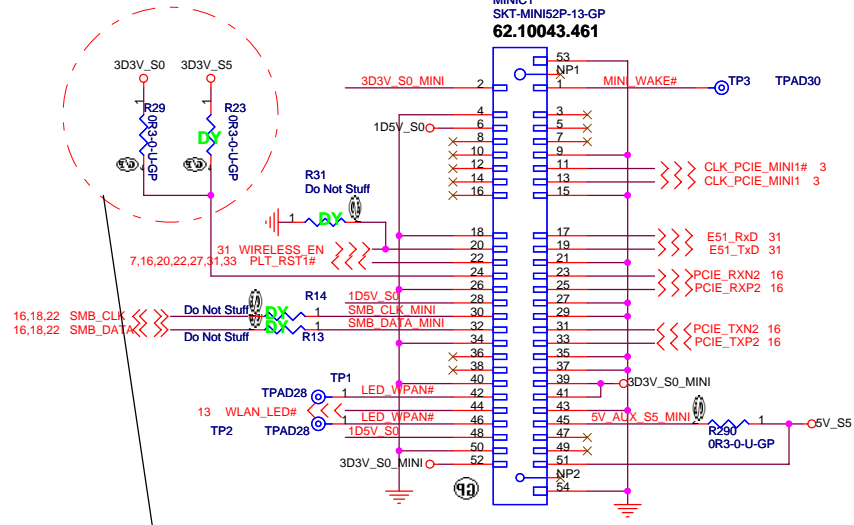
Reserve the symbol
for bottom side
connector

NEW1
CARDBUS26P-8GP
62.10024.881

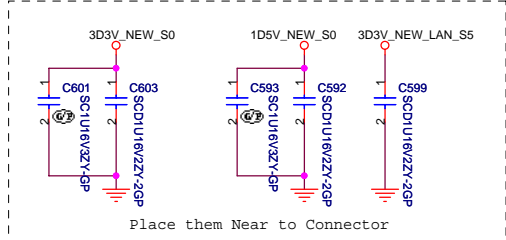
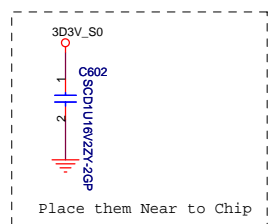
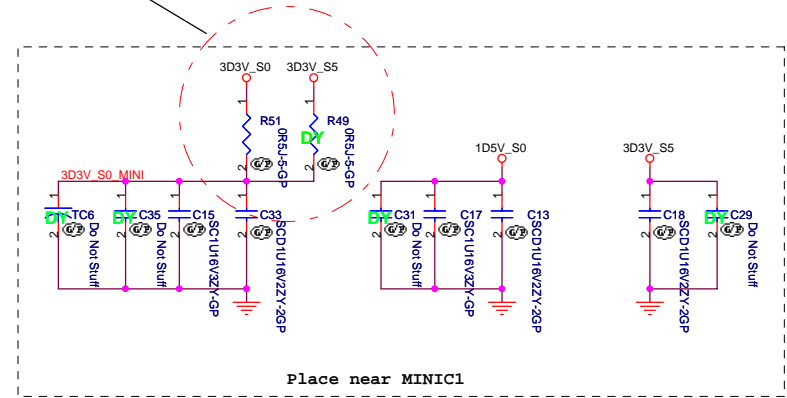
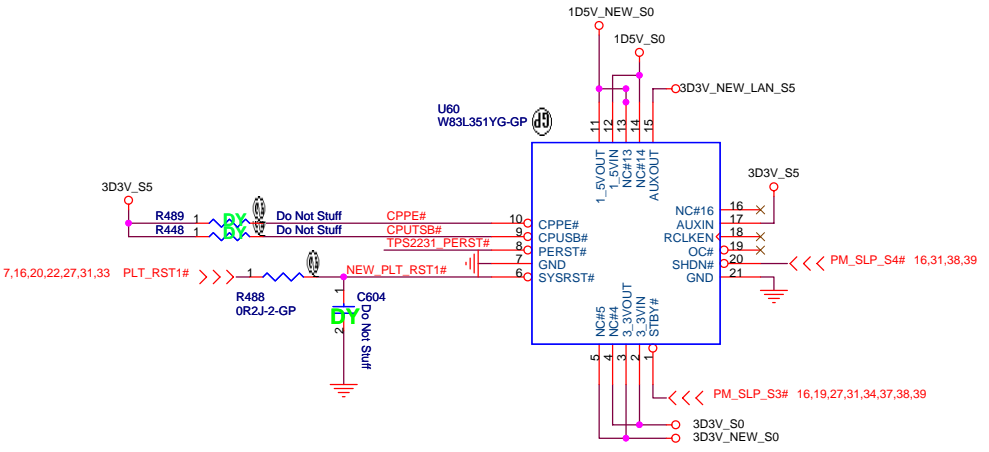


Mini Card Connector

MINIC1
SKT-MINI52P-13-GP
62.10043.461



PCIE Mini Card For WLA W/O iAMT, TV or 3G



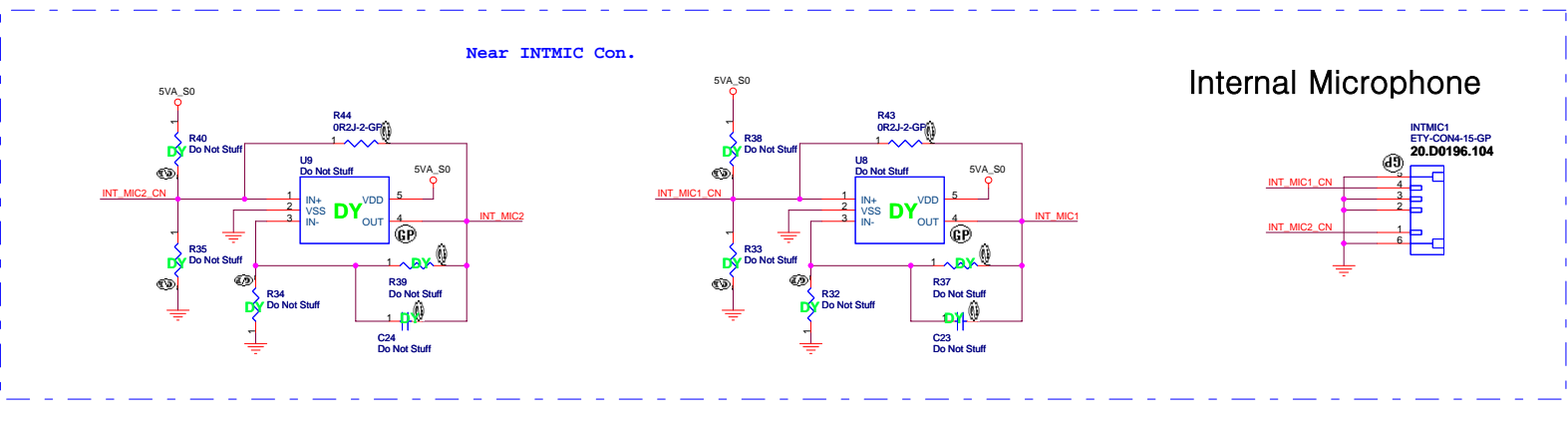
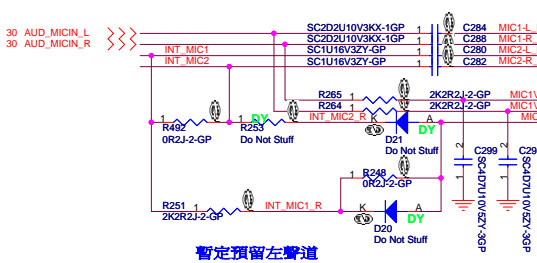
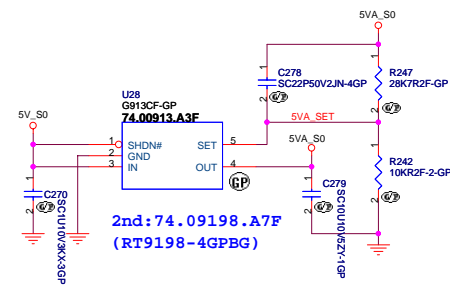
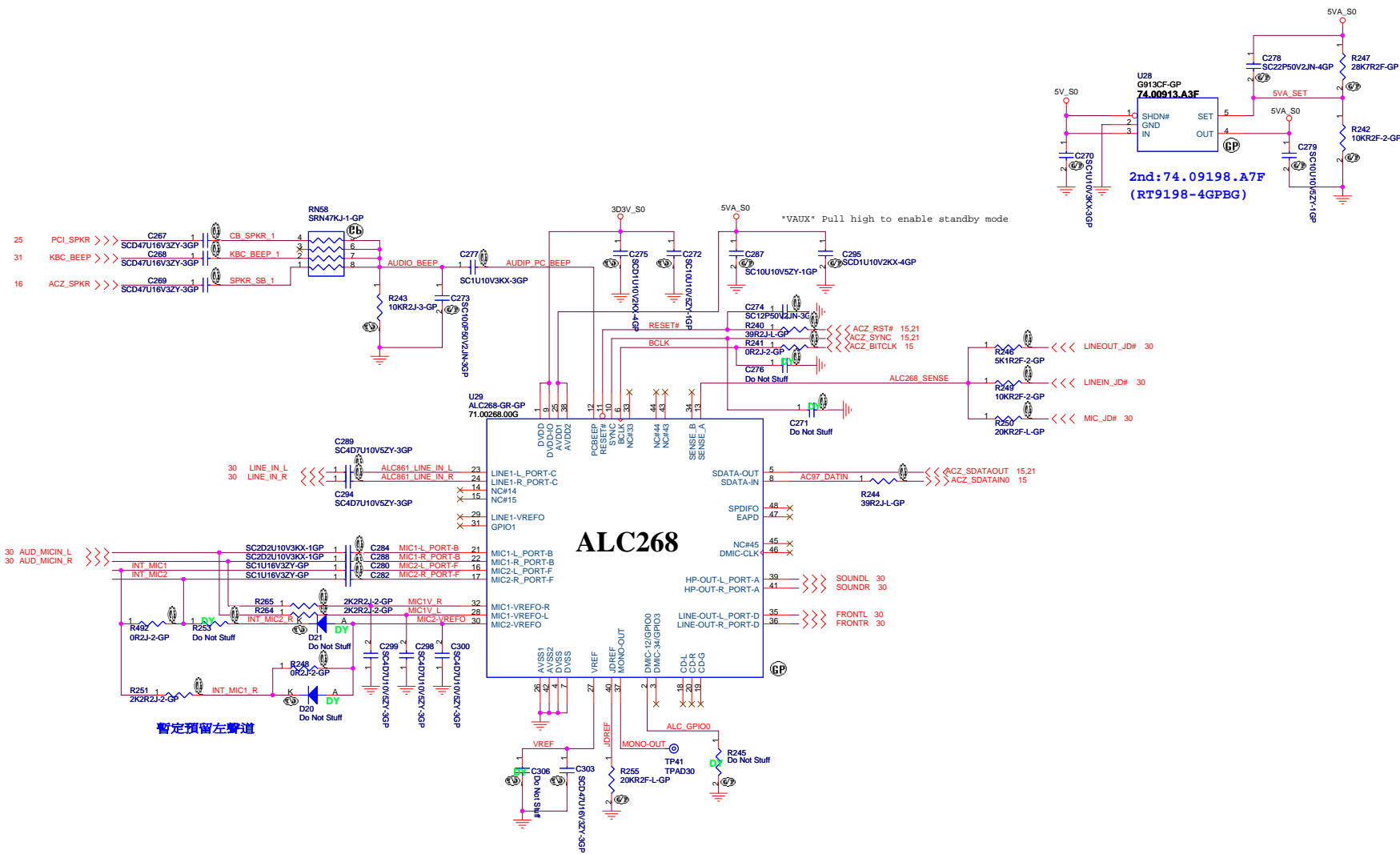
UMA

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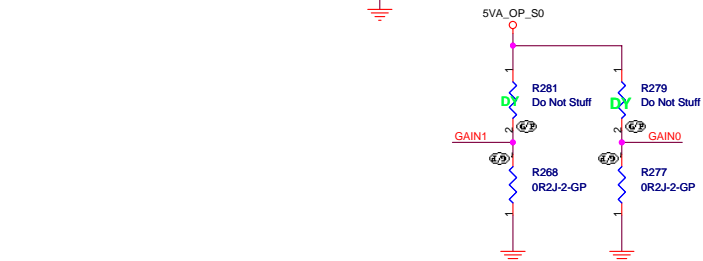
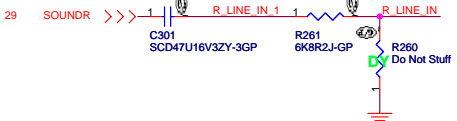
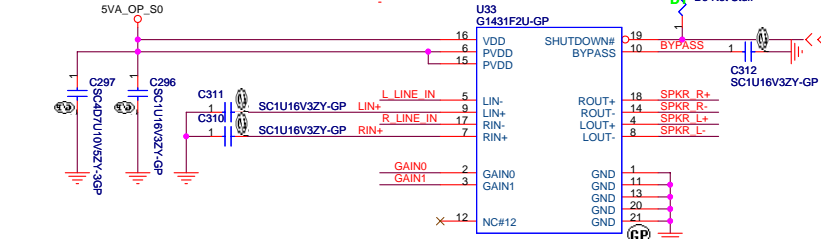
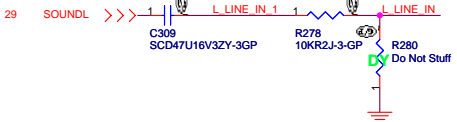
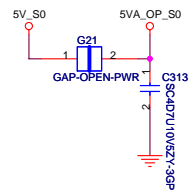
Title: **MINI CARD / NEW CARD**

Size: A3, Document Number: **Dellen**, Rev: SA

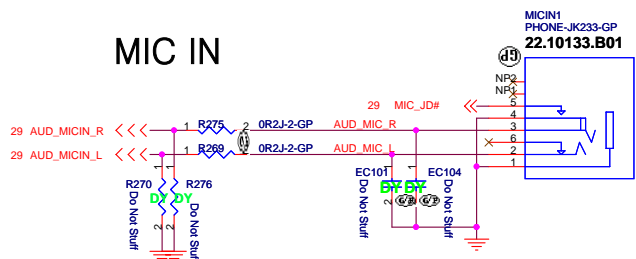
Date: Tuesday, January 16, 2007, Sheet: 28 of 43



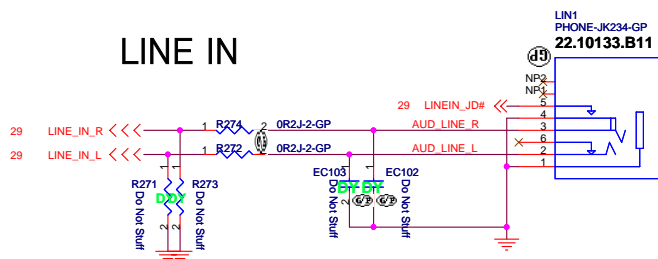
AUDIO OP AMPLIFIER



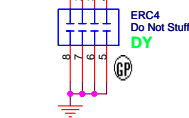
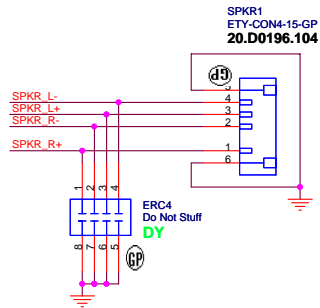
MIC IN



LINE IN



Internal Speaker

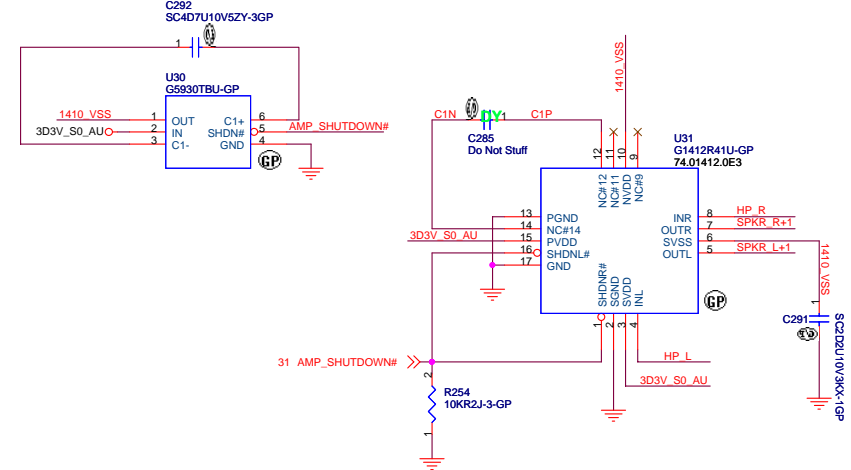
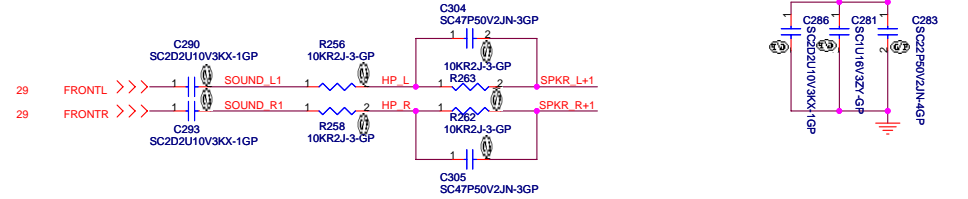


R,L 1.5W Speaker
 mount R274,R281
 R269->63.36334.1DL
 R268->63.33334.1DL

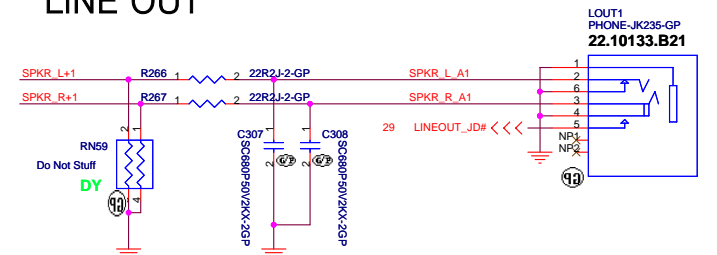
R,L 1W Speaker
 mount R280,R281
 R269->63.15334.1DL
 R268->63.12334.1DL

R,L 1.2W Speaker
 mount R280,R281
 R269->63.10334.1DL
 R268->63.68234.1DL

KBC_MUTE_GPIO8



LINE OUT



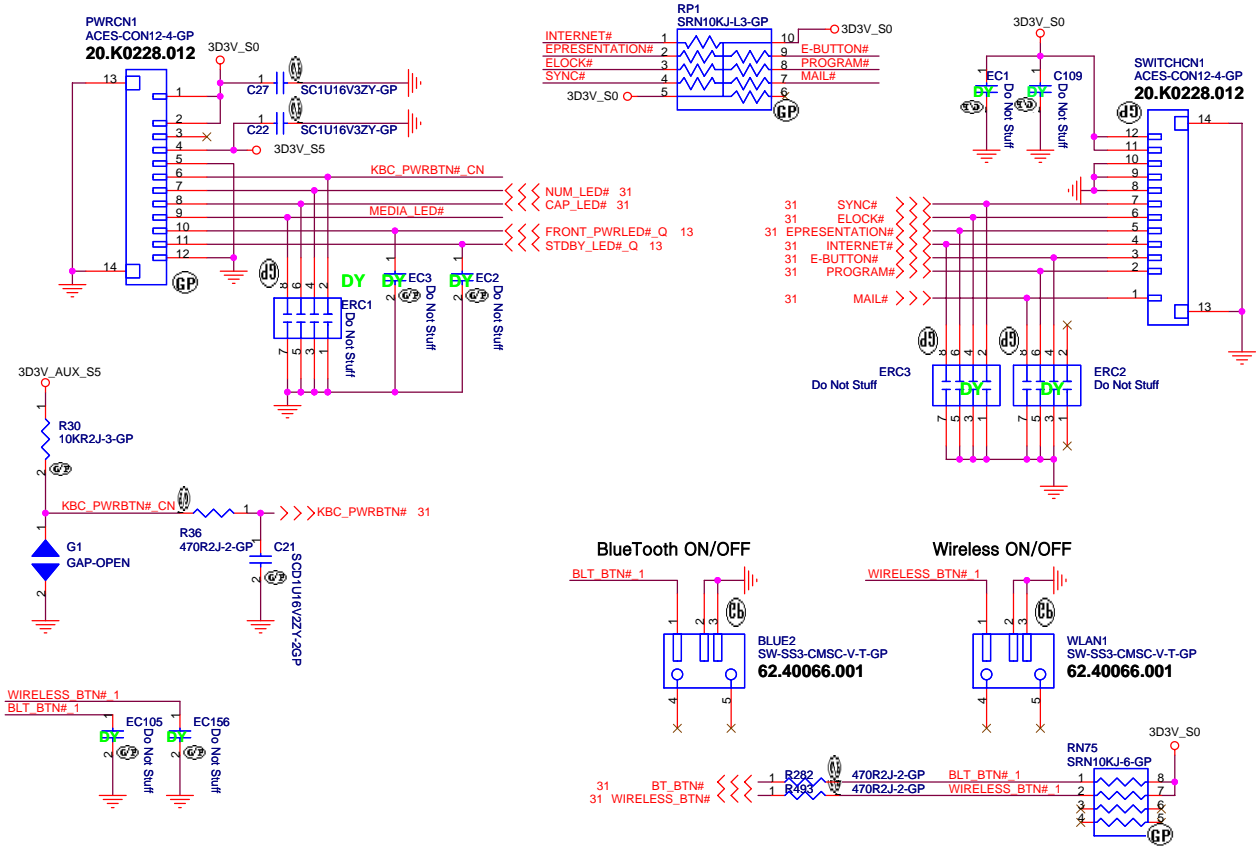
UMA

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 Taipei Hsien 221, Taiwan, R.O.C.

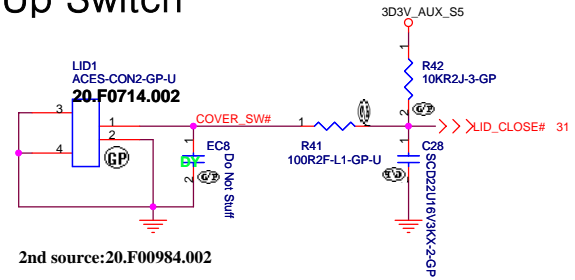
Title: **AUDIO AMP AND JACK**

Size: Custom Document Number: Dellen Rev: SA

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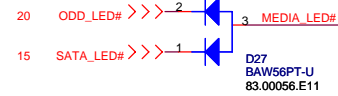
Cover Up Switch



Check test point

- 3D3V_AUX_S5 ○ ○ TP86 TPAD30
- 3D3V_S5 ○ ○ TP90 TPAD30
- 5V_S5 ○ ○ TP89 TPAD30
- 16,31 PM_PWRBTN# <<< ○ TP88 TPAD30
- 4,15,34 H_PWRGD <<< ○ TP9 TPAD30
- 31,37 SS_ENABLE <<< ○ TP87 TPAD30
- 4,6 H_CPURST# <<< ○ TP45 TPAD30

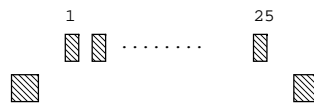
Test Point 放在 Dimm Door 打開可量測處



EMI Bypass cap.

KCOL13	EC32	1	SC220P50V2JN-3GP
KCOL14	EC33	1	SC220P50V2JN-3GP
KCOL15	EC34	1	SC220P50V2JN-3GP
KCOL16	EC35	1	SC220P50V2JN-3GP
KCOL5	EC28	1	SC220P50V2JN-3GP
KCOL6	EC29	1	SC220P50V2JN-3GP
KCOL7	EC30	1	SC220P50V2JN-3GP
KCOL8	EC31	1	SC220P50V2JN-3GP
KCOL1	EC46	1	SC220P50V2JN-3GP
KCOL2	EC47	1	SC220P50V2JN-3GP
KCOL3	EC48	1	SC220P50V2JN-3GP
KCOL4	EC49	1	SC220P50V2JN-3GP
KCOL17	EC36	1	SC220P50V2JN-3GP
KCOL18	EC37	1	SC220P50V2JN-3GP
KROW8	EC41	1	SC220P50V2JN-3GP
KROW7	EC40	1	SC220P50V2JN-3GP
KROW6	EC39	1	SC220P50V2JN-3GP
KROW5	EC38	1	SC220P50V2JN-3GP
KROW4	EC57	1	SC220P50V2JN-3GP
KROW3	EC56	1	SC220P50V2JN-3GP
KROW2	EC55	1	SC220P50V2JN-3GP
KROW1	EC54	1	SC220P50V2JN-3GP
KCOL9	EC50	1	SC220P50V2JN-3GP
KCOL10	EC51	1	SC220P50V2JN-3GP
KCOL11	EC52	1	SC220P50V2JN-3GP
KCOL12	EC53	1	SC220P50V2JN-3GP

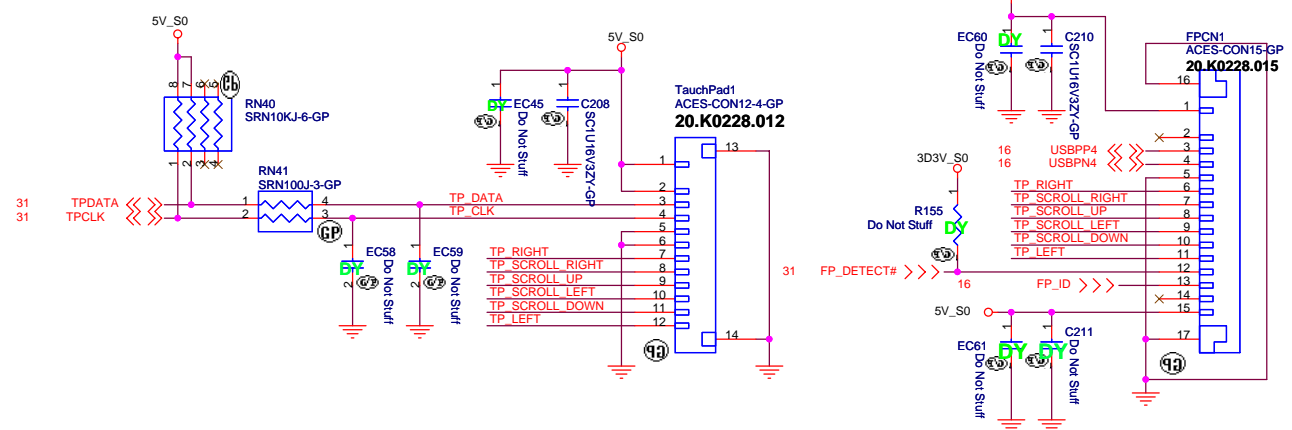
Internal KeyBoard conn.



CHECK KB SPEC. AND PIN DEFINE

>>> KROW[1..8] 31
>>> KCOL[1..18] 31

TouchPad & FingerPad



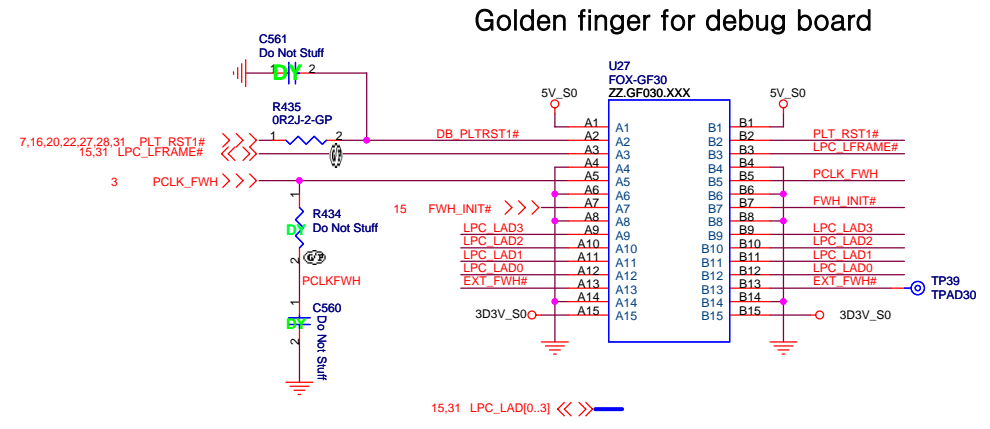
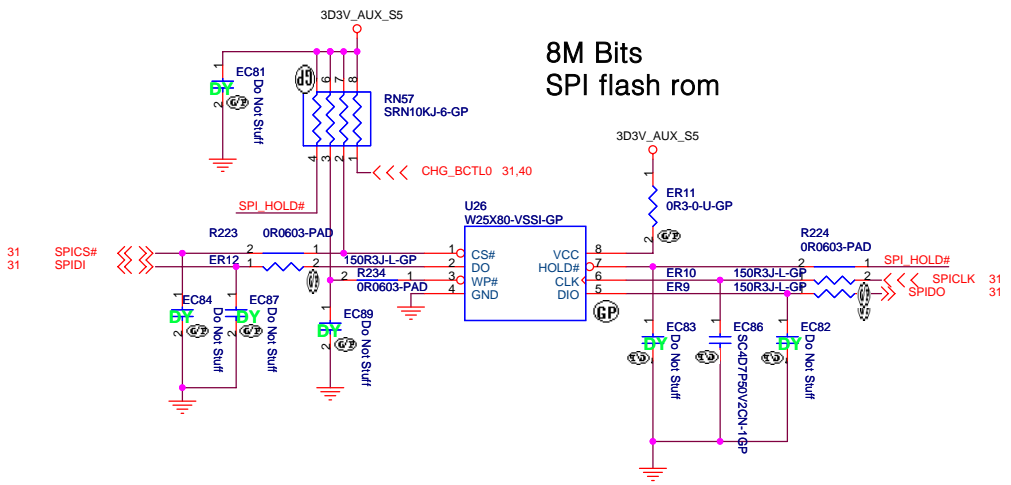
UMA

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Title: **BUTTONS / KB / TOUCHPAD / FP**

Size: A3 Document Number: **Dellen** Rev: SA

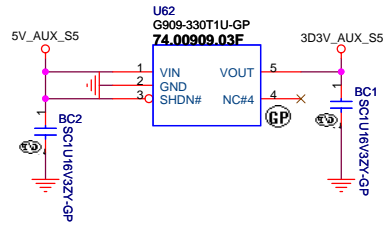
Date: Tuesday, January 16, 2007 Sheet 32 of 43



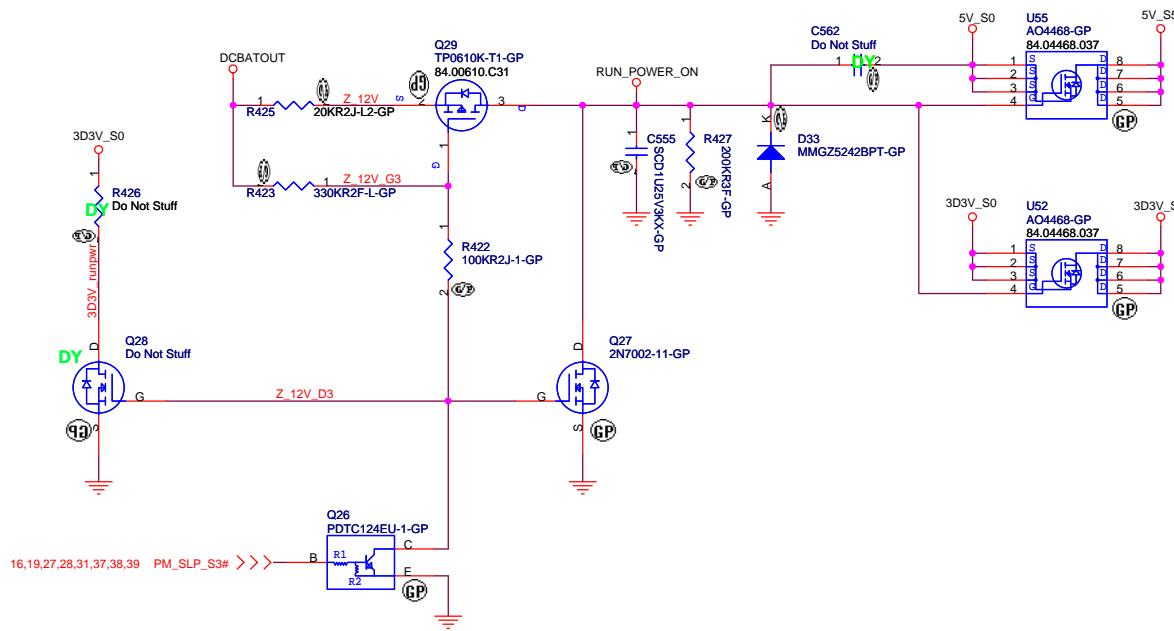
Aux Power

3D3V_AUX_S5

I max = 150 mA

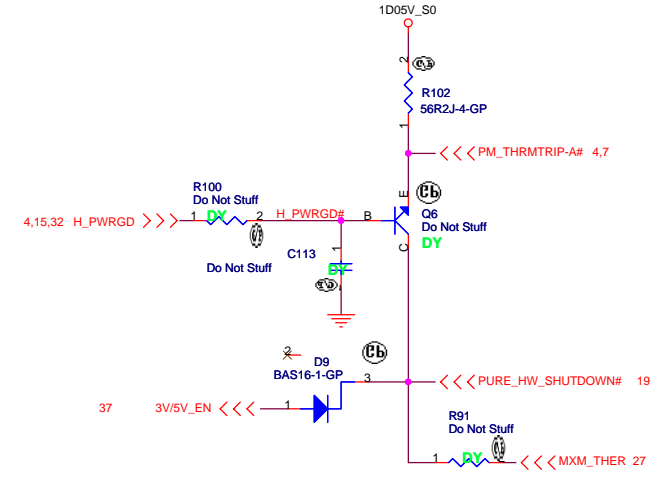


Run Power



5V_S0

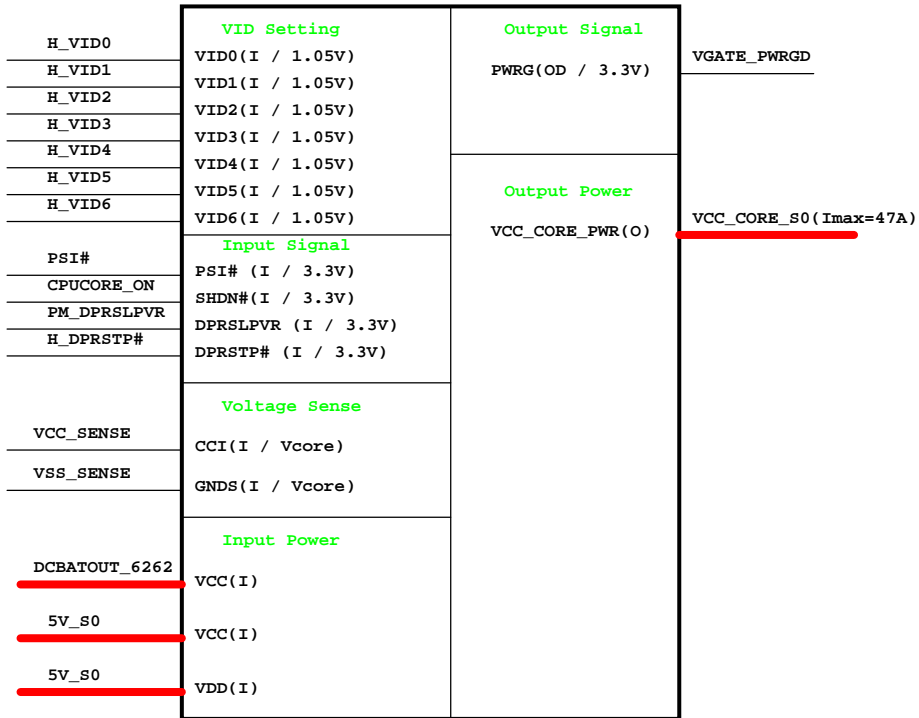
3D3V_S0



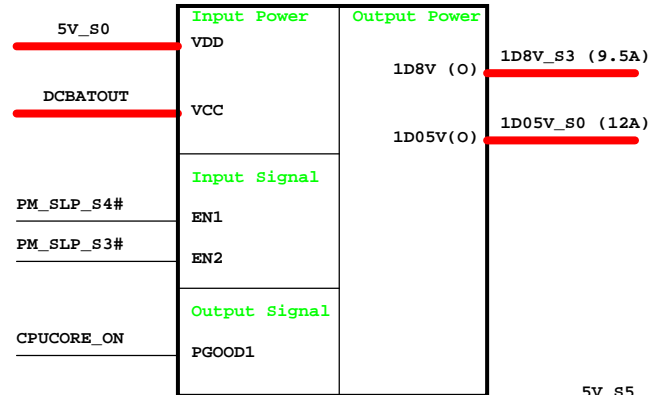
UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
3D3V_AUX_S5 / 3D3V_S0 / 5V_S0		
Size	Document Number	Rev
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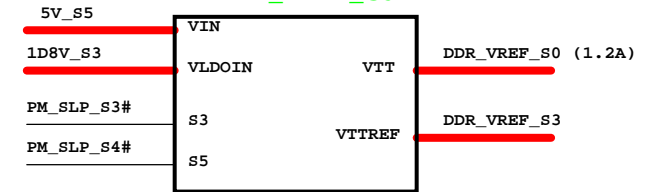
**CPU_CORE
MAX8770**



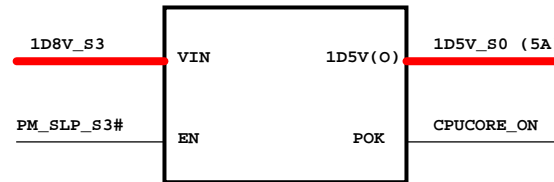
**MAX8717
1D8V_S3 / 1D05V_S0**



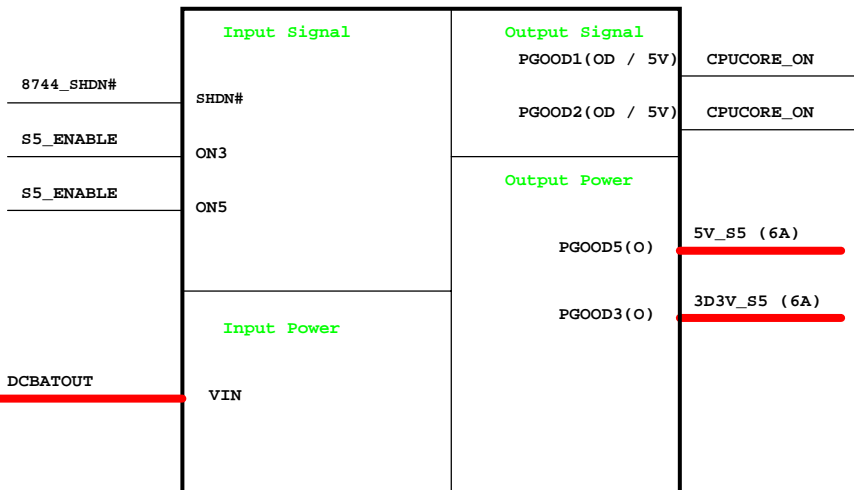
**TPS51100
DDR_VREF_S0**



**APL5912
1D5V_S0**



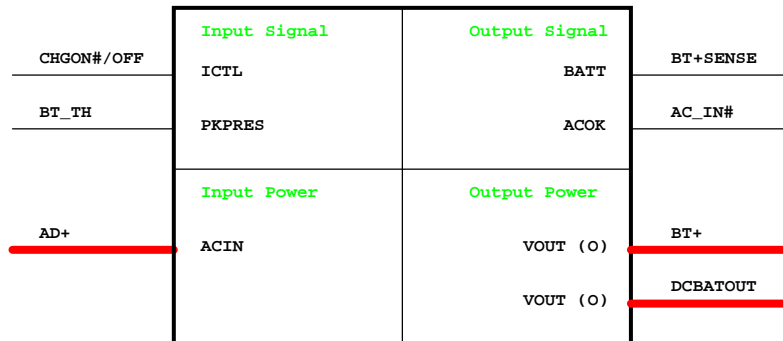
**MAX8744
5V_S5 / 3D3V_S5**



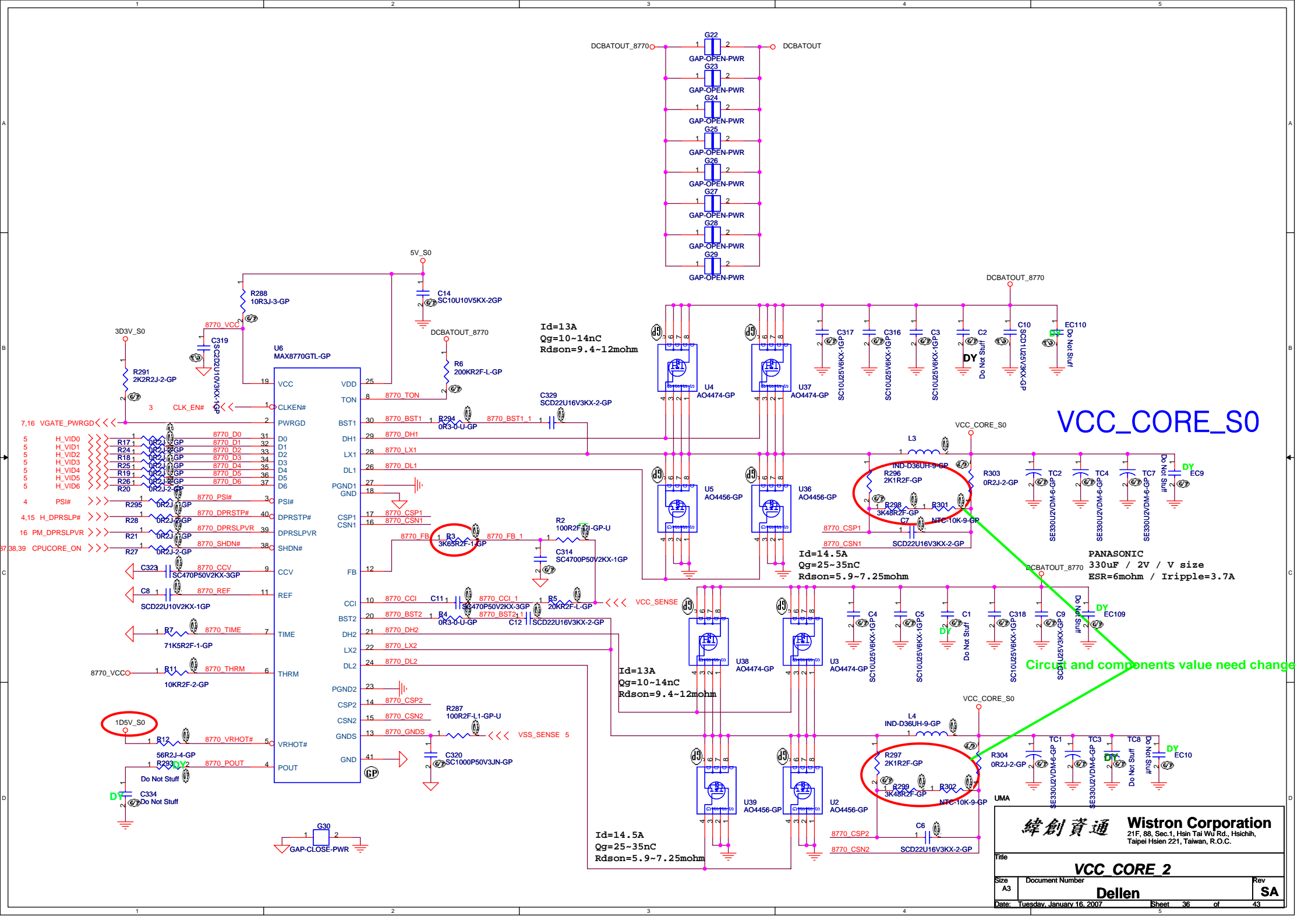
**APL5312
2D5V_S0**



Charger ISL6255



UMA		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Power Block Diagram			
Size: A3	Document Number: Dellen	Rev: SA	
Date: Tuesday, January 16, 2007 Sheet 35 of 43			



$I_d=13A$
 $Q_g=10\sim14nC$
 $R_{dson}=9.4\sim12mohm$

$I_d=14.5A$
 $Q_g=25\sim35nC$
 $R_{dson}=5.9\sim7.25mohm$

$I_d=14.5A$
 $Q_g=25\sim35nC$
 $R_{dson}=5.9\sim7.25mohm$

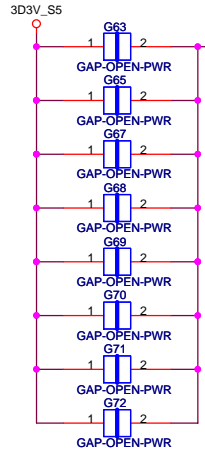
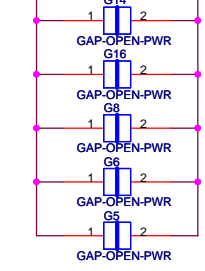
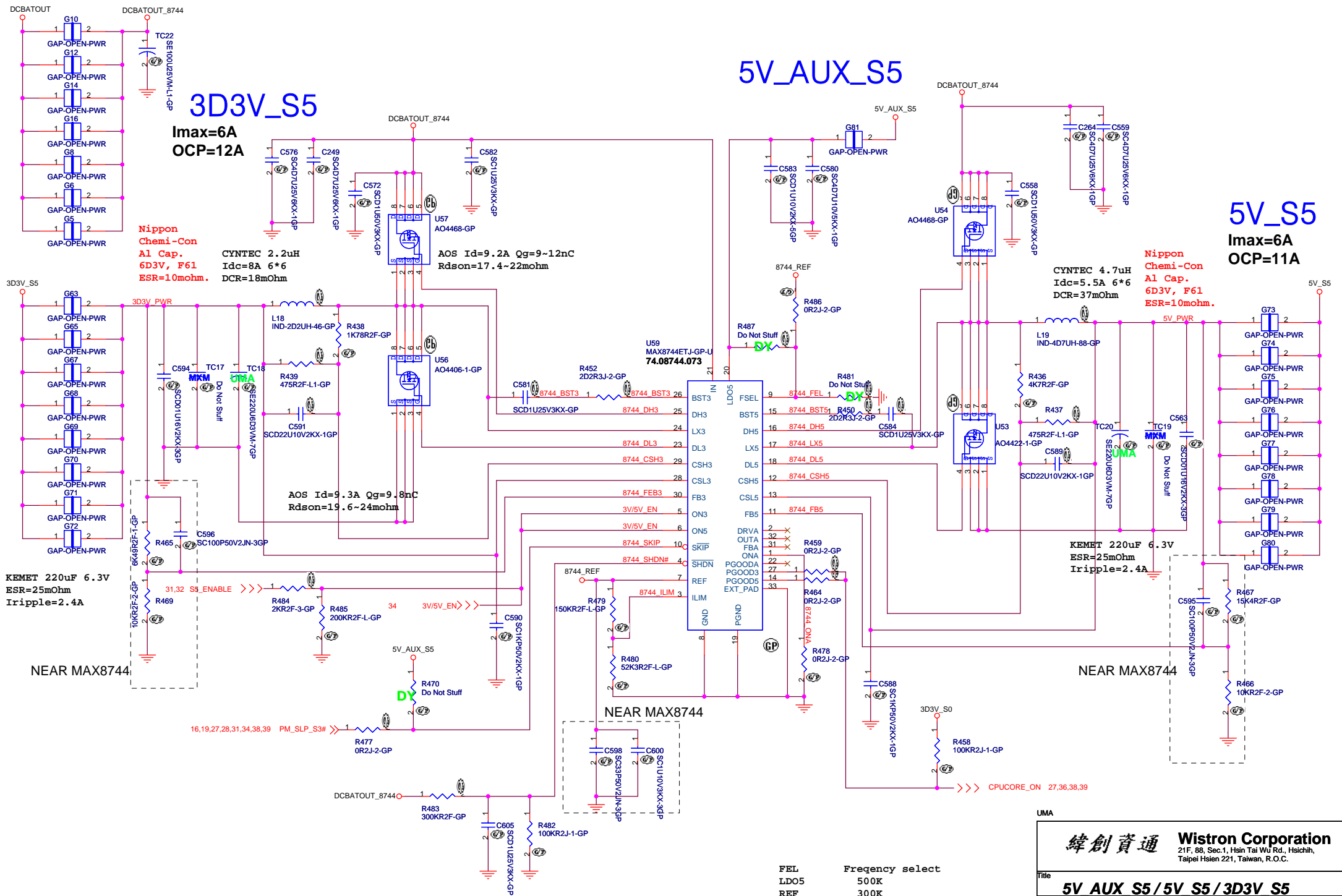
VCC_CORE_S0

PANASONIC
 330uF / 2V / V size
 ESR=6mohm / Irripple=3.7A

Circuit and components value need change

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 Taipei Hsien 221, Taiwan, R.O.C.

Title		
VCC CORE 2		
Size	Document Number	Rev
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Date: Tuesday, January 16, 2007	Sheet 36	of 43



KEMET 220uF 6.3V
ESR=25mOhm
Iripple=2.4A

NEAR MAX8744

3D3V_S5

I_{max}=6A
OCP=12A

Nippon Chemi-Con Al Cap.
6D3V, F61
ESR=1.0mohm, DCR=18mOhm

CYNTec 2.2uH
I_{dc}=8A 6*6

AOS I_d=9.2A Q_g=9~12nC
R_{dson}=17.4~22mohm

AOS I_d=9.3A Q_g=9.8nC
R_{dson}=19.6~24mohm

5V_AUX_S5

5V_S5

I_{max}=6A
OCP=11A

CYNTec 4.7uH
I_{dc}=5.5A 6*6
DCR=37mOhm

Nippon Chemi-Con Al Cap.
6D3V, F61
ESR=1.0mohm.

KEMET 220uF 6.3V
ESR=25mOhm
Iripple=2.4A

NEAR MAX8744

FEL	Frequency select
LDO5	500K
REF	300K
GND	200K

UMA

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Title: **5V AUX S5/5V S5/3D3V S5**

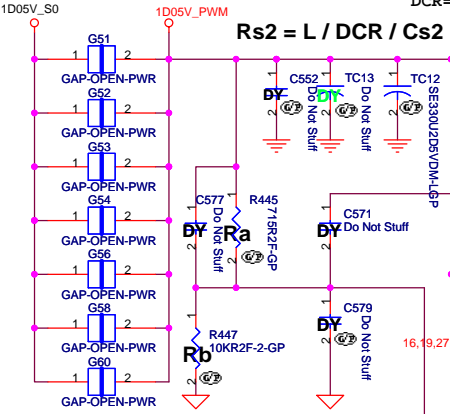
Size: A3 Document Number: **Dellen** Rev: **SA**

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1D05V_S0

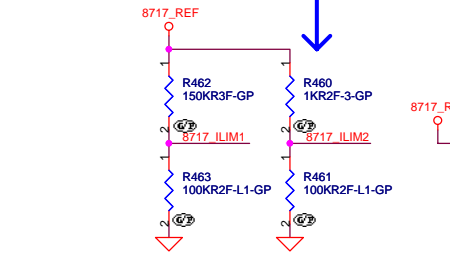
1D05V I_{omax}=12A
OCP>19A

V_{cal} = 1.0511V



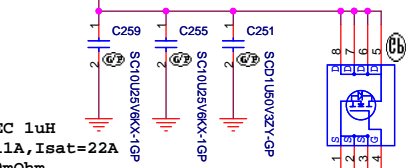
$V_{out} = (1 + R_a/R_b) \cdot I$
Panasonic 330uF
2.5V ESR=15mOhm
I_{ripple}=3.1A

Adjust the current limit threshold from R14, R15

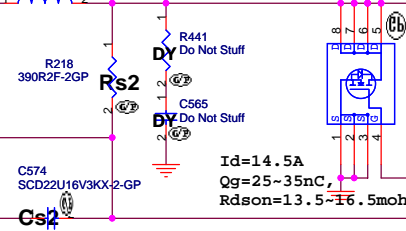


V_{ILIM} = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - di/2

Id=13A
Qg=10~14nC,
R_{dson}=9.4~12mohm



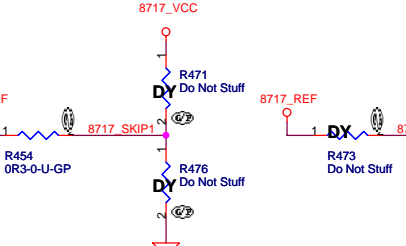
$R_{s2} = L / DCR / C_{s2}$



Id=14.5A
Qg=25~35nC,
R_{dson}=13.5~16.5mohm



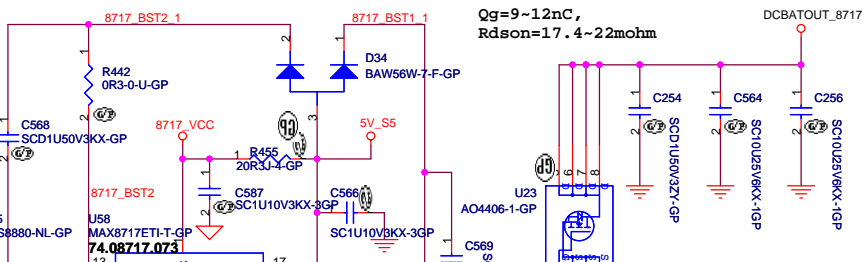
SKIP
VCC=Force PWM
REF=Low noise
GND= Pulse Skipping



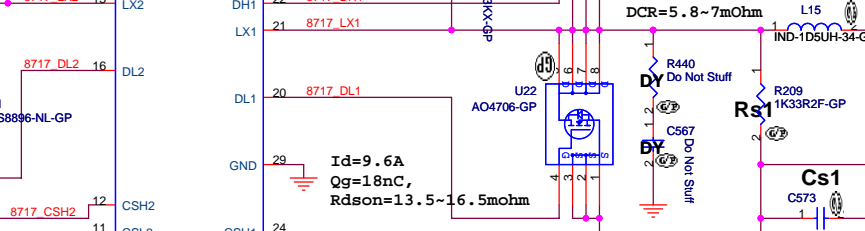
1D8V_S3

I_{omax}=9.5A
OCP>17A

V_{cal} = 1.8V



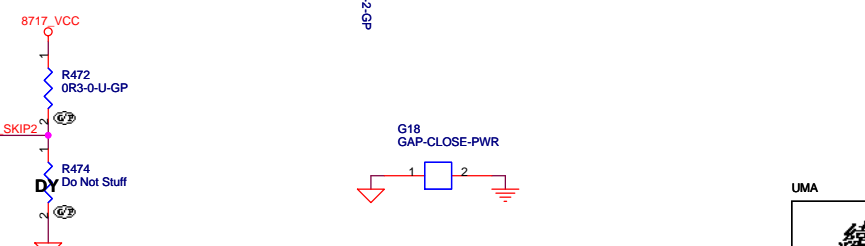
$R_{s1} = L / DCR / C_{s1}$



Id=9.6A
Qg=18nC,
R_{dson}=13.5~16.5mohm



FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz



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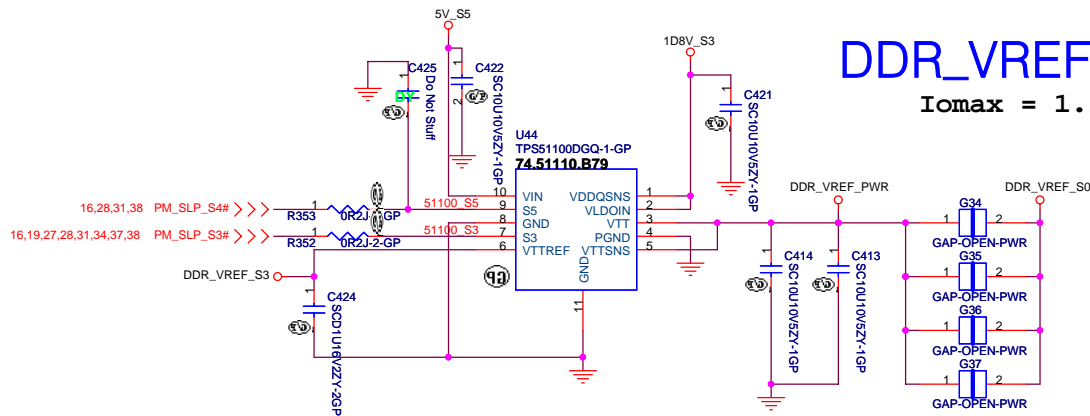
Title: **MAX8717 1D8V S3/1D05V S0**

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DDR_VREF_S0

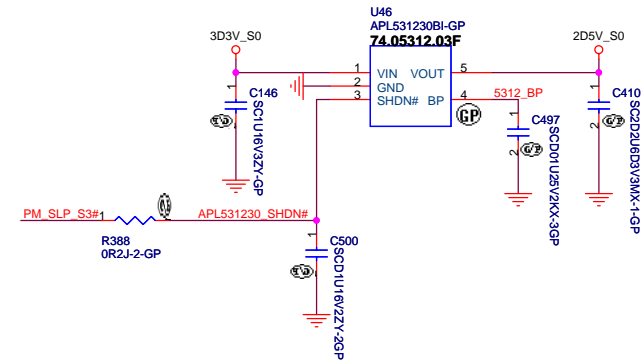
I_{omax} = 1.2A



DDR_VREF_S3

2D5V_S0

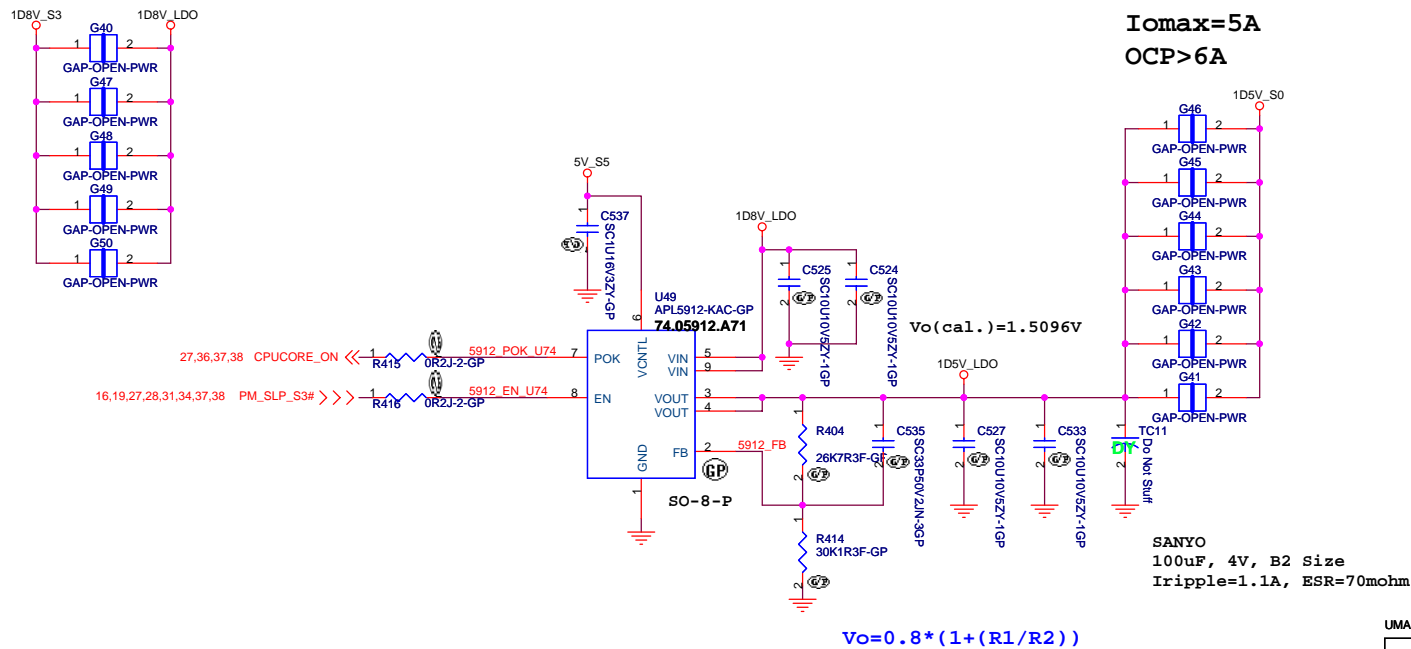
I_{omax} = 130mA



1D5V_S0

I_{omax}=5A

OCP>6A

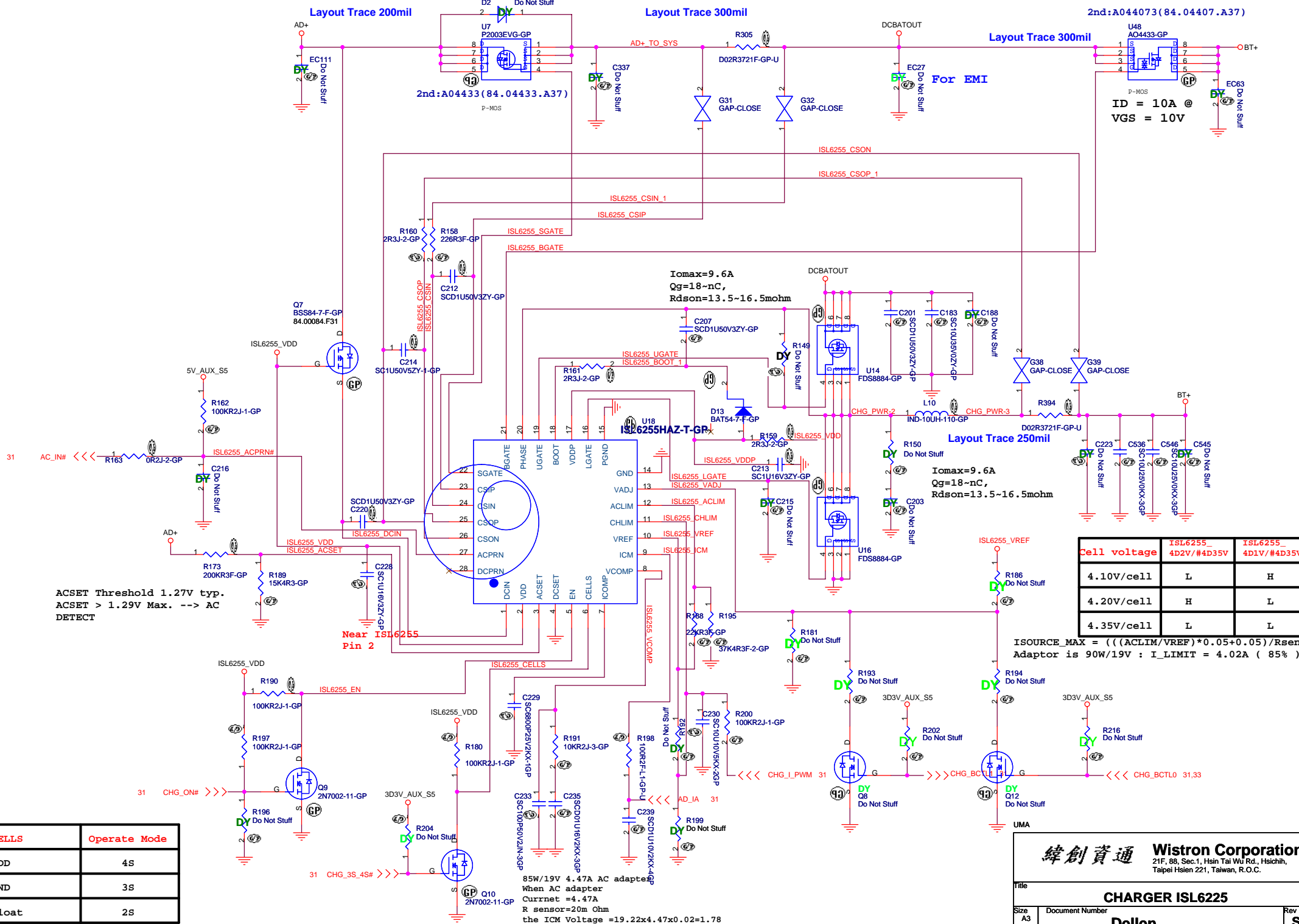


$$V_o = 0.8 * (1 + (R1/R2))$$

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Taipei Hsien 221, Taiwan, R.O.C.

Title 1D5V_S0 / 2D5V_S0 / DDR_VREF_S0		
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Layout Trace 200mil Layout Trace 300mil Layout Trace 300mil

2nd:A04433(84.04433.A37)

2nd:A044073(84.04407.A37)

ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --> AC
DETECT

I_omax=9.6A
Q_g=18-nC,
R_{dson}=13.5~16.5mohm

I_omax=9.6A
Q_g=18-nC,
R_{dson}=13.5~16.5mohm

Cell voltage	ISL6255_4D2V/#4D35V	ISL6255_4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

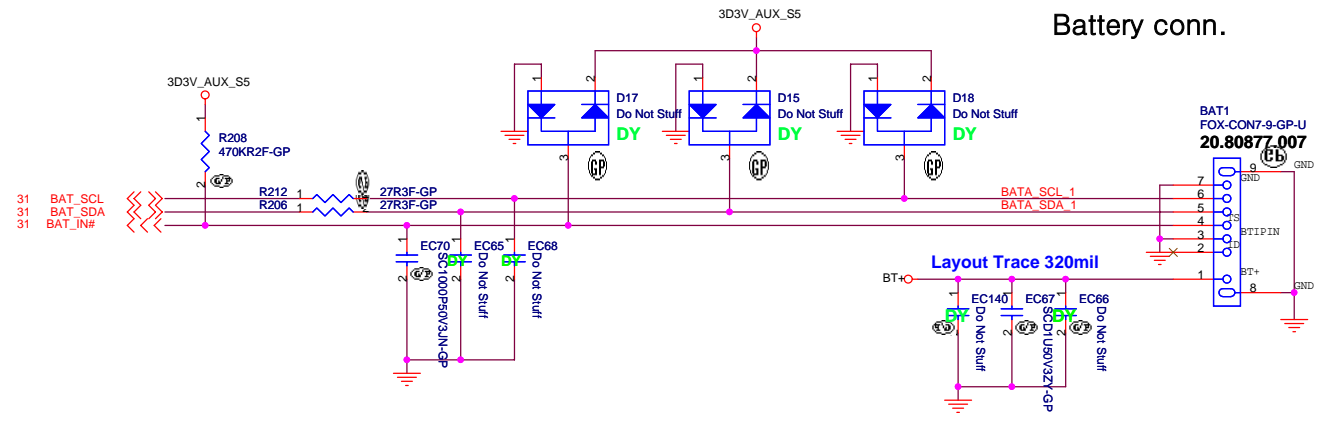
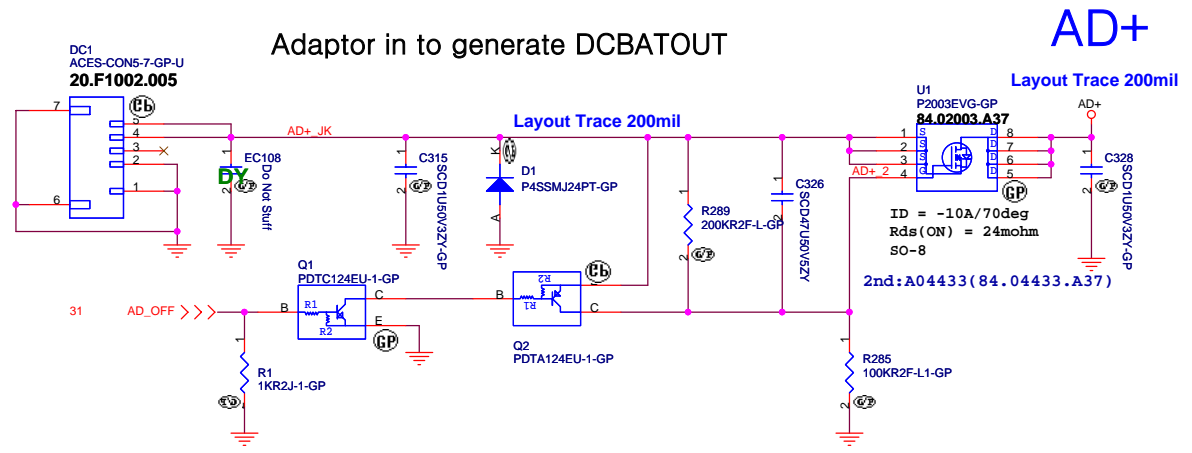
CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

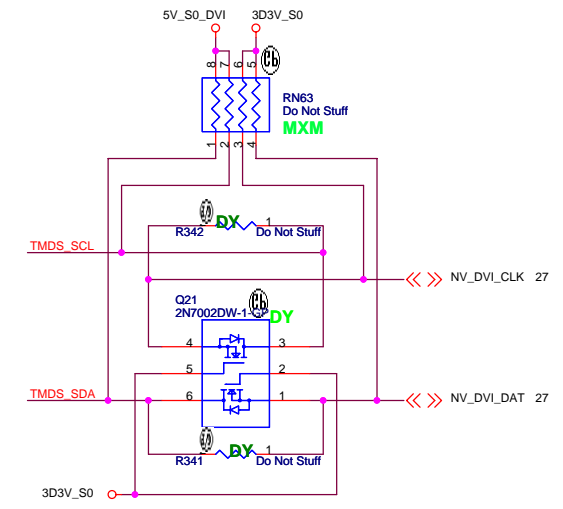
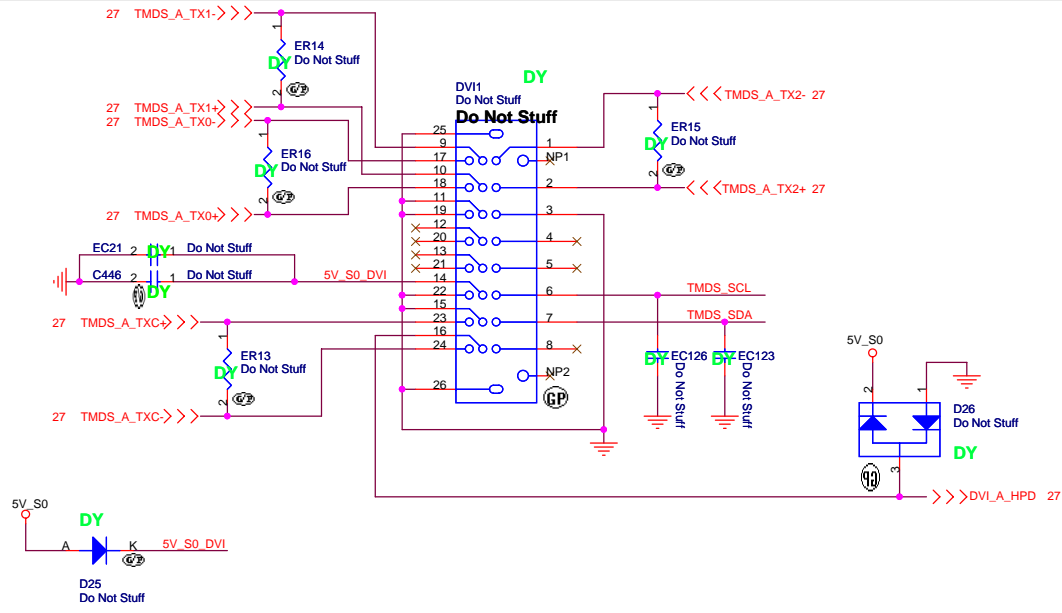
85W/19V 4.47A AC adapter
When AC adapter
Current =4.47A
R sensor=20m Ohm
the ICM Voltage =19.22x4.47x0.02=1.78

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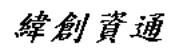
CHARGER ISL6255

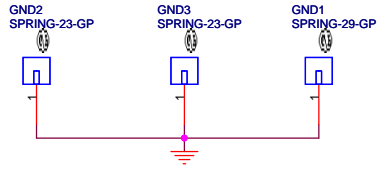
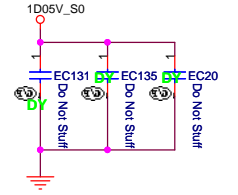
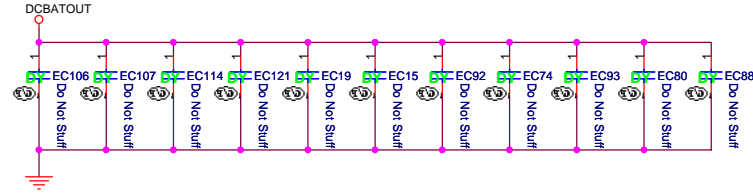
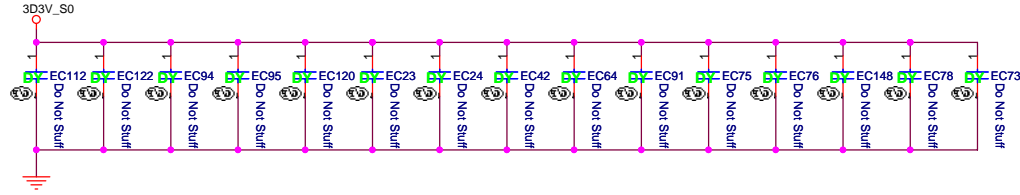
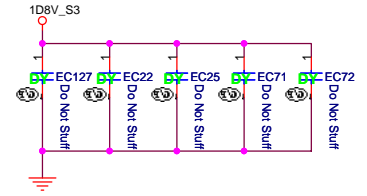
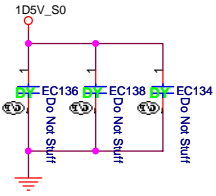
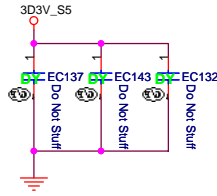
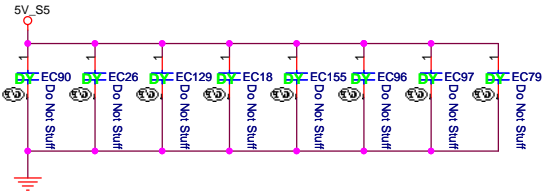
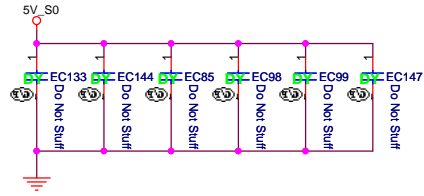
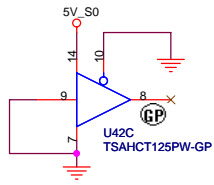
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DVI CONNECTOR		
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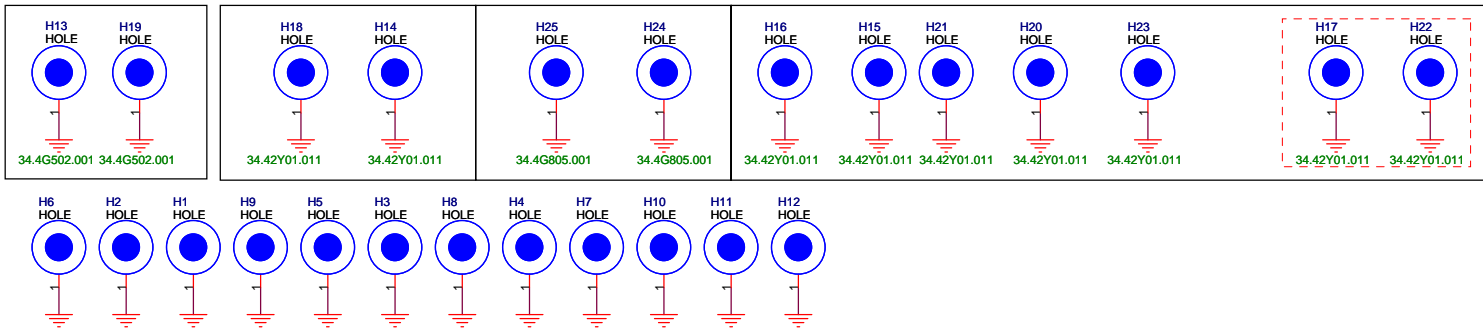


Spring

GND 1 : 34.42T14.001
GND 2/3 : 34.39S07.003

MINI CARD

Fan



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Title	EMI / Spring / Boss		
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A3			
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