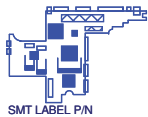


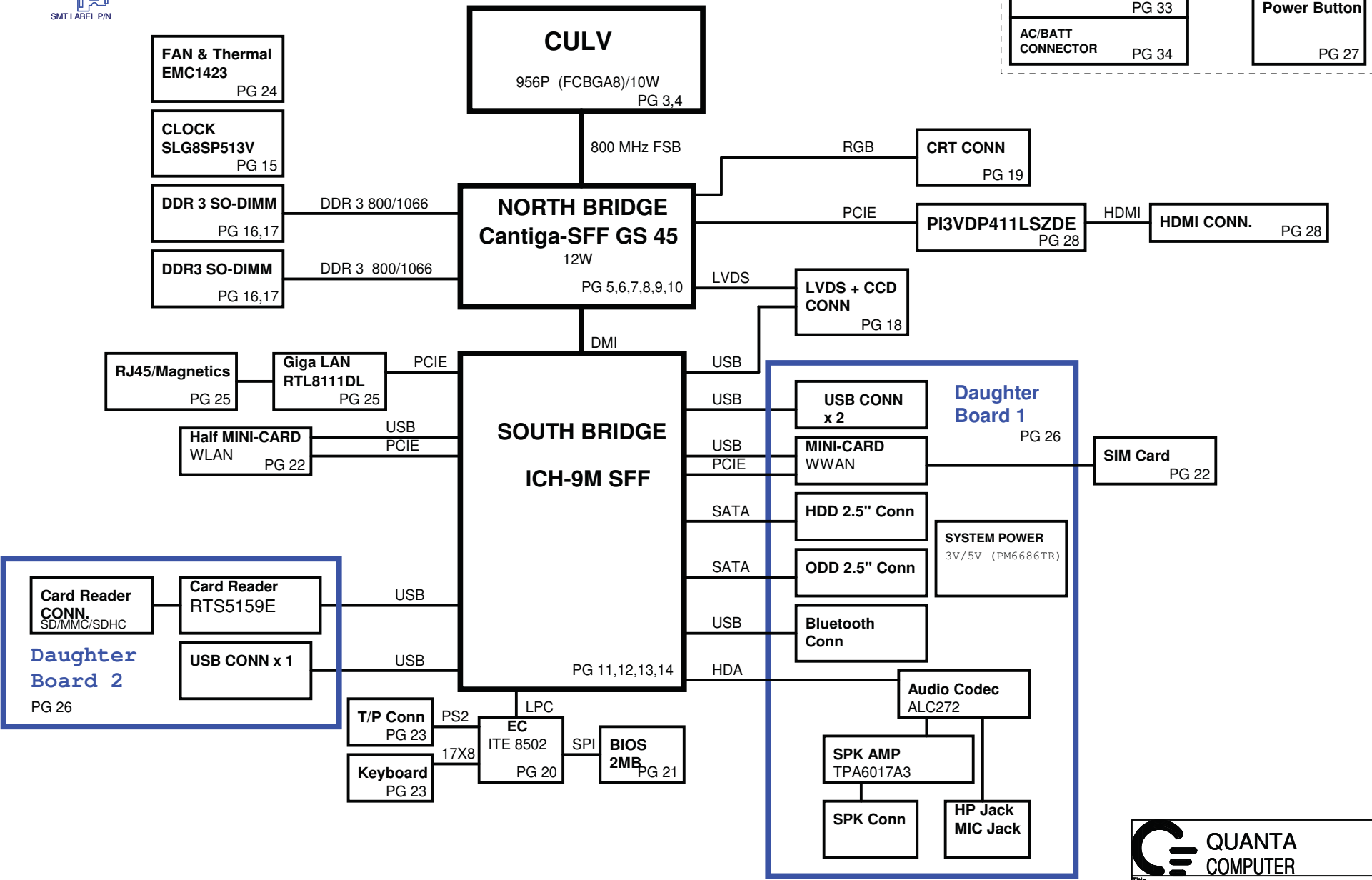
# 14" & 15.6" ULV + GS45 Block Diagram

<http://hobi-elektronika.net>

Rev: X01



POWER	
1.5VSUS & 0.75VTT (RT8207A) PG 32	CHARGER (MAX8731A) PG 29
CPU CORE(ADP3211A) PG 31	1.05_VCCP(OZ8116) PG 30
RUN POWER SW PG 33	Power Button PG 27
AC/BATT CONNECTOR PG 34	



**QUANTA COMPUTER**








Title: Index & Power Status

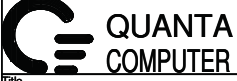
Size: Document Number UM2 UMA Rev 2A

Date: Tuesday, May 26, 2009 Sheet 1 of 36

Table of Contents	
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	CULV
5-10	Cantiga
11-14	ICH9-M
15	Clock Generator
16-17	DDR3 SO-DIMM
18	LCD/CCD
19	CRT
20	SIO(ITE8502)
21	FLASH/RTC
22	WLAN/SIM CONN.
23	TP/KB
24	FAN/THERMAL
25	LAN RTL8111+RJ45
26	IO BOARD CONN.
27	POWER SWITCH
28	HDMI
29	CHARGE MAX8731A
30	1.05VCCP
31	CPU_ADP3211A
32	1.5VSUS & 0.75VTT
33	Run Power Switch
34	DCin & Batt
35	SMBUS BLOCK
36	PAD&SCREW&SPRING

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38,52,53	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
 8731AGND	46	
 AGND_0.9V	49	
 AGND_DC/DC	52	
 AGND_DC2	48	
 AGND_DDR	49	
 AGND_ISL6260	51	
 GND	ALL	

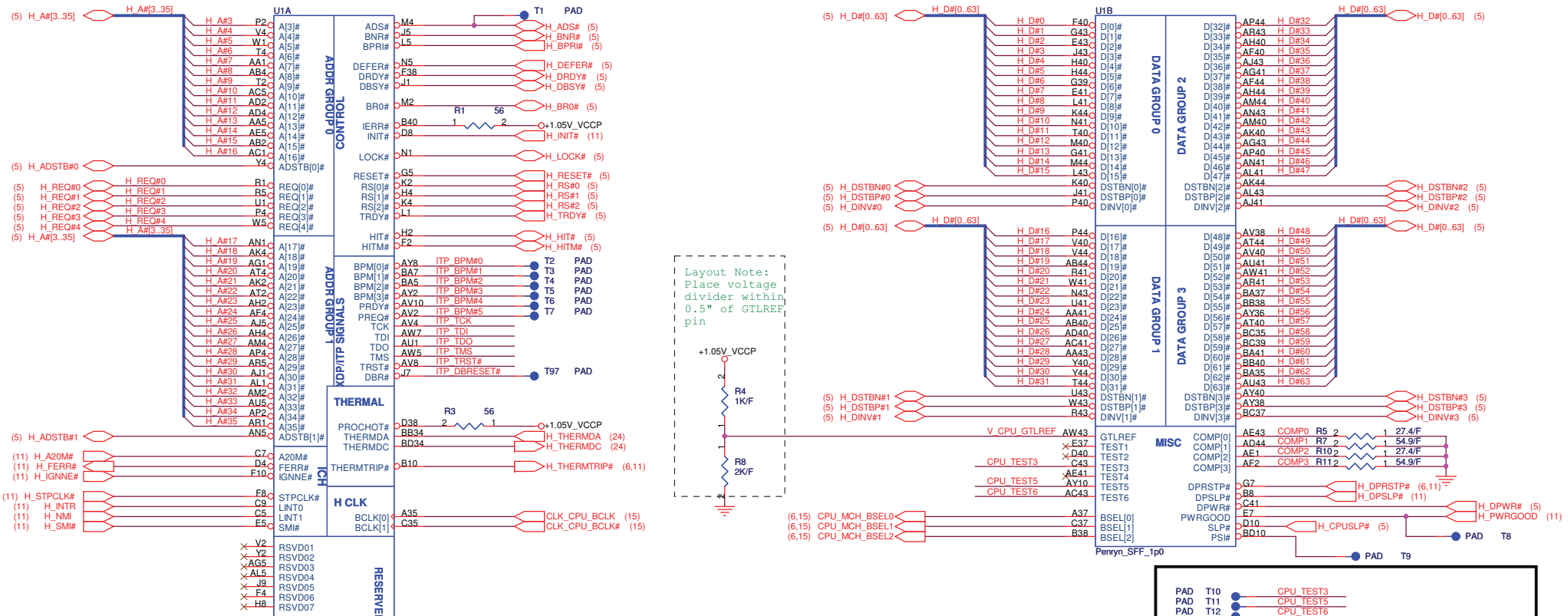


**QUANTA  
COMPUTER**

Title: Index & Power Status

Size	Document Number UM2 UMA	Rev 2A
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Date: Tuesday, May 26, 2009      Sheet 2 of 36

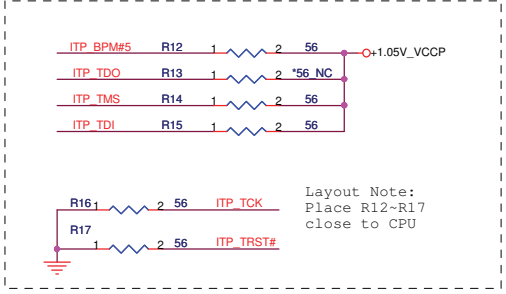


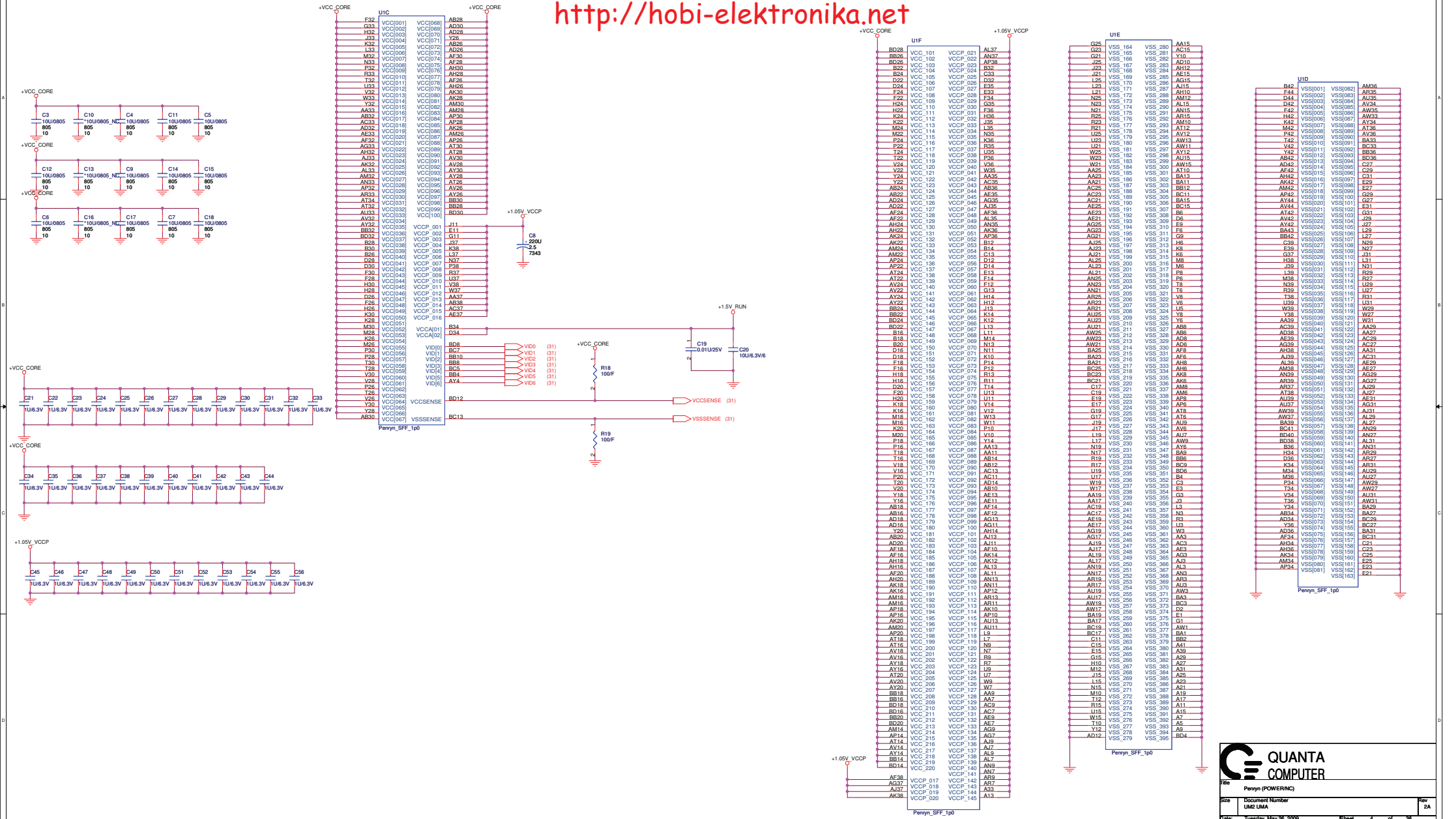
Layout Note:  
Place voltage divider within 0.5" of GTLREF pin

PAD T10 CPU TEST3  
PAD T11 CPU TEST5  
PAD T12 CPU TEST6

For the purpose of testability, route these signals through a ground referenced Z0 = 50ohm trace which ends in a via that is near a GND via and is accessible through an oscilloscope connection.

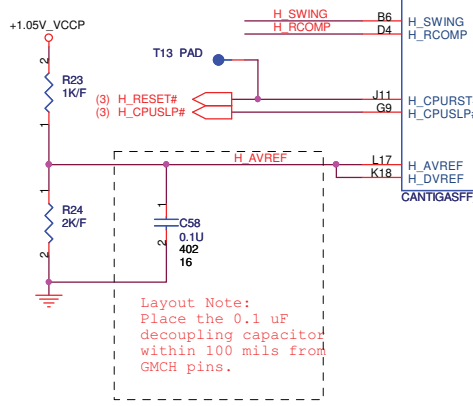
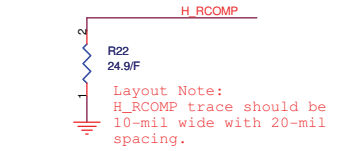
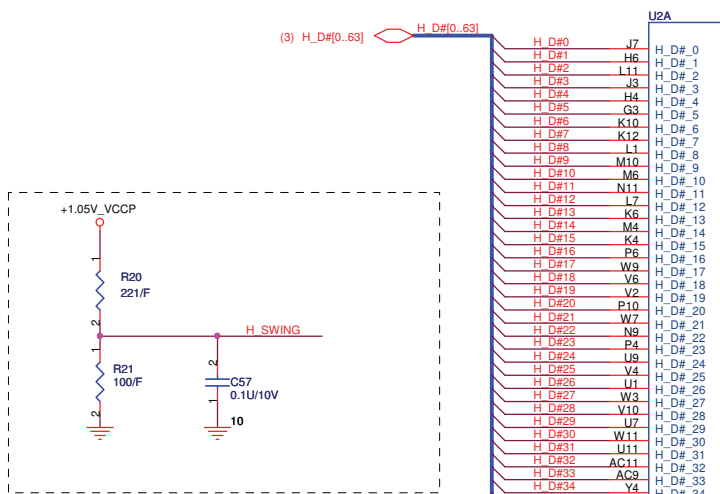
- AJSLB5VVT01  
CPU (956P)SU9400 1.4G SLB5V(BGA)WIN B/S
- AJSLGFMTT03  
CPU (956P)SU3500 1.4G SLGFM(BGA)WIN BSQ
- AJSLGS8VT03  
CPU (956P)SU2700 1.3G SLGS8(BGA)WIN BSQ





**QUANTA COMPUTER**

File: Permy (POWER)NC  
 Size: Document Number: LHM LMA  
 Date: Tuesday, May 26, 2009 Sheet: 4 of 36



U2A

H_D#0	J7	H_D#_0
H_D#1	H6	H_D#_1
H_D#2	L11	H_D#_2
H_D#3	J3	H_D#_3
H_D#4	H4	H_D#_4
H_D#5	G3	H_D#_5
H_D#6	K10	H_D#_6
H_D#7	K12	H_D#_7
H_D#8	L1	H_D#_8
H_D#9	M10	H_D#_9
H_D#10	M6	H_D#_10
H_D#11	N11	H_D#_11
H_D#12	L7	H_D#_12
H_D#13	K6	H_D#_13
H_D#14	M4	H_D#_14
H_D#15	K4	H_D#_15
H_D#16	P6	H_D#_16
H_D#17	W9	H_D#_17
H_D#18	V6	H_D#_18
H_D#19	V2	H_D#_19
H_D#20	P10	H_D#_20
H_D#21	W7	H_D#_21
H_D#22	N9	H_D#_22
H_D#23	P4	H_D#_23
H_D#24	U9	H_D#_24
H_D#25	V4	H_D#_25
H_D#26	U1	H_D#_26
H_D#27	W3	H_D#_27
H_D#28	V10	H_D#_28
H_D#29	U7	H_D#_29
H_D#30	W11	H_D#_30
H_D#31	U11	H_D#_31
H_D#32	AC11	H_D#_32
H_D#33	AC9	H_D#_33
H_D#34	Y4	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	AB6	H_D#_36
H_D#37	AA9	H_D#_37
H_D#38	AB10	H_D#_38
H_D#39	AA1	H_D#_39
H_D#40	AC3	H_D#_40
H_D#41	AC7	H_D#_41
H_D#42	AD12	H_D#_42
H_D#43	AB4	H_D#_43
H_D#44	Y6	H_D#_44
H_D#45	AD10	H_D#_45
H_D#46	AA11	H_D#_46
H_D#47	AB2	H_D#_47
H_D#48	AD4	H_D#_48
H_D#49	AE7	H_D#_49
H_D#50	AD2	H_D#_50
H_D#51	AD6	H_D#_51
H_D#52	AE3	H_D#_52
H_D#53	AG9	H_D#_53
H_D#54	AG7	H_D#_54
H_D#55	AE11	H_D#_55
H_D#56	AK6	H_D#_56
H_D#57	AF6	H_D#_57
H_D#58	AJ9	H_D#_58
H_D#59	AH6	H_D#_59
H_D#60	AF12	H_D#_60
H_D#61	AH4	H_D#_61
H_D#62	AJ7	H_D#_62
H_D#63	AE9	H_D#_63

HOST

H_A#_3	L15	H_A#3
H_A#_4	B14	H_A#4
H_A#_5	C15	H_A#5
H_A#_6	D12	H_A#6
H_A#_7	F14	H_A#7
H_A#_8	G17	H_A#8
H_A#_9	B12	H_A#9
H_A#_10	J15	H_A#10
H_A#_11	D16	H_A#11
H_A#_12	C17	H_A#12
H_A#_13	D14	H_A#13
H_A#_14	K16	H_A#14
H_A#_15	F16	H_A#15
H_A#_16	B16	H_A#16
H_A#_17	C21	H_A#17
H_A#_18	D18	H_A#18
H_A#_19	J19	H_A#19
H_A#_20	J21	H_A#20
H_A#_21	B18	H_A#21
H_A#_22	D22	H_A#22
H_A#_23	G19	H_A#23
H_A#_24	J17	H_A#24
H_A#_25	L21	H_A#25
H_A#_26	L19	H_A#26
H_A#_27	G21	H_A#27
H_A#_28	D20	H_A#28
H_A#_29	K22	H_A#29
H_A#_30	F18	H_A#30
H_A#_31	K20	H_A#31
H_A#_32	F20	H_A#32
H_A#_33	F22	H_A#33
H_A#_34	B20	H_A#34
H_A#_35	A19	H_A#35

H_ADS#	F10	H_ADS# (3)
H_ADSTB#_0	A15	H_ADSTB#0 (3)
H_ADSTB#_1	C19	H_ADSTB#1 (3)
H_BNR#	C9	H_BNR# (3)
H_BPRI#	B8	H_BPRI# (3)
H_BREQ#	C11	H_BREQ# (3)
H_DEFER#	E5	H_DEFER# (3)
H_DBSY#	D6	H_DBSY# (3)
HPLL_CLK	AH10	CLK_MCH_BCLK (15)
HPLL_CLK#	AJ11	CLK_MCH_BCLK# (15)
H_DPWR#	G11	H_DPWR# (3)
H_DRDY#	H2	H_DRDY# (3)
H_HIT#	C7	H_HIT# (3)
H_HITM#	F8	H_HITM# (3)
H_LOCK#	A11	H_LOCK# (3)
H_TRDY#	D8	H_TRDY# (3)

H_DINV#_0	L9	H_DINV#0 (3)
H_DINV#_1	N7	H_DINV#1 (3)
H_DINV#_2	AA7	H_DINV#2 (3)
H_DINV#_3	AG3	H_DINV#3 (3)

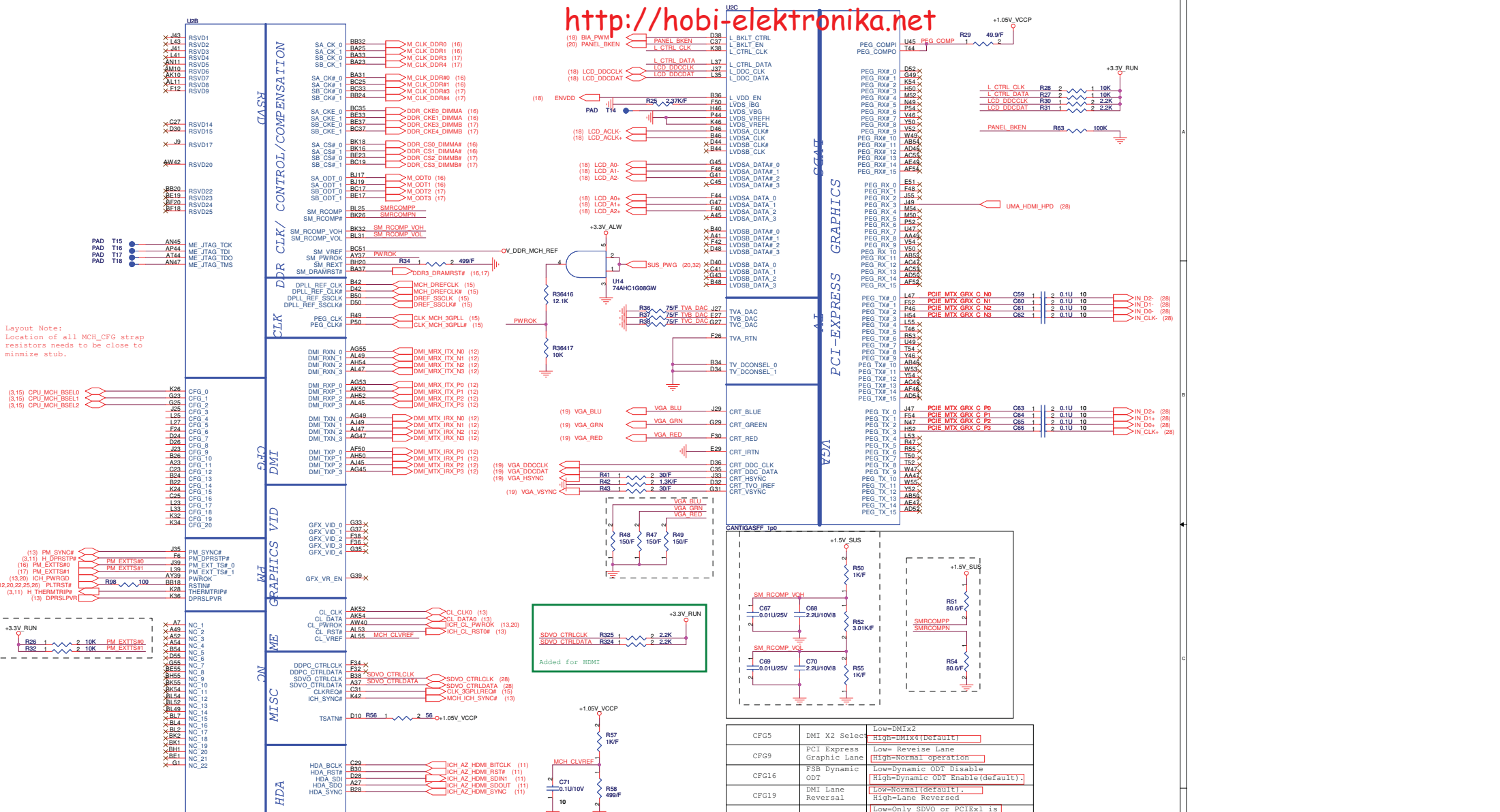
H_DSTBN#_0	K2	H_DSTBN#0 (3)
H_DSTBN#_1	N3	H_DSTBN#1 (3)
H_DSTBN#_2	AA3	H_DSTBN#2 (3)
H_DSTBN#_3	AF4	H_DSTBN#3 (3)

H_DSTBP#_0	L3	H_DSTBP#0 (3)
H_DSTBP#_1	M2	H_DSTBP#1 (3)
H_DSTBP#_2	Y2	H_DSTBP#2 (3)
H_DSTBP#_3	AF2	H_DSTBP#3 (3)

H_REQ#_0	J13	H_REQ#0 (3)
H_REQ#_1	L13	H_REQ#1 (3)
H_REQ#_2	C13	H_REQ#2 (3)
H_REQ#_3	G13	H_REQ#3 (3)
H_REQ#_4	G15	H_REQ#4 (3)

H_RS#_0	F4	H_RS#0 (3)
H_RS#_1	F2	H_RS#1 (3)
H_RS#_2	G7	H_RS#2 (3)





Layout Note:  
Location of all MCH\_CFG strap resistors needs to be close to minimize stub.

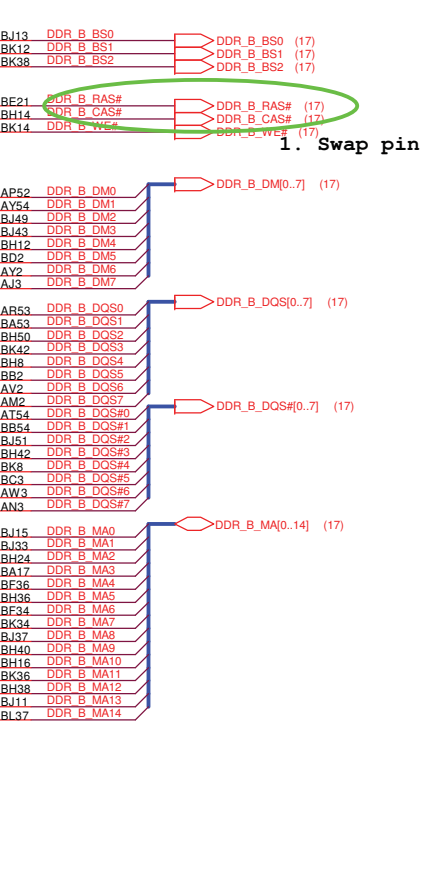
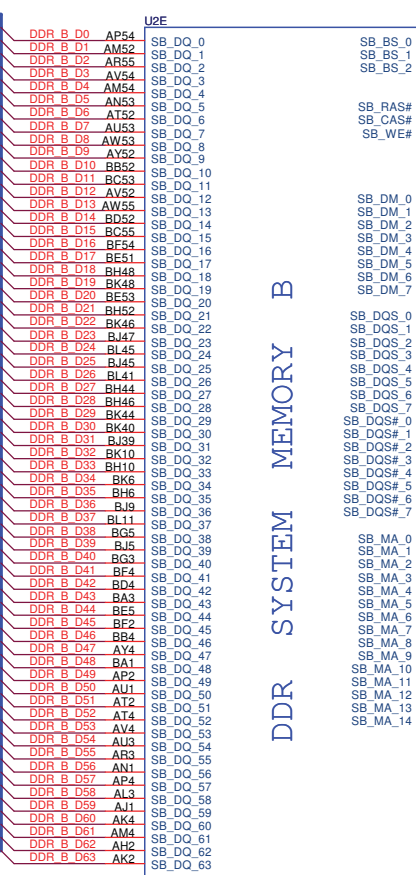
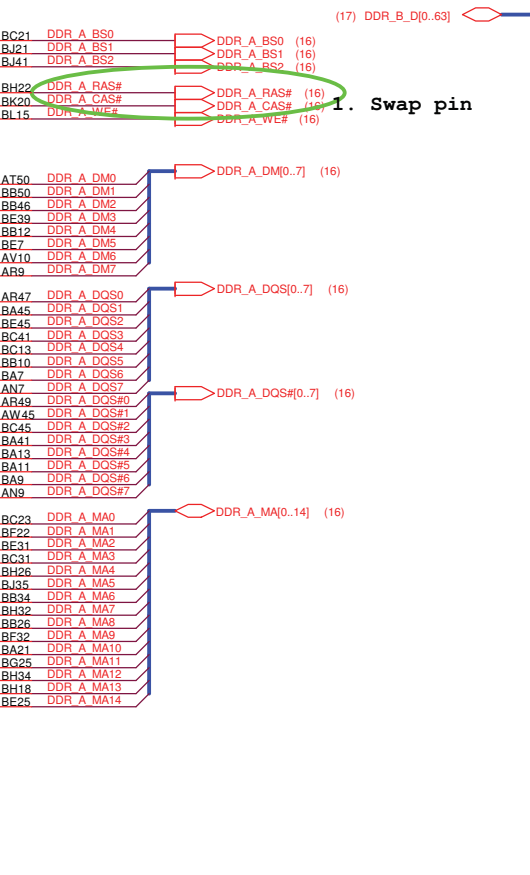
CFG5	DMI X2 Select	Low=DMiX2 High=DMiX4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal(Default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

SDVO/HDMI/DP Configuration		
	SDVO_CTRLDATA	DDPC_CTRLDATA
PEG	0	0
PEG Enabled	1	1
SDVO/HDMI/DP Enabled	1	1

DDPC\_CTRL\_DATA & SDVO\_CTRL\_DATA straps should both be high to enable DisplayPort.





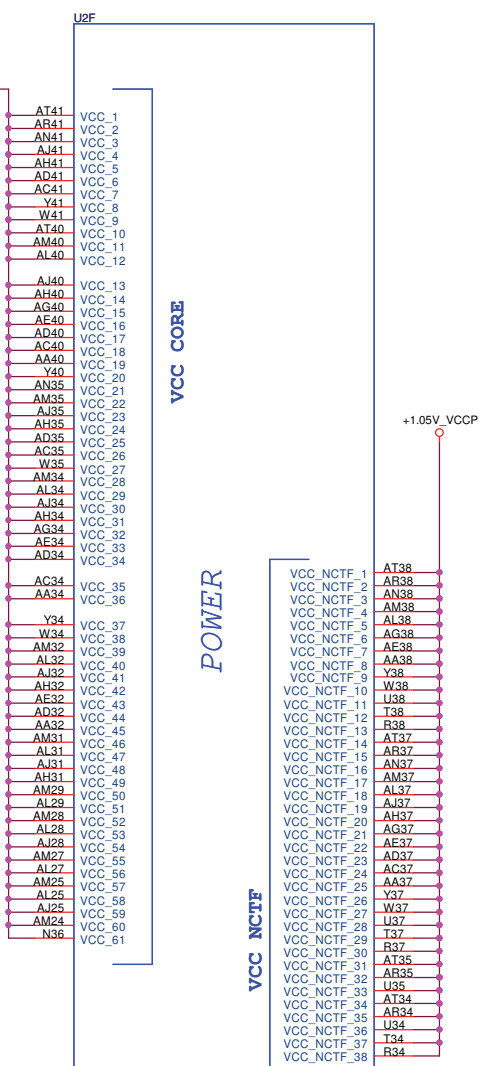
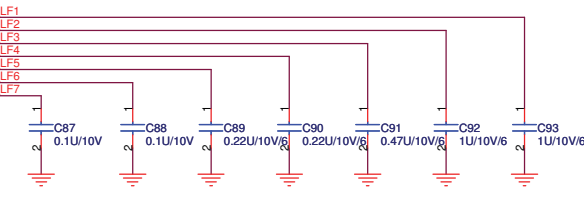
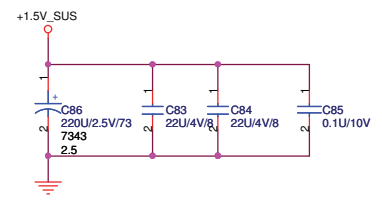
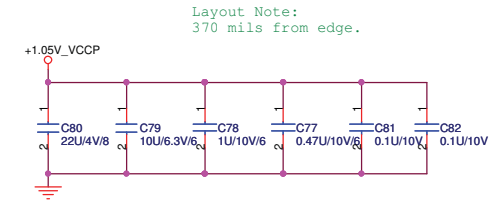
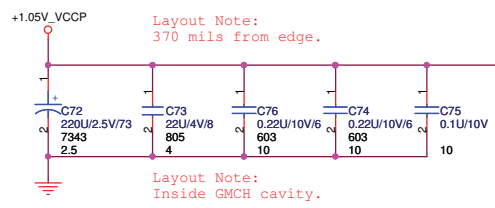
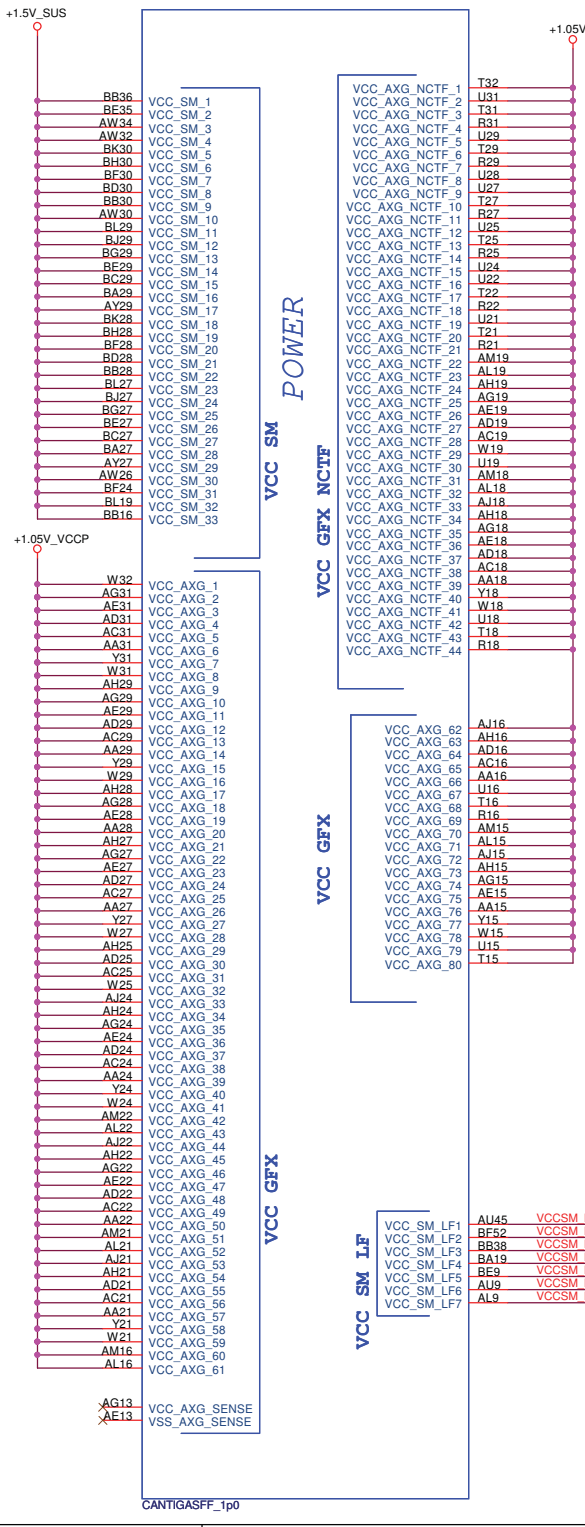


**QUANTA COMPUTER**

Title: Cantiga\_C (DDR3)

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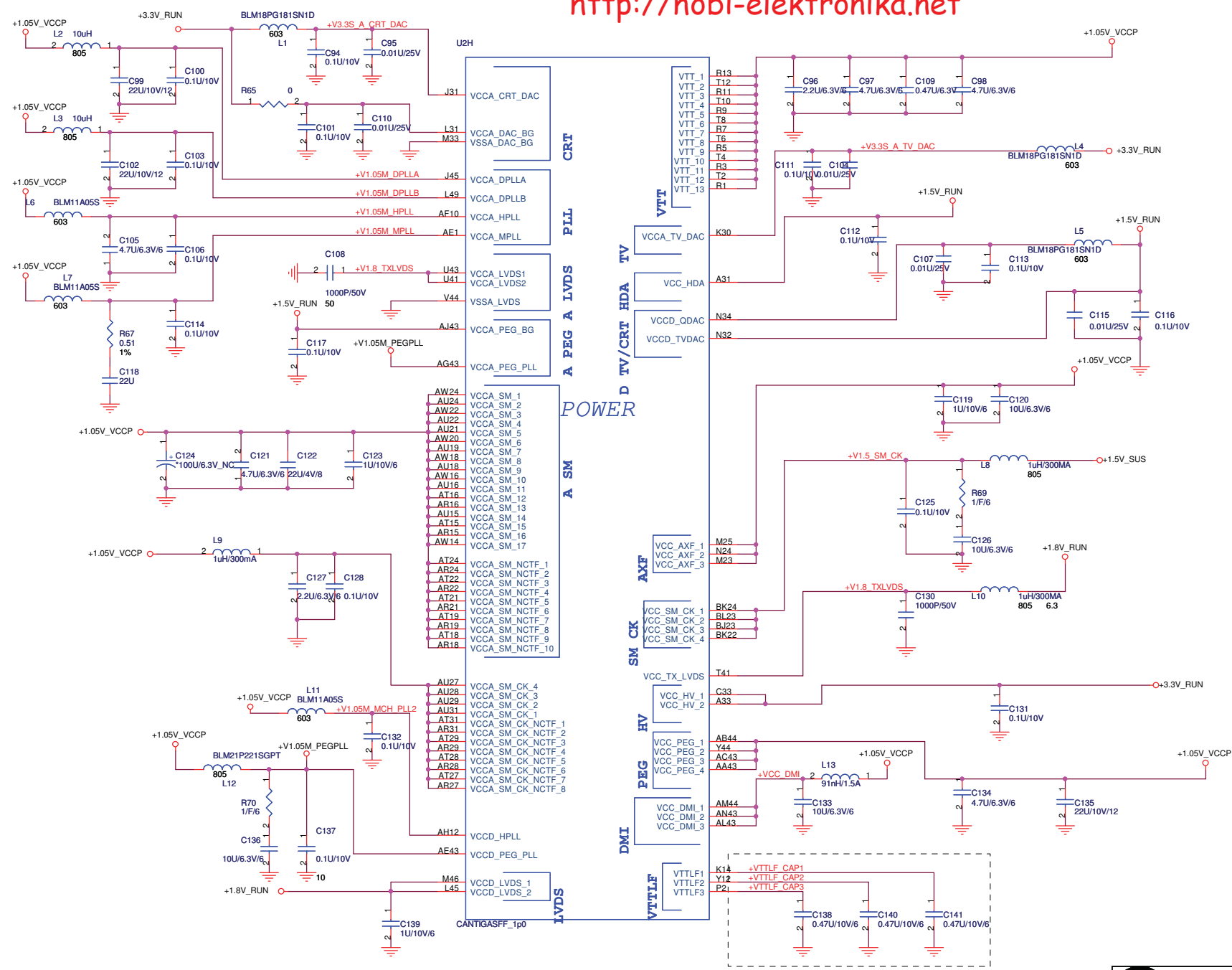
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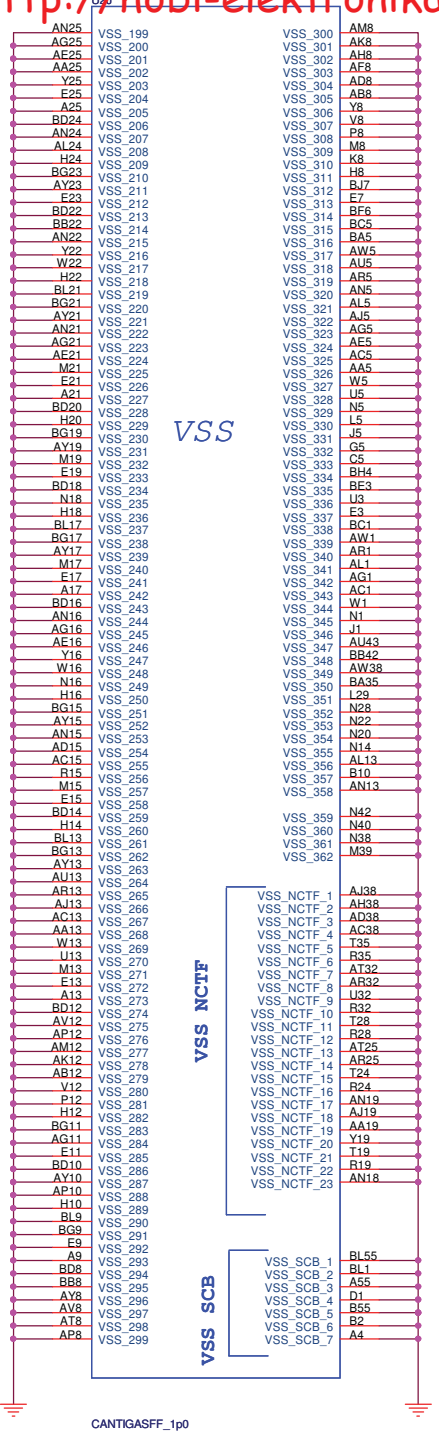
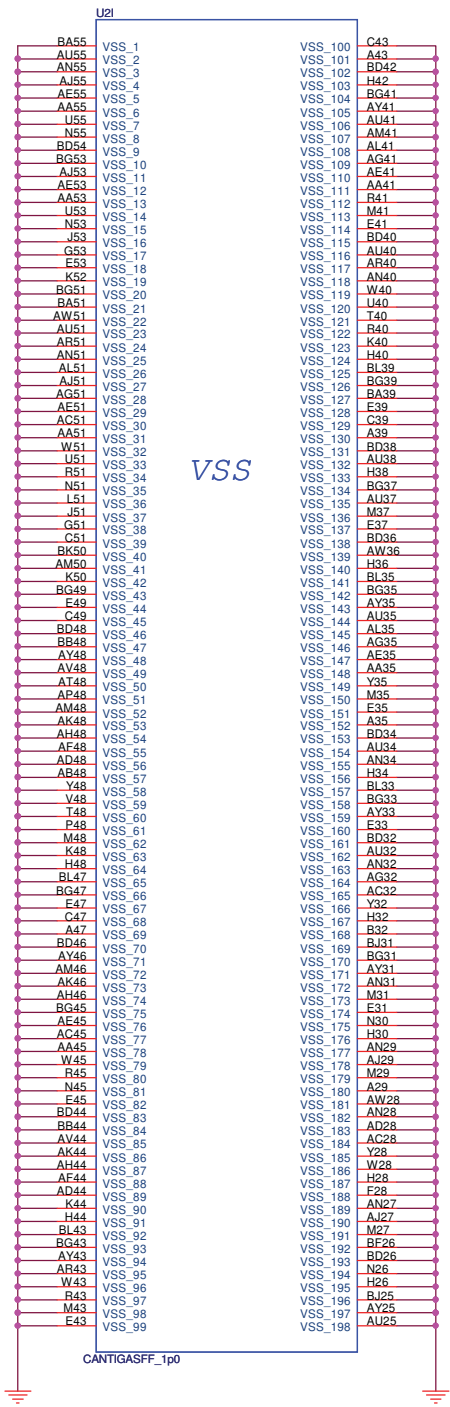
Title: Cantiga\_D (VCC,NCTF)

Size: Document Number UM2 UMA Rev 2A

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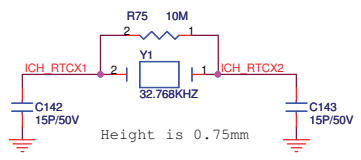
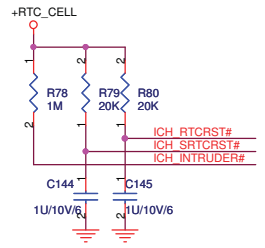


**QUANTA  
COMPUTER**

Title: Cantiga\_F (VSS)

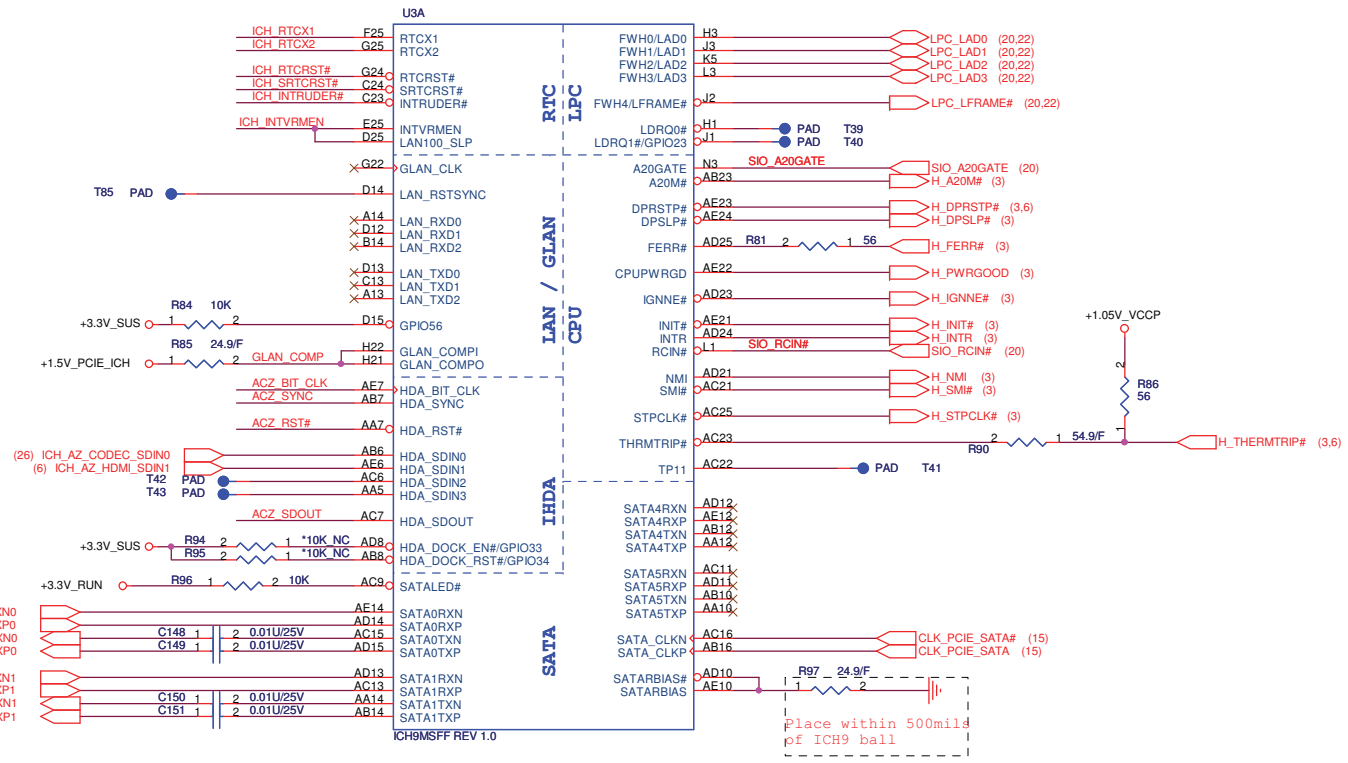
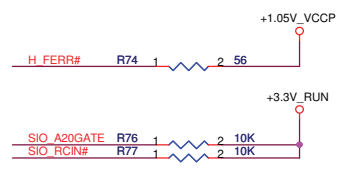
Size: Document Number UM2 UMA Rev 2A

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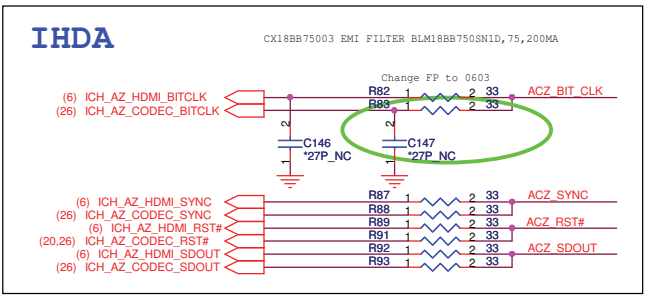


(Internal VRM enabled for VccSus1\_05, VccSus1\_5, VccCL1\_5, VccLAN1\_05 and VccCL1\_05)

ICH_INTVRMEN	Low = Internal VR Disabled
ICH_INTVRMEN	High = Internal VR Enabled(Default)



ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)

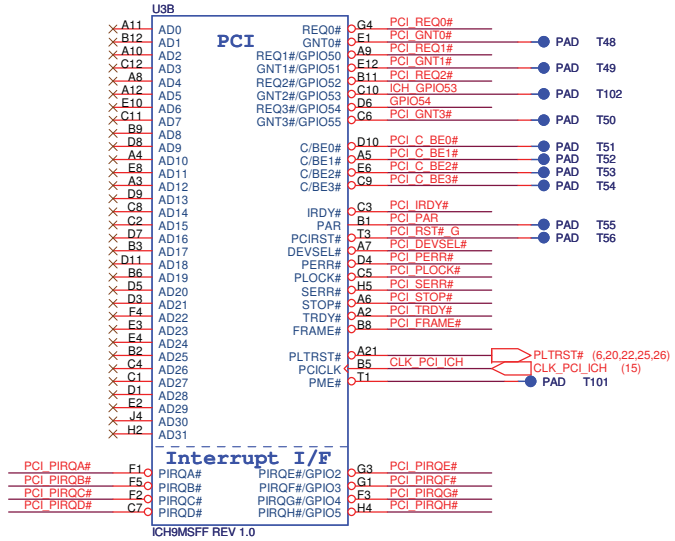
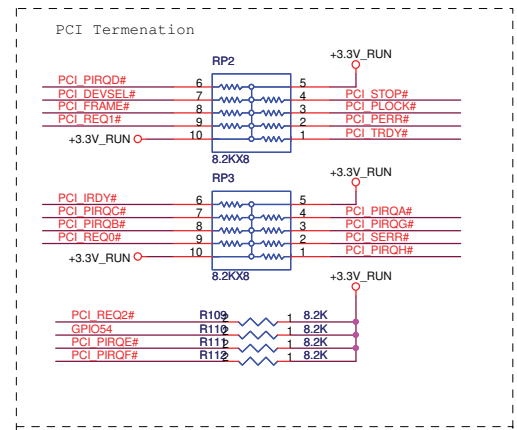
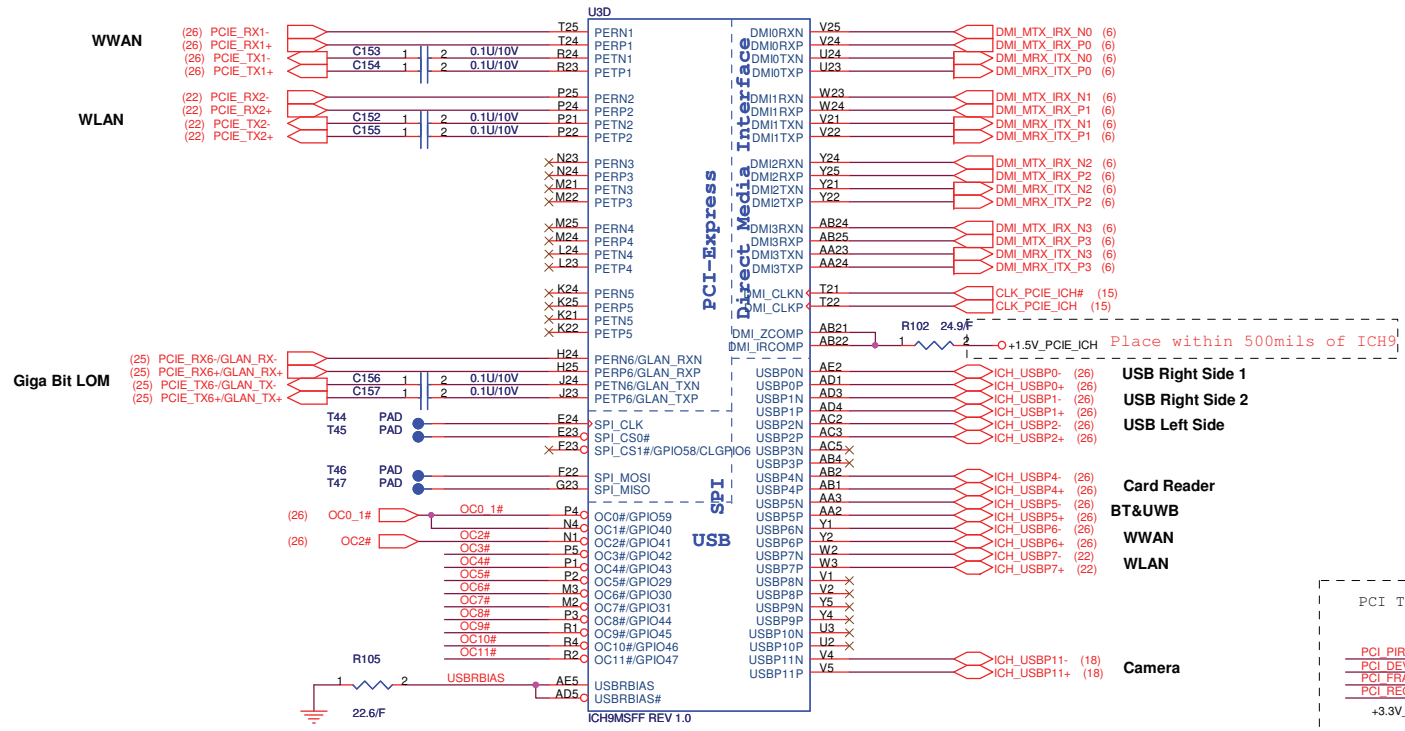


**QUANTA COMPUTER**

Title: ICH9-M (CPU,SATA,IDE)

Size: Document Number UM2\_UMA Rev 2A

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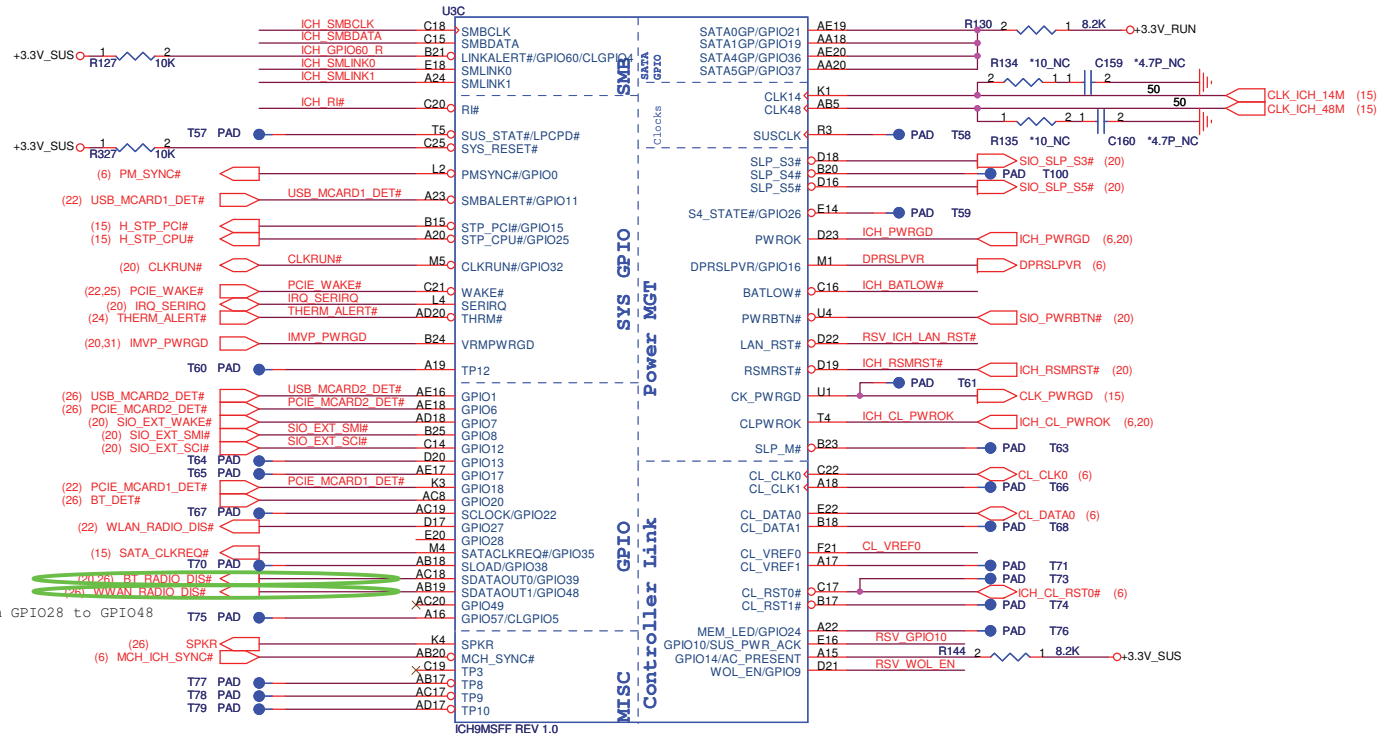
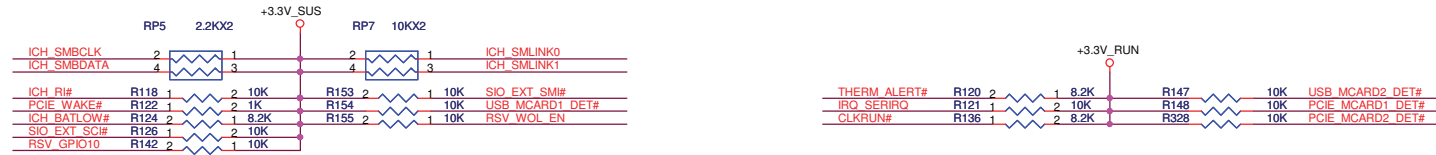
Reserved for EMI. Place resistor and cap close to ICH.

**QUANTA COMPUTER**

Title: ICH9-M(USB,PCIE,DMI)

Size: Document Number UM2 UMA Rev 2A

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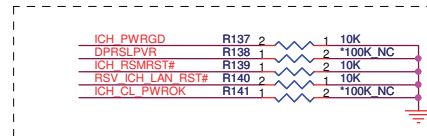
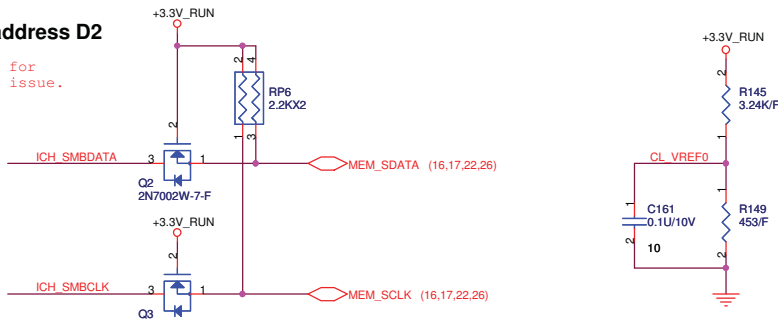


12. Change BT\_RADIO\_DIS# to SB

13. change WWAN\_RADIO\_DIS# from GPIO28 to GPIO48

**SMBus address D2**

These are for backdrive issue.

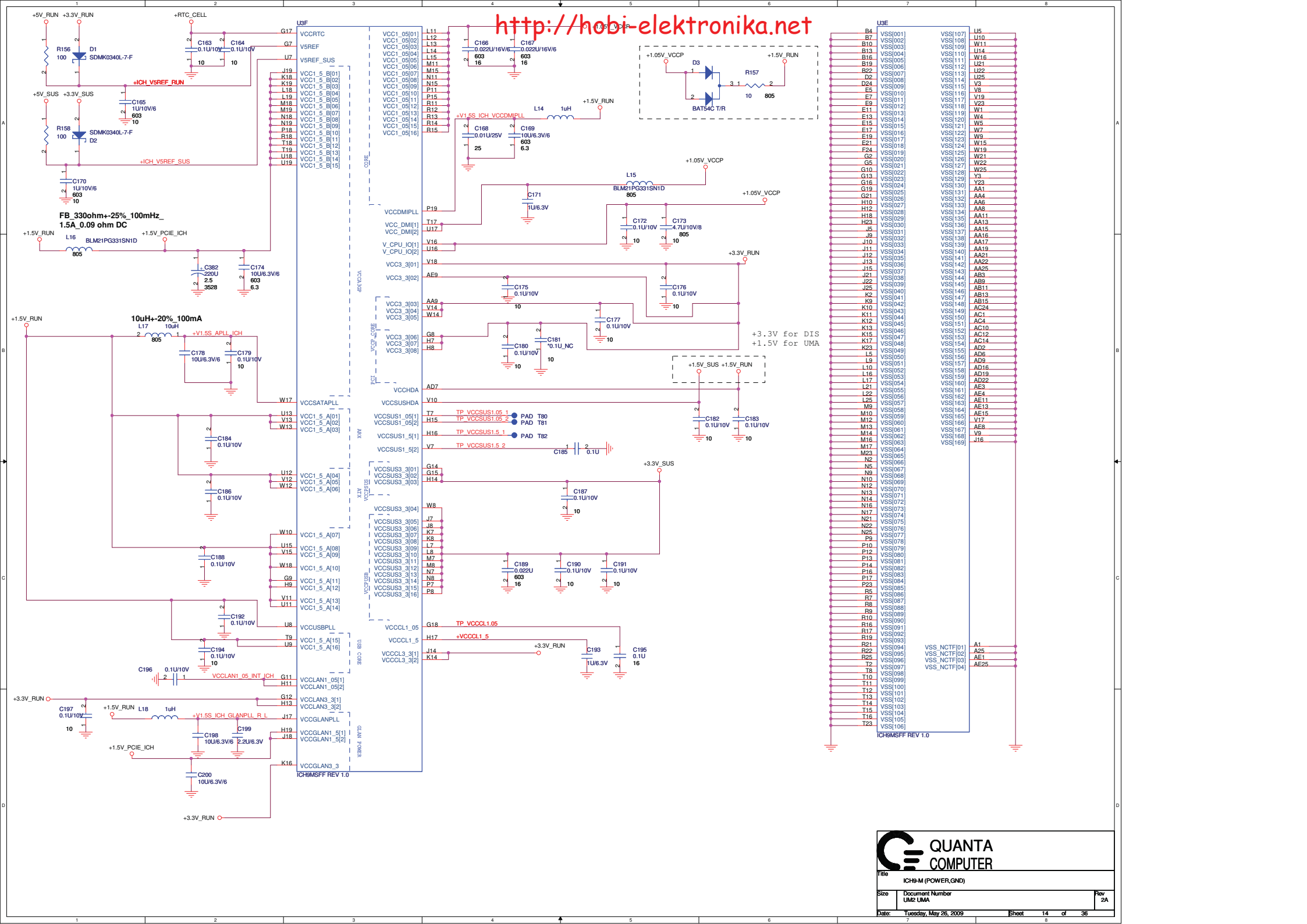


**QUANTA COMPUTER**

Title: ICH9-M (PM,GPIO,SMB)

Size: Document Number UM2 UMA Rev 2A

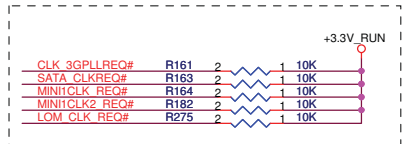
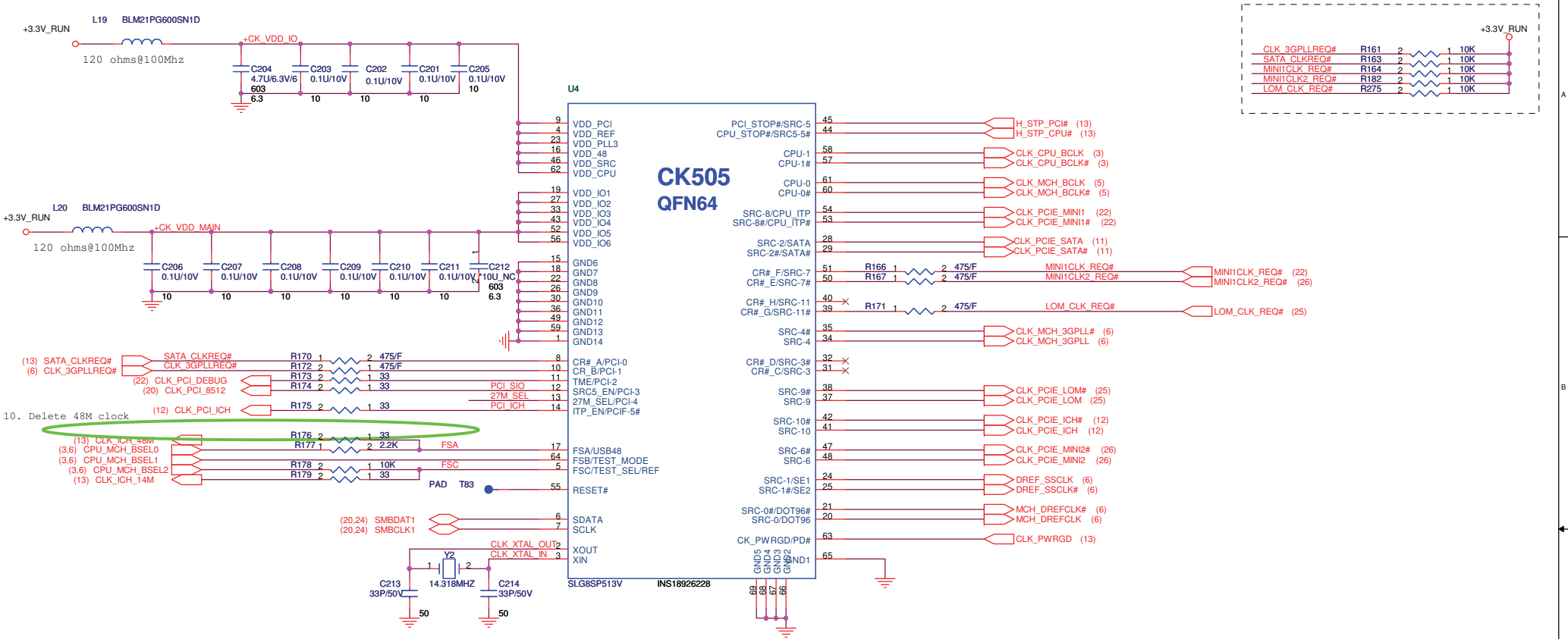
Date: Tuesday, May 26, 2009 Sheet 13 of 36



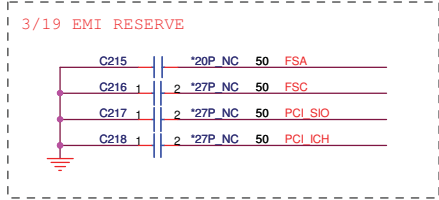
USE	VSS	U5
B4	VSS[001]	U5
B7	VSS[002]	U10
B10	VSS[003]	VSS[008]
B11	VSS[004]	W11
B13	VSS[005]	VSS[009]
B16	VSS[006]	U14
B19	VSS[007]	VSS[110]
B22	VSS[008]	W16
D2	VSS[009]	U21
D24	VSS[010]	VSS[112]
E5	VSS[011]	U22
E7	VSS[012]	VSS[113]
E9	VSS[013]	VSS[114]
E11	VSS[014]	V8
E13	VSS[015]	VSS[115]
E15	VSS[016]	VSS[116]
E17	VSS[017]	VSS[117]
E19	VSS[018]	VSS[118]
E21	VSS[019]	VSS[119]
E24	VSS[020]	VSS[120]
G5	VSS[021]	VSS[121]
G10	VSS[022]	VSS[122]
G13	VSS[023]	VSS[123]
G16	VSS[024]	VSS[124]
G19	VSS[025]	VSS[125]
G21	VSS[026]	VSS[126]
H10	VSS[027]	VSS[127]
H12	VSS[028]	VSS[128]
H18	VSS[029]	VSS[129]
J5	VSS[030]	VSS[130]
J9	VSS[031]	VSS[131]
J10	VSS[032]	VSS[132]
J11	VSS[033]	VSS[133]
J12	VSS[034]	VSS[134]
J13	VSS[035]	VSS[135]
J15	VSS[036]	VSS[136]
J25	VSS[037]	VSS[137]
J26	VSS[038]	VSS[138]
J27	VSS[039]	VSS[139]
J28	VSS[040]	VSS[140]
K9	VSS[041]	VSS[141]
K11	VSS[042]	VSS[142]
K12	VSS[043]	VSS[143]
K13	VSS[044]	VSS[144]
K15	VSS[045]	VSS[145]
K17	VSS[046]	VSS[146]
K23	VSS[047]	VSS[147]
L5	VSS[048]	VSS[148]
L9	VSS[049]	VSS[149]
L10	VSS[050]	VSS[150]
L16	VSS[051]	VSS[151]
L17	VSS[052]	VSS[152]
L21	VSS[053]	VSS[153]
L22	VSS[054]	VSS[154]
L25	VSS[055]	VSS[155]
M2	VSS[056]	VSS[156]
M10	VSS[057]	VSS[157]
M12	VSS[058]	VSS[158]
M13	VSS[059]	VSS[159]
M14	VSS[060]	VSS[160]
M16	VSS[061]	VSS[161]
M17	VSS[062]	VSS[162]
M23	VSS[063]	VSS[163]
N2	VSS[064]	VSS[164]
N5	VSS[065]	VSS[165]
N6	VSS[066]	VSS[166]
N10	VSS[067]	VSS[167]
N12	VSS[068]	VSS[168]
N13	VSS[069]	VSS[169]
N14	VSS[070]	VSS[170]
N16	VSS[071]	VSS[171]
N17	VSS[072]	VSS[172]
N21	VSS[073]	VSS[173]
N22	VSS[074]	VSS[174]
N25	VSS[075]	VSS[175]
P10	VSS[076]	VSS[176]
P9	VSS[077]	VSS[177]
P12	VSS[078]	VSS[178]
P13	VSS[079]	VSS[179]
P14	VSS[080]	VSS[180]
P16	VSS[081]	VSS[181]
P17	VSS[082]	VSS[182]
P23	VSS[083]	VSS[183]
R5	VSS[084]	VSS[184]
R6	VSS[085]	VSS[185]
R7	VSS[086]	VSS[186]
R8	VSS[087]	VSS[187]
R9	VSS[088]	VSS[188]
R10	VSS[089]	VSS[189]
R16	VSS[090]	VSS[190]
R17	VSS[091]	VSS[191]
R19	VSS[092]	VSS[192]
R21	VSS[093]	VSS[193]
R22	VSS[094]	VSS[194]
R25	VSS[095]	VSS[195]
T2	VSS[096]	VSS[196]
T8	VSS[097]	VSS[197]
T10	VSS[098]	VSS[198]
T11	VSS[099]	VSS[199]
T12	VSS[100]	VSS[200]
T13	VSS[101]	VSS[201]
T14	VSS[102]	VSS[202]
T15	VSS[103]	VSS[203]
T16	VSS[104]	VSS[204]
T23	VSS[105]	VSS[205]
T25	VSS[106]	VSS[206]
VSS_NCTFF[01]	A1	
VSS_NCTFF[02]	A25	
VSS_NCTFF[03]	AE1	
VSS_NCTFF[04]	AE25	







10. Delete 48M clock

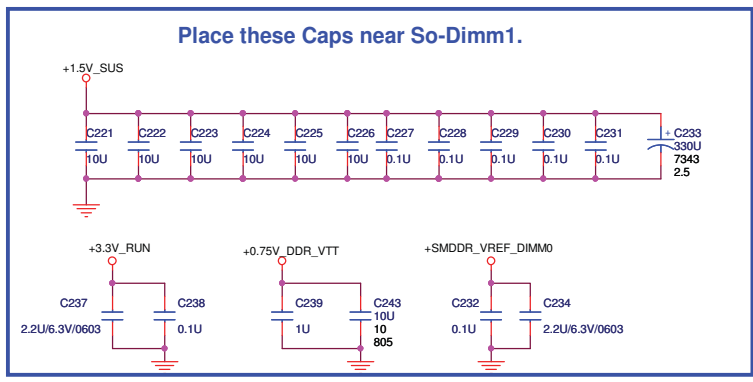
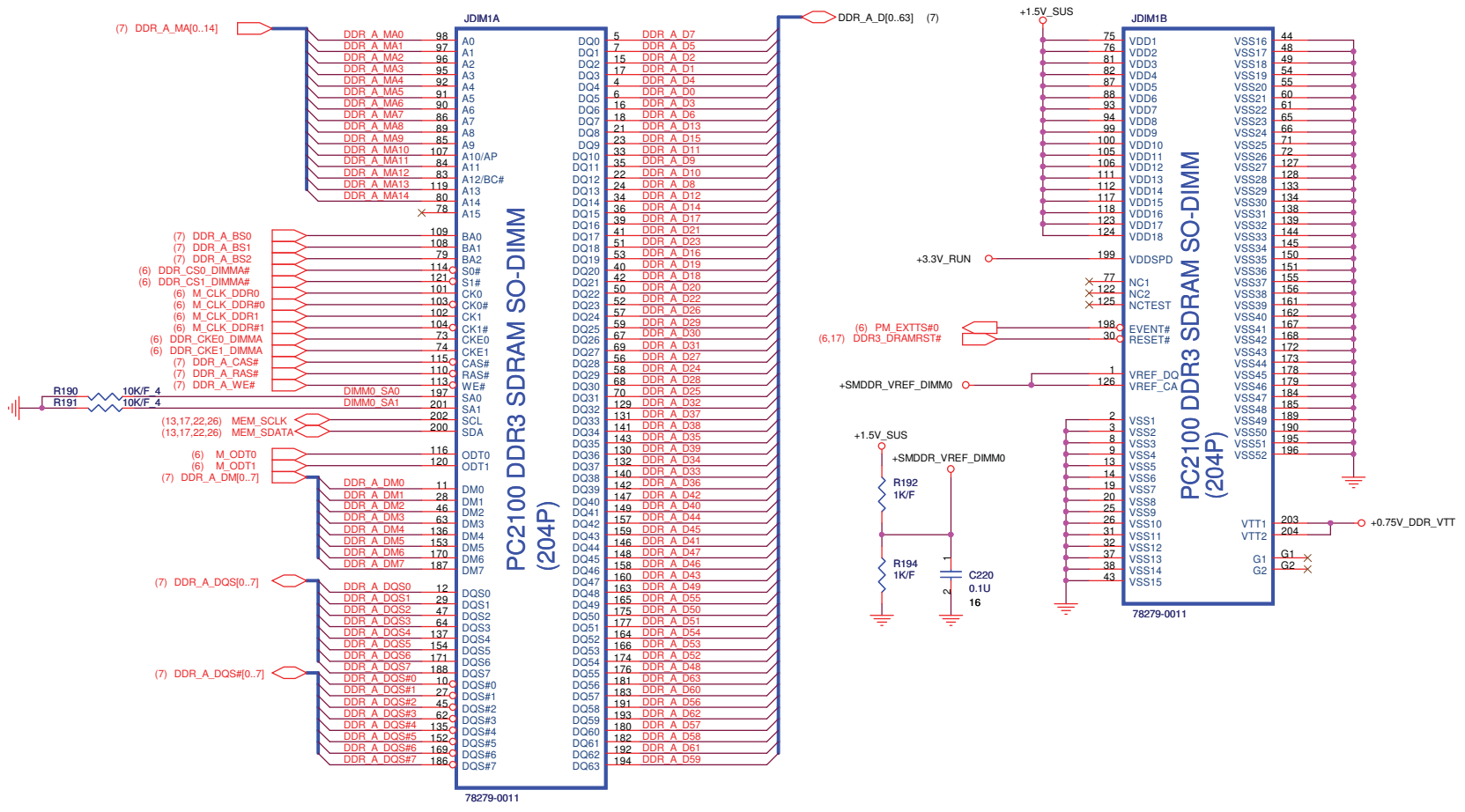


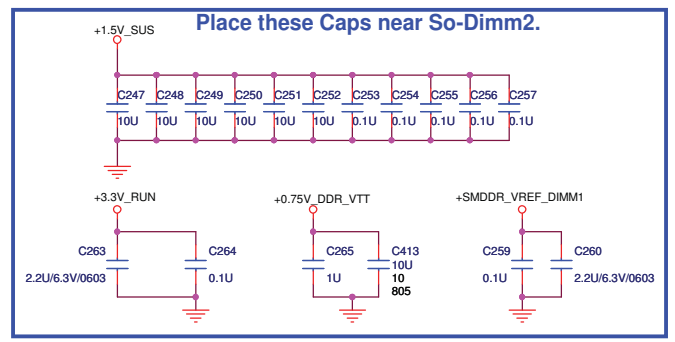
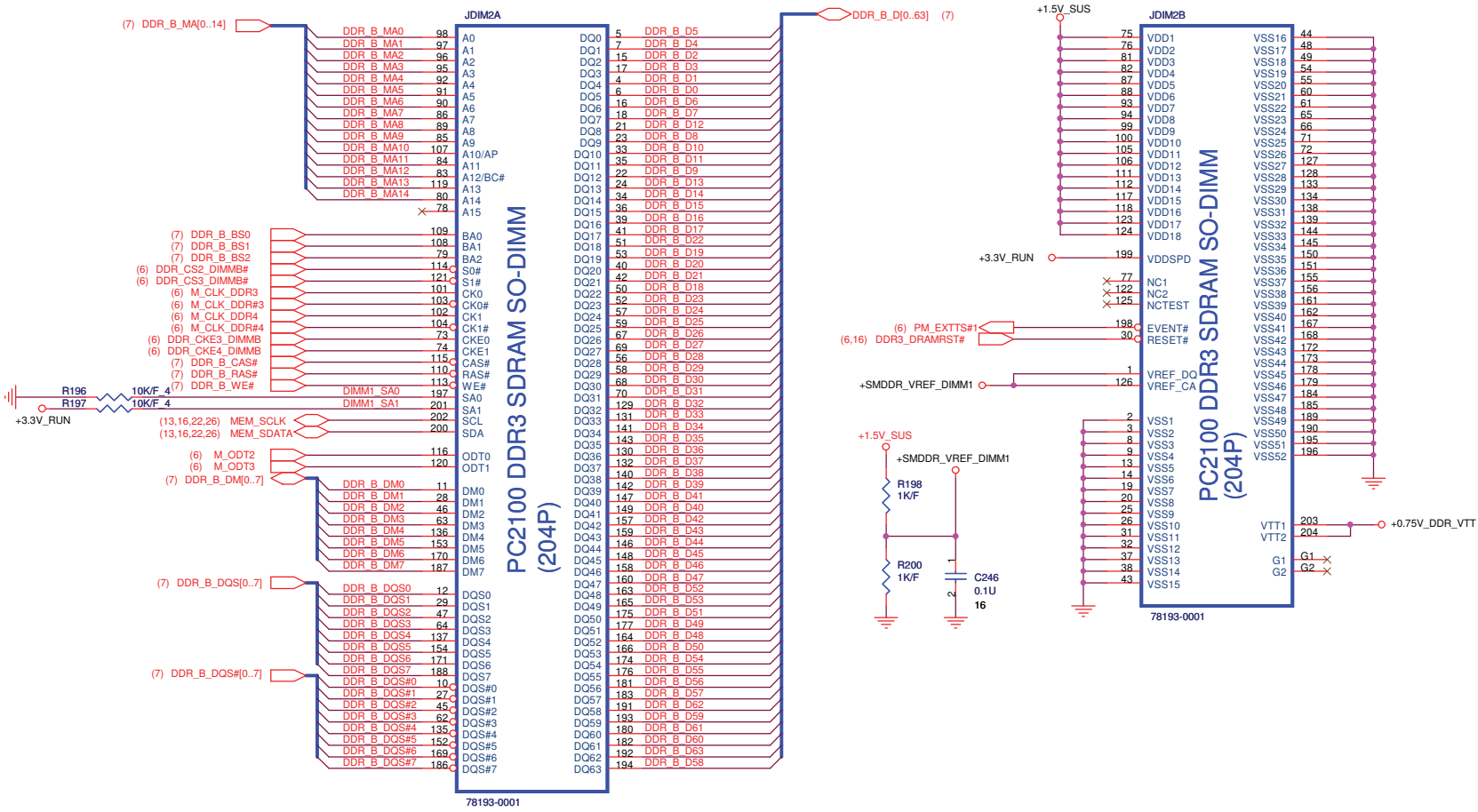
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	FSD	100	33

27M\_SEL

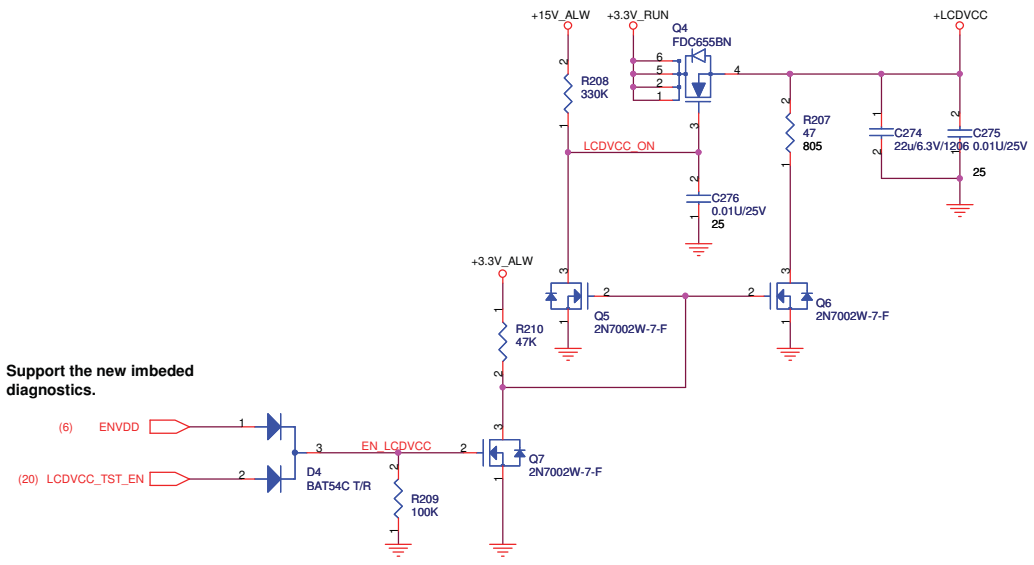
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	100M_T	100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



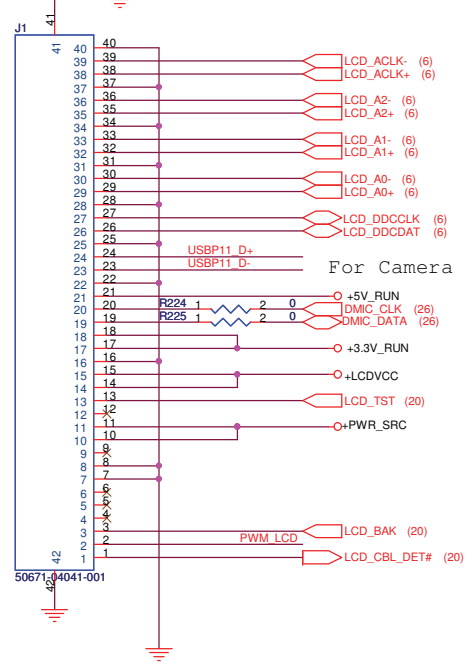




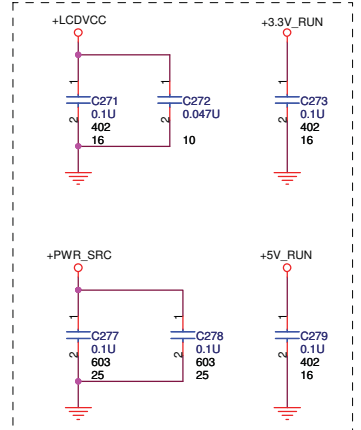
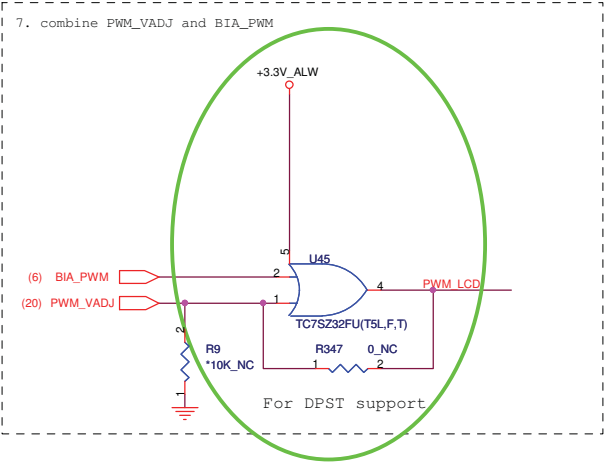
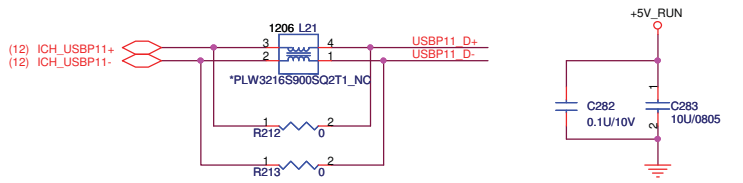
LCD



Support the new imbedded diagnostics.



CCD

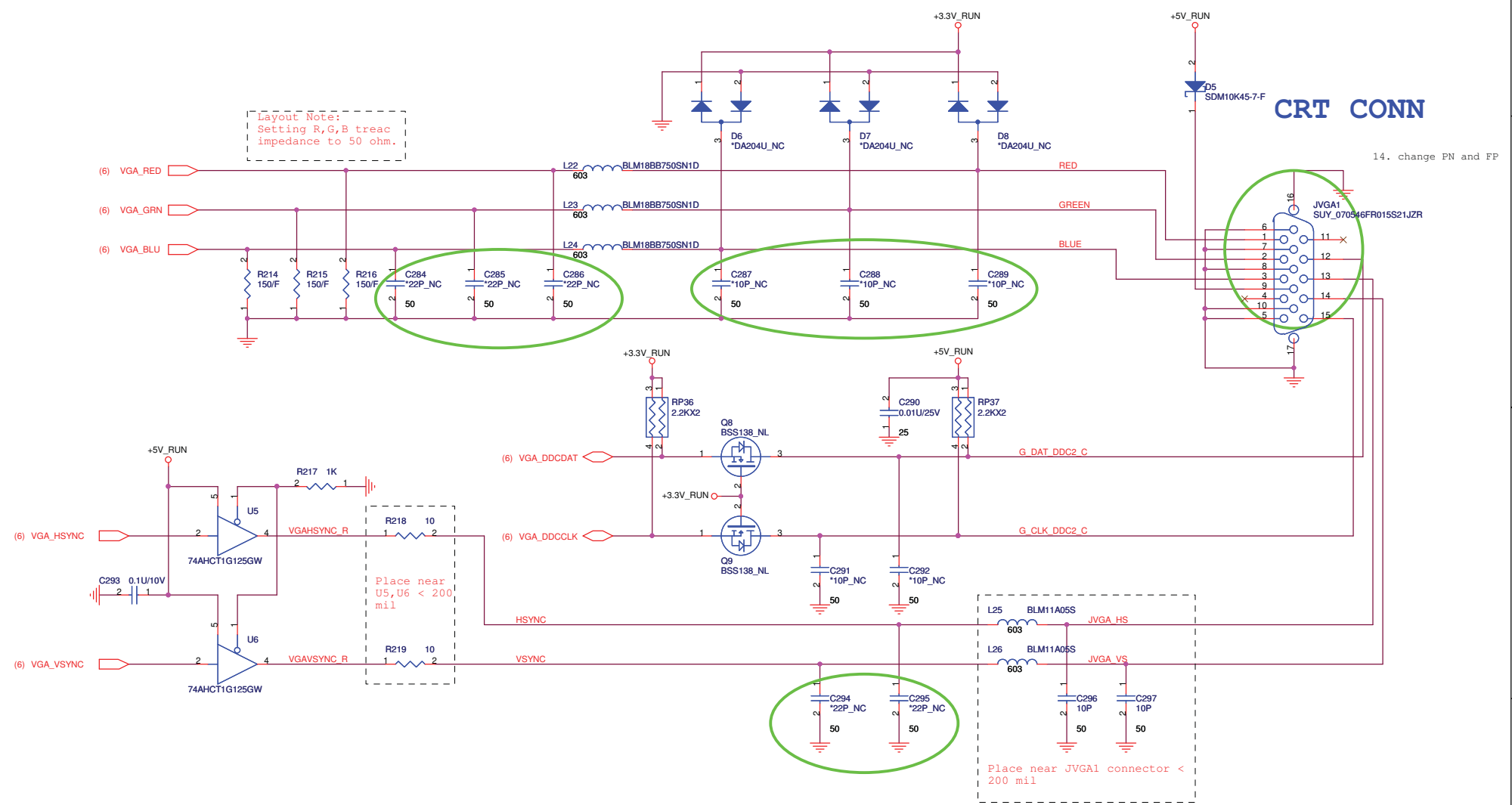


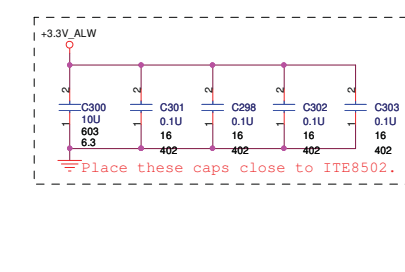
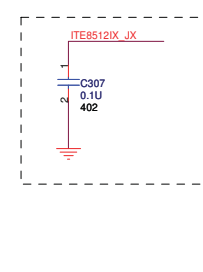
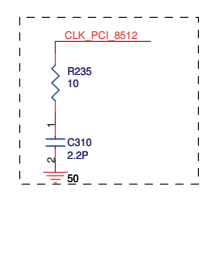
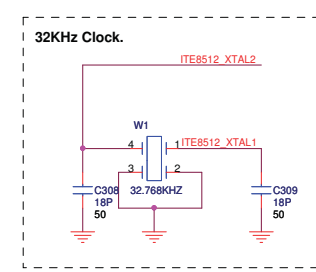
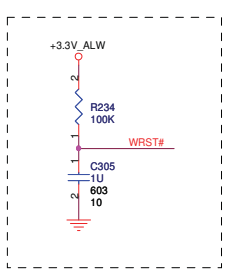
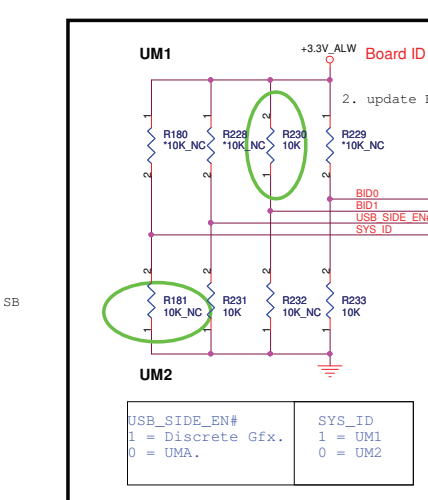
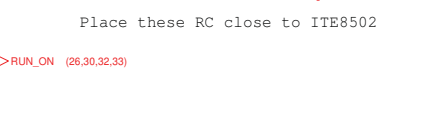
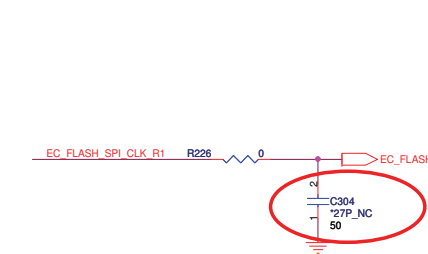
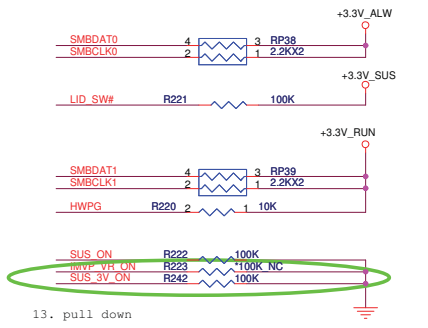
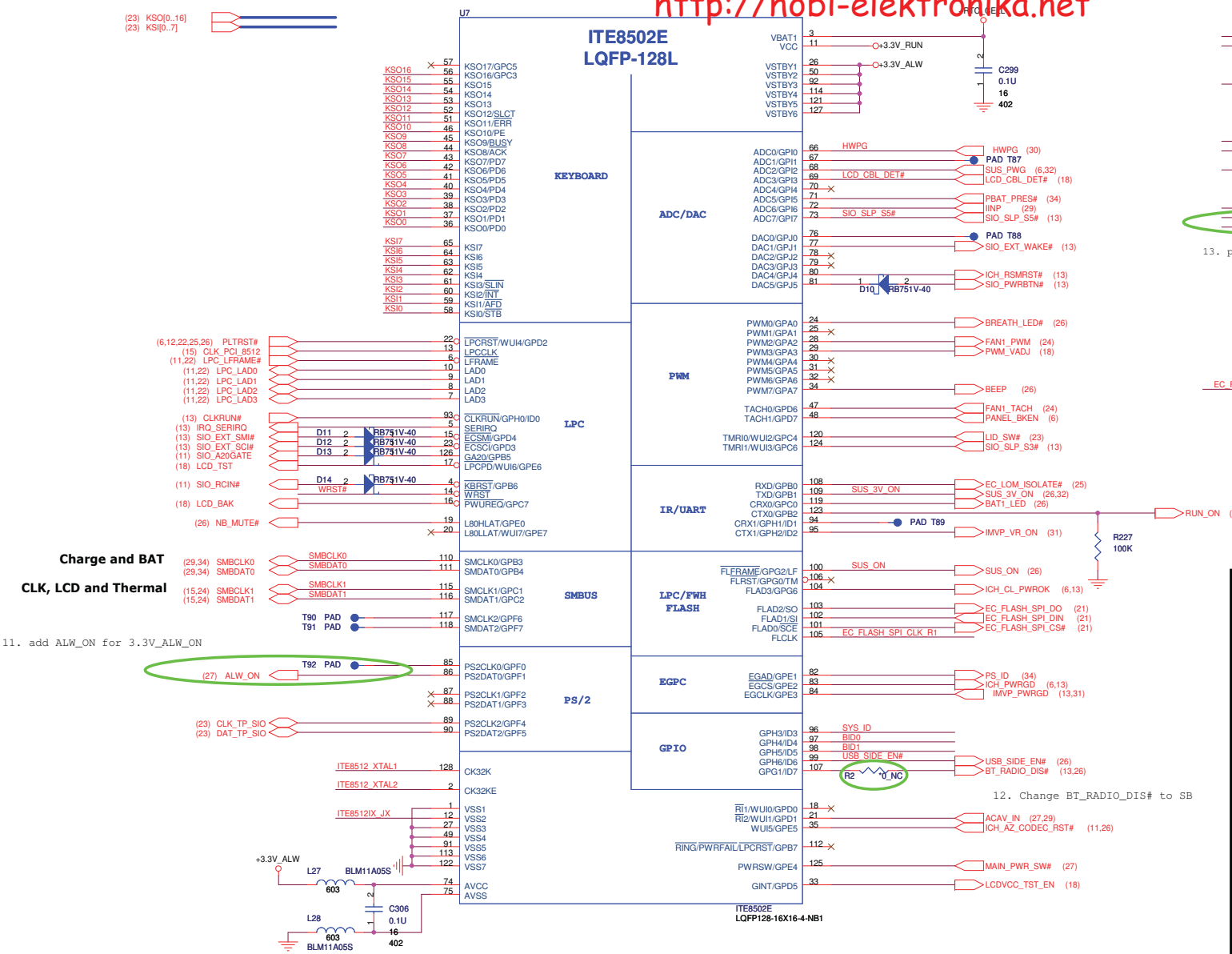
**QUANTA COMPUTER**

Title: LCD CONN & CCD

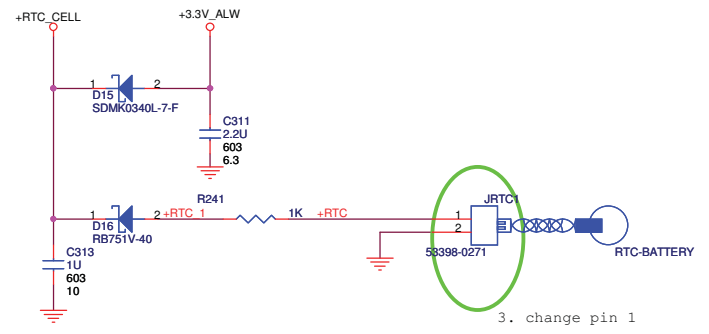
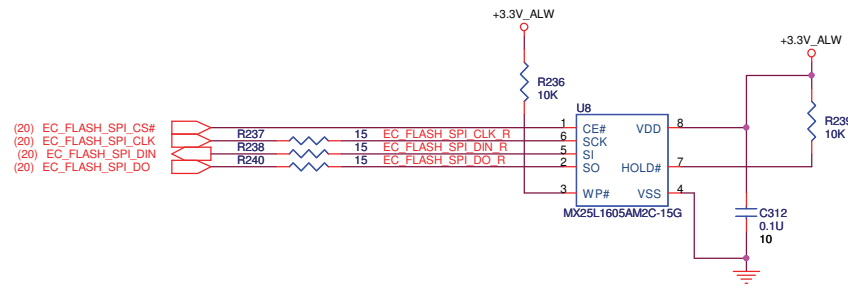
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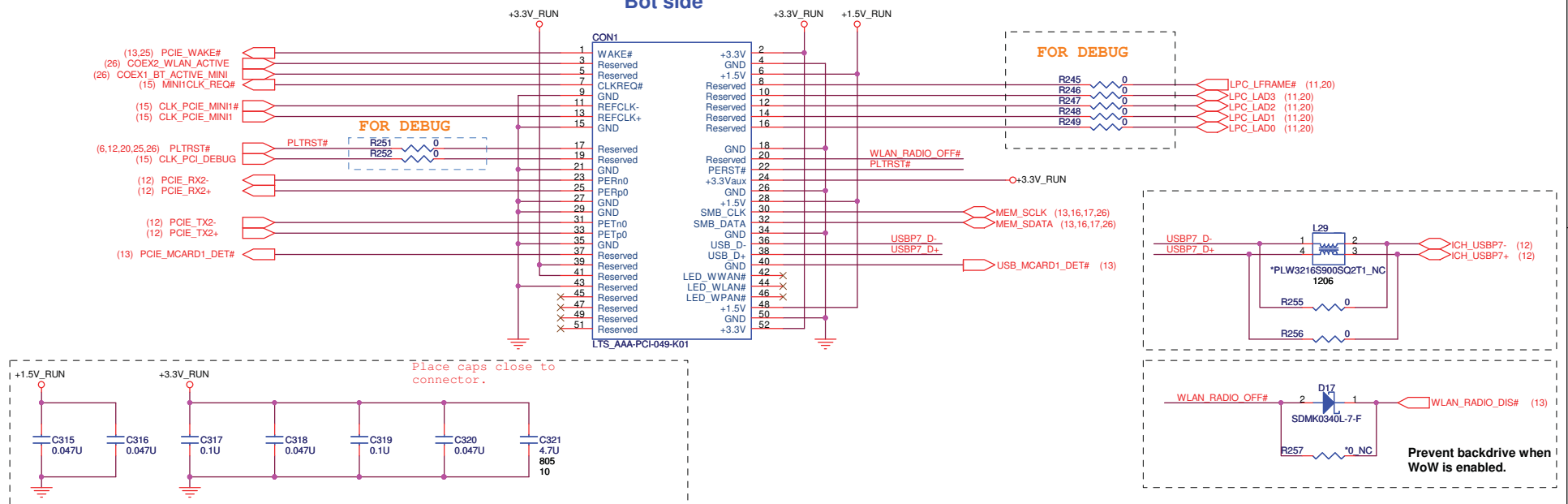


**QUANTA COMPUTER**

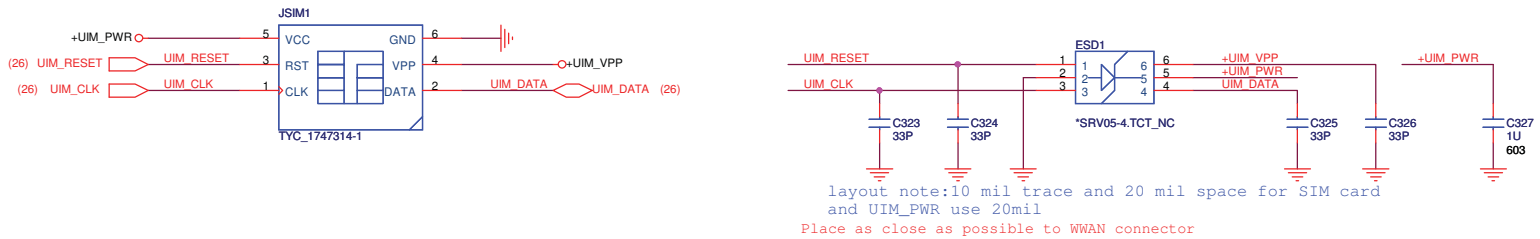
Title: Flash / RTC

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Bot side

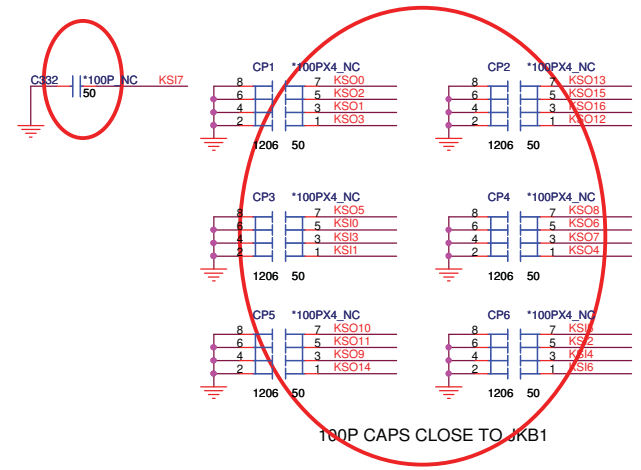
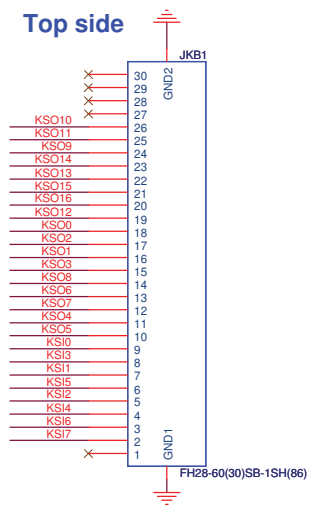


SIM CONN

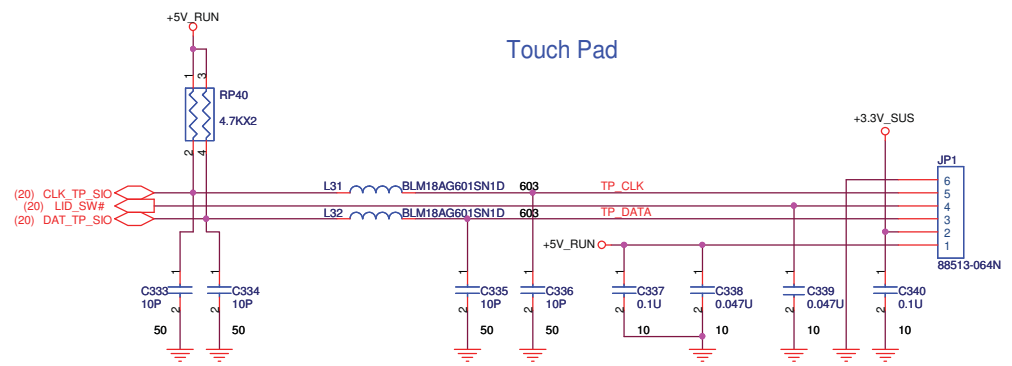


**KEYBOARD CONN**

(20) KSO[0..16]  
(20) KSI[0..7]



**Touch Pad CONN**



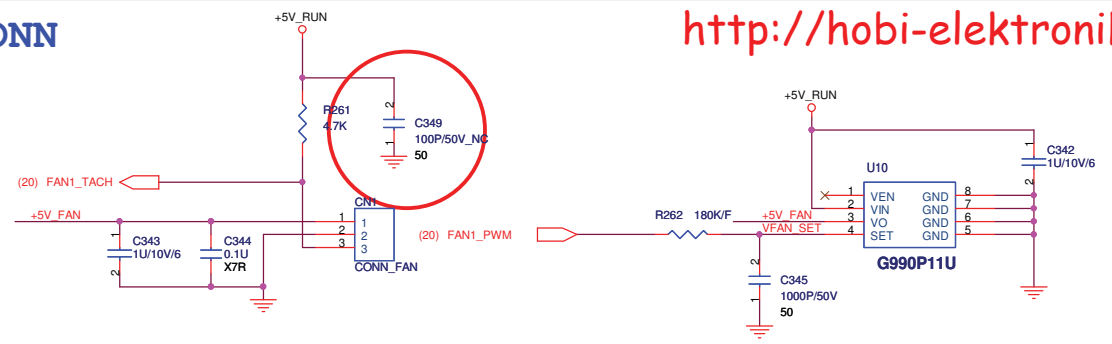
**QUANTA COMPUTER**

Title: TOUCH PAD, KEYBOARD

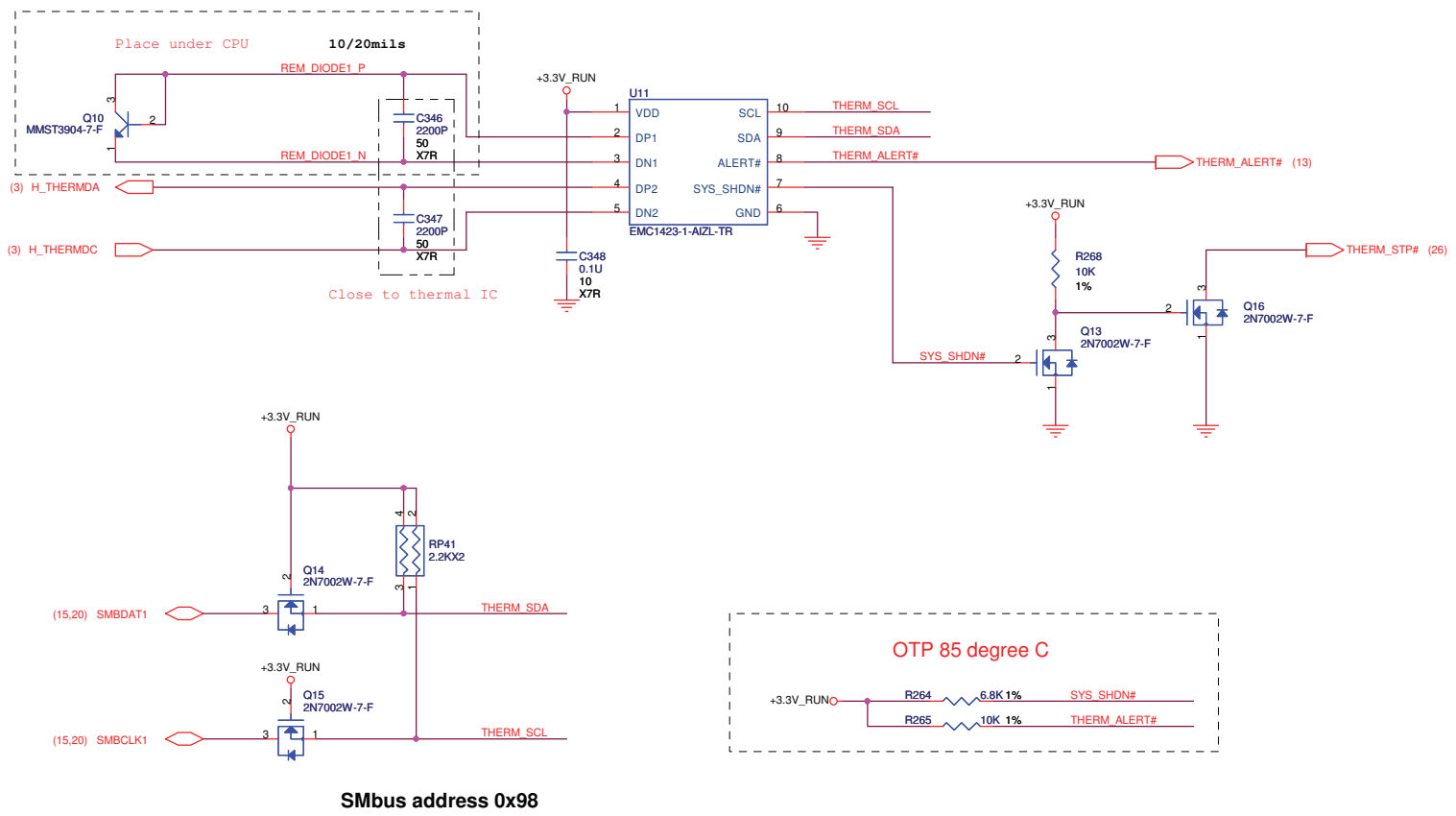
Size: Document Number UM2 UMA Rev 2A

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### FAN CONN

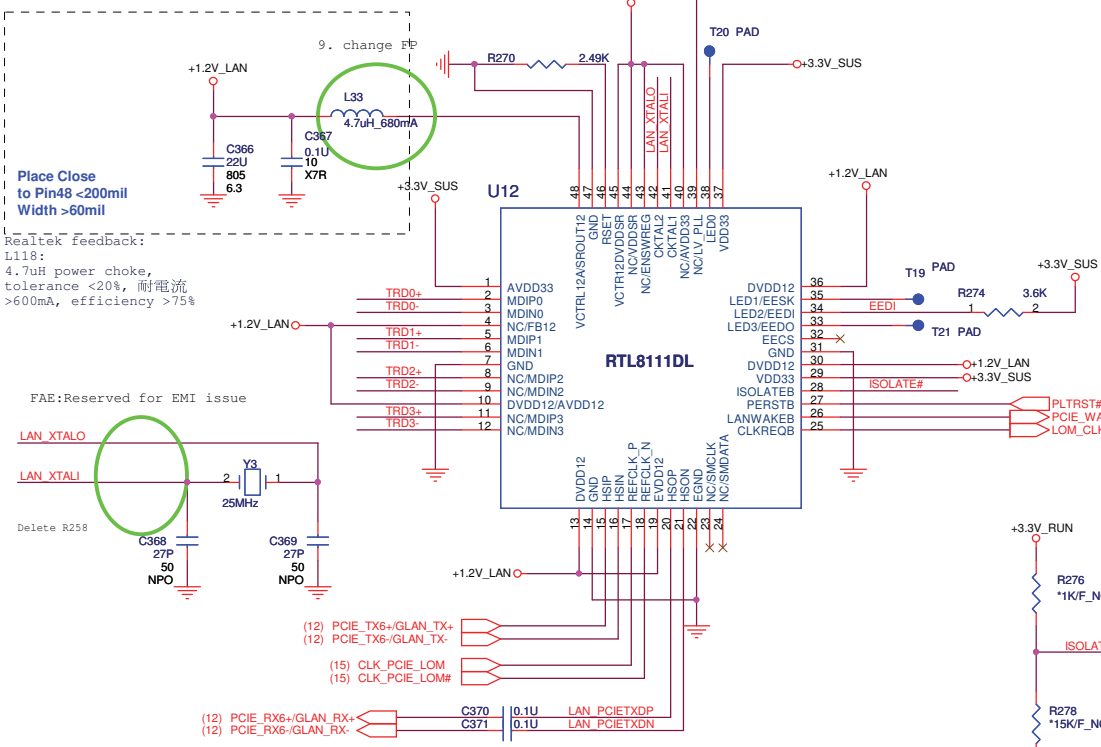
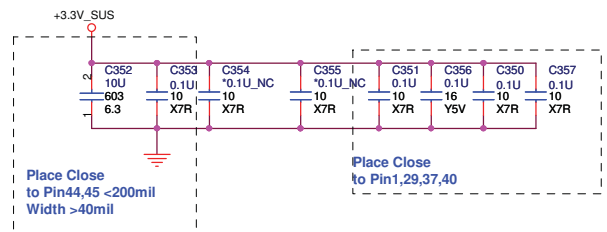
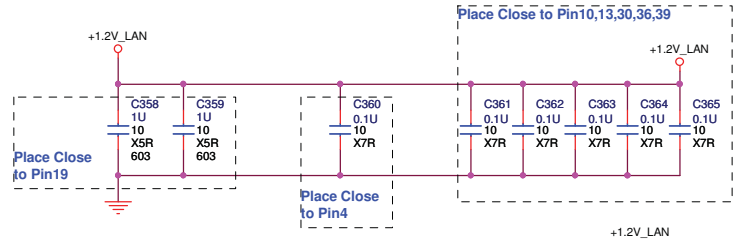


### THERMAL IC

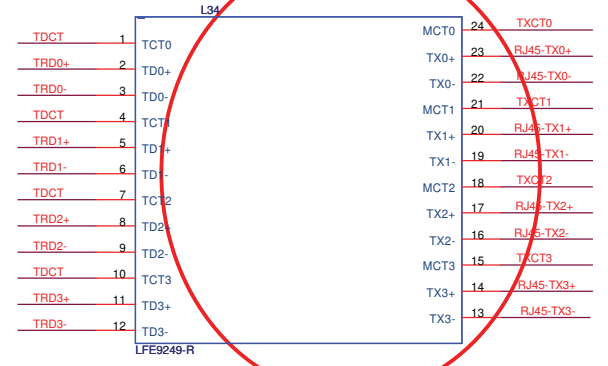
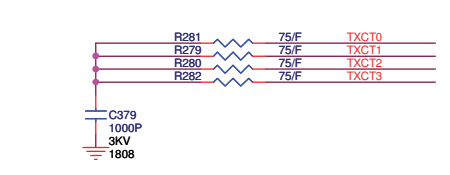
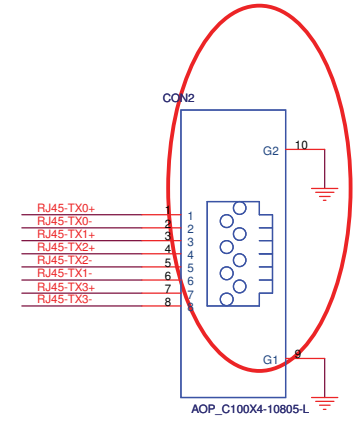


SMBus address 0x98

Title FAN & THERMAL		
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ISOLATEB  
 Datasheet(V1.4)P5:  
 Used to isolate the RTL8111DL from the PCI-E bus. RTL8111DL will not drive its PCI-E outputs(excluding LANWAKEB) and will not sample its PCI-E input as long as the isolate pin is asserted.  
 Realtek feed back:  
 進入S3,S4,S5要  
 拉low 離開S3,S4,S5要拉high for WOL support



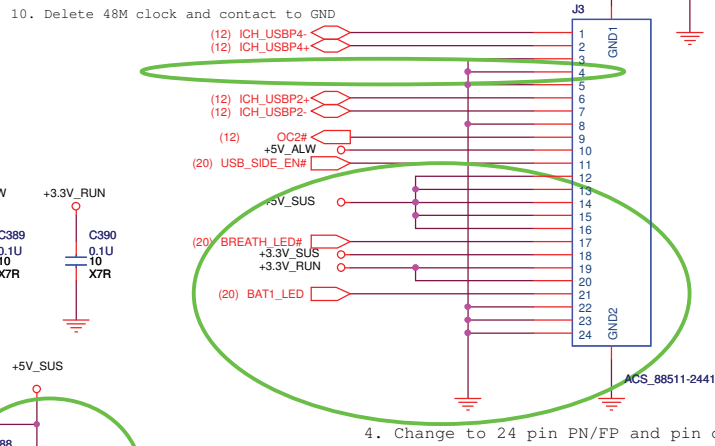
LAYOUT NOTE:  
 CAP CLOSE TO TRANSFORMER  
 one cap for each pin  
 Reserved for EMI.



Title LAN/RJ45		
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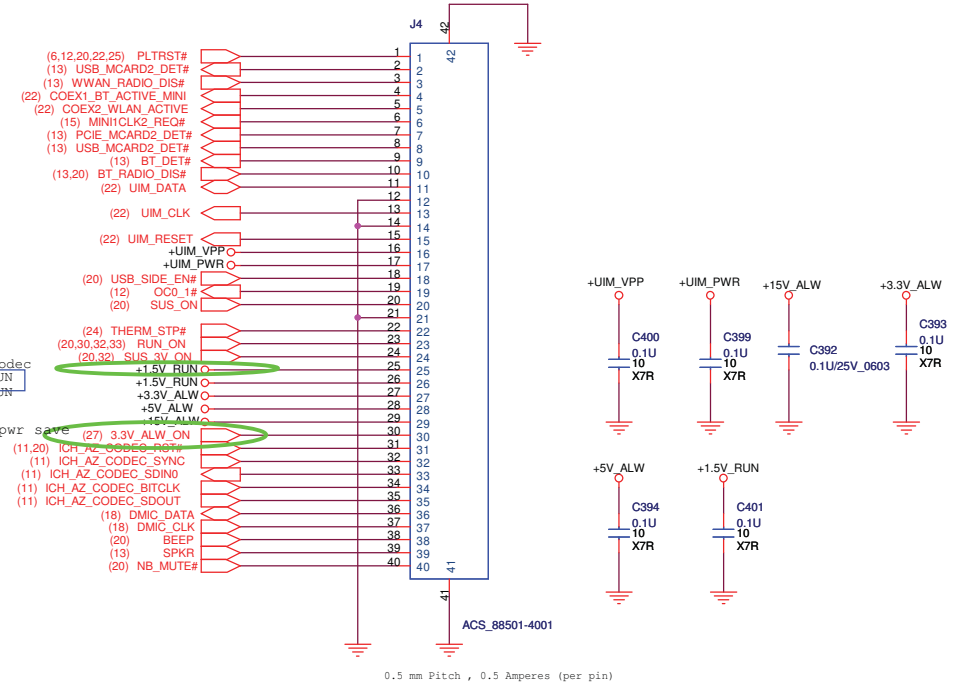
## To CardReader Board

Cable connect to DB directly  
DB need to reverse pin definition with MB



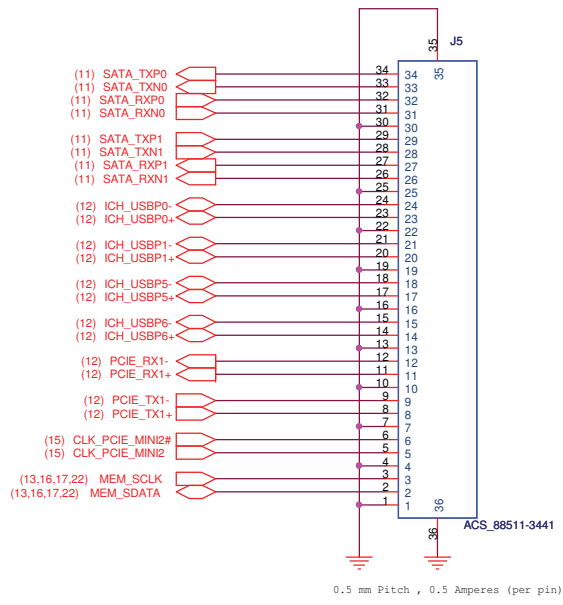
## To I/O Board

FFC connect to DB with one turn  
DB need to follow pin definition with MB

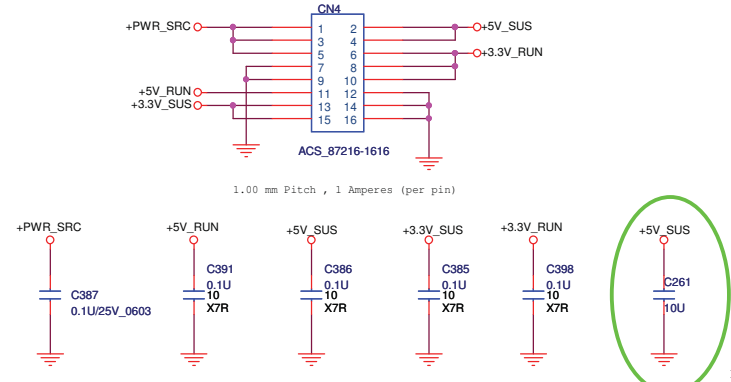


## To I/O Board

Cable connect to DB directly  
DB need to reverse pin definition with MB  
Zo=95



## To I/O Board



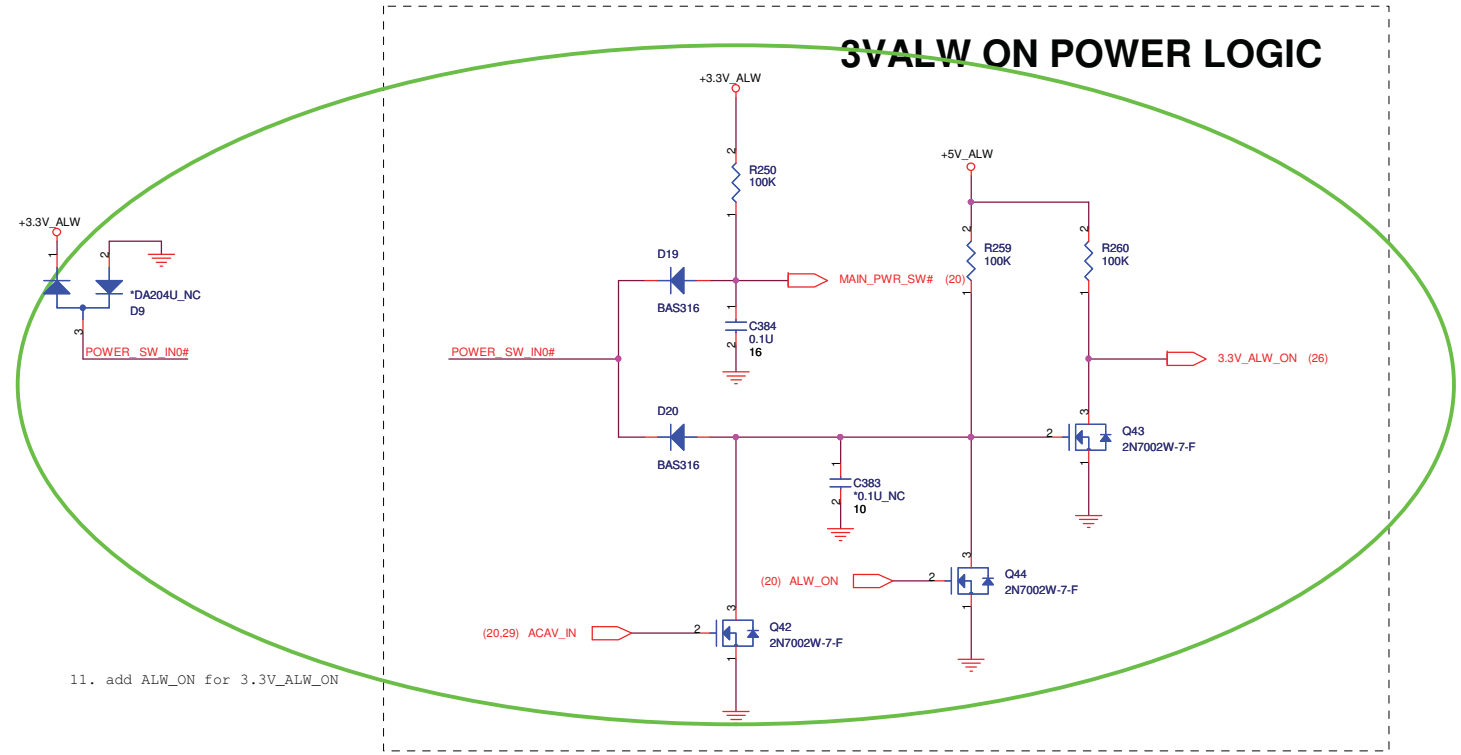
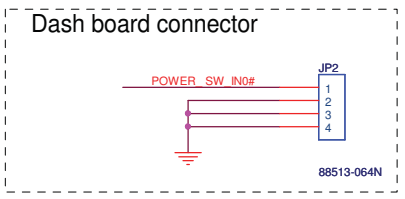
**QUANTA COMPUTER**

Title: IO BOARD


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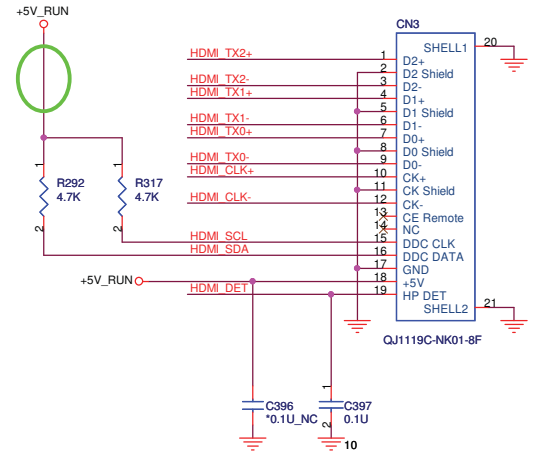
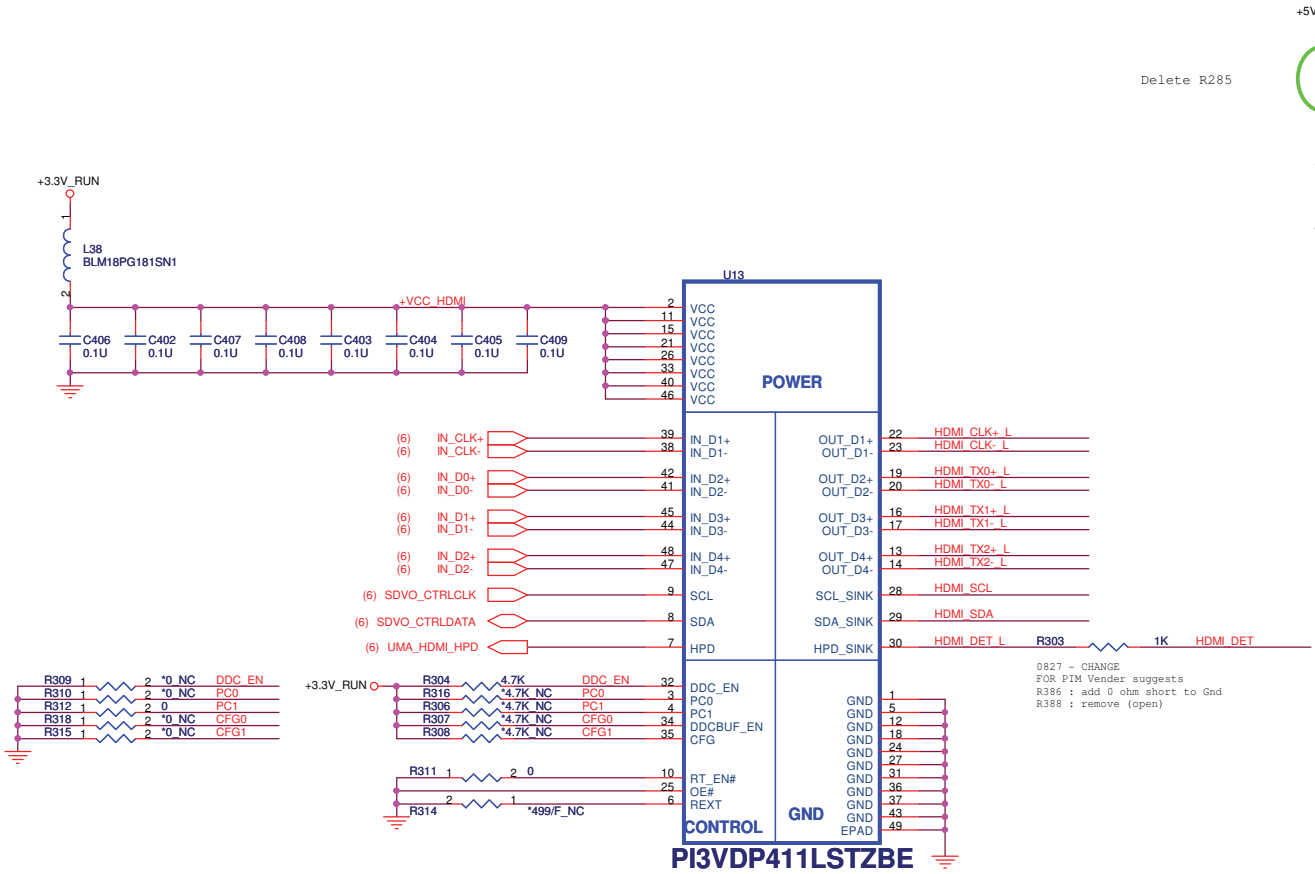




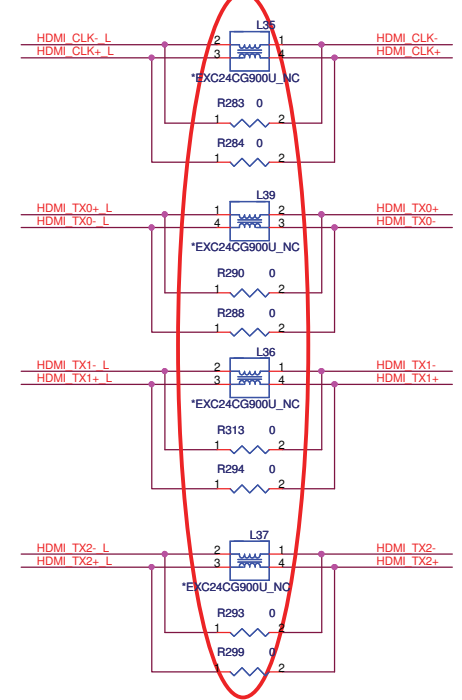
11. add ALW\_ON for 3.3V\_ALW\_ON

 <b>QUANTA COMPUTER</b>		
Title POWER SWITCH		
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# HDMI Connector



Reserve for EMI and close to HDMI CONN

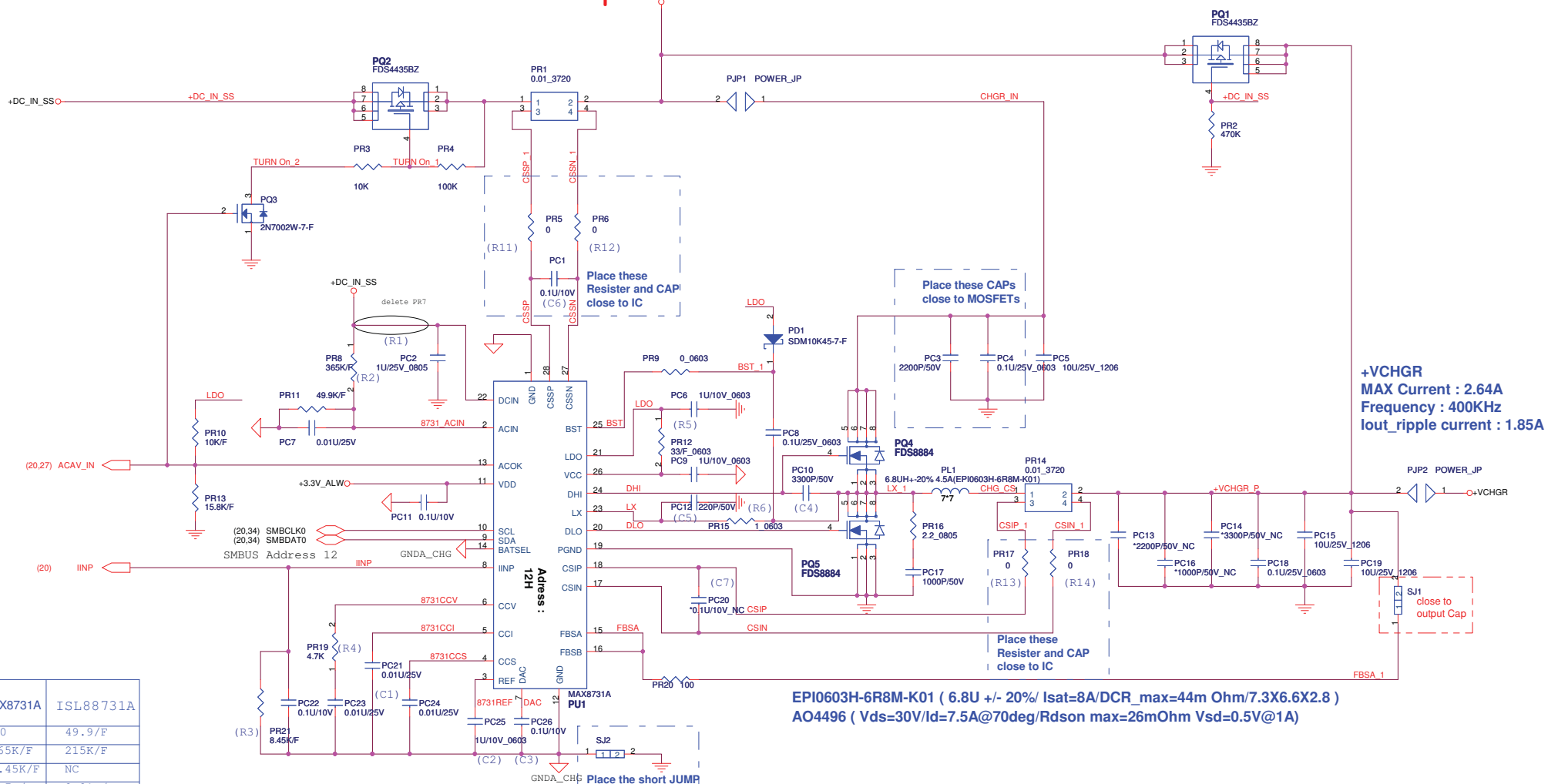


**EQUALIZATION SETTING**  
 PC1:PC0=0:0 8dB  
 PC1:PC0=0:1 4dB Recommended  
 PC1:PC0=1:0 12dB  
 PC1:PC0=1:1 0dB

**SCLZ/SDAZ Low-level input/output Voltage**  
 CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)  
 CFG1:CFG0=0:1 VIL:<0.36V VOL:0.55V  
 CFG1:CFG0=1:0 VIL:<0.44V VOL:0.65V  
 CFG1:CFG0=1:1 VIL:<0.36V VOL:0.6V



Title HDMI		
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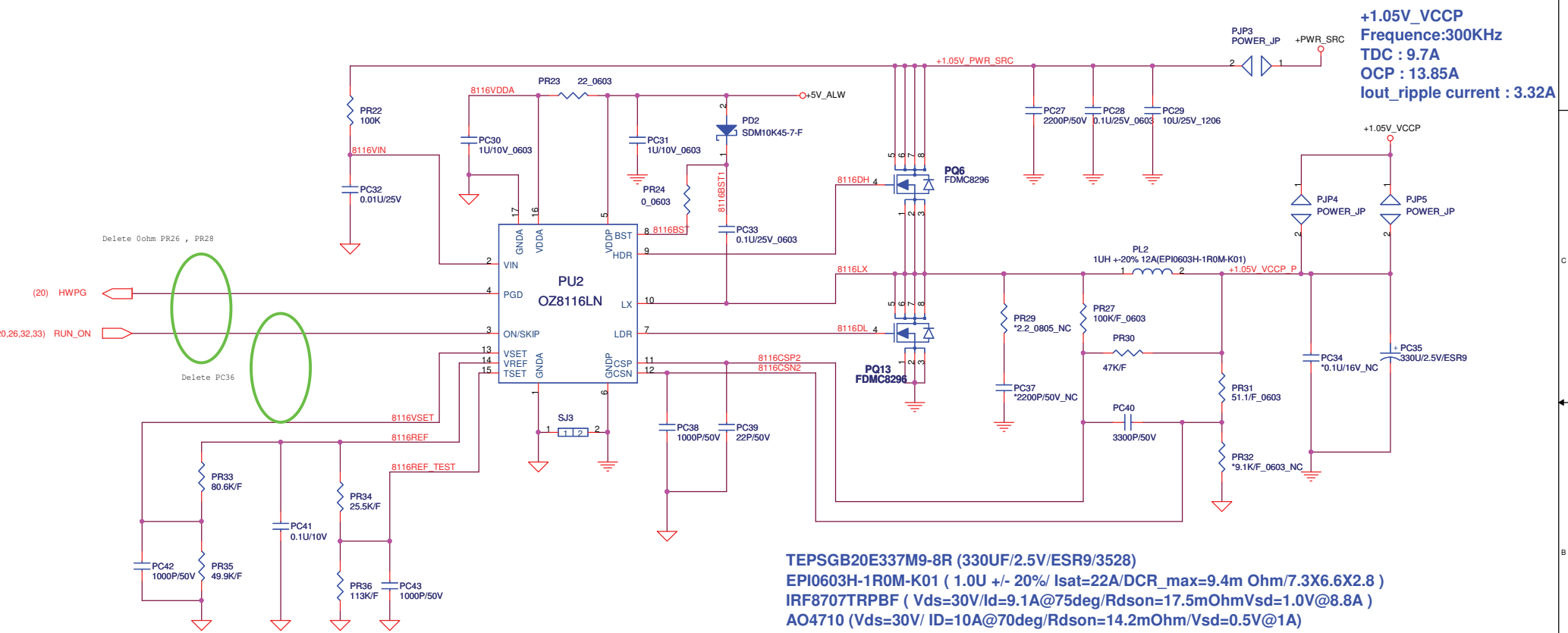


**+VCHGR**  
 MAX Current : 2.64A  
 Frequency : 400KHz  
 Iout\_ripple current : 1.85A

**EPI0603H-6R8M-K01 ( 6.8U +/- 20%/ Isat=8A/DCR\_max=44m Ohm/7.3X6.6X2.8 )**  
**AO4496 ( Vds=30V/Id=7.5A@70deg/Rdson max=26mOhm Vsd=0.5V@1A)**

	MAX8731A	ISL88731A
R1	0	49.9/F
R2	365K/F	215K/F
R3	8.45K/F	NC
R4	4.7K/F	2.21K/F
R5	33/F	4.7/F
R6	1	0
R7	NC	NC
R8	0	0
R9	NC	NC
R10	0	0
R11	0	10/F
R12	0	10/F
R13	0	10/F
R14	0	10/F
C1	0.01uF	NC
C2	1uF	NC
C3	0.1uF	NC
C4	3300PF	NC
C5	220PF	NC
C6	NC	0.1uF
C7	NC	0.1uF

ADAPTER (W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.28

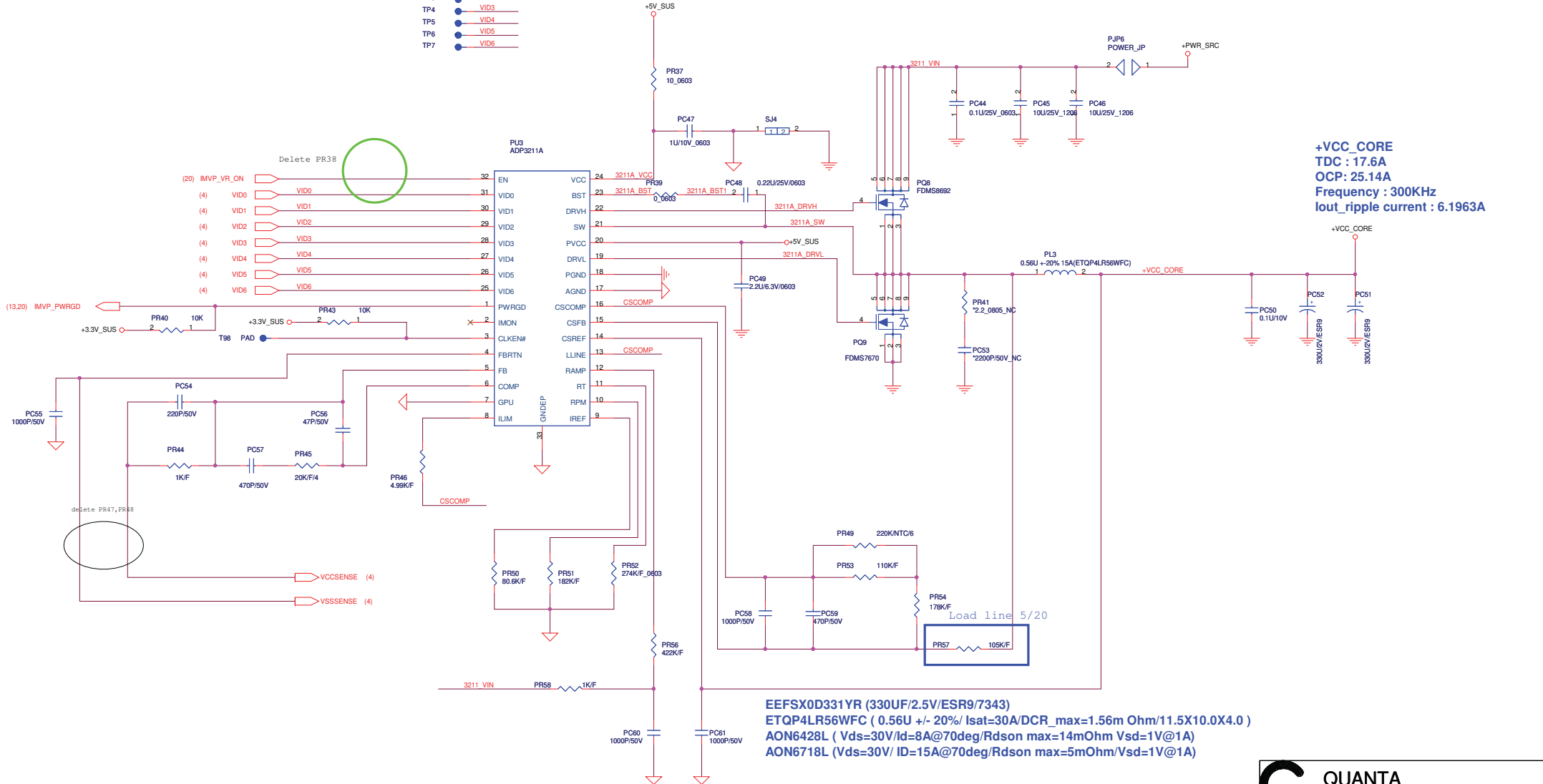


**+1.05V\_VCCP**  
 Frequence:300KHz  
 TDC : 9.7A  
 OCP : 13.85A  
 Iout\_ripple current : 3.32A

TEPSGB20E337M9-8R (330UF/2.5V/ESR9/3528)  
 EPI0603H-1R0M-K01 ( 1.0U +/- 20%/ Isat=22A/DCR\_max=9.4m Ohm/7.3X6.6X2.8 )  
 IRF8707TRPBF ( Vds=30V/Id=9.1A@75deg/Rdson=17.5mOhmVsd=1.0V@8.8A )  
 AO4710 (Vds=30V/ ID=10A@70deg/Rdson=14.2mOhm/Vsd=0.5V@1A)

CPU CORE

- TP1 ● VID0
- TP2 ● VID1
- TP3 ● VID2
- TP4 ● VID3
- TP5 ● VID4
- TP6 ● VID5
- TP7 ● VID6

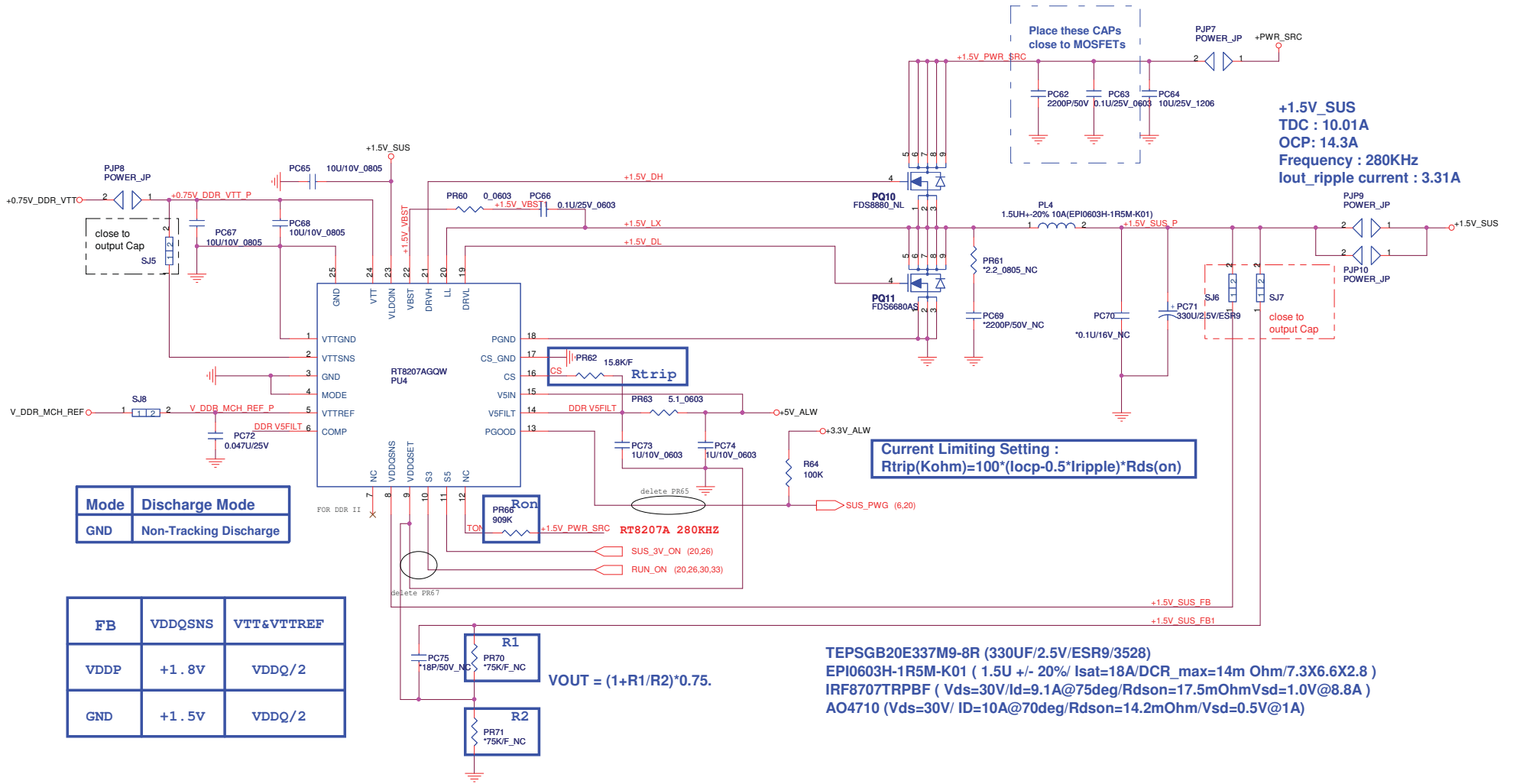


**+VCC\_CORE**  
 TDC : 17.6A  
 OCP: 25.14A  
 Frequency : 300KHz  
 Iout\_ripple current : 6.1963A

EEFSX0D331YR (330UF/2.5V/ESR9/7343)  
 ETQP4LR56WFC ( 0.56U +/- 20%/ Isat=30A/DCR\_max=1.56m Ohm/11.5X10.0X4.0 )  
 AON6428L ( Vds=30V/Id=8A@70deg/Rdson max=14mOhm Vsd=1V@1A )  
 AON6718L ( Vds=30V/ ID=15A@70deg/Rdson max=5mOhm/Vsd=1V@1A )

**QUANTA COMPUTER**

Title	CPU_(ADO3211A)	
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**+1.5V\_SUS**  
 TDC : 10.01A  
 OCP: 14.3A  
 Frequency : 280KHz  
 Iout\_ripple current : 3.31A

**Current Limiting Setting :**  
 $R_{trip}(Kohm) = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$

<b>Mode</b>	<b>Discharge Mode</b>
GND	Non-Tracking Discharge

FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

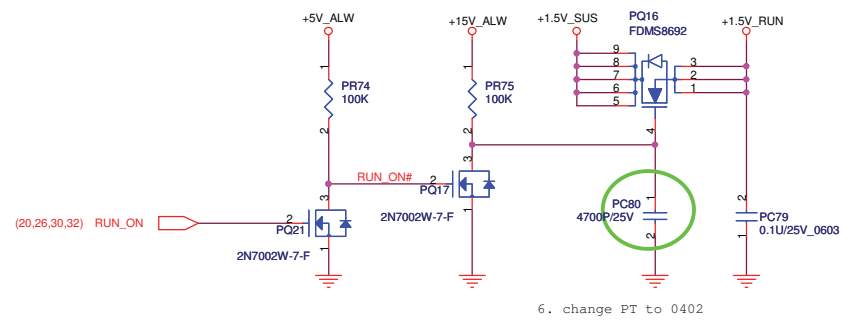
$V_{OUT} = (1 + R1/R2) * 0.75.$

TEPSGB20E337M9-8R (330UF/2.5V/ESR9/3528)  
 EPI0603H-1R5M-K01 ( 1.5U +/- 20% / Isat=18A/DCR\_max=14m Ohm/7.3X6.6X2.8 )  
 IRF8707TRPBF ( Vds=30V/Id=9.1A@75deg/Rdson=17.5mOhm/Vsd=1.0V@8.8A )  
 AO4710 ( Vds=30V/ ID=10A@70deg/Rdson=14.2mOhm/Vsd=0.5V@1A )



### +1.5V\_RUN

Max current(TDC) : 1.6A



### +1.8V\_RUN

Max current (TDC) ->105mA  
For UMA

