AND8331/D

Quasi-Resonant Current-Mode Controller for High-Power ac-dc Adapters

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Introduction

This document describes the implementation of the DAP013 inside an AC-DC adapter.

The DAP013 offers everything to build high performance AC-DC converters or offline adapters. Thanks to a novel valley lockout system, the controller is able to switch inside the drain-source valley and is immune to valley jumping instabilities. When the output load decreases significantly, the controller toggles to a fixed peak current/variable frequency mode that ensures very low standby power consumption. And last, but not least, the DAP013 features the usual protections that help to build cheap and safe power supplies: OVP, OTP, Brown-Out (C and D options), Short-circuit protection (latched for A, C versions and auto-recovery for D, F versions), soft-start, OPP, internal TSD...

To summarise, the DAP013 offers the following characteristics:

- Quasi-resonant Peak Current-mode Control Operation
- Valley Switching Operation with Valley-lockout for Noise-immune Operation
- VCO Mode (fixed peak current, variable frequency) in Light Output Load for Improved Standby Dissipation
- Internal 5 ms Soft-start
- Loss-free Adjustable Over Power Protection
- Auto-recovery or Latched Internal Output Short-circuit Protection
- Adjustable Timer for Improved Short-circuit Protection
- Over-voltage and Over-temperature Protection Inputs
- Brown-out Input for C and D Versions
- +500 mA / –800 mA Peak Current Source/Sink Capability
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- 3 μs Blanking Delay to Ignore Leakage Ringing at Turn-off
- Extremely Low No-load Standby Power
- SO14 Package

Pin Description

Over Power Protection pin (OPP, pin 1): applying a negative voltage on this pin reduces the internal maximum peak current set point.

Over Temperature Protection pin (OTP, pin 2): Connect an NTC between this pin and ground. An internal current source biases the NTC. When the NTC pulls the pin down, the circuit permanently latches-off.

Timer pin (Timer, pin 3): Wiring a capacitor from this pin to ground helps selecting the timer duration.

Zero Voltage Detection pin (ZCD, pin 4): Connected to the auxiliary winding, this pin detects the core reset event.

Timing Capacitor pin (Ct, pin 5): A capacitor connected to this pin acts as the timing capacitor in VCO mode.

Feedback pin (FB, pin 6): Hooking an optocoupler collector to this pin will allow regulation.

Current Sense pin (CS, pin 7): This pin monitors the primary current and triggers the fault if needed.

Ground pin (GND, pin 8): The controller ground.

Driver pin (DRV, pin 9): This pin delivers pulses to the power MOSFET.

Power Supply pin (V_{CC}, pin 10): This pin supplies the controller and accepts voltage up to 28 V.

Brown-Out pin (BO, pin 11): Allows shutting-down the controller for a chosen input voltage level. (C and D versions only)

Over Voltage Protection pin (OVP, pin 12): By pulling this pin high, the controller can be permanently latched-off.

High Voltage pin (HV, pin 14): Connected to the bulk capacitor, this pin powers the internal current source to deliver a start-up current that charges the V_{CC} capacitor.

I. Over Power Protection

1. How Does It Work?

A flyback operated in Quasi Resonant mode exhibits wide peak current variations in relationship to the input voltage conditions. As a result, the converter output power range widens as the input voltage increases. To cope with safety requirements, the designer needs to make the power output capability independent from the input conditions. A possible

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way of doing it is call Over Power Protection (OPP). The novel technique implemented in the DAP00X takes benefits of the auxiliary winding voltage whose negative amplitude relates to the input rail voltage. When the power MOSFET is conducting, the auxiliary winding voltage becomes the input voltage V_{IN} affected by the auxiliary to primary turn ratio $\left(N_{p,aux} = \frac{N_{aux}}{N_p}\right)$:

$$V_{aux} = -N_{p,aux}V_{IN} \quad \text{(eq. 1)}$$

By applying this voltage through a resistor divider on the OPP pin, we have an image of the input voltage transferred to the controller via this pin. This voltage is added internally to the 0.8 V reference and affects the maximum peak current (see Figure 1). As the OPP voltage is negative, an increase of input voltage implies a decrease of the maximum peak current setpoint:

$$V_{CS,max} = 0.8 + V_{OPP} \quad \text{(eq. 2)}$$

If OPP pin is grounded, there is no decrease of the peak current setpoint.

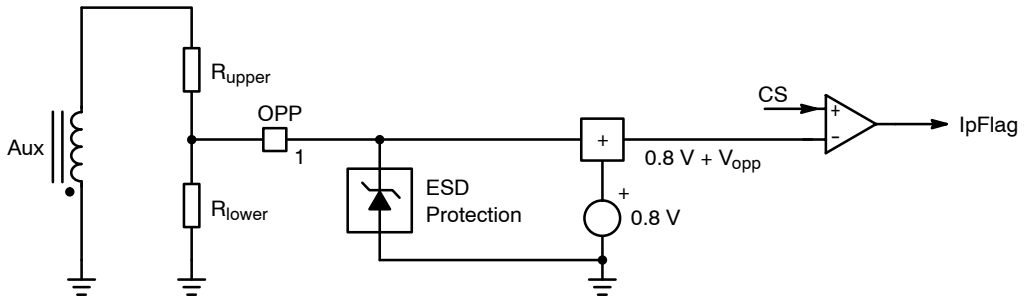

Figure 1. OPP Circuitry

The amount of negative voltage that can be applied on the OPP pin is limited by the ESD diode placed on the pin to protect the silicon. Temperature characterization shows that this diode will start to conduct if the applied bias (V_{OPP}) is lower than −300 mV. Thus, if a voltage lower than −300 mV is applied on the OPP pin, the peak current decrease will no longer be linear.

But knowing the amount of current that will circulate inside the OPP diode for these values of V_{OPP}, it is possible to set a higher bias current inside the resistor divider in order to neglect the diode leakage for OPP voltage lower than −300 mV. Figure 2 shows the diode leakage at different junction temperatures according to V_{OPP}. In any case, it is forbidden to inject current higher than 2 mA in this pin otherwise, substrate injections could occur, leading to a possible erratic behaviour.

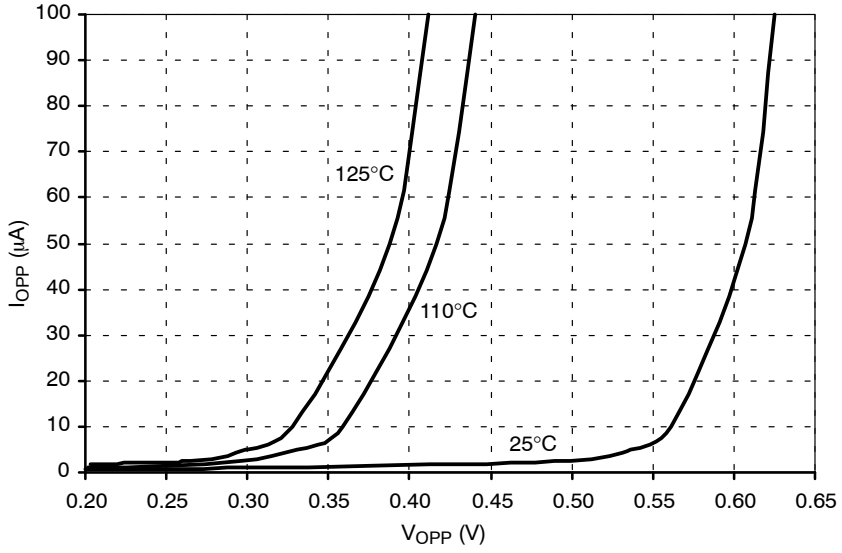

Figure 2. OPP Diode Leakage Current vs. V_{OPP} at T_J = 25°C, 110°C, 125°C

In order to filter the switching noise on OPP signal, the designer can add a small capacitor between OPP and GND. This capacitor value can be adjusted according to the power MOSFET on-time duration at high line and must not be higher than 200 pF.

2. OPP Resistors Calculation

Let us assume the design needs a peak current reduction of 34% at 370 V dc, therefore, the amount of voltage we must apply on pin 2 is:

$$V_{OPP} = -0.8 \times 0.34 = -272\ mV \quad \text{(eq. 3)}$$

By using the resistor divider law on R_{upper}, R_{lower} we obtain:

$$V_{OPP} = -\frac{R_{lower}}{R_{upper} - R_{lower}} N_{p,aux} V_{IN} \quad \text{(eq. 4)}$$

Or:

$$\frac{R_{upper}}{R_{lower}} = -\frac{N_{p,aux} V_{IN} - V_{OPP}}{V_{OPP}} \quad \text{(eq. 5)}$$

If our auxiliary to primary turn ratio is 0.12, we obtain:

$$\frac{R_{upper}}{R_{lower}} = -\frac{0.12 \times 370 - (-0.272)}{-0.272} \approx 164 \quad \text{(eq. 6)}$$

Thus, we can select:

R_{upper} = 160 kΩ and R_{lower} = 1 kΩ

The bridge current during the on time is:

$$I_{bridge} = \frac{V_{OPP}}{R_{lower}} \quad \text{(eq. 7)}$$

$$I_{bridge} = \frac{0.272}{1000} = 272\ \mu A \quad \text{(eq. 8)}$$

3. Why is the OPP Non Dissipative?

Let us try to calculate the average current in the OPP bridge:

$$I_{bridge,mean} = \frac{1}{T_{sw}} \int_0^{T_{sw}} \left| \frac{V_{aux}(t)}{R_{upper} + R_{lower}} \right| dt \quad \text{(eq. 9)}$$

After some calculations, we obtain:

$$I_{bridge,mean} = \frac{1}{R_{upper} + R_{lower}} \left(\frac{T_{on}}{T_{sw}} N_{p,aux} V_{IN} + \frac{T_{off}}{T_{sw}} (V_{CC} + V_f) \right) \quad \text{(eq. 10)}$$

Keeping up with our example from before, we can measure T_{on}, T_{off}, T_{sw} on our adapter at 370 V dc, light output load (we are in VCO mode): T_{on} = 1.2 μs, T_{off} = 3.6 μs, T_{sw} = 40 μs

$$I_{bridge,mean} = \frac{1}{160\ k + 1\ k} \left(\frac{1.2\ \mu}{40\ \mu} \times 0.12 \times 370 + \frac{3.6\ \mu}{40\ \mu} 25.6 \right) = 2.26\ \mu A \quad \text{(eq. 11)}$$

If we had selected R_{lower} = 100 Ω and R_{upper} = 16 kΩ (meaning we impose a higher bias current in the resistor bridge), we would have I_{bridge} = 22.6 μA only!

4. OPP Trick

From our previous example, we have calculated the OPP resistors in order to have a peak current reduction of 34% at 370 V dc that corresponds to V_{OPP} = -272 mV.

We obtained: R_{lower} = 1 kΩ and R_{upper} = 160 kΩ

Now, with these resistors what will be the peak current reduction at 110 V dc?

$$V_{OPP} = -\frac{R_{lower}}{R_{upper} + R_{lower}} N_{aux,p} V_{IN} = \frac{1}{161} \times 0.12 \times 110 = 82\ mV \quad \text{(eq. 12)}$$

This corresponds to a peak current reduction of 10.2% at low line. However because of the internal propagation delay, the peak current reduction is smaller is reality.

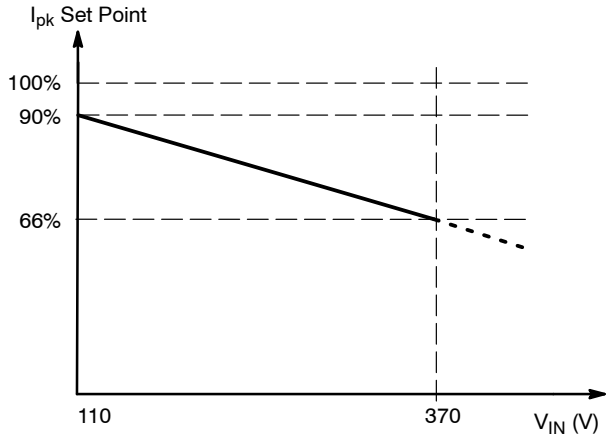

Figure 3. Peak Current Set Point over the Input Voltage with R_{upper} = 160 kΩ and R_{lower} = 1 kΩ

If we want to avoid losing 10% maximum of peak current at low line, we can introduce a simple threshold in the OPP circuitry through a zener diode placed in series with the resistive divider as shown in Figure 4.

This extra diode allows selecting the input voltage at which we want to start applying over power compensation.

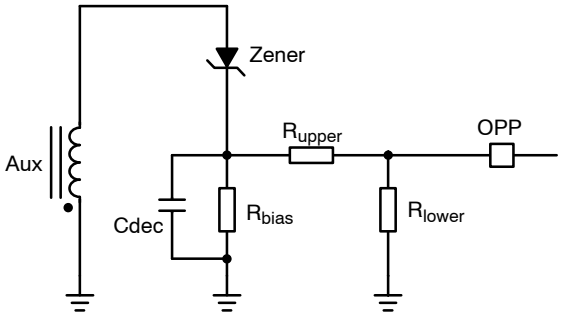

Figure 4. OPP with Zener Diode

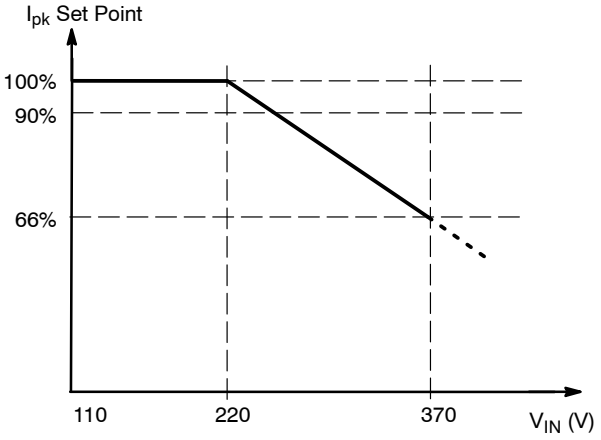

Figure 5. Ipk Set Point over Input Voltage using a Zener in Series with the OPP Resistors

Design Example:

We want to start reducing the maximum peak current around 220 V dc (roughly 155 Vrms).

This corresponds to an auxiliary winding voltage:

$$V_{aux} = -N_{p,aux}V_{IN} = -0.12 \times 220 = -26.4\ V \quad \text{(eq. 13)}$$

So we need a zener diode with a breakdown voltage:

$$BV_{DZ} = 0.12 \times (370 - 220) = 18\ V \quad \text{(eq. 14)}$$

The new values for OPP resistors can be calculated using Equation 15:

$$\frac{R_{upper}}{R_{lower}} = -\frac{N_{p,aux}V_{IN} - BV_{DZ} - V_{OPP}}{V_{OPP}} \quad \text{(eq. 15)}$$

$$\frac{R_{upper}}{R_{lower}} = -\frac{0.12 \times 370 - 18 - (-0.272)}{-0.272} = 98 \quad \text{(eq. 16)}$$

We choose: R_{upper} = 100 kΩ and R_{lower} = 1 kΩ

II. Over Temperature Protection

The adapter operating in a confined area, e.g. the plastic case protecting the converter, it is important to look after the internal ambient temperature. If this temperature would increase beyond a certain point, catastrophic failures could occur through semiconductors thermal runaway or transformer saturation. To prevent this from happening, the DAP00X embeds a novel Over Temperature Protection (OTP) circuitry appearing in Figure 6.

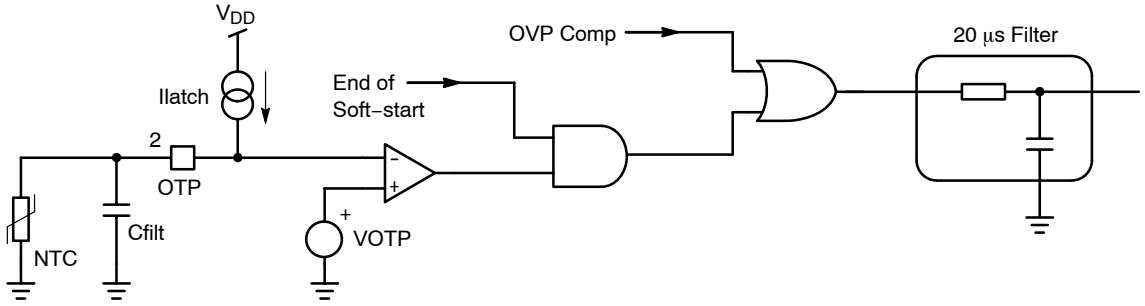

Figure 6. OTP Schematic

The I_{latch} current (91 μA typ.) biases the Negative Temperature Coefficient sensor (NTC), naturally imposing a dc voltage on the OTP pin. When the temperature increases, the NTC's resistance reduces (at 110°C, R_{NTC} = 8.8 kΩ instead of 470 kΩ at 25°C) bringing the pin 2 voltage down until it reaches a typical value of 0.8 V: the comparator trips and latches-off the controller (Figure 7). Controller reset occurs when a) the V_{CC} is cycled from on to off b) the brown-out pin senses a stop condition on the bulk voltage.

During start-up and soft-start, the output of the OTP comparator is masked to allow the voltage on pin OTP to grow if a filtering capacitor is installed across the NTC.

The filtering capacitor value should be 1 nF.

In DAP013, the OTP trip point corresponds to a resistance of:

$$R_{NTC} = \frac{V_{OTP}}{I_{latch}} = \frac{0.8}{91\ \mu} = 8.79\ k\Omega \qquad \text{(eq. 17)}$$

This corresponds to a temperature of 110°C using the TTC03-474.

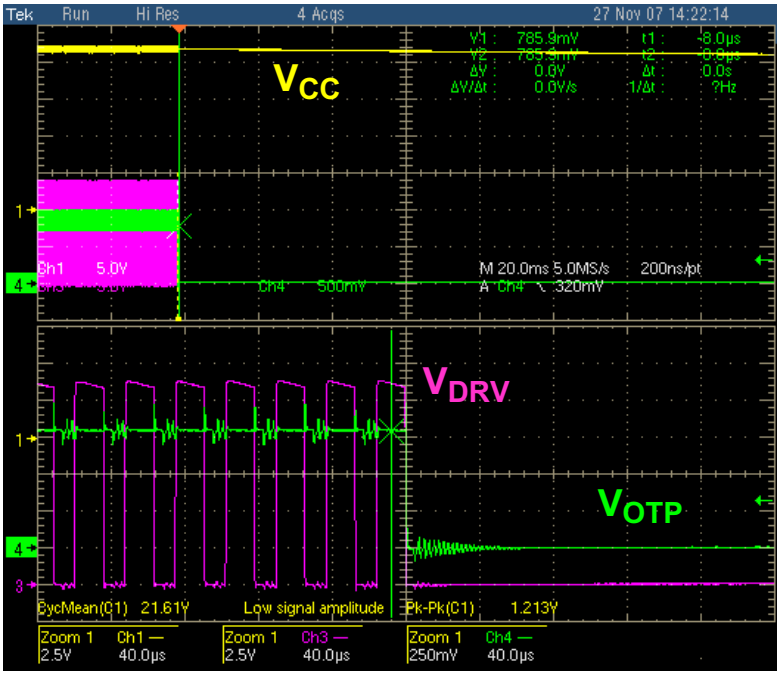

Figure 7. Capture of an OTP Event. Here, the NTC was Heated with a Hairdryer...

III. Timer Pin and Fault Management

Protection against short-circuit or overload is insured by monitoring the current sense signal. The controller reaction is thus fully independent from the auxiliary to power winding coupling. When the primary current exceeds I_{Limit}, the "Max Ip" comparator trips and the timer capacitor charges by the I_{timerC} current source. When the current comes back within safe limits, the "Max Ip" comparator becomes silent and the PWM comparator triggers the discharge of the timer capacitor. The timer capacitor is thus discharged by a constant current I_{timerD}. The internal circuitry appears in Figure 8.

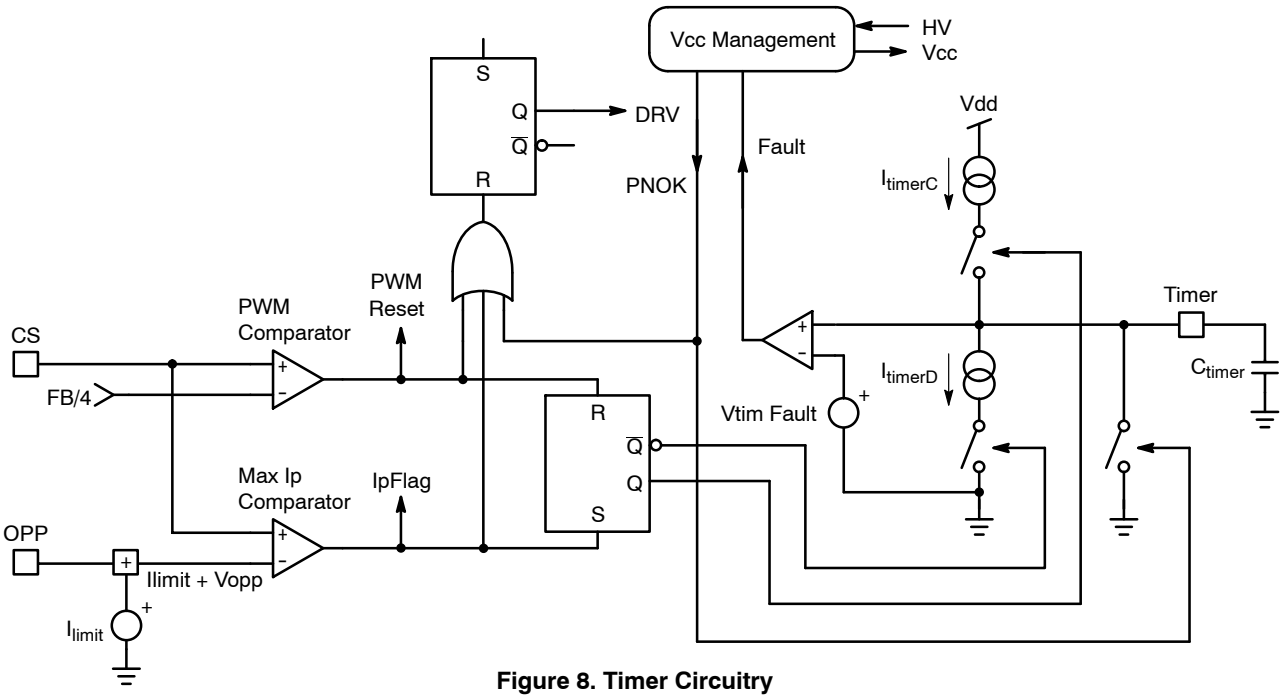

Figure 8. Timer Circuitry

For D and F versions, when the voltage of timer capacitor reaches $V_{timFault}$, the output pulses are stopped and the controller tries to re-start via a triple hiccup. (see Figure 9): this is the so-called auto-recovery operation.

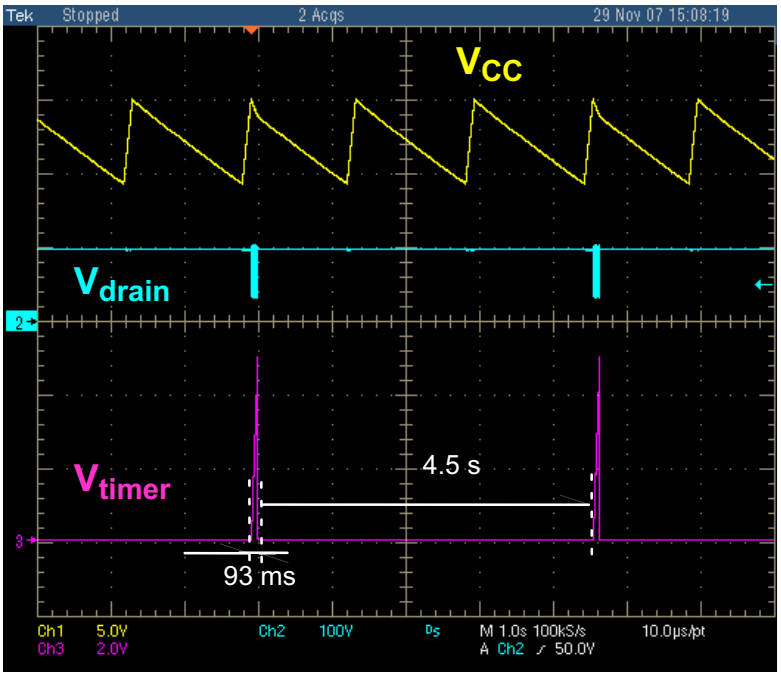

Figure 9. The Triple Hiccup in Fault Mode

The triple hiccup helps to reduce the power consumption in fault mode. In Figure 9, the burst is only 2% for a 60 W adapter (with C_{Vcc} = 100 µF).

For versions A and C, when V_{timer} reaches $V_{timFault}$, the controller stops pulsing and stays latched. To reset the controller, the user must unplug the power supply to allow V_{CC} to drop below $V_{CCreset}$ level (5.5 V). (see Figure 10)

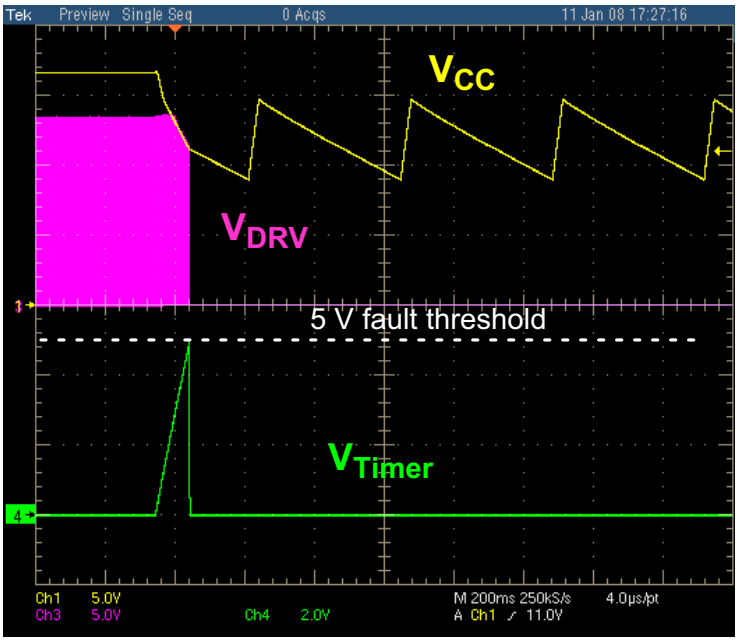

Figure 10. The Latched Short-circuit Protection in A and C Versions

Choosing Timer Duration and Timer Capacitor

While choosing the timer duration, the user must ensure that it is long enough to allow the power supply to enter regulation at low line and full load. (see Figure 11)

The timer capacitor value can be calculated with:

$$C_{timer} = \frac{T_{fault} I_{timerC}}{V_{timFault}} \qquad \text{(eq. 18)}$$

Where :

- T_{fault} is the duration before the fault validation
- I_{timerC} is the charging current (10 µA typ. from datasheet)
- $V_{timFault}$ is the timer voltage threshold at which the fault is validated (5 V typ. from datasheet)

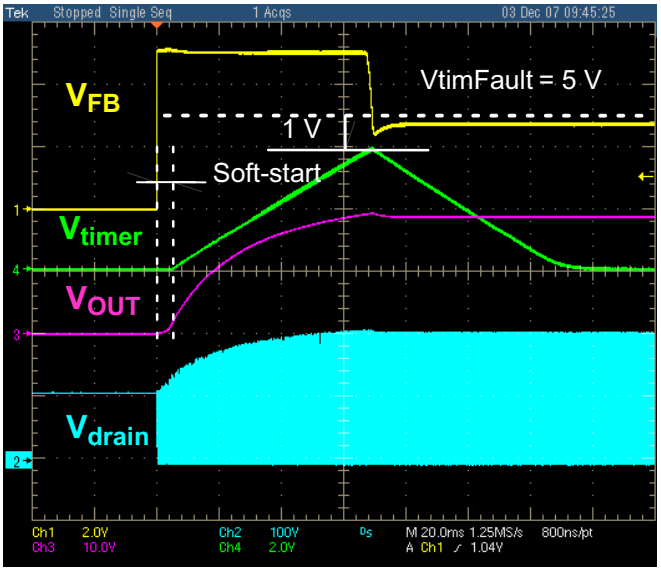

Figure 11. Timer Margin at Low Line, Full Load on a 19 V / 3 A Adapter

IV. Zero Voltage Crossing Detection

The Zero Crossing Detection circuit (ZCD) allows turning on the power MOSFET when the drain-source voltage is the lowest. This detection is achieved by monitoring the auxiliary winding voltage. The typical detection level is around 50 mV (Figure 12). By delaying this signal thanks to an RC network (the internal ESD protection features a parasitic capacitance of 10 pF) it is possible to switch right in the valley of the drain-source voltage.

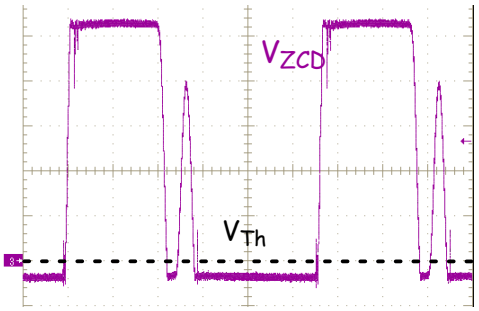

Figure 12. Typical ZCD Signal. Here, the Power Supply Operates in 2nd Valley

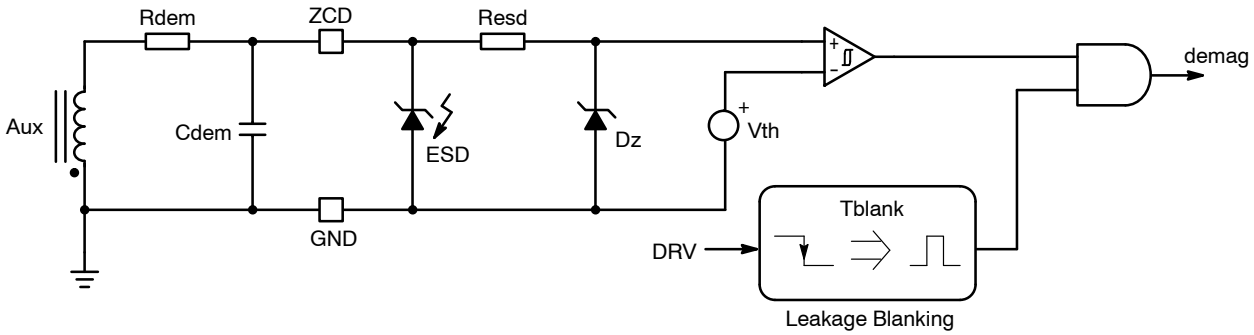

Figure 13. Zero Voltage Crossing Detection Circuit

R_{dem} should be calculated to limit the current inside pin 4 to less than +3 mA/-2 mA.

For example, if the voltage on auxiliary winding is –45 V at highest line, R_{dem} should be higher than 45/0.002 = 22.5 kΩ.

In order to avoid false triggering by the leakage inductance, a blanking circuit masks the ZCD signal during 2 to 4 μs. So when designing the power supply, the designer must ensure that during valley operation, the demagnetization duration is higher than 4 μs. If not, the 1st valley will also be blanked and valley switching instabilities will occur.

V. VCO Mode and Timing Capacitor

1. How Does it Work?

At nominal power, the power supply operates in a variable frequency system where discrete frequency steps occur as the controller looks for the different valley positions. At low output power, the controller enters a Voltage-Controlled Oscillator (VCO) mode where the switching frequency is folded back. This mode is entered when V_{FB} drops below 0.8 V. The controller remains in this mode until V_{FB} increases above 1.4 V. During the VCO operation (V_{FB} < 0.8 V), the peak current is frozen to 25% of its maximum value and the frequency diminishes as the output power decreases. (Figure 14)

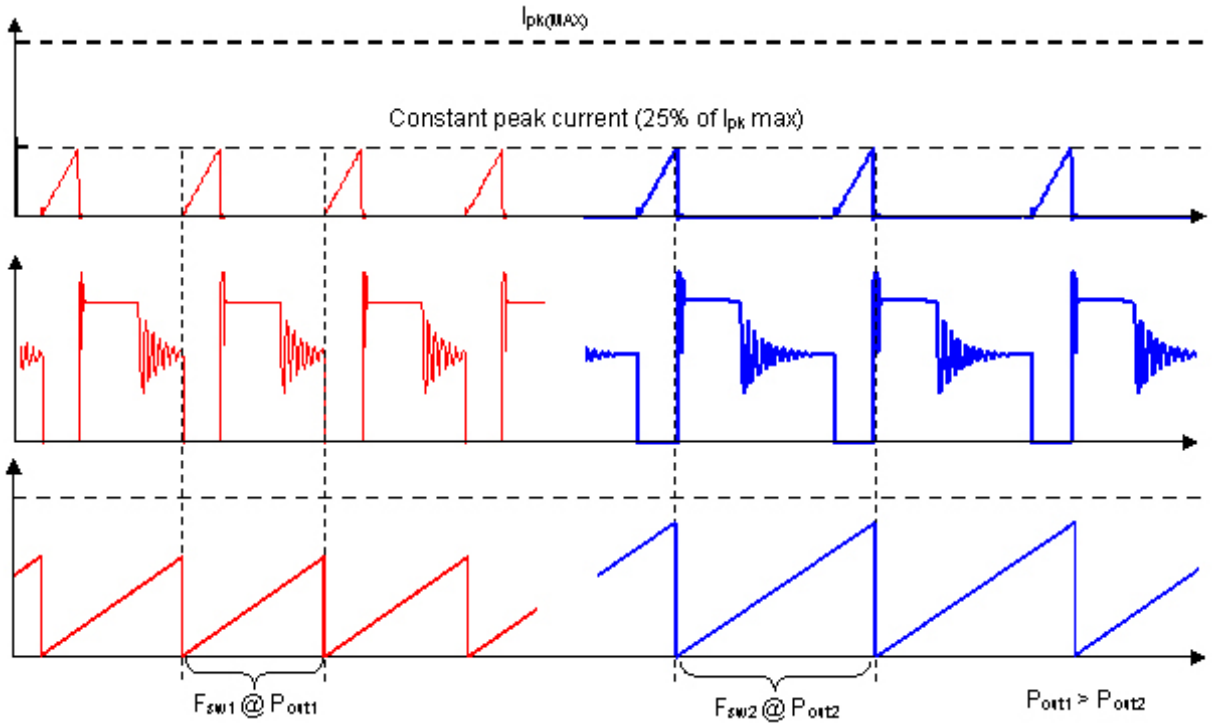

Figure 14. I_{drain}, V_{drain}, V_{Ct}, at Different Output Loads in VCO Mode

The switching frequency is set by the end of charge of the timing capacitor C_t. This capacitor is charged by a constant current source I_{Ct} and its voltage V_{Ct} is compared to an internal threshold fixed by the FB loop. When V_{Ct} reaches the threshold, the capacitor is rapidly discharged down to 0 V and a new period starts. The relationship between FB voltage and the internal threshold is:

$$V_{FBth} = 6.5 - (10/3)V_{FB} = V_{Ct} \qquad \text{(eq. 19)}$$

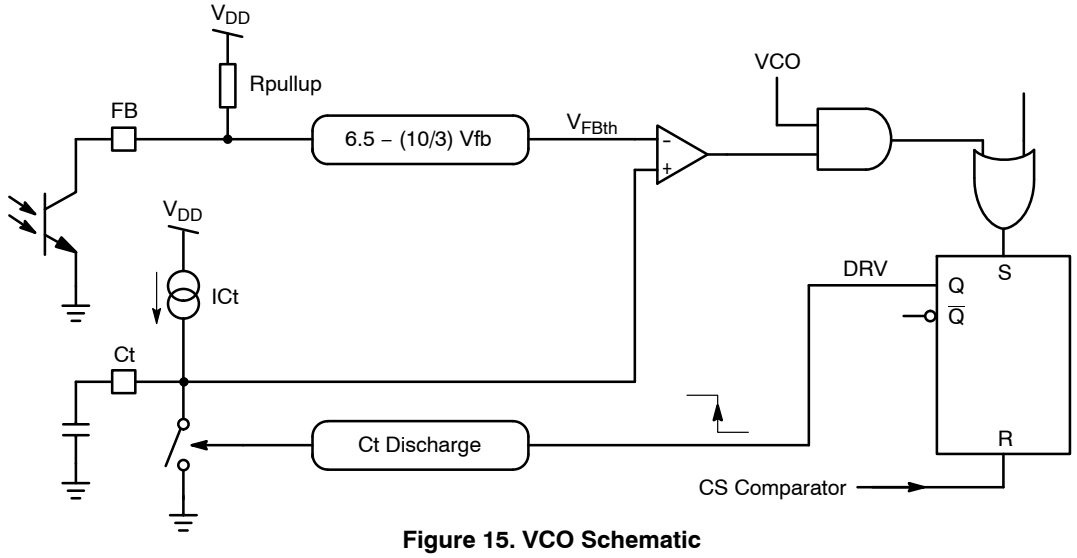

Figure 15. VCO Schematic

2. How to Calculate the Timing Capacitor Value?

The timing capacitor must be selected with care. Indeed, when the controller leaves the valley switching mode to enter the VCO mode, the frequency changes from a valley-position-controlled value to a switching frequency imposed by the C_t capacitor. If a too big gap exists between the switching frequency in the 4th valley and the switching frequency imposed by the C_t capacitor, the frequency jump may create an instability by forcing the peak current to leave its frozen state: an hesitation between 4th valley and the VCO mode takes place (Figure 16) and can create output ripple and noise.

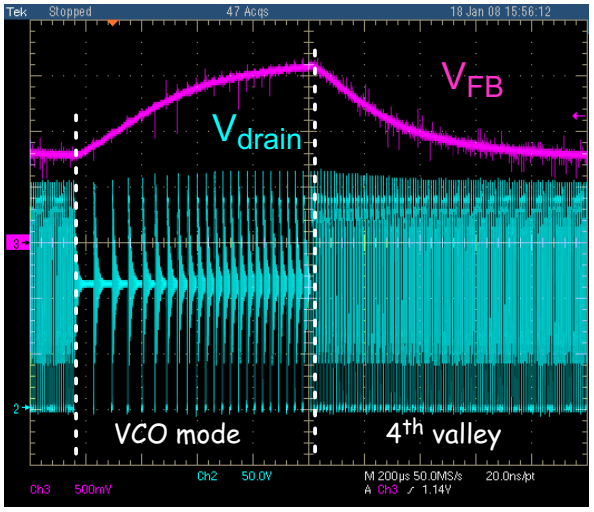

Figure 16. The Controller Hesitates between VCO Mode and 4th Valley: C_t is Too Big!

Figure 17 shows a normal transition from 4th valley to the VCO mode. At the beginning, the output load is such that it imposes a V_{FB} near 0.8 V in 4th valley operation, with a switching period T_{sw1}. Then, if the load is slightly decreased, the FB voltage also passes below the 0.8 V threshold: the VCO mode is entered and the switching frequency decreases. (In VCO mode, the switching frequency is imposed by the FB voltage regardless of the position in the drain signal). The controller will stay in VCO mode until the FB voltage increases above 1.4 V. If we have an optimum timing capacitor value, the new steady state point is such that V_{FB} is near 1.4 V and imposes a switching period T_{sw2} larger than T_{sw1}.

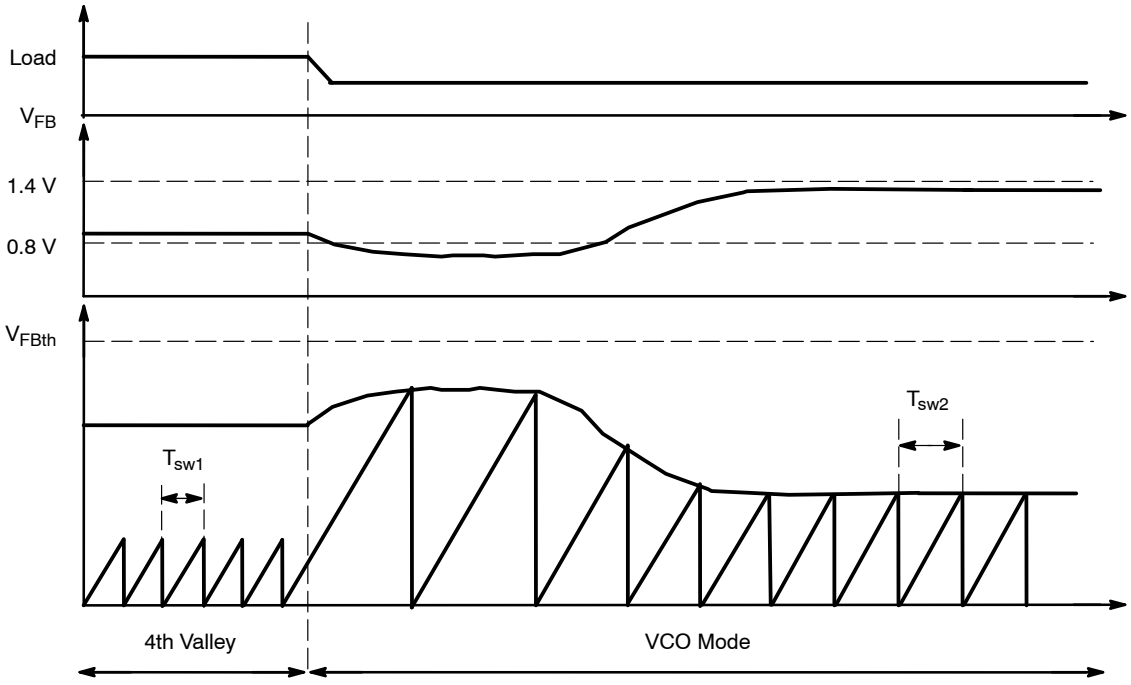

Figure 17. 4th Valley to VCO Mode Transition with an Optimum Timing Capacitor C_t

To calculate C_t, we first need to estimate the switching period at the end of the 4th valley operation, for a FB voltage near 0.8 V by using Equation 20 or by directly measuring it on our adapter:

$$T_{sw1} = \frac{0.2}{R_{sense}} L_p \left(\frac{1}{V_{IN,minDC}} + \frac{N_{ps}}{V_{out} + V_f} \right) + 7\pi \sqrt{L_p C_{lump}} \qquad \text{(eq. 20)}$$

Where:
- R_{sense} is the sense resistor
- 0.2 relates to the voltage setpoint on the current-sense comparator when V_{FB} = 0.8 V.
- L_p is the primary inductance
- $V_{IN,minDC}$ is the minimum DC input voltage, bulk ripple included
- $N_{ps} = N_s/N_p$ is the primary to secondary turn ratio of the transformer
- V_{out} is the output voltage
- V_f is the output diode forward voltage
- C_{lump} regroups all capacitances surrounding the drain node (MOSFET capacitor, transformer parasitics...). As a first approximation, you can use the MOSFET drain-source capacitance C_{OSS} instead of C_{lump}.

Based on lab experiments, the switching period gap between the end of 4th valley operation (T_{sw1}) and VCO mode (T_{sw2}) for a FB voltage near 1.4 V (which is the threshold for VCO mode to 4th valley transition, V_{FB} increasing) must not exceed 12 μs. Thus, for V_{FB} = 1.4 V, we will have:

$$T_{sw2} = T_{sw1} + 12\ \mu s \qquad \text{(eq. 21)}$$

Equation 13 allows calculating V_{Ct} for V_{FB} = 1.4 V:

$$V_{Ct} = 6.5 - (10/3) \times 1.4 = 1.83\ V \qquad \text{(eq. 22)}$$

Thus, we can deduce the timing capacitor value knowing V_{Ct}, T_{sw2} and the charging current source I_{Ct} (20 μA typ. from datasheet):

$$C_t = \frac{I_{Ct} T_{sw2}}{1.83} \qquad \text{(eq. 23)}$$

Application Example: **19 V/60 W Adapter**

- $V_{IN,minDC}$ = 100 V
- $V_{out} + V_f$ = 19 + 0.6 V
- L_p = 190 μH
- C_{lump} = 200 pF
- N_{ps} = 0.25
- R_{sense} = 0.25

First, with Equation 14, we estimate T_{sw1} which is the switching period of our power supply for an output load corresponding to a V_{FB} = 0.8 V:

$$T_{sw1} = \frac{0.2}{R_{sense}} L_P \left(\frac{1}{V_{IN,minDC}} + \frac{N_{ps}}{V_{out} + V_f} \right) + 7\pi \sqrt{L_p C_{lump}} \qquad \text{(eq. 24)}$$

$$= \frac{0.2}{0.25} 190 \times 10^{-6} \left(\frac{1}{100} + \frac{0.25}{19 + 0.6} \right) + 7\pi \sqrt{190 \times 10^{-6} \times 200 \times 10^{-12}} = 7.75\ \mu s\ (129\ kHz)$$

When measured on the adapter we have: T_{sw1} = 8.47 μs (F_{sw1} = 118 kHz) corresponds to an ouput power of 9 W.
We calculate the timing capacitor value:

$$C_t = \frac{I_{CT}(T_{sw1} + 12\ \mu)}{1.83} = \frac{20 \times 10^{-6}(7.75 \times 10^{-6} + 12 \times 10^{-6})}{1.83} = 216\ pF \qquad \text{(eq. 25)}$$

We select $\mathbf{C_t = 220\ pF}$.

VI. Feedback

The feedback pin features an internal pull-up resistor which connects to the optocoupler, as shown in Figure 18. This pin is also connected to the internal valley comparators that will select the operating valley according to the FB voltage (see datasheet).

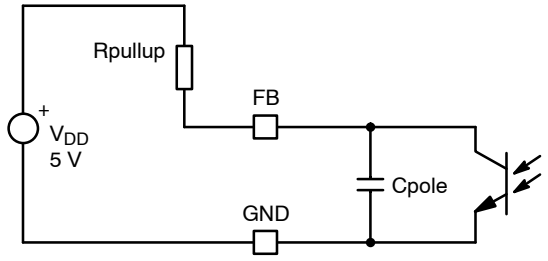

Figure 18. FB Pin Features an Internal Pull-up Resistor...

The pull-up resistor value is typically around 20 kΩ and is referenced in the datasheet.

It is recommended to add a capacitor between FB pin and GND pin of the controller. This capacitor has two advantages: it offers a filtering action on the FB signal and it forms with R_{pullup} a pole located at:

$$f_p = \frac{1}{2\pi R_{pullup} C_{pole}} \qquad \text{(eq. 26)}$$

This pole will help you to stabilize the power supply.

VII. VCC

The DAP013 includes a high voltage startup circuitry that derives current from the bulk line to charge the V_{CC} capacitor. When the power supply is first connected to the mains outlet, the internal current source is biased and charges up the V_{CC} capacitor. When the voltage on this V_{CC} capacitor reaches the V_{CCon} level, the current source turns off, reducing the amount of power being dissipated. At this time, the controller is only supplied by the V_{CC} capacitor, and the auxiliary supply should take over before V_{CC} collapses below V_{CCmin}. Figure 19 shows the internal arrangement of this structure:

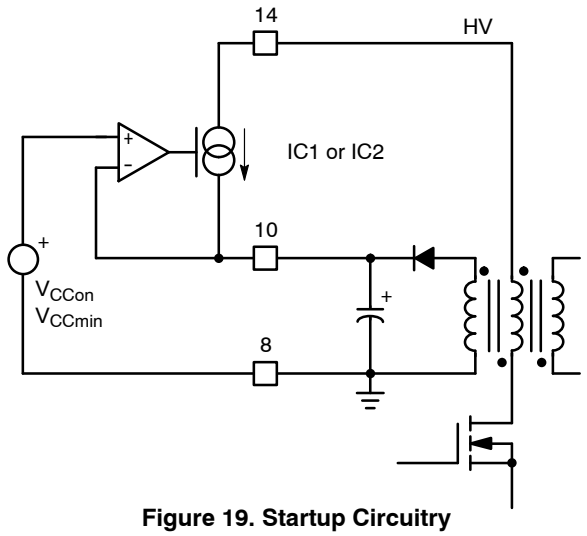

Figure 19. Startup Circuitry

1. How to Choose V_{CC} Capacitor?

The V_{CC} capacitor is calculated to allow the power supply to close the loop before V_{CC} drops to V_{CCmin}. If we call t_{reg} the time needed by the power supply to close the loop, the V_{CC} capacitor can be estimated with:

$$C_{Vcc} = \frac{(I_{CC2} + Q_g F_{sw}) t_{reg}}{V_{CCon} - V_{CCmin}} \quad \text{(eq. 27)}$$

Where:

- I_{CC2} is the controller consumption (see datasheet)
- Q_g is the MOSFET total gate charge
- F_{sw} is the switching frequency in maximum load, minimum input voltage

Now, we need to estimate the total startup time.

The high voltage startup circuit features two startup levels, I_{C1} and I_{C2}. At power-up, as long as V_{CC} is below V_{Th} (0.70 V typ.), the source delivers I_{C1} (around 300 µA typical). The duration is:

$$t_1 = C_{Vcc} \frac{V_{Th}}{I_{C1}} \quad \text{(eq. 28)}$$

Then, when V_{CC} reaches 0.70 V, the source smoothly transitions to I_{C2} (6 mA typ.) and delivers its nominal value. When V_{CC} reaches V_{CCon}, the source is turned-off:

$$t_2 = C_{Vcc} \frac{V_{CCon} - V_{Th}}{I_{C2}} \quad \text{(eq. 29)}$$

The total startup time is the sum of t_1, t_2 and t_{reg}.

$$t_{startup} = C_{Vcc}\left(\frac{V_{Th}}{I_{C1}} + \frac{V_{CCon} - V_{Th}}{I_{C2}}\right) + t_{reg} \quad \text{(eq. 30)}$$

For Example:

The time needed by the power supply to enter regulation is 45 ms worst case (full load).

The MOSFET is a 6A / 600 V with a gate charge:

Q_g = 24 nC

$$C_{Vcc} = \frac{(I_{CC2} + Q_q F_{sw}) t_{reg}}{V_{CCon} - V_{CCmin}} = \frac{(2.5 \times 10^{-3} + 24 \times 10^{-9} \times 65000)\, 45 \times 10^{-3}}{15 - 9} = 30.45\ \mu F \quad \text{(eq. 31)}$$

We choose: C_{Vcc} = 47 µF

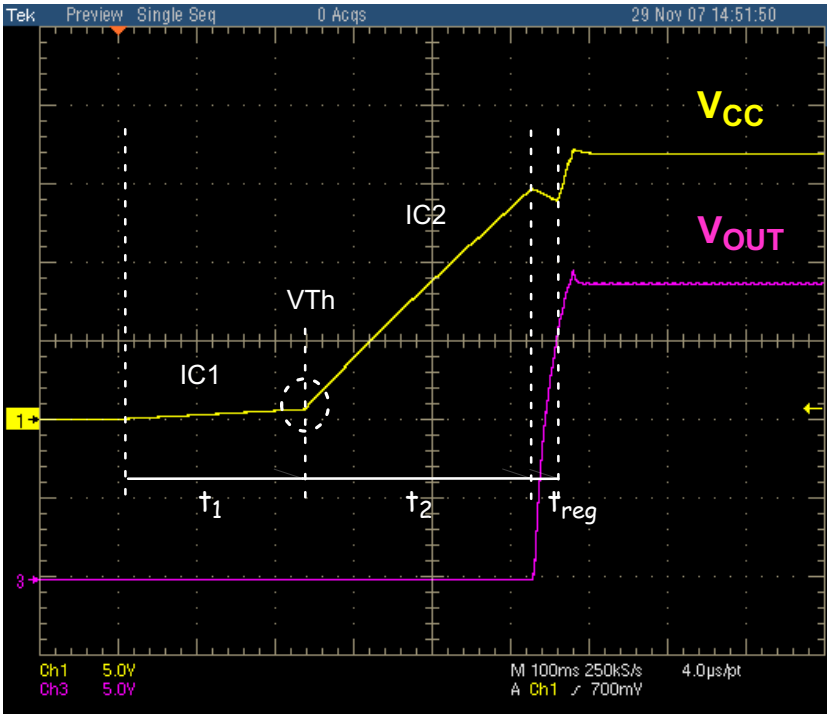

Figure 20. The Dual Level Startup Current Source in Action, Here with a V_{cc} Capacitor of 100 µF

2. What is the Benefit of Using a Dual Level Startup Current Source?

The dual level startup current source allows to limit the power dissipation of the controller in case of short-circuit between V_{CC} and GND.

Without the dual level startup, in high line conditions (V_{HV} = 370 V dc), the current delivered by the startup device will seriously increase the junction temperature. For instance, since I_{C2} equals 3 mA (the minimum corresponds to the highest T_J), the device would dissipate 370 x 3 m = 1.11 W.

Thanks to the dual level startup, the current source deliver I_{C1} = 300 μA if V_{cc} is below 0.70 V. Thus, in case of short-circuit between V_{CC} and GND, the power dissipation will drop to 370 x 300u = 111 mW.

VIII. Brown Out

The C and D versions of DAP013 feature a Brown Out pin (BO) which protects the power supply against low input voltage conditions (Figure 21). This pin permanently monitors a fraction of the bulk voltage through a voltage divider. When this image of bulk voltage is below the BO threshold, the controller stops switching. When the bulk voltage comes back within safe limits, the circuit goes through a new startup sequence including soft-start and re-starts switching (Figure 24). The hysteresis on brown-out pin is implemented with a low side current source sinking 10 μA when the brown-out comparator is low (V_{bulk} < $V_{bulk(ON)}$). This offers adequate precision at shutdown.

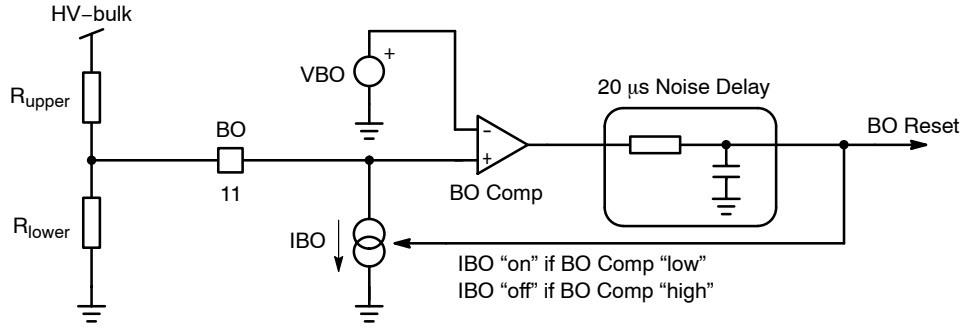

Figure 21. Brown-Out Circuit

1. Calculating the BO Resistors

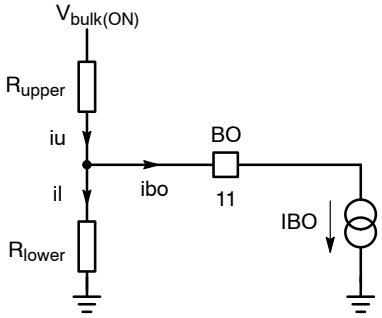

Figure 22. Brown-out Equivalent Schematic at Startup

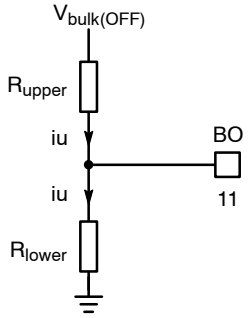

Figure 23. Brown-out at Shutdown

First of all, select the bulk voltage value at which the controller must start switching ($V_{bulk(ON)}$) and the bulk voltage for shutdown ($V_{bulk(OFF)}$). According to Figure 22, we have:

$$i_u = i_l + I_{BO} \qquad \text{(eq. 32)}$$

Where: I_{BO} is the brown-out hysteresis current.

By replacing i_u and i_l by their values, the previous equation becomes:

$$\frac{V_{bulk(ON)} - V_{BO}}{R_{upper}} = \frac{V_{BO}}{R_{lower}} + I_{BO} \qquad \text{(eq. 33)}$$

When V_{bulk} reaches $V_{bulk(ON)}$, the hysteresis current source is turned OFF. Thus, at shutdown, the BO voltage only depends of $V_{bulk(OFF)}$ and R_{upper}, R_{lower} (Figure 23).

$$V_{BO} = \frac{R_{lower}}{R_{upper} + R_{lower}} V_{bulk(OFF)} \qquad \text{(eq. 34)}$$

Deducing R_{upper} from Equatio 34, we replace R_{upper} by its expression in Equation 33. We obtain:

$$R_{lower} = \frac{V_{BO}(V_{bulk(ON)} - V_{bulk(OFF)})}{I_{BO}(V_{bulk(OFF)} - V_{BO})} \qquad \text{(eq. 35)}$$

$$R_{upper} = \frac{R_{lower}(V_{bulk(OFF)} - V_{BO})}{V_{BO}} \qquad \text{(eq. 36)}$$

Design Example

- V_{BO} = 0.8 V
- I_{BO} = 10 μA
- $V_{bulk(ON)}$ = 120 V
- $V_{bulk(OFF)}$ = 60 V

$$R_{lower} = \frac{V_{BO}(V_{bulk(ON)} - V_{bulk(OFF)})}{I_{BO}(V_{bulk(OFF)} - V_{BO})} = \frac{0.8(120 - 60)}{10\ \mu(60 - 0.8)} = 81.1\ k\Omega \quad \text{(eq. 37)}$$

$$R_{upper} = \frac{R_{lower}(V_{bulk(OFF)} - V_{BO})}{V_{BO}} = \frac{81.1\ k \times (60 - 0.8)}{0.8} = 6\ M\Omega \quad \text{(eq. 38)}$$

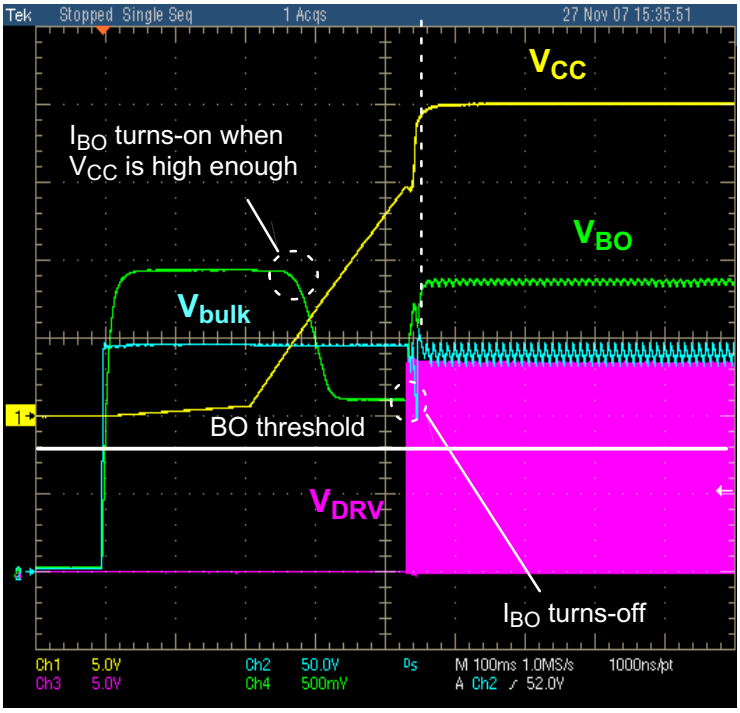

Figure 24. BO at Startup. The Controller Starts Pulsing if V_{BO} > BO Threshold and V_{CC} > V_{CCon}

IX. Over Voltage Protection

The DAP013 also provides a protection against an over voltage condition (OVP), e.g. in case of the optocoupler destruction (Figure 25).

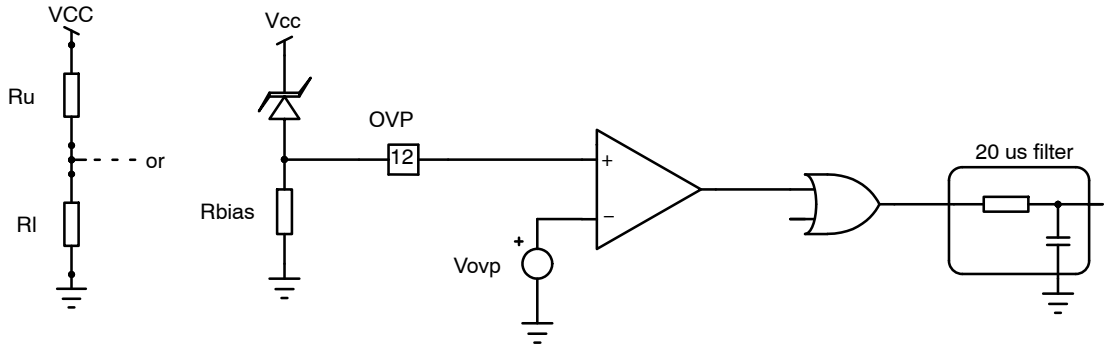

Figure 25. OVP Circuit

The OVP pin (12) is connected to an internal comparator that will latch the controller if a voltage higher than 3 V is applied on this pin. Once the controller is latched, the user must unplug the power supply to allow V_{CC} falling below $V_{CCreset}$ (around 5 V) to reset the controller.

As pin 12 is high impedance, the over voltage protection can be implemented also by using a resistor divider instead of the traditional zener diode.

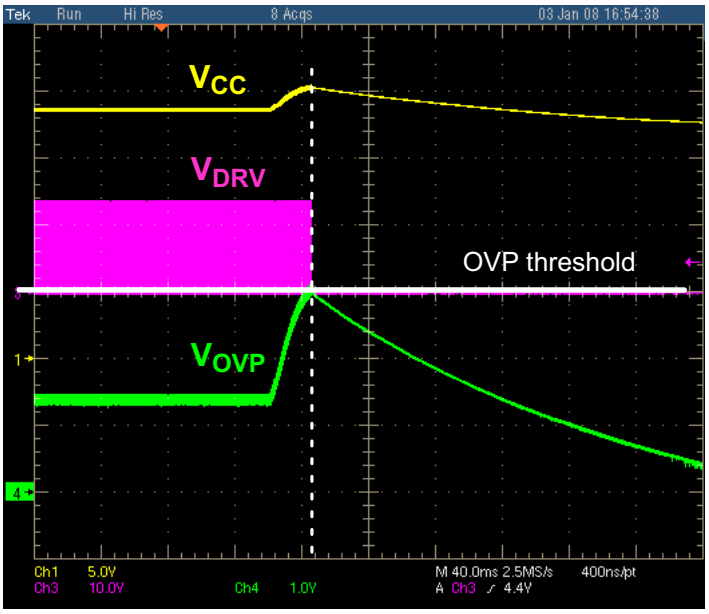

Figure 26. Scope Shot of an Over voltage Event. Here, the OVP was Implemented with an 18 V Zener Diode

X. Typical Application Schematic

The schematic in Figure 27 shows the implementation of DAP013 inside a 19 V/60 W power supply.

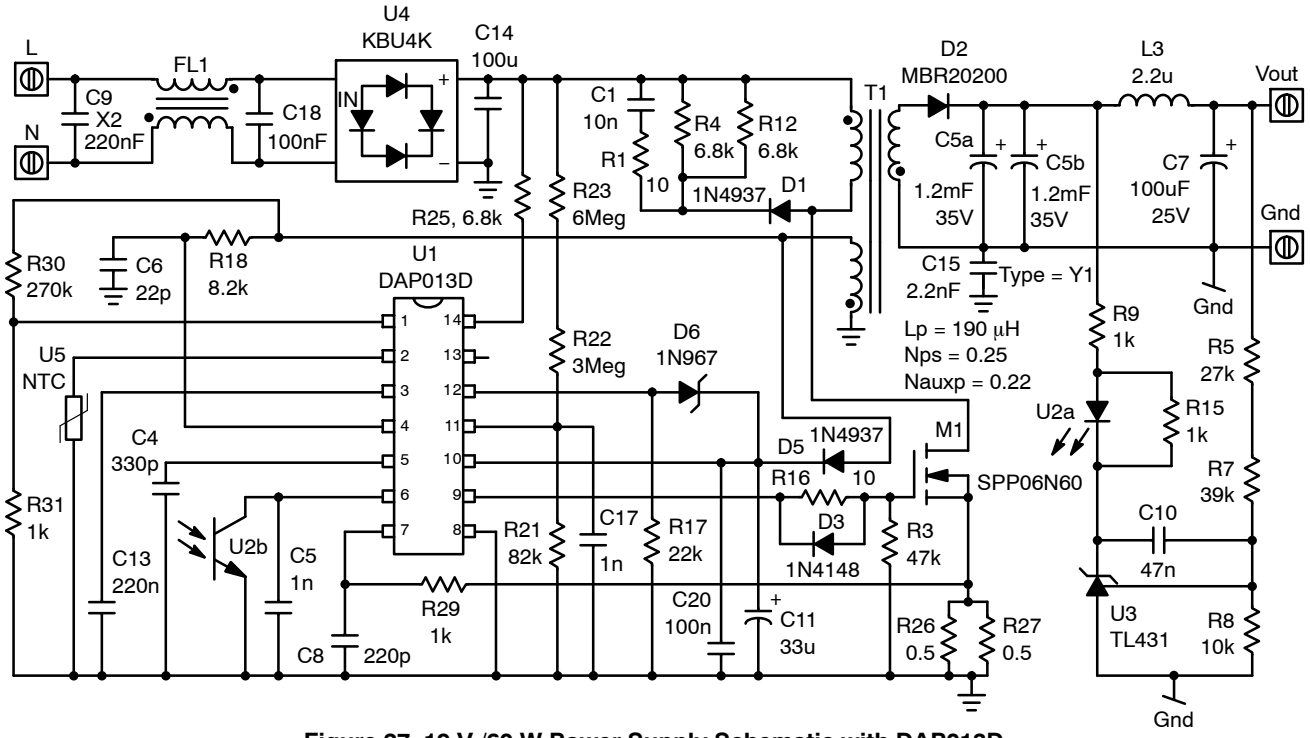

Figure 27. 19 V /60 W Power Supply Schematic with DAP013D

Conclusion

The DAP013 contains all the features (OPP, OVP, OTP, short-circuit protection, BO...) to build high performance ac-dc power supplies.

This controller associate a quasi-resonant operation mode for high output loads with a VCO mode to improve the efficiency of the power supply at light loads.

This application note has described in detail how to select the components surrounding the DAP013.

PUBLICATION ORDERING INFORMATION

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