

# Compal Confidential

## QIWG5/QIWG6 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

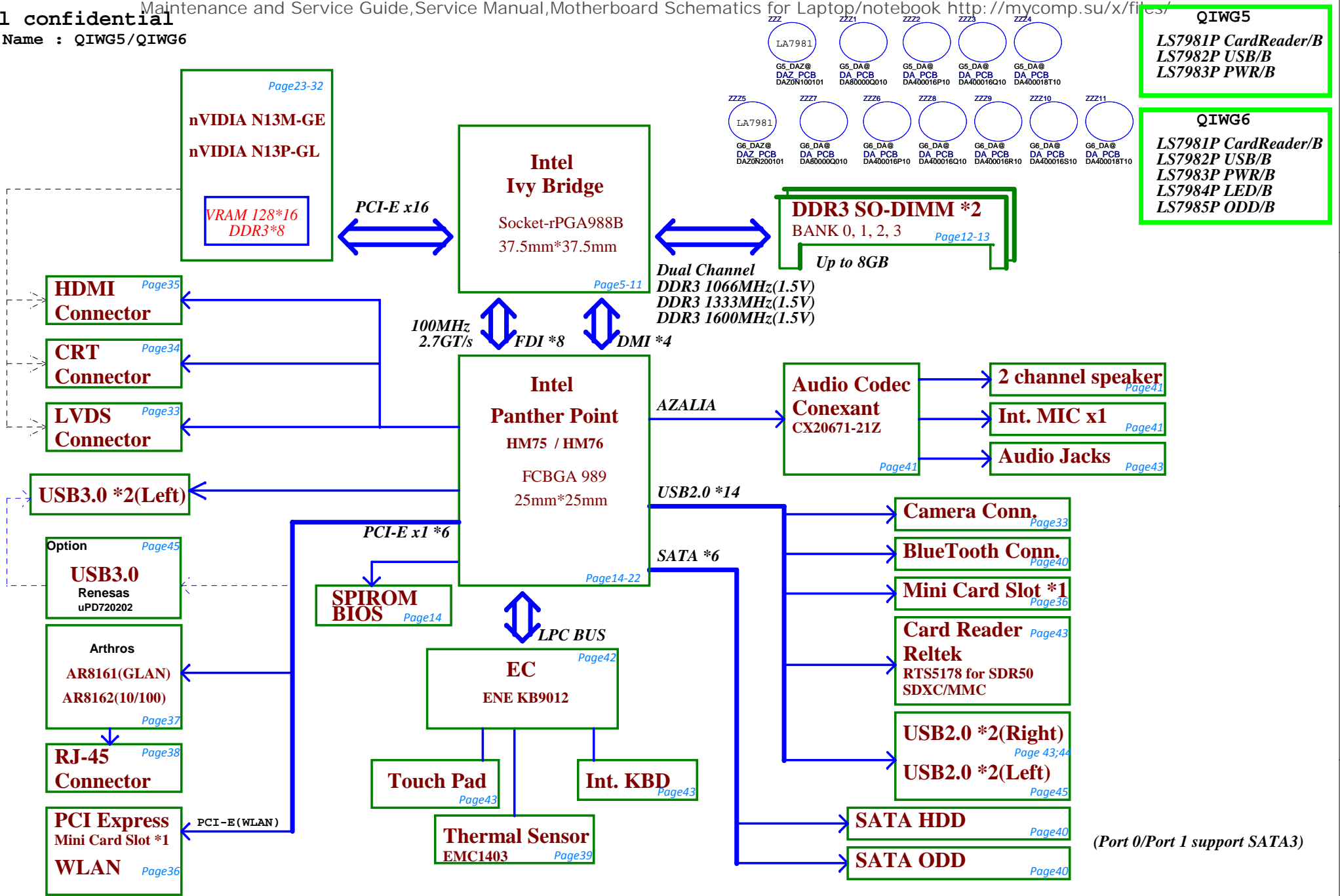
nVIDIA N13X

2012-02-01

LA-7981P

REV:1.0

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**QIWG5**  
LS7981P CardReader/B  
LS7982P USB/B  
LS7983P PWR/B

**QIWG6**  
LS7981P CardReader/B  
LS7982P USB/B  
LS7983P PWR/B  
LS7984P LED/B  
LS7985P ODD/B

(Port 0/Port 1 support SATA3)

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### Voltage Rails

power plane	+B	+5VALW	+1.5V	+3VS	+1.5VS	+V1.05S_VCCP	+VCC_CORE	+VGA_CORE	+VCC_GFXCORE_AXG
		+3VALW		+1.8VS	+0.75VS	+1.05VS			
State									
S0	○	○	○	○					
S3	○	○	○	○	X				
S5 S4/AC	○	○	X	X	X				
S5 S4/ Battery only	○	X	X	X	X				
S5 S4/AC & Battery don't exist	X	X	X	X	X				

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	CLock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%	Board ID / SKU ID Table for AD channel						
Ra/Rc/Re	100K +/- 5%	Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Project	Phase
		0	0	0 V	0 V	0 V	G-series	MP
		1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
		2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
		3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
		4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
		5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
		6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
		7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

### USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB Port (Right Side CR-BD)
		2	USB Port (Left Side) USB3.0
	UHCI1	3	USB Port (Left Side) USB3.0
		4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	USB/B (Right Side USB-BD)
		10	Mini Card(WLAN)
		11	Card Reader
		12	
UHCI6	13	Blue Tooth	

### BOM Structure Table

BTO Item	BOM Structure
GPU:N13P-GL	N13P@
GPU:N13M-GE	N13M@
HDMI	HDMI@
Interna-Intel-USB3.0	IU3@
External-NEC-USB3.0	EU3@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8162@
GIGA LAN	GIGA@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
Camera	CMOS@
For QIWG5 (14")	14@
For QIWG6 (15")	15@
Unpop	@
G5/G6/G9(Low/Mid END)	nonBBH@
G9 High-END	BBH@
G9	G9 @
G5/G6/G9(Low/Mid END)	15_nonBBH@

### EC SM Bus1 address

### EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011Xb	Thermal Sensor F75303M	1001_101xb

### PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

### NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

### SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	√	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	√
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	√	√	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SMLCLK	PCH	X	X	X	X	X	X	X
SMLDATA	+3VALW							
SML1CLK	PCH	√	X	√	X	X	√	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

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Hot plug detect for IFP link C

VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	

Performance Mode P0 TDP at Tj = 102 C\* (GDDR3)

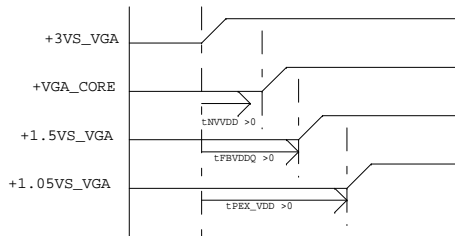
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

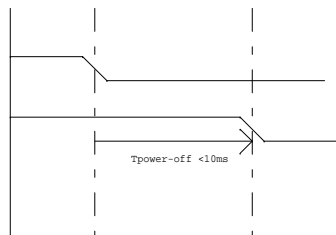
	Device ID
N13P-GL (28nm)	??
N13M-GE (28nm)	???

GPU	FB Memory (GDDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N13P-GL N13M-GE	Samsung 2500MHz	K4G10325FG-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ1H24BFR-T2C						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
	Samsung 2500MHz	K4G20325FG-HC04						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ2H24MFR-T2C						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K

X76



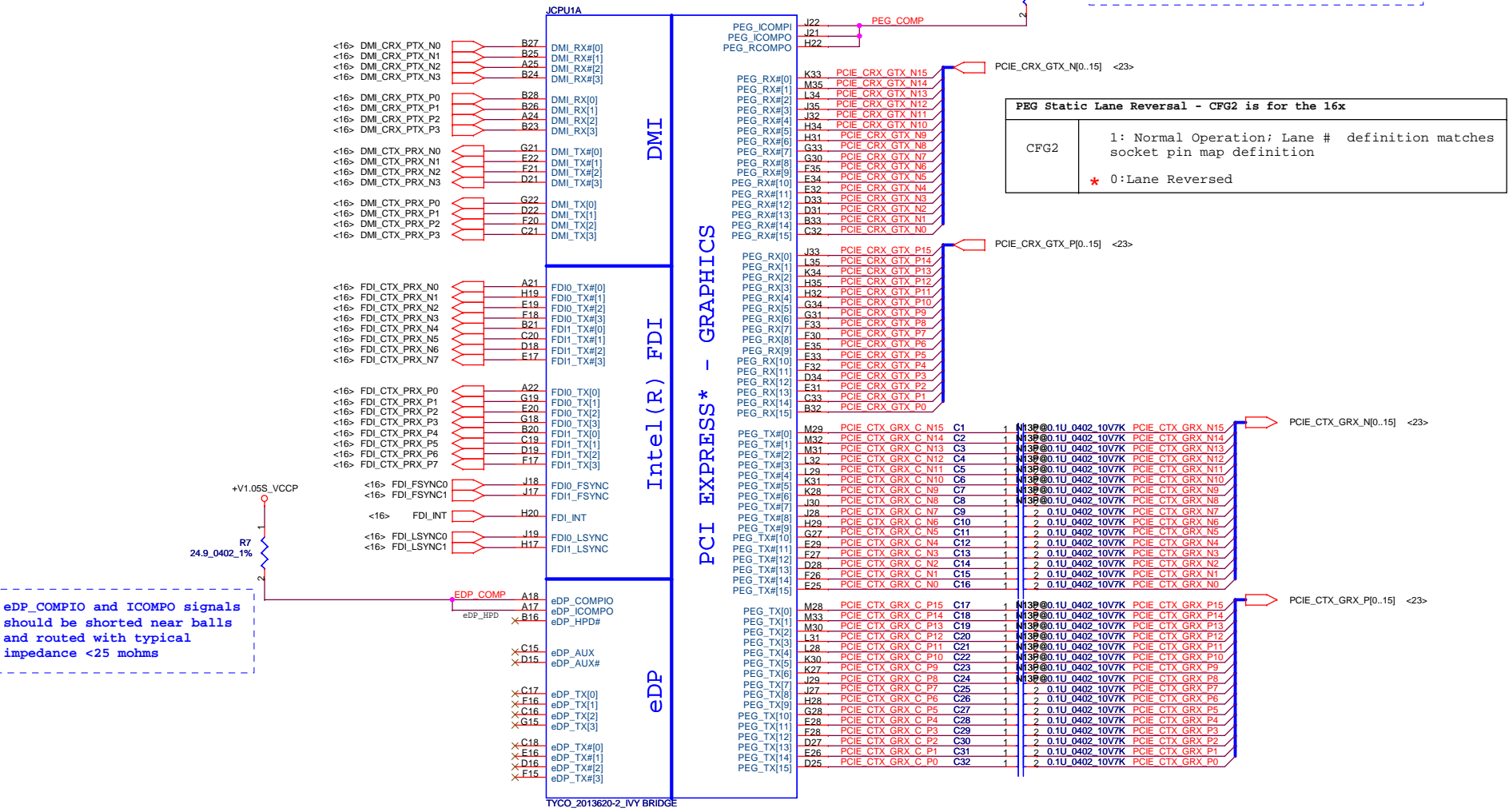
1. all power rail ramp up time should be larger than 40us
2. Optimus system VDDb33 avoids drop down earlier than NVDD and FBVDDQ



1. all GPU power rails should be turned off within 10ms

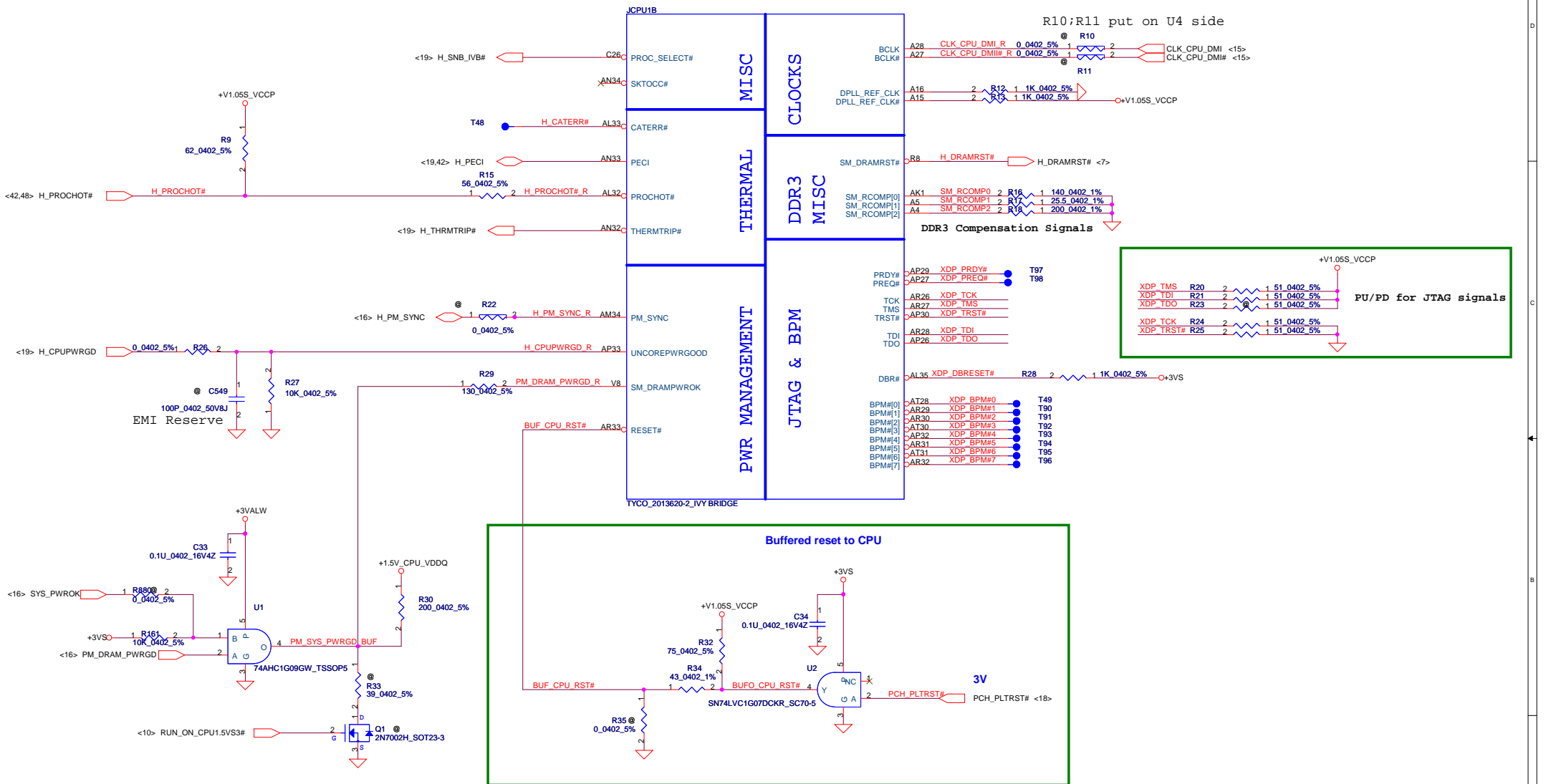
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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

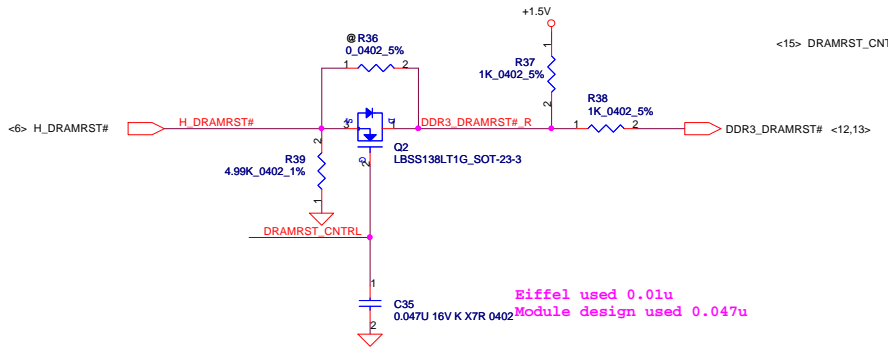
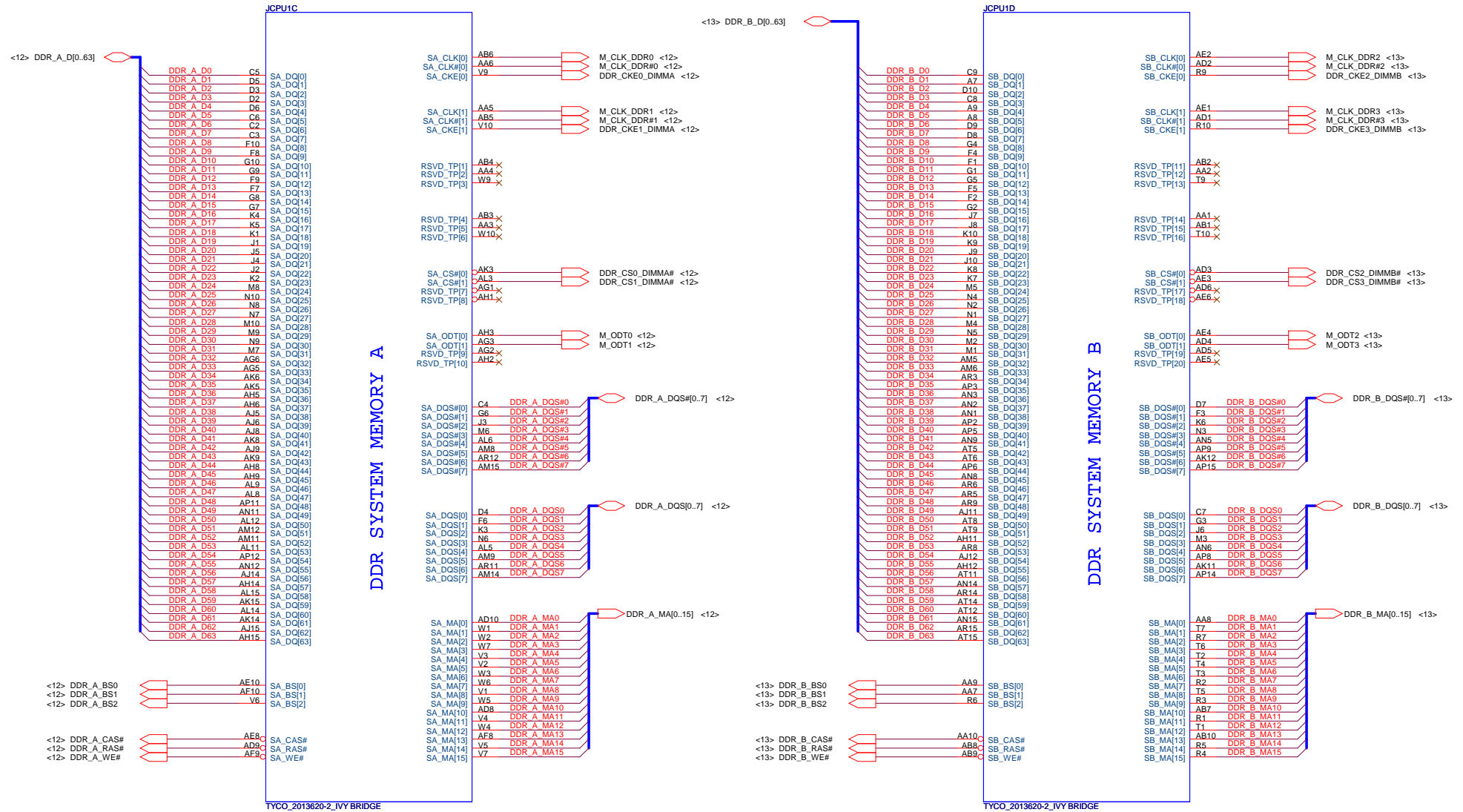
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	PROCESSOR(1/7) DMI,FDI,PEG	
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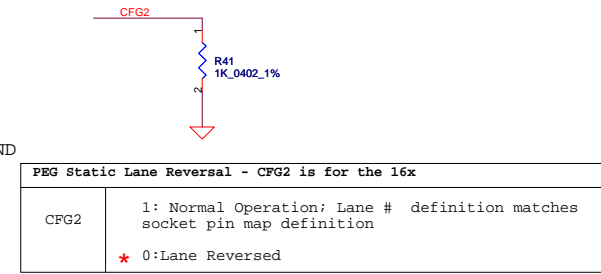
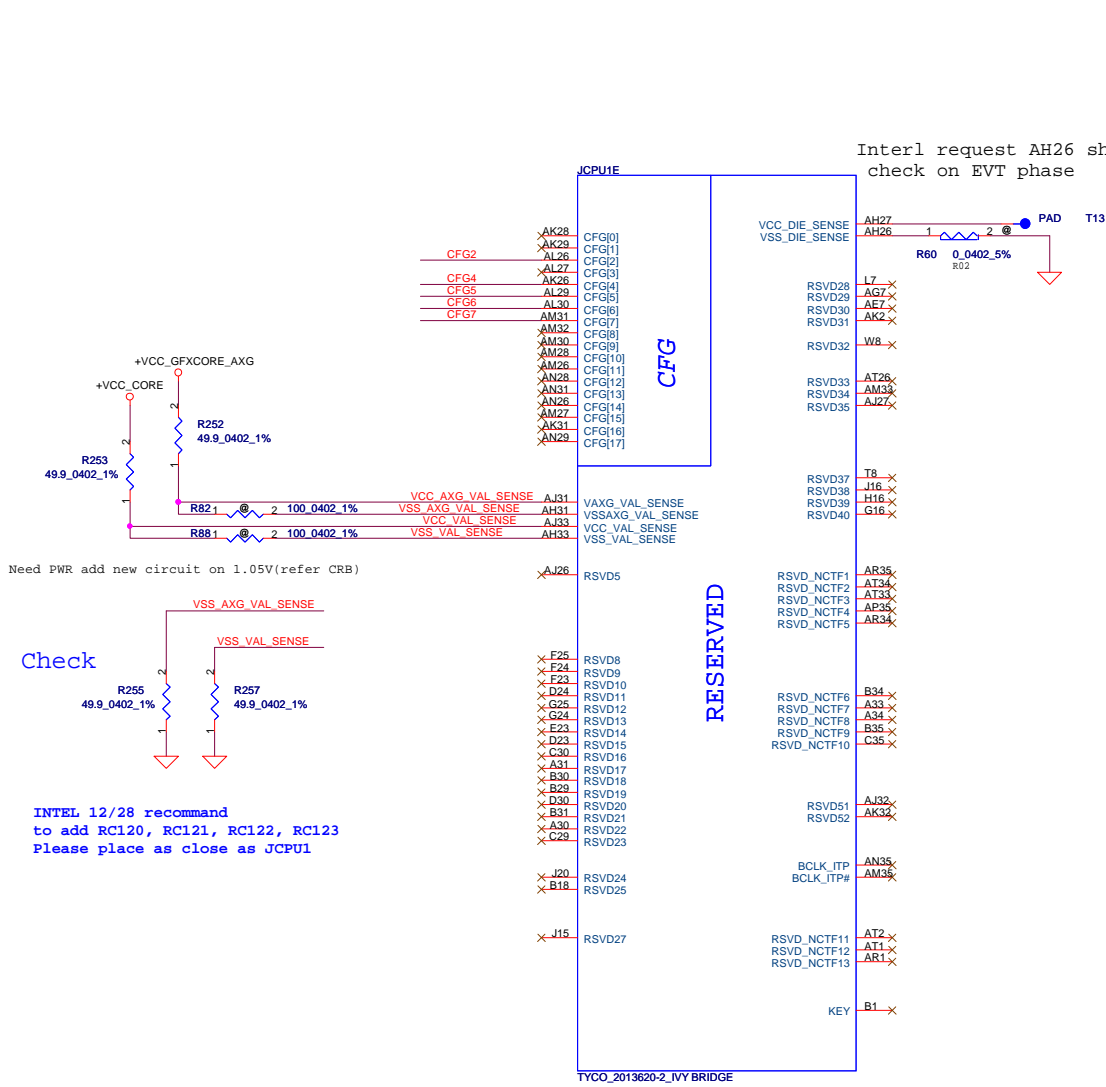
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Compal Electronics, Inc.			
Title <b>PROCESSOR(2/7) PM,XDP,CLK</b>			
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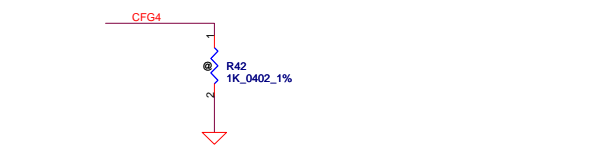


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	<b>PROCESSOR(3/7) DDRIII</b>
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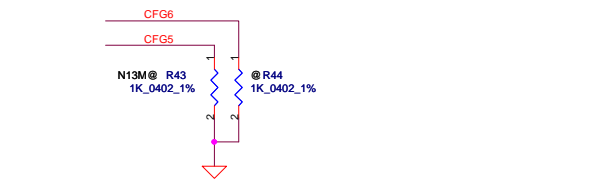
### CFG Straps for Processor



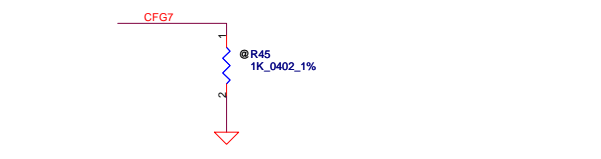
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



# POWER

+VCC\_CORE  
**QC=94A**  
**DC=53A**

JCPU1F

+V1.05S\_VCCP  
**8.5A**

## CORE SUPPLY

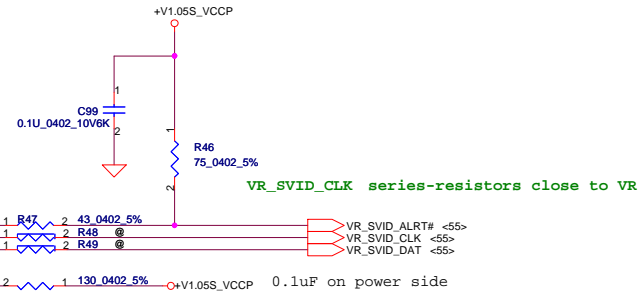
## PEG AND DDR

## SVID

## SENSE LINES

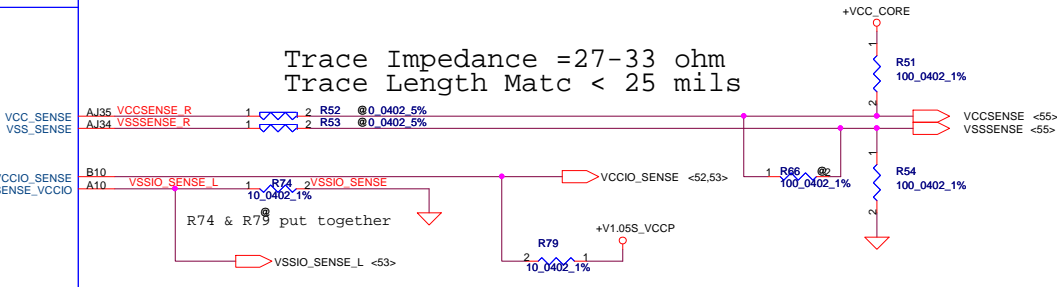
- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AD35 VCC20
- AD34 VCC21
- AD33 VCC22
- AD32 VCC23
- AD31 VCC24
- AD30 VCC25
- AD29 VCC26
- AD28 VCC27
- AD27 VCC28
- AD26 VCC29
- AC35 VCC30
- AC34 VCC31
- AC33 VCC32
- AC32 VCC33
- AC31 VCC34
- AC30 VCC35
- AC29 VCC36
- AC28 VCC37
- AC27 VCC38
- AC26 VCC39
- AA35 VCC40
- AA34 VCC41
- AA33 VCC42
- AA32 VCC43
- AA31 VCC44
- AA30 VCC45
- AA29 VCC46
- AA28 VCC47
- AA27 VCC48
- AA26 VCC49
- Y35 VCC50
- Y34 VCC51
- Y33 VCC52
- Y32 VCC53
- Y31 VCC54
- Y30 VCC55
- Y29 VCC56
- Y28 VCC57
- Y27 VCC58
- Y26 VCC59
- V35 VCC60
- V34 VCC61
- V33 VCC62
- V32 VCC63
- V31 VCC64
- V30 VCC65
- V29 VCC66
- V28 VCC67
- V27 VCC68
- V26 VCC69
- V25 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

- VCCIO1 AH13
- VCCIO2 AH10
- VCCIO3 AG10
- VCCIO4 AC10
- VCCIO5 Y10
- VCCIO6 L10
- VCCIO7 P10
- VCCIO8 L10
- VCCIO9 J14
- VCCIO10 J13
- VCCIO11 J12
- VCCIO12 J11
- VCCIO13 H14
- VCCIO14 H12
- VCCIO15 H11
- VCCIO16 G14
- VCCIO17 G13
- VCCIO18 G12
- VCCIO19 F14
- VCCIO20 F13
- VCCIO21 F12
- VCCIO22 F11
- VCCIO23 E14
- VCCIO24 E12
- VCCIO25 E11
- VCCIO26 D14
- VCCIO27 D13
- VCCIO28 D12
- VCCIO29 D11
- VCCIO30 C14
- VCCIO31 C13
- VCCIO32 C12
- VCCIO33 C11
- VCCIO34 B14
- VCCIO35 B12
- VCCIO36 A14
- VCCIO37 A13
- VCCIO38 A12
- VCCIO39 A11
- VCCIO40 J23



VCC\_SENCE 100ohm +-1% pull-up to VCC near processor

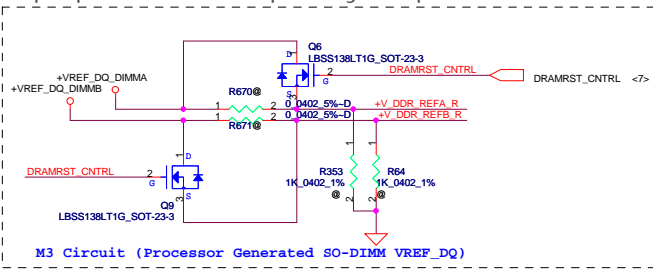
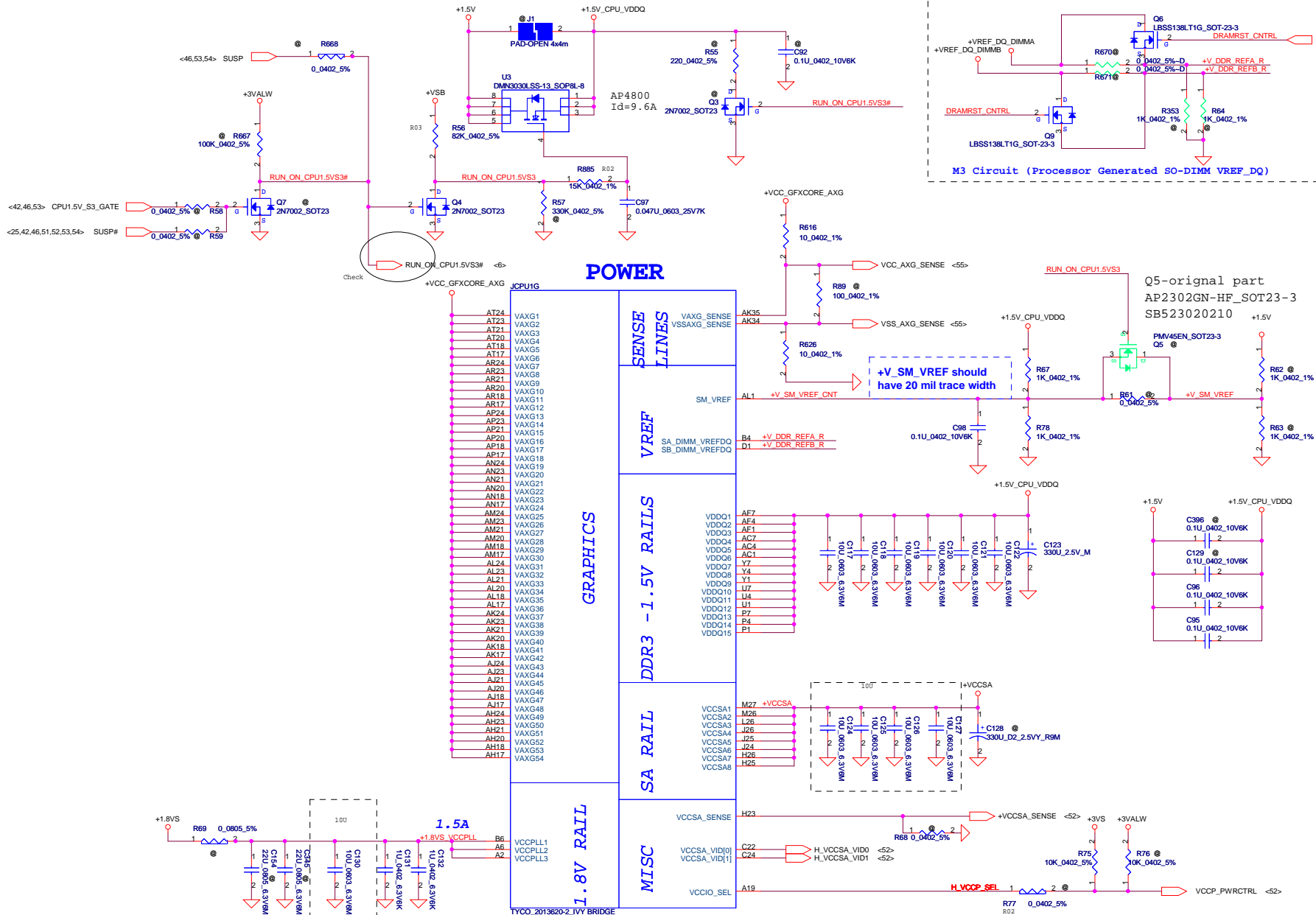
Trace Impedance =27-33 ohm  
 Trace Length Matc < 25 mils



VSS\_SENCE 100ohm +-1% pull-down to GND near processor

TYCO\_2013620-2\_IVY BRIDGE

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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Size	Processor(5/7) PWR,BYPASS
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**POWER**

**GRAPHICS**

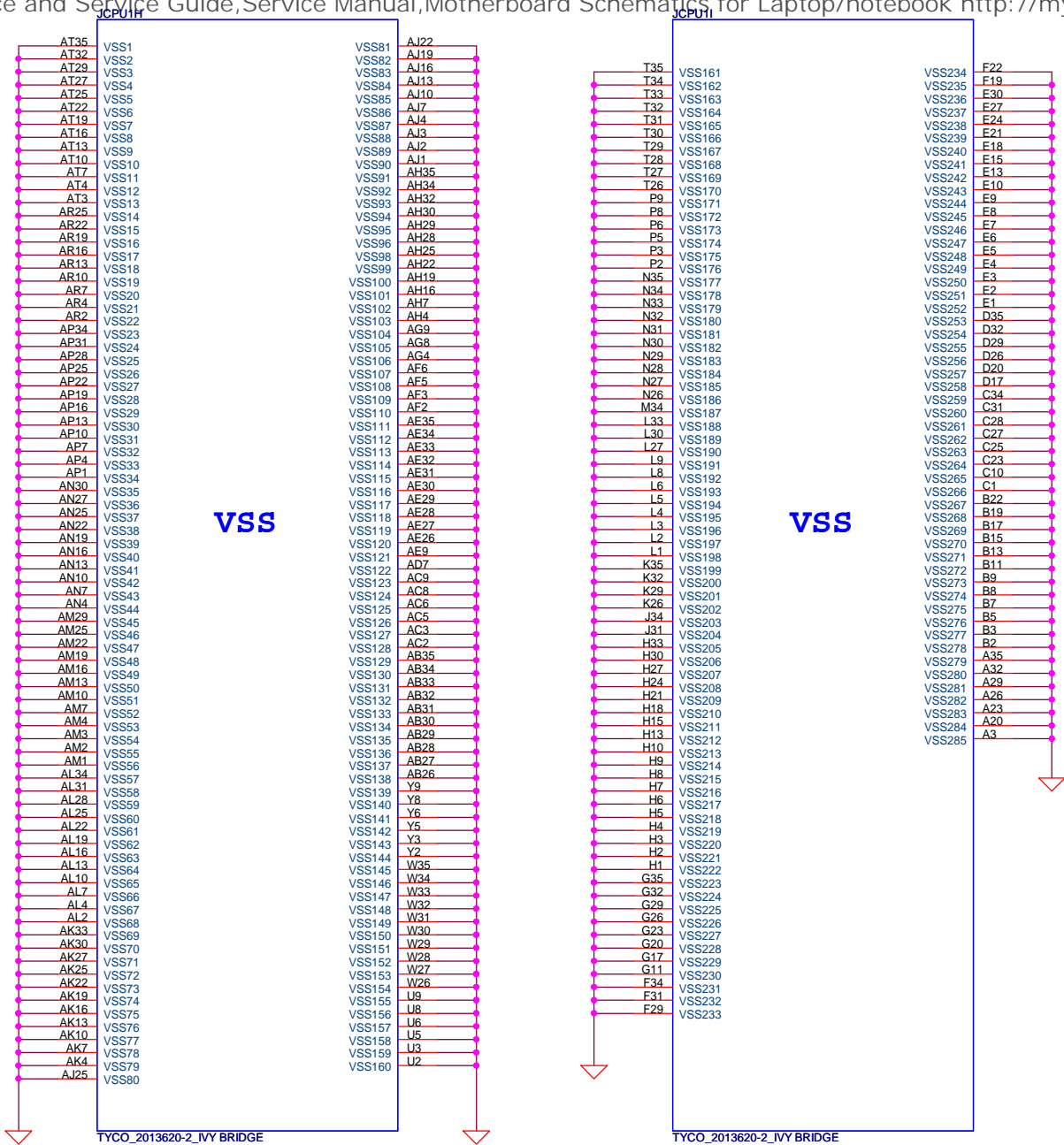
**MISC**

- AT24 VAXG1
- AT23 VAXG2
- AT20 VAXG3
- AT19 VAXG4
- AT18 VAXG5
- AT17 VAXG6
- AR24 VAXG7
- AR23 VAXG8
- AR21 VAXG9
- AR20 VAXG10
- AR18 VAXG11
- AR17 VAXG12
- AP24 VAXG13
- AP23 VAXG14
- AP21 VAXG15
- AP20 VAXG16
- AP18 VAXG17
- AP17 VAXG18
- AN24 VAXG19
- AN23 VAXG20
- AN21 VAXG21
- AN20 VAXG22
- AN18 VAXG23
- AN17 VAXG24
- AM24 VAXG25
- AM23 VAXG26
- AM21 VAXG27
- AM20 VAXG28
- AM18 VAXG29
- AM17 VAXG30
- AL24 VAXG31
- AL23 VAXG32
- AL21 VAXG33
- AL20 VAXG34
- AL18 VAXG35
- AL17 VAXG36
- AK24 VAXG37
- AK23 VAXG38
- AK21 VAXG39
- AK20 VAXG40
- AK18 VAXG41
- AK17 VAXG42
- AJ24 VAXG43
- AJ23 VAXG44
- AJ21 VAXG45
- AJ20 VAXG46
- AH24 VAXG47
- AH23 VAXG48
- AH21 VAXG49
- AH20 VAXG50
- AH18 VAXG51
- AH17 VAXG52
- AH16 VAXG53
- AH15 VAXG54

+V\_SM\_VREF should have 20 mil trace width

IVY Bridge drives VCCIO\_SEL low  
 VCCP\_PWRCTRL:0  
 Sandy Bridge is NC for A19  
 VCCP\_PWRCTRL:1

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Date	Tuesday, February 14, 2012	Sheet	10 of 60

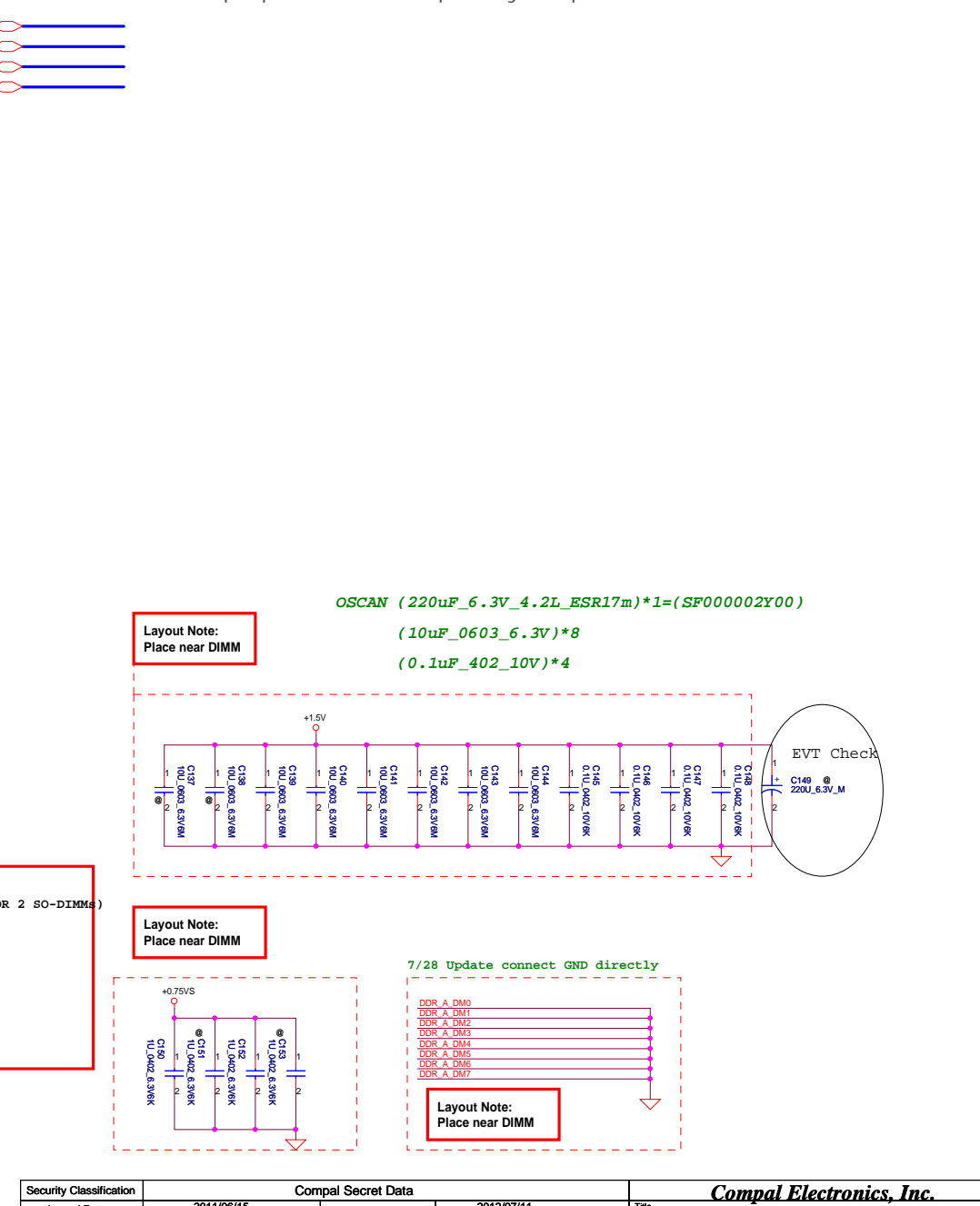
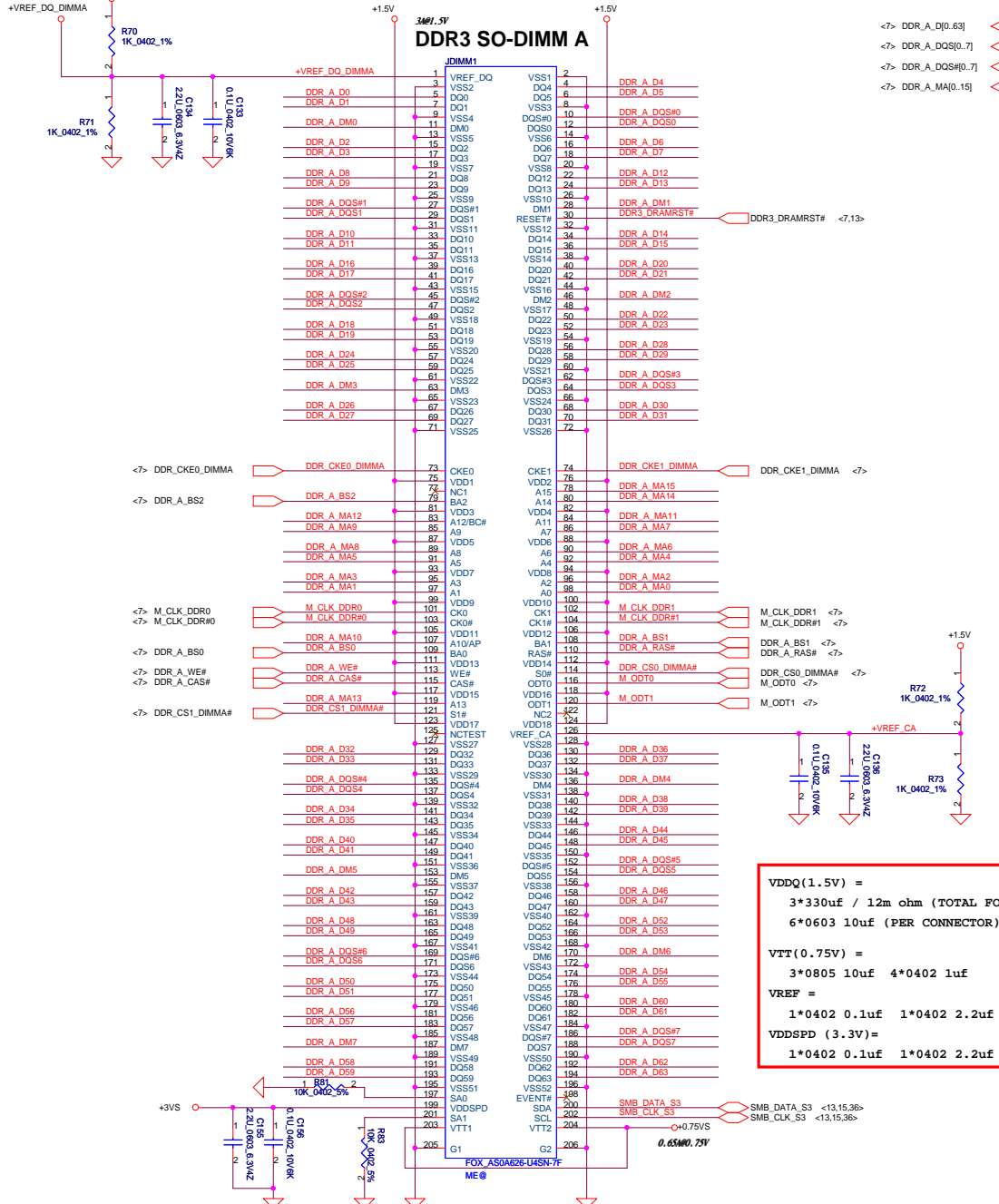


VSS

VSS

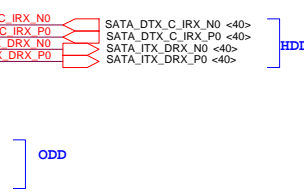
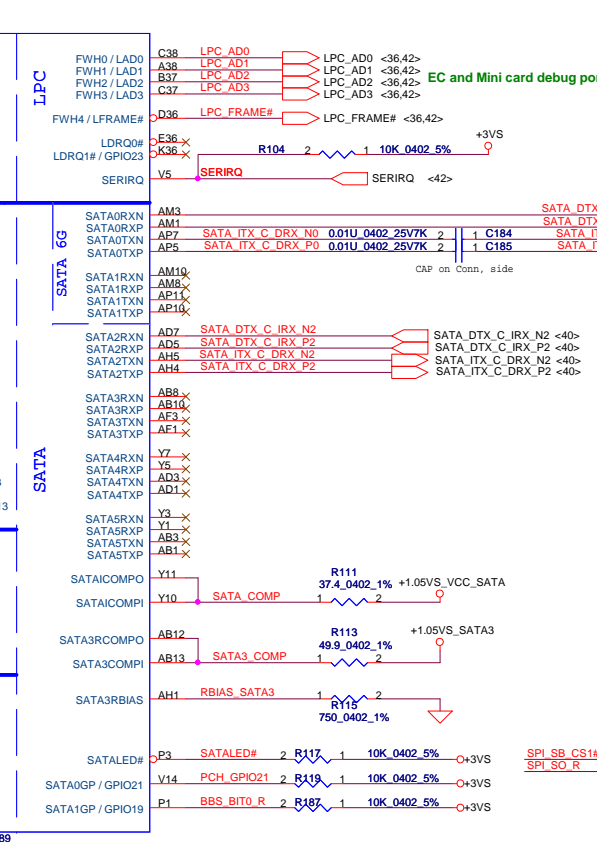
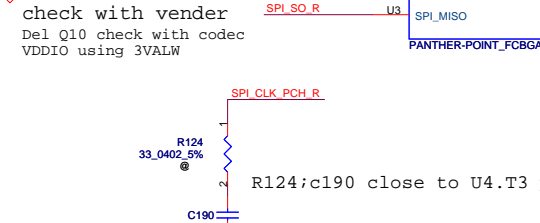
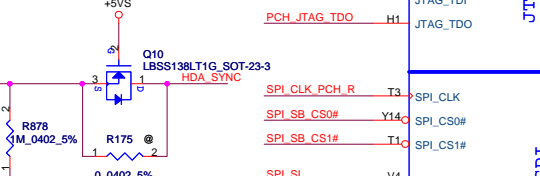
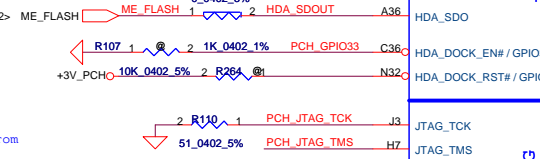
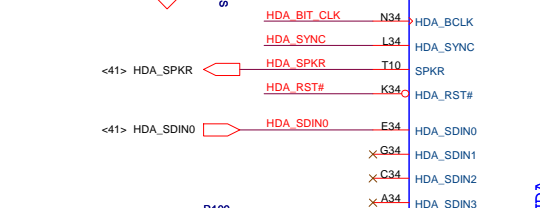
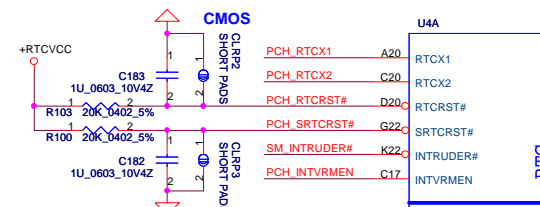
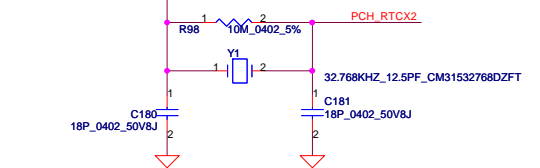
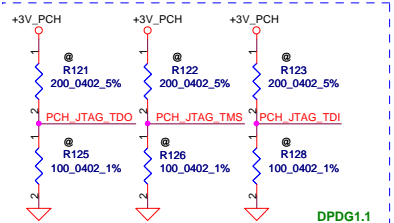
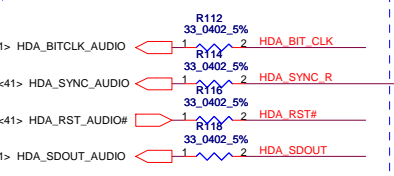
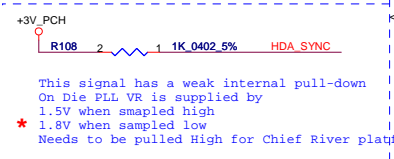
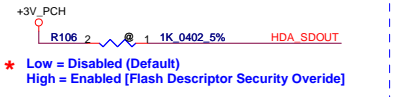
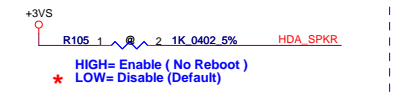
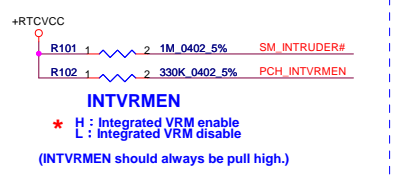
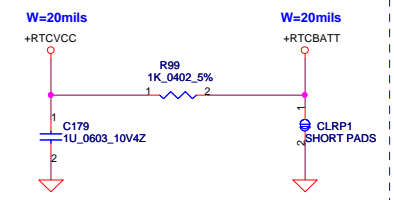
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<b>PROCESSOR(7/7) VSS</b>	
Title	Document Number
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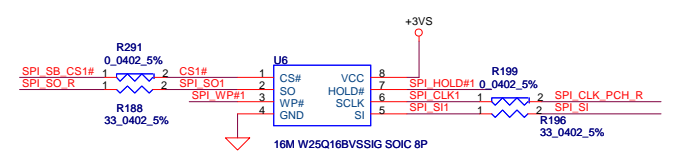


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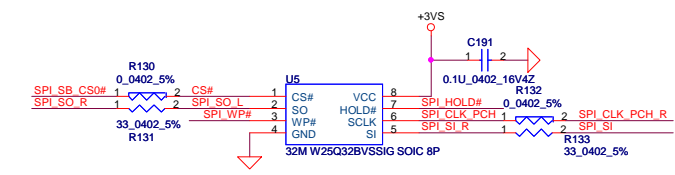




**8MB SPI ROM FOR ME & Non-share ROM.**

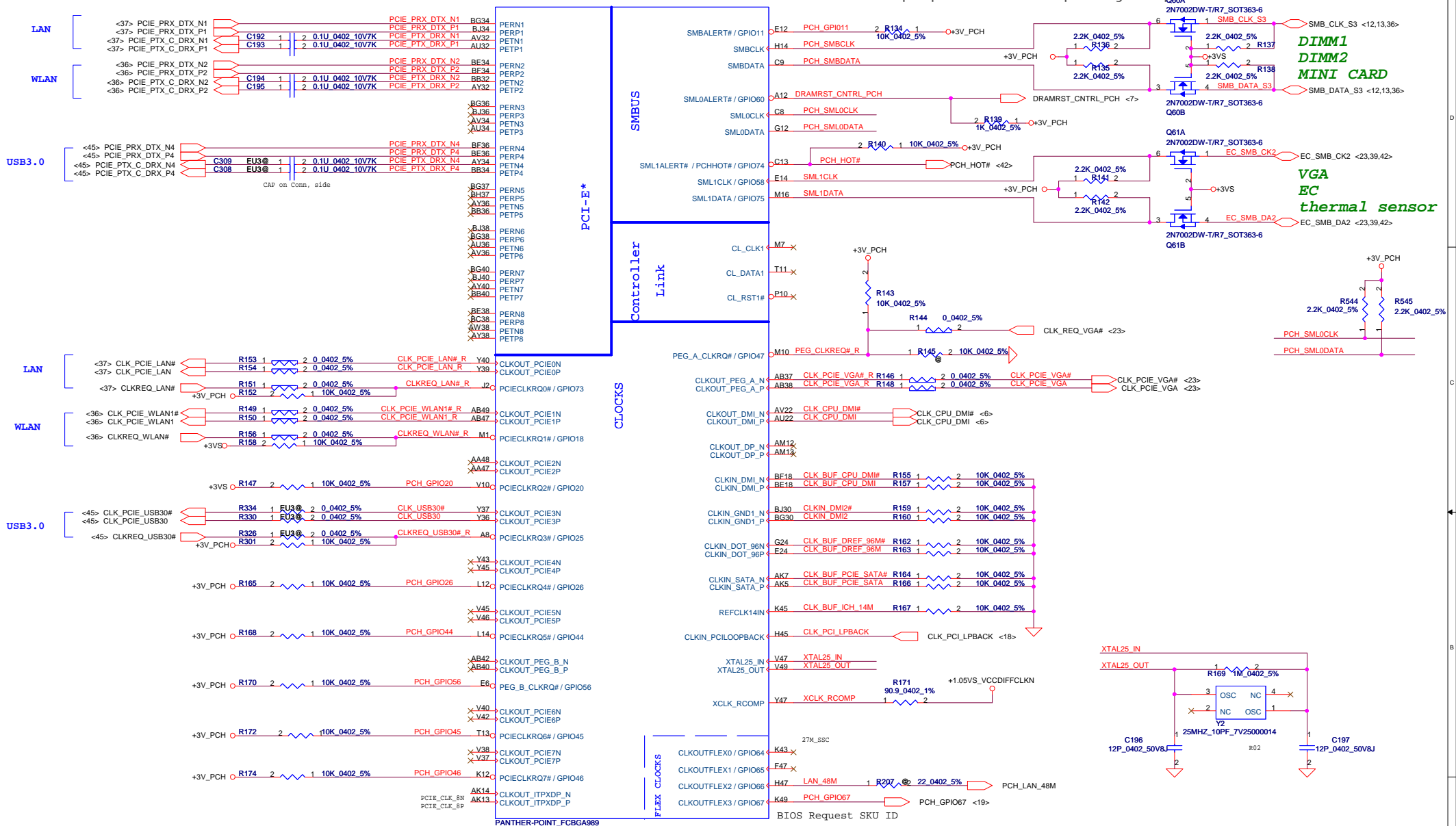


**U6 Rersver 4M+2M Solution**



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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	<b>PCH (I/9) SATA, HDA, SPI, LPC, XDP</b>	
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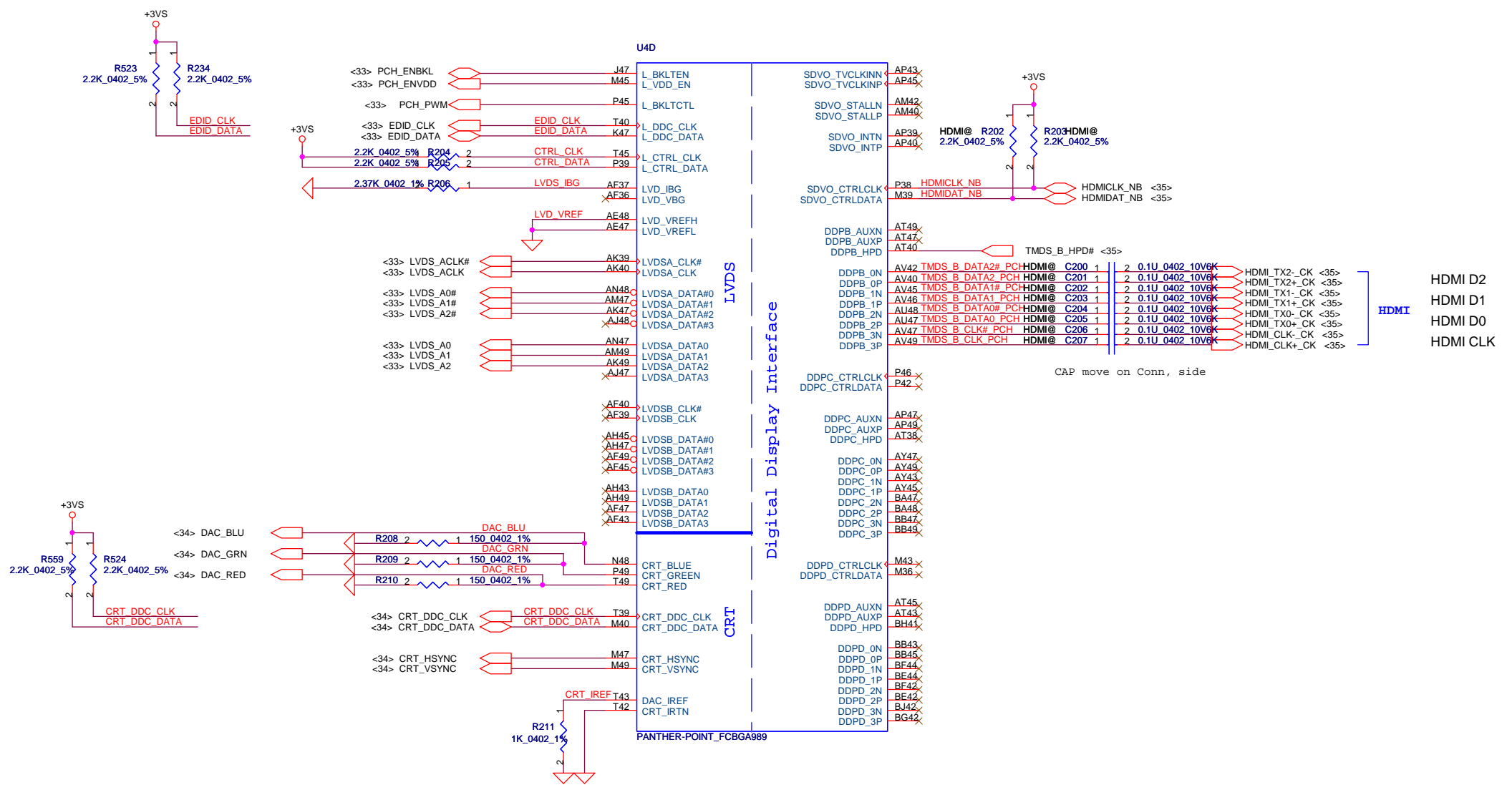
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Issued Date	2011/06/15	Deciphered Date
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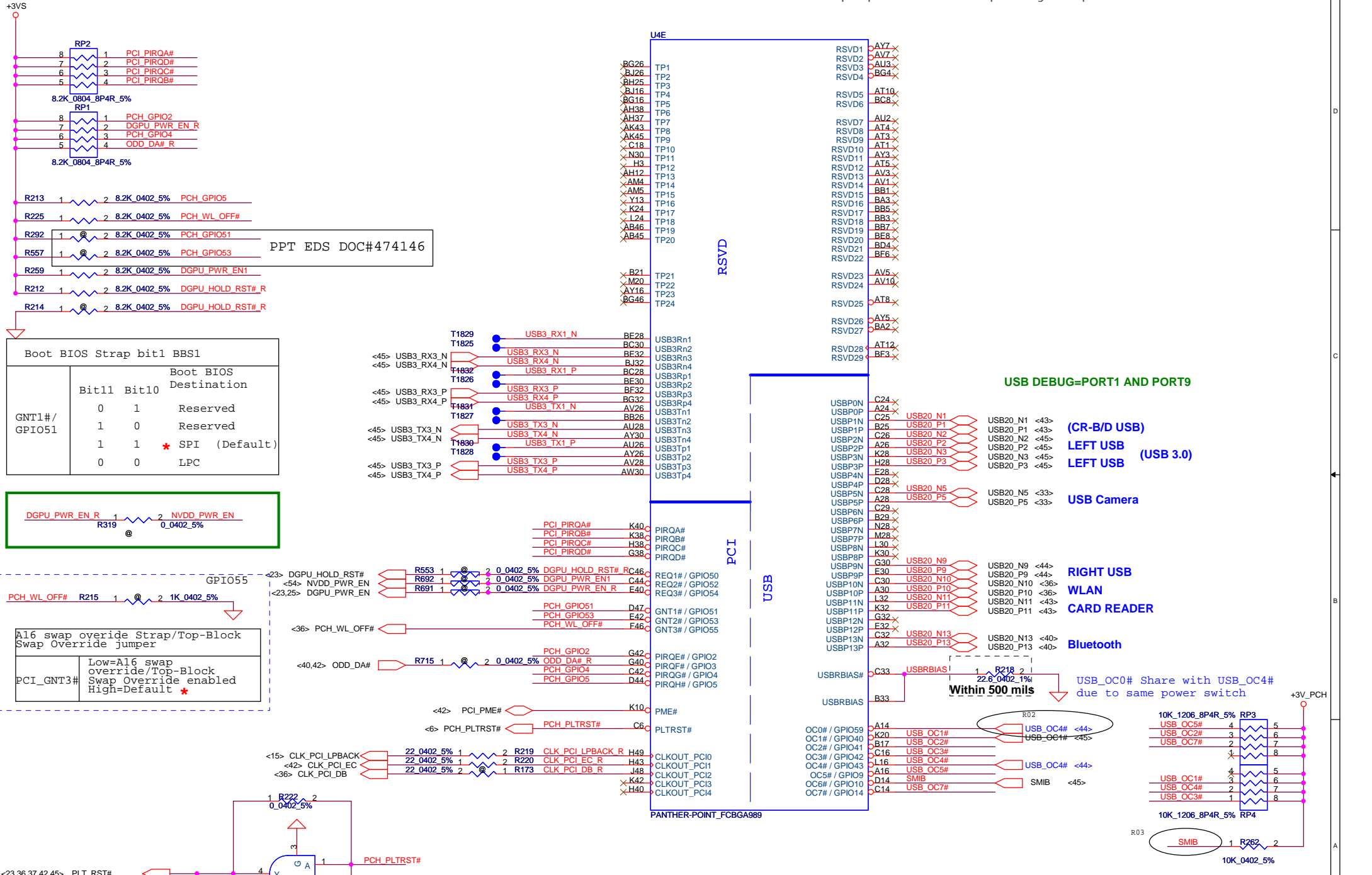
<b>Compal Electronics, Inc.</b>		
<b>PCH (2/9) PCIE, SMBUS, CLK</b>		
Size	Document Number	Rev
Custom	<b>LA-7981P</b>	0.2
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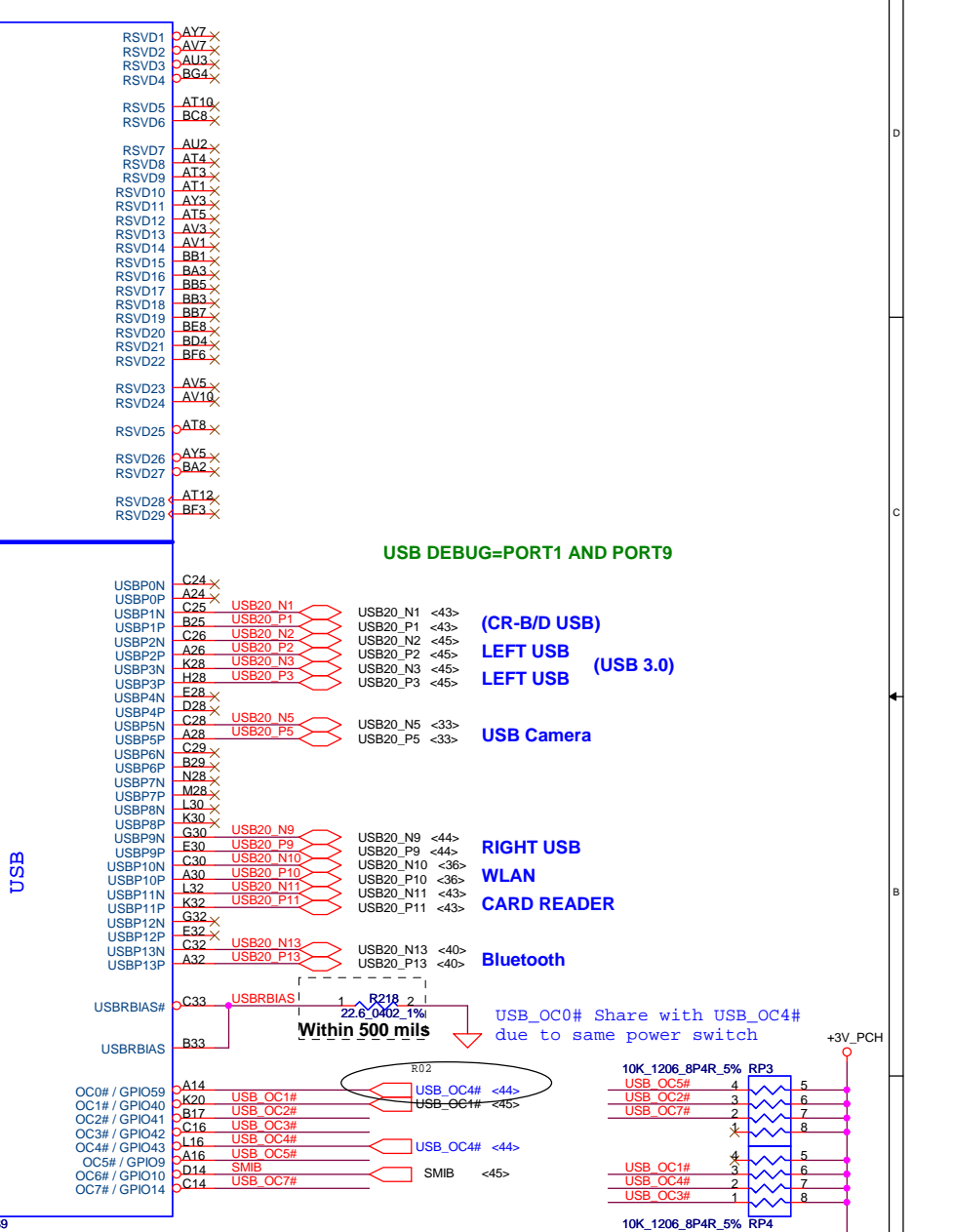
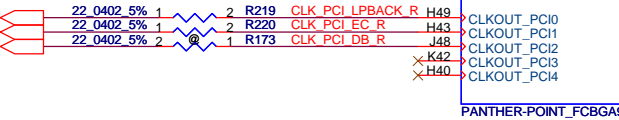
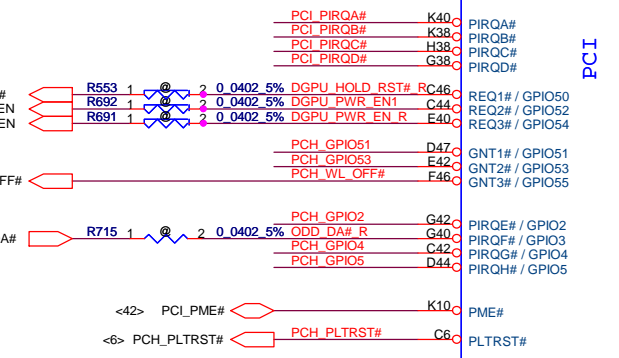
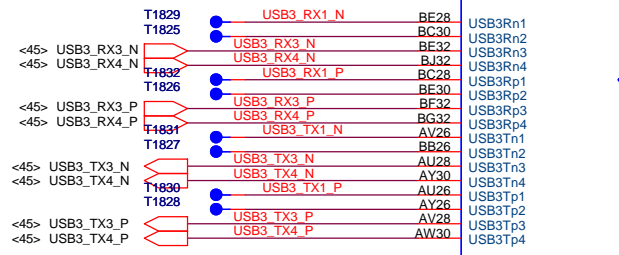
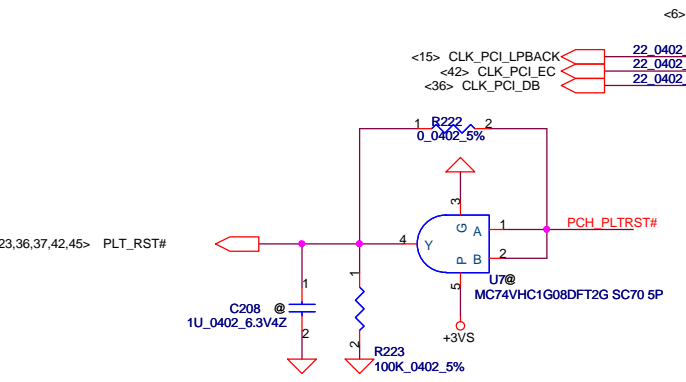
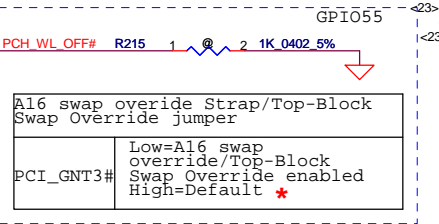
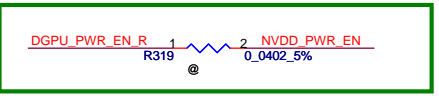


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	PCH (4/9) LVDS,CRT,DP,HDMI	
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Boot BIOS Strap bit1 BBS1

GNT1#/ GPIO51	Bit11	Bit10	Boot BIOS Destination
	0	1	Reserved
	1	0	Reserved
	1	1	* SPI (Default)
	0	0	LPC

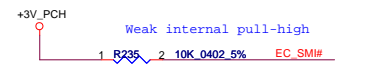


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Title	<b>PCH (5/9) PCI, USB</b>	
Size	Document Number	Rev
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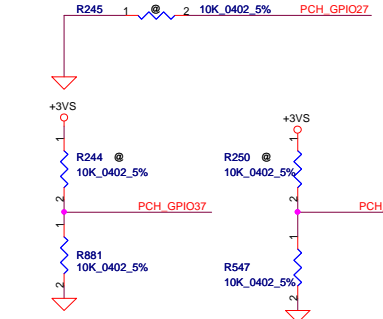
PCH_GPIO69	Function
0	HM76 by PCH
1	HM70 by PCH

PCH_GPIO70	Function
0	14/15"
1	17"
PCH_GPIO71	
0	USB3.0 by PCH
1	USB3.0 by NEC

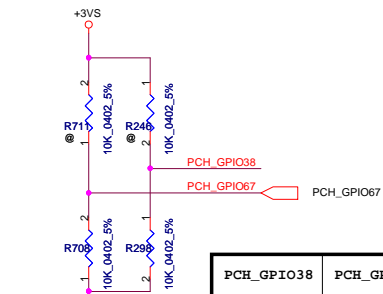


**GPIO28**  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
\* H : On-Die voltage regulator enable  
L : On-Die PLL Voltage Regulator disable

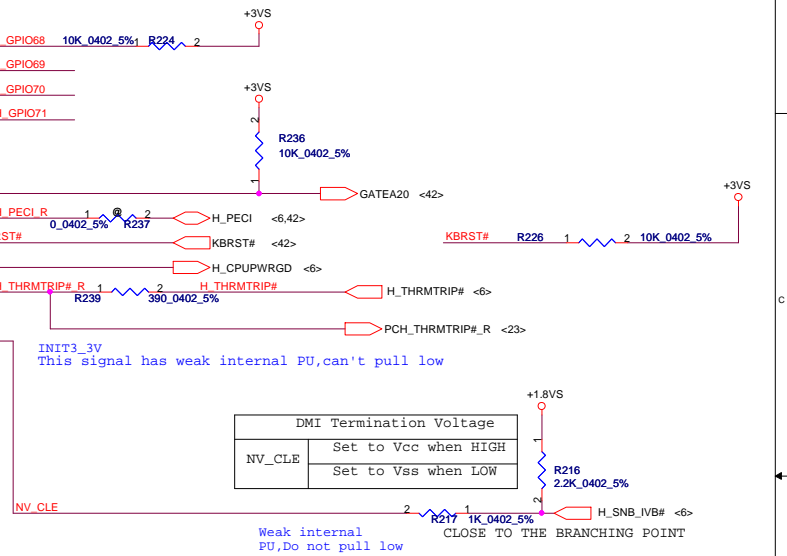
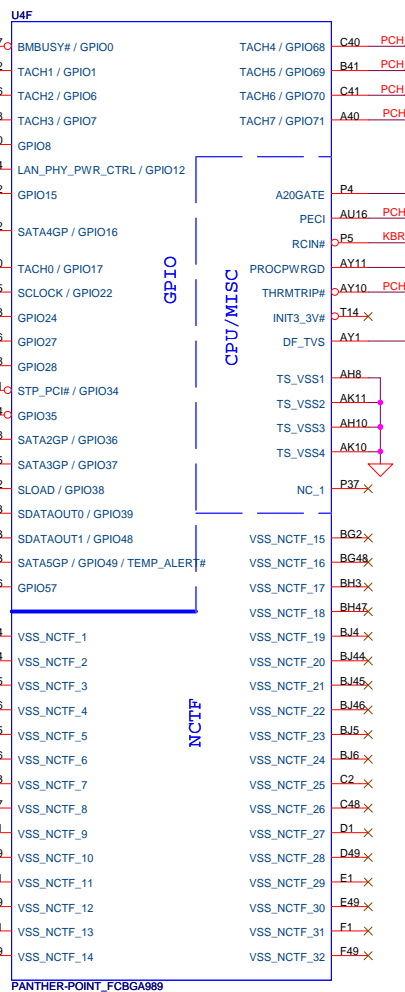
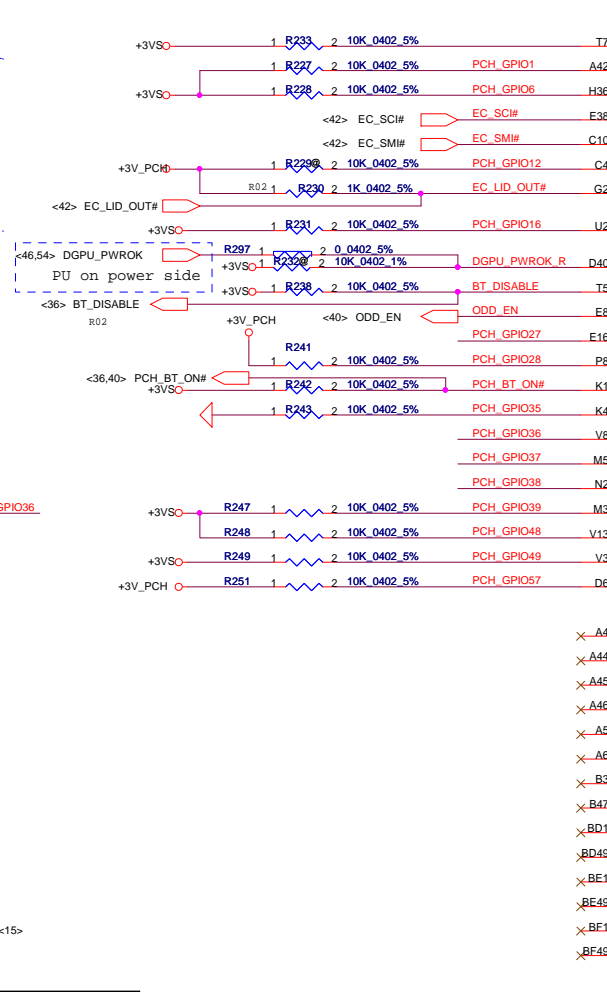
\* **PCH\_GPIO27** (Have internal Pull-High)  
High: VCCVRM VR Enable  
Low: VCCVRM VR Disable



BIOS Request SKU ID



PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA



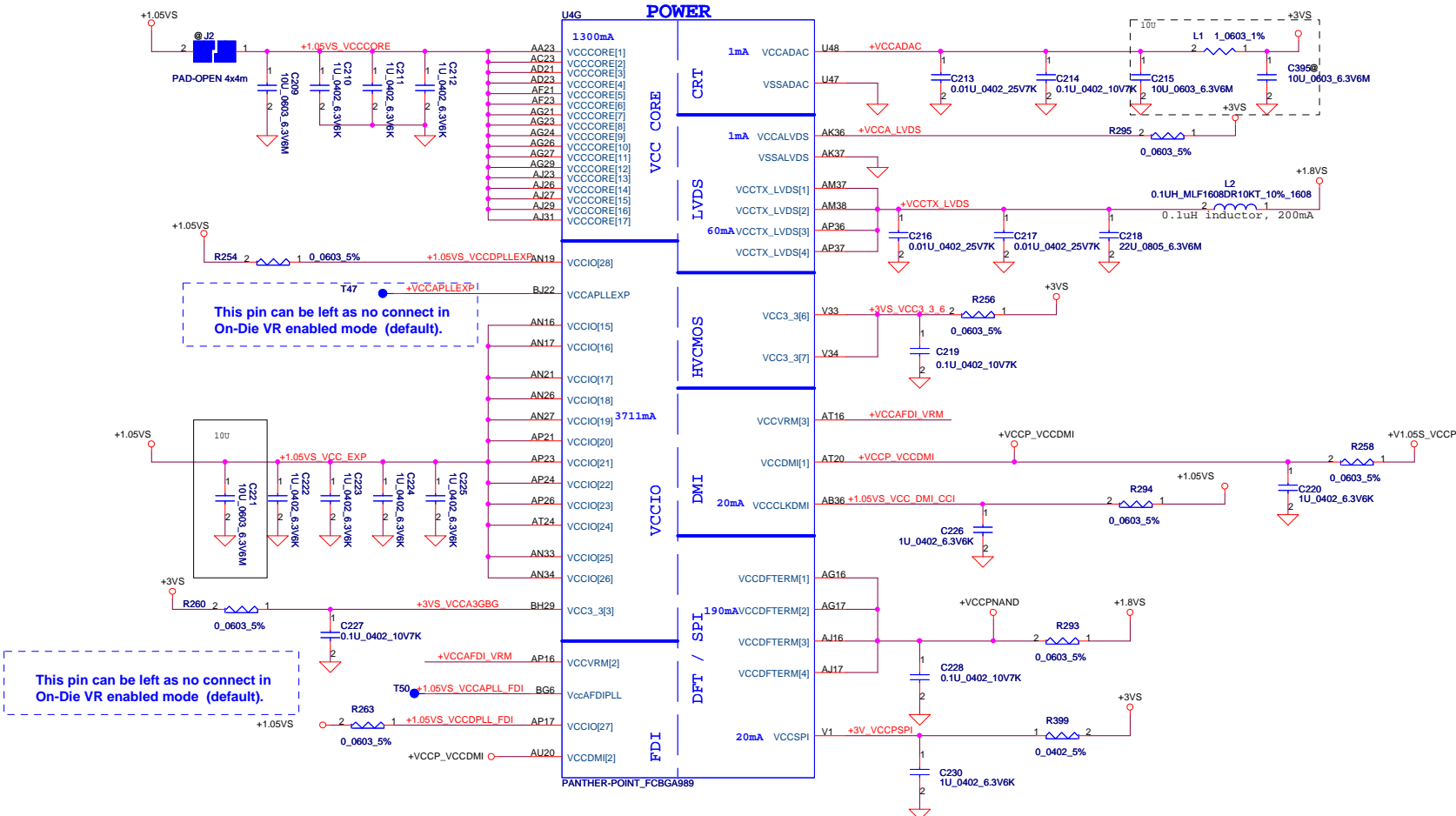
DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
NV_CLE	Set to Vss when LOW

Weak internal PU, Do not pull low  
CLOSE TO THE BRANCHING POINT

<b>Security Classification</b>	Compal Secret Data			<b>Title</b>	<b>PCH (6/9) GPIO, CPU, MISC</b>	
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L1 Change to 1 ohm P/N  
S RES 1/10W 1 +-1% 0603

PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



This pin can be left as no connect in On-Die VR enabled mode (default).

This pin can be left as no connect in On-Die VR enabled mode (default).

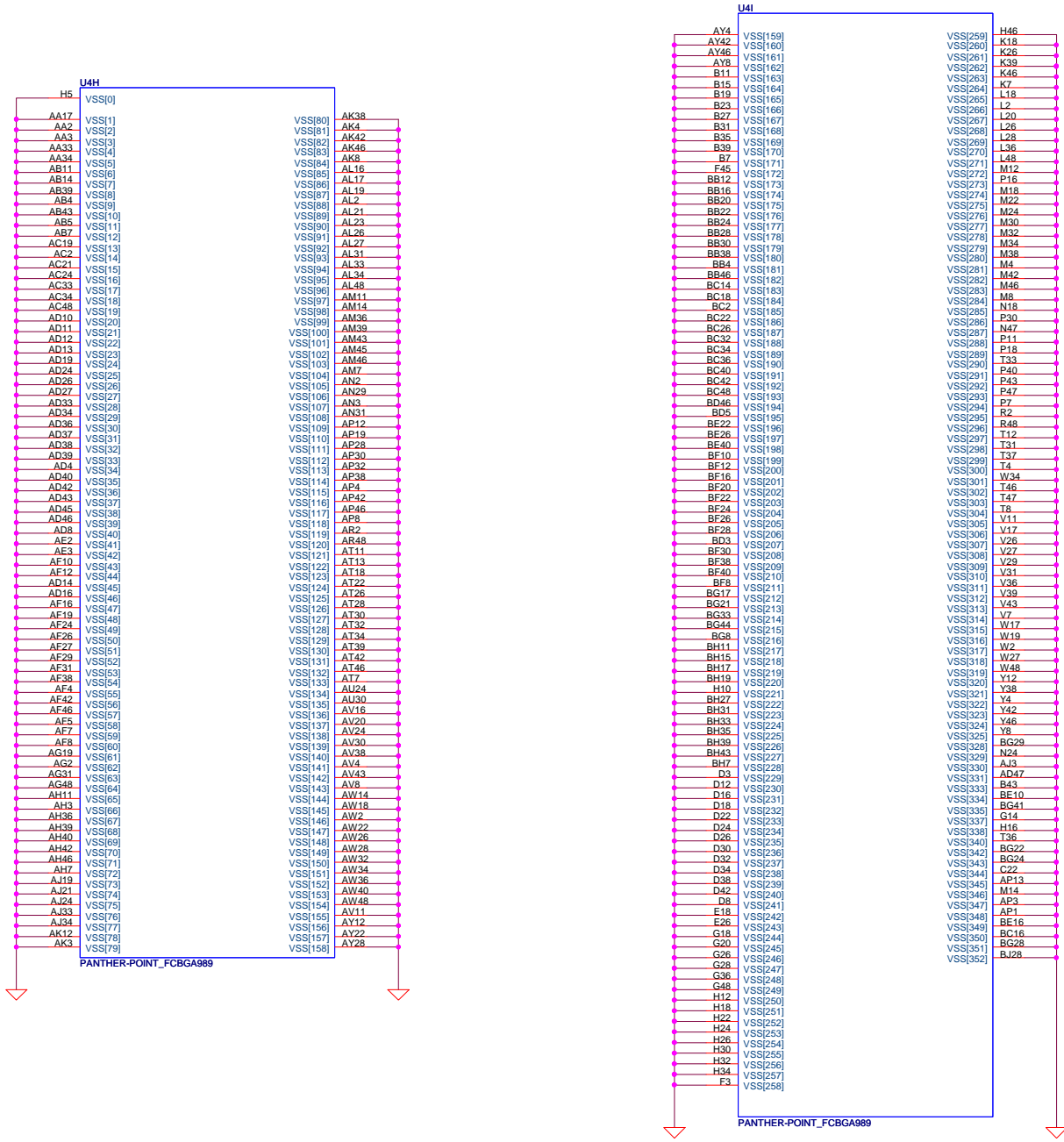
Intel recommend VCCVRM=>1.5V FOR MOBILE  
stuff R265 and unstuff R266 VCCVRM=>1.8V FOR DESKTOP  
VCCVRM = 160mA detail waiting for newest spec

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<b>PCH (7/9) PWR</b>		
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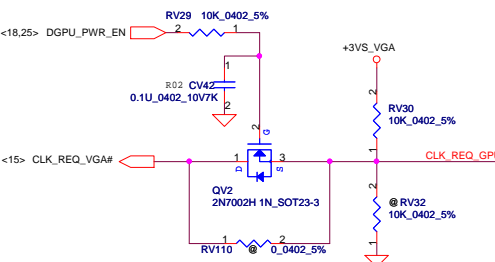
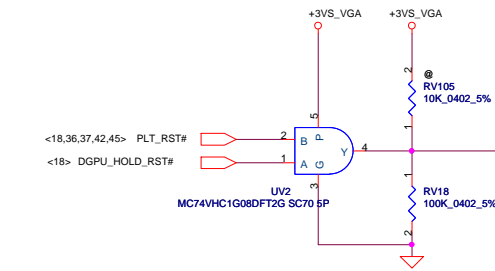
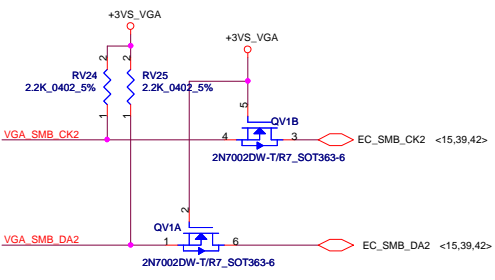
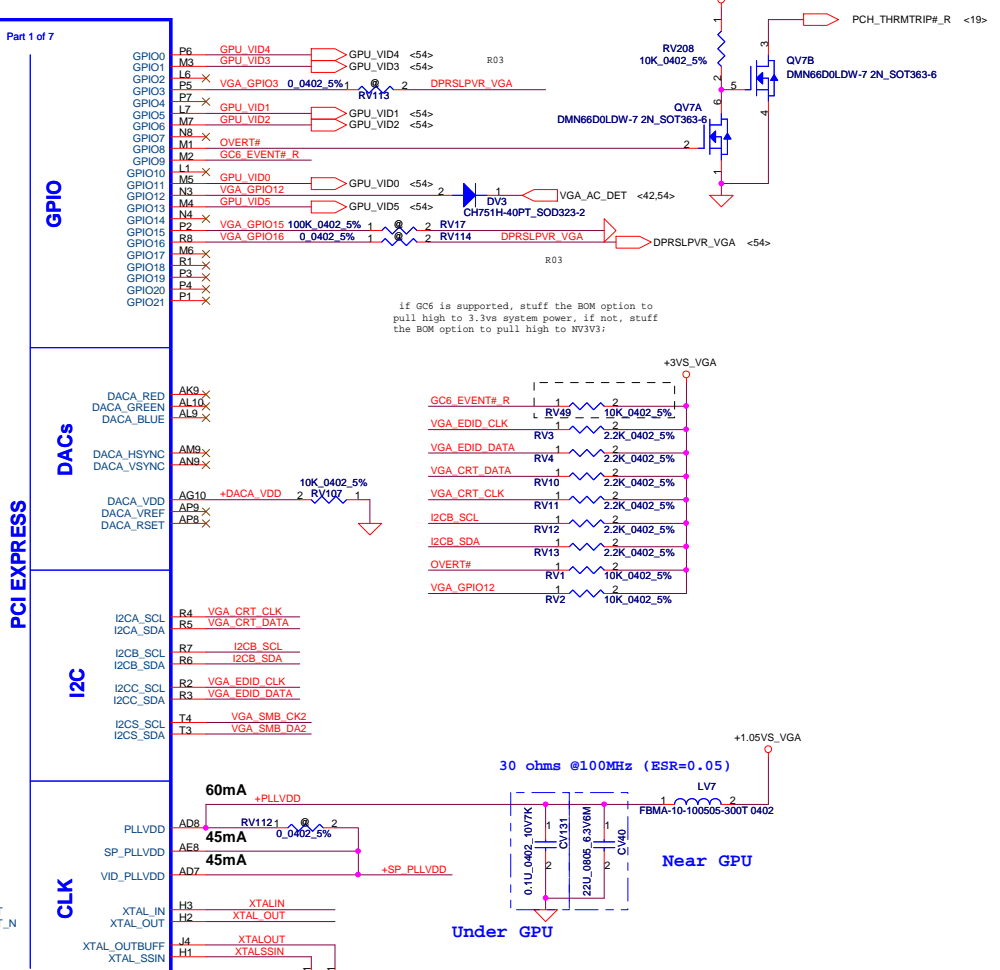
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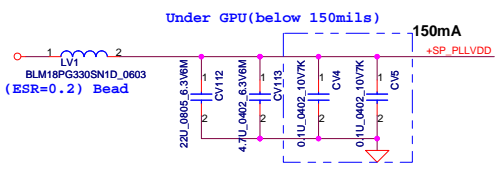
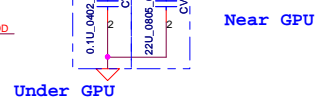
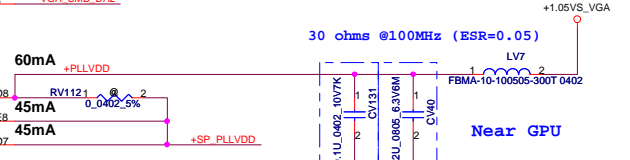
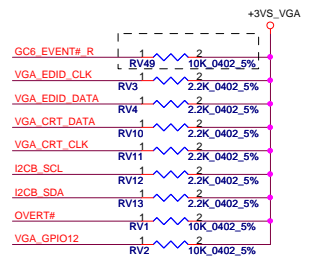
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- <5> PCIE\_CTX\_GRX\_P[0..15]
- <5> PCIE\_CRX\_GTX\_N[0..15]
- <5> PCIE\_CRX\_GTX\_P[0..15]

PCIE_CTX_GRX	PCIE_CRX_GTX	PCIE_CRX_C_GTX	PCIE_TX	PEX
PCIE_CTX_GRX P0	AN12	PEX_RX0		
PCIE_CTX_GRX N0	AM12	PEX_RX0_N		
PCIE_CTX_GRX P1	AN14	PEX_RX1		
PCIE_CTX_GRX N1	AM14	PEX_RX1_N		
PCIE_CTX_GRX P2	AN16	PEX_RX2		
PCIE_CTX_GRX N2	AM16	PEX_RX2_N		
PCIE_CTX_GRX P3	AN18	PEX_RX3		
PCIE_CTX_GRX N3	AM18	PEX_RX3_N		
PCIE_CTX_GRX P4	AN20	PEX_RX4		
PCIE_CTX_GRX N4	AM20	PEX_RX4_N		
PCIE_CTX_GRX P5	AN22	PEX_RX5		
PCIE_CTX_GRX N5	AM22	PEX_RX5_N		
PCIE_CTX_GRX P6	AN24	PEX_RX6		
PCIE_CTX_GRX N6	AM24	PEX_RX6_N		
PCIE_CTX_GRX P7	AN26	PEX_RX7		
PCIE_CTX_GRX N7	AM26	PEX_RX7_N		
PCIE_CTX_GRX P8	AN28	PEX_RX8		
PCIE_CTX_GRX N8	AM28	PEX_RX8_N		
PCIE_CTX_GRX P9	AN30	PEX_RX9		
PCIE_CTX_GRX N9	AM30	PEX_RX9_N		
PCIE_CTX_GRX P10	AN32	PEX_RX10		
PCIE_CTX_GRX N10	AM32	PEX_RX10_N		
PCIE_CTX_GRX P11	AN34	PEX_RX11		
PCIE_CTX_GRX N11	AM34	PEX_RX11_N		
PCIE_CTX_GRX P12	AN36	PEX_RX12		
PCIE_CTX_GRX N12	AM36	PEX_RX12_N		
PCIE_CTX_GRX P13	AN38	PEX_RX13		
PCIE_CTX_GRX N13	AM38	PEX_RX13_N		
PCIE_CTX_GRX P14	AN40	PEX_RX14		
PCIE_CTX_GRX N14	AM40	PEX_RX14_N		
PCIE_CTX_GRX P15	AN42	PEX_RX15		
PCIE_CTX_GRX N15	AM42	PEX_RX15_N		

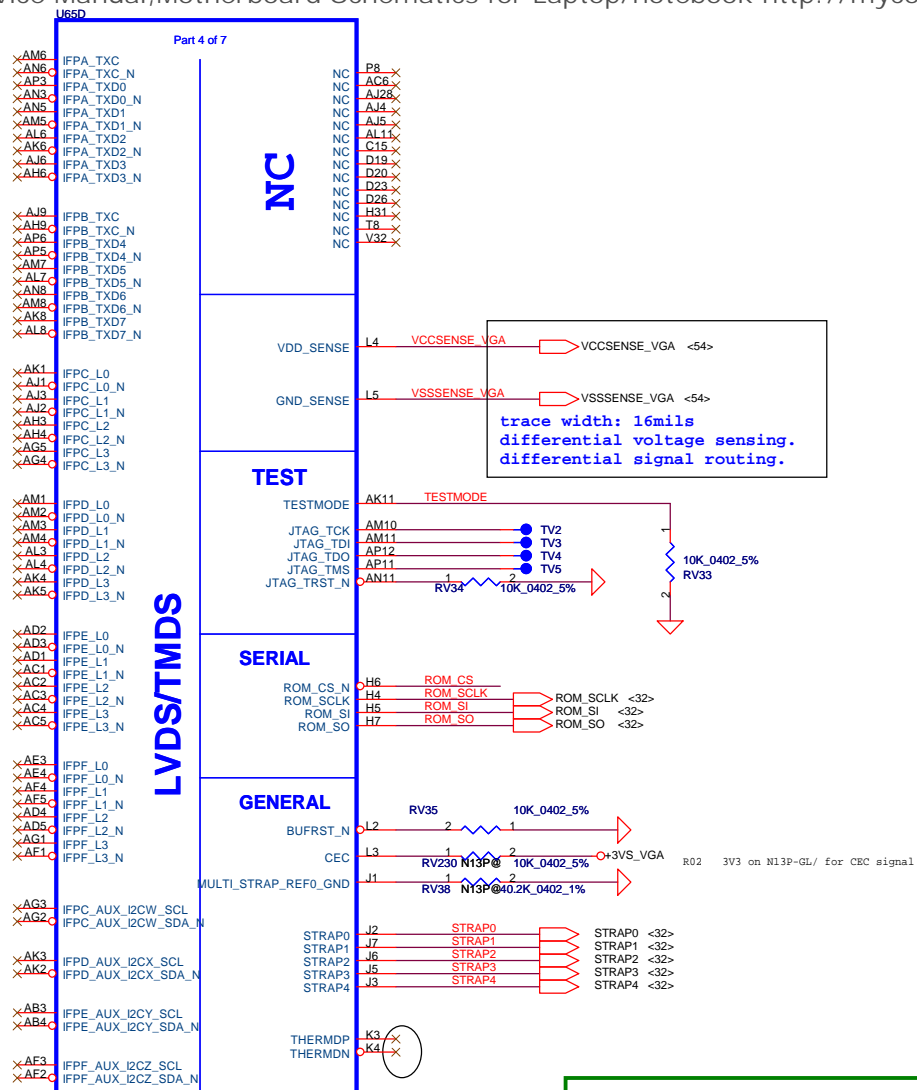
PCIE_CRX_GTX	PCIE_CRX_C_GTX	PCIE_TX	PEX
PCIE_CRX_GTX P0	AK14	PEX_TX0	
PCIE_CRX_GTX N0	AJ14	PEX_TX0_N	
PCIE_CRX_GTX P1	AH14	PEX_TX1	
PCIE_CRX_GTX N1	AG14	PEX_TX1_N	
PCIE_CRX_GTX P2	AK16	PEX_TX2	
PCIE_CRX_GTX N2	AJ16	PEX_TX2_N	
PCIE_CRX_GTX P3	AK18	PEX_TX3	
PCIE_CRX_GTX N3	AJ18	PEX_TX3_N	
PCIE_CRX_GTX P4	AK20	PEX_TX4	
PCIE_CRX_GTX N4	AJ20	PEX_TX4_N	
PCIE_CRX_GTX P5	AK22	PEX_TX5	
PCIE_CRX_GTX N5	AJ22	PEX_TX5_N	
PCIE_CRX_GTX P6	AK24	PEX_TX6	
PCIE_CRX_GTX N6	AJ24	PEX_TX6_N	
PCIE_CRX_GTX P7	AK26	PEX_TX7	
PCIE_CRX_GTX N7	AJ26	PEX_TX7_N	
PCIE_CRX_GTX P8	AK28	PEX_TX8	
PCIE_CRX_GTX N8	AJ28	PEX_TX8_N	
PCIE_CRX_GTX P9	AK30	PEX_TX9	
PCIE_CRX_GTX N9	AJ30	PEX_TX9_N	
PCIE_CRX_GTX P10	AK32	PEX_TX10	
PCIE_CRX_GTX N10	AJ32	PEX_TX10_N	
PCIE_CRX_GTX P11	AK34	PEX_TX11	
PCIE_CRX_GTX N11	AJ34	PEX_TX11_N	
PCIE_CRX_GTX P12	AK36	PEX_TX12	
PCIE_CRX_GTX N12	AJ36	PEX_TX12_N	
PCIE_CRX_GTX P13	AK38	PEX_TX13	
PCIE_CRX_GTX N13	AJ38	PEX_TX13_N	
PCIE_CRX_GTX P14	AK40	PEX_TX14	
PCIE_CRX_GTX N14	AJ40	PEX_TX14_N	
PCIE_CRX_GTX P15	AK42	PEX_TX15	
PCIE_CRX_GTX N15	AJ42	PEX_TX15_N	



if GC6 is supported, stuff the BOM option to pull high to 3.3vs system power, if not, stuff the BOM option to pull high to NV3V3;

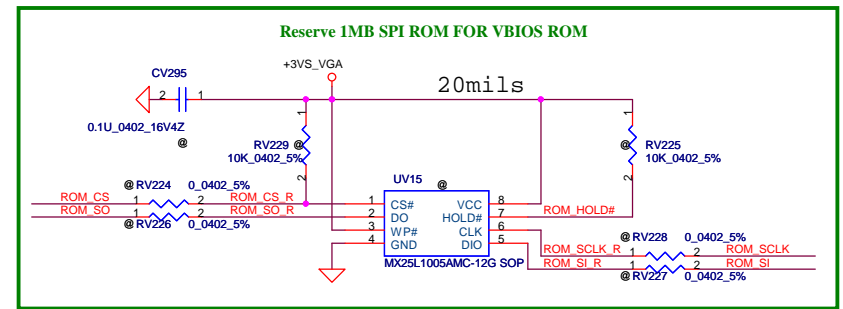


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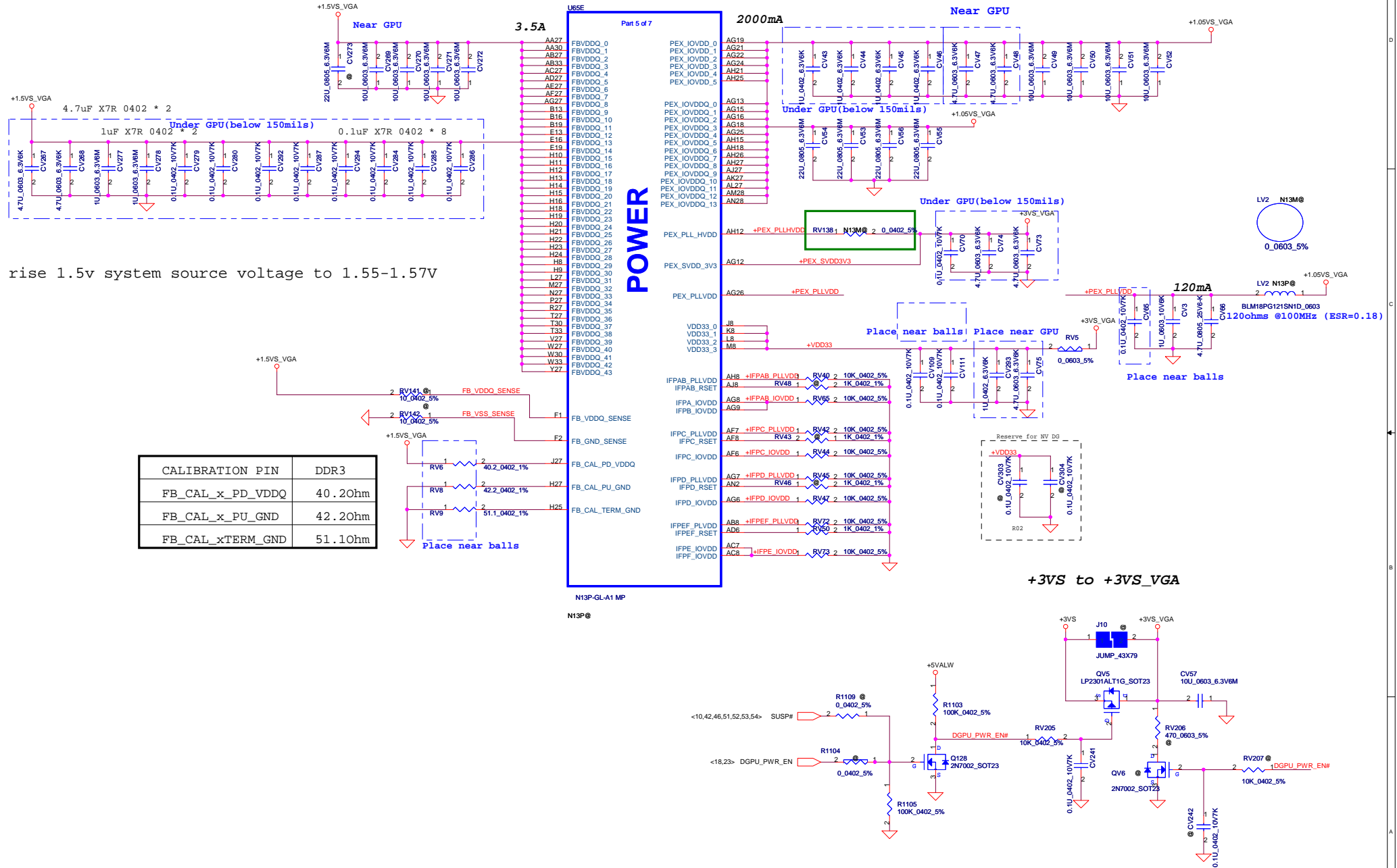
N13P-GL-A1 MP

N13P@



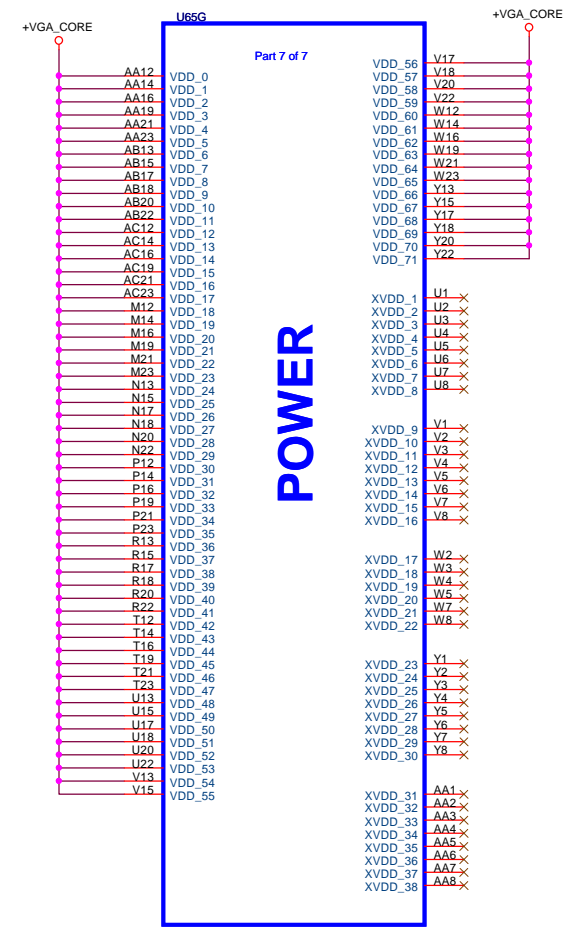
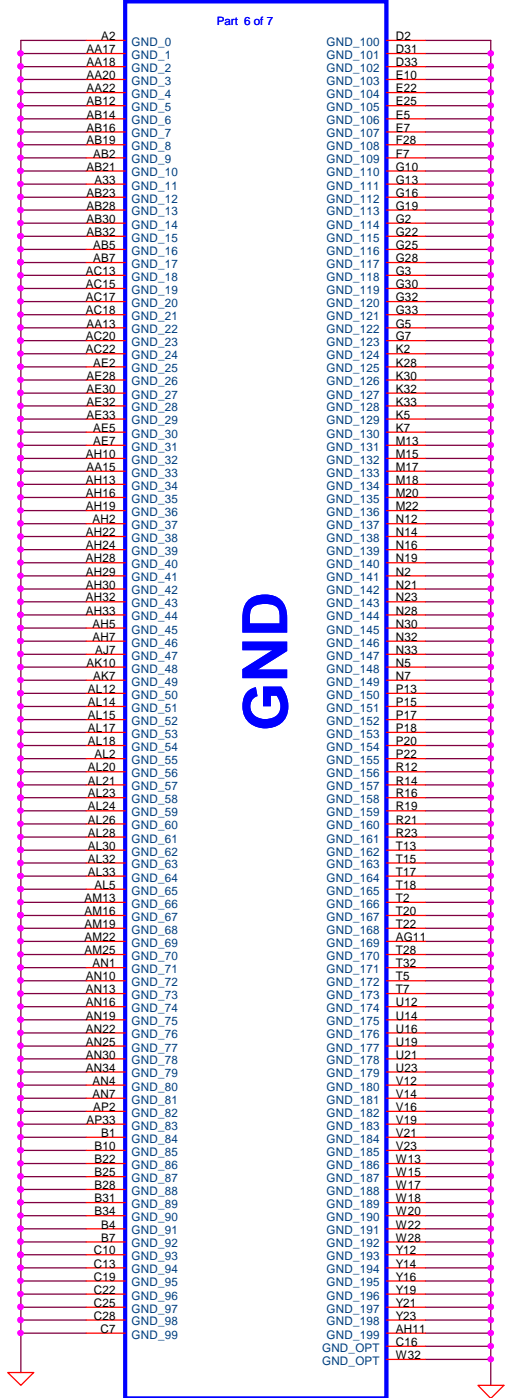
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title		
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Size	Document Number		LA-7981P		Rev	0.2
Date:	Tuesday, February 14, 2012		Sheet	24	of	60





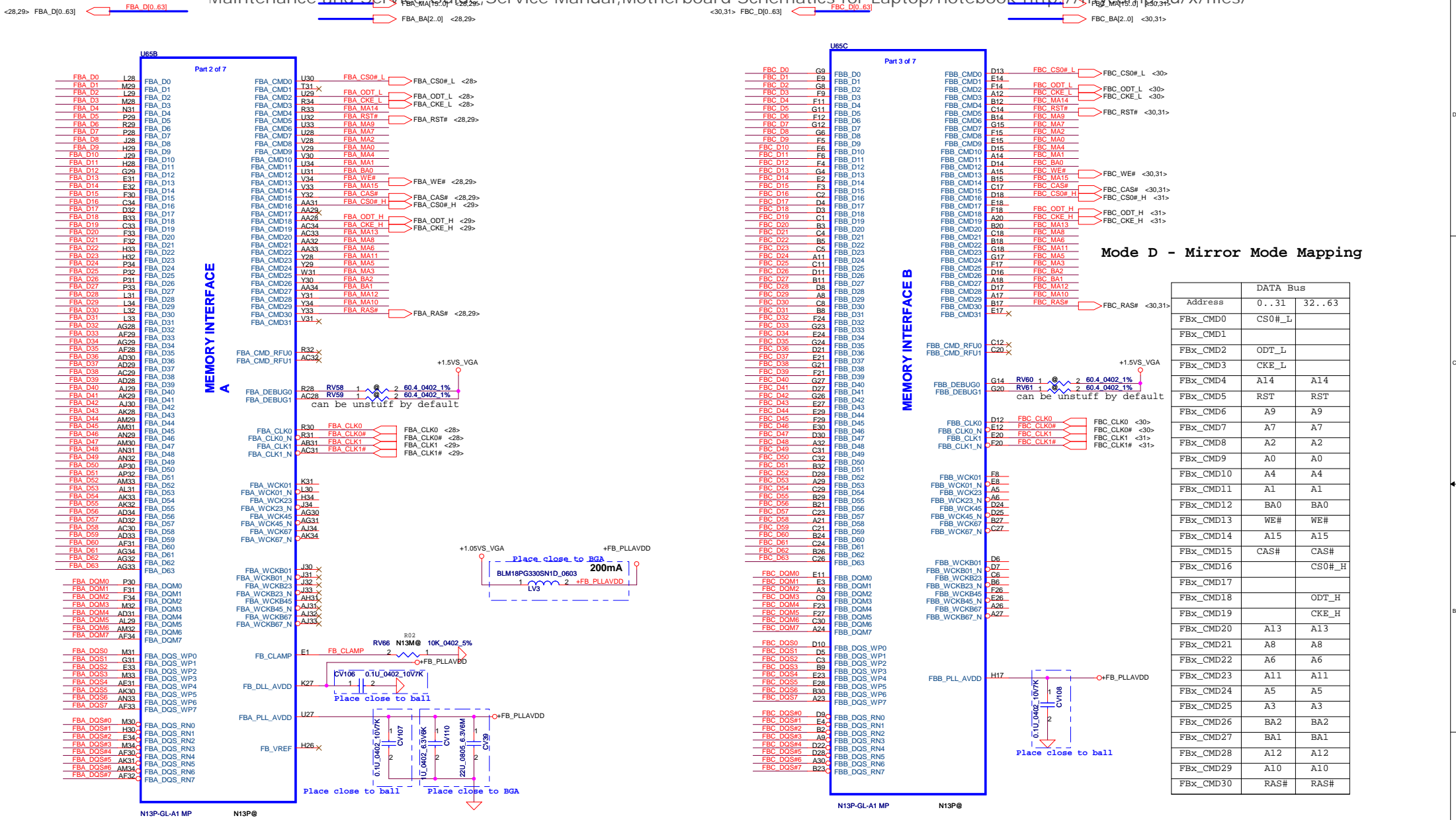
rise 1.5v system source voltage to 1.55-1.57V

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.20ohm
FB_CAL_x_PU_GND	42.20ohm
FB_CAL_x_TERM_GND	51.10ohm



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<b>Compal Electronics, Inc.</b>		
<b>Title</b> <b>N13-VGA CORE, GND</b>		
Size	Document Number <b>LA-7981P</b>	Rev 0.2
Date:	Tuesday, February 14, 2012	Sheet 26 of 60

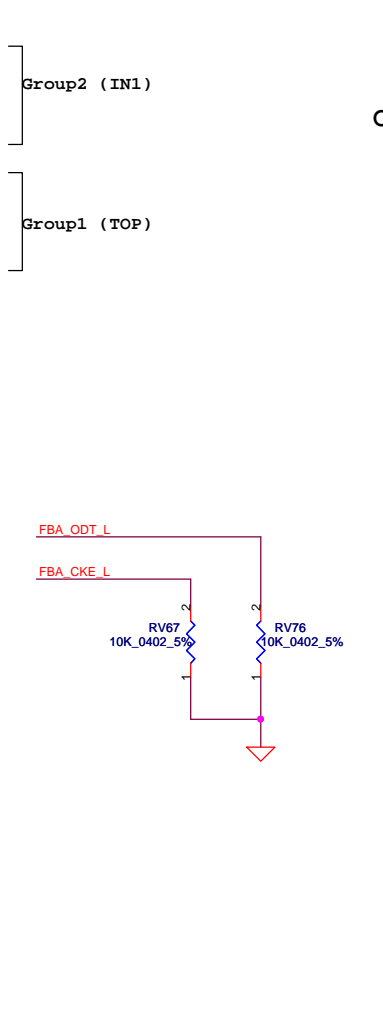
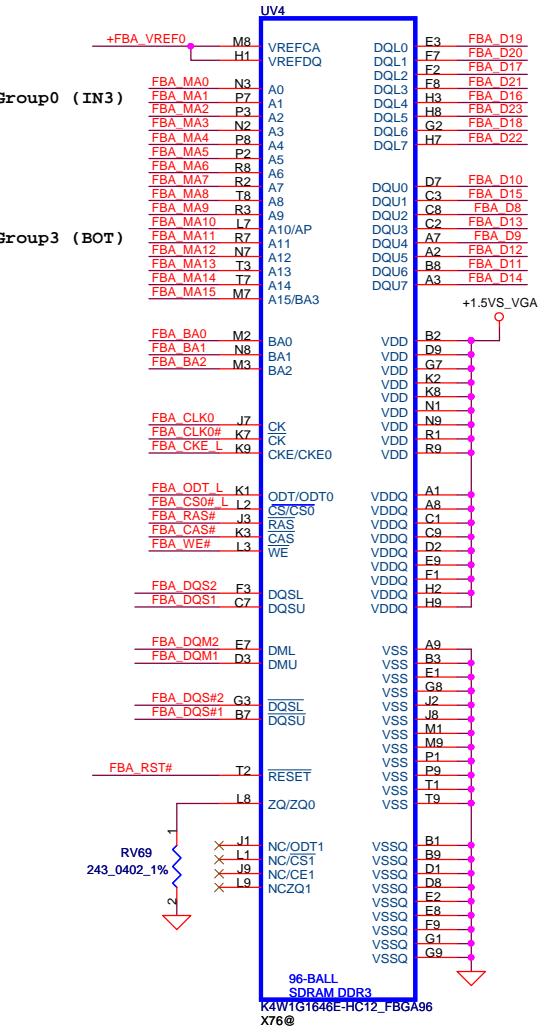
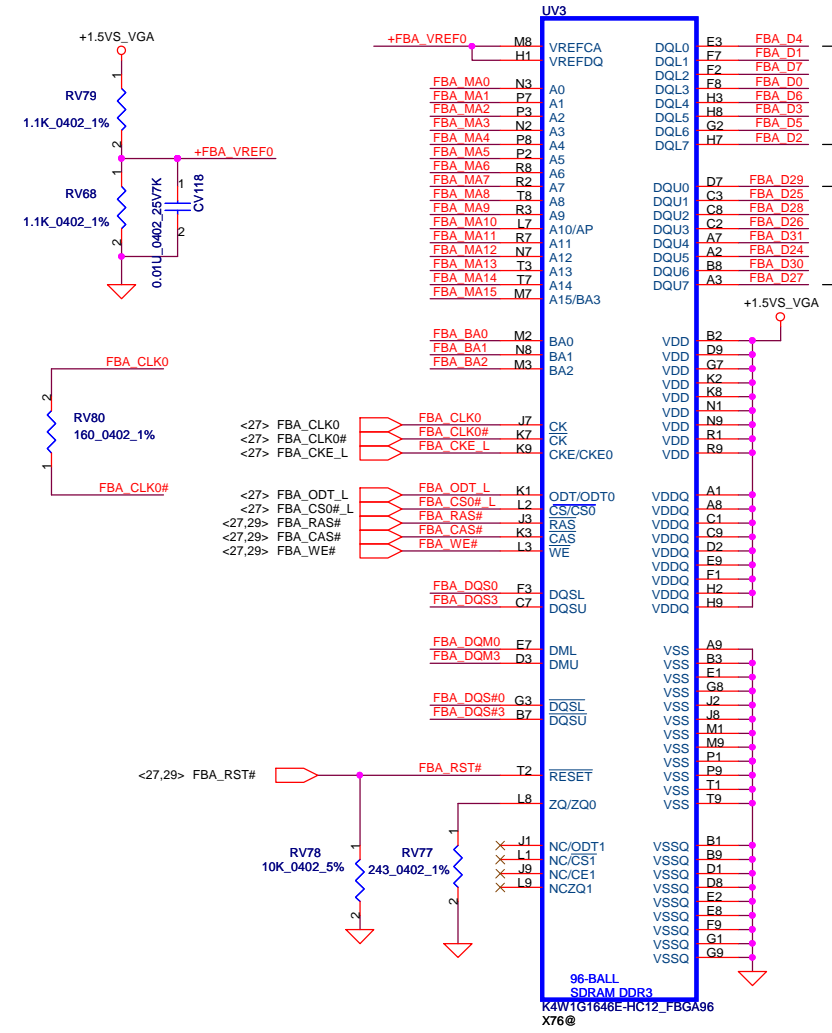
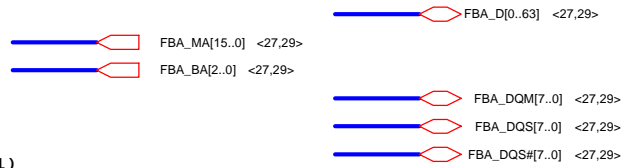


Mode D - Mirror Mode Mapping

	DATA Bus	
	Address 0..31	32..63
FbX_CMD0	CS0#_L	
FbX_CMD1		
FbX_CMD2	ODT_L	
FbX_CMD3	CKE_L	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE#	WE#
FbX_CMD14	A15	A15
FbX_CMD15	CAS#	CAS#
FbX_CMD16	CS0#_H	
FbX_CMD17		
FbX_CMD18	ODT_H	
FbX_CMD19	A10	A10
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RAS#	RAS#



# Memory Partition A - Lower 32 bits



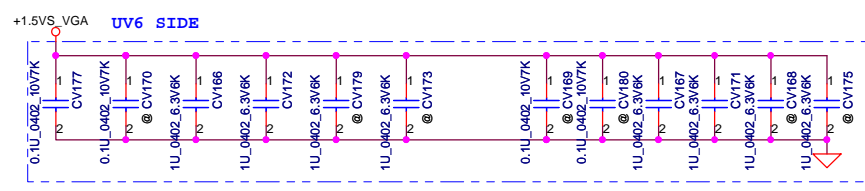
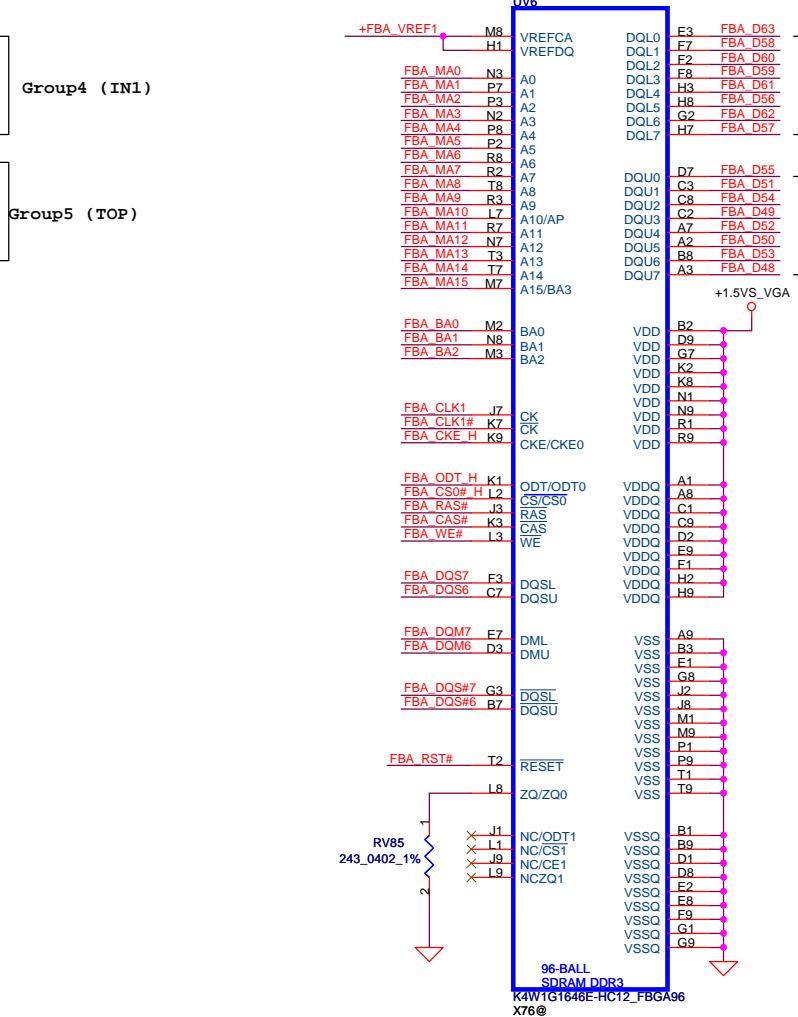
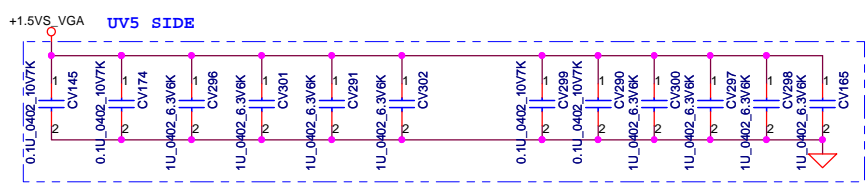
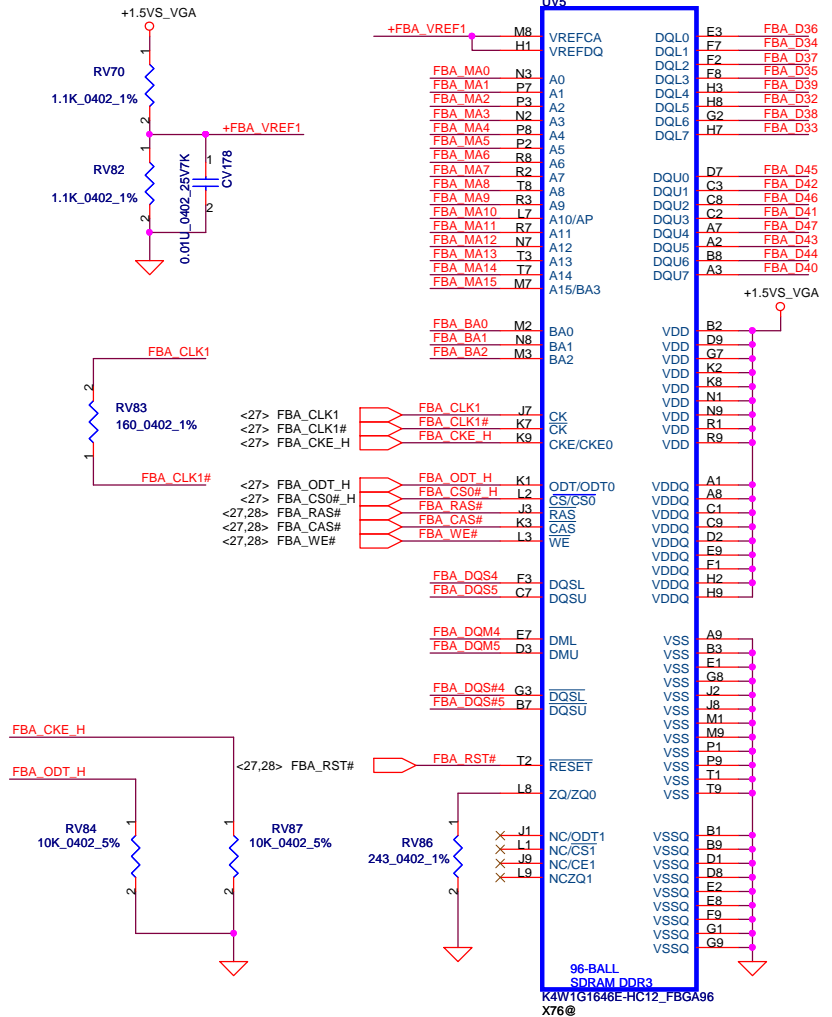
## CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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<b>Compal Electronics, Inc.</b>		
<b>N13X-VRAM A Lower</b>		
Title	Document Number	Rev
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# Memory Partition A - Upper 32 bits



- FBA\_D[0..63] <27,28>
- FBA\_MA[15..0] <27,28>
- FBA\_BA[2..0] <27,28>
- FBA\_DQM[7..0] <27,28>
- FBA\_DQS[7..0] <27,28>
- FBA\_DQS#[7..0] <27,28>

## CMD mapping mod Mode D

Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

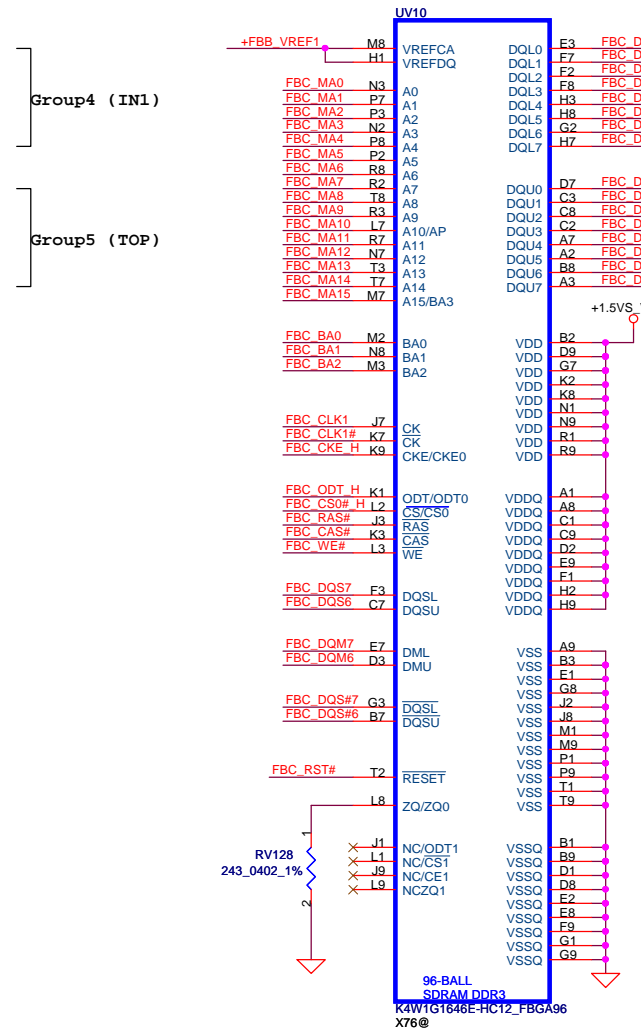
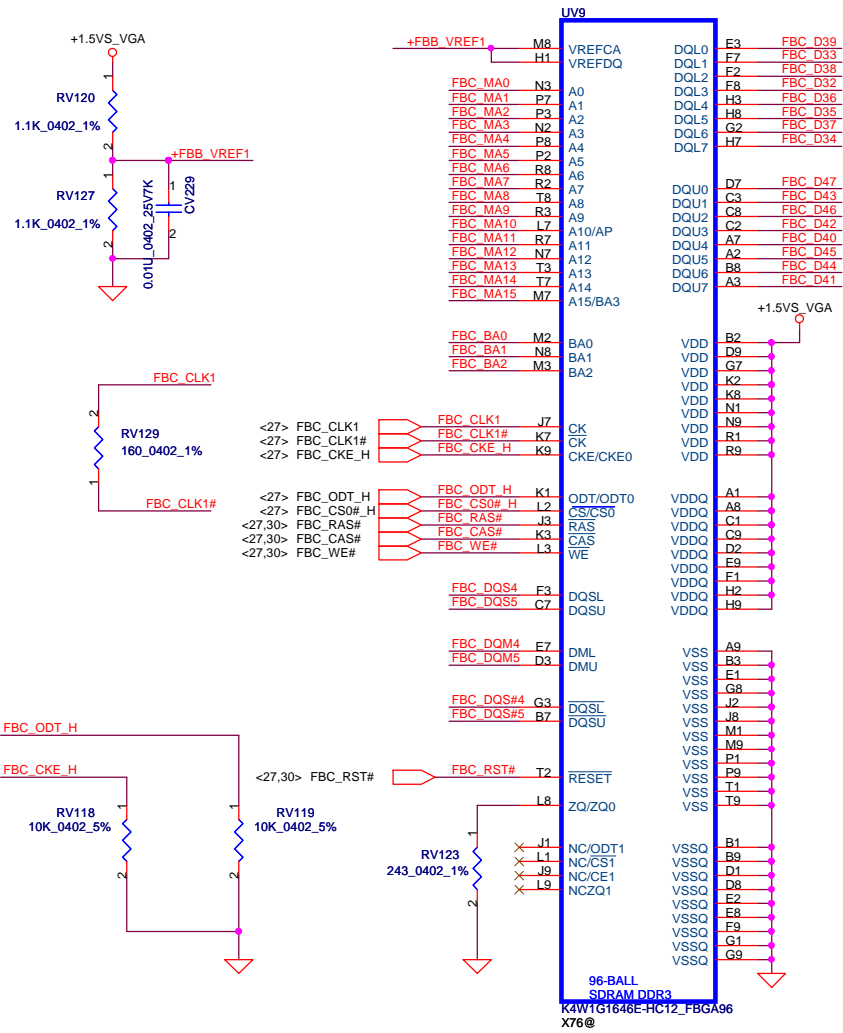
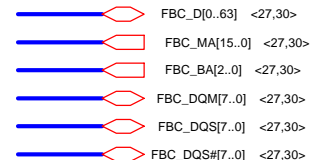
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<b>N13X-VRAM A Upper</b>		
Size	Document Number	Rev 0.2
<b>LA-7981P</b>		
Date:	Tuesday, February 14, 2012	Sheet 29 of 60



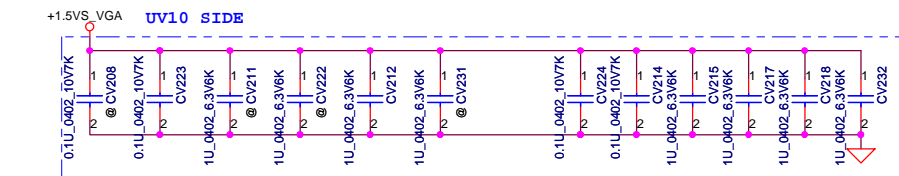
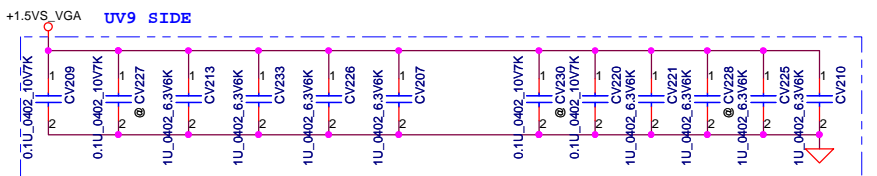


# Memory Partition C - Upper 32 bits

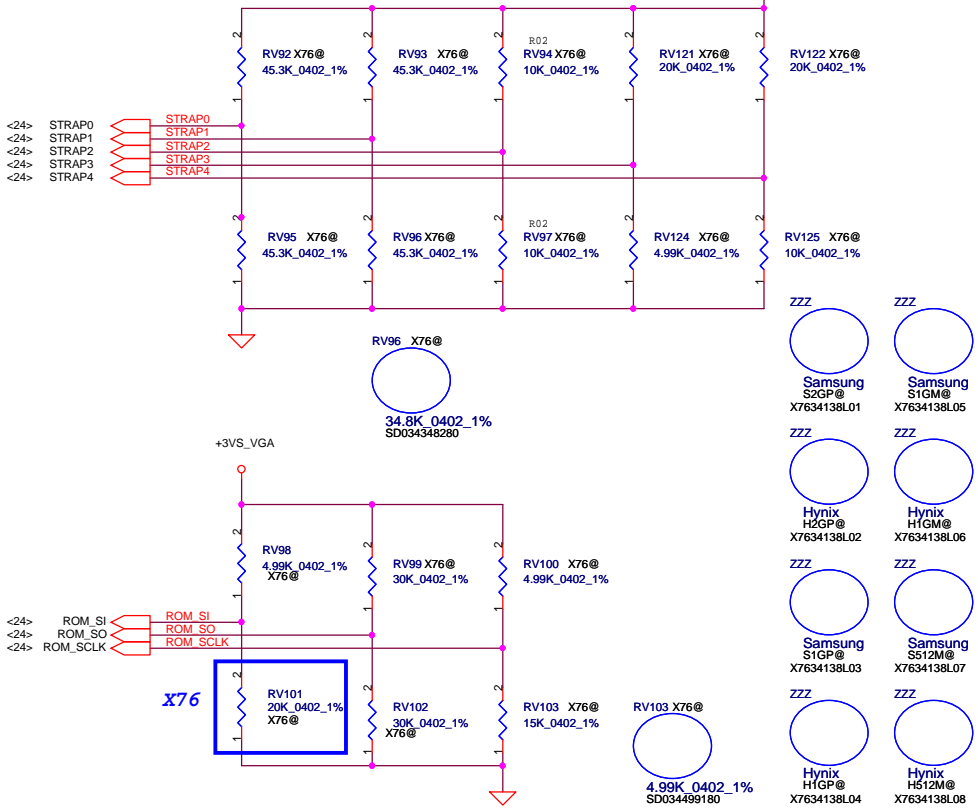


## CMD mapping mod Mode D

Address	DATA Bus	
FBx_CMD0	0..31	32..63
FBx_CMD1	CS0#_L	
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

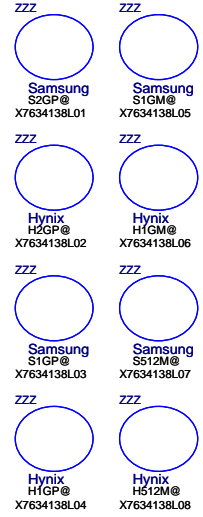


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				Date Tuesday, February 14, 2012	Rev 0.2
				Sheet 31 of 60	



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

For N13P-GL strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8	Samsung (2Gb)	R	R	R	R	R	R	R	R
			K4W2G1646C-HC11	PU 45K	PD 45K	PU 10K	n/a	n/a	PD 45K	PD 10K	PD 15K
N13P-GL	900 MHz	128M* 16* 8	Hynix (2Gb)	R	R	R	R	R	R	R	R
			H5TQ1G63DFR-11C	PU 45K	PD 45K	PU 10K	n/a	n/a	PD 35K	PD 10K	PD 15K
N13P-GL	900 MHz	64M* 16* 8	Samsung (1Gb)	R	R	R	R	R	R	R	R
			K4W1G1646G-BC11	PU 45K	PD 45K	PU 10K	n/a	n/a	PD 20K	PD 10K	PD 15K
N13P-GL	900 MHz	64M* 16* 8	Hynix (1Gb)	R	R	R	R	R	R	R	R
			H5TQ1G63DFR-11C	PU 45K	PD 45K	PU 10K	n/a	n/a	PD 15K	PD 10K	PD 15K

For N13M-GE strap table

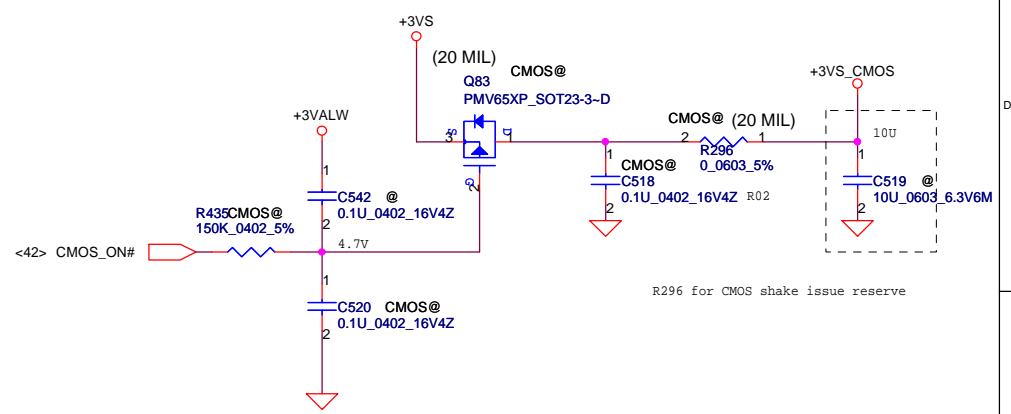
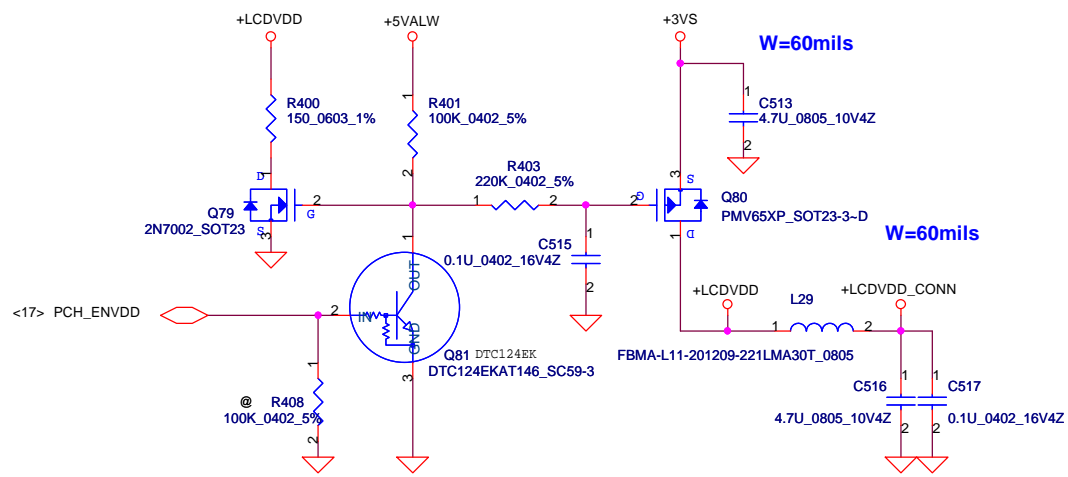
GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE	900 MHz	128M* 16* 4	Samsung (2Gb)	R	R	R	R	R	R	R	R
			K4W2G1646C-HC11	PU 10K	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
N13M-GE	900 MHz	128M* 16* 4	Hynix (2Gb)	R	R	R	R	R	R	R	R
			H5TQ1G63DFR-11C	PD 10K	PU 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
N13M-GE	900 MHz	64M* 16* 4	Samsung (1Gb)	R	R	R	R	R	R	R	R
			K4W1G1646G-BC11	PU 10K	PU 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
N13M-GE	900 MHz	64M* 16* 4	Hynix (1Gb)	R	R	R	R	R	R	R	R
			H5TQ1G63DFR-11C	PD 10K	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K

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Size Custom	Document Number	<b>LA-7981P</b>		Rev	0.2
Date:	Tuesday, February 14, 2012	Sheet	32	of	60

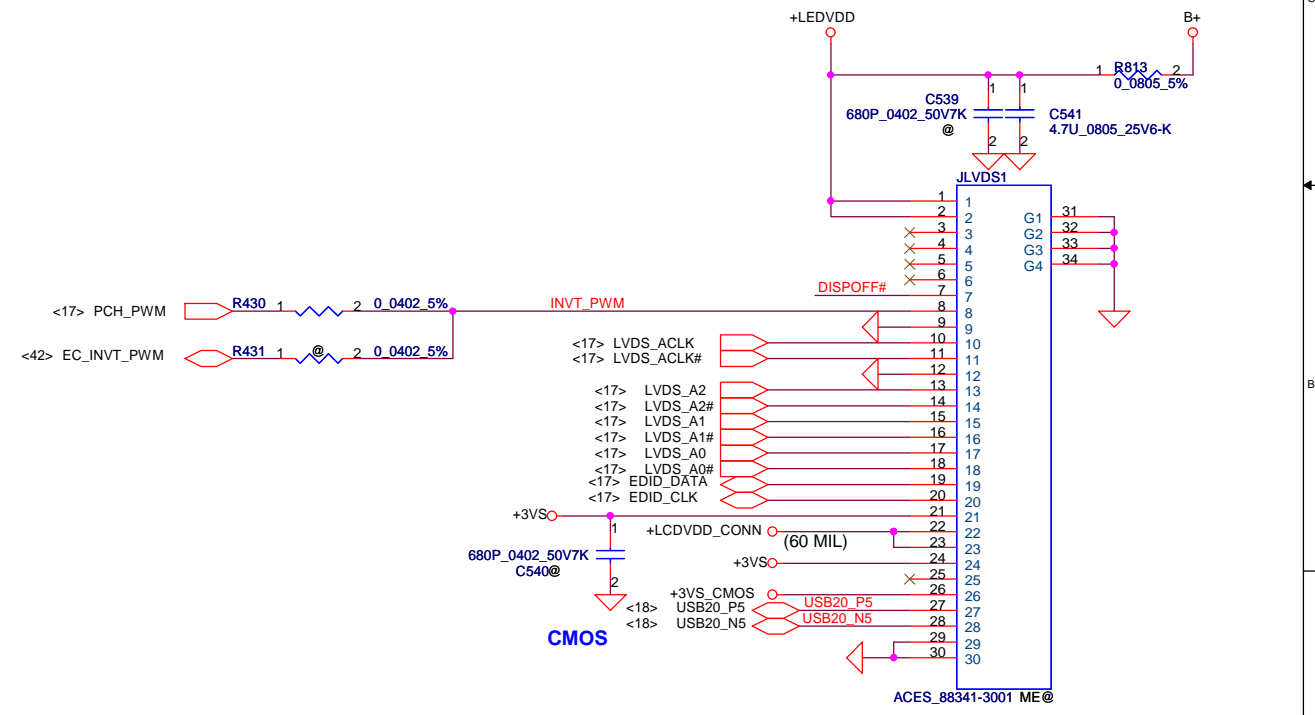
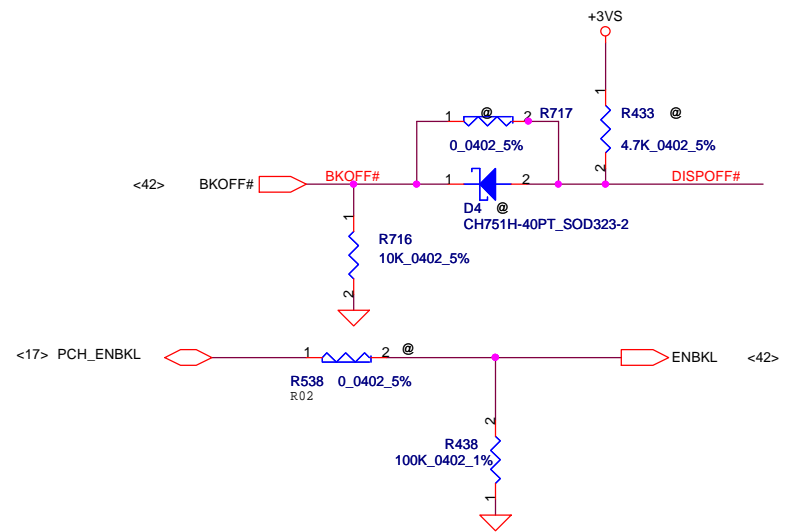


# LCD POWER CIRCUIT

# CMOS Camera

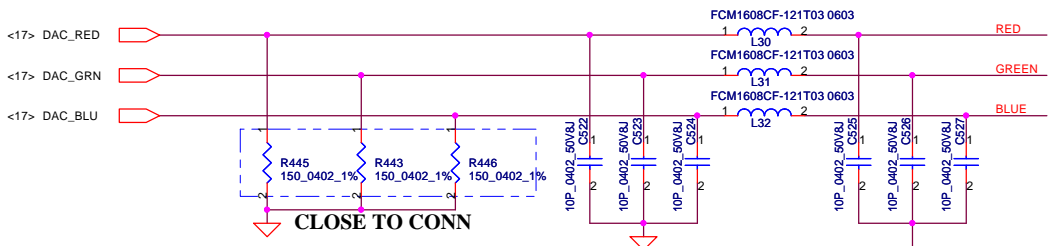
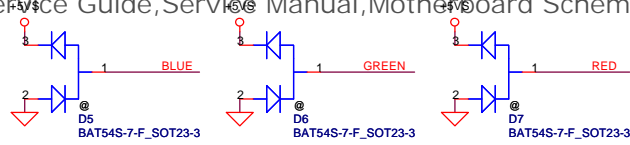


# VGA LCD/PANEL BD. Conn.

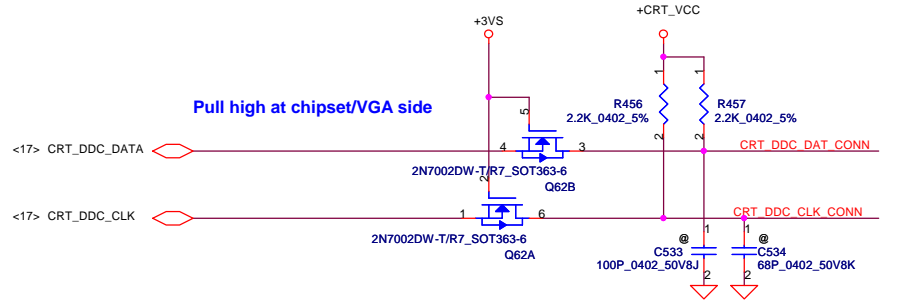
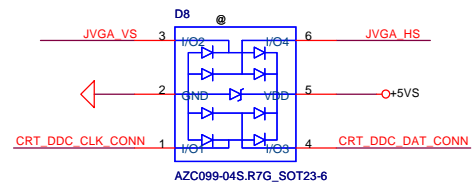
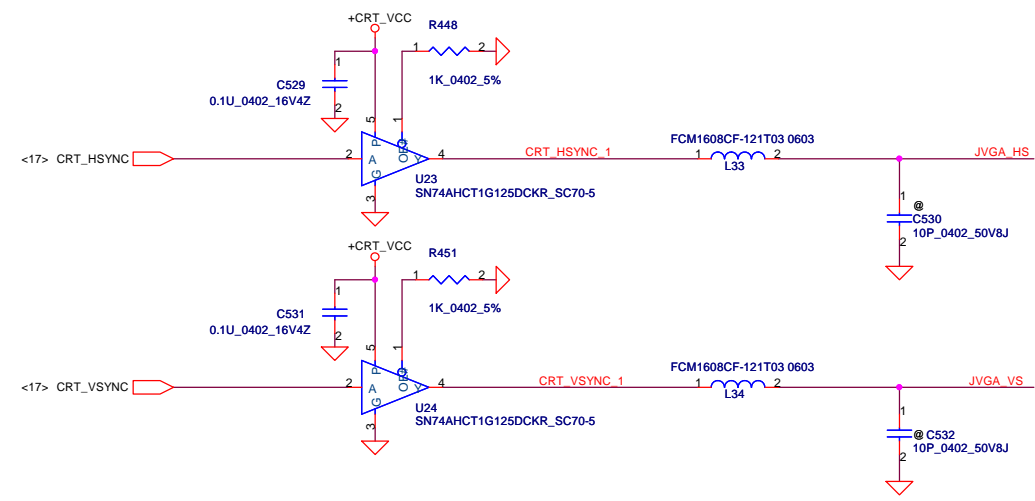
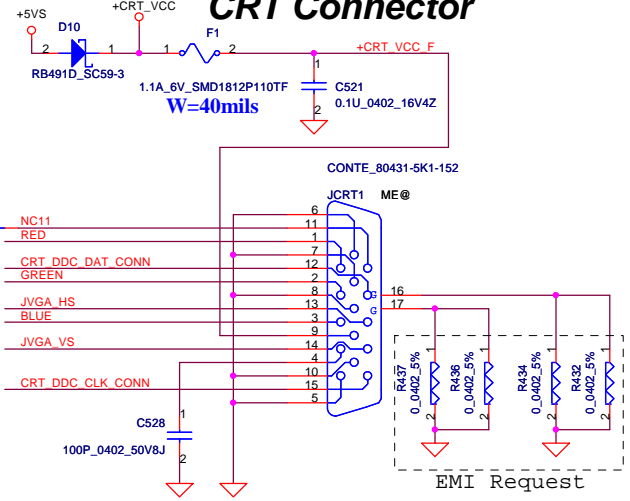


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Title		<b>LVDS/CAMERA</b>	
Size	Document Number	Rev	
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Date:	Tuesday, February 14, 2012	Sheet	33 of 60

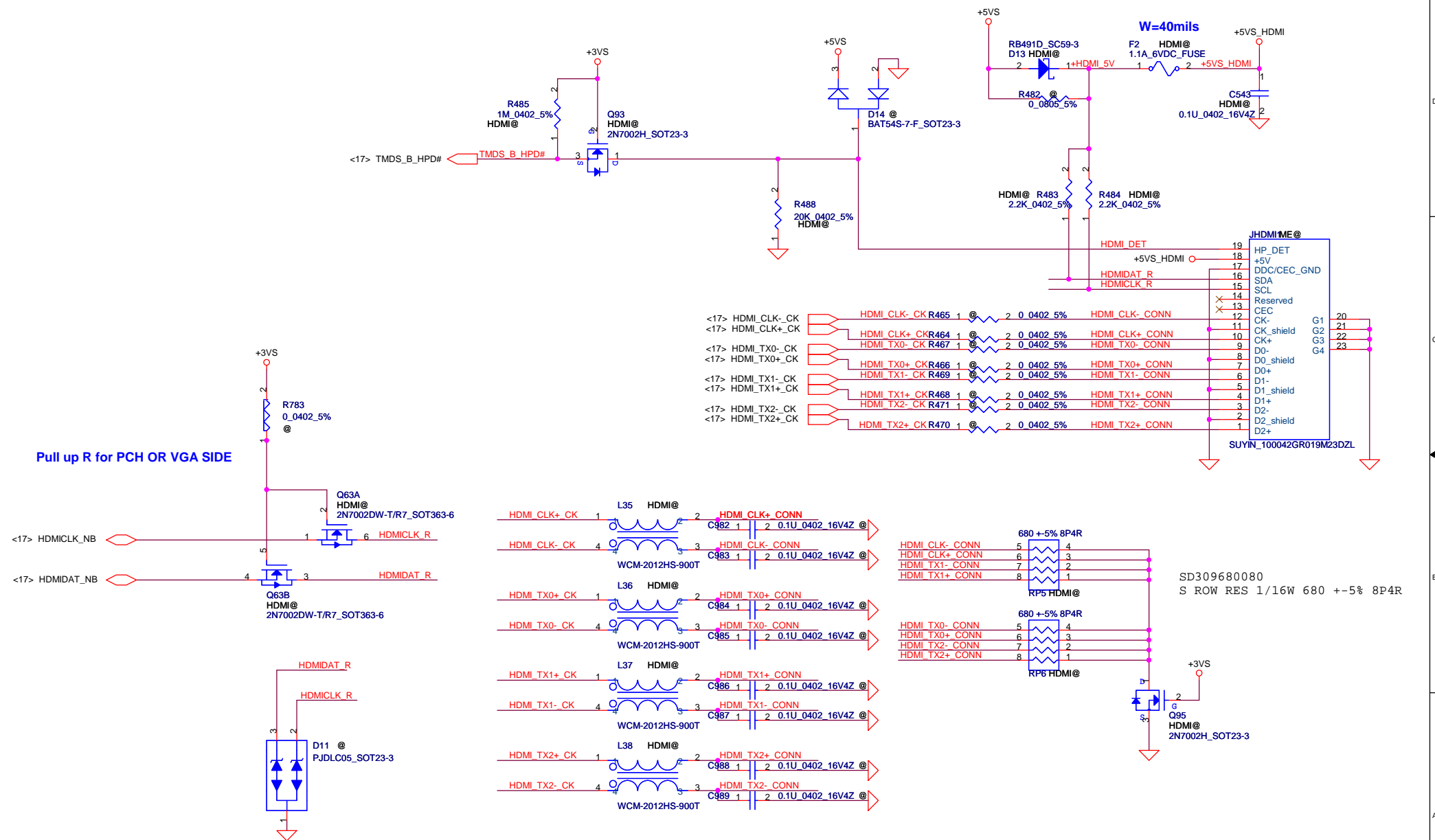


### CRT Connector



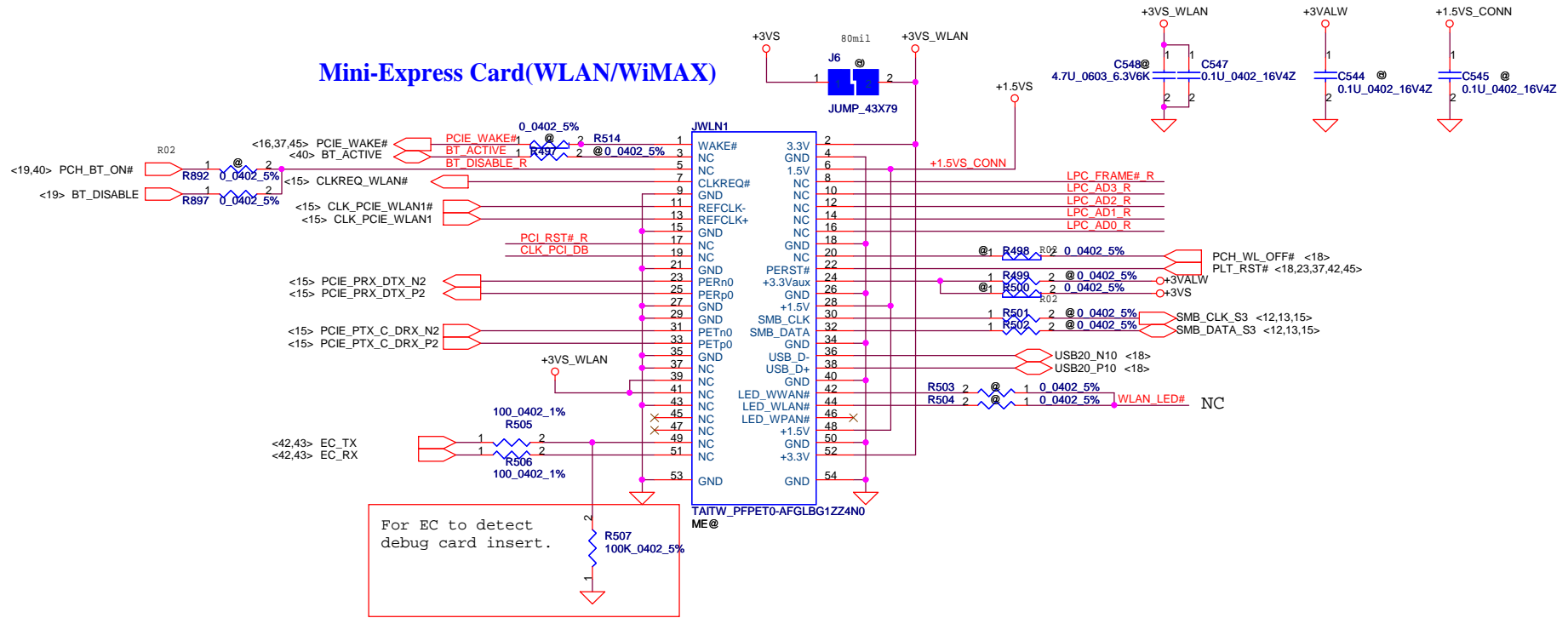
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Issued Date	2011/06/15	Deciphered Date	2012/07/11
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Compal Electronics, Inc.		
Title <b>CRT Connector</b>		
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Size	Document Number			Rev	0.2
				LA-7981P	
Date: Tuesday, February 14, 2012				Sheet	35 of 60

# Mini-Express Card for WLAN/WiMAX(Half)



For EC to detect debug card insert.

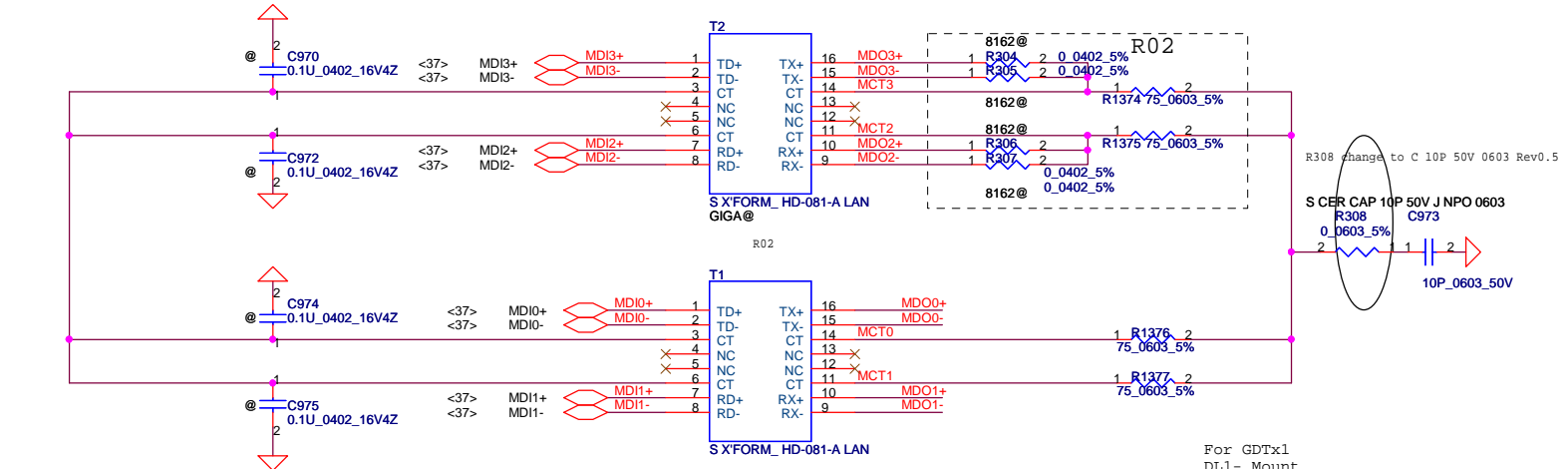
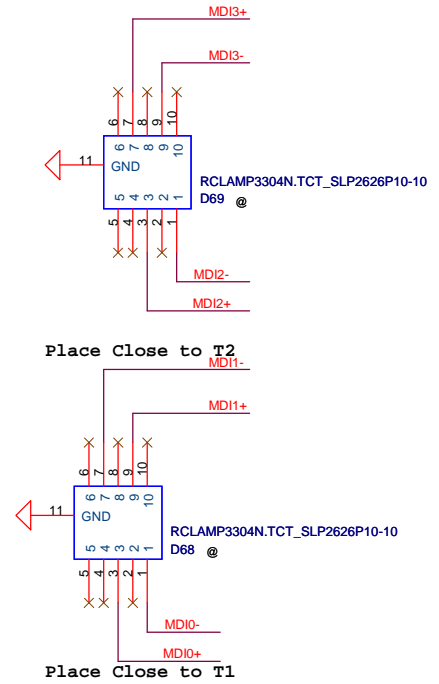
**Reserve for SW mini-pcie debug card.**  
**Series resistors closed to KBC side.**

LPC_FRAME# R	R508	1	@	2	0.0402 5%	LPC_FRAME#	LPC_FRAME# <14,42>
LPC_AD3 R	R509	1	@	2	0.0402 5%	LPC_AD3	LPC_AD3 <14,42>
LPC_AD2 R	R510	1	@	2	0.0402 5%	LPC_AD2	LPC_AD2 <14,42>
LPC_AD1 R	R511	1	@	2	0.0402 5%	LPC_AD1	LPC_AD1 <14,42>
LPC_AD0 R	R512	1	@	2	0.0402 5%	LPC_AD0	LPC_AD0 <14,42>
PCI_RST# R	R513	1	@	2	0.0402 5%	PLT_RST#	PLT_RST# <18>
CLK_PCI_DB						CLK_PCI_DB	CLK_PCI_DB <18>

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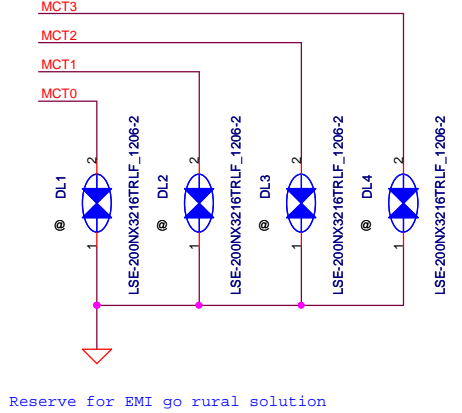
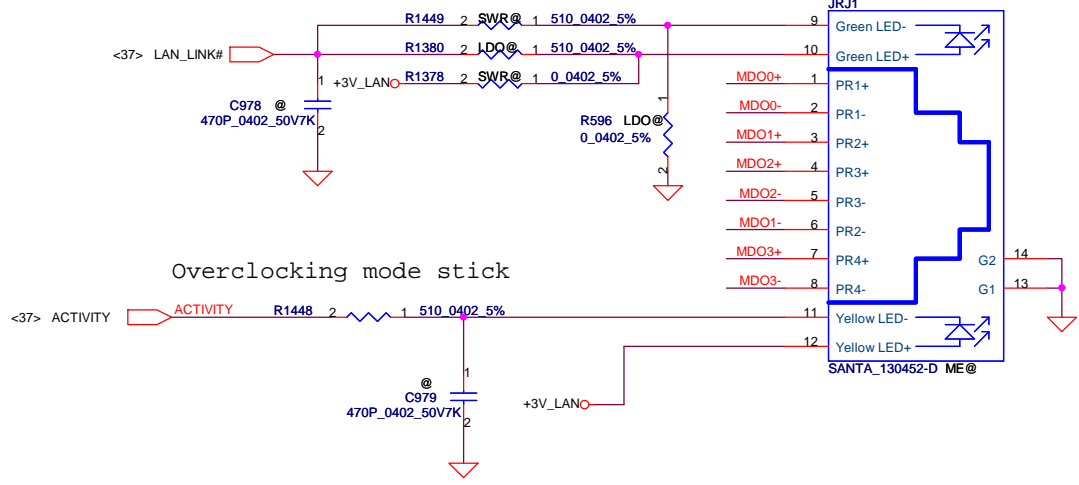
<b>Compal Electronics, Inc.</b>		
<b>Mini-Card/NEW Card/SIM</b>		
Title		
Size	Document Number	Rev
	<b>LA-7981P</b>	0.2
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For GDTx1  
 DL1- Mount  
 DL2/DL3/DL4- NC  
 R308- 75 ohm  
 R1374/R1375/R1376/R1377- 0 ohm

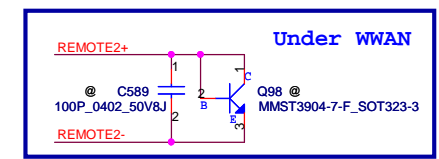
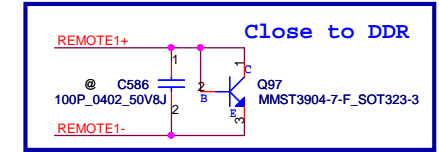
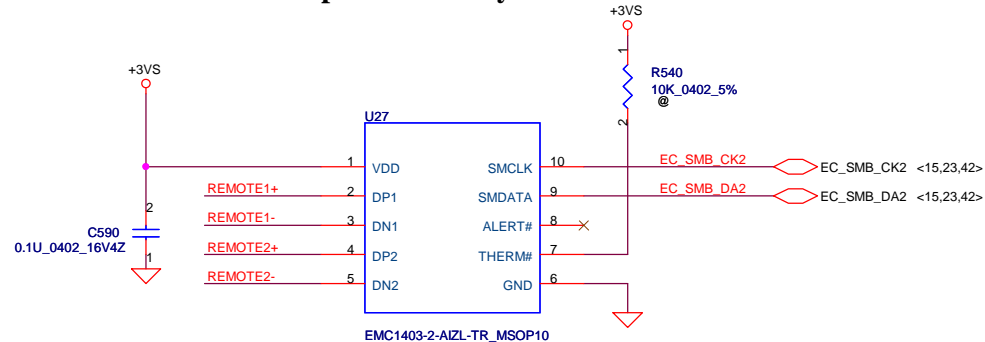
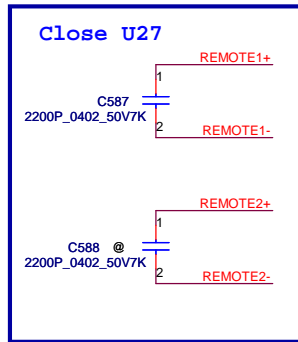
LDO Mode: pop R1380;R596  
 SWR Mode: pop R1449;R1378



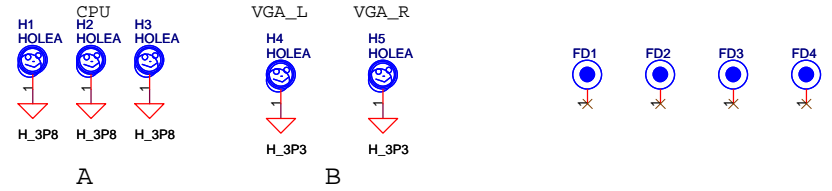
Reserve for EMI go rural solution

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Size	Document Number			Rev	
	LA-7981P			0.2	
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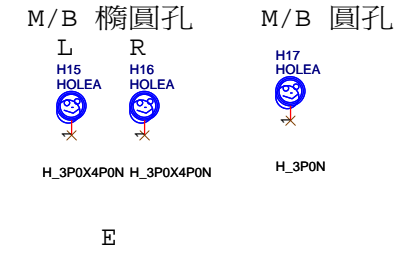
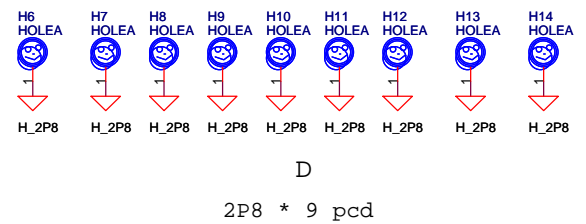
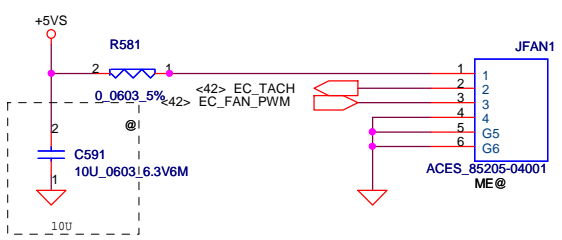
### SMSC thermal sensor placed near by VRAM



REMOTE1,2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

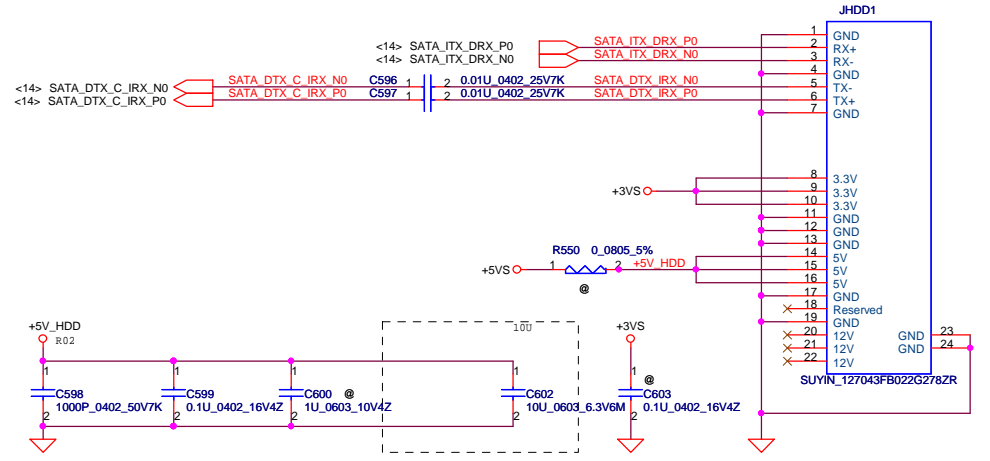
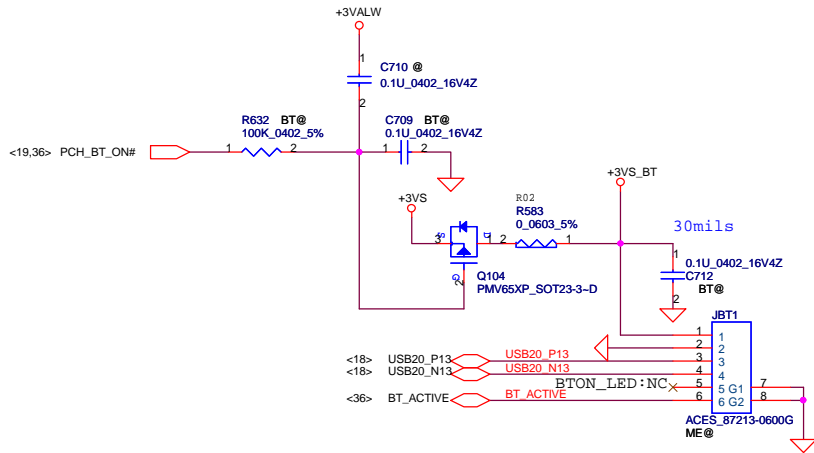


### FAN1 Conn

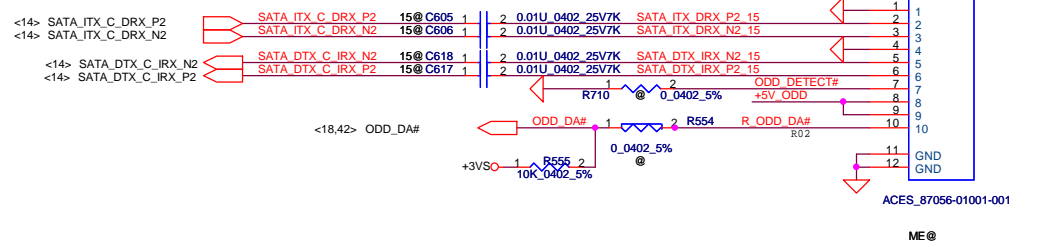
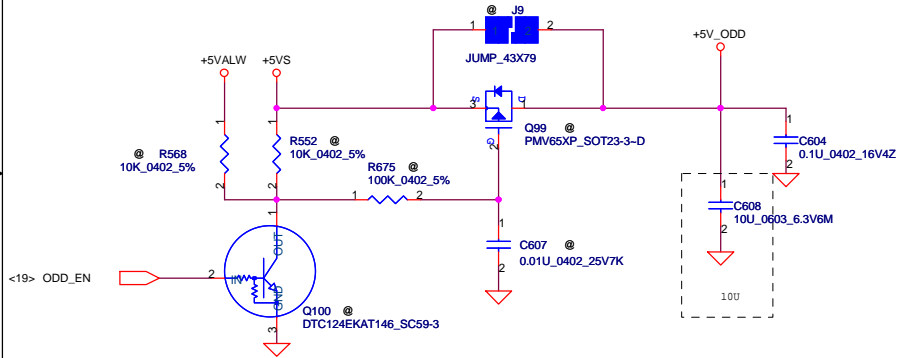


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**BT MODULE CONN**

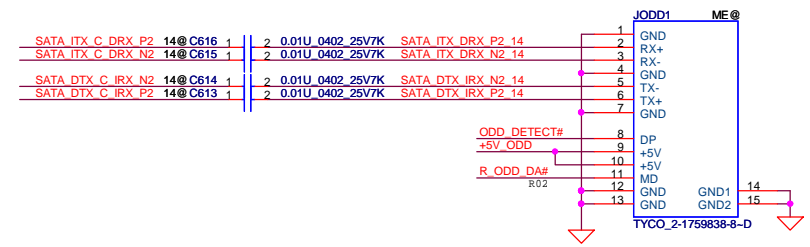


**ODD Power Control**



**FOR 15" SATA ODD FFC Conn.**

**FOR 14" SATA ODD Conn.**

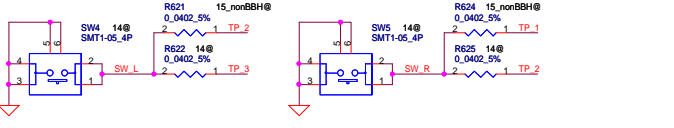
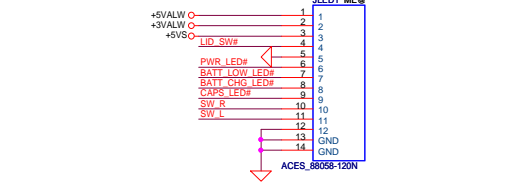
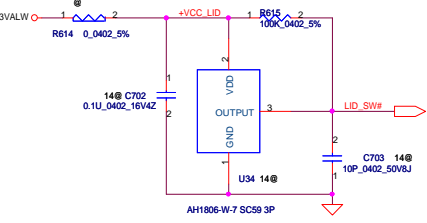
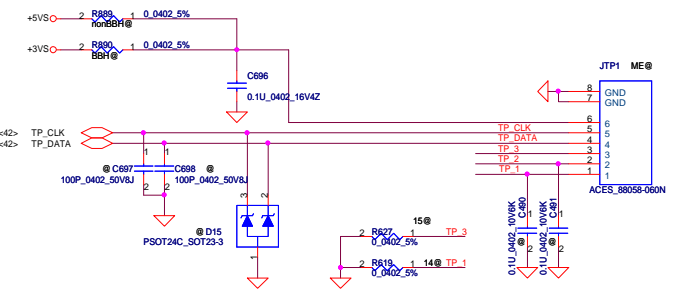
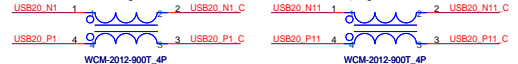
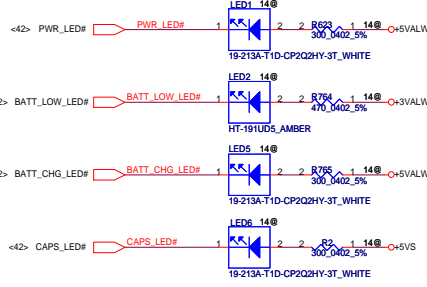
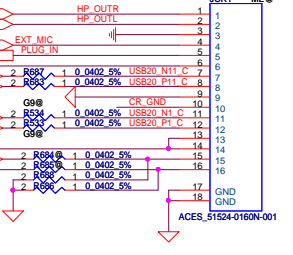
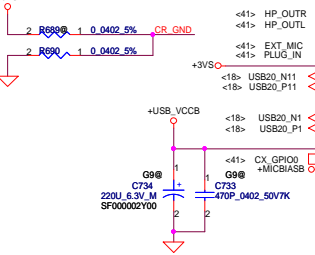
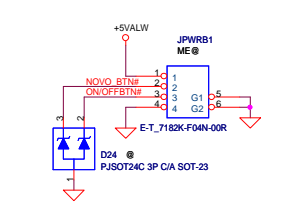
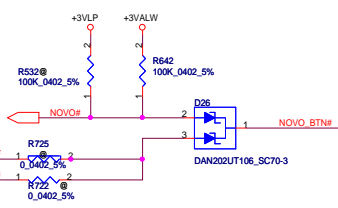
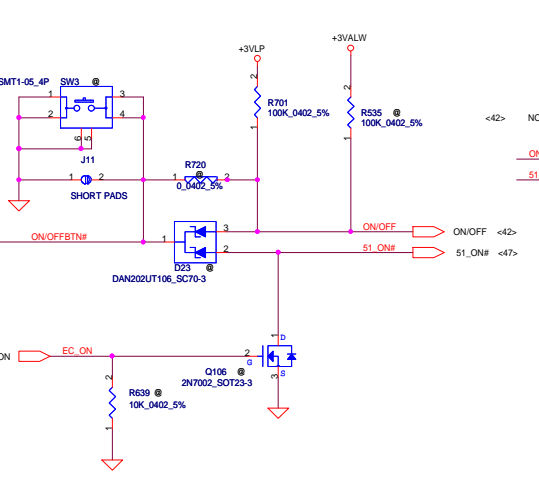
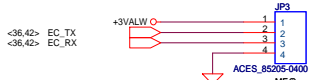
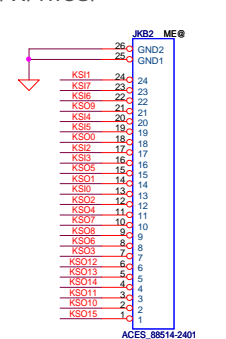
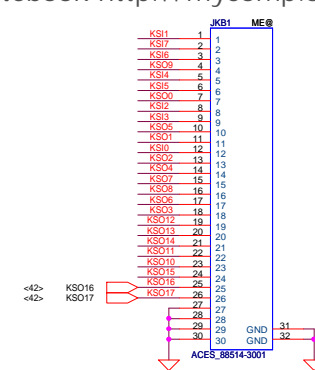
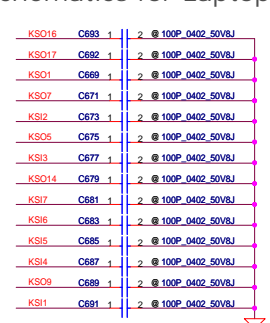
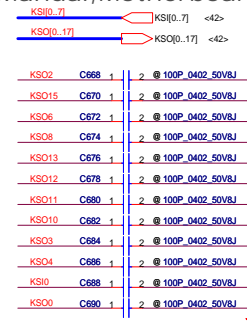


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				Date: Tuesday, February 14, 2012	Sheet 40 of 60



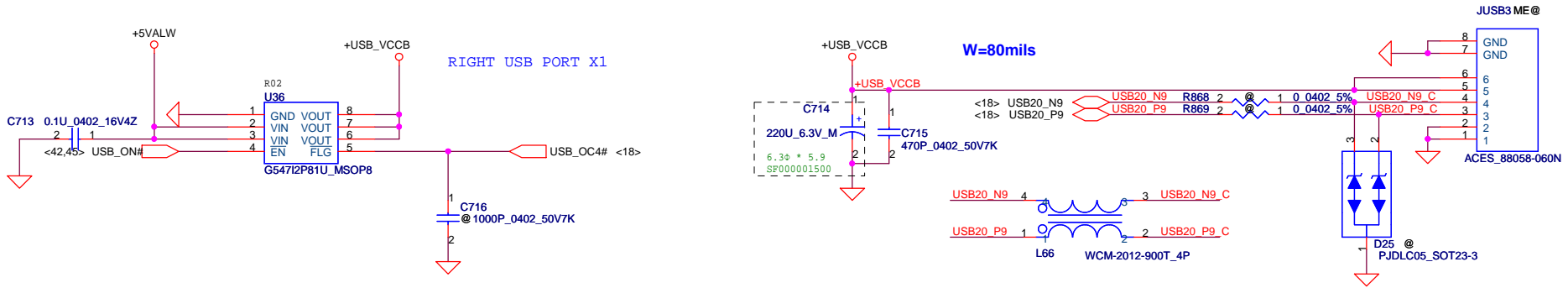




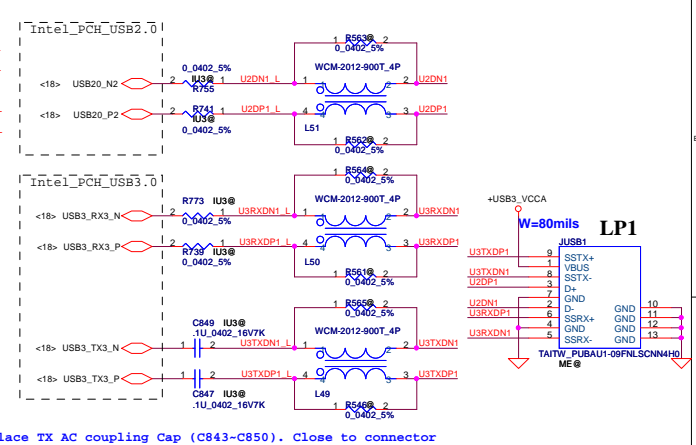
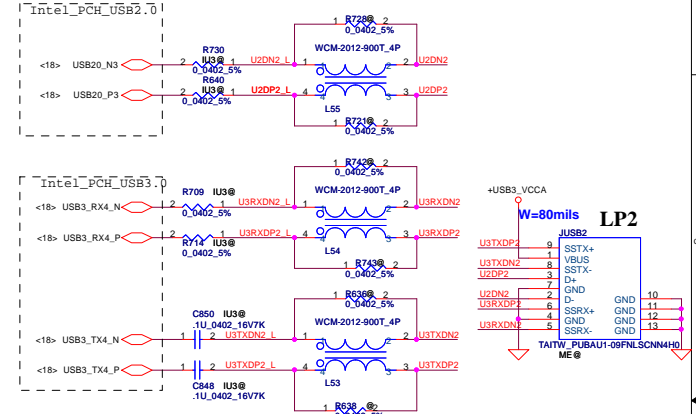
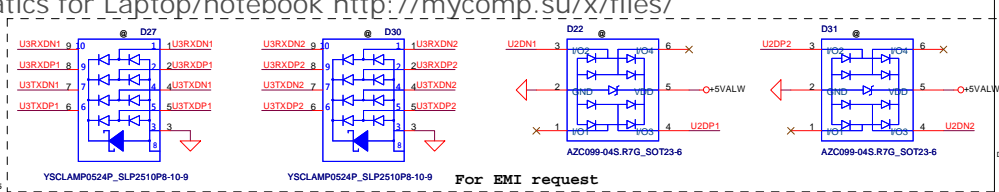
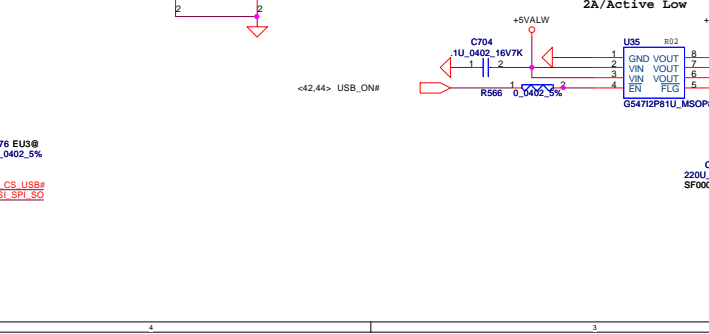
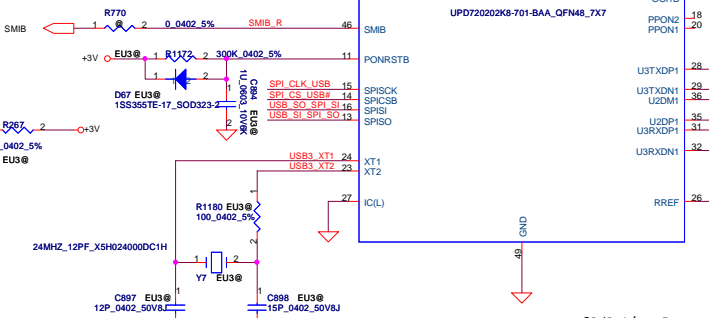
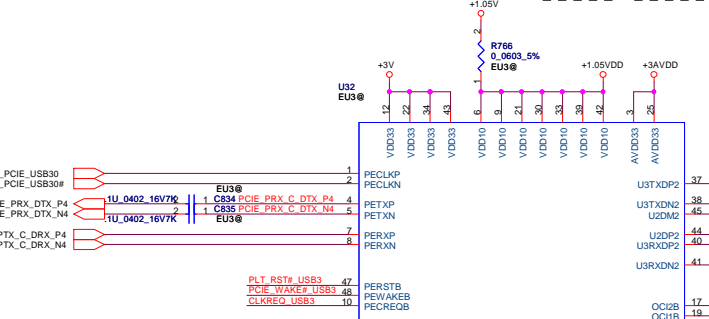
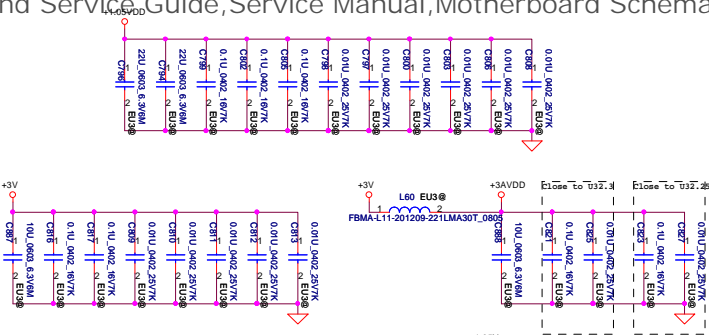
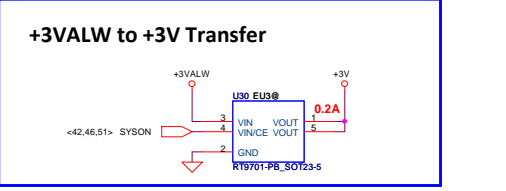
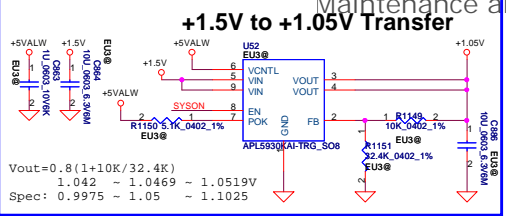


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Size C	Document Number	LA-7981P		Rev	0.2
Date:		Tuesday, February 14, 2012	Sheet	43	of 60

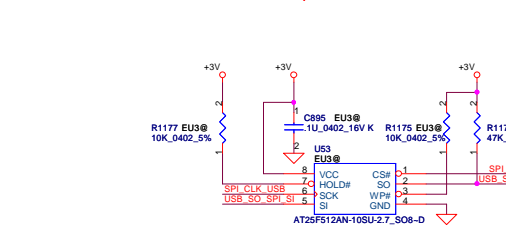
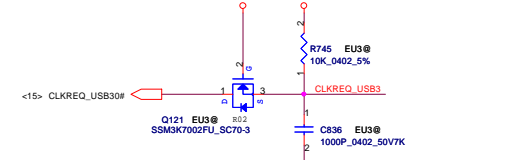
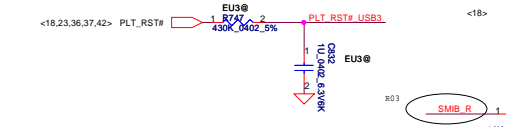
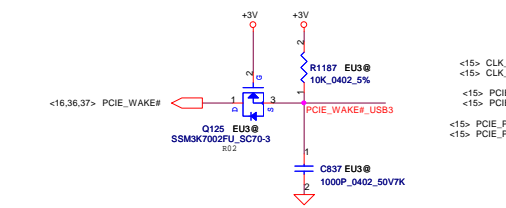
### Right Ext.USB Conn.



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				Size B	Document Number	Rev
				Date:	Tuesday, February 14, 2012	Sheet 44 of 60

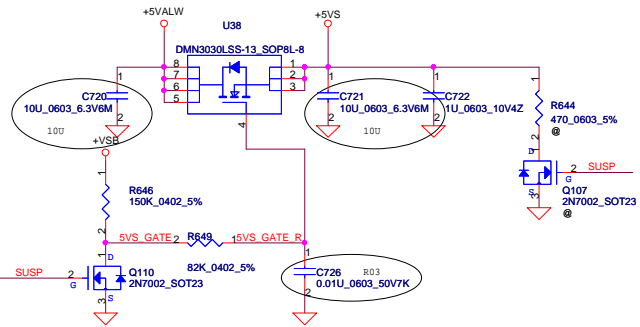


Place TX AC coupling Cap (C843-C850). Close to connector

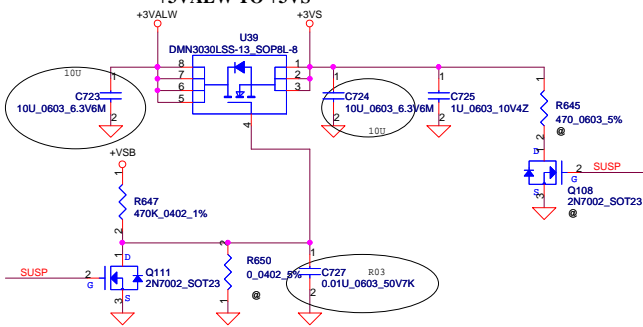


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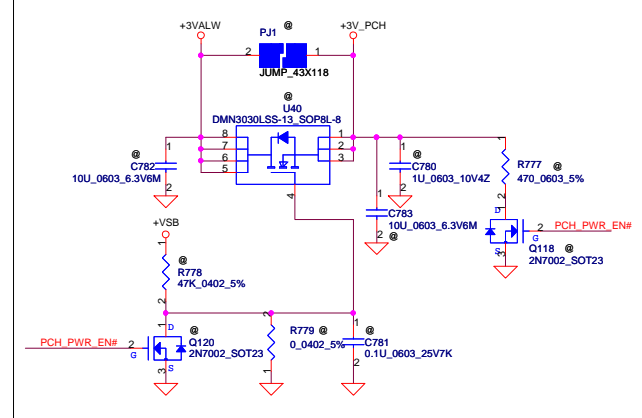
**+5VALW TO +5VS**



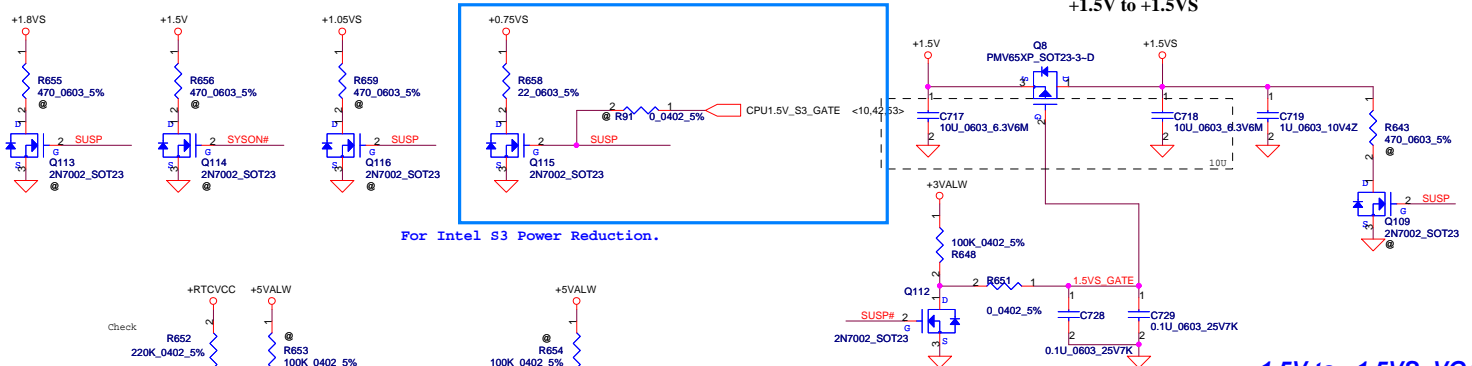
**+3VALW TO +3VS**



**+3VALW TO +3VALW(PCH AUX Power)**

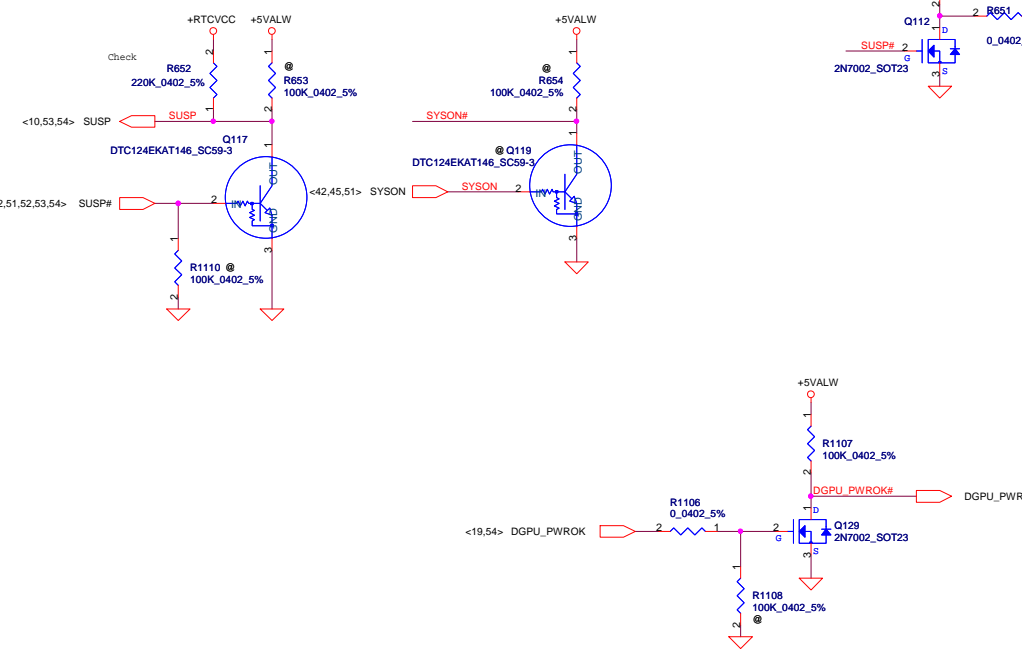
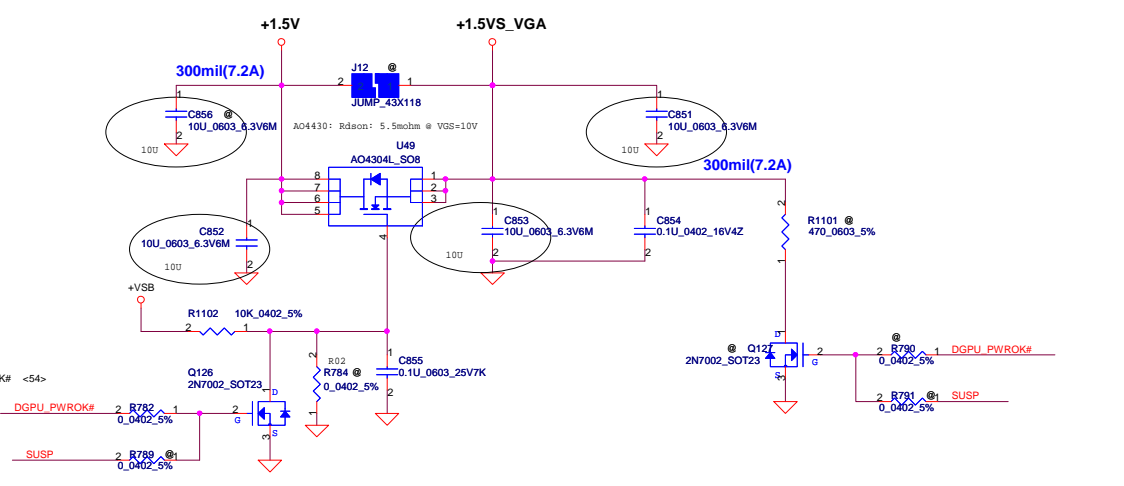


**+1.5V to +1.5VS**



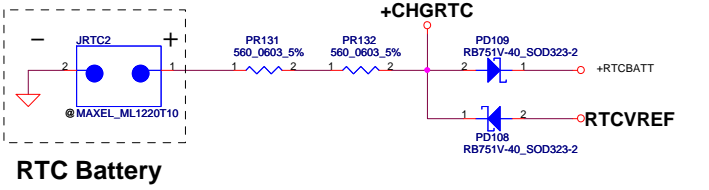
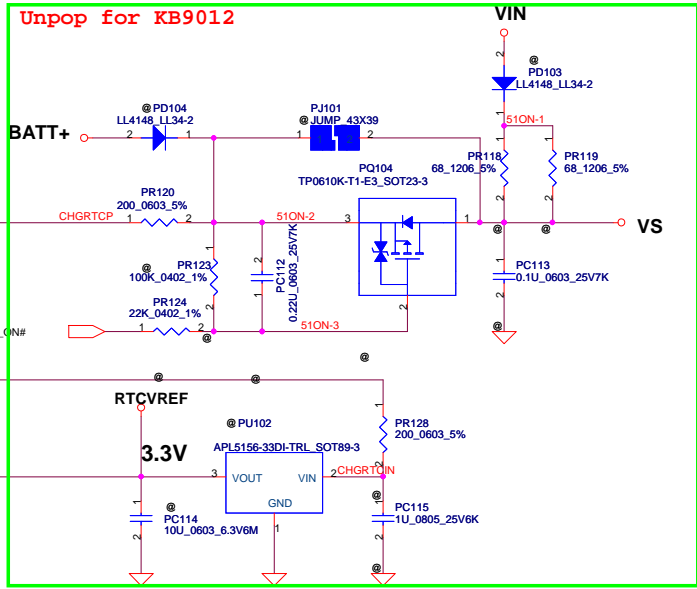
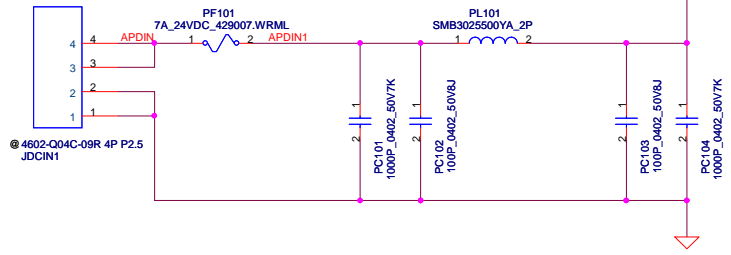
For Intel S3 Power Reduction.

**+1.5V to +1.5VS\_VGA Transfer**



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				LA-7981P	0.2
				Date: Tuesday, February 14, 2012	Sheet 46 of 60

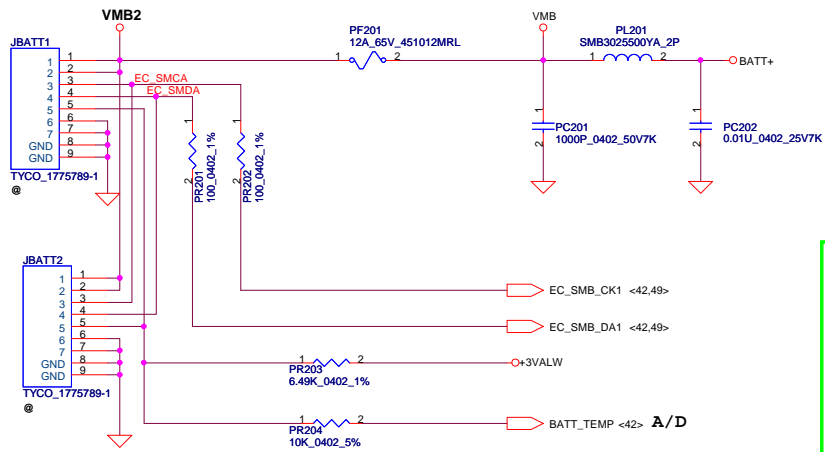
**DC030006J00**



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Compal Electronics, Inc.			
Title: <b>PWR DCIN / Vin Detector /Pre-charge</b>			
Size	Document Number	Rev	
Custom	<b>C38-G series Chief River Schematic</b>	0.1	
Date:	Tuesday, February 14, 2012	Sheet	47 of 60





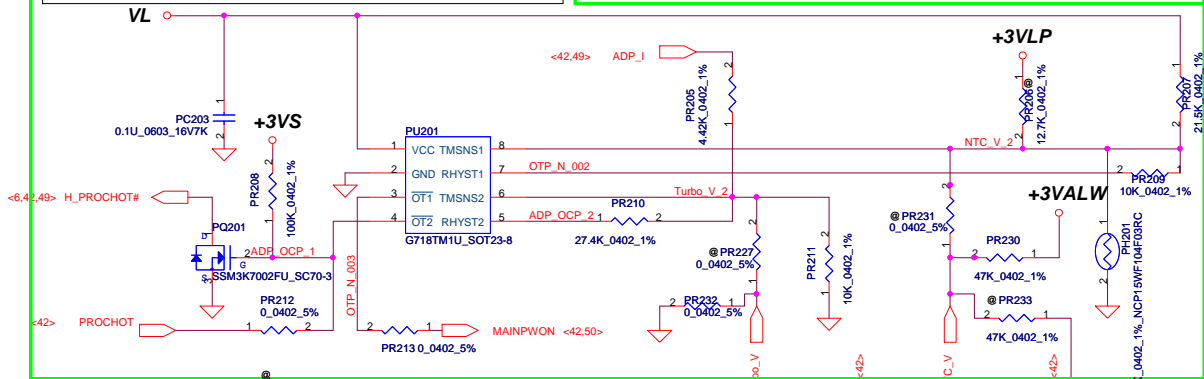
ADP\_I need to write Charge Options Register (0x12H)=> bit6=1

0: IOUT is the 20x current amplifier output <default @ POR>

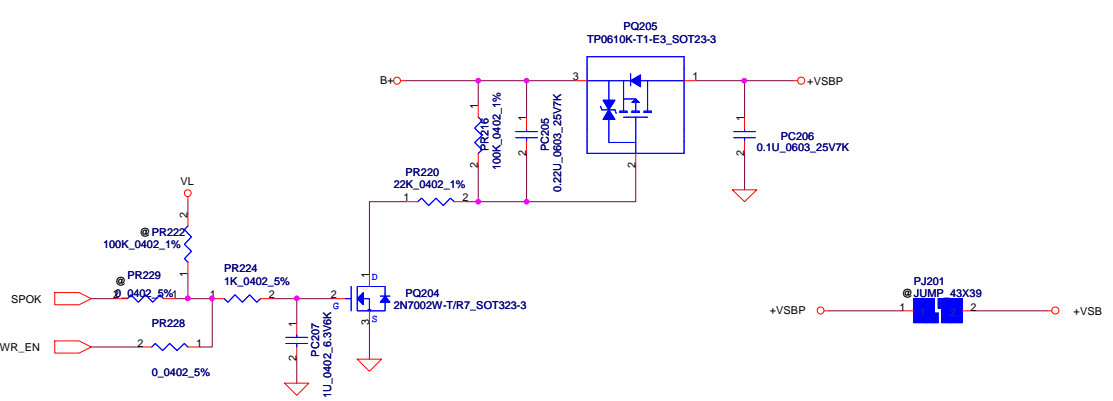
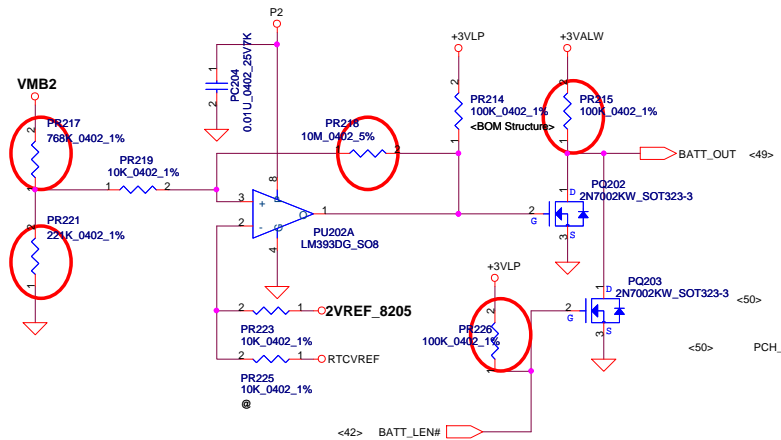
1: IOUT is the 40x current amplifier output

**PH1 under CPU bottom side :**  
**CPU thermal protection at 93 +-3 degree C**  
**Recovery at 56 +-3 degree C**

**For KB930 --> Keep PU201 circuit (Vth = 1.25V)**  
**For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206, PH201, PR205, PR211, PQ201, PR208, PR212**

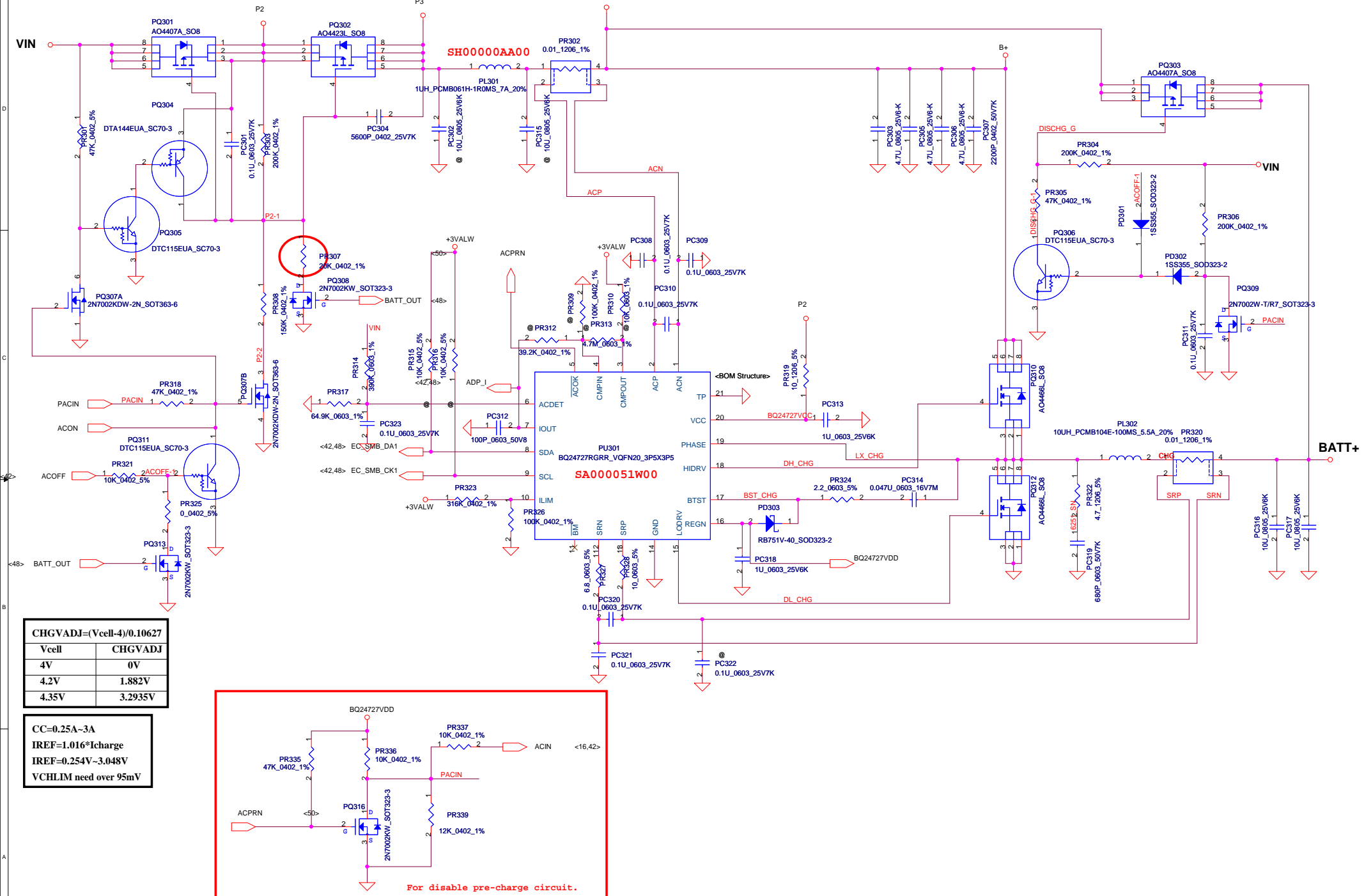


**90W(DIS) : PR205=4.42K**  
**PR210=27.4K**  
**65W(UMA) : PR205=402(SD034020080)**  
**PR210=5.11K**



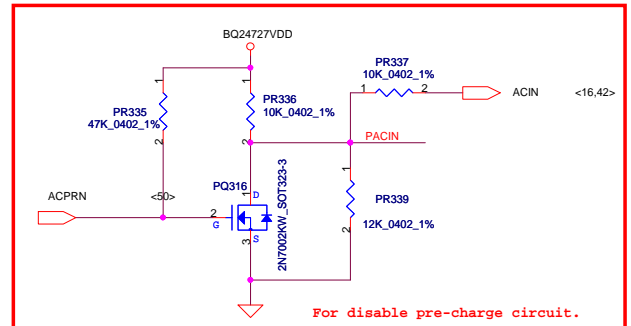
Security Classification	Compal Secret Data	
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Compal Electronics, Inc.		
Title <b>PWR-BATTERY CONN/OTP</b>		
Size	Document Number	Rev
Custom	<b>C38-G series Chief River Schematic</b>	0.1
Date:	Tuesday, February 14, 2012	Sheet 48 of 60



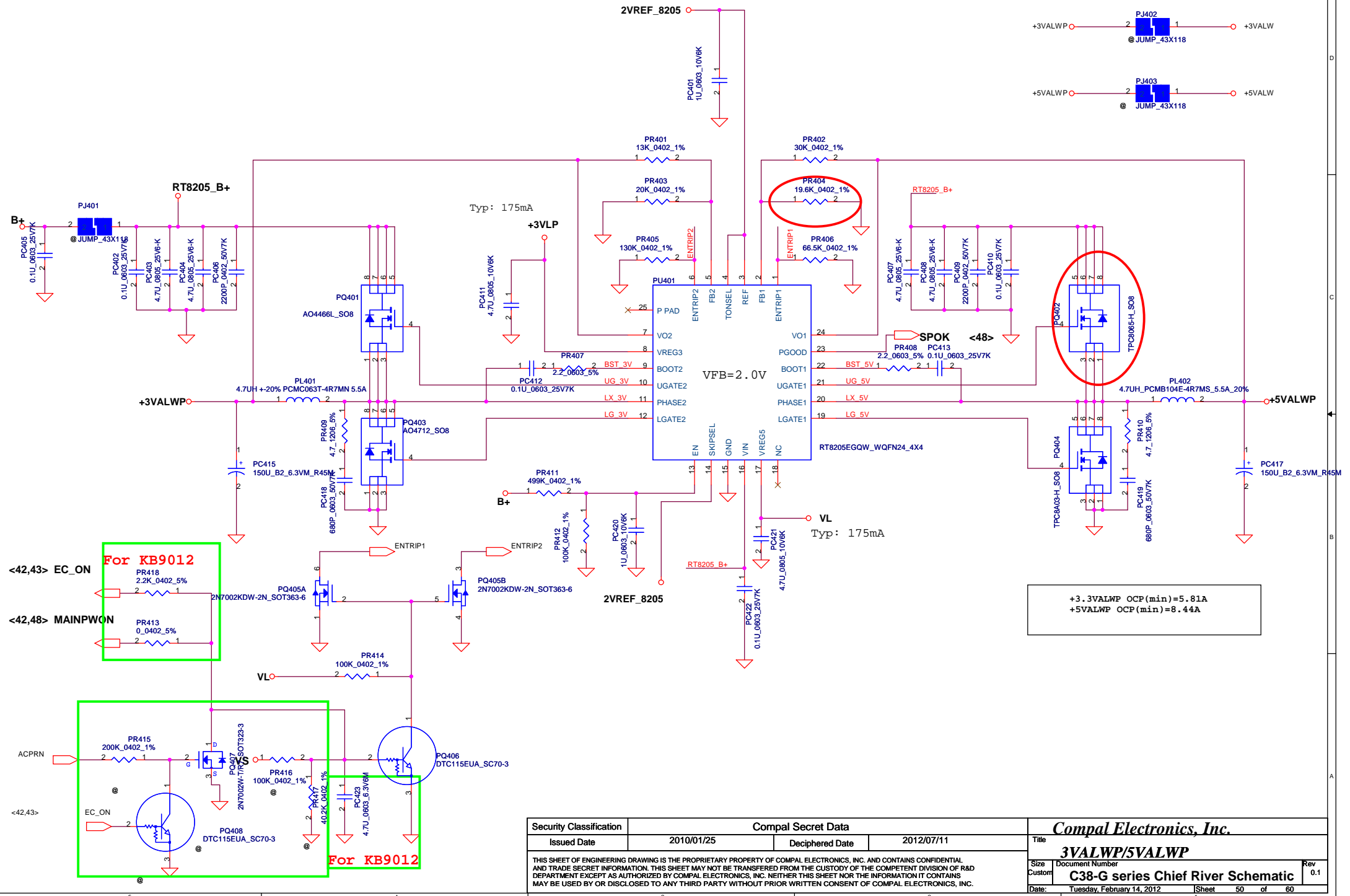
<b>CHGVADJ=(Vcell-4)/0.10627</b>	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

**CC=0.25A-3A**  
**IREF=1.016\*Icharge**  
**IREF=0.254V-3.048V**  
**VCHLIM need over 95mV**



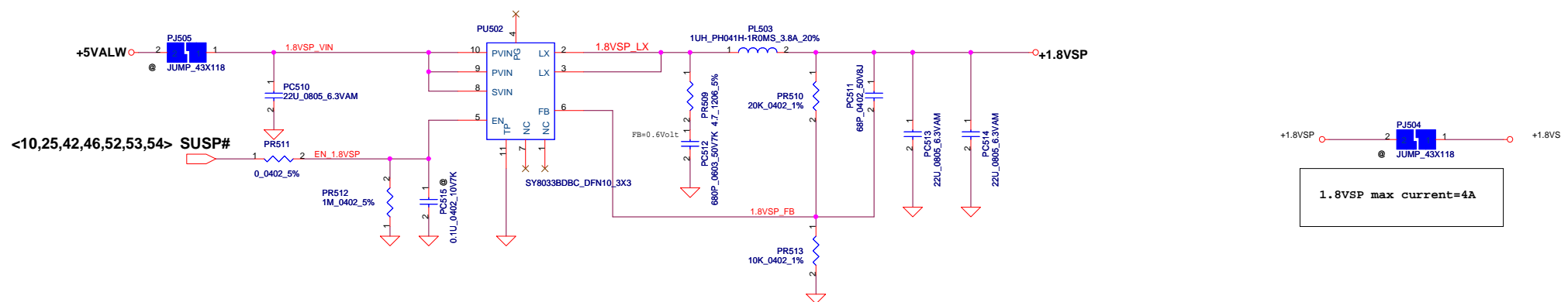
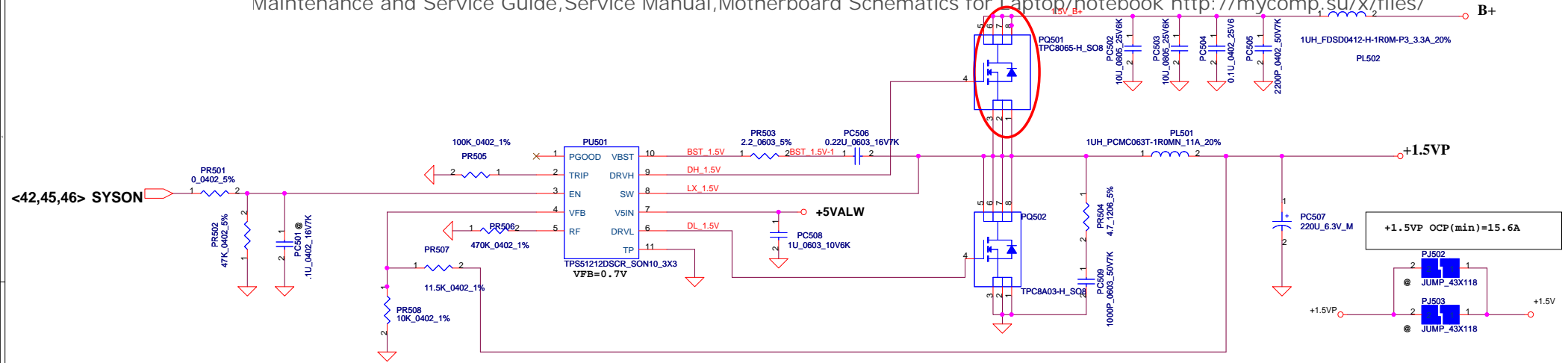
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/13	Deciphered Date	2012/07/11	Title	
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Note:  
 Use TPS51125 IC can remove RTC referenece LDO  
 Use TPS51427 IC must keep RTC referenece LDO



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<b>Compal Electronics, Inc.</b>		
Title	<b>3VALWP/5VALWP</b>	
Size	Document Number	Rev
Custom	<b>C38-G series Chief River Schematic</b>	0.1
Date:	Tuesday, February 14, 2012	Sheet 50 of 60



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Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	<b>PWR-+1.5VP/+1.8VSP</b>
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Size	Custom	Document Number	C38-G series Chief River Schematic		Rev 0.1
Date:	Tuesday, February 14, 2012	Sheet	51	of	60

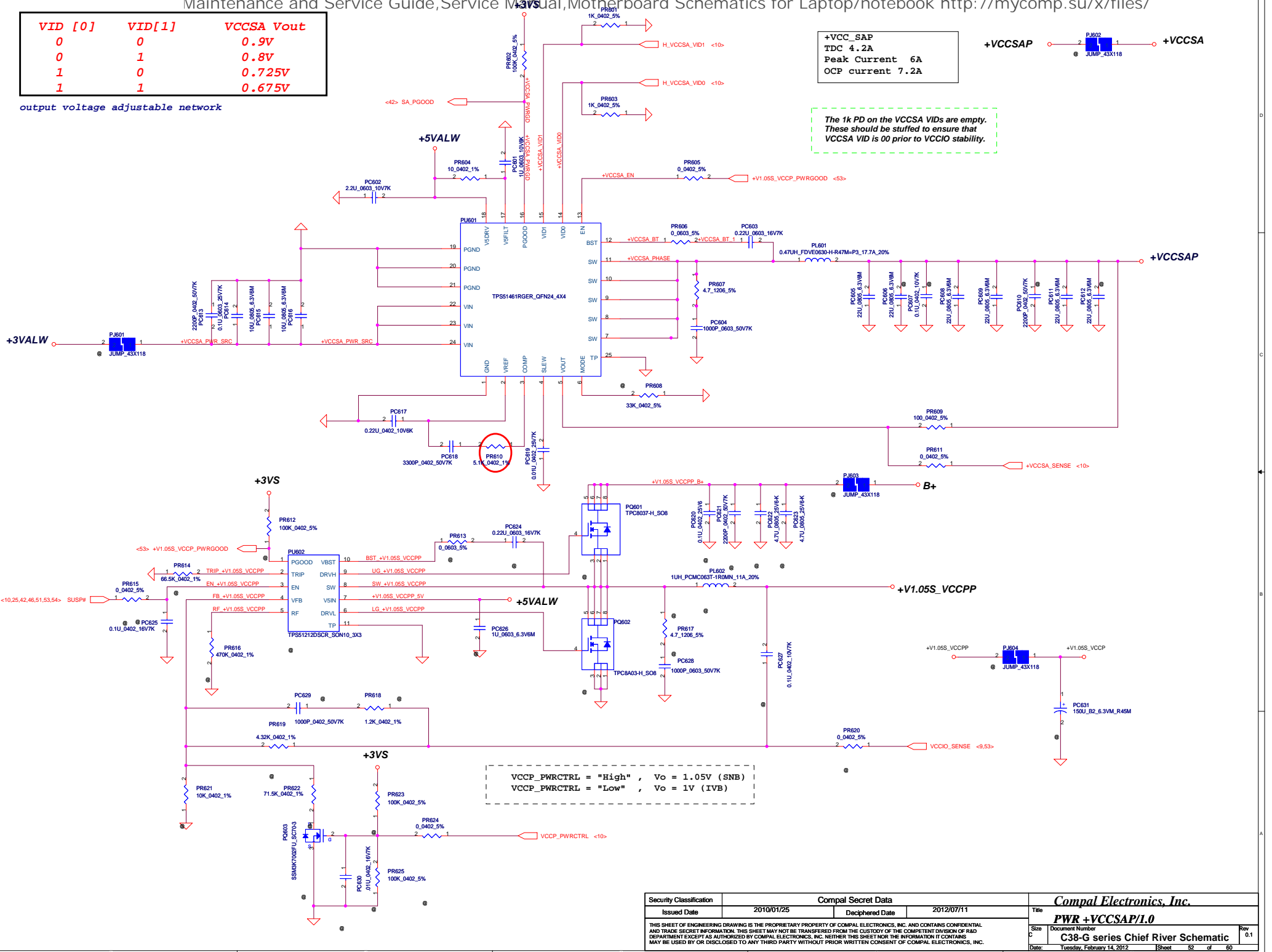
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

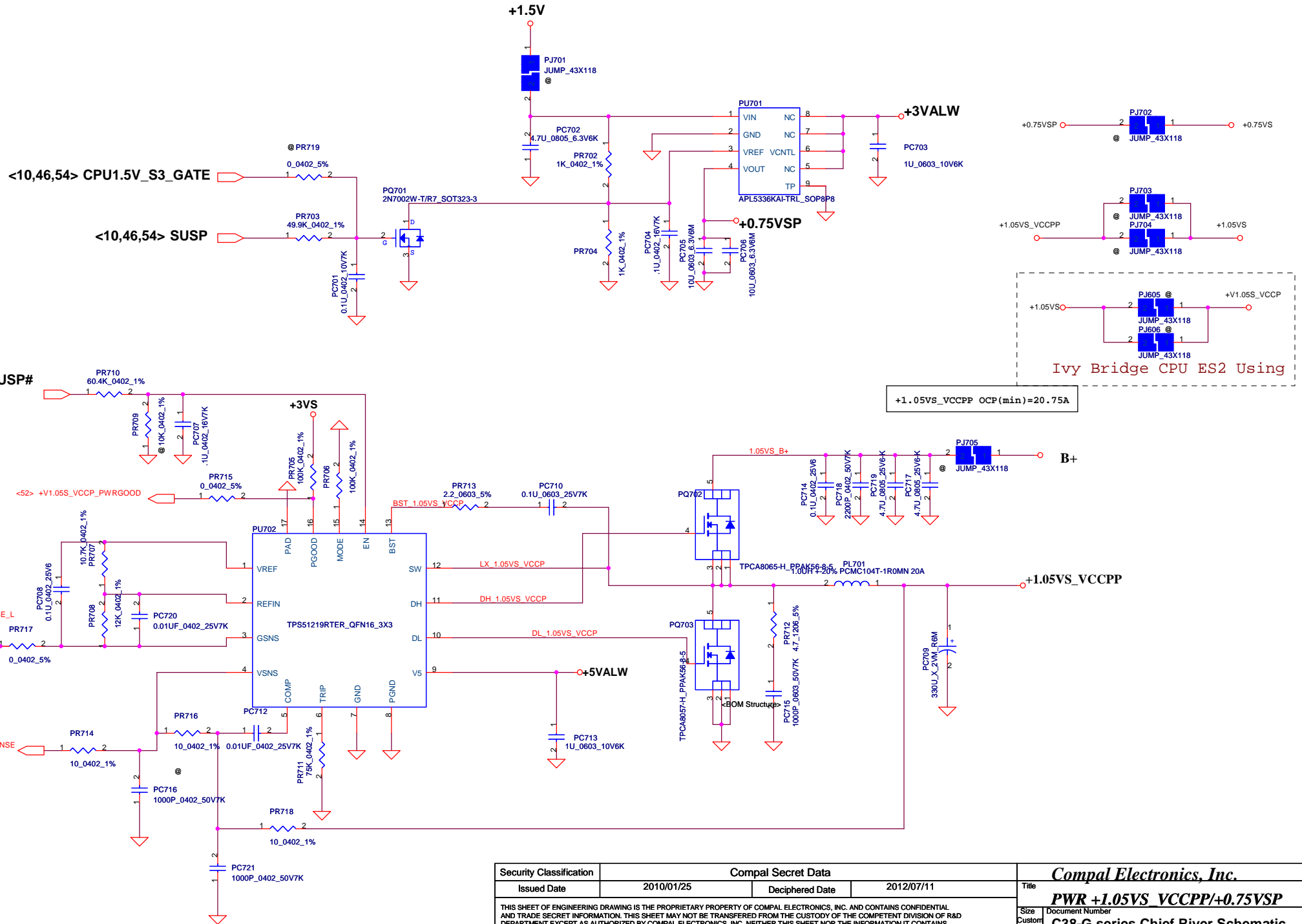
+VCC\_SAP  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A

+VCCSAP JUMP\_43X118 +VCCSA

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



VCCP\_PWRCTRL = "High" , Vo = 1.05V (SNB)  
VCCP\_PWRCTRL = "Low" , Vo = 1V (IVB)

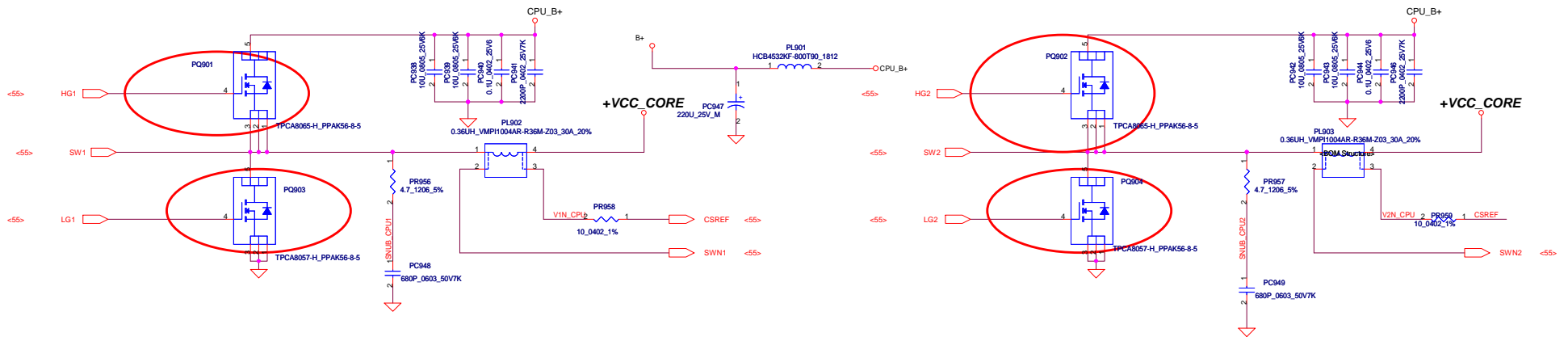


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				Custom	0.1
				Date: Tuesday, February 14, 2012	
				Sheet 53 of 60	



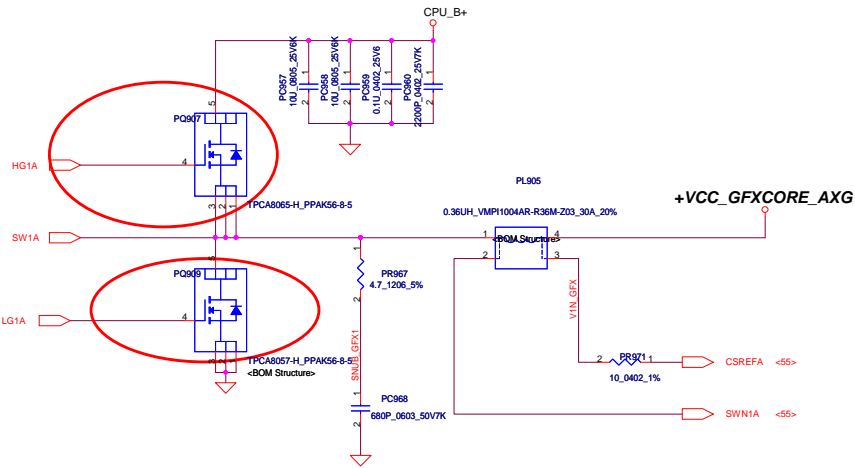






QC 45W CPU  
 VID1=0.9V  
 IccMax=94A  
 Icc\_Dyn=66A  
 Icc\_TDC=52A  
 R\_LL=1.9m ohm  
 OCP-110A

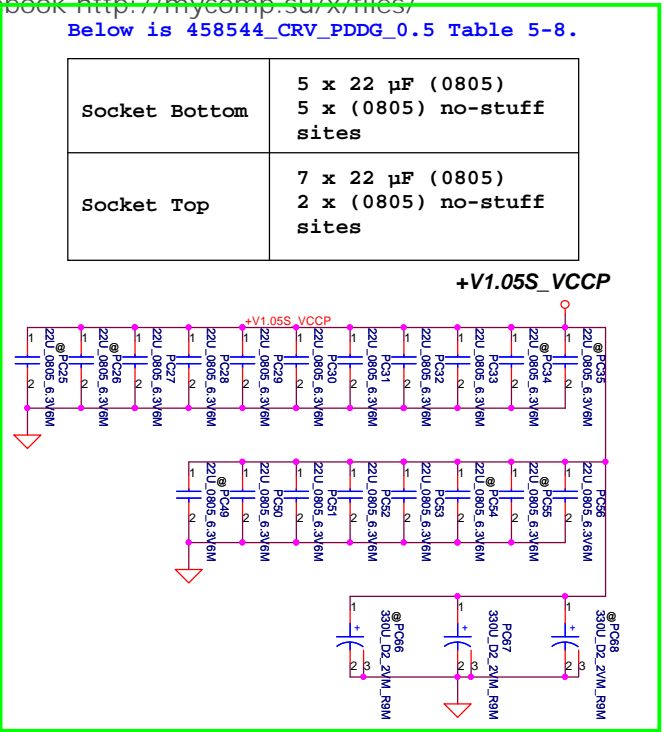
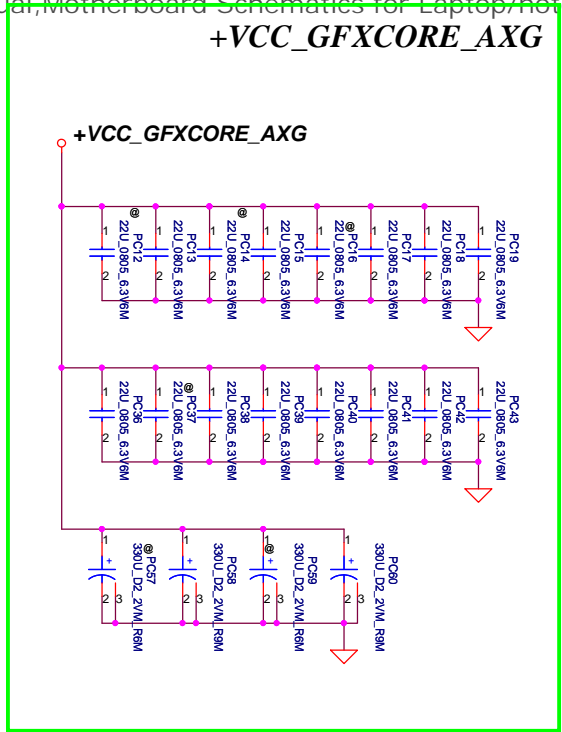
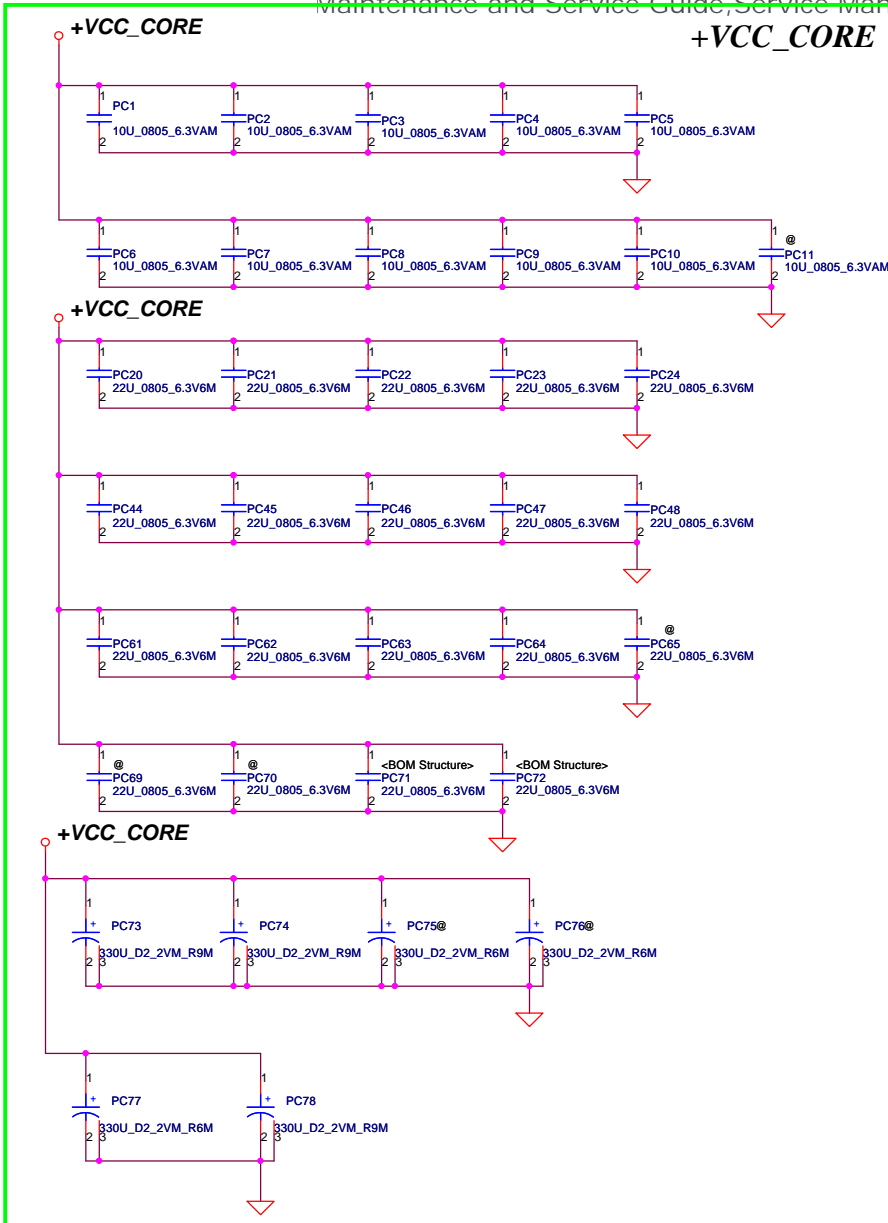
DC 35W CPU  
 VID1=1.05V  
 IccMax=53A  
 Icc\_Dyn=43A  
 Icc\_TDC=36A  
 R\_LL=1.9m ohm  
 OCP-65A



QC 45W GT2  
 VID1=1.23V  
 IccMax=46A  
 Icc\_Dyn=37A  
 Icc\_TDC=38A  
 R\_LL=3.9m ohm  
 OCP-55A

DC 35W GT2  
 VID1=1.23V  
 IccMax=33A  
 Icc\_Dyn=20.2A  
 Icc\_TDC=21.5A  
 R\_LL=3.9m ohm  
 OCP-40A

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Date: Tuesday, February 14, 2012			Sheet 56 of 60	Rev 0.1



Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites

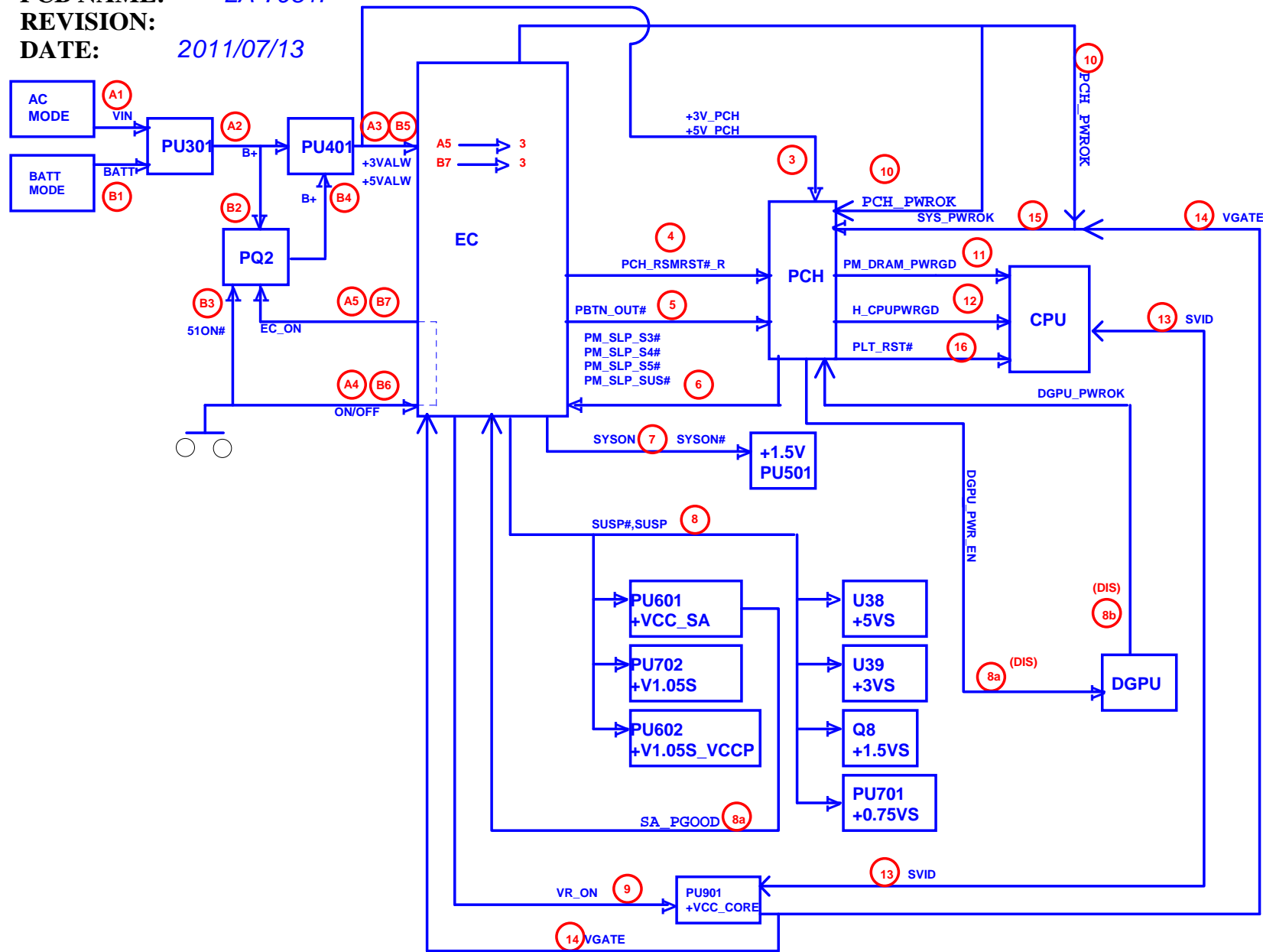
**Version change list (P.I.R. List)**

Item	Reason for change	PG#	Modify List	Date	Phase
1	add PR865 for ISL62883 one phase solution and unpop for two phase solution.	P54	add PR865	2011.08.29	DVT
2	unpop PR315,PR316 for SMBus SPEC.	P49	unpop PR315,PR316	2011.08.29	DVT
3	delet PSI#_VGA for NV chip.	P54		2011.10.14	DVT2
4	change NTC_V pull high voltage from +3VLP to +3VALW	P48			
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Size	Document Number
Custom	C38-G series Chief River Schematic	0.1			
Date:	Tuesday, February 14, 2012	Sheet	58	of	60

# COMPAL CONFIDENTIAL

**MODEL NAME:** *Power Sequence Block Diagram*  
**PCB NAME:** *LA-7981P*  
**REVISION:**  
**DATE:** *2011/07/13*



Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Compal Electronics, Inc.
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Size	Document Number	Rev		
Custom	LA-7981P	0.2		
Date:	Tuesday, February 14, 2012	Sheet	59	of 60

**Version change list (P.I.R. List)**

Item	Reason for change	PG#	Modify List	Date	Phase
1	GPU 13M GPU Device loss (Pcie lan x8 issue)	8	Add R43		DVT
2	HDD no function	40	Add R550		DVT
3	10/100 lan no function & change to overclocking mode	37	ADD R1372 ; DEL R31		DVT
4	For DGPU_PWROK leakage issue.(Let timing +5VS > +3VS)	46	Change C726 from 0.1uF to 0.01uF		DVT
5	For S3 can't wake up	10	Change R56 from 15K to 4.7K change R885 from 0 ohm to 15K		DVT
6	Can unstuff RV66 for N13P-GL & as NV DG	27	RV66 change to N13M@		DVT
7	GPU N13P-GL QS sample change strap	32	RV94 change from 45.3K to 10K		DVT
8	PCH 25Mhz for vender crystal test report change CL to 12pF	15	C196;C197		DVT
9	GPU 27Mhz for vender crystal test report change CL to 15pF	23	CV37;CV38		DVT
10	EC_LID_OUT# internal PD 20K, follow ORB change R230 from 10k to 1K	19	R230		DVT
11	For GPIO70;GPIO71 voltage level issue ( internal Pull High 20k )	19	R705;R706 Change from 10K to 200K		DVT
12	for DVT board ID Change R695 from 33k to 18k	42	R695		DVT
13	LAN Surge test fail change P/N from SP050006E00 to SP050006W00	27	T1;T2		DVT
14	Del ODD Power Control function component	40	R568;Q100;R675;C607;Q99		DVT
15	AO4430L(SB000007010)EOL Change to AO4304 (SB00000RV00)	46	U49		DVT
16	Del (PCH AUX Power) Reserve component no use	46	C780;C781;C782;C783;R778;Q120;U40		DVT
17	PCH(U4) P/N Change from SA00004NQ30 to SA00004NQ80	14	U4		DVT
18	NV-GPU (U65)P/N change N13M from SA00004V000 to SA00004V010 N13P Keep SA000051A00	23	U65		DVT
19	EXT USB 3.0 IC PCIE_WAKE# ; CLKREQ_USB30# leakage on S4	45	Swap Q125;Q121 pin1 & pin3		DVT
20	No function	45	DEL R769		DVT
21	add LAN LDO mode function	37;38	ADD R65;R596;R1449;R1380		DVT
22	USB_OC0# Share with USB_OC4# due to same power switch	18	short USB_OC0#;USB_OC4# ; del R267		DVT
23	Add Capsensor B/D Conn. For best buy use	42	ADD JCAP1 Conn.		DVT

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				Size	Document Number
				Date: Tuesday, February 14, 2012 Sheet 60 of 60	

## Version change list (P.I.R. List)

Page 2 of 2 for HW PIR

Item	Reason for change	PG#	Modify List	Date	Phase
24	L1 change to 1 ohm R	20	L1 change to R footprint		DVT
25	Reserve 0 ohm for CMOS Camera shake	33	add R296 0 ohm		DVT
26	Reserve 0 ohm for U49 MOS VGS 20V will burn out issue	46	add R784 0 ohm		DVT
27	For HDD +5VS Power plant del C601; change C598 pin1 power name for good power plant	40	change from +5VS to +5V_HDD ;DEL C601		DVT
28	For Audio jack support APPLE and NOKIA function Reserve	43	add R684;R685;R688;R686 0ohm R		DVT
29	For standard part cost down change 10uF 0805 type to 0603 type	10, 20 21, 33 37, 39 40, 46	C124;C125;C126;C127;C130;C221;C215;C395; C231;C519;C937;C953;C954;C591;C608;C602; C720;C721;C723;C724;C782;C783;C717;C718; C856;C852;C851;C853		DVT
30	change Crystal foot print follow standard parts from 5032 to 3225 package	15;23; 37	Y2;Y6;YV1		DVT
31	change 0ohm to short-pad (R0402_0ohm)	7;8; 10;15 16;20; 33;36; 40;43	R40;R60;R77;R144;R190;R193;R198;R181;R185; R265;R538;R498;R500;R583;R614		DVT
32	Reserve BT_DISABLE (GPI022) for combo card(BT+WLAN)	19	ADD R892;R897		DVT
33	U35;U36 Change footprint without thermal PAD type	44;45	U35;U36		DVT
34	PU 10K with 3V3 on N13P-GL/ for CEC signal	24	RV230		DVT
35	VGA_GPIO3;VGA_GPIO16 change connect DPRSLPVR_VGA to PSI#_VGA	23;54	RV113;RV114		DVT
36	Fix VGA power on CLKREQ has drop (QV2 gate add 0.1uF)	23	CV42		DVT
37	LED5 和LED2 Location sawp ; Location name D9 change to LED6	43	LED2;LED5;LED6		DVT
38	For Lan surge fail add 0 ohm on MDO2-;MDO2+;MDO3-;MDO3+	38	R304;R305;R306;R307		DVT
39	Change UV2 PN from SA007080B90 to SA000000H00	23	UV2	09/28	DVT
40	Change 2M BIOS ROM from SA00003FO00 to SA00003FO10	14	U6	09/29	DVT
41	Correct PCIE_PRX_DTX_P4/N4 of U32 (SWAP)	45	U32	10/03	DVT
42	Reserve +5VS to JCR1, add R689 ,R690	43	R689 (@),R690	10/03	DVT
43	Update Power sheet of 1003 version	47~58		10/04	

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				Custom	LA-7981P
				Date	Tuesday, February 14, 2012
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**Version change list (P.I.R. List)**

Item	Reason for change	PG#	Modify List	Date	Phase
44	CPU Symbol Update	5,6,7, 8,9,10,11	Location : Jcpul		PVT
45	Change 10P 50V Cap from 1206 to 0603	38	Location : C973		PVT
46	S3 Reduction	53	Reserve PR719 for 0.75V		PVT
47	LAN CO-lay x1 GDT & 75ohm	38	Location : R308,R304,R305,R306,R307,DL1,DL2,DL3,DL4		PVT
48	R750 for Power request	42	Location :R750		PVT
49	JUSB3 From 4PIN TO 6 PIN FOR VOLTAGE DROP	44	Location : JUSB3		PVT
50	Add C535 100pF on +3VLP for ESD request - Pony	42	Location : C535		PVT
51	FOR TP POWER SOLUTION	42	Location : R598.R603		PVT2
52	FOR POWER REQUEST	42	Location : R738		PVT2
52	Change C from 0.22uF to 0.11uF	5 23	Location : C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, CV6, CV7, CV8, CV9, CV10, CV11, CV12, CV13, CV15, CV17, CV19, CV14, CV16, CV18, CV20, CV22, CV24, CV26, CV21, CV23, CV25, CV27, CV29, CV31, CV33, CV28, CV30, CV32, CV36, CV41, CV34, CV35,		SVT

Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	<b>Compal Electronics, Inc.</b>	
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