

Compal Confidential

Model Name : V5WE2/T2/C2 (EA/EG/BA50_HW)

File Name : LA-9531P

Compal Confidential

EA50_HW M/B Schematics Document

Intel Shark Bay ULT (Hasswell + Lynx Point-LP)

AMD MARS / SUN

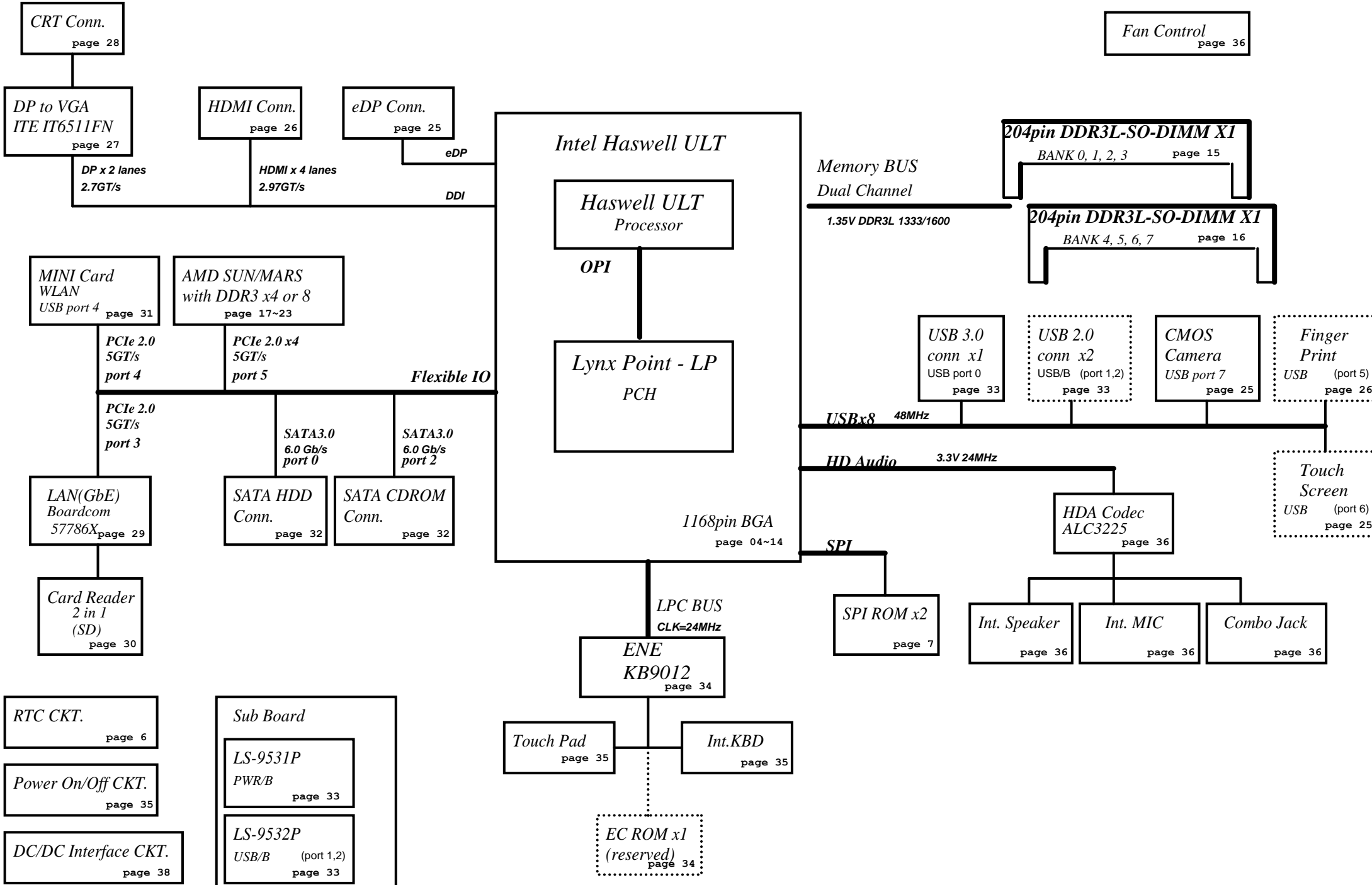
2013-04-11

REV: 1.0

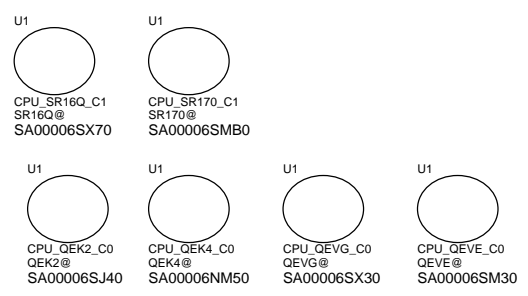
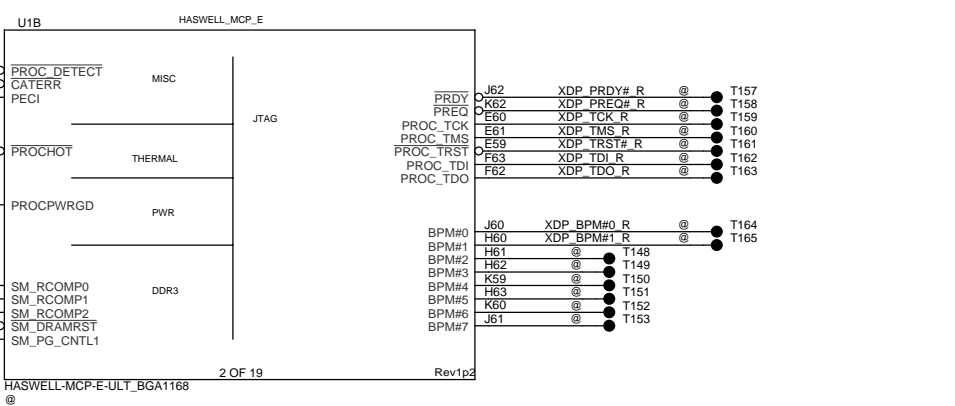
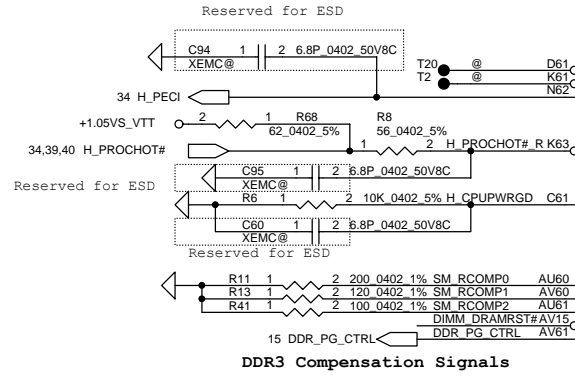
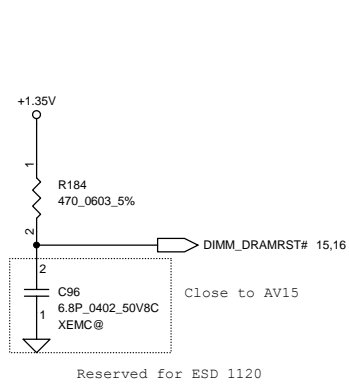
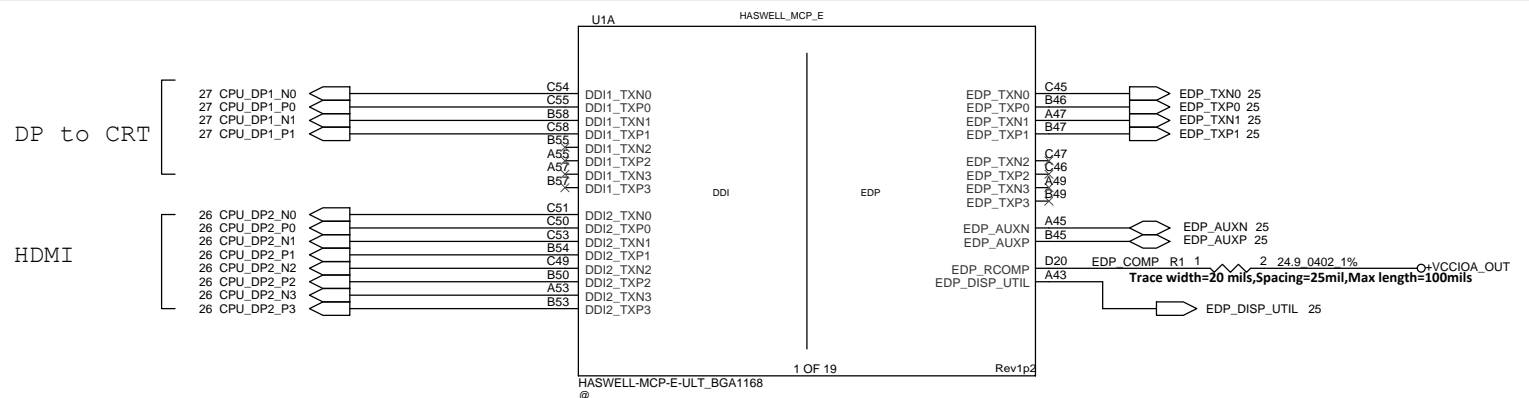
ZZZ

Part Number	Description
DAZ0VR00100 V5WE2_PCB	PCB V5WE2 LA-9531P LS-9531P/9532P

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title
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				1.0
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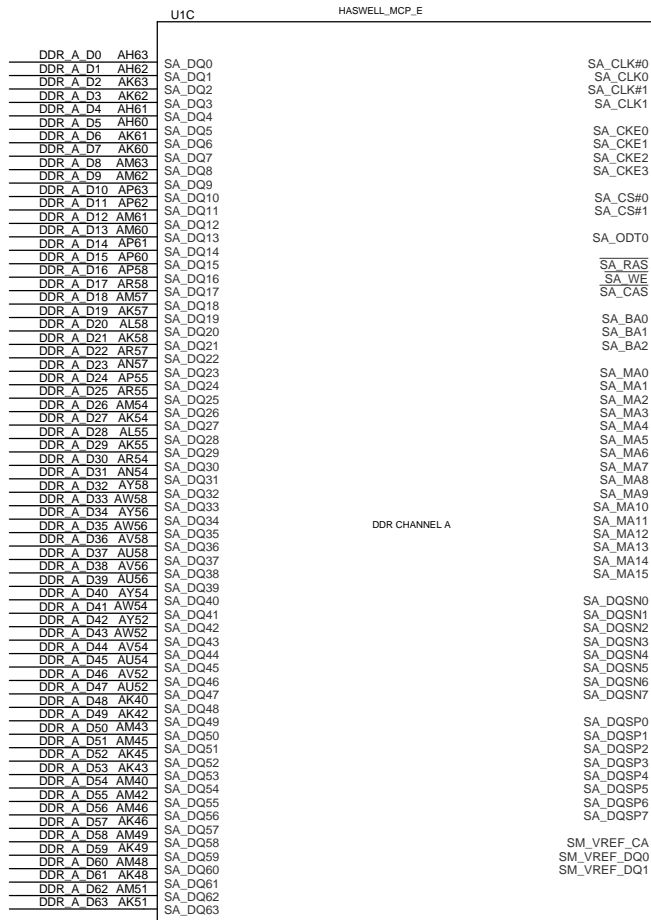


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				V5WE2 M/B LA-9531P Schematic	1.0
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Issued Date		2012/07/10	Deciphered Date	2013/07/10	Title
					HSW MCP(1/11) DDI,MSIC,XDP
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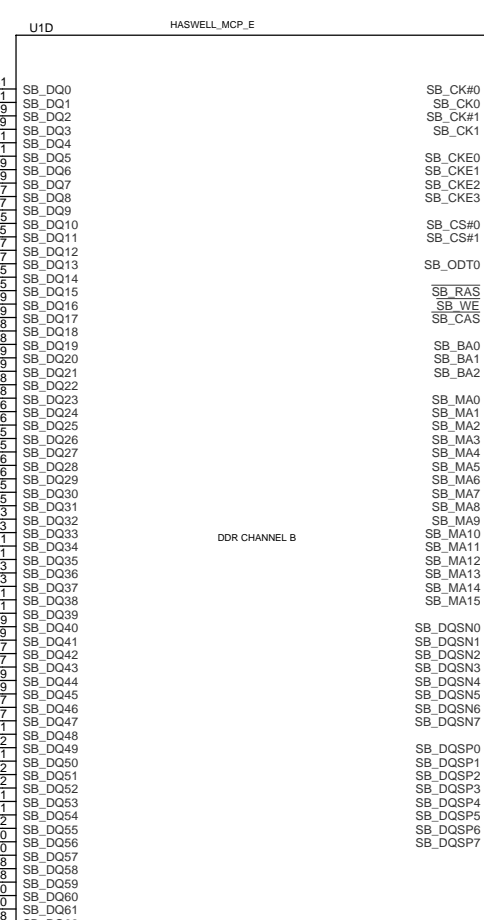
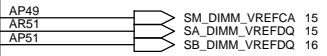
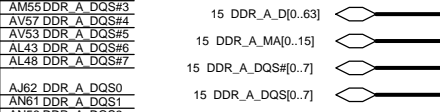
Document Number: **V5WE2 M/B LA-9531P Schematic**
 Rev: 1.0



HASWELL-MCP-E-ULT_BGA1168

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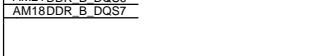
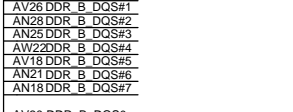
Rev1p2



HASWELL-MCP-E-ULT_BGA1168

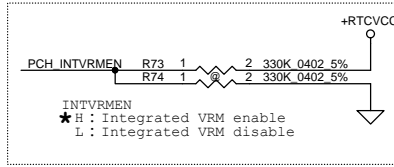
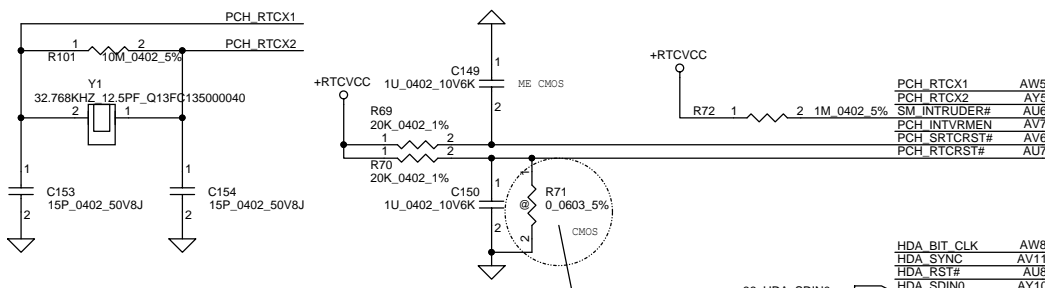
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Rev1p2

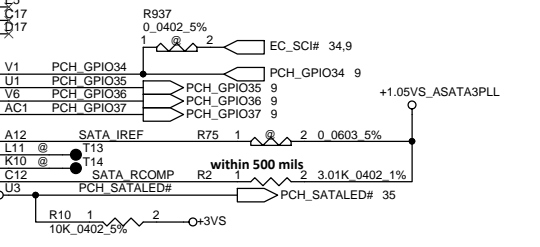
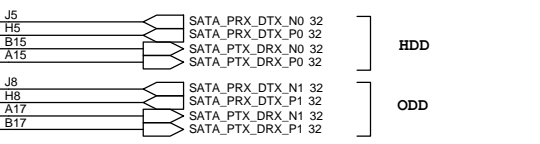
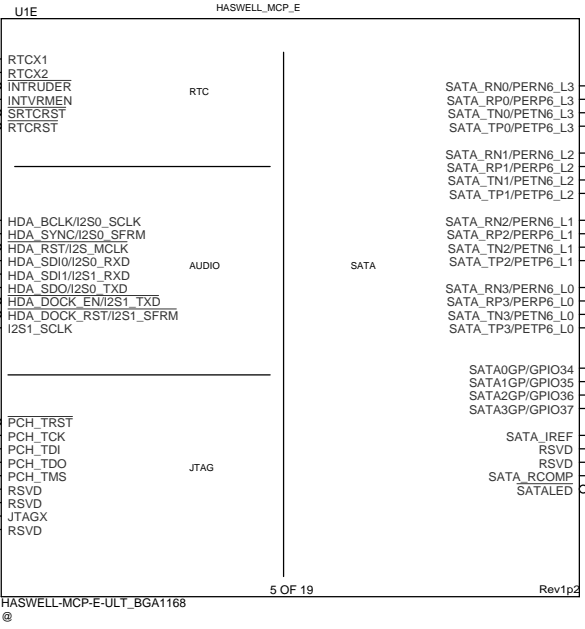
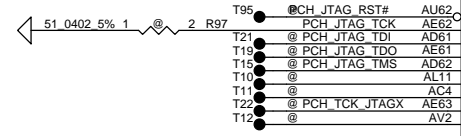
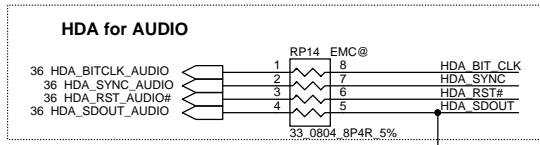


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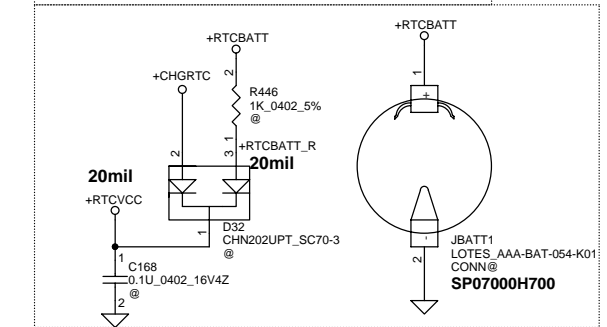
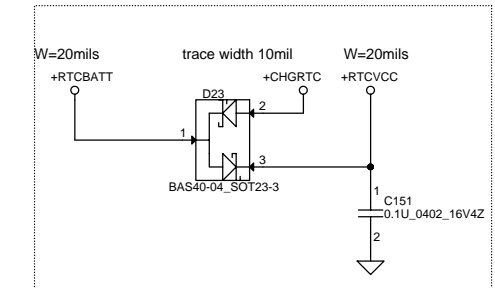
Document Number
V5WE2 M/B LA-9531P Schematic
Rev 1.0

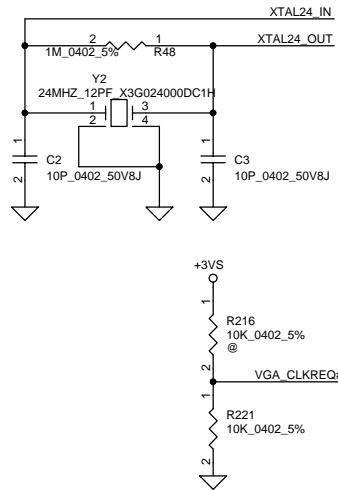


RTCRST close RAM door

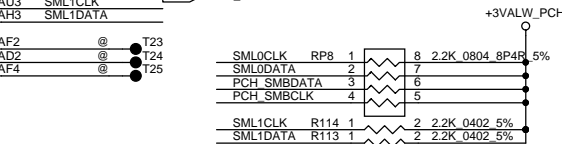
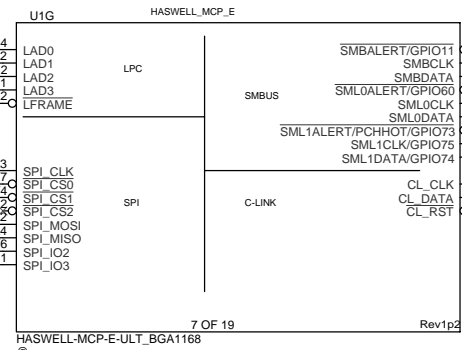
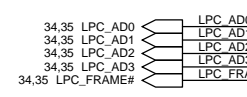
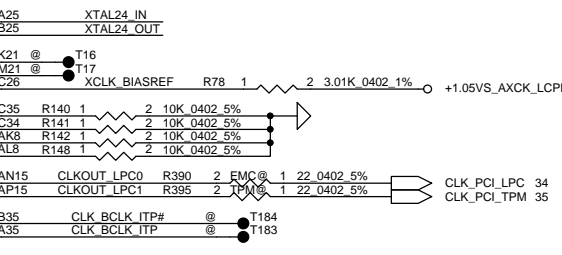
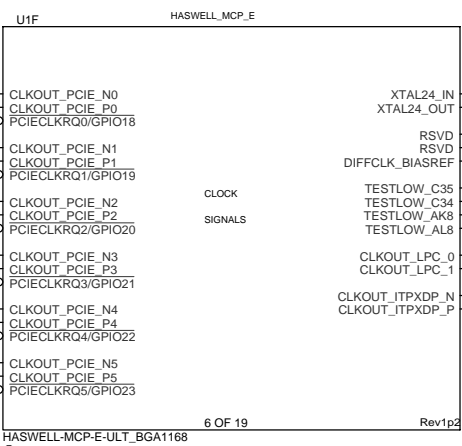
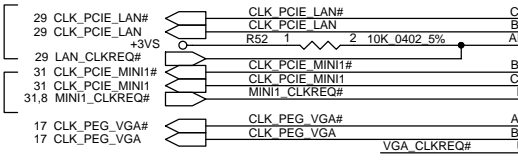


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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title HSW MCP(3/11) RTC,SATA,XDP	
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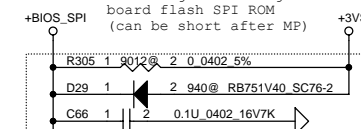




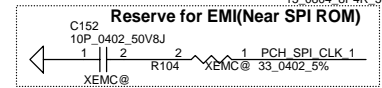
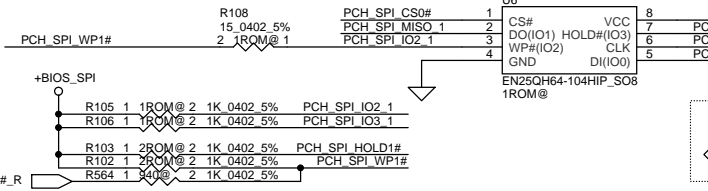
PCIE LAN
WLAN



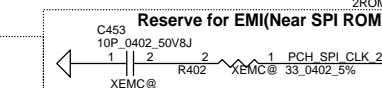
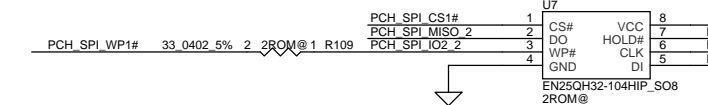
D29 design for Debug board flash SPI ROM (can be short after MP)



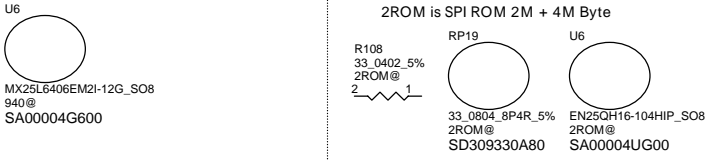
SPI ROM (8MByte)



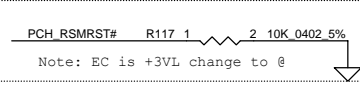
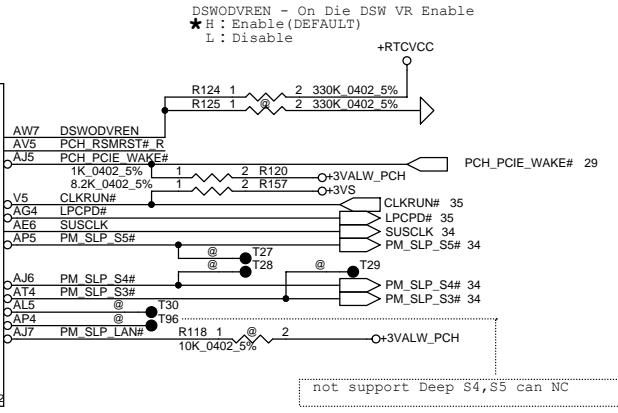
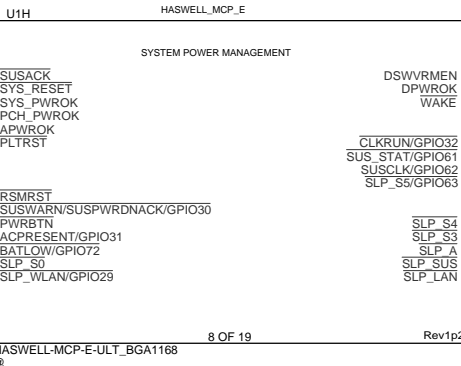
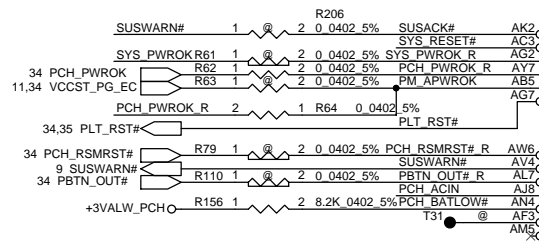
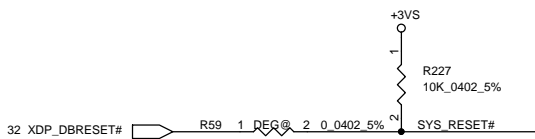
SPI ROM (4MByte)



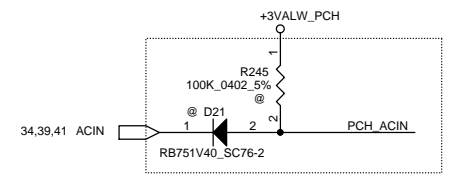
SPI ROM (8MByte for Chrome)



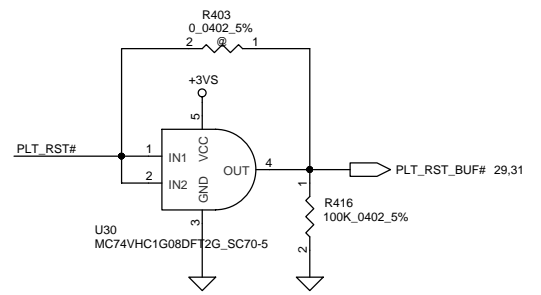
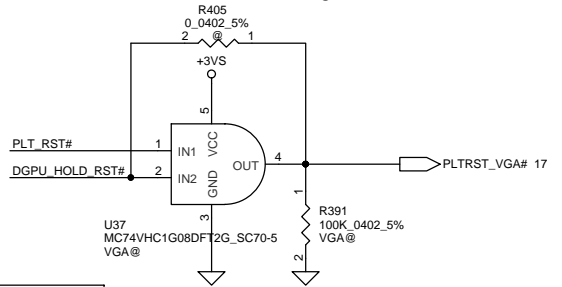
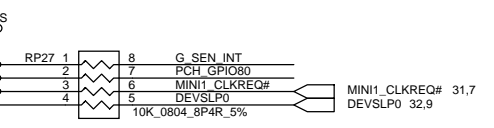
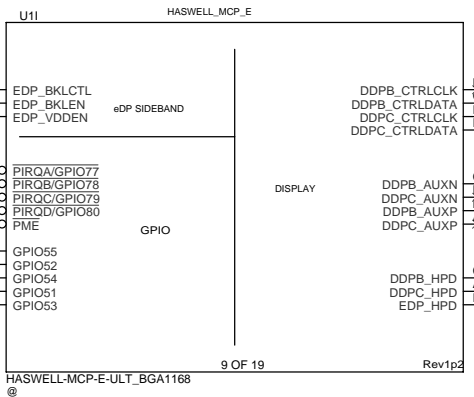
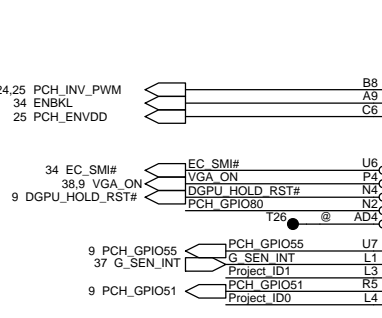
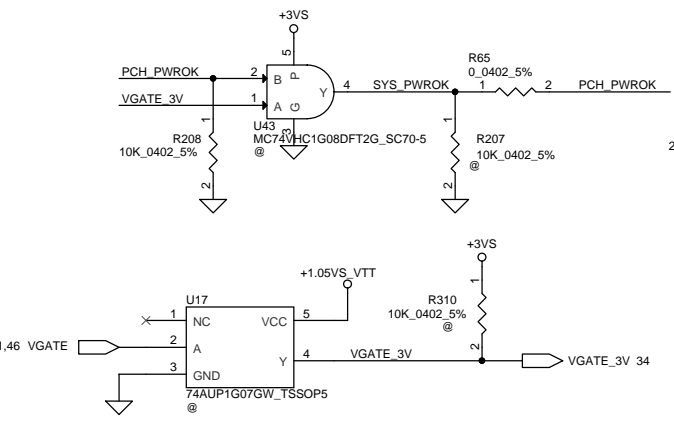
Security Classification		Compal Secret Data		Title	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Compal Electronics, Inc. HSW MCP(4/11) CLK,SPI,SMBUS	
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Note: Deep Sx need use EC GPIO for ACPRESENT function



DDPB_CTRLCLK: Port B Detected
 DDPB_CTRLDATA: Port C Detected
 * 1: Port B or C is detected
 0: Port B or C is not detected
 (Have internal PD)

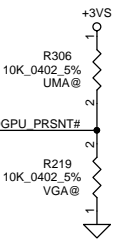
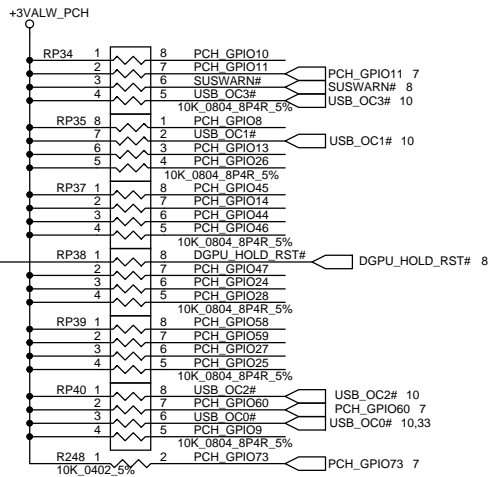
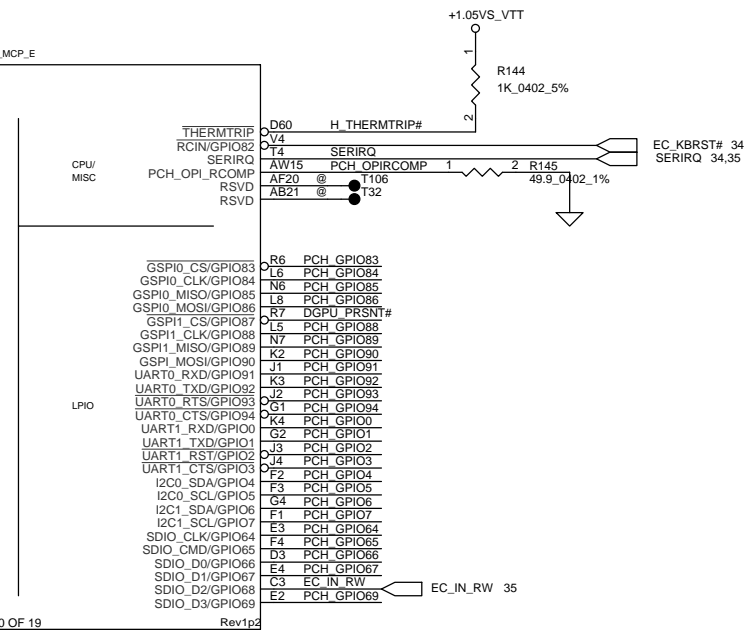
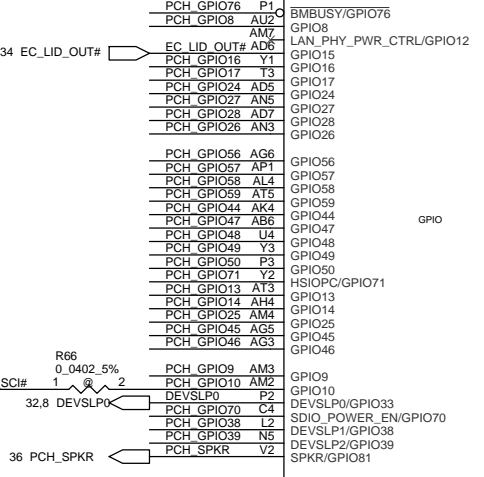
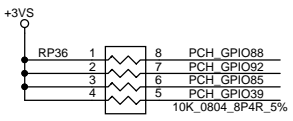
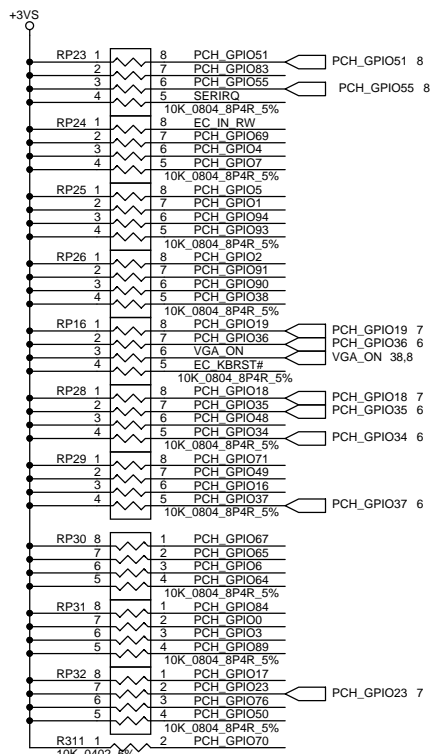


Project ID	Project_ID1 GPIO54	Project_ID0 GPIO53
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Reserved	0	1
Reserved	1	0
Reserved	1	1

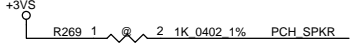
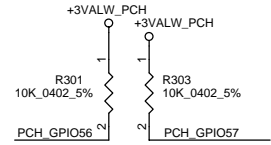
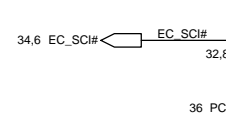
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Compal Electronics, Inc.			
HSW MCP(5/11) PM,GPIO,DDI			
Document Number	V5WE2 M/B LA-9531P Schematic		Rev 1.0
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	GPIO87 DGPU_PRST#
DIS,Optimus	0
UMA	1



GPIO15 : TLS Confidentiality

1: Intel ME TLS with confidentiality
 * 0: Intel ME TLS with no confidentiality (Have internal PD)

GSPI0_MOSI / GPIO86 : Boot BIOS Strap

1: ENABLED
 * 0: SPI ROM (Have internal PD)

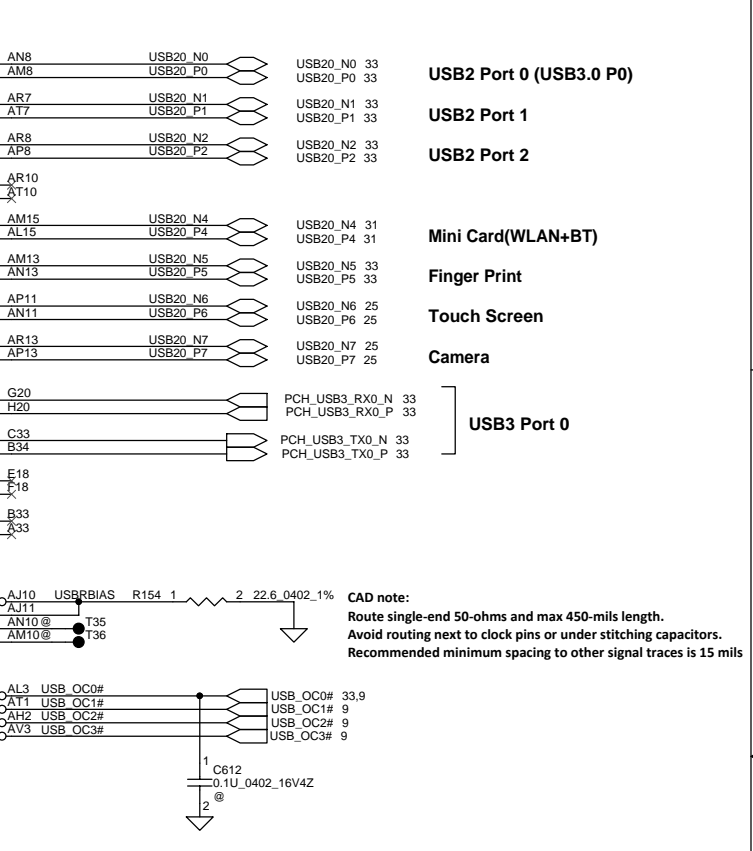
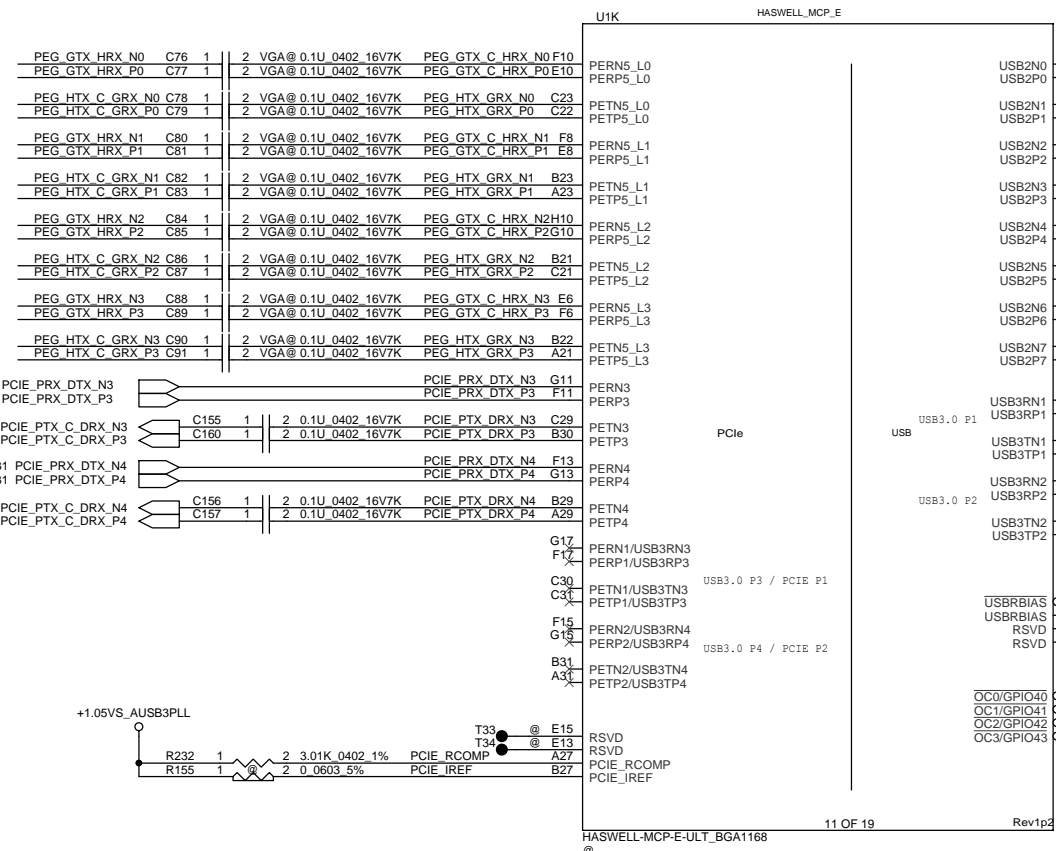
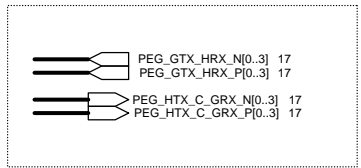
SPKR / GPIO81 : NO REBOOT

1: ENABLED
 * 0: DISABLED (Have internal PD)

SDIO_D0 / GPIO66 : Top-Block Swap Override

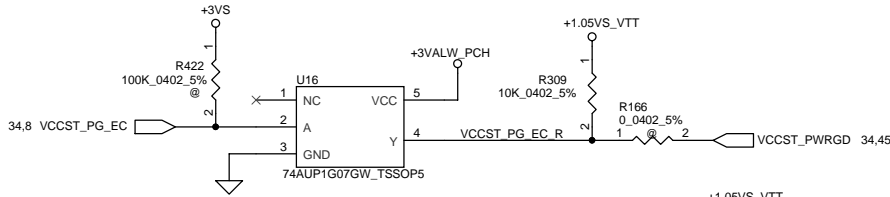
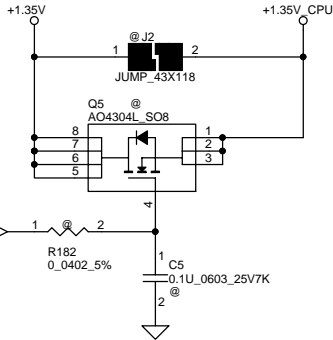
1: ENABLED
 * 0: DISABLED (Have internal PD)

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2012/07/10		2013/07/10		Tuesday, March 26, 2013	
<p style="text-align: center;">Compal Electronics, Inc.</p> <p style="text-align: center;">HSW MCP(6/11) GPIO,LPIO</p>					
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Size	Document Number	Date		Sheet	Rev
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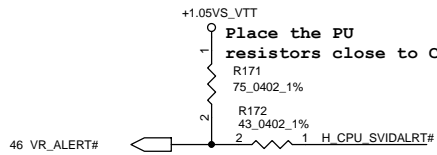


Security Classification		Compal Secret Data		Title	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Compal Electronics, Inc. HSW MCP(7/11) PCIE,USB	
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				V5WE2 M/B LA-9531P Schematic	1.0
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Shark Bay ULT have internal gate for VDDQ

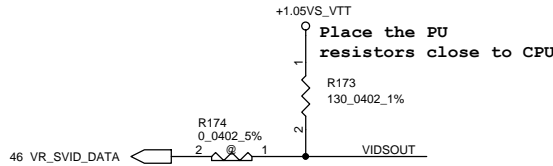


SVID ALERT

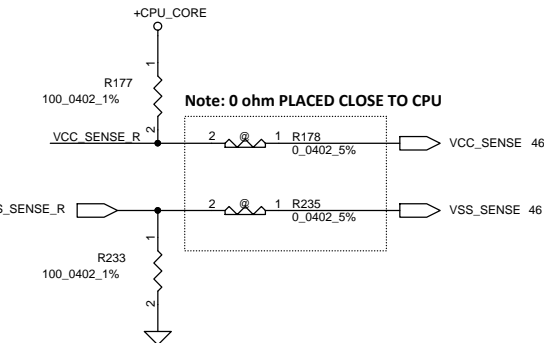


Place the PU resistors close to CPU

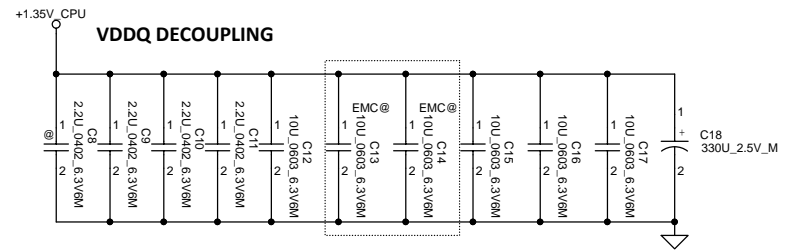
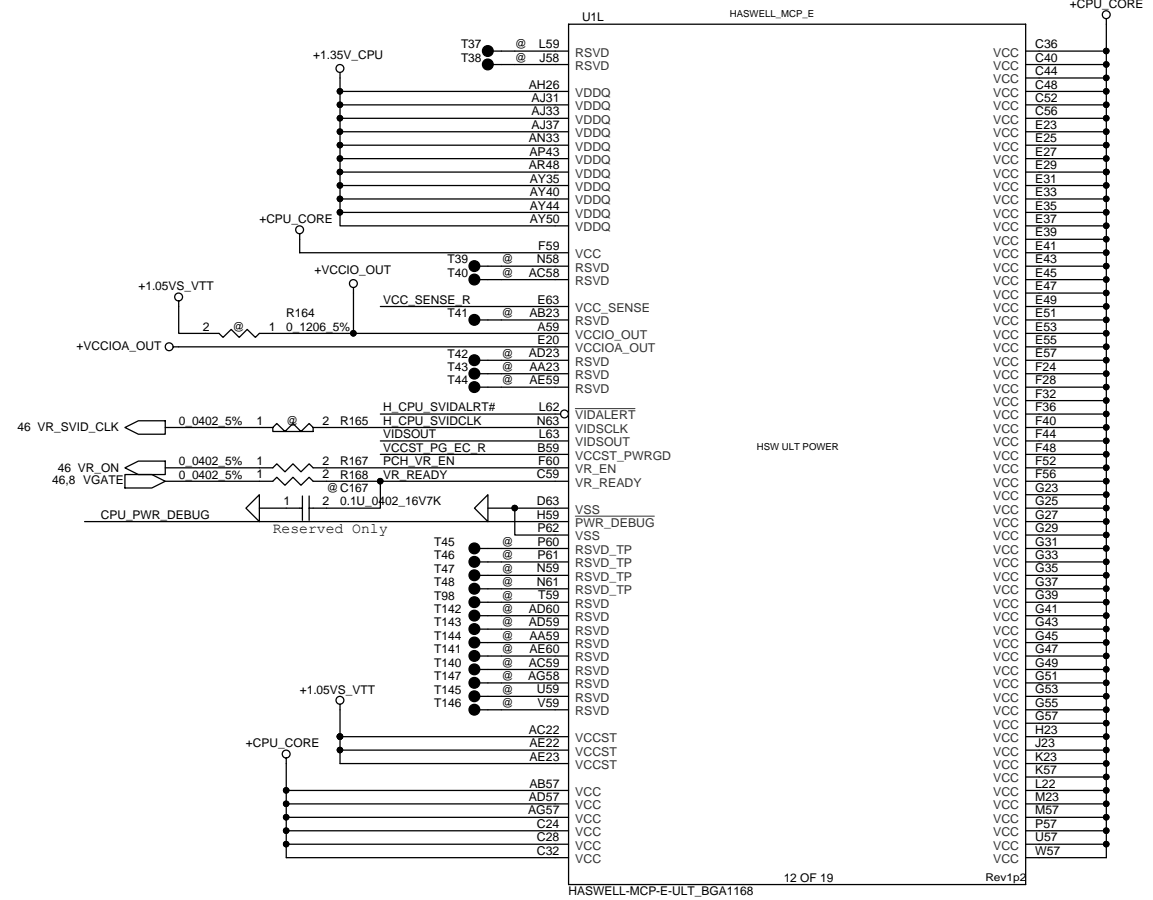
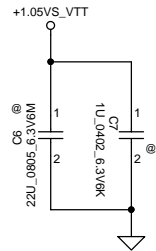
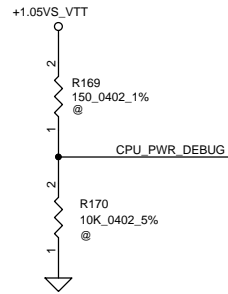
SVID DATA



Place the PU resistors close to CPU



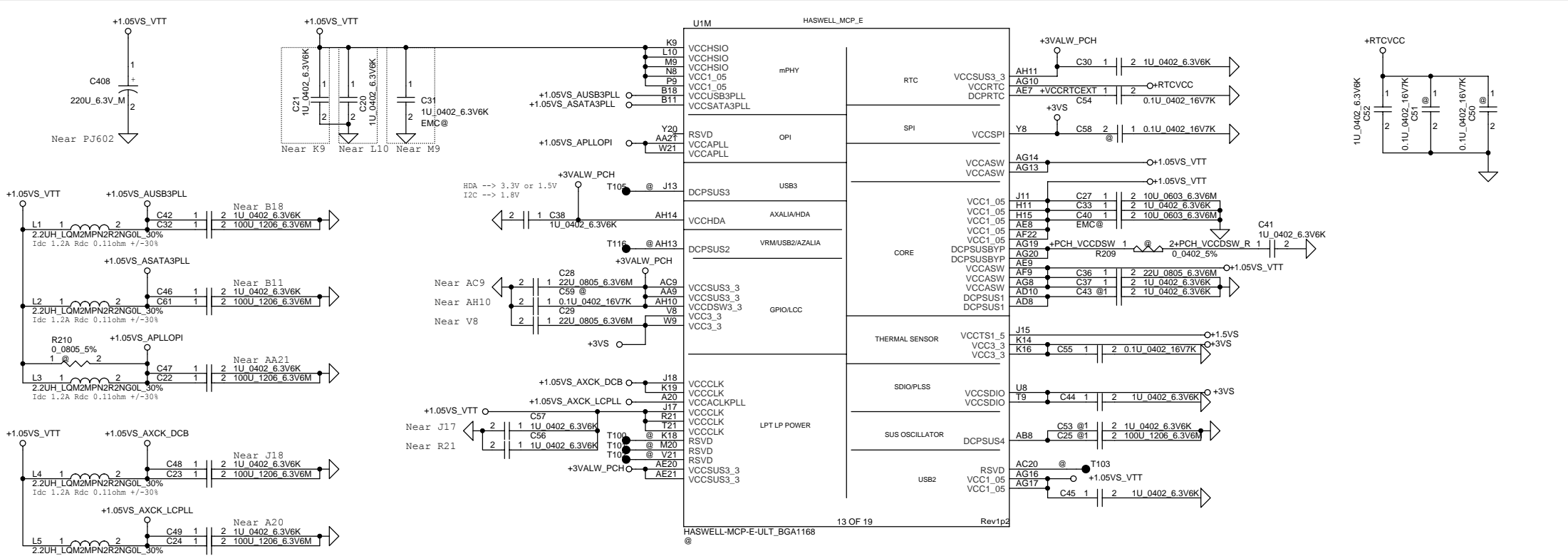
Note: 0 ohm PLACED CLOSE TO CPU



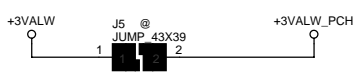
For ESD

- +1.35V : 470UF/2V/7343 *2
- 10UF/6.3V/0603 * 6
- 2.2UF/6.3V/0402 * 4

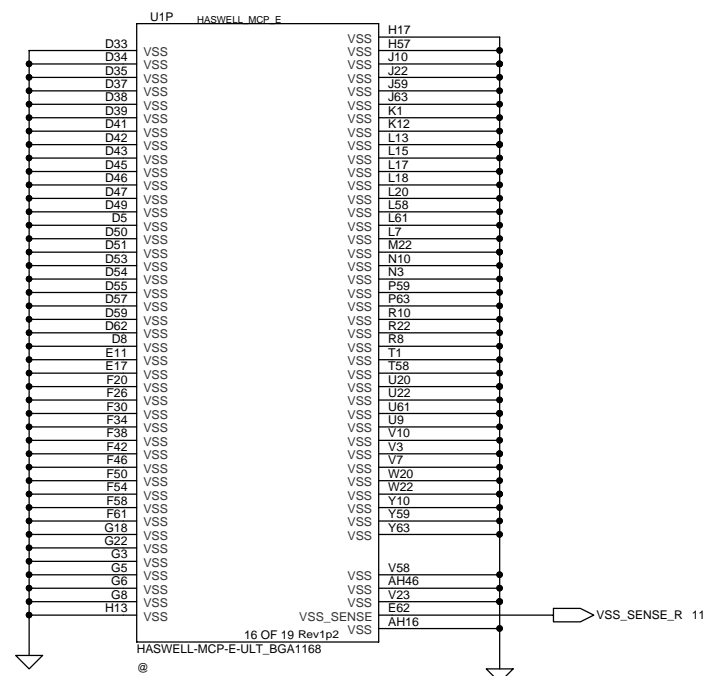
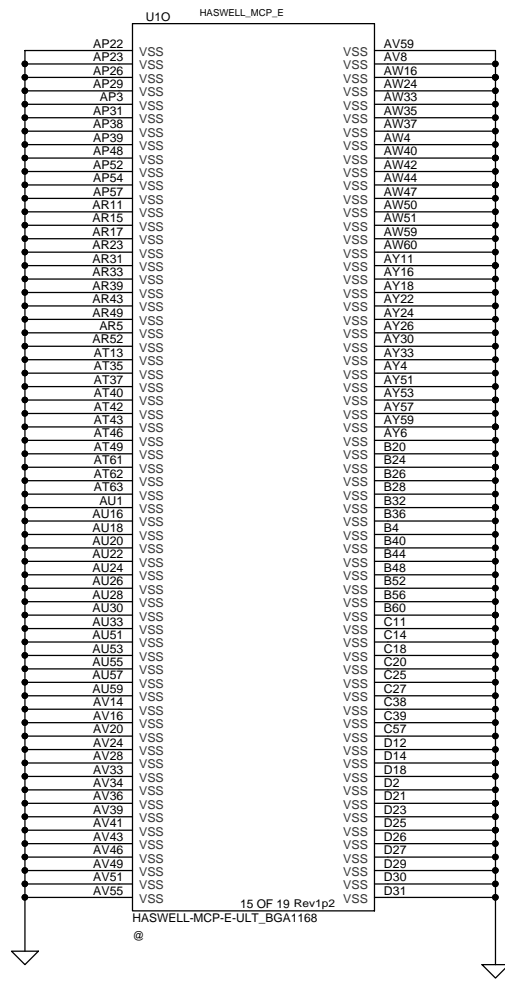
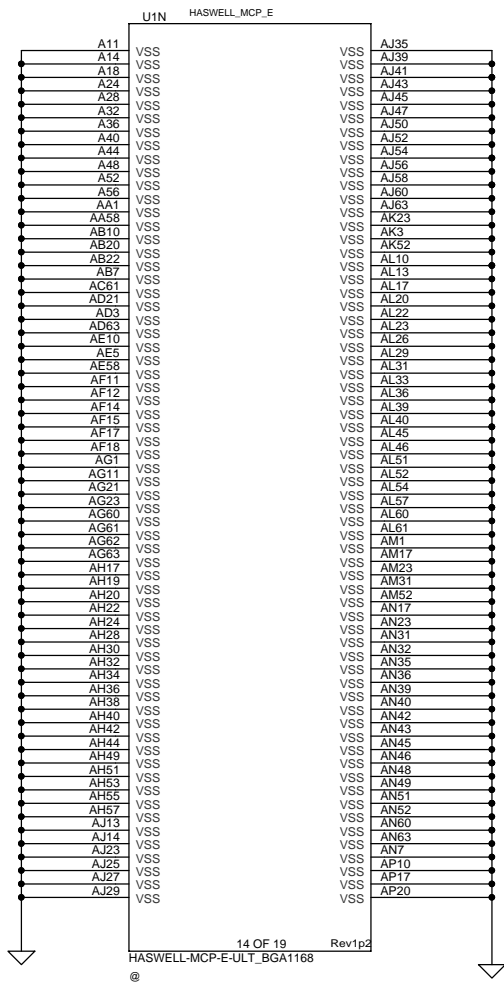
Security Classification				Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title				
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				Custom	V5WE2 M/B LA-9531P Schematic	1.0		
				Date:	Tuesday, March 26, 2013	Sheet	11	of 52



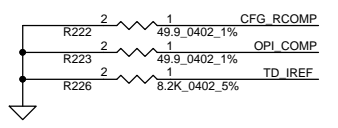
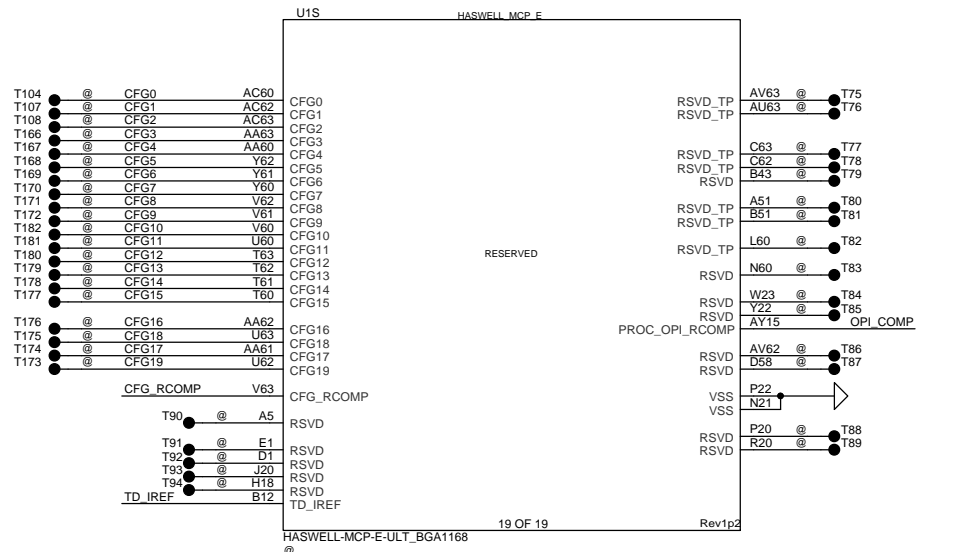
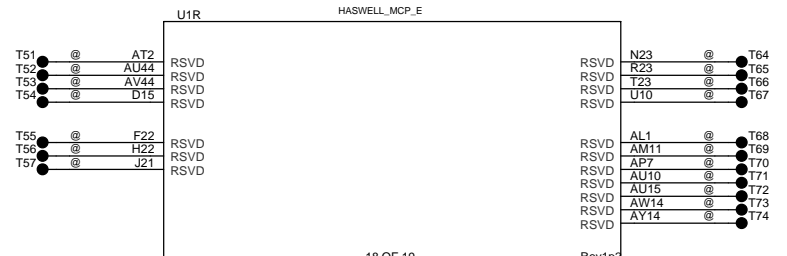
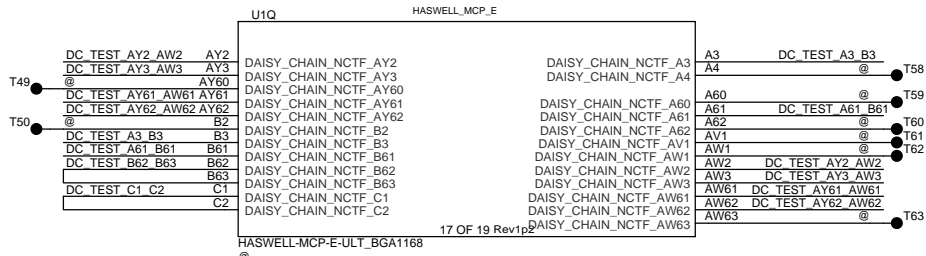
+3VALW TO +3VALW(PCH AUX Power)
 Short J5 for PCH VCCSUS3.3



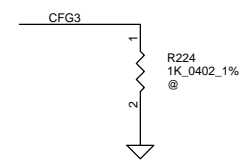
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				V5WE2 M/B LA-9531P Schematic	1.0
Date:				Tuesday, March 26, 2013	Sheet 12 of 52



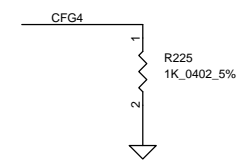
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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title HSW MCP(10/11) GND	
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				V5WE2 M/B LA-9531P Schematic	1.0
Date:	Tuesday, March 26, 2013	Sheet	13	of	52



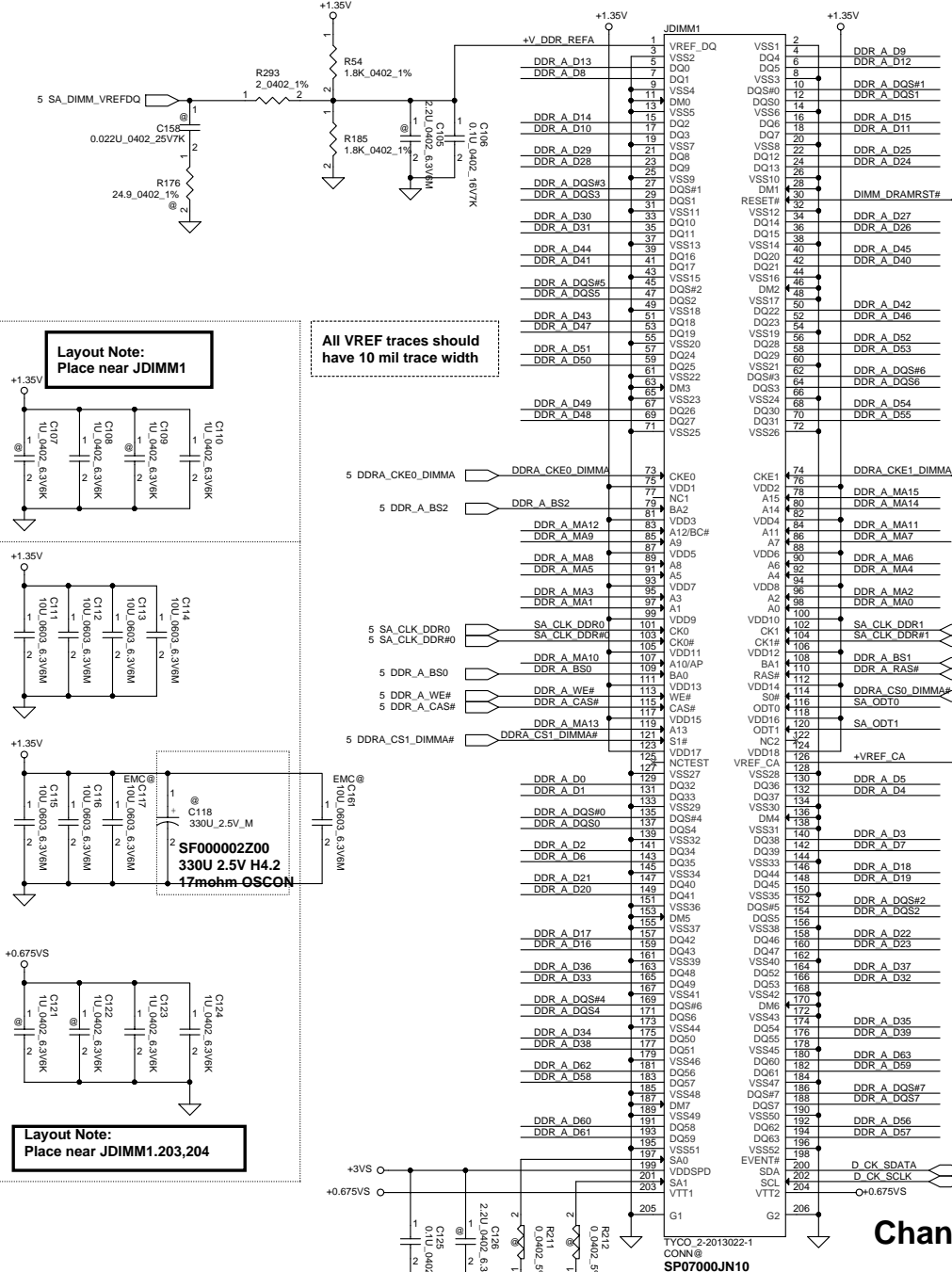
CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



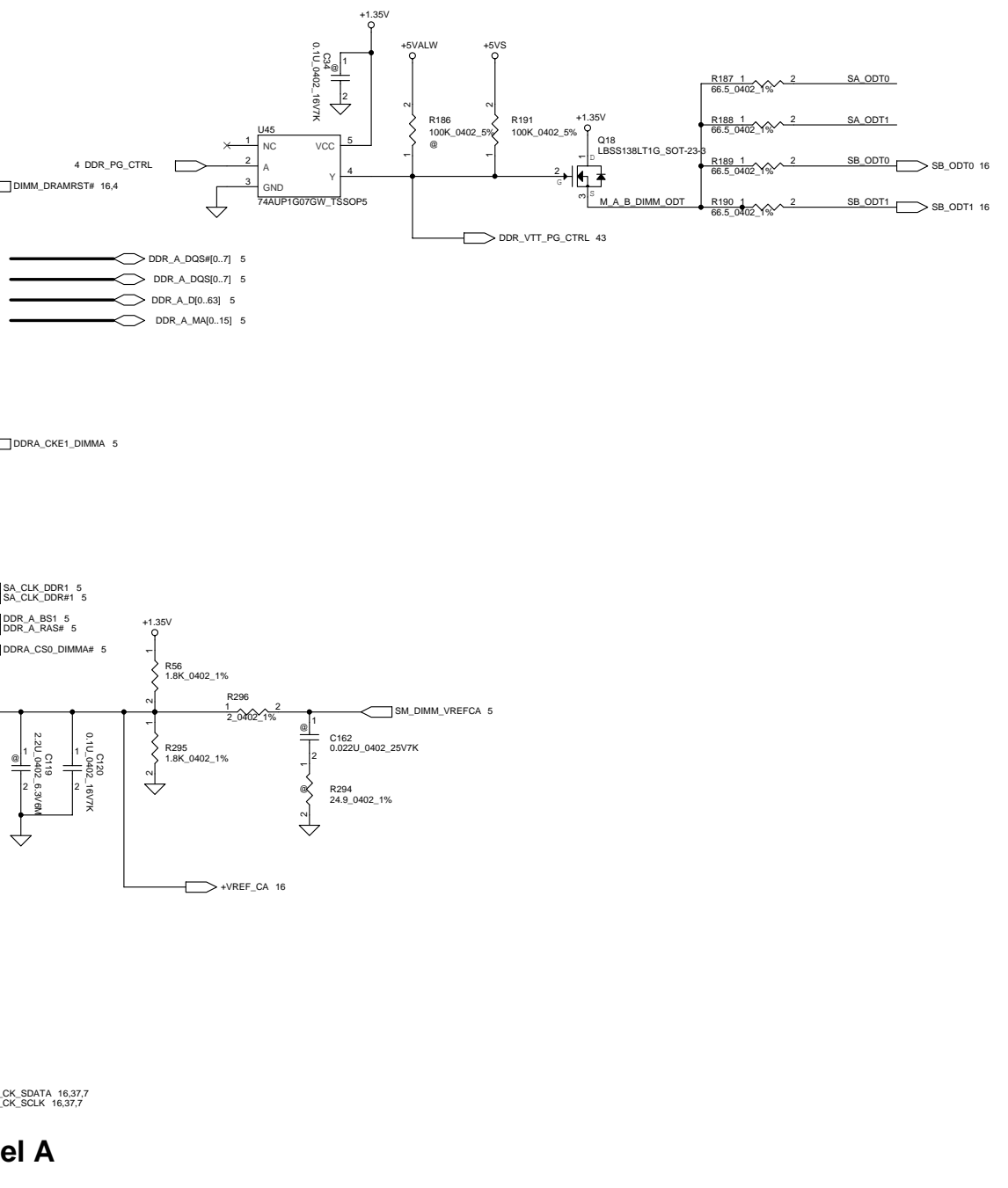
Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width

SF000002Z00
330U 2.5V H4.2
17mohm OSCON

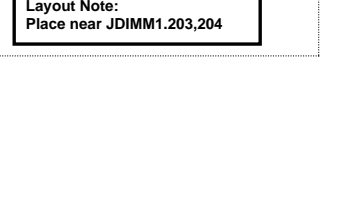
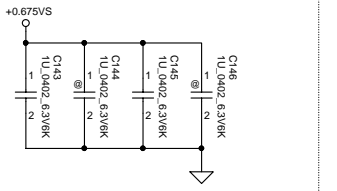
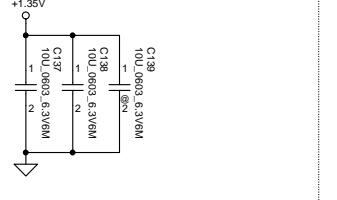
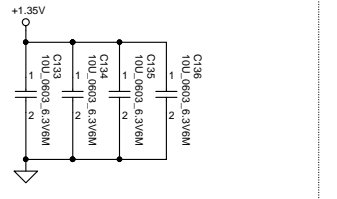
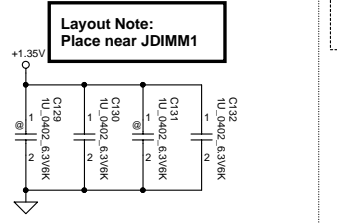
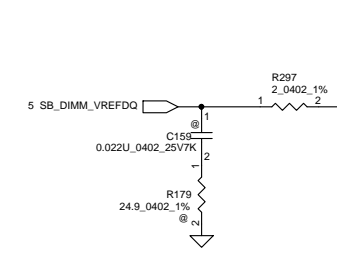
Layout Note:
Place near JDIMM1.203,204

<Address: SA1:SA0=00>
DIMM_1 STD H:4mm



Channel A

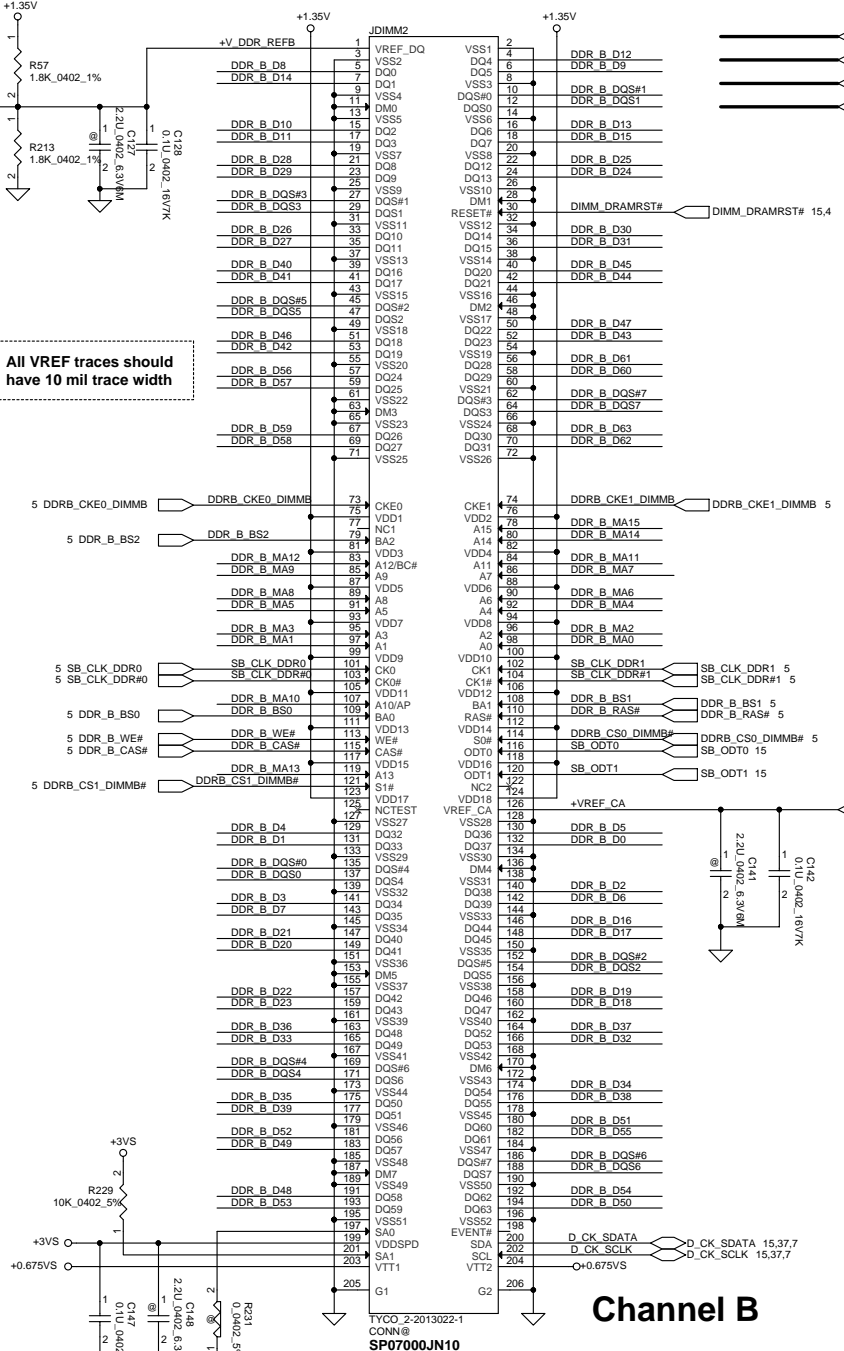
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Customer			Document Number	VSW E2 M/B LA-9531P Schematic
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All VREF traces should have 10 mil trace width

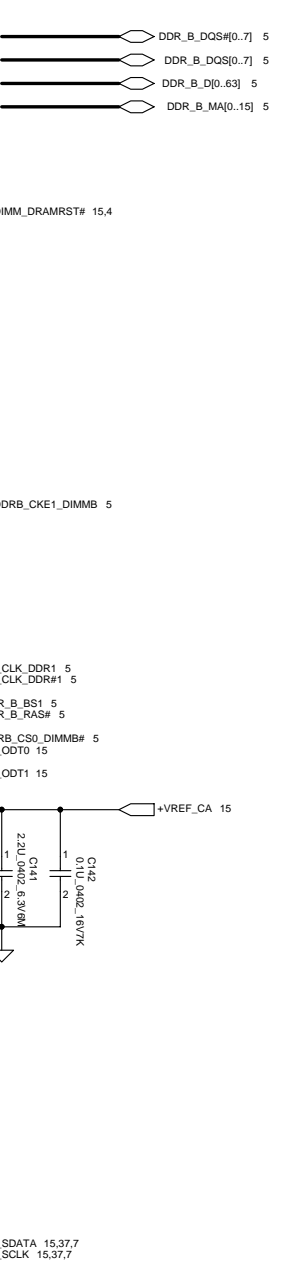
Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204



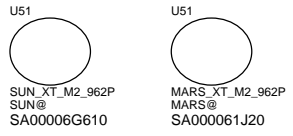
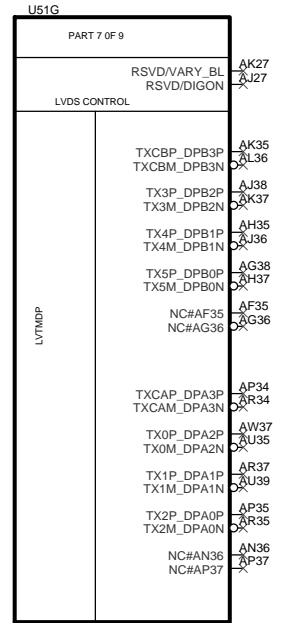
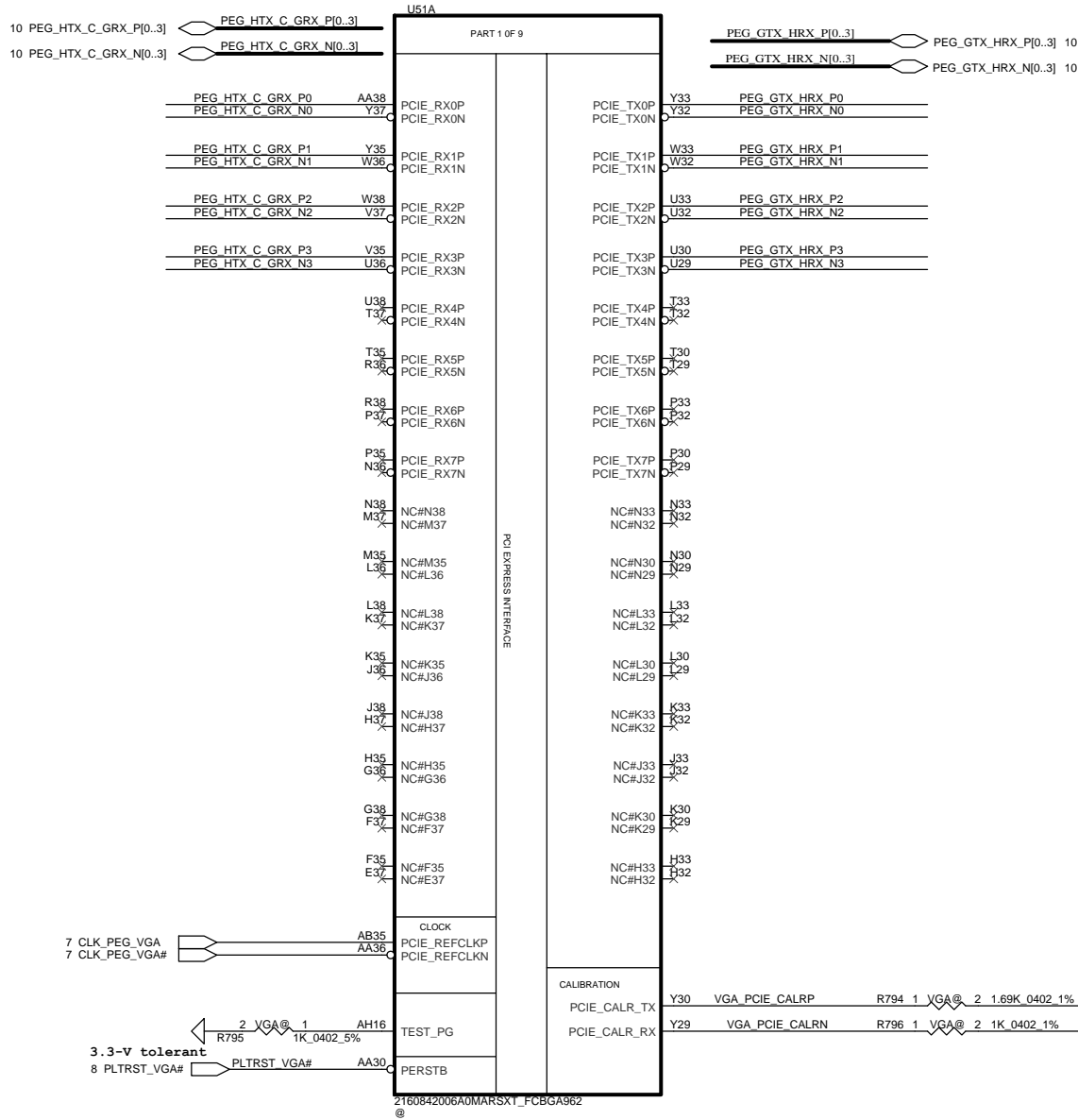
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DIMM_2 STD H:4mm

Channel B



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2012/07/10		2013/07/10		DDR III DIMMB	
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Document Number				Customer	
VSW2 M/B LA-9531P Schematic				Date: Tuesday, March 26, 2013	
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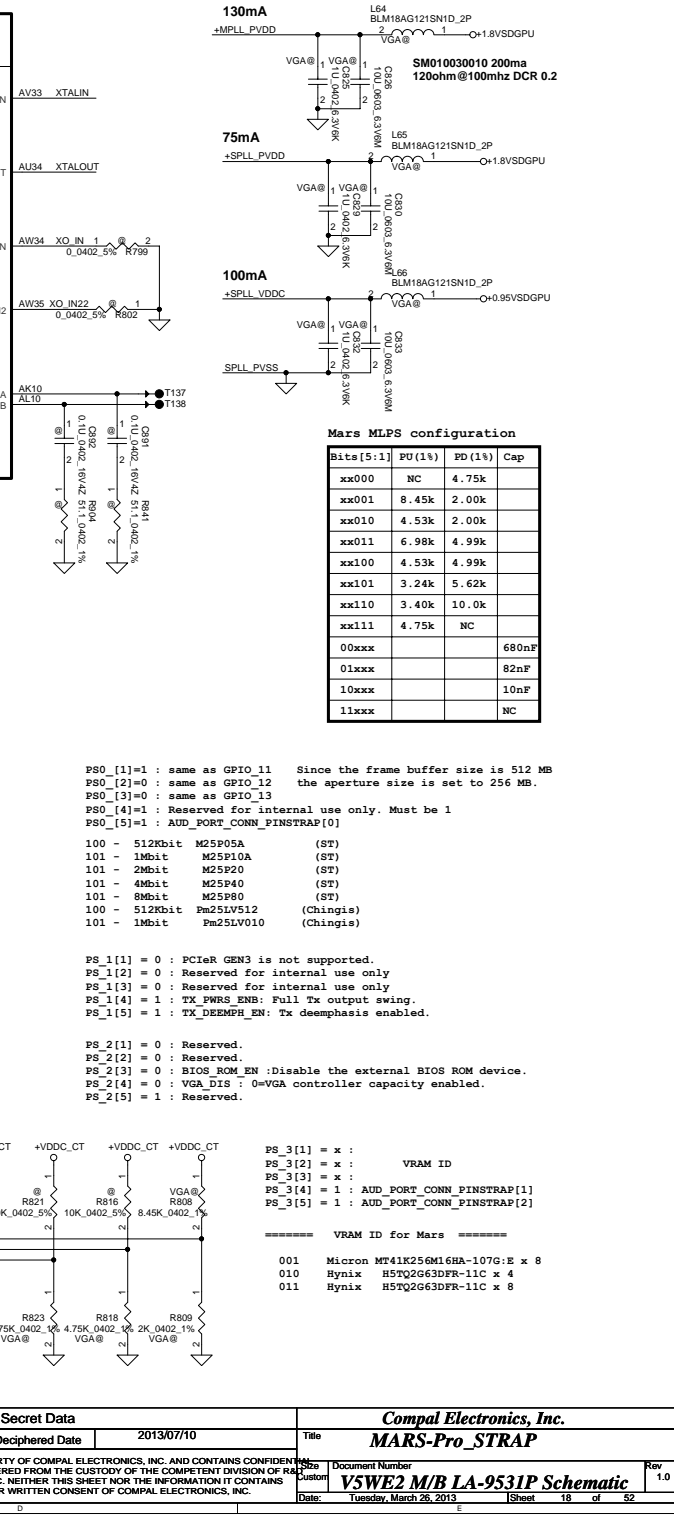
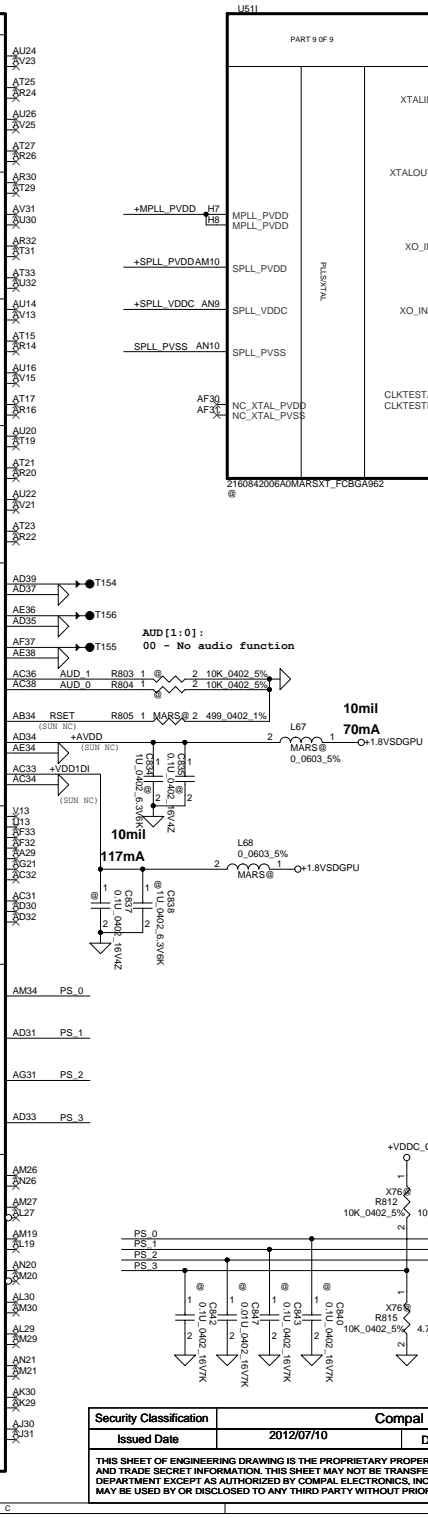
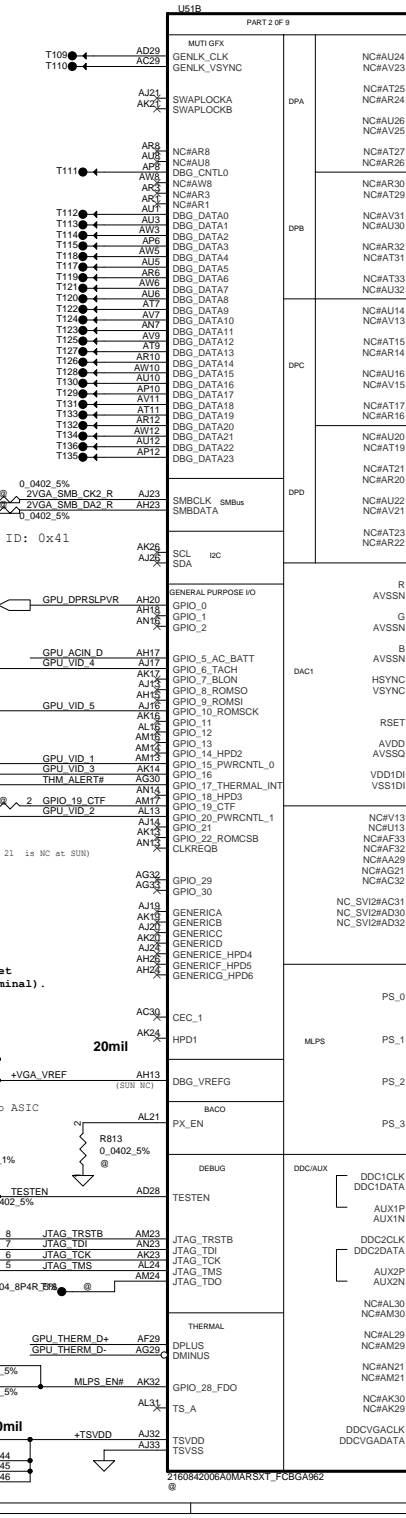
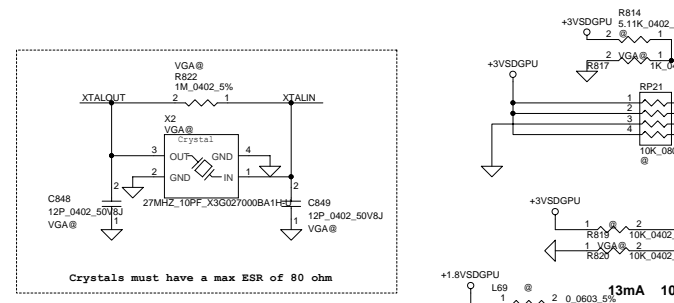
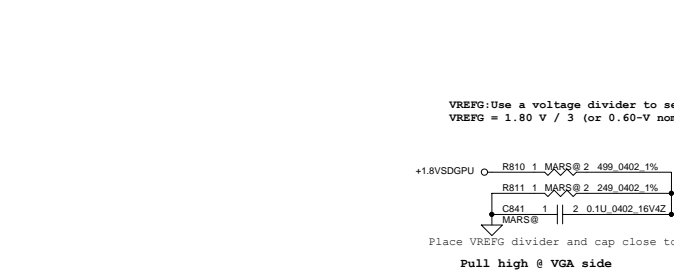
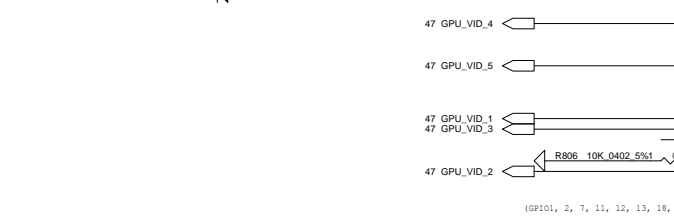
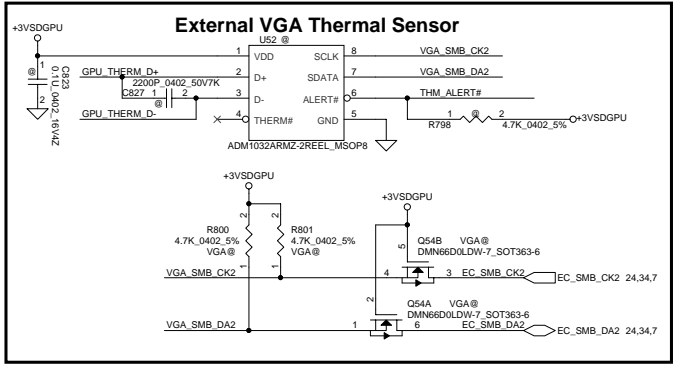
GFX PCIE LANE REVERSAL



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2012/07/10		2013/07/10		MARS@ SA00006J20	
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Date: Thursday, April 11, 2013				Sheet 17 of 52	

2160842006A0MARSX1_FCBGA962 @

2160842006A0MARSX1_FCBGA962 @



Mars MLPS configuration

Bits [5:1]	PU (1%)	PD (1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

PS0 [1]=1 : same as GPIO 11 Since the frame buffer size is 512 MB
 PS0 [2]=0 : same as GPIO 12 the aperture size is set to 256 MB.
 PS0 [3]=0 : same as GPIO 13
 PS0 [4]=1 : Reserved for internal use only. Must be 1
 PS0 [5]=1 : AUD_POR_NN_PFNSTRAP[0]

100 - 512kbit M25P05A (ST)
 101 - 1Mbit M25P10A (ST)
 101 - 2Mbit M25P20 (ST)
 101 - 4Mbit M25P40 (ST)
 101 - 8Mbit M25P80 (ST)
 100 - 512kbit Pm25LV512 (Chingis)
 101 - 1Mbit Pm25LV010 (Chingis)

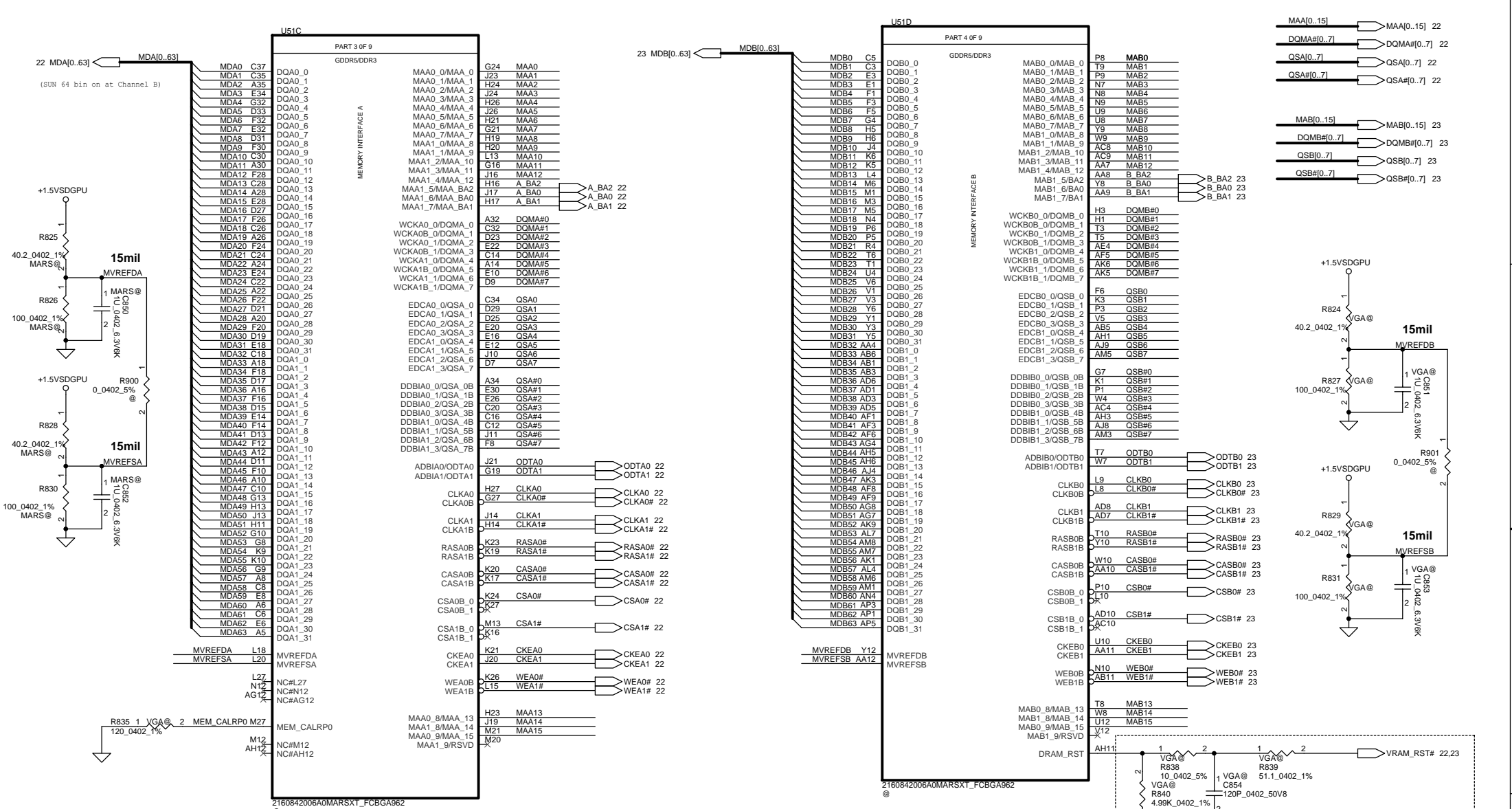
PS 1[1] = 0 : FCIEr GEN3 is not supported.
 PS 1[2] = 0 : Reserved for internal use only
 PS 1[3] = 0 : Reserved.
 PS 1[4] = 1 : TX_PWRS_ENB: Full TX output swing.
 PS 1[5] = 1 : TX_DEEMPH_EN: Tx deemphasis enabled.

PS 2[1] = 0 : Reserved.
 PS 2[2] = 0 : Reserved.
 PS 2[3] = 0 : BIOS_ROM_EN :Disable the external BIOS ROM device.
 PS 2[4] = 0 : VGA_DIS = 0:VGA controller capacity enabled.
 PS 2[5] = 1 : Reserved.

PS 3[1] = x : VRAM ID
 PS 3[2] = x :
 PS 3[3] = x :
 PS 3[4] = 1 : ADD_POR_NN_PFNSTRAP[1]
 PS 3[5] = 1 : ADD_POR_NN_PFNSTRAP[2]

===== VRAM ID for Mars =====
 001 Micron MT41K256M16RA-107G: E x 8
 010 Hynix H5TQ2G63DFR-11C x 4
 011 Hynix H5TQ2G63DFR-11C x 8

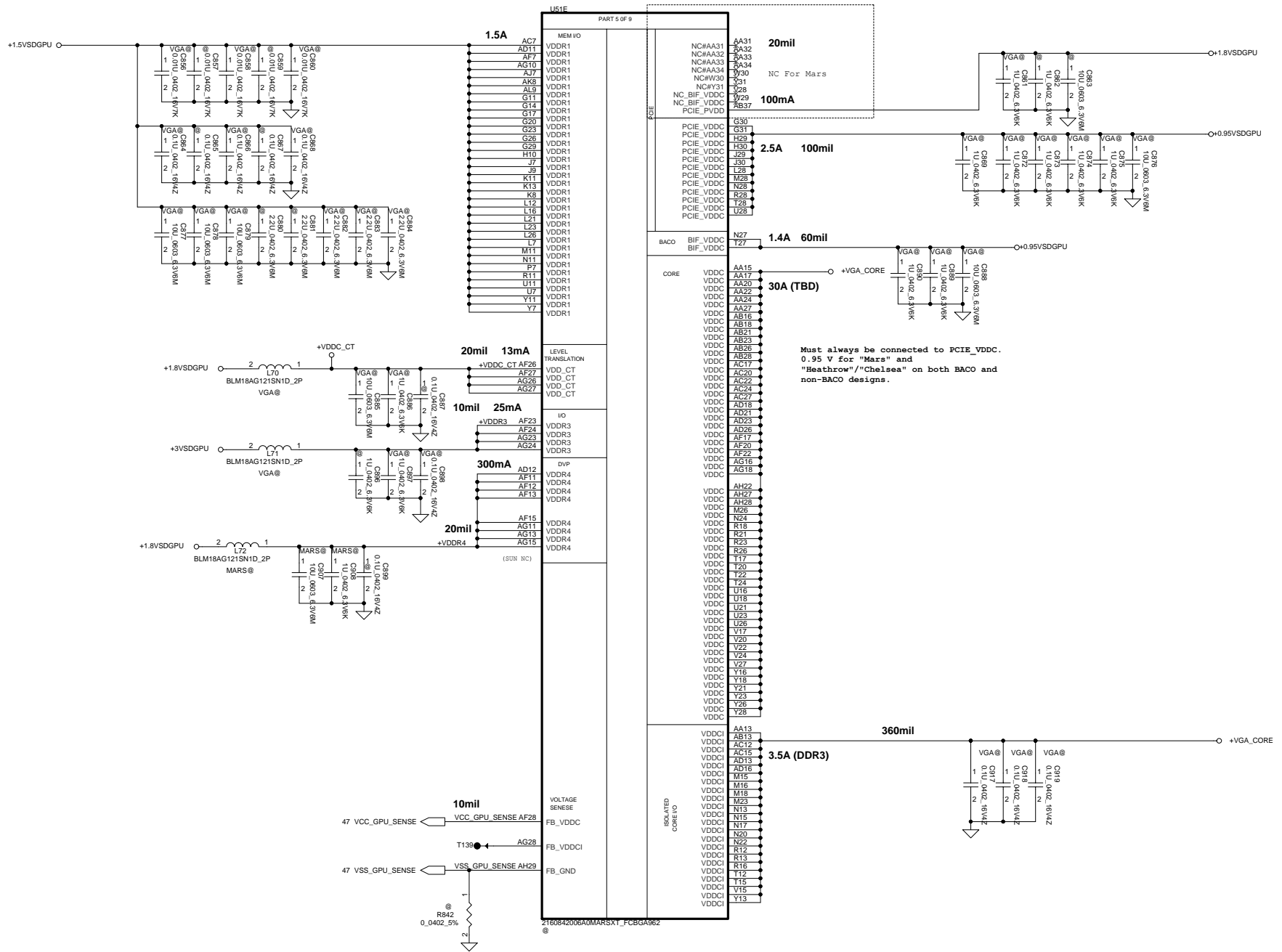
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Customer	Document Number		Date		Rev	
	V5WE2 M/B LA-9531P Schematic		Tuesday, March 26, 2013		1.0	
			[Sheet 18 of 52]			



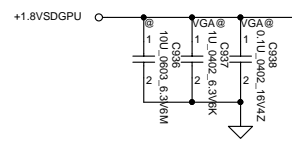
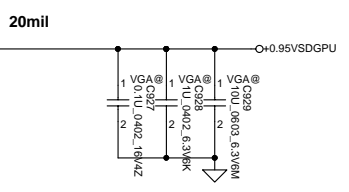
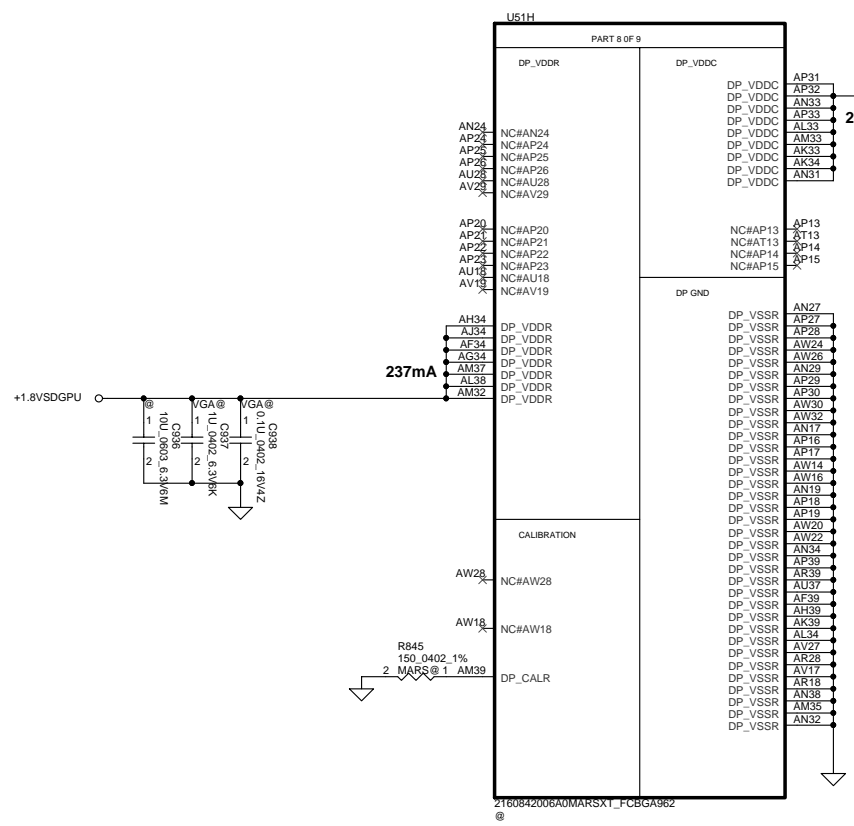
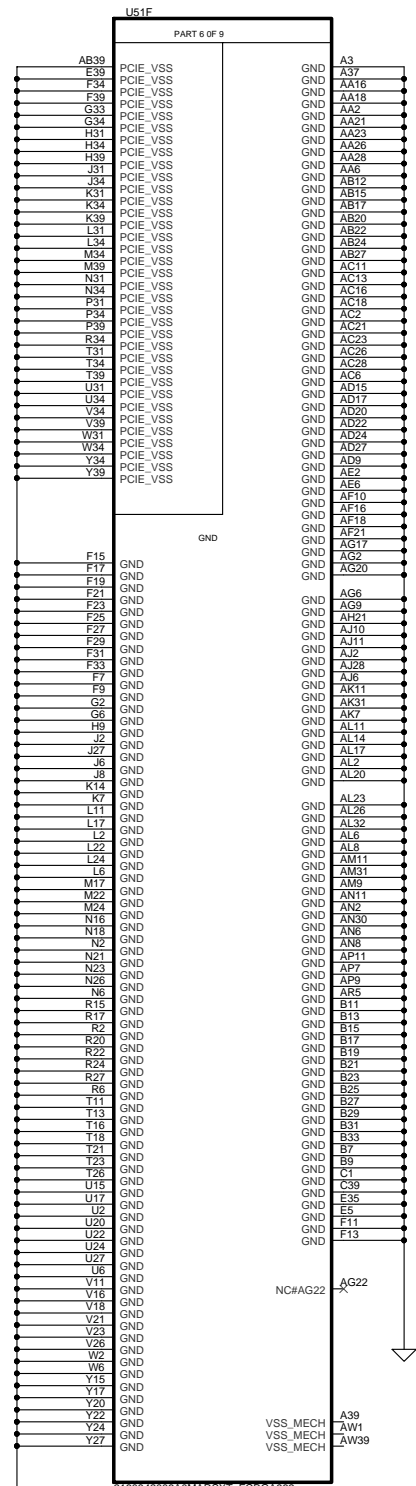
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within5mm) except Rser2

The suggested components are tested on the AMD reference board only. Customers must measure the slew on each memory part to ensure that the slew rate meets the DRAM specification.

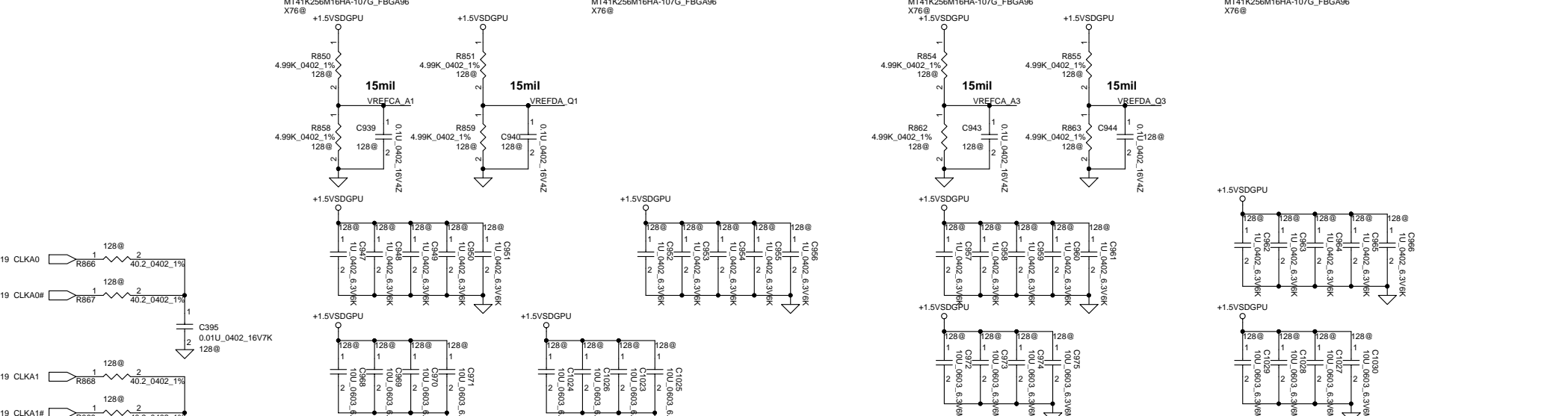
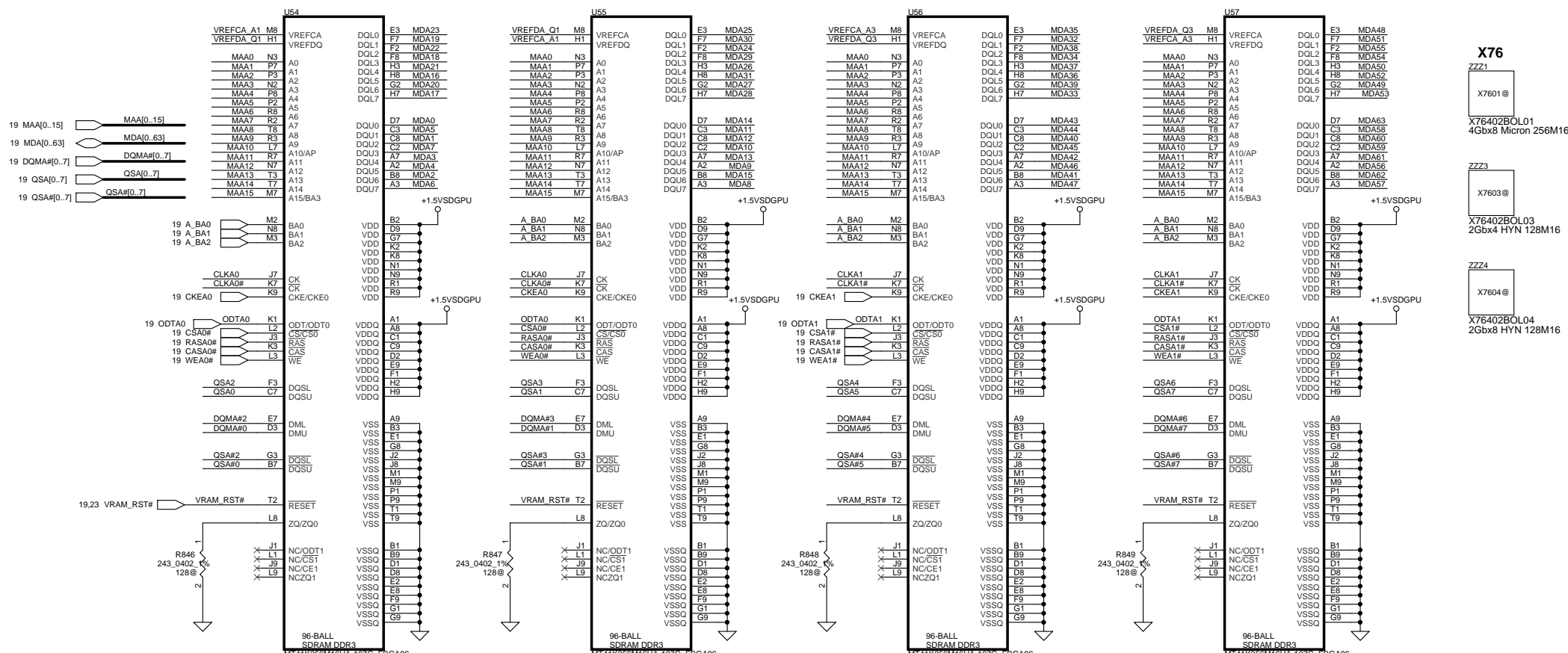
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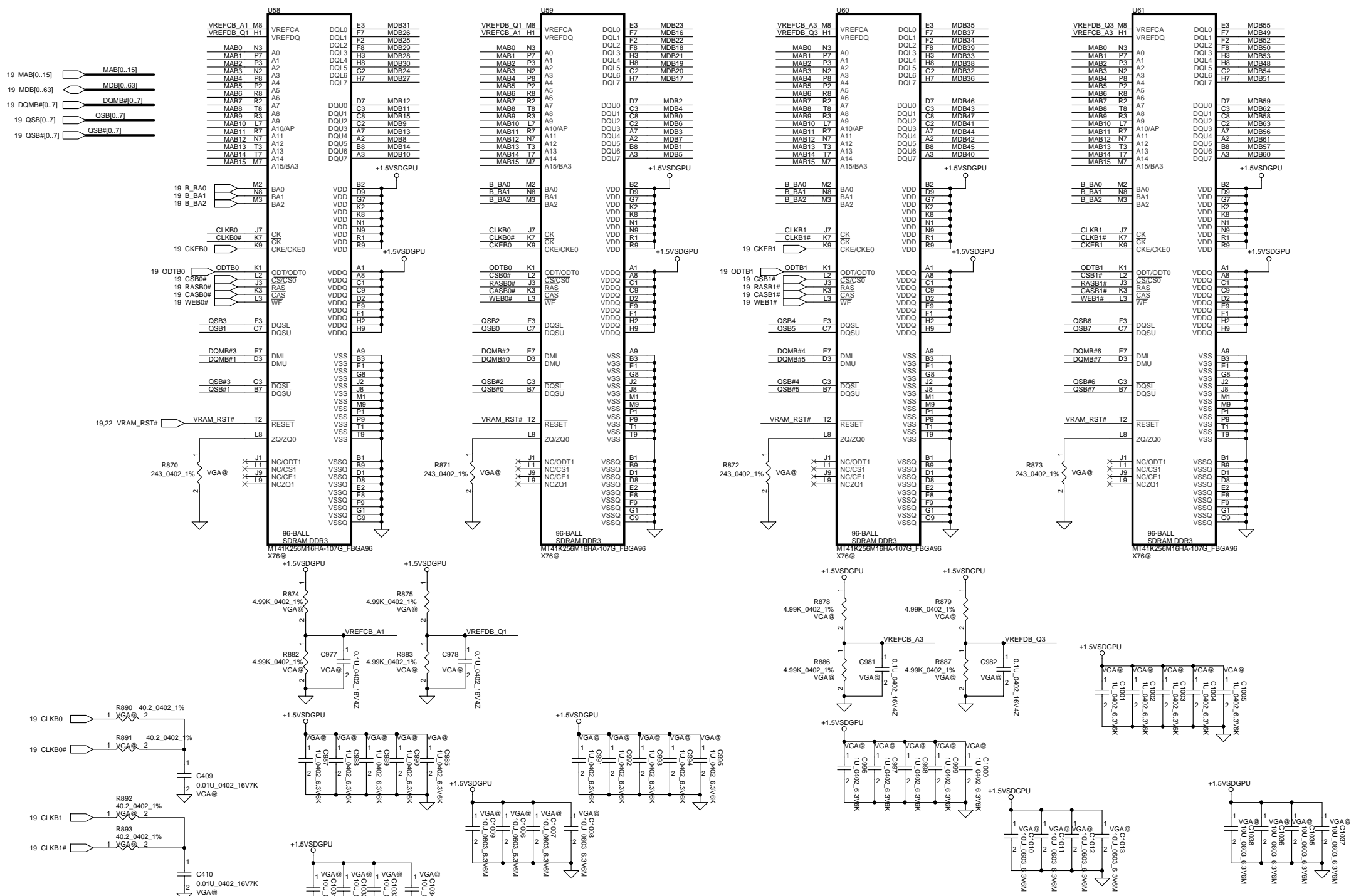
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Date:	Tuesday, March 26, 2013	Sheet	20	of	52



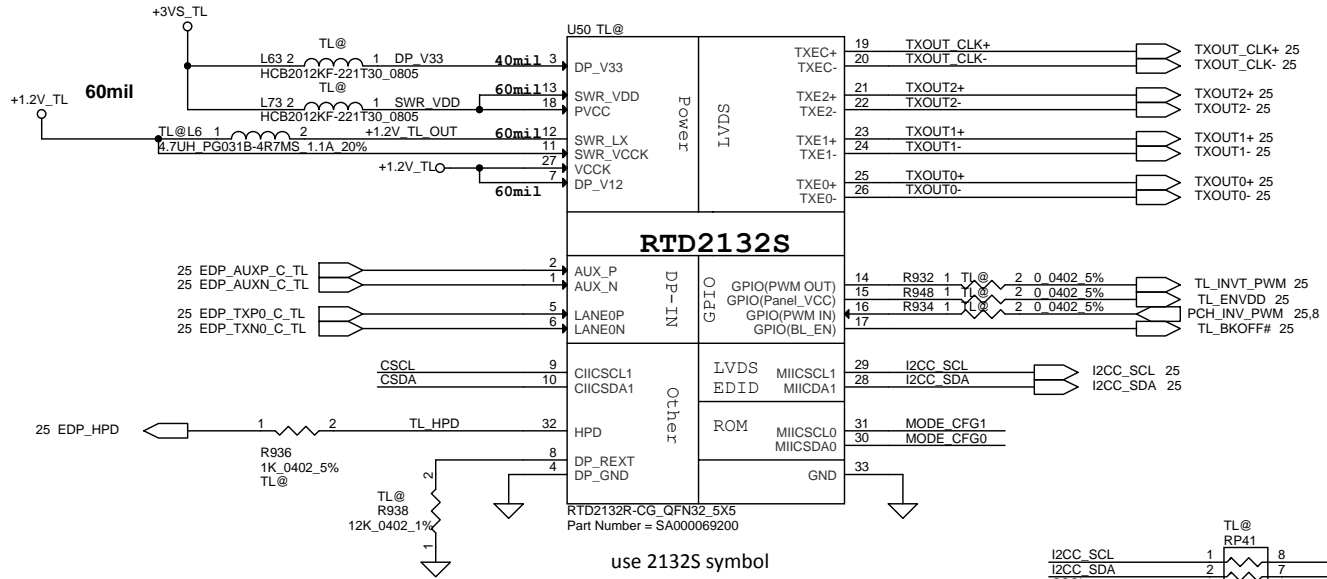
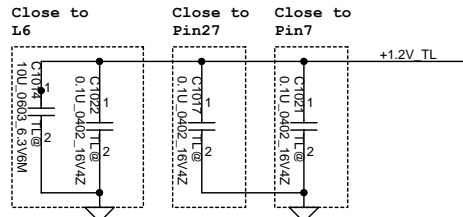
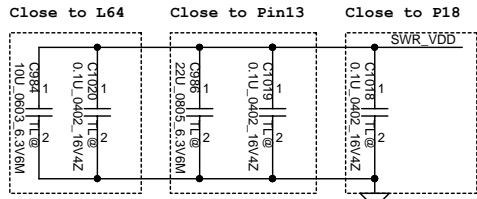
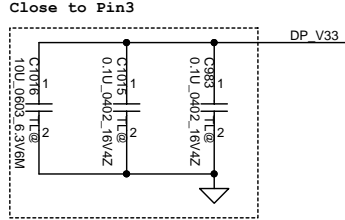
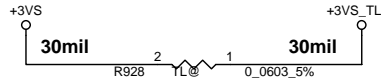
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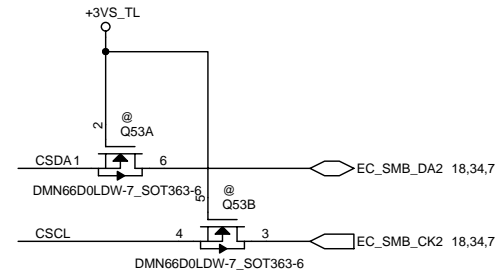
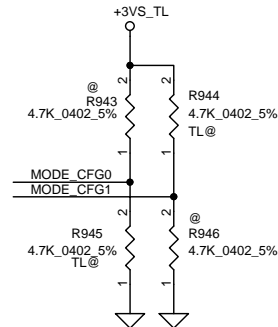
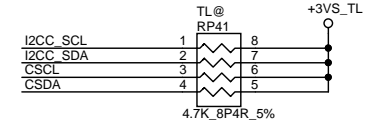
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title
				VRAM_DDR3 / Channel A
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Security Classification		Compal Secret Data		Title	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	VRAM DDR3 / Channel B	
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Date:	Tuesday, March 26, 2013	Sheet	23	Rev 1.0	



use 2132S symbol

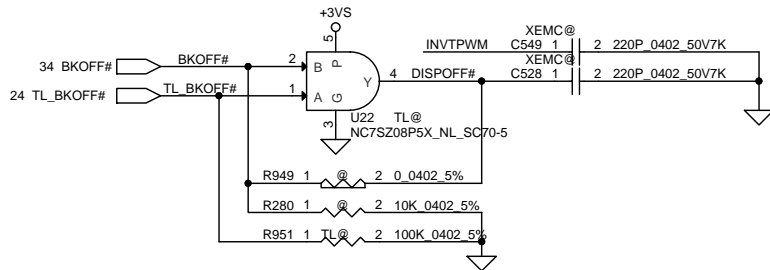
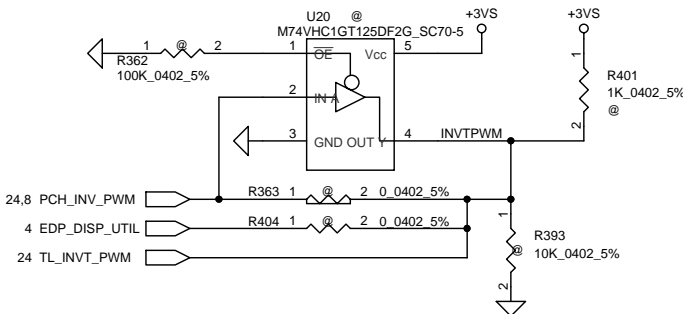
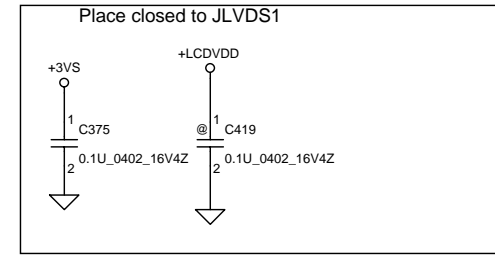
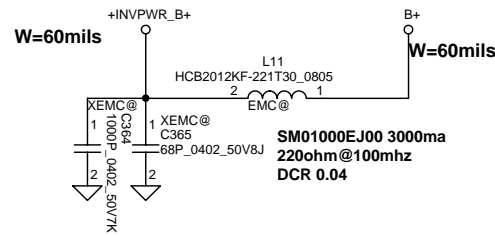
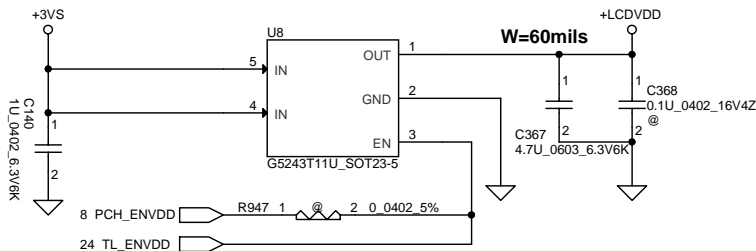


		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE*	EEPROM MODE

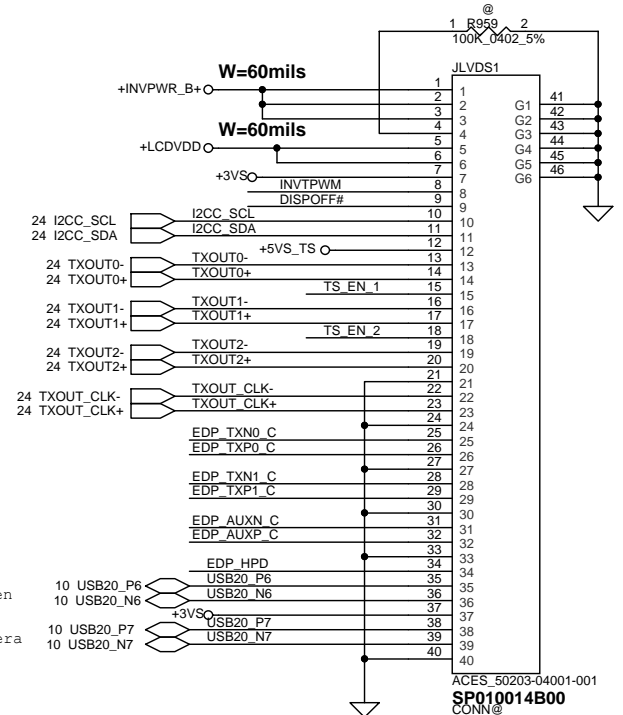
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Issued Date	2011/07/08	Deciphered Date	2015/07/08
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Title	LVDS Translator - RTD2132R		
Document Number	V5WE2 M/B LA-9532P Schematic		
Date	Tuesday, March 26, 2013	Sheet	24 of 52
Rev	1.0		

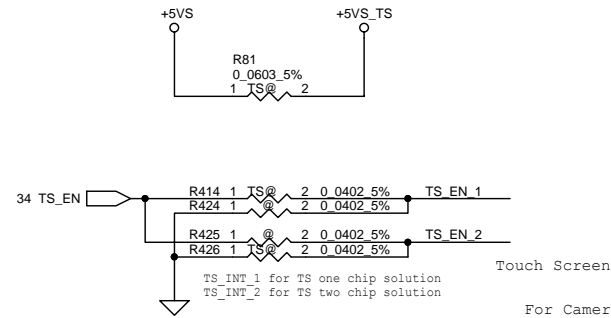
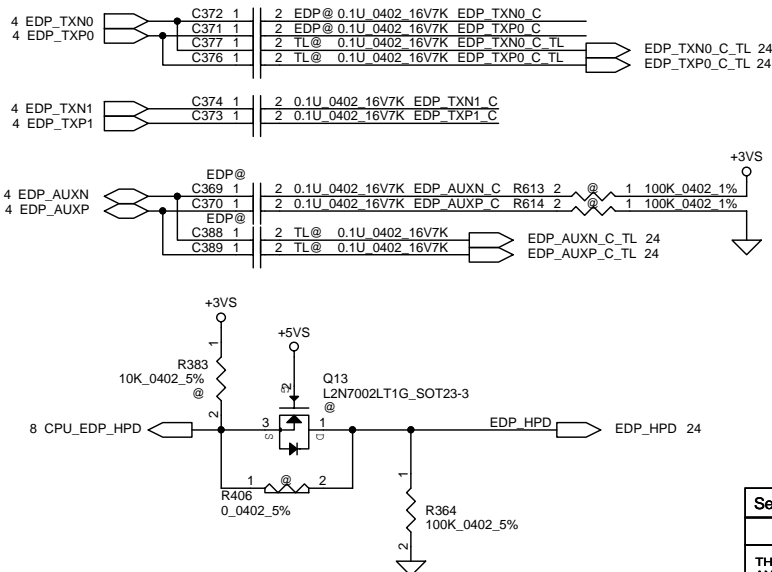
LCD POWER CIRCUIT



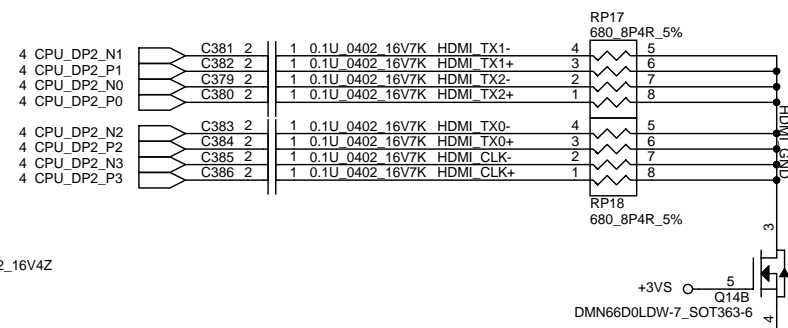
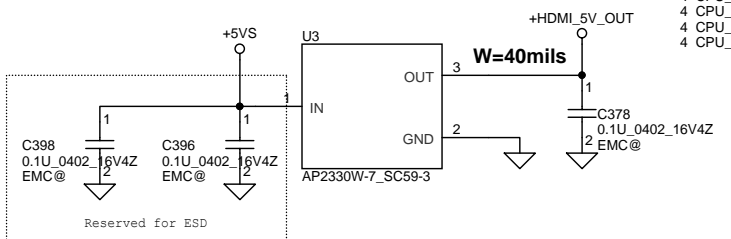
LCD/ LED PANEL Conn.



eDP

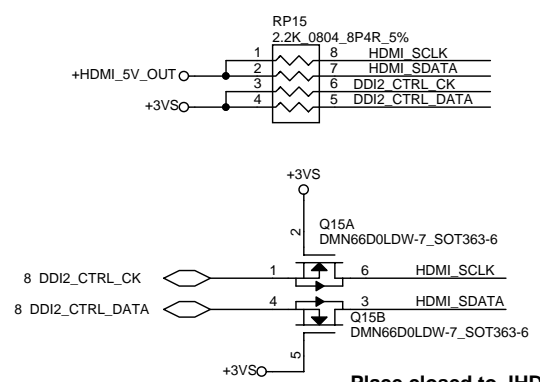
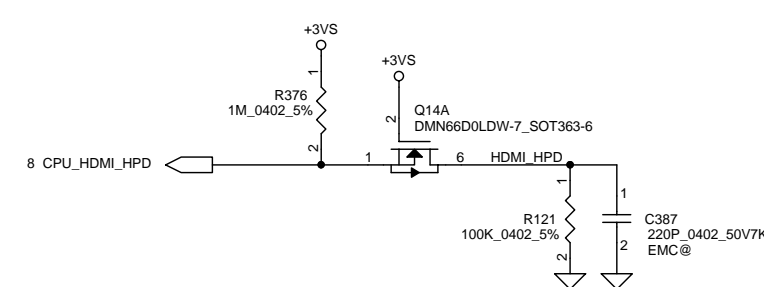


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Document Number	V5WE2 M/B LA-9531P Schematic			Rev	1.0
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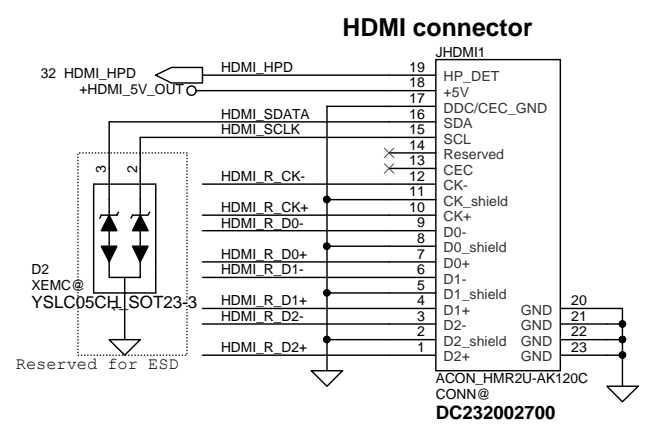


SM070001310 400ma 90ohm @100mhz DCR 0.3

HDMI CLK-	R368	1	XEMC@ 2	0.0402 5%	HDMI R CK-
HDMI CLK+	R369	1	XEMC@ 2	0.0402 5%	HDMI R CK+
HDMI TX0-	R370	1	XEMC@ 2	0.0402 5%	HDMI R D0-
HDMI TX0+	R371	1	XEMC@ 2	0.0402 5%	HDMI R D0+
HDMI TX1-	R372	1	XEMC@ 2	0.0402 5%	HDMI R D1-
HDMI TX1+	R373	1	XEMC@ 2	0.0402 5%	HDMI R D1+
HDMI TX2-	R374	1	XEMC@ 2	0.0402 5%	HDMI R D2-
HDMI TX2+	R375	1	XEMC@ 2	0.0402 5%	HDMI R D2+



Place closed to JHDMI1



ZZZ

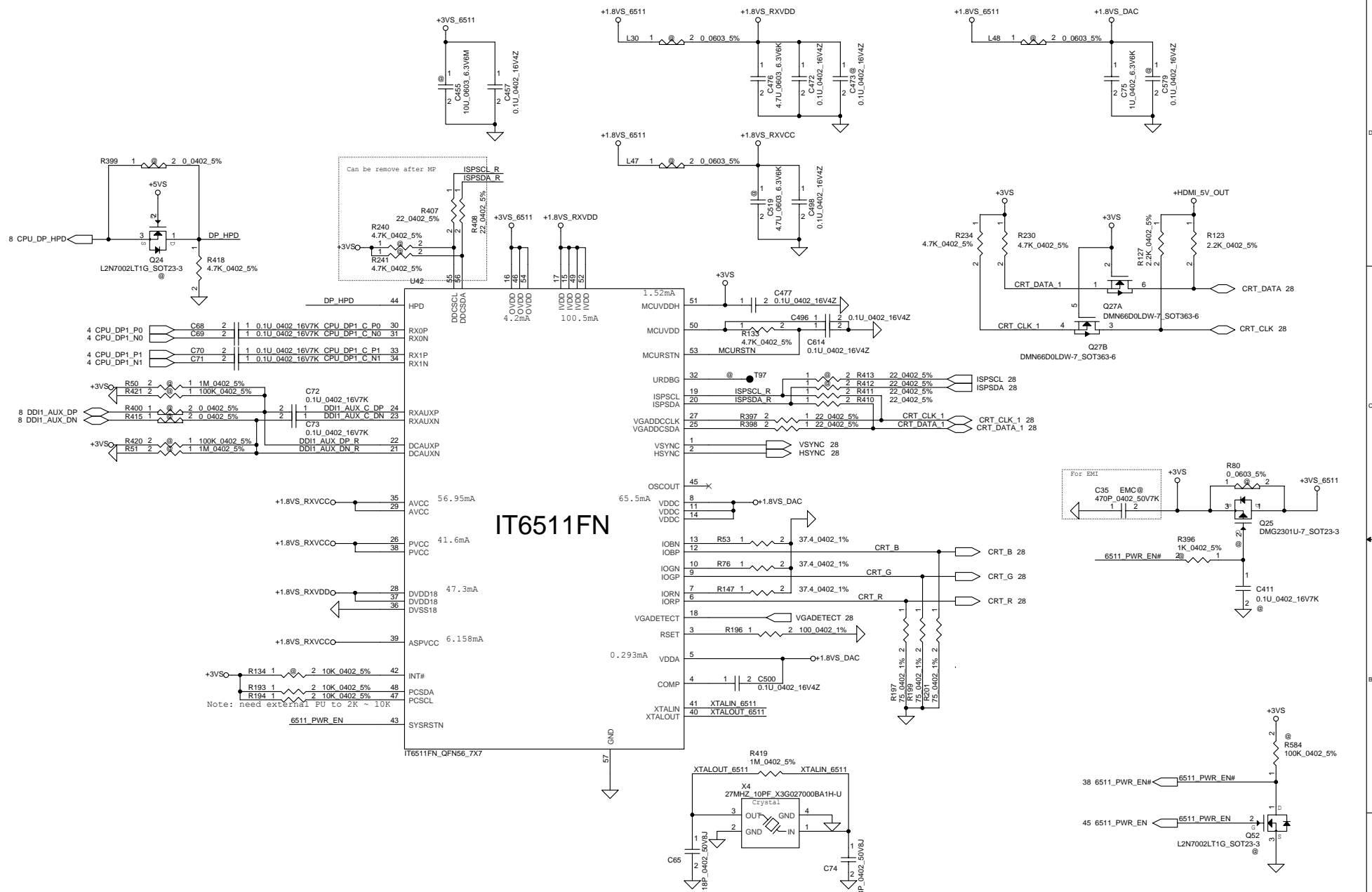
HDMI_ROYALTY

ROYALTY HDMI W/LOGO+HDCP

RQ0000003HM

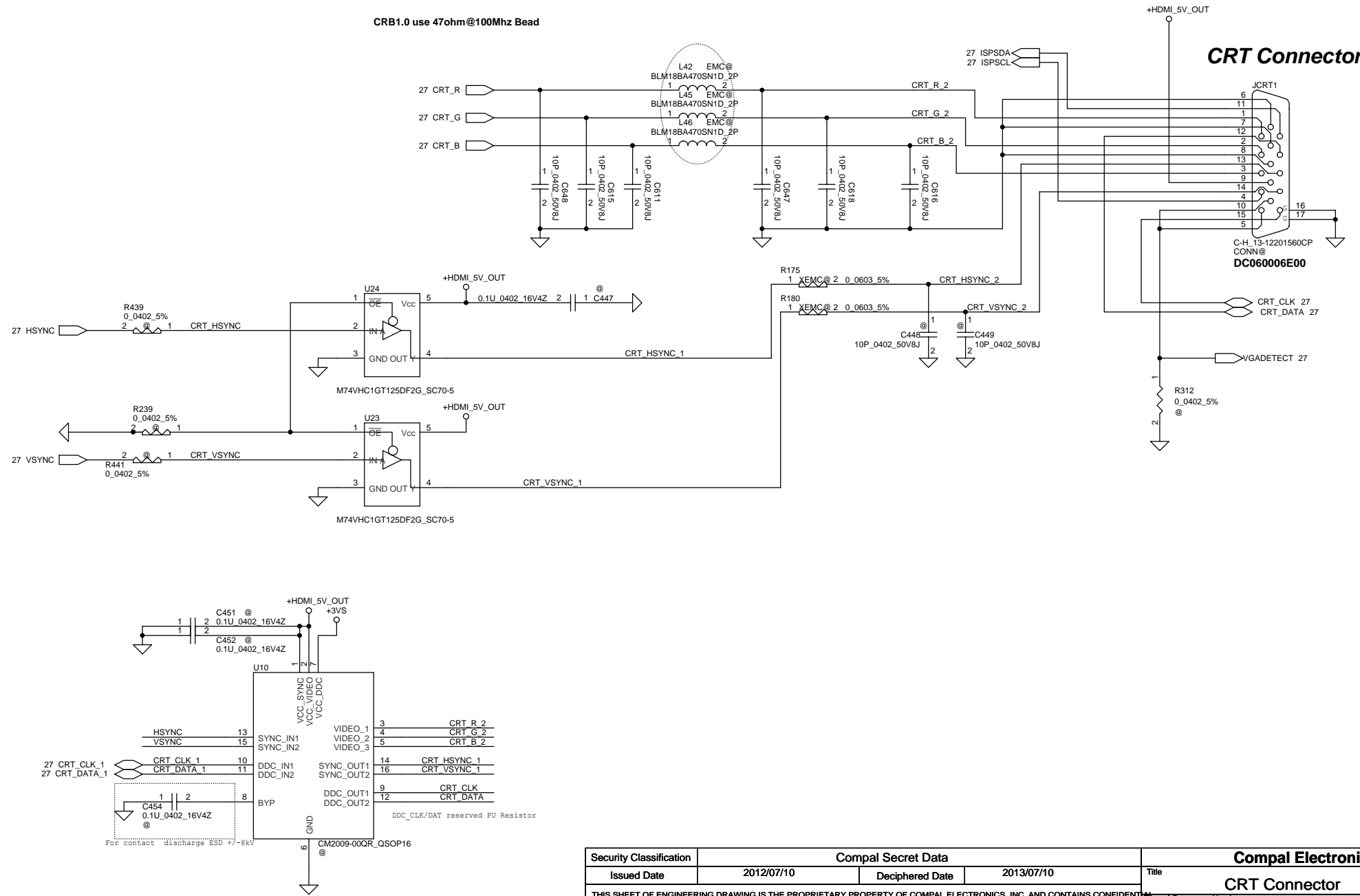
45@

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Issued Date	2012/07/10	Deciphered Date	2013/07/10	HDMI Conn	
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				Size Custom	Document Number V5WE2 M/B LA-9531P Schematic 1.0
				Date: Tuesday, March 26, 2013	Sheet 26 of 52



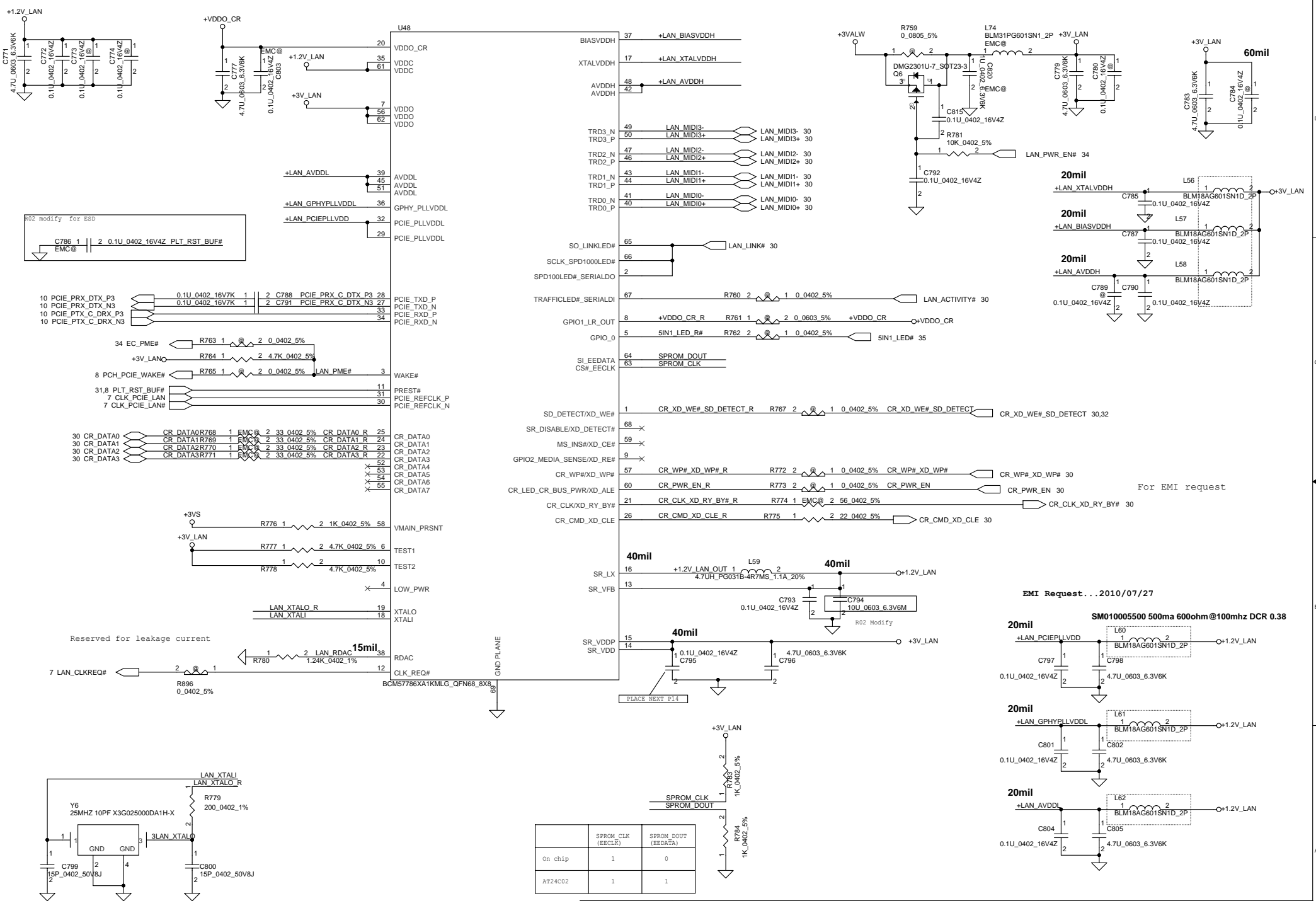
W=40mils

CRB1.0 use 47ohm@100Mhz Bead

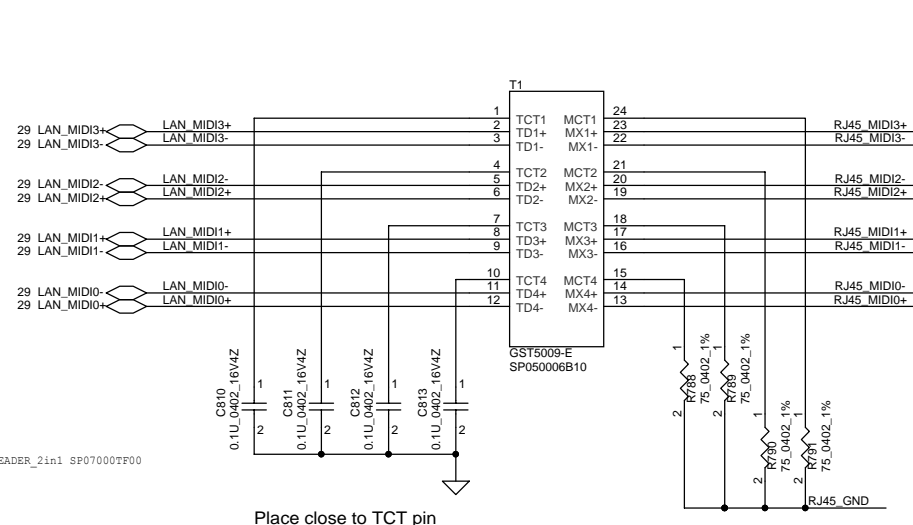


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	
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Date: Tuesday, March 26, 2013				Sheet	28 of 52

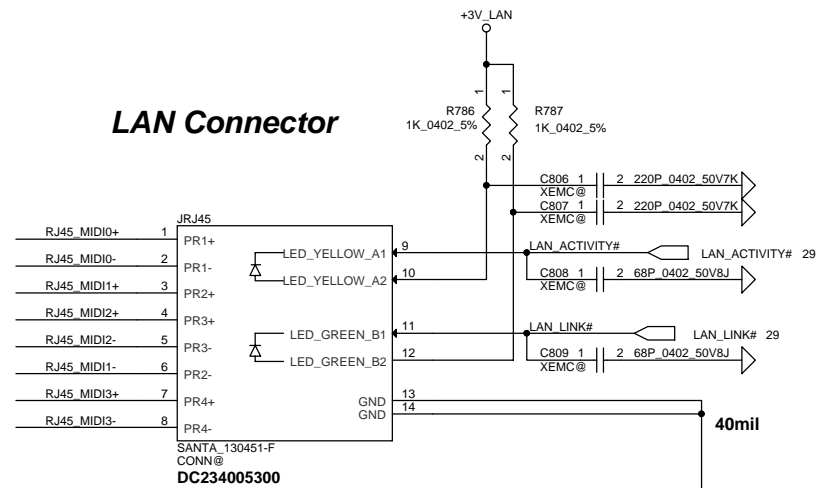
For contact discharge ESD +/-8KV



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<small>Document Number</small> V5WE2 M/B LA-9531P Schematic			<small>Rev</small> 1.0
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LAN Connector



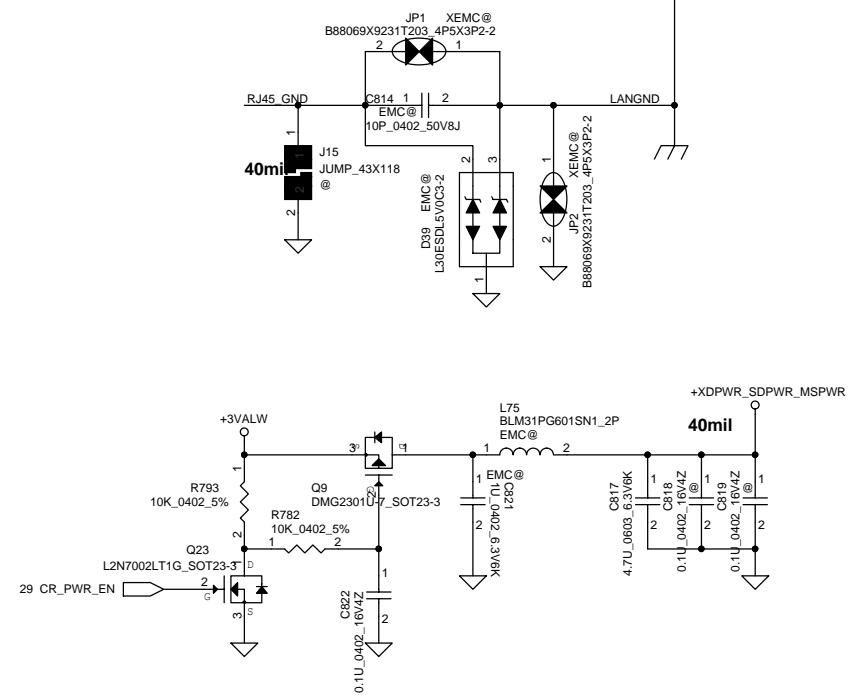
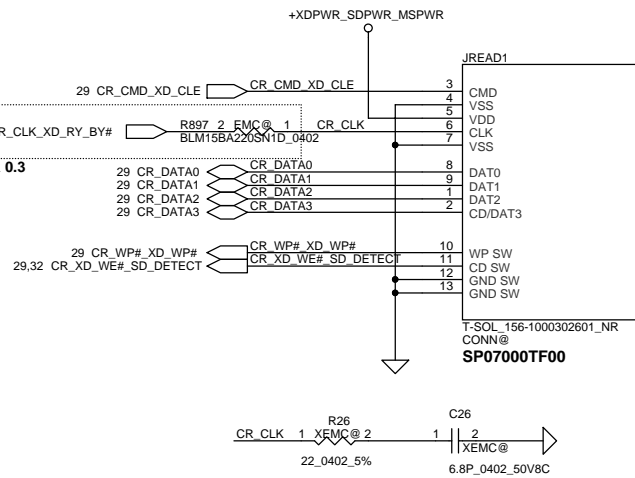
CARD READER_2in1 SP07000TF00

Place close to TCT pin

BOTHHAND: S X'FORM_ GST5009-E LF LAN, SP050006B10
 TIMAG:S X'FORM_IH-160 LAN , SP050006F00
 MHPC:S X'FORM_ NS892403 LAN , SP050008500

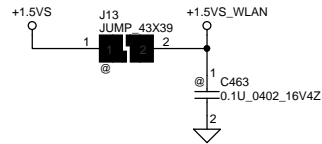
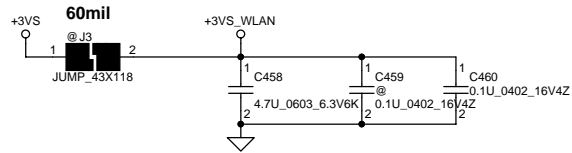
Card Reader Connector

For EMI change to 22 ohm Bead
 SM01000LU00 300ma 22ohm@100mhz DCR 0.3

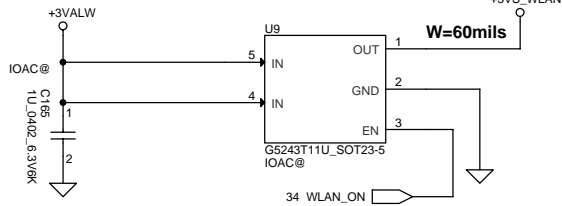
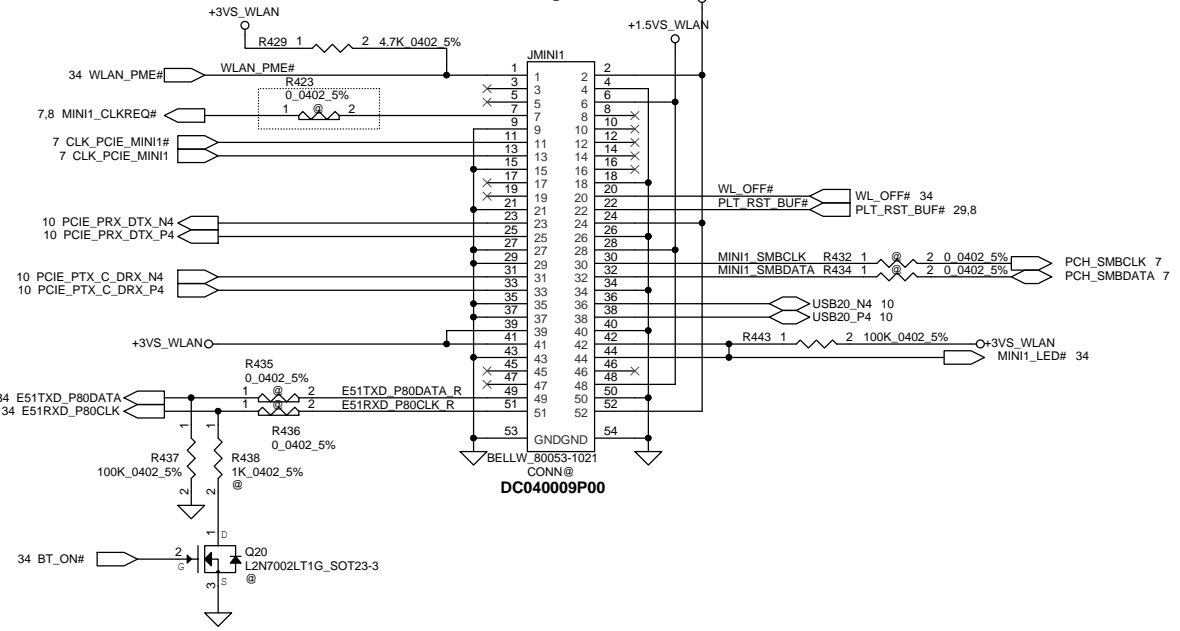


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				V5WE2 M/B LA-9531P Schematic	1.0
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For Wireless LAN



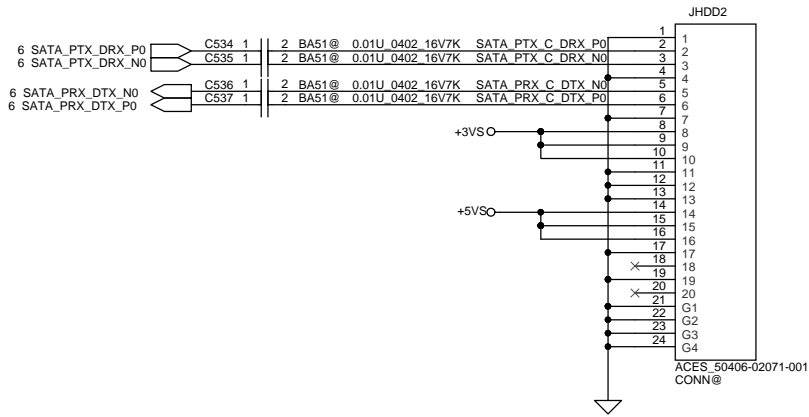
Mini Card Power Rating



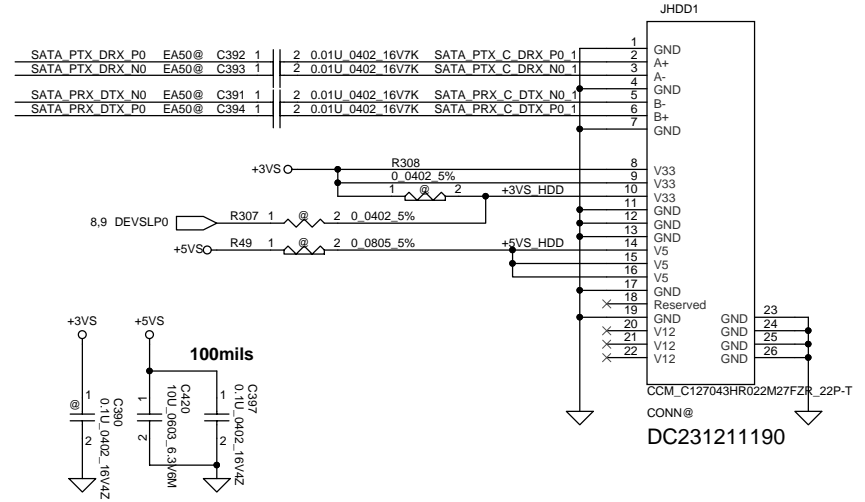
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SATA HDD1 Conn.

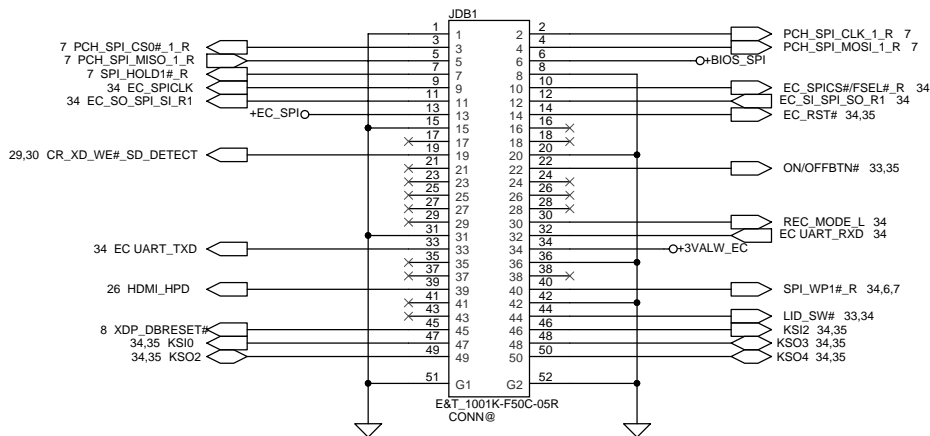
CL 4.0 mm



SATA HDD1 Conn.

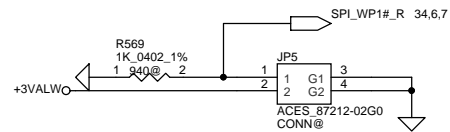


Debug Board

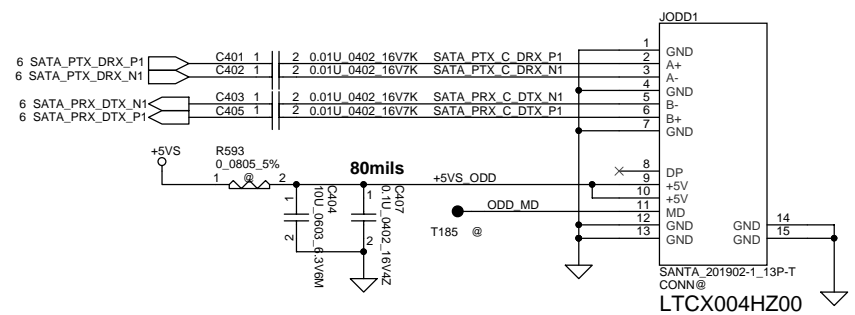


Kill SW

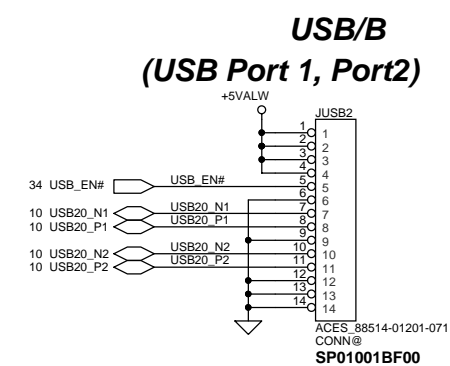
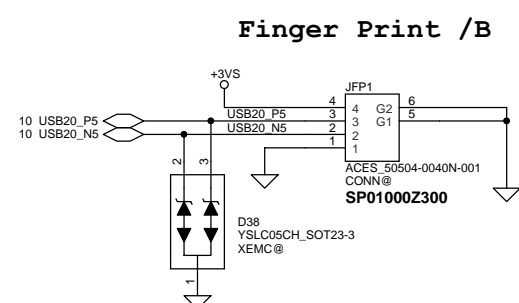
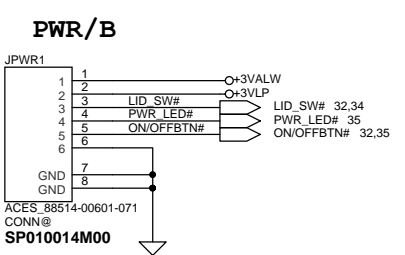
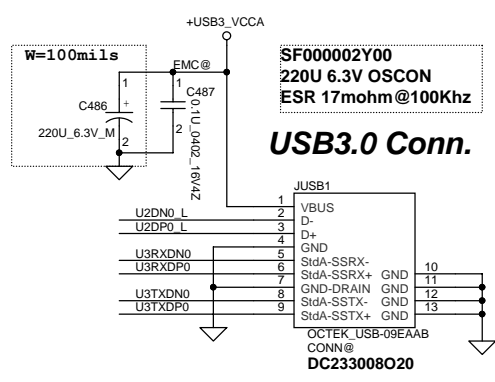
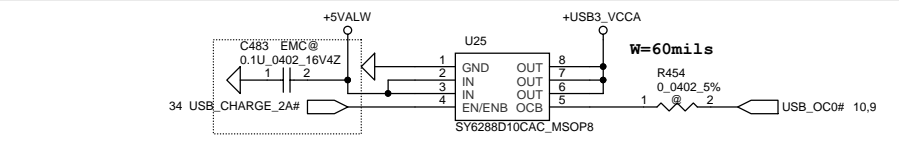
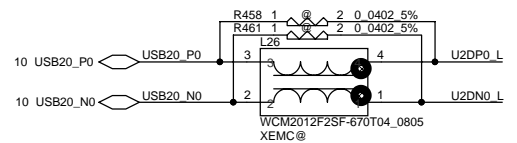
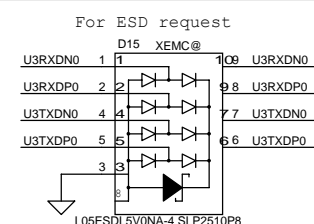
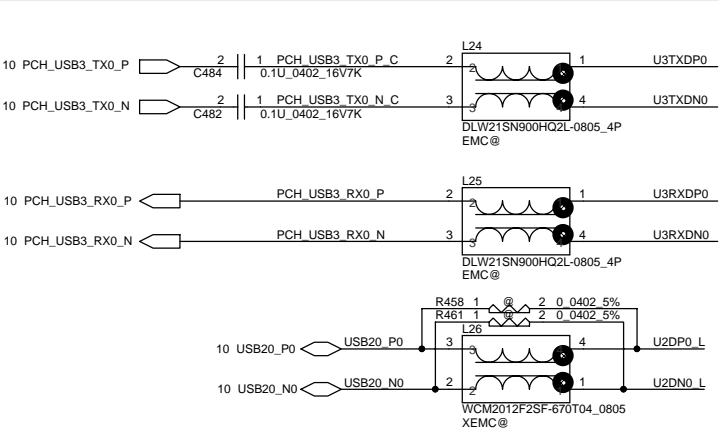
Ctrl (L, 58)	C03, R04 (KSI2, KSO3)
Ctrl (R, 64)	C01, R04 (KSI0, KSO3)
D (33)	C01, R03 (KSI0, KSO2)
F3 (114)	C03, R03 (KSI2, KSO2)
Enter (43)	C01, R05 (KSI0, KSO4)
Space (61)	C03, R05 (KSI2, KSO4)



SATA ODD Conn.

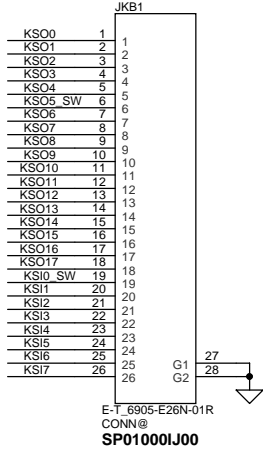


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				V5WE2 M/B LA-9531P Schematic	1.0
Date:				Tuesday, March 26, 2013	Sheet 32 of 52

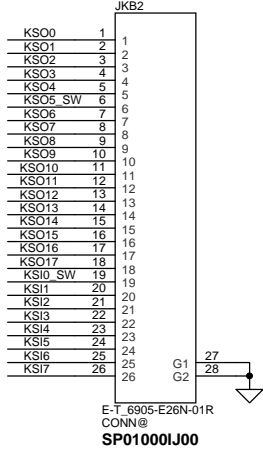


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Date:	Tuesday, March 26, 2013	Sheet	33	of	52

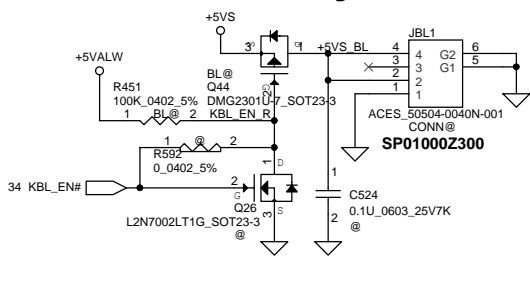
KB Conn.



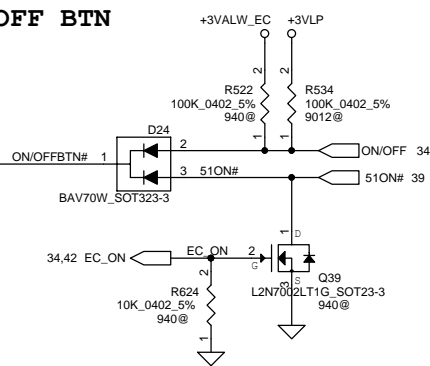
KB Conn.



KB BackLight Conn.



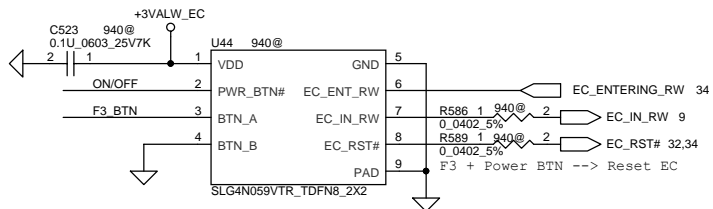
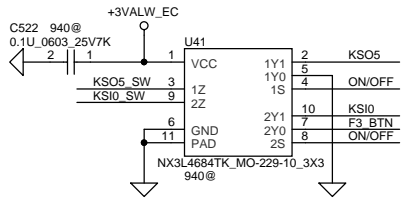
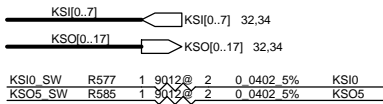
ON/OFF BTN



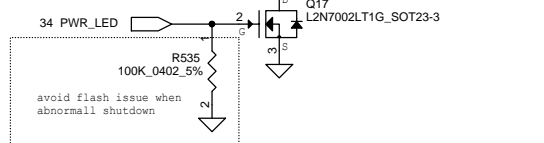
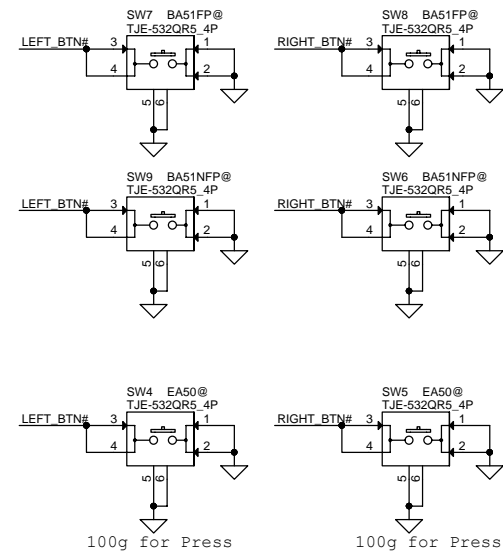
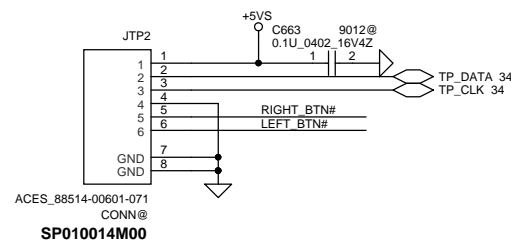
Test Only

TOP

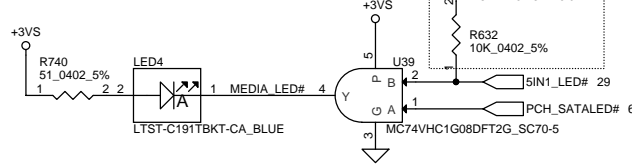
32,33 ON/OFFBTN#



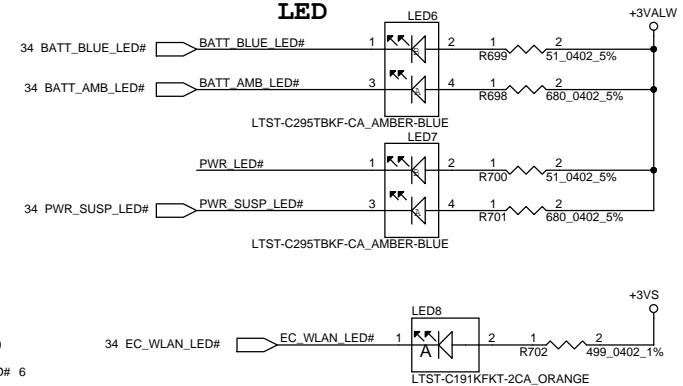
To TP/B Conn.



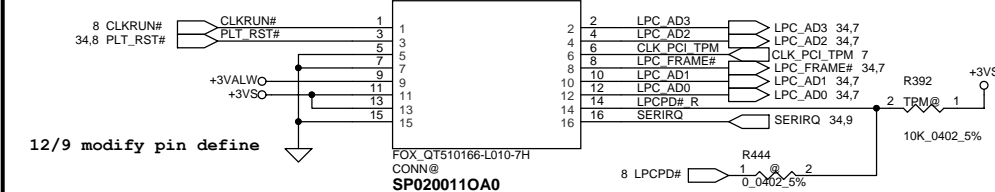
HDD LED



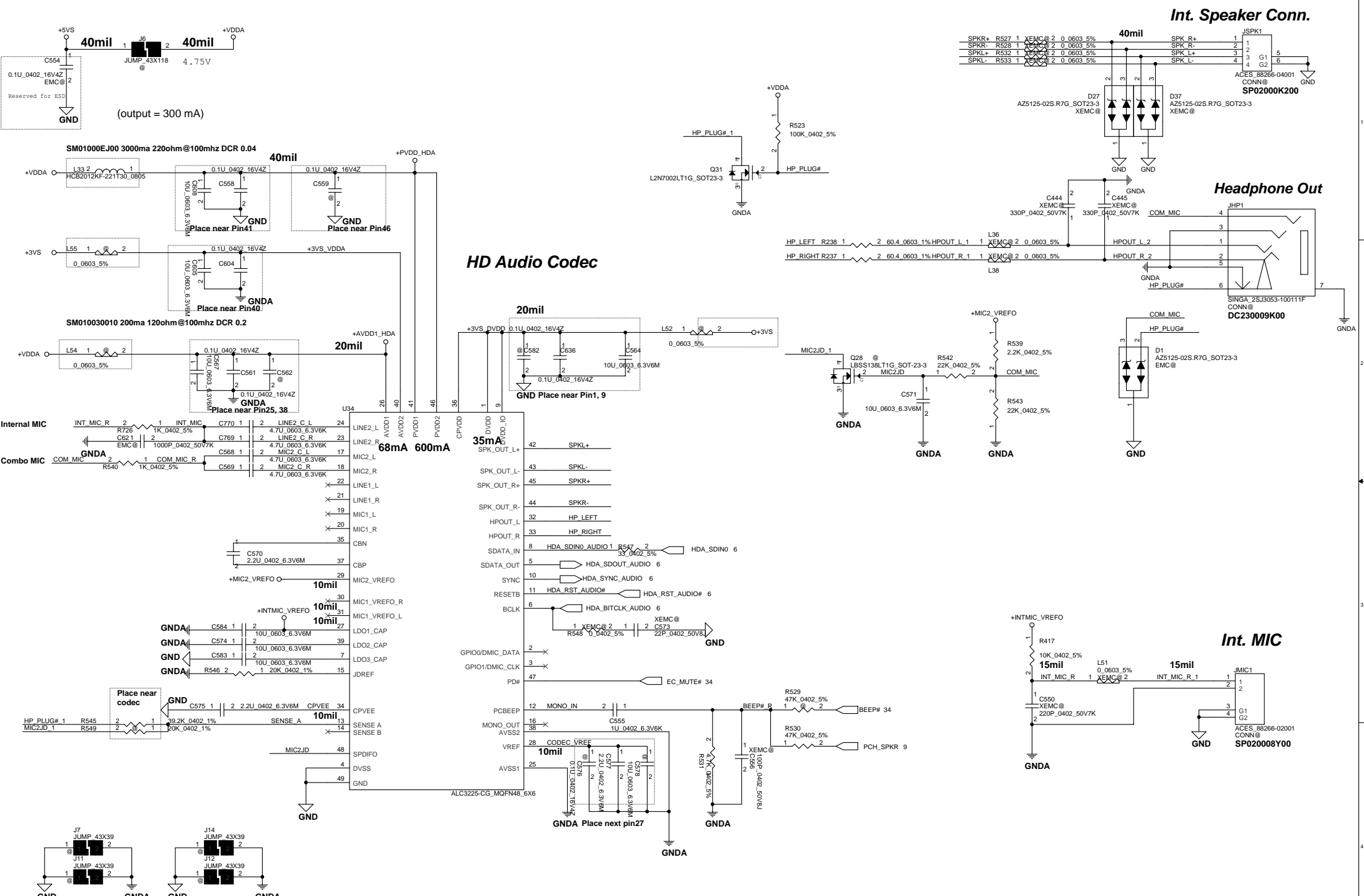
LED



TPM Board



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HD Audio Codec

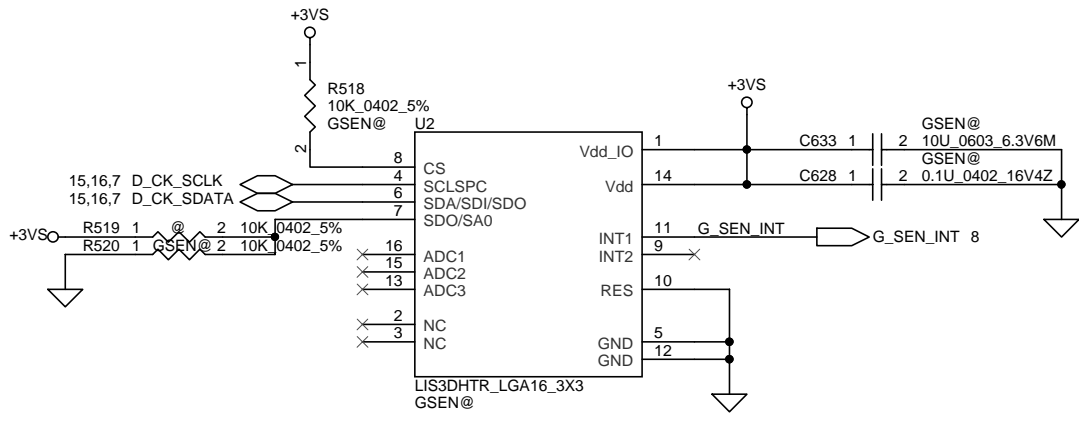
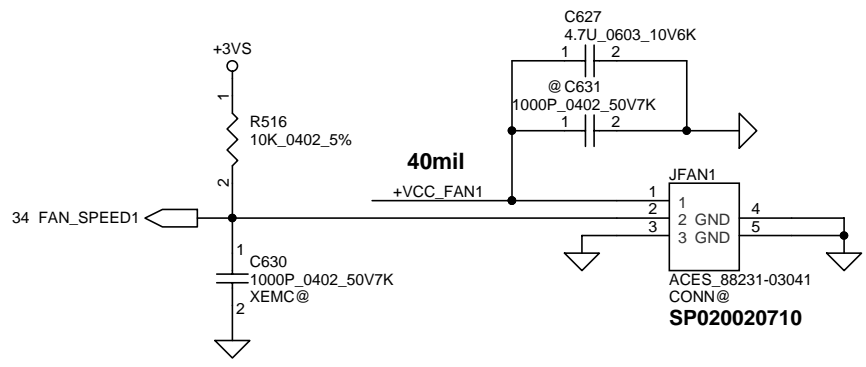
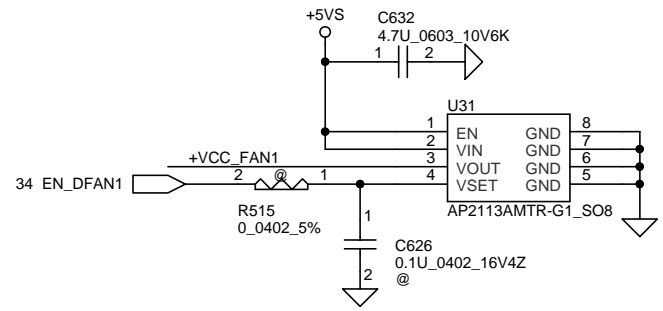
Int. Speaker Conn.

Headphone Out

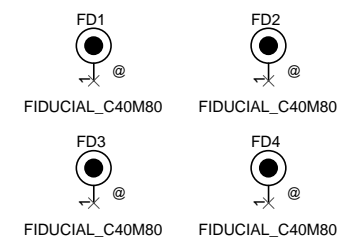
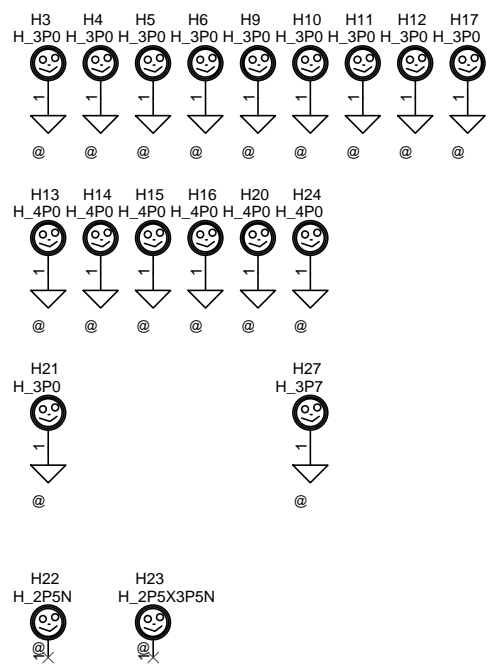
Int. MIC

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FAN1 Conn



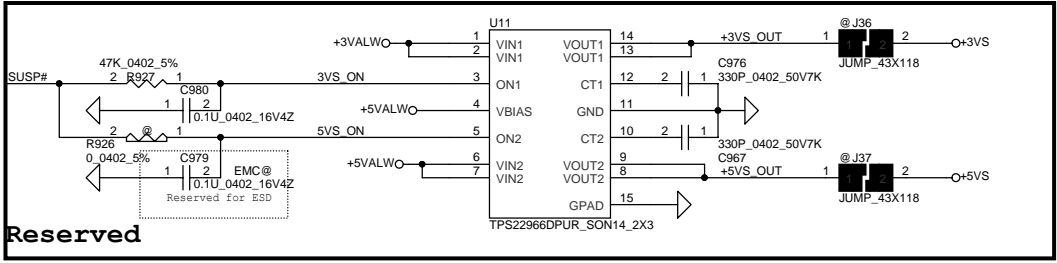
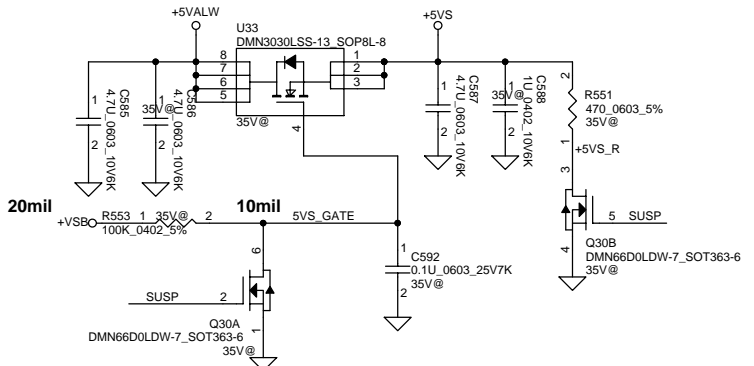
LIS3DH
 SA0 ->0, Address is 0011 000 (0x30h)
 SA0 ->1, Address is 0011 001 (0x32h)



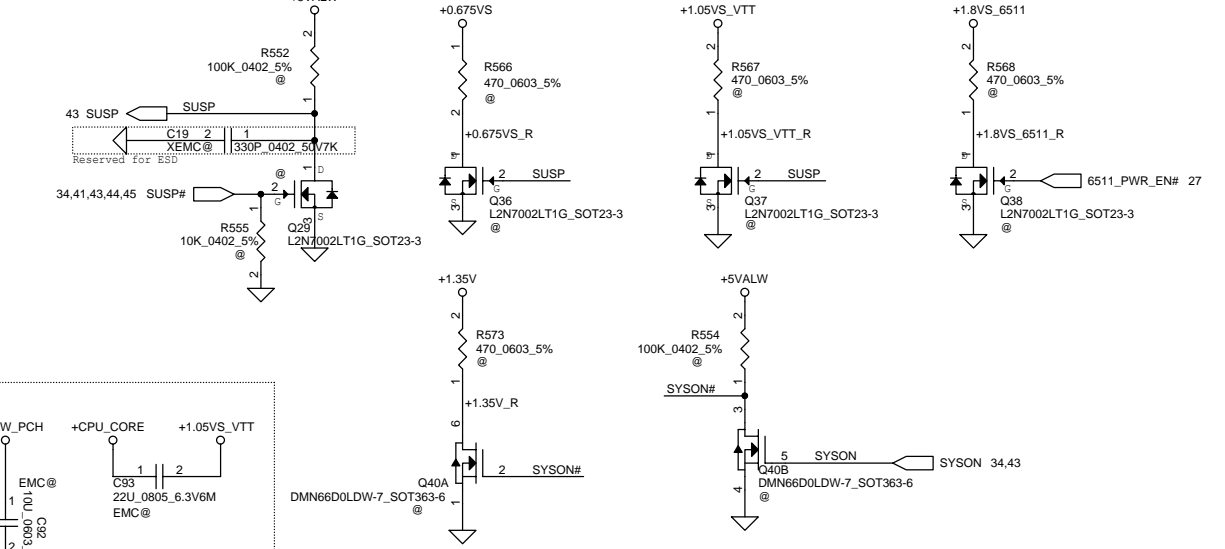
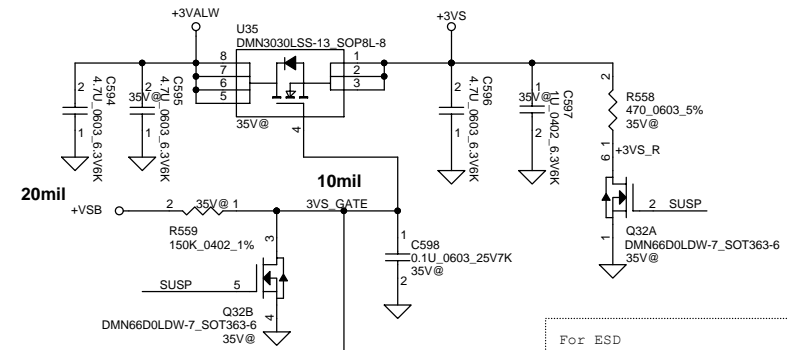
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Normal Platform (Not support M-STATE and Deep Sleep)

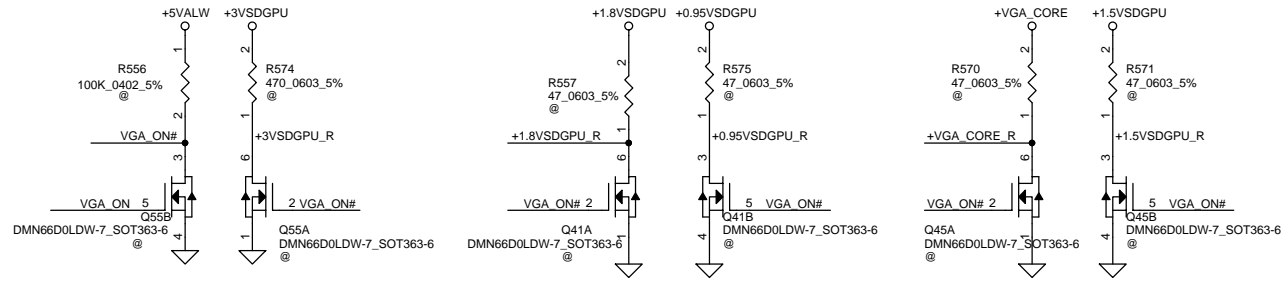
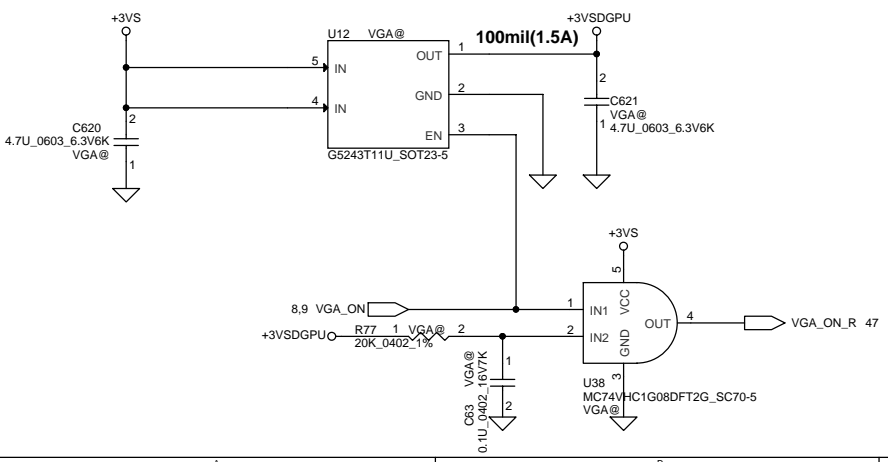
+5VALW TO +5VS



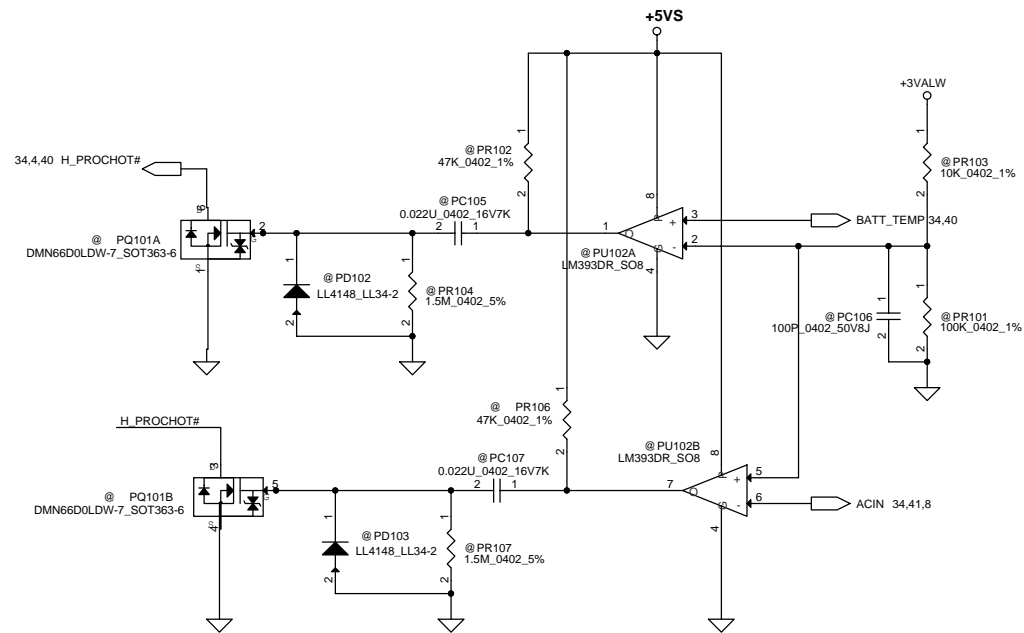
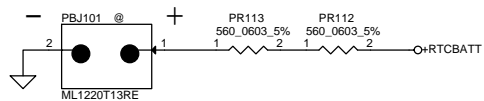
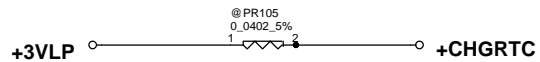
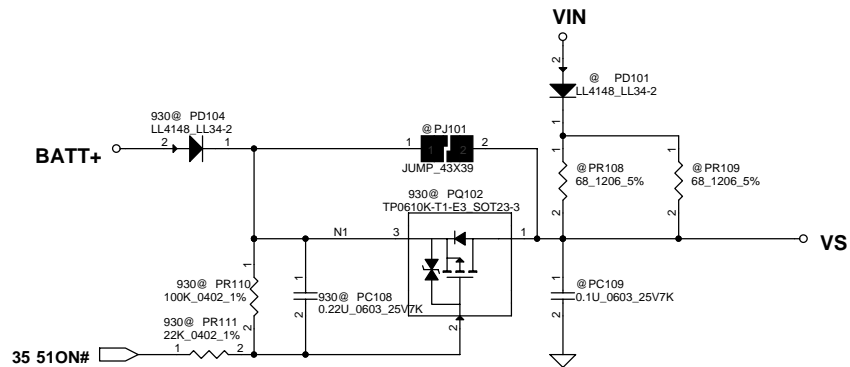
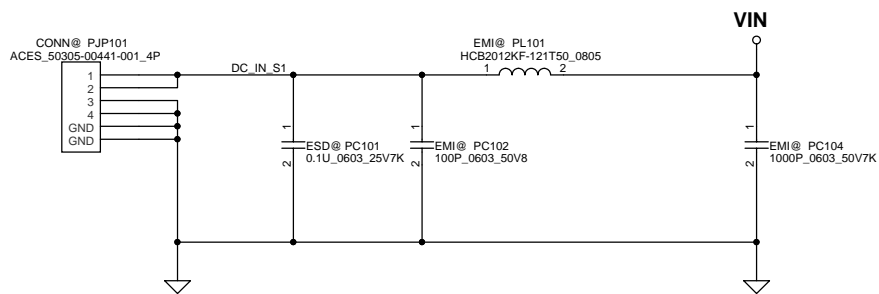
+3VALW TO +3VS



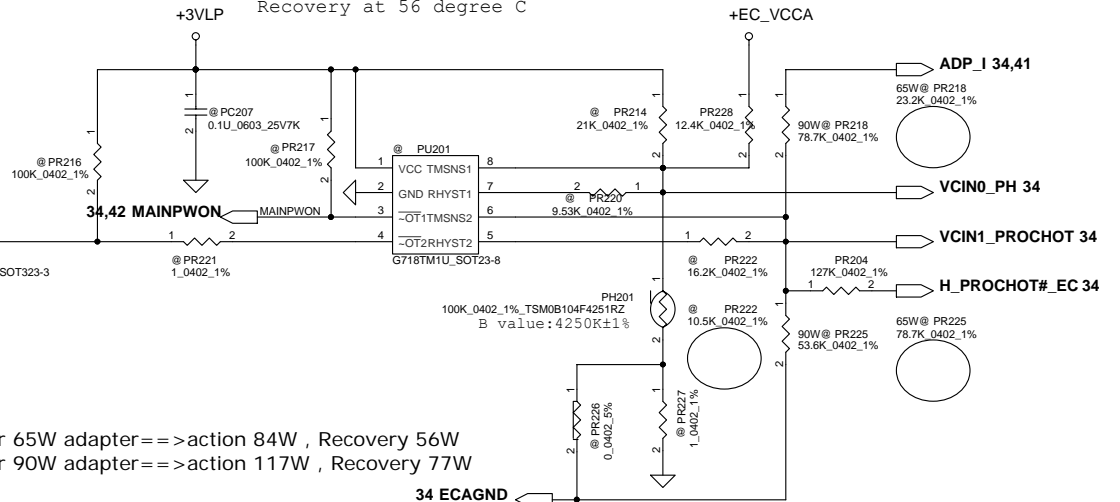
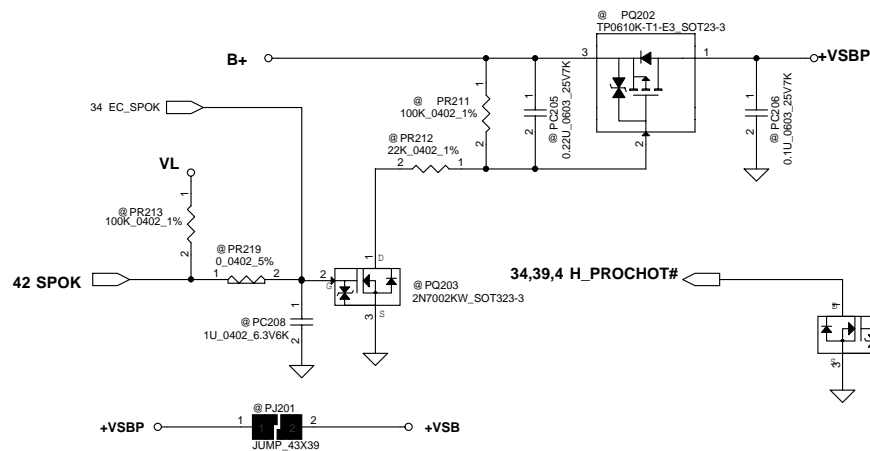
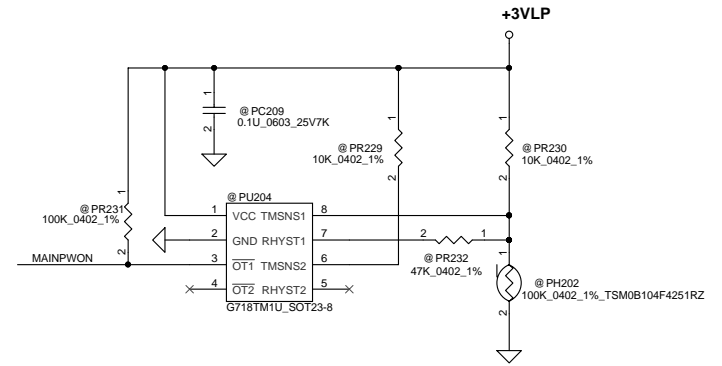
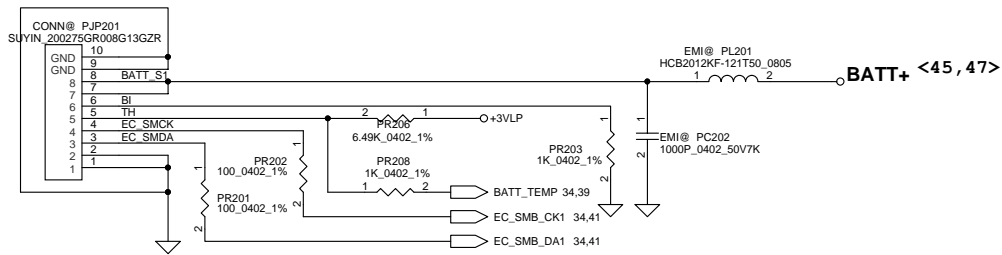
+3VS to +3VSDGPU for GPU



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For KB9012 OTP	
92	1.2V, Active
56	2.255V, Recovery

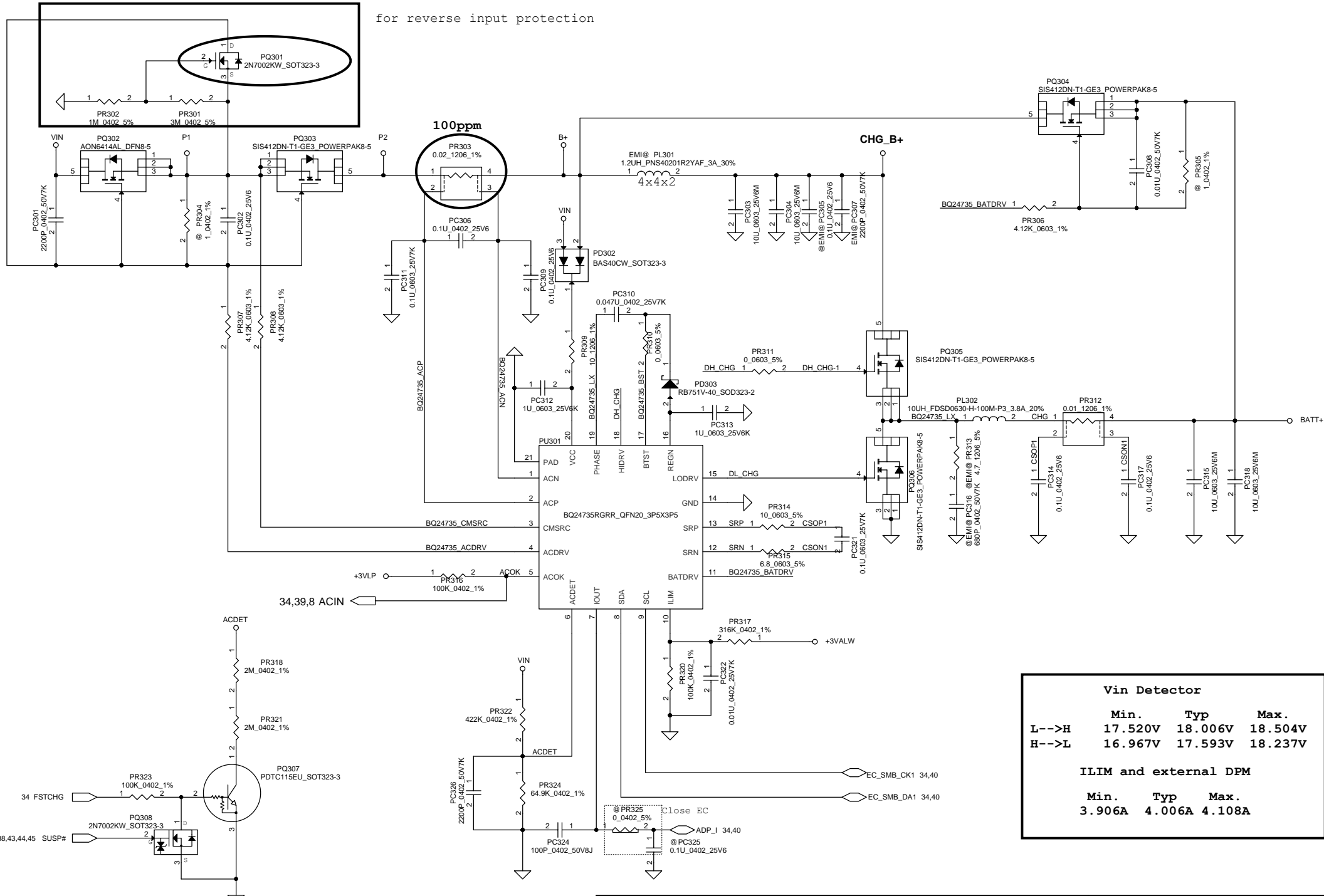
For KB9012 sense 20mΩ	Active	Recovery
65W	84W, 1.2V	56W, 1.2V
90W	117W, 1.2V	77W, 1.2V
120W		

PH201 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

For 65W adapter ==> action 84W , Recovery 56W
For 90W adapter ==> action 117W , Recovery 77W

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				BATTERY CONN / OTP	
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Size	Document Number	Rev			
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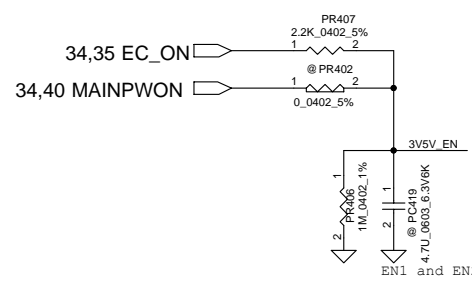
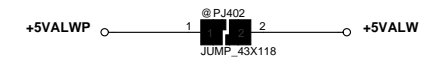
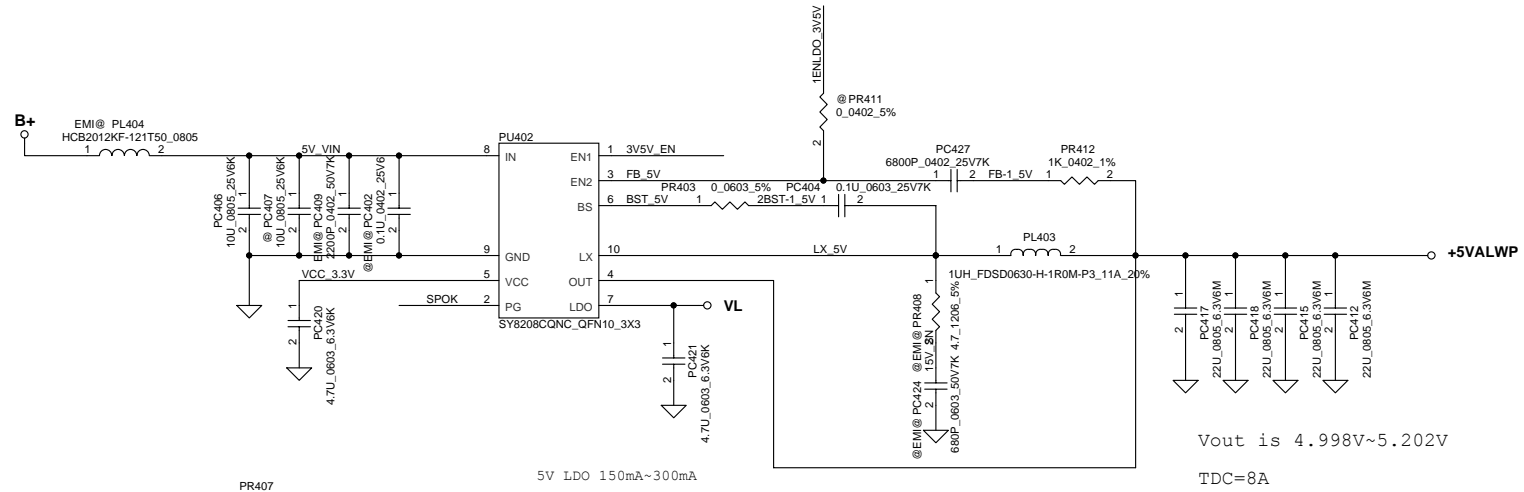
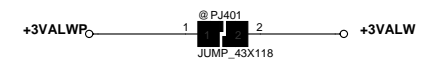
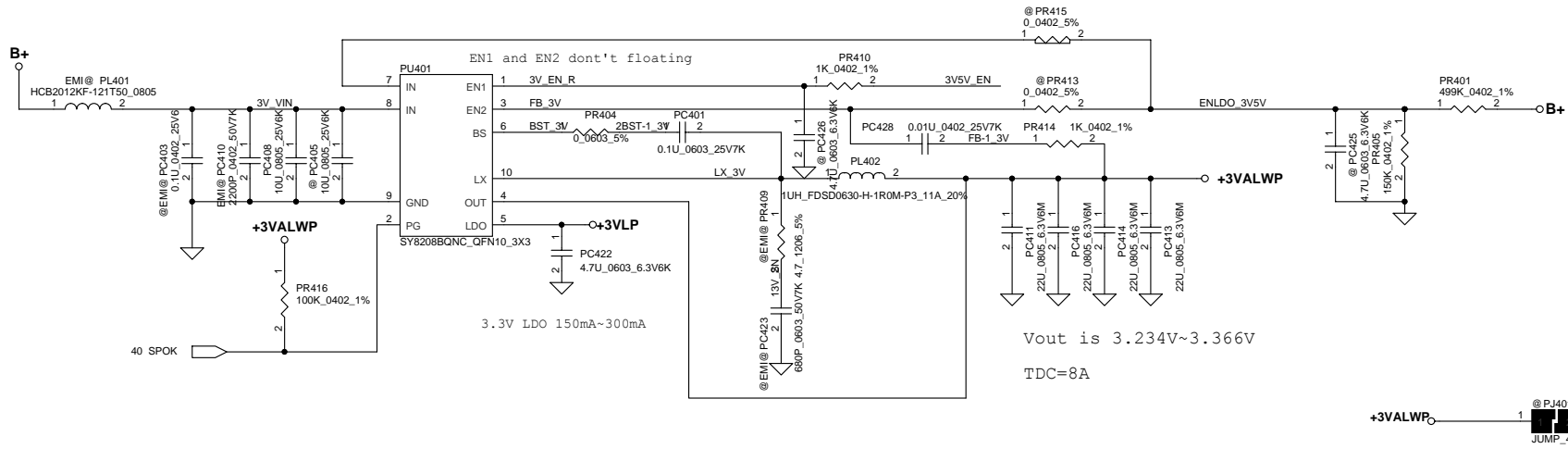
for reverse input protection



Vin Detector			
	Min.	Typ	Max.
L-->H	17.520V	18.006V	18.504V
H-->L	16.967V	17.593V	18.237V

ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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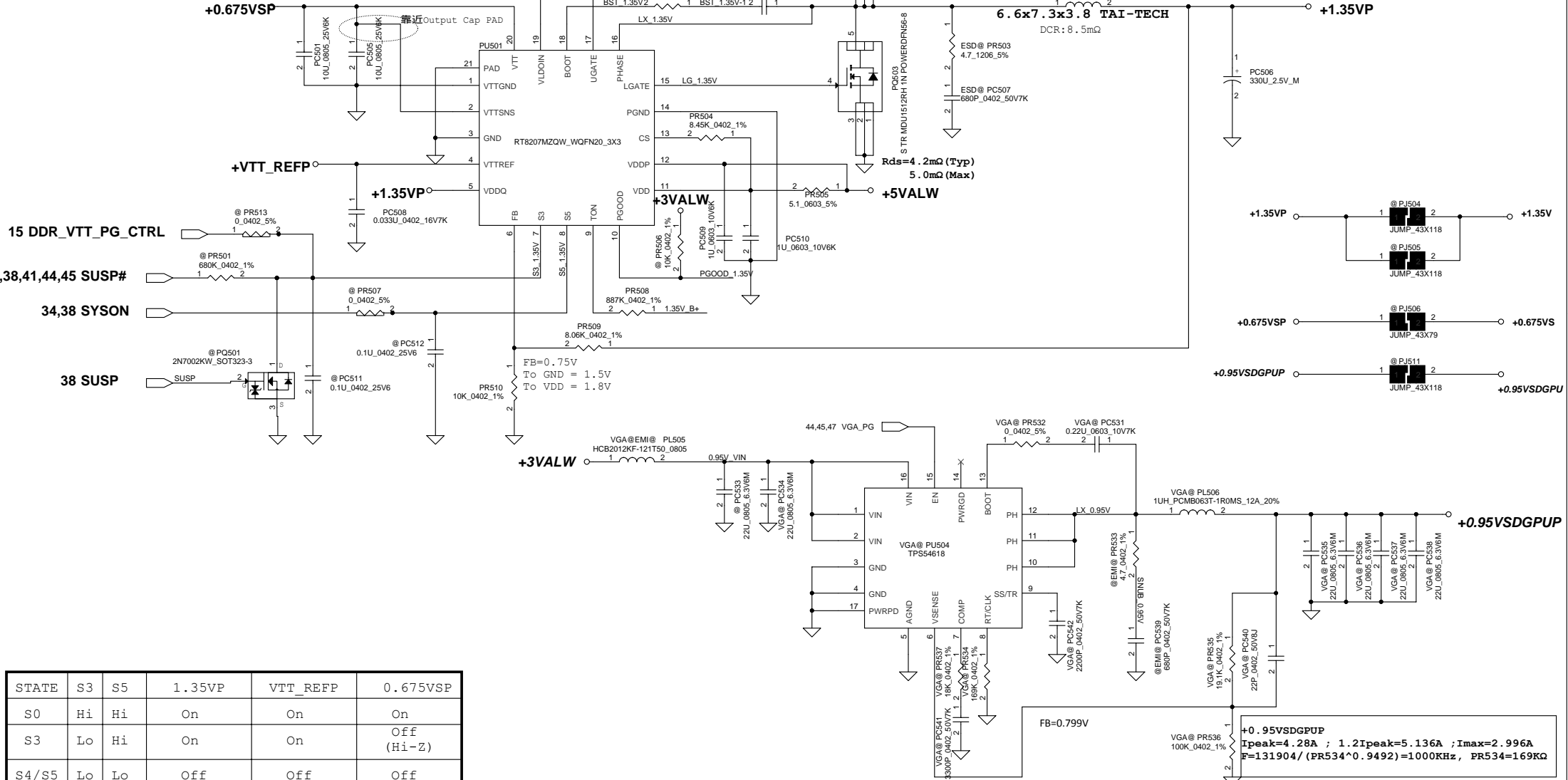


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+1.35VP
 $I_{peak} = \max\{0.7 \cdot I_{budget}, 1st + 2nd \text{ max loading}\}$
 $I_{peak} = \max\{12.34 \cdot 0.7, 4.2 + 8.14\}$
 $I_{peak} = 12.34A ; 1.2I_{peak} = 14.808A ; I_{max} = 8.638A$
 $1/2\Delta I = 0.7353A (F=300K \text{ Hz})$
 $PR504 = (1.2I_{peak} - 1/2\Delta I) \cdot R_{ds(on)} \cdot \max\{1.2/9uA = 8.45Kohm\}$
 choose $PR504 = 8.45Kohm$ (for safety $> 1.2I_{peak}$)
 $R_{ds(on)} = 5.0m \text{ ohm (max)} ; R_{ds(on)} = 4.2m \text{ ohm (typical)}$
 $I_{limit_min} = (8.366K \cdot 9uA) / (5.0m \cdot 1.2) = 15.058A$
 $I_{limit_max} = (8.535K \cdot 11uA) / (4.2m \cdot 1.2) = 22.352A$
 $I_{ocp} = I_{limit} + 1/2\Delta I = 15.79A \sim 23.09A$
 $I_{ocp(min)} > 1.2I_{peak}$

2012/9/6

OVP=110% 115% 120%



STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

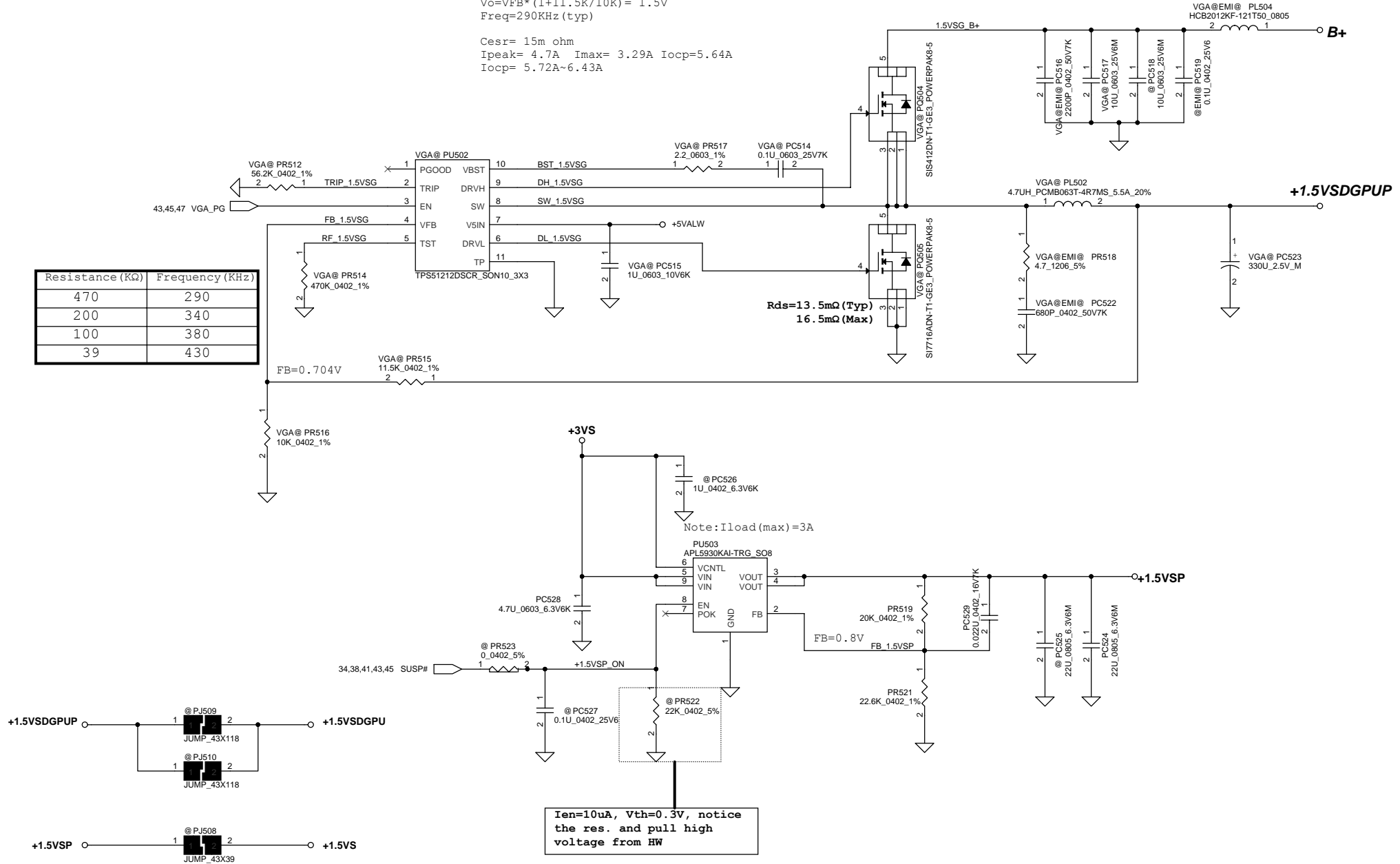
Note: S3 - sleep ; S5 - power off

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Note: Use VCCSA_SEL to switch High & Low Level for VDD111

$V_{FB} = 0.704V$
 $V_o = V_{FB} * (1 + 11.5K/10K) = 1.5V$
 $Freq = 290KHz (typ)$
 $C_{esr} = 15m\ ohm$
 $I_{peak} = 4.7A$ $I_{max} = 3.29A$ $I_{ocp} = 5.64A$
 $I_{ocp} = 5.72A \sim 6.43A$

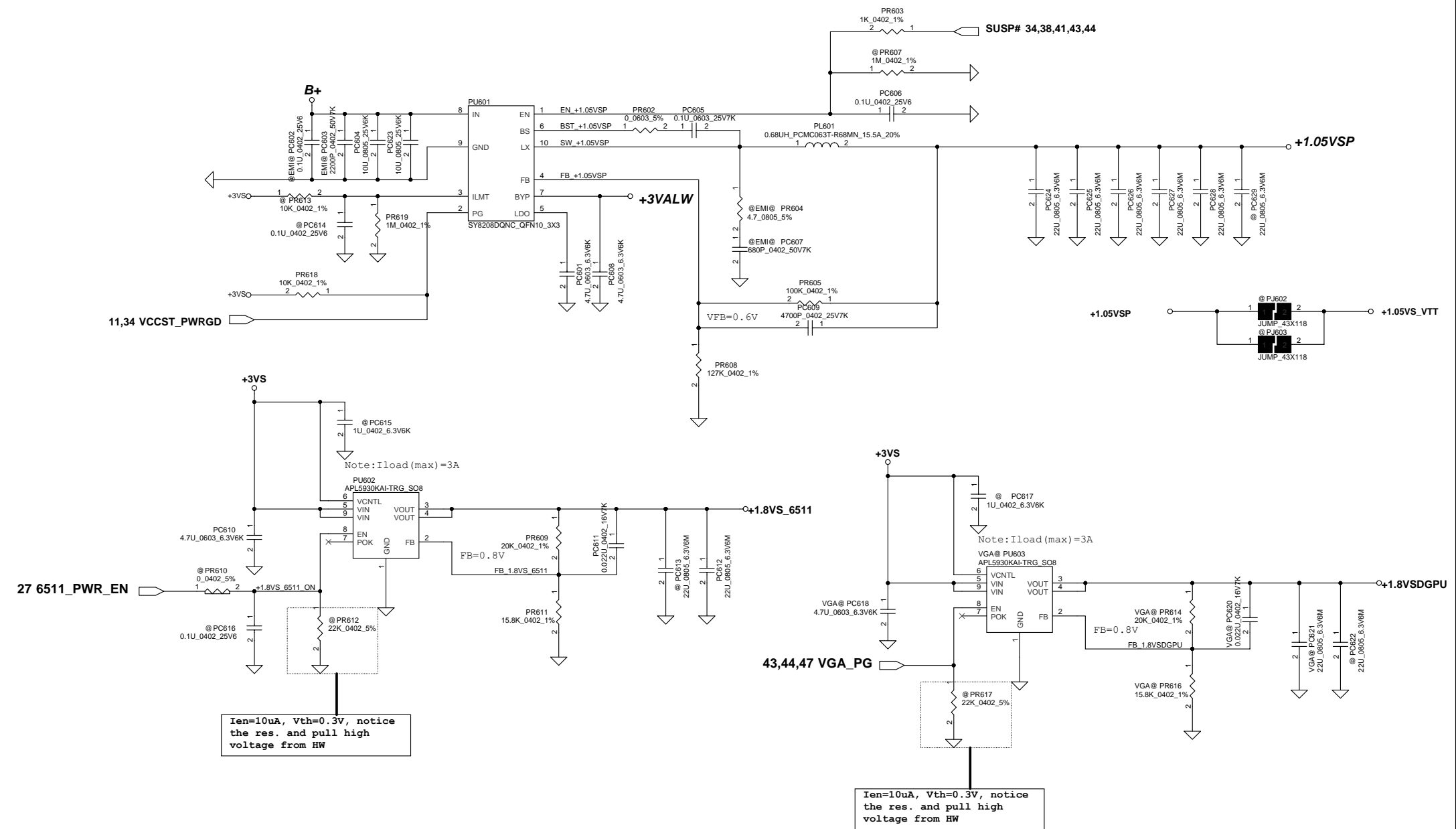
Resistance (KΩ)	Frequency (KHz)
470	290
200	340
100	380
39	430



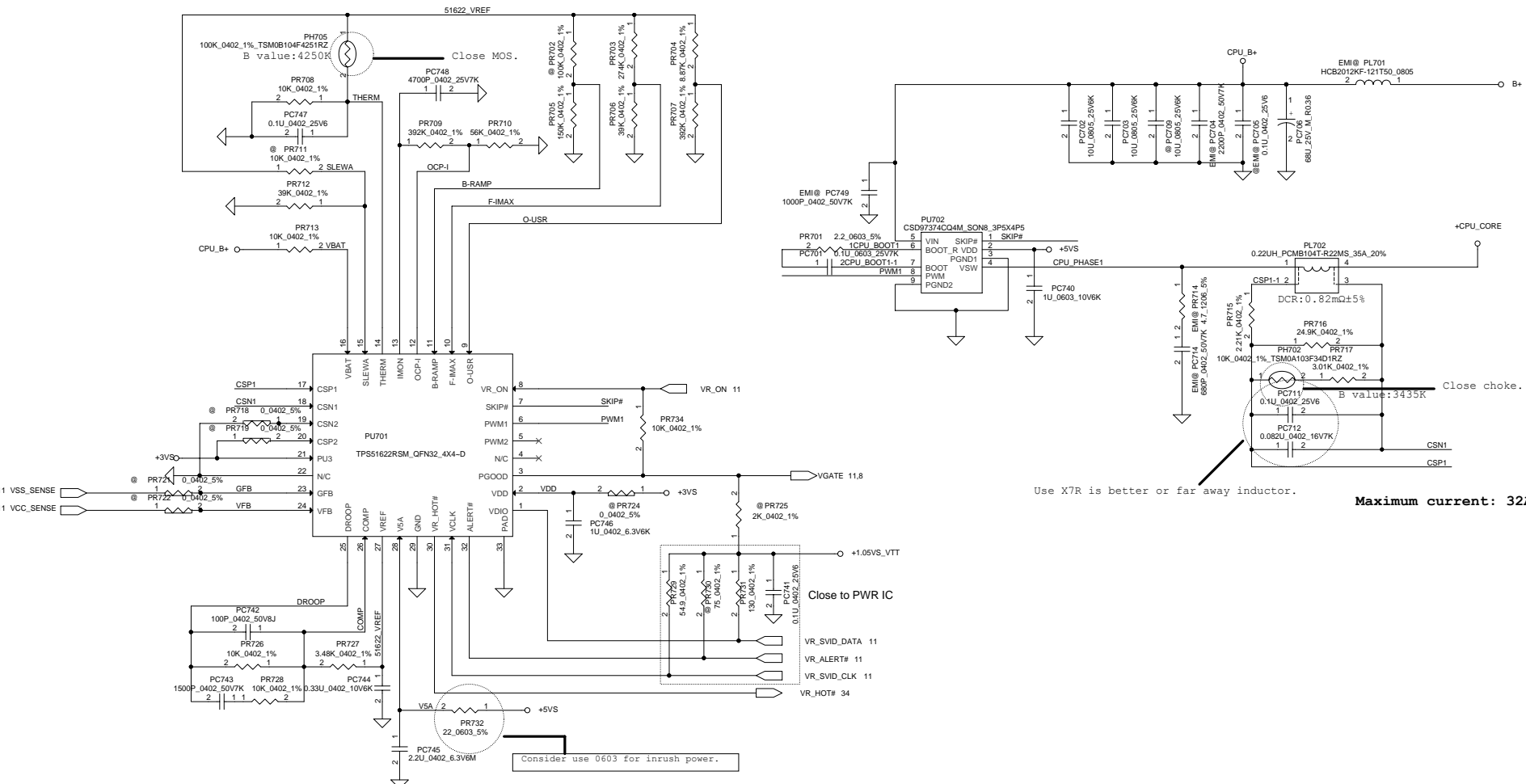
$I_{en} = 10\ \mu A$, $V_{th} = 0.3V$, notice
 the res. and pull high
 voltage from HW

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+1.05VSP I_{peak}=5.36A ; I_{max}=3.752A ; 1.2I_{peak}=6.432
 Delta I=0.xxxxA->1/2Delta I=0.xxxxA, F= 800K Hz (typ)



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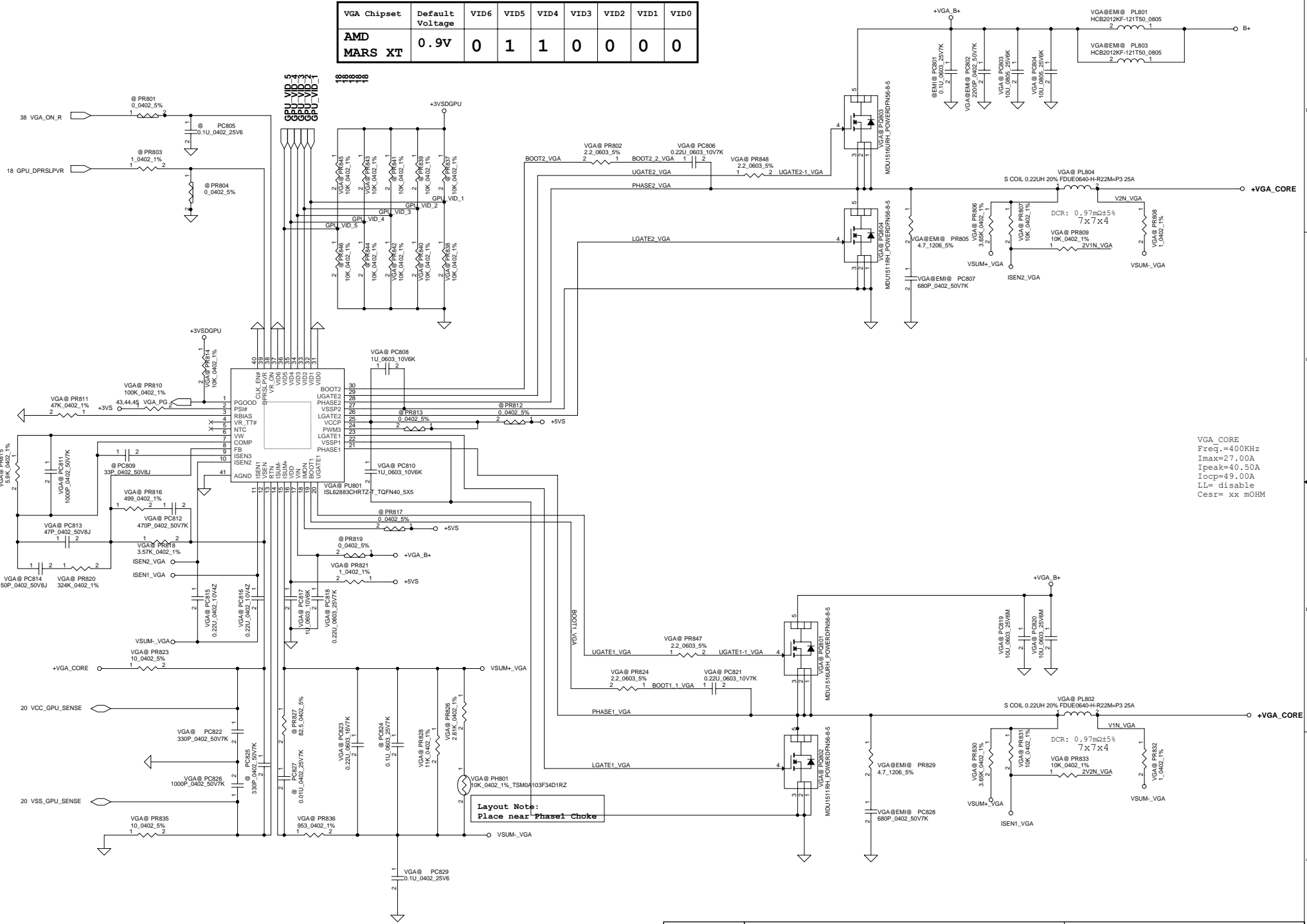
Use X7R is better or far away inductor.

Maximum current: 32A

VIN	12V-20V
MAX current	32A
Thermal current	10A
Dynamic current	27A
Over current level	45A
Switching frequency	600KHz
Boot voltage	1.7V
DC Load- line	2m Ohm

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				+CPU_CORE	
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VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
AMD MARS XT	0.9V	0	1	1	0	0	0	0

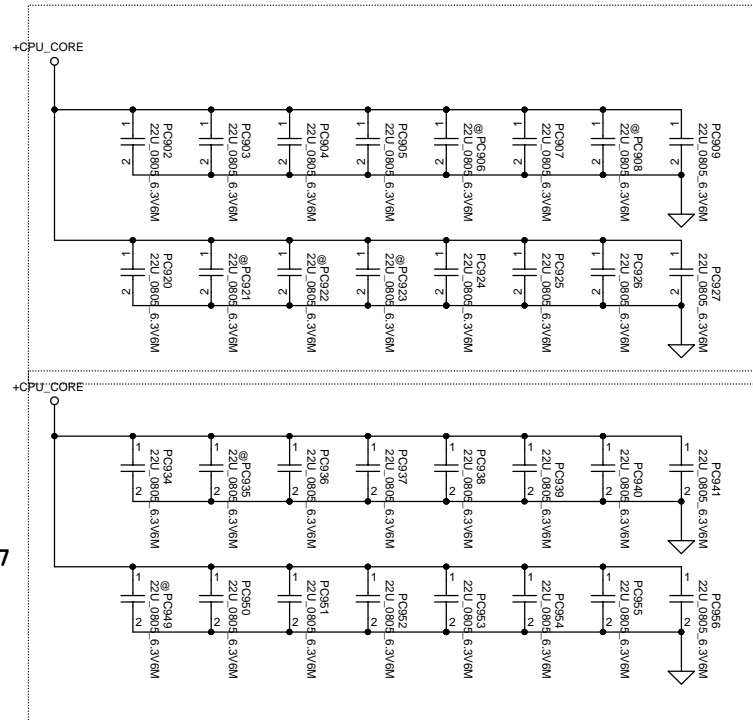


VGA_CORE
 Freq.=400KHz
 I_{max}=27.00A
 I_{peak}=40.50A
 I_{ocp}=49.00A
 IL=disable
 C_{esr}=xx mOHM

Layout Note:
 Place near Phase1 Choke

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PWR Rule
CPU DCLL=1.5m ohm dedign 330uF/9m *0, 22uF *30

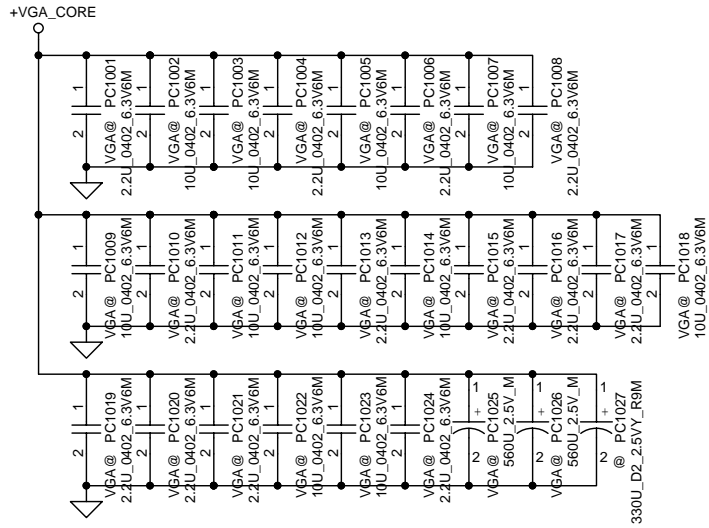


For BOT side

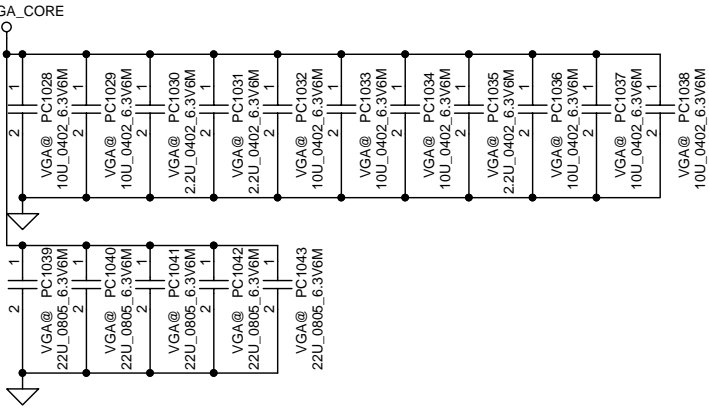
For TOP side

22u *25, @*7

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**AMD MARS
GPU_CORE
560uF*2+330uF*1
10uF*8+2.2uF*16**



**AMD MARS
meet ripple
22uF*5+10uF*11**

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Tune VGA sequence	Tune VGA sequence		VGA	PR801 change to 20K Add PC805, PR814 Delete PR615, PC619, PR511, PC513, PR530, PR531, PC530	11/06	DVT
2	Module Design	Module Design change 3/5V solution		3/5V		11/13	DVT
3		Change RTC type to non-charge		39	Un-pop PR112, PR113	11/13	DVT
4		Check no need keep with HW		39	Delete PR112, PR113, PB101	11/20	DVT
5	EMI request			EMI	Add PR518, PC522, PR714, PC714, PR829, PC828, PR806, PC807, PC749 Change PR701 to 2.2	11/20	DVT
6	EMI request	EMI confirm remove		EMI	Delete PL102, PC103, PC101, PL202, PC201 and PL703	11/26	DVT
7	Costdown			42	Change PL402, PL403 from 5x5x3 to 7x7x3	12/13	DVT2
8		SY8208B/C update		42	Add PR411, PR413	12/22	DVT2
9	+1.05V ripple close upper and mean too low	Adjust output voltage and add Cff		45	Add PC609 into 4700P Change PR608 from 133K to 127K	12/22	DVT2
10	VGA_CORE can't disable	Modify VR_ON to VGA_ON_R net		47	Change PR801 from 20K to 0 Reserve PC805	01/04	DVT2
11		Improve CPU transient character		46	Change PR709 from 150K to 390K, PR732 from 10 to 22, PC745 from 1U to 2.2U, PC711 from 0.082U to 0.1U	01/09	DVT2
12		Improve CPU transient character		48	Unpop PC902	01/09	DVT2
13		Tune sequence		42	Change PC428 from 4700p to 10n, PC427 from 0.047u to 6.8n	02/04	PVT
14		0 ohm reduce			Change PR801, PR507, PR513, PR523 to R-pad	02/22	PVT
15		To meet MARS/AMD ripple SPEC		49	Add PC1028~PC1043	02/22	PVT
16		Provide 3/5V PG signal to EC		42	Add PR416	02/22	PVT
17	EMI request	Modify H-Gate resistor		47	Change PR847, PR848 from 0 to 2.2	02/25	PVT
18	ESD request			39	Add PC101 into 0.1uF	02/26	PVT
19	ESD request			43	Add PC521, PR503, PC507	02/26	PVT
20		Use HW to control VCIN1 function		40	Add PR204	03/05	PVT
21	ME issue	Shrink component to reduce Z height			Change PC303, PC304, PC315, PC318, PC517, PC819, PC820 from 0805 to 0603	03/26	PVT2

Recovery at PVT phase

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A --> B1 Change List

1203A-----
 1.Page11, R169 change to @
 2.Page36, Mound R417 (Cancel AMIC@)
 3.Page18, R898, R899, R409, D22 change BOM Structure to VGA@
 4.Page34, R485, R483 change to 90L2@
 R479, R478 change to 940@
 5.Page35, C663, SW4, SW5 change to 90L2@
 6.Page19, Delete R1035, X7601/X7603/X7604
 7.Page17, R1006 change to VGA@
 8.Page06, R306 add BOM structure UMA@
 9.Page06, C153, C154 change to L5P_0402
 10. Page18, C848, C849 change to L2P_0402
 11. Page07, C2, C3 change to 10P_0402
 1129A-----
 1. Page32, JODD1.11 Reserve a TestPoint for DFT
 2. Page29, Pop C779, C783
 3. Page17, Update U51 BOM Structure for BOM Select
 4. Page04, Add QDJUC@ BOM Structure for U1
 1128A-----
 1. Page18, Add D22 to prevent GPU ACIN leakage
 2. Broadcom recommend modify(Add Component Function Field is 45.1)
 Page29, Add C803 0.1uF to U48.20 (VDDO_CR),
 Page29, Add L74 (BLM31PG601SN1) between Q6.1 and +3V_LAN
 Add C820 (1uF) to Q6.1
 Page30, Add L75 (BLM31PG601SN1) between Q9.1 and
 +XDPWR_SDPWR MSPWR
 Add C820 (1uF) to Q9.1
 3. Page18, Change L69 to R_Short
 4. Page20, Change L72 to BLM18AG121SN1D (the same to L71)
 5. SW confirmed function
 Page08, unpop R245,d21 (ACPRESENT tp PCH no need)
 Page36, unpop R529 (EC_BEEP no need)
 6. Default EC_SCI# to GPIO34
 Page06, Pop R937
 Page09, Unpop R66
 7. Reserve DGPU_HOLD_RST# direct to PLTRST_VGA# path
 Page08, Add R405 0ohm connect DGPU_HOLD_RST# and PLTRST_VGA#
 8. Page35, Chagne R702 to 680ohm (ME ConfIr)
 9. Page35, Delete SW1 (debug) for Layout convenience
 10. Page24, Change L6 to (4.7uH SH00000GS00) same as Q5WV8
 11. Page29, Change RP22 to R768,R769,R770.R771 for SD 3.0 EMI
 1127A-----
 1. Page24, Change U50.11 connect from L6.2 to L6.1
 2. Page34, Change R502 from R_short to 940@ 0ohm
 3. Page36, Change R237,R238 to 60 Ohm(Codec vendor recommend)
 4. Page09, Add R67 for EC_SCI# -> GPIO 10 option
 1126A-----
 1. Page36, Delete D26 (ESD Confirm)
 2. EMI part Schematics modify(EMI confirm1123)
 Page26, Change R368,R369,R370,R371,R372,R373,R374,R375 to 0403
 R_short
 Page28, Change R175,R180 to 0603 R_short
 Page36, Change L36,L38,L51,R527,R528,R532,R533 to 0603 R_short
 Page32, Delete C408,C398
 Page33, Delete R453,R455,R456,R457
 3. Page38, Change 3/5 VS circuit BOM Structer to 35V@
 4. Page32, Modify JHDD1 to LTCX004LGA0 (S H-CONN CCM
 C127043HR022M27FZR 22P H3.05 HDD)
 Modify JODD1 to LTCX004HZ00 (S H-CONN SANTA 20190X-X 13P
 H3.6 ODD)

1123A-----
 1. Delete +3VALW to +3VALW_PCH MOS Circuit:
 Page12, Delete C589,C414,R77,Q10,C590,C591
 Page34, Delete U28.16 PCH_PWR_EN# off page
 2. Page12, Unpop R210 Pop L3 and C22 for +1.05VS_VTT high ripple
 3. Unpop and Component reduce-----
 Page16, Delete C824,C828,C831,C836,C839 for unpop reduce.
 Page20, Delete C870,C871,C923,C922,C921,C920 for unpop reduce.
 Page27, Change R399,L30,L47 TO R_Short
 Delete C456,C637,C474,C497,C580,C581
 Pop R80 and unpop R396,Q25,C411,R584,Q52
 Page28, Delete C606,C646,C607
 Change R239 to R_short
 Page29, Delete C775,C776,C778,C781,C782
 Page31, Delete C461,C462
 Change R423 to R_short
 Page32, Delete C161
 Change R308 to R_short
 Page34, Change R495 to R_short
 Page36, Chagne L55,L54,L52 to R_short
 4. Page24, SWAP RP41.1,RP41.2
 5. Page27, Change R123,R127 Pull high to +HDMI_5V_OUT
 1122A-----
 1. Page22, Add X7603@ for VRAM 2Gb*4 HYN 128M16
 Add X7604@ for VRAM 2Gb*8 HYN 128M16
 1121A-----
 1. Page06, Add R937 for EC_SCI# Path to GPIO34
 2. Page09, RP28.5 connect to GPIO34
 1120A-----
 1. Page06, Delete chargeable RTC circuit
 Change ODD to SATA port1
 Page32, Modify ODD SATA netname to SATA port 1 .
 2. Page29, +1.2V LAN_OUT add 680P for EMI
 3. Page37, Modify H21 from 2P5 to 3P0
 4. Page38, Add 2 jump for power consumption measure
 J36(+3VS),J37(+5VS)
 5. Delete XDP port and related circuit
 Page04, Delete C63,C64,C96,C97,C98,R20,R21,R22,R23,R27-R31
 Delete R3,R86,R87,R88,R89,R90,R91,R4,C92,C93
 Delete R5,R14,R15,R16,R7,R19,R25,C35,JXDP1
 Page07, Delete R66,R67
 6. ESD DVT Modify:
 Page08, Delete C39
 Page24, Delete D6
 Page28, Delete D7,D18
 Page30, Delete D38
 Page33, Delete D16
 Page35, Delete D25,D30,D34
 Page36, Delete D26,R544,C572
 Page37, Delete ESD TP JUMPS:
 J10,J20,J17,J21,J16,J19,J18
 J22,J24,J28,J25,J29,J23,J27
 J26,J30,J31,J33,J32,J34,J35
 C786 change to EMC@
 Page04, Add C96 to DIMM DRAMRST#
 Page33, C487 change to EMC@ and 0.1uF
 Delete D4
 Page26, C378 change to EMC@
 C387 change to EMC@
 1119A-----
 1. Page06, Add a nochargeable RTC battery.
 2. Page15, Add R191 for DDR_VTT_PG_CTRL pull high +5VS option.
 3. Add page24, Reserve eDP to LVDS translator (RTD2132R)
 Add bom structure TL@ (translate) and EDP@ (eDP mode)
 4. Page25, Add R947 for ENVDD option.
 Add connect TL_INV# PW to INVTPWM
 Add connect RTD2132R TL_HPD to EDP_HPD
 Modify JLVDS1 pin net name fo Co-Lay eDP & LVDS

1107A-----
 1. Page04, Move R25 to JXDP1.60
 Update U1 option component for CPU
 2. Page6,8, Change EC_SMI from GPIO77 to GPIO34
 Delete R445
 3. Page07, Change X2 to X3G024000DC1H(SJ10000CS00)
 4. Page08, U17, U43, R310 change to @
 Mount R65
 R310.1 change to +3VS
 5. Change all 932@ to 940@
 R161, D29, R564, U6, R569, C522, C523, C552, D36, Q39, R522,R586, R589, R607,
 R610, R624, R693, U41, U44, C516, C518, D28, R146, R158, R159, R160, R496, R499,
 R504, R507, R508, R511, R601, U28, U29
 6. Page11, R169 change to XDP@
 7. Page12, add C414 and change PCH_PWR_EN to PCH_PWR_EN#
 delete Q33, R561, R563
 8. Page16, delete R58, R298, R300, C163, R299, R302
 9. Page17, Add option component (U51) for SUN_XT
 10. Page19, Add R900, R901 with BOM structure @
 11. Page24, delete R405, U20, R362, R401, C164
 Change U8 to G5243AT11U(SA000028Y10)
 12. Page25, delete R367, D7, F1, D8, D19
 13. Page26, change L47, L48 to BLM18AG121SN1D(SM010030010)
 14. Page27, Delete D31, F2, C450
 15. Page28, Delete R781, D23, R782, R785, U49, C803
 16. Page29, Delete R792
 change T1 to GST5009-E (SP050006B10)
 delete R414, C166
 R438, Q20 change to @
 Change U9 to G5243AT11U(SA000028Y10) with BOM@
 18. Page31, delete R595, R597, Q34, R597, R596, R562
 19. Page32, Change U25 to SY6288D10CAC MSOP8(SA00004KB10)
 Change JUSB1 to OCTEK USB-09EAA(BDC233008020)
 Delete R472, R469, R460, R462, C635, U46, R459, R463, R464
 Mount R503
 Change R506 to 8.2K
 Change R509 to R_Short with BOM @
 Delete R491, R493, D20
 21. Page34, add R535 (100K_0402)
 Mount R632
 21. Page35, L51 change to BLM18AG121SN1D(SM010030010)
 Change JMIC1 to ACES_88266-02001(SP020008Y00)
 Delete R143, R668, R162, R181, C719, R671
 23. Page37, delete R424, C169
 Change U12 to G5243AT11U(SA000028Y10)
 24. Page43, SW1 change BOM Structure to @
 1015A-----
 1. Modify BOM Structure/Function Field for EMC@(45.1)
 Page06, RP14
 Page07, RP19, R390
 Page24, L11
 Page25, R368, R369, R370, R371, R372, R373, R374, R375
 Page27, L42, L45, L46,R175, R180
 Page28, R774
 Page29, R897, C814, D39
 Page32, L24, L25, R458, R461
 Page35, R527, R528, R532, R533, L36, L38, D1, C62
 2. Modify BOM Structure/Function Field for XEMC@(45.1)
 Page04, C63, C64, C96, C97, C98, C94, C95, C60, C92, C93, C35
 Page07, R104, C152, R402, C453
 Page08, C39
 Page24, C528, C549, C364, C365, D6
 Page25, D2, L13, L14, L15, L16
 Page28, C792, C786
 Page29, R26, C26, C806, C807, C808, C809, JP1, JP2, D38
 Page31, C408, C398
 Page32, D15, D16, D4, C487, R453,R455, R456, R457, L26
 Page33, R477, C501, R513, C520, C506, C507, C511
 Page34, C551, C553, D25, D30, D34
 Page35, R548, C573, R671, C719, C556, C550, C444, C445, D27, D37, D26, R544, C572
 Page36, C630
 3. Modify Function Field to 45.1 only (BOM Structure is same as before)
 Page04, R27, R28, R29, R30, R31
 Page07, RP20
 Page33, R160
 Page35, R143, L51
 4. Display BOM structure and Value of U1 (CPU)
 5. Display BOM structure of R0402_OOHH-NEW and R0603_OOHH-NEW (R Short Pad show BOM Structure @)
 6. Page08, Update note of GPIO66

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B1 --> B2 Change List

0114-----
 1. Page03, Add U1 with QDJA@
 2. Page30, R897 change to SM01000LU00
 3. Page24, L63,L73 change to SM01000EJ00
 4. Page25, L11 change to SM01000EJ00
 5. Page36, L33 change to SM01000EJ00
 6. Page31, U9, C165 with IOAC@
 0110-----
 1. Page32, Delete R312,R313,R314,R315
 Add C392,C393,C391,C394 with EA50@
 2. Page27, Add C35
 3. Page38, Delete Q45,R570,R571
 0108-----
 1. Page33, R458, R461 change to R0402_0OHM-NEW
 Add JFP1
 2. Page26, Delete L13, L14, L15, L16
 3. Page29, Delete C792, C99
 4. Page31, Delete J4
 5. Page10,25 change Touch screen port from USB port 5 to port6.
 6. Page25,34 change net name of TS_INT to TS_EN
 7. Page10 add USB port 5 for Finger Print
 8. Page38, Add C19
 9. Page26, Add C396, C398
 10. Page36, Mount C554
 11. Page38, Mount C979
 12. Page35, Reserved SW6,SW7,SW8,SW9
 13. Page32, Add C534, C535, C536, C537 for JHDD2 with BA51@
 change C391,C392,C393,C394 to R312,R313,R314,R315
 Update Power schematics
 0107-----
 1. Page06, R937 change to R0402_0OHM-NEW
 R75 change to R0603_0OHM-NEW
 2. Page07, R108 change to 15_0402_5% with 1ROM@
 RP19 change to 15_0804_8P4R_5% with 1ROM@
 Add R105, R106 with 1ROM@ for PCH_SPI_I02_1, PCH_SPI_I03_1
 Change R102, R103, R109, U7, C67, PR20 to 2ROM@
 3. Page08, R62, R65 change to 0402_0OHM-NEW
 4. Page10, Change Touch Screen USB port frum Port3 to Port5.
 R155 change to R0603_0OHM-NEW
 Change Q53 to @
 5. Page24, R947,R363,R949 change to R0402_0OHM-NEW
 Add C376,C377,C388,C389 with TL@
 Add R414, R426
 Add R424, R425 with @
 7. Page27, R80 change to R0603_0OHM-NEW
 L48 change to R0603_0OHM-NEW
 8. Page29, C99 change to XEMC@
 R774 change to 56_0402_5%
 9. Page32, R49, R593 change to R0805_0OHM-NEW
 9. Page34, R236 change to R0805_0OHM-NEW
 10. Page38, R926 change to R0402_0OHM-NEW
 0103-----
 1. Page35, R698,R701 change to 680 ohm
 R702 change to 499 ohm
 2. Page18, Un-mount C847
 3. Page38, Add U38, R77, C63
 Update Power Schematics
 1228-----
 1. Page25, Add USB20_P3/N3 on JLVDS1.35/36
 Add R81
 2. Page35, Delete JTP1, R609, R610, C552, R693, R607, R608, D36
 3. Page34, change Q50 to L2N7002LT1G SOT23-3
 change R506 to 18K_0402_5%

B2 --> C Change List

0306-----
 1. Page27, Mount R410, R411
 Change R240, R241 with @
 Change R418 to 4.7K
 0304-----
 1. Page20, Mount C872, C873, C874, C889, C917, C918, C919
 2. Page25, change C371,C372, C369, C370 with EDP@
 3. Page33, Change L24, L25 to SM070001E00
 0301-----
 1. Page08, change R62,R65 to 0 ohm
 2. Page12, Add C408
 3. Page34, Add D25
 Reserved D26
 0227-----
 1. Page29, Del R766
 2. Page32, change JDB1 to E-T_1001K-F50C-05R_50P-S
 0226B-----
 Modify for ESD
 1. Page11, Mount C13,C14 (10U_0603)
 1. Page12, Change C40 to 10U_0603
 Mount C31 (1U_0402)
 3. Page15, Mount C117 (10U_0603)
 Add C161 10U_0603
 4. Page33, Mount C483 with 0.1U
 Reserved D3 with XEMC@
 5. Page38, Add C39, C64,C92,C93 22U_0805
 Update power schematics
 0226-----
 1. Page12, Del T99
 2. Page27, Mount R204,R241, R407,R408
 Change R412,R413 with @
 3. Page28, Add R312 with @
 4. Page34, Del R590 (Add offpage for H_PROCHOT#_EC)
 Del R505
 Update Power Schematics
 0221-----
 1. Page18, R898, R899 change to R0402_0OHM-NEW
 2. Page25, Add TS@ for R81, R414, R426
 0219-----
 1. Page08,34,37 G_SEN_INT connecto to PCH_GPI080
 Change U2.4, U2.6 to D_CK_SCLK/D_CK_SDATA
 2. Page29, Reserved C815
 3. Page22, Add C1024, C1025, C1026, C1023, C1027, C1028, C1029, C1030 with 128@
 4. Page23, Add C1031, C1032, C1033, C1034, C1038, C1036, C1037, C1035 with VGA@
 5. Page38, Reserved R556, R574, Q55, R557, R575, Q41, R570, R571, Q45
 0218-----
 1. Page06, Update Y1 CIS Symbol
 Add D23, C151
 Change R446, D32, C168 to @
 2. Page18, Change C823, C827, U52, R798 with @
 2. Page29, Add R781, C792
 3. Page30, Add R782 and Mount C822
 2. Page34, Change R506 to 33K

C --> Pre-MP Change List

0411-----
 1. Change U51 FN to R3 (SA00006G610, SA000061J20)
 2. Page06, unmount R446, C168, D32
 Mount D23, C151
 0329-----
 1. Page04, Add SR160@ and SR170@ for U1
 2. Page06, Change C151, D23 with @
 Mount R446, D32, C168
 0326-----
 1. Page1, Change PCB FN to DA60000XL10
 2. Page29, Mount C815
 Update Power Schematics
 0321-----
 1. Page8, G_SEN_INT change from GPIO80 to GPIO52.
 2. Page34, Change R506 to 100K_0402_5%

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