

# Compal Confidential

## Q5WV8 Schematics Document

### AMD "Comal" Platform

### AMD Trinity APU / Hudson M3 FCH / ATI Thames XT

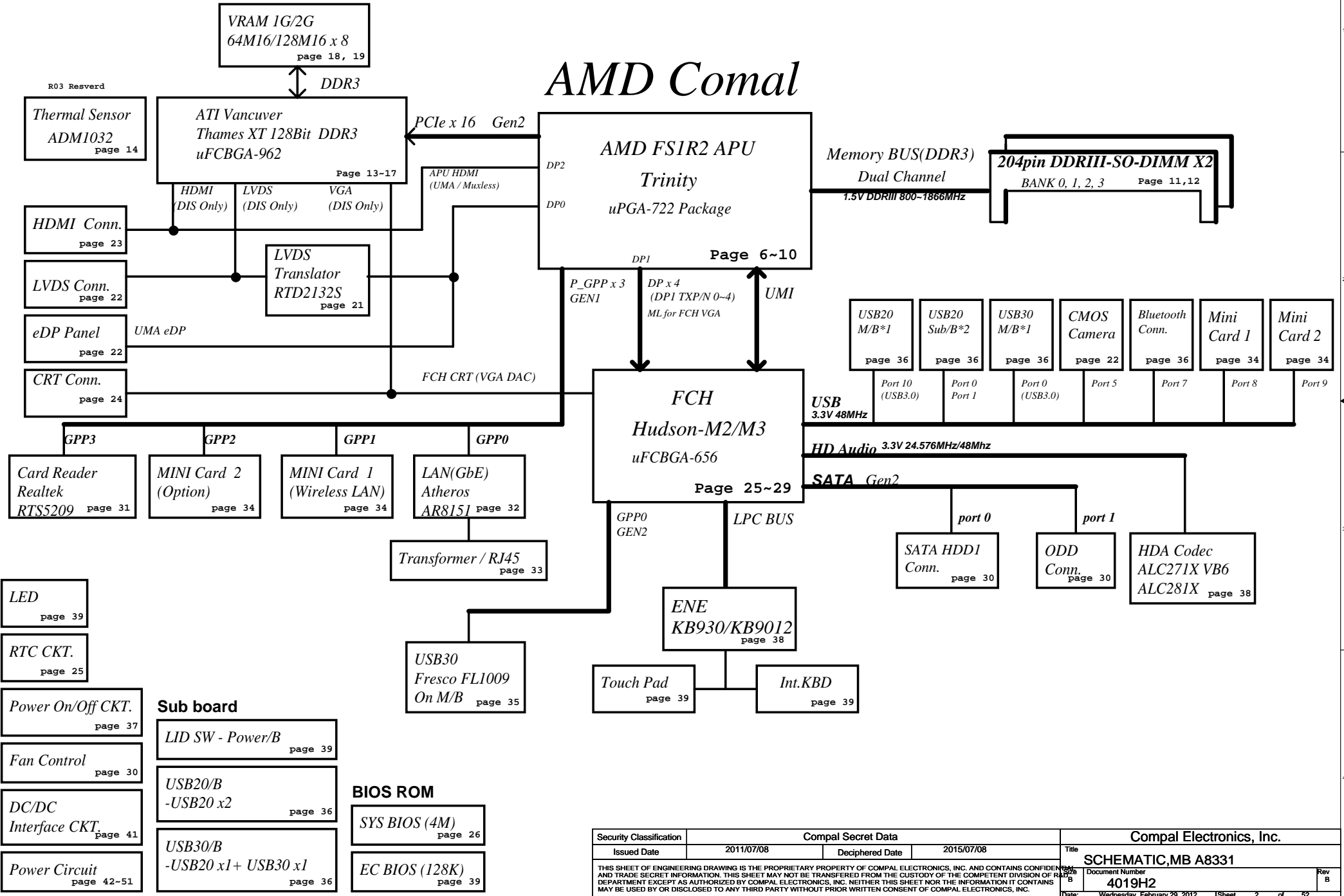
2012-01-05A

LA-8331P REV: 0.4

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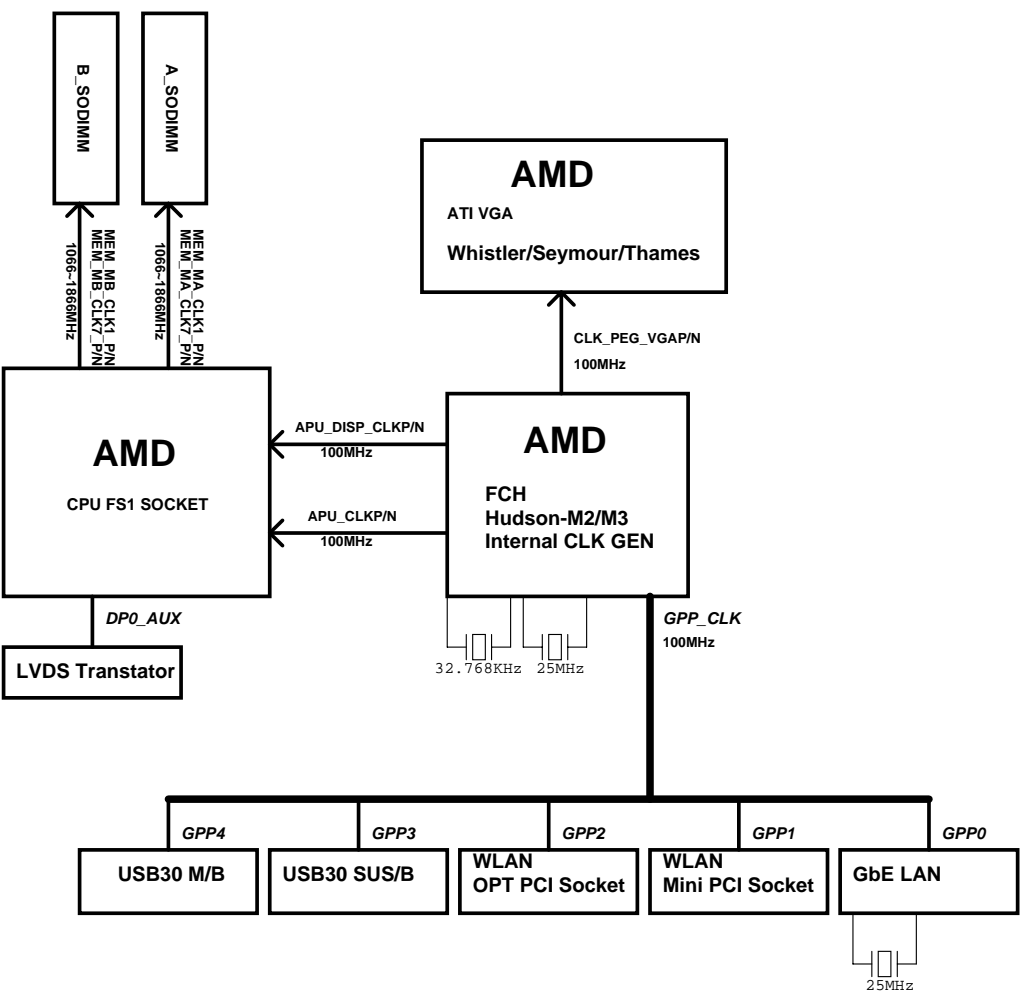
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Model Name : Q5WV8

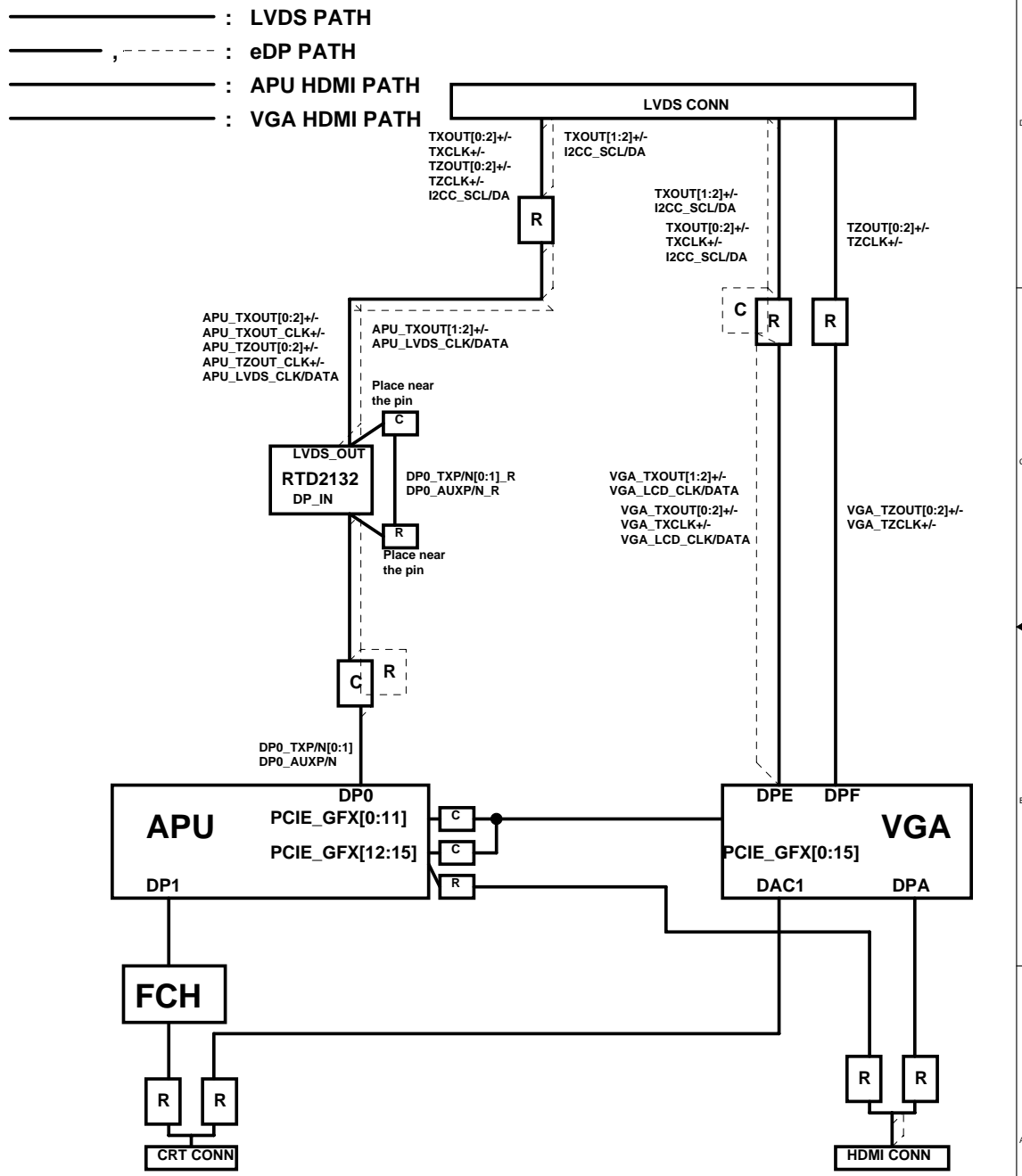


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# CLOCK DISTRIBUTION



# DISPLAY DISTRIBUTION



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# Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices			
Device	IDSEL#	REQ#/GNT#	Interrupts

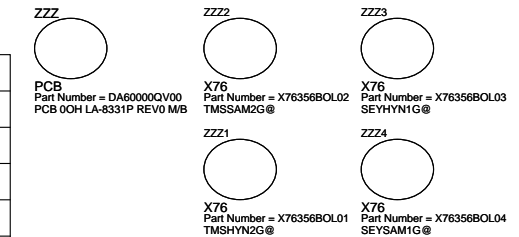
EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (VGA)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR (RTD-2132S)	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address			FCH SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	90			
DDR DIMM2	1101 001X b	94			

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	1.8K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V



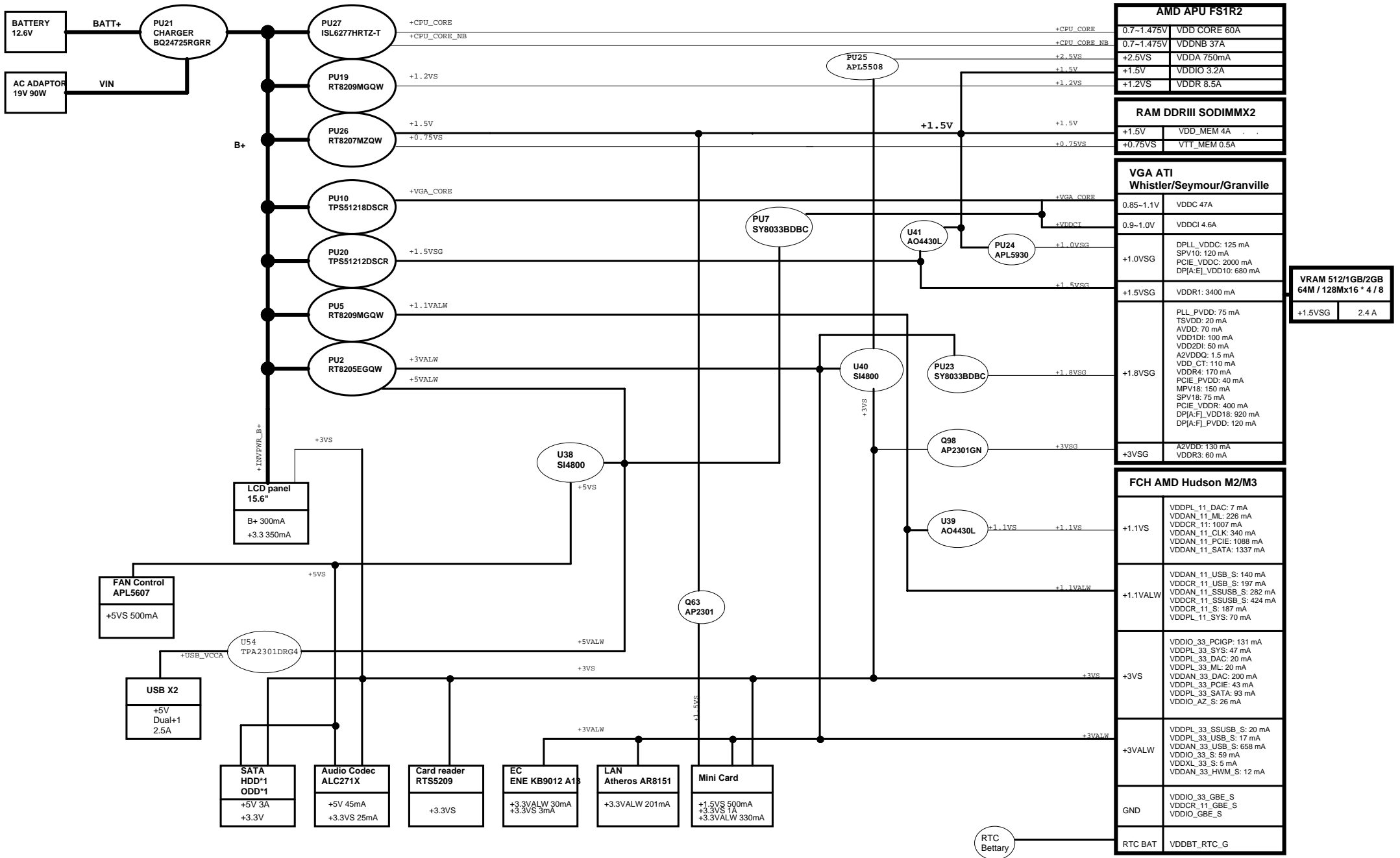
## BOARD ID Table

Board ID	PCB Revision
0	EVT
1	EVT2
2	DVT
3	
4	
5	
6	
7	

## BOM Option Table

BOM Structure	Description	UMA	Thames	EVT2 UMA	DVT UMA-LVDS	DVT UMA-eDP	DVT PX5 1G-LVDS	DVT PX5 1G-eDP	DVT PX5 2G-LVDS
M2@	Use Hudson-M2			V					
M3@	Use Hudson-M3	V	V		V	V	V	V	V
930@	Use EC 930	V	V						
9012@	Use EC 9012			V	V	V	V	V	V
UMA@	Display output from APU (UMA only or PX)	V	V	V	V	V	V	V	V
DISO@	Display output from VGA (DIS only)								
VGALVDS@	VGA output LVDS (DIS only)								
VGA@	Use VGA (PX or DIS only)		V				V	V	V
THA@	VGA: Thames		V				V	V	V
SEY@	VGA: Seymour								
128@	Use VRAM channel A&B		V				V	V	V
PX@	PX function		V				V	V	V
BACO@	BACO function (PX4.0)		V						
NOBACO@	Without BACO function (DISO and PX5.0)						V	V	V
TL@	LVDS Translator (for LVDS)	V	V	V	V		V		V
EDP@	Use eDP Panel					V		V	
APUEDP@	APU output eDP					V		V	
VGAEDP@	VGA output eDP (DIS only)								
271@	Realtek ALC271x VB6	V	V	V	V	V	V	V	V
281@	Realtek ALC281x								
ZERO@	ZERO Power ODD function								
FL@	Fresco FL1009 USB3.0 Controller			V					
8151@	LAN Atheros AR8151 10/100/1000M LAN			V	V	V	V	V	V
8152@	LAN Atheros AR8152 10/100M LAN								
X76@	VRAM ID Table (Load By X76J)								
CONN@	Connector (Control by ME)								

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AMD APU FS1R2	
0.7-1.475V	VDD CORE 60A
0.7-1.475V	VDDNB 37A
+2.5VS	VDDA 750mA
+1.5V	VDDIO 3.2A
+1.2VS	VDDR 8.5A

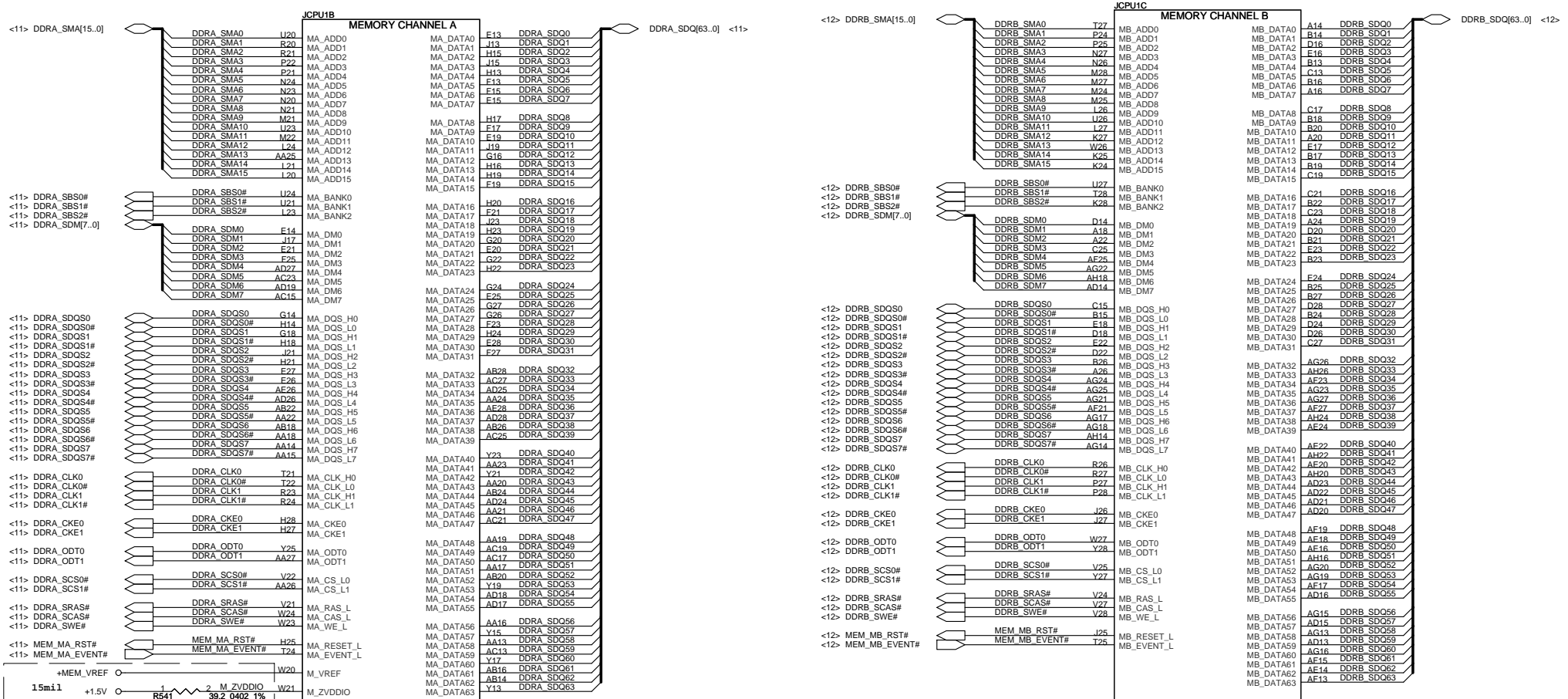
RAM DDRIII SODIMM X2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A

VGA ATI Whistler/Seymour/Granville	
0.85-1.1V	VDDC 47A
0.9-1.0V	VDDCI 4.6A
+1.0VSG	DPLL_VDDC: 125 mA SPV10: 120 mA PCI_E_VDDC: 2000 mA DP[A,E]_VDD10: 680 mA
+1.5VSG	VDDR1: 3400 mA
+1.8VSG	PLL_PVDD: 75 mA TSVDD: 20 mA AVDD: 70 mA VDD1DI: 100 mA VDD2DI: 50 mA A2VDDQ: 1.5 mA VDD_CT: 110 mA VDDR4: 170 mA PCI_E_PVDD: 40 mA MPV18: 150 mA SPV18: 75 mA PCI_E_VDDR: 400 mA DP[A,F]_VDD18: 320 mA DP[A,F]_PVDD: 120 mA
+3VSG	A2VDB: 130 mA VDDR3: 60 mA

VRAM 512/1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A

FCH AMD Hudson M2/M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 197 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA
+3VS	VDDIO_33_PCIGP: 131 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 20 mA VDDAN_33_DAC: 200 mA VDDPL_33_PCIE: 43 mA VDDPL_33_SATA: 93 mA VDDIO_AZ_S: 26 mA
+3VALW	VDDPL_33_SSUSB_S: 20 mA VDDPL_33_USB_S: 17 mA VDDAN_33_USB_S: 658 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G

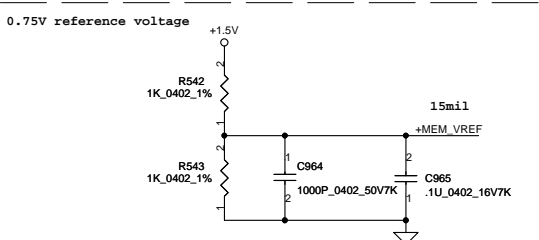
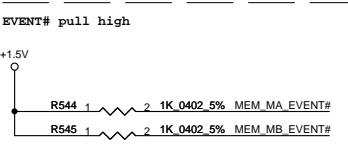




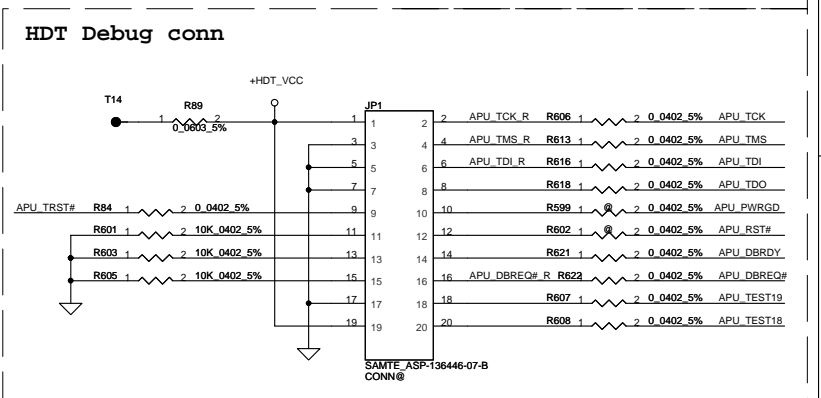
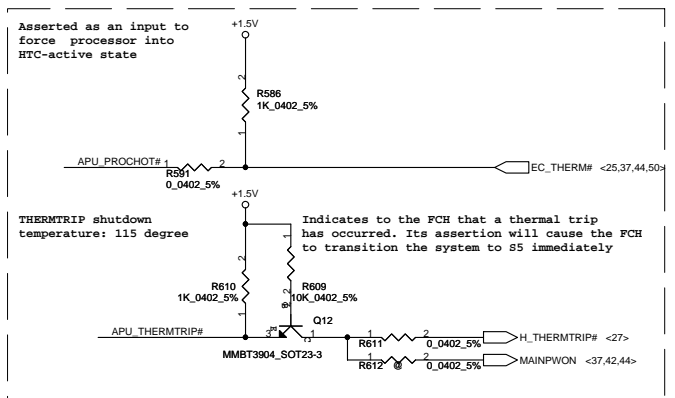
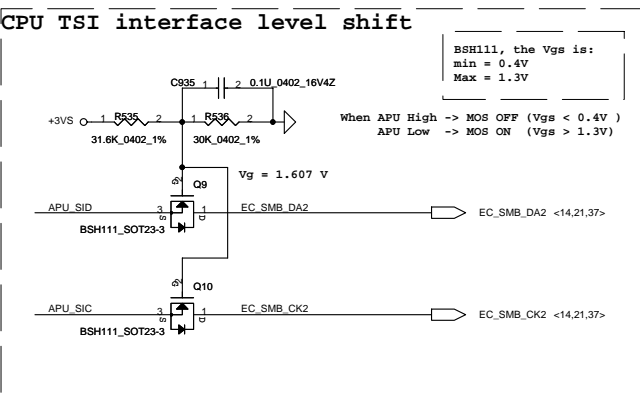
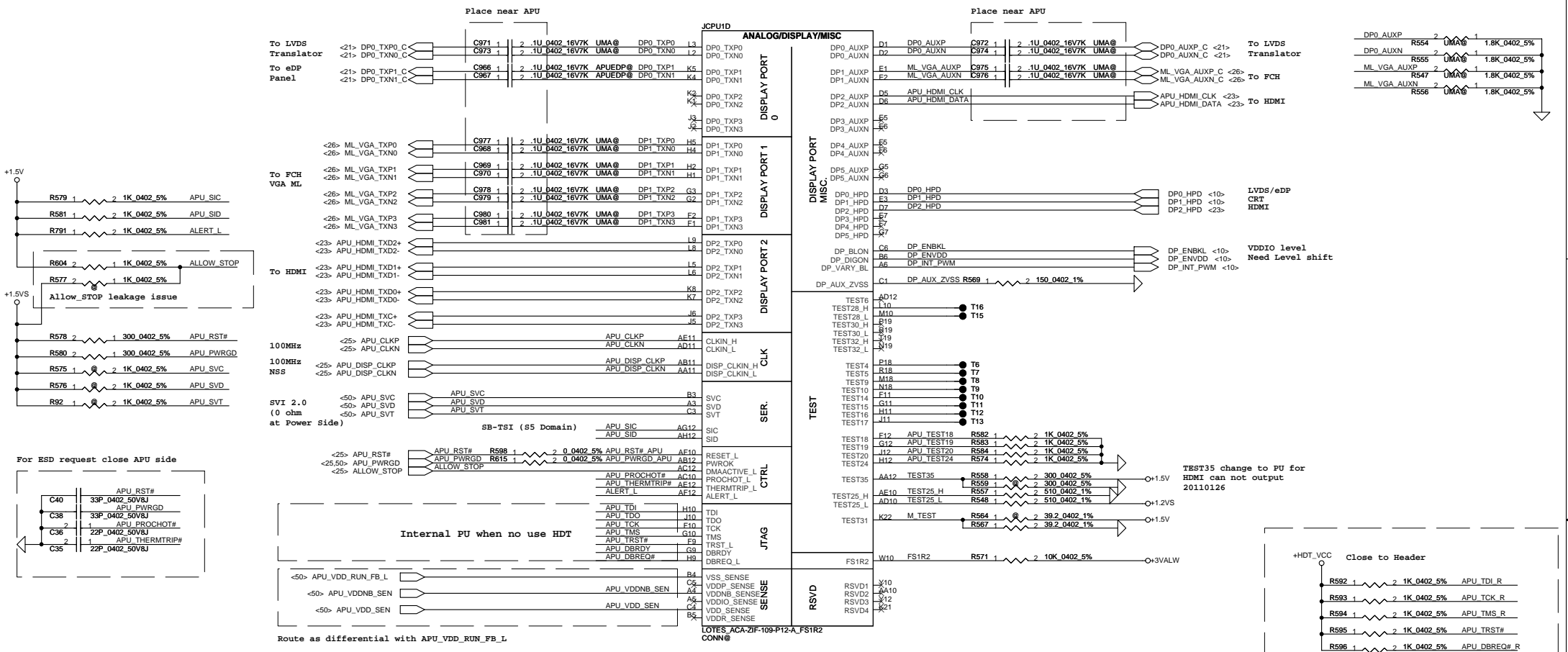
Place them close to APU within 1"

LOTES\_ACA-ZIF-109-P12-A\_FS1R2 CONN@

LOTES\_ACA-ZIF-109-P12-A\_FS1R2 CONN@



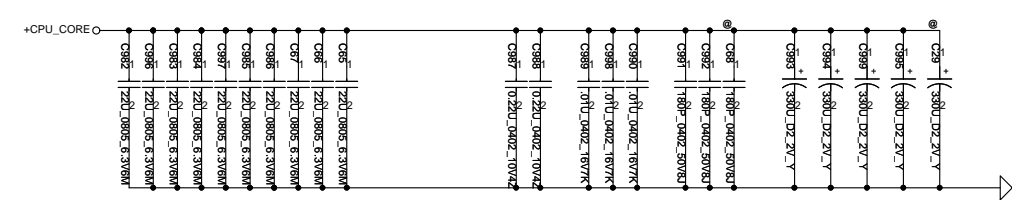
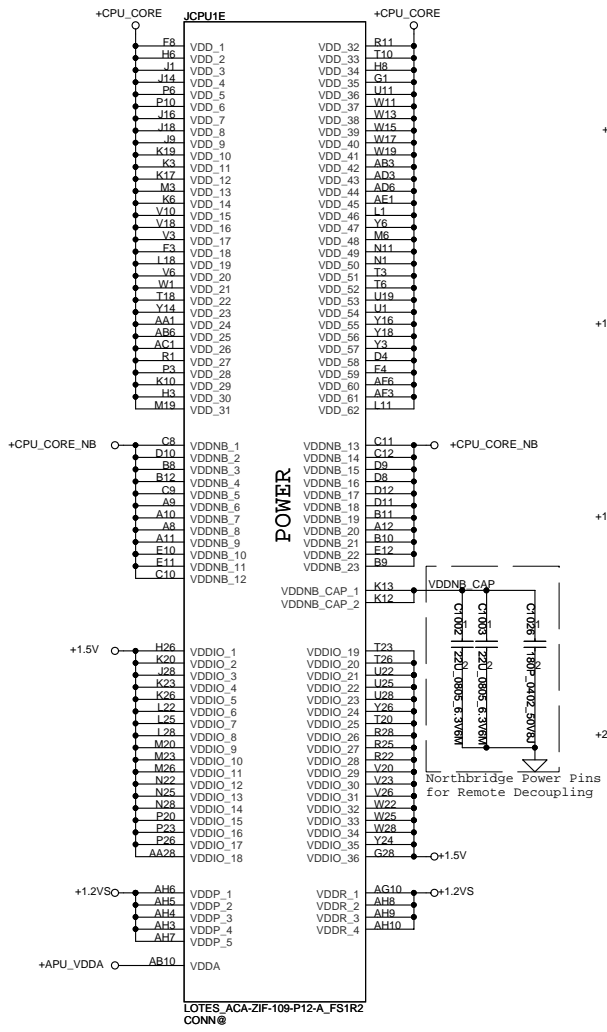
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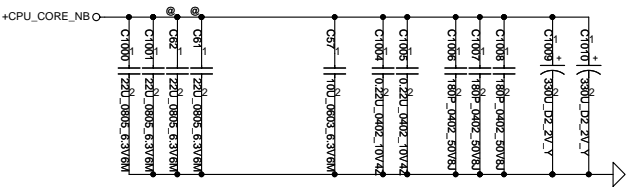
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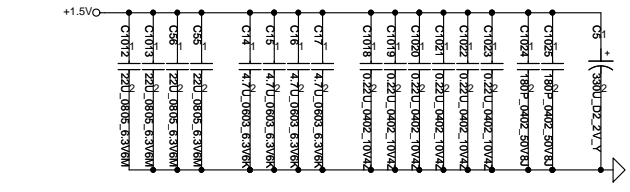
Power Name	Consumption
VDD +CPU_CORE	<b>60A</b>
VDDNB +CPU_CORE_NB	<b>37A</b>
VDDIO +1.5V	<b>3.2A</b>
VDDP / VDDR +1.2VS	<b>5A / 3.5A</b>
VDDA +2.5VS	<b>0.75A</b>



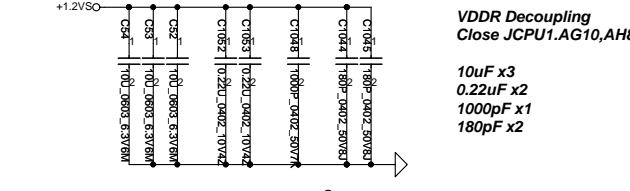
**+CPU\_CORE Decoupling**  
 330uF x 3 @ x2  
 22uF x 10 @ x5  
 0.22uF x 2  
 0.01uF x 3  
 180pF x 2 @ x1



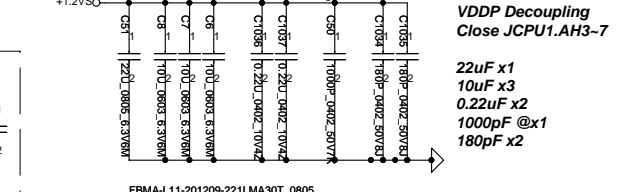
**+CPU\_CORE\_NB Decoupling**  
 330uF x 2  
 22uF x 2 @ x5  
 10uF x 1  
 0.22uF x 2  
 180pF x 3



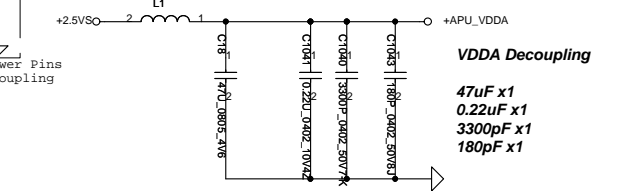
**+1.5V / VDDIO Decoupling**  
 330uF x 1  
 22uF x 4  
 4.7uF x 4  
 0.22uF x 6  
 180pF x 1 @ x1



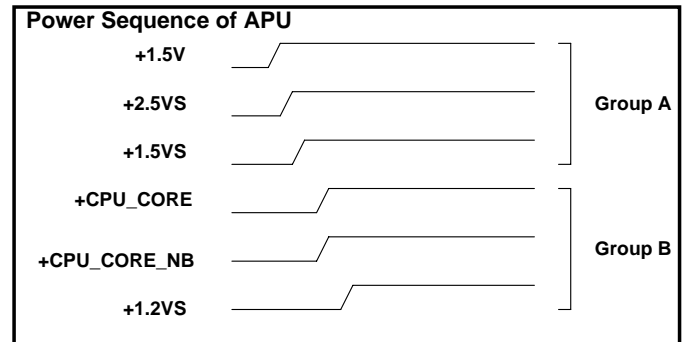
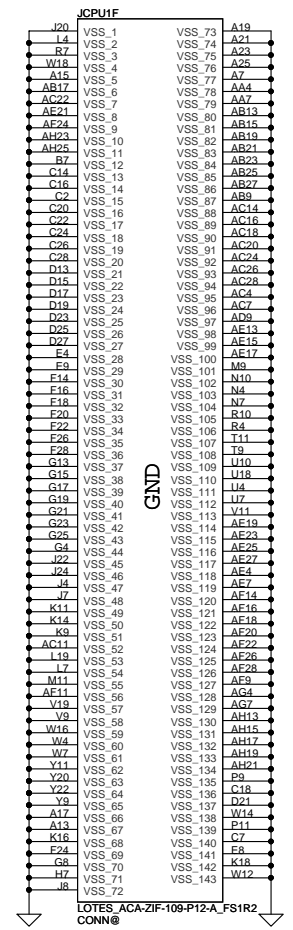
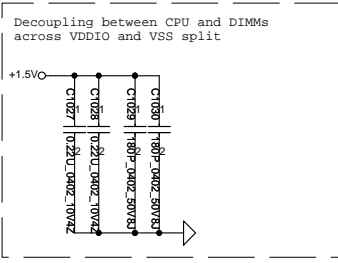
**VDDR Decoupling**  
 Close JCPU1.AG10,AH8,AH9,AH10  
 10uF x 3  
 0.22uF x 2  
 1000pF x 1  
 180pF x 2



**VDDP Decoupling**  
 Close JCPU1.AH3-7  
 22uF x 1  
 10uF x 3  
 0.22uF x 2  
 1000pF @ x1  
 180pF x 2



**VDDA Decoupling**  
 47uF x 1  
 0.22uF x 1  
 3300pF x 1  
 180pF x 1

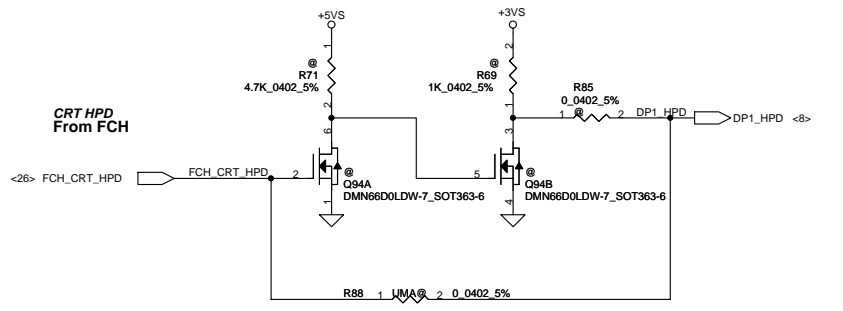
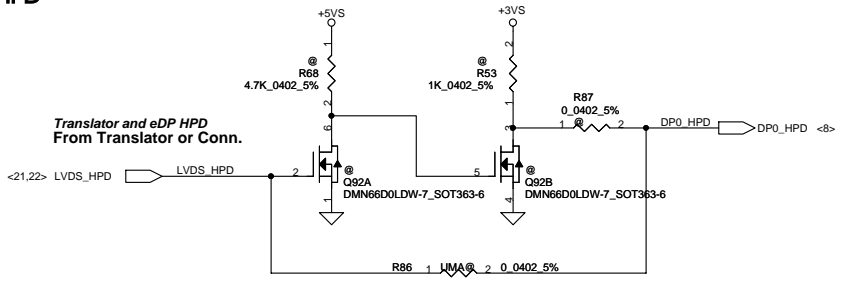


**Decoupling Caps.**

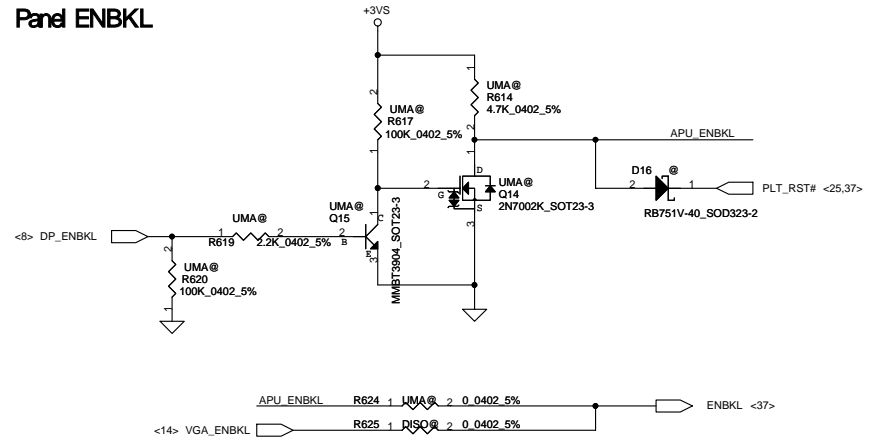
Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0		0	19/11	7	5	17	3	1	1 / 1	13/3	
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

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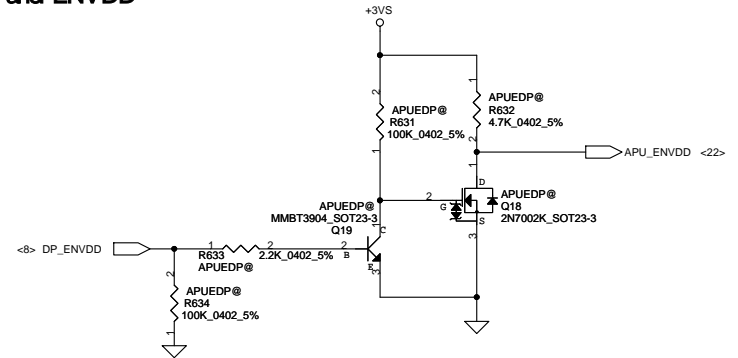
HPD



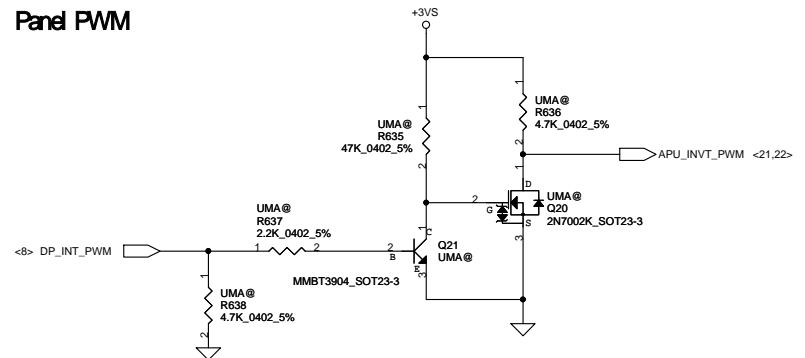
Panel ENBKL



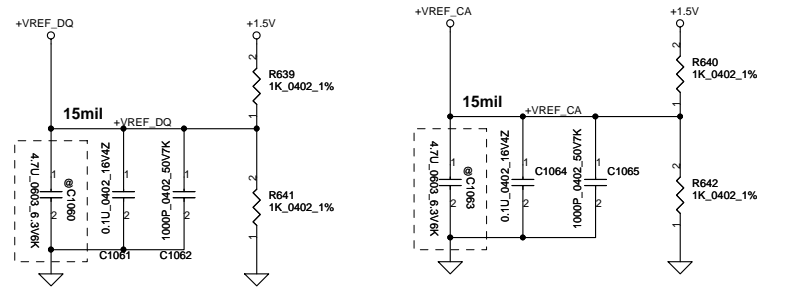
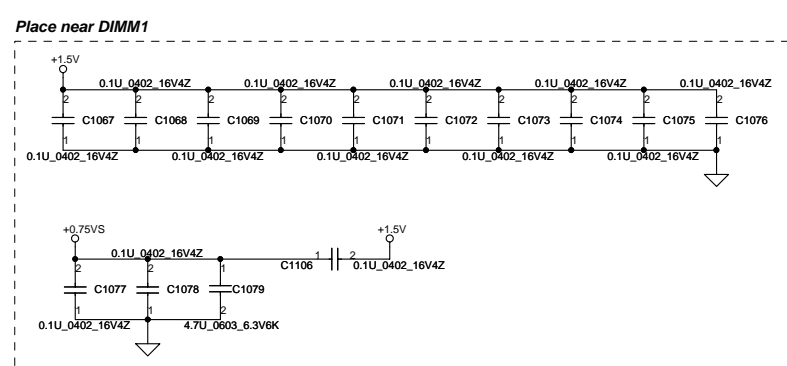
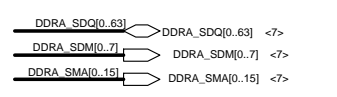
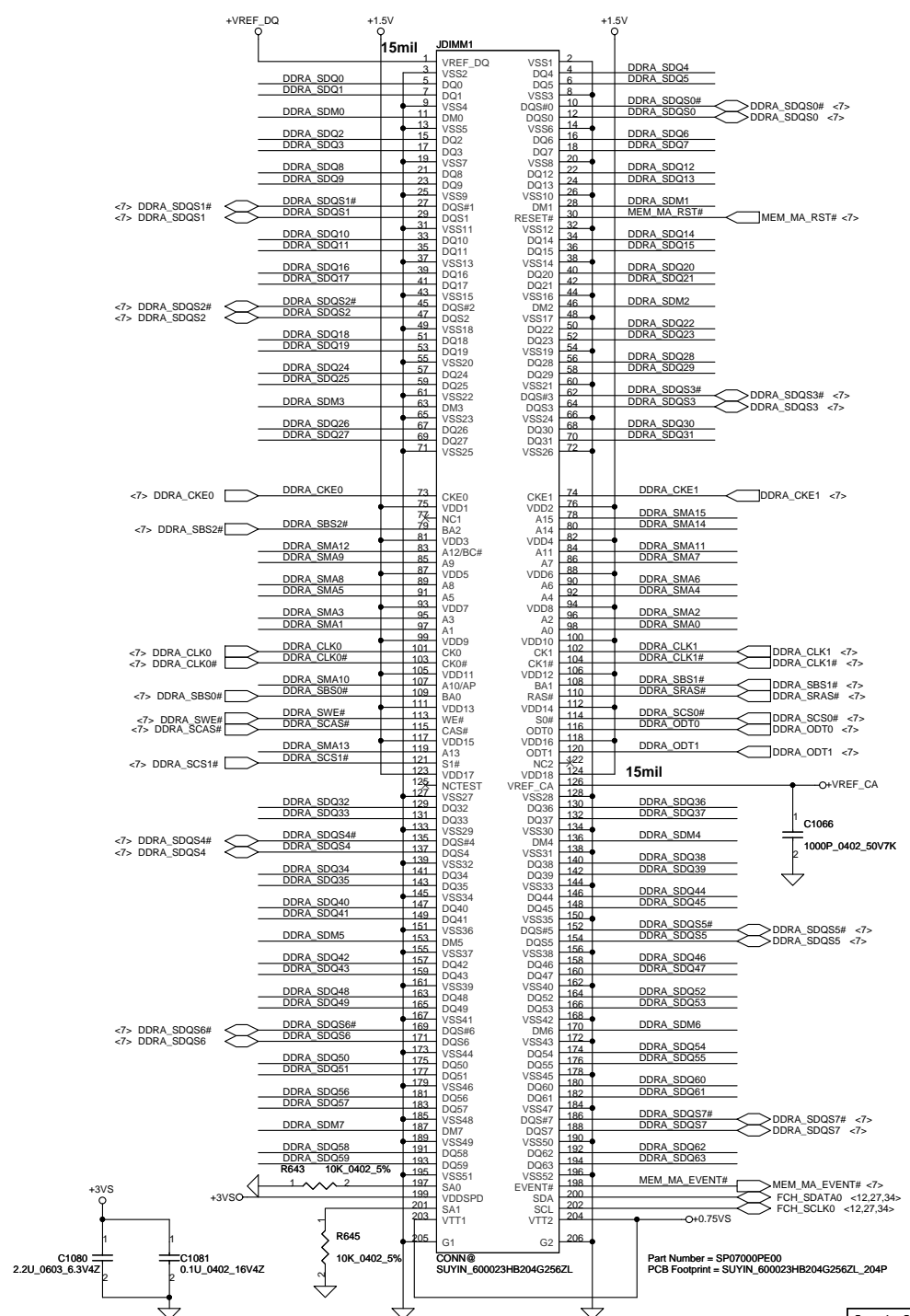
Panel ENVDD



Panel PWM



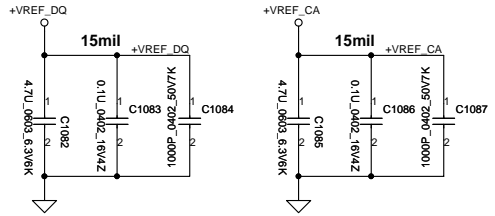
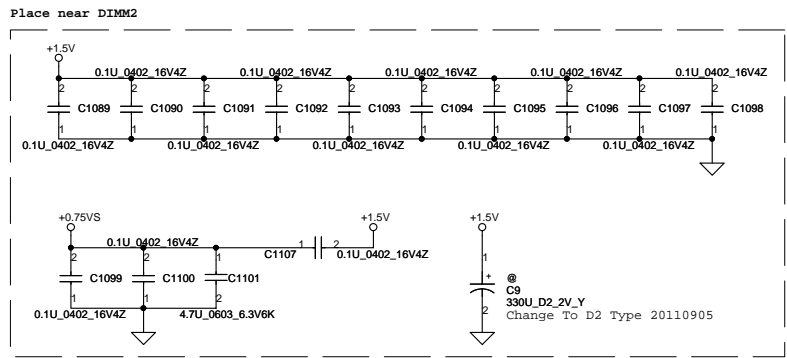
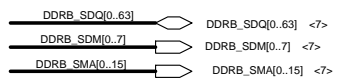
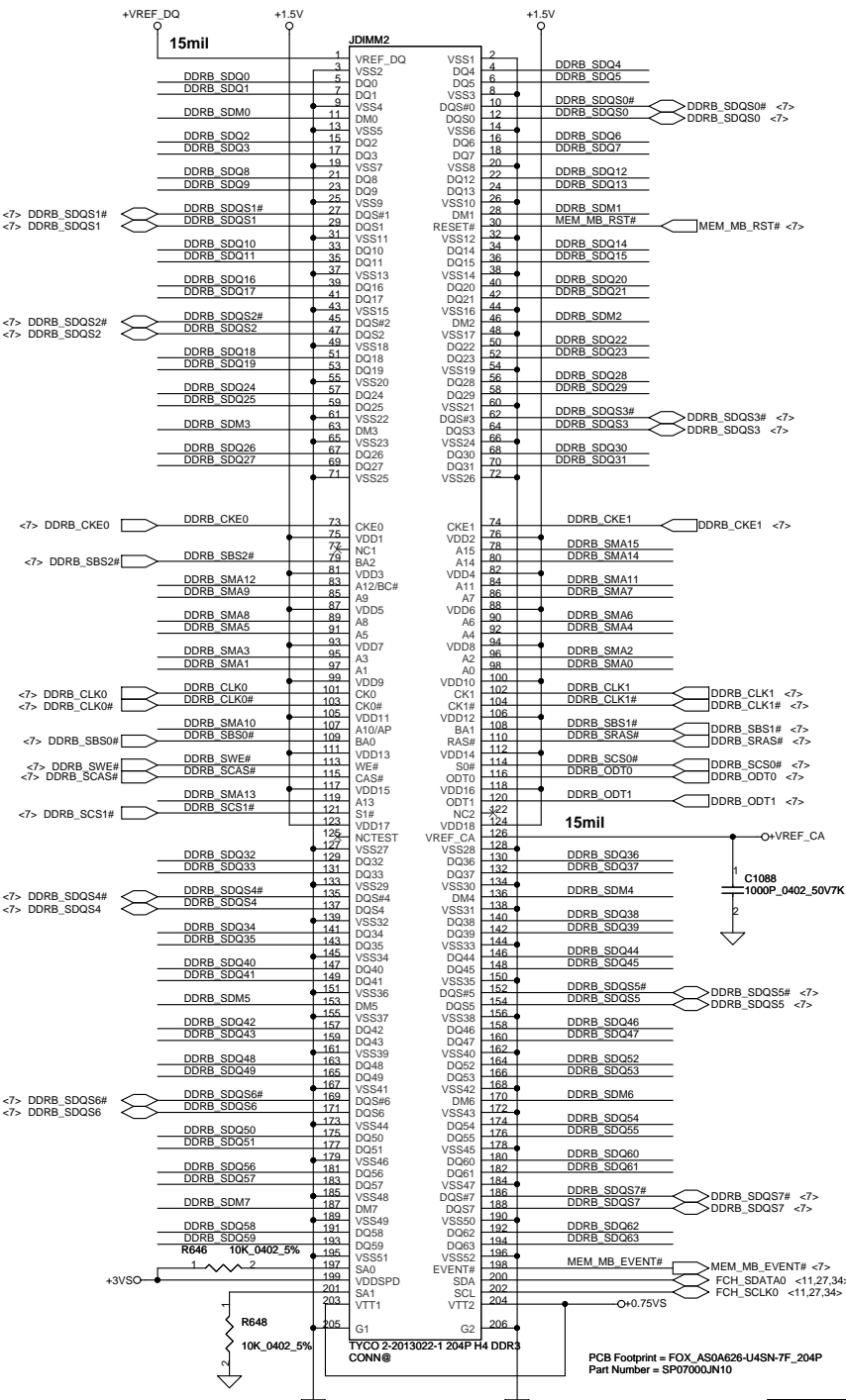
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Date: Wednesday, February 28, 2012			Sheet 10 of 52	Document Number 4019H2



**DIMM\_A STD H:8mm**  
 <Address: 00>

Part Number = SP07000PE00  
 PCB Footprint = SUYIN\_600023HB204G256ZL\_204P

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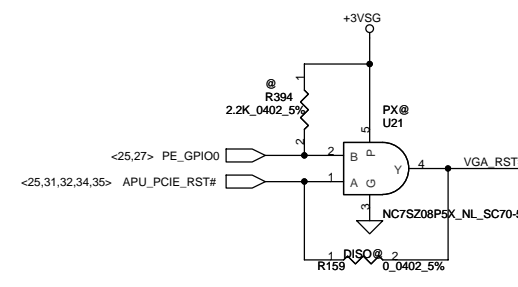
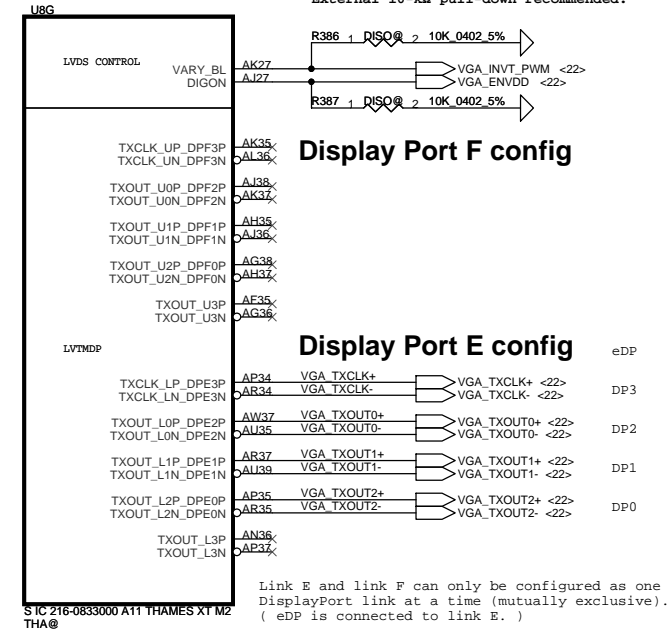
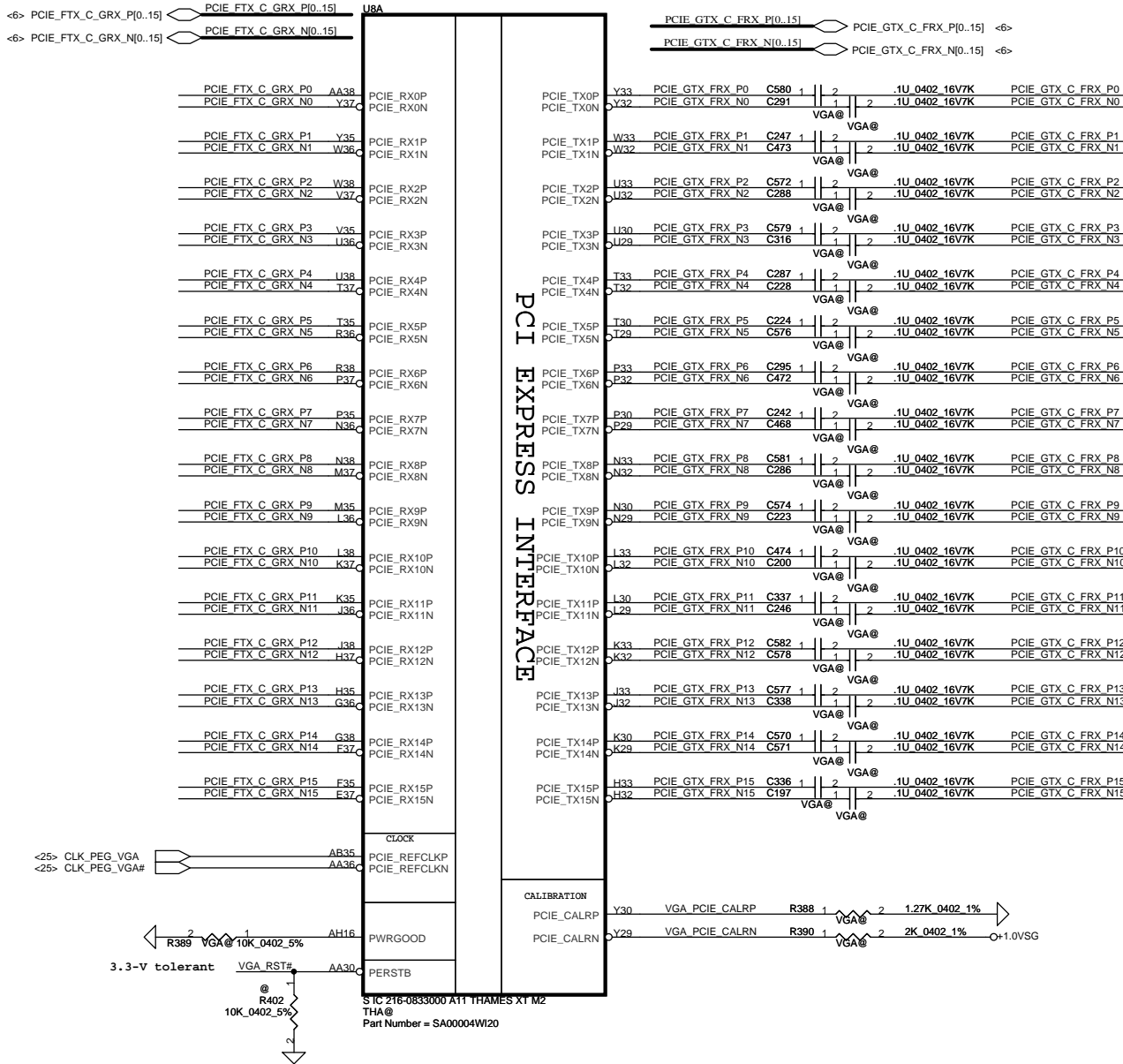
**DIMM\_B STD H:4mm**  
 <Address: 01>

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# GFX PCI E LANE REVERSAL

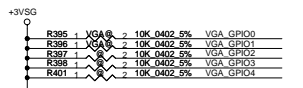
<DIGON>  
Controls panel digital power on/off.  
Active High  
External 10-kΩ pull-down recommended.

<VARY\_BL>  
LCD PWM (pulse width modulated)  
output to adjust LCD brightness  
Active High  
External 10-kΩ pull-down recommended.



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Strap Name	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (ENCLK_V2SYNC) VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	(Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines CONFIG[3:0] 128 MB 000 the ROM type.	001
CONFIG[1]	GPIO12	
CONFIG[0]	GPIO11	
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device (Internal PD) 0: Diabte, 1: Enable	0
AUD[1]	HSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected;	11
AUD[0]	VSYNC 11: Audio for both DisplayPort and HDMI	
BIF_GEN2_EN	GPIO2 0: Advertises the PCIe device as 5.0 GT/s capable at power-on 1: Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	HSYNC GENCLK GPIO8 GPIO21 Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

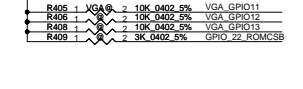


**Global Swap Lock on Multiple GPUs**

GPIO5 fast-power reduction:  
HW control will cause display disturb  
should use SW method control

GPIO6 voltage control signal, No use can NC

Move to DDCCCLK\_AUX3P,DDCDATA\_AUX3N



**VRAM ID**

GPIO Controls backlight on/off.  
Active High, need external PD  
If GPIO22 High, GPIO 11-13 <CFG[0:2]>  
Config ROM type, GPU has internal PD

GPIO6,15,16,20  
Voltage control signal  
GPIO6,15 no use can NC  
Thermal monitor interrupt

Critical temperature fault

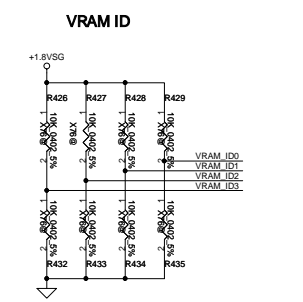
Reserved

External BIOS device  
ON(1)OFF(0) inter PD

Internal Debug  
no use can floating  
ON(1)OFF(0)

Stereo Sync  
no use can NC

For ATI Cross fire  
no use can NC



**VREF**

VREFFG: Use a voltage divider to set VREFFG = 1.80 V / 3  
(or 0.60-V nominal).

+1.8VSG

+3VSG

VGA@ L10

VGA@ L11

VGA@ L12

VGA@ L13

VGA@ L14

VGA@ L15

VGA@ L16

VGA@ L17

VGA@ L18

VGA@ L19

VGA@ L20

VGA@ L21

VGA@ L22

VGA@ L23

VGA@ L24

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VGA@ L92

VGA@ L93

VGA@ L94

VGA@ L95

VGA@ L96

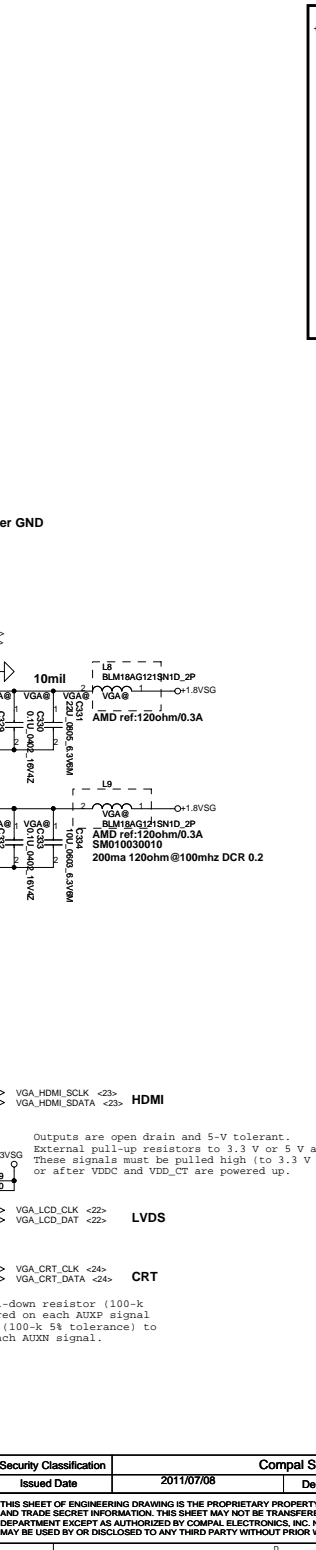
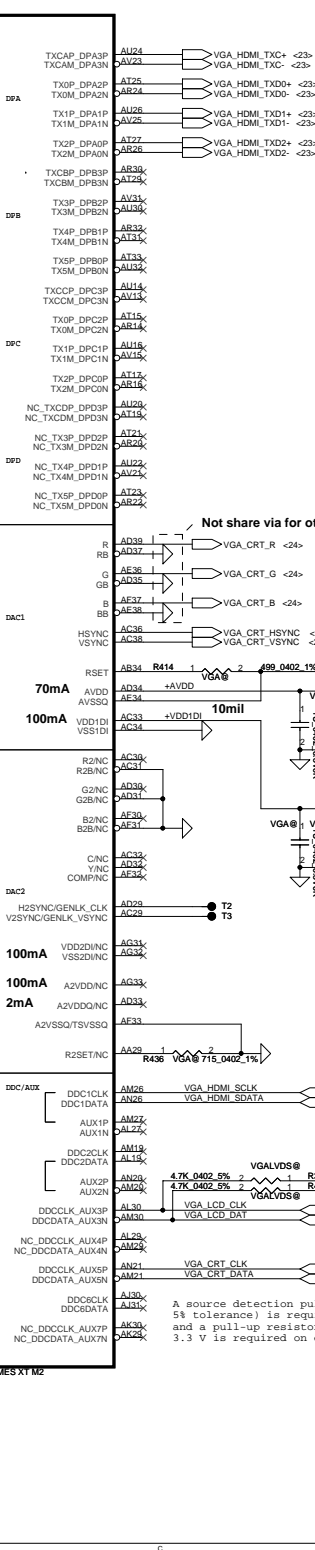
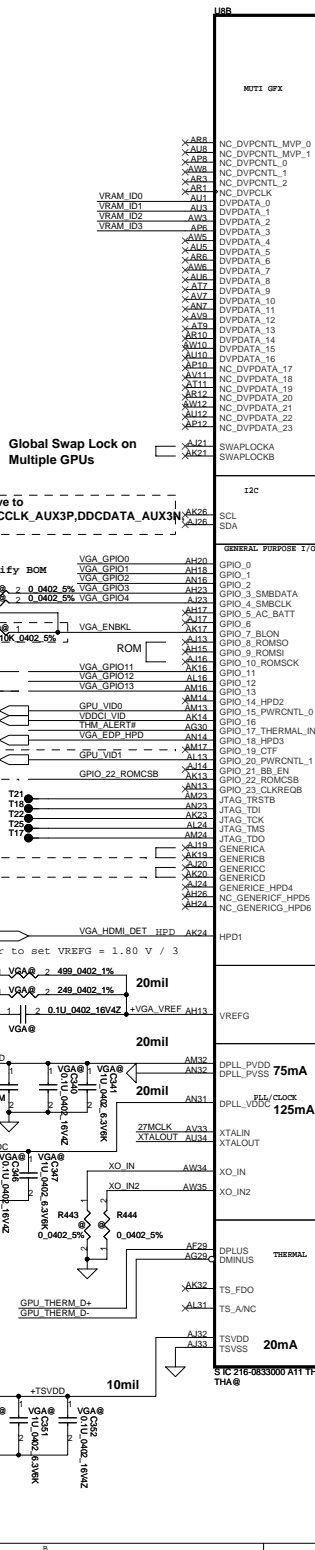
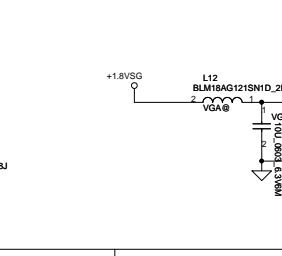
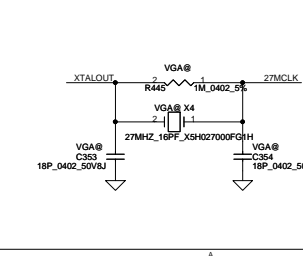
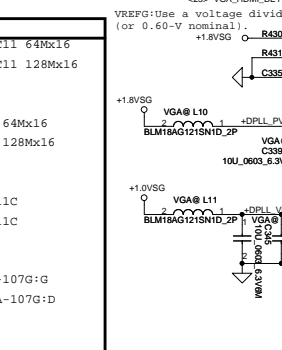
VGA@ L97

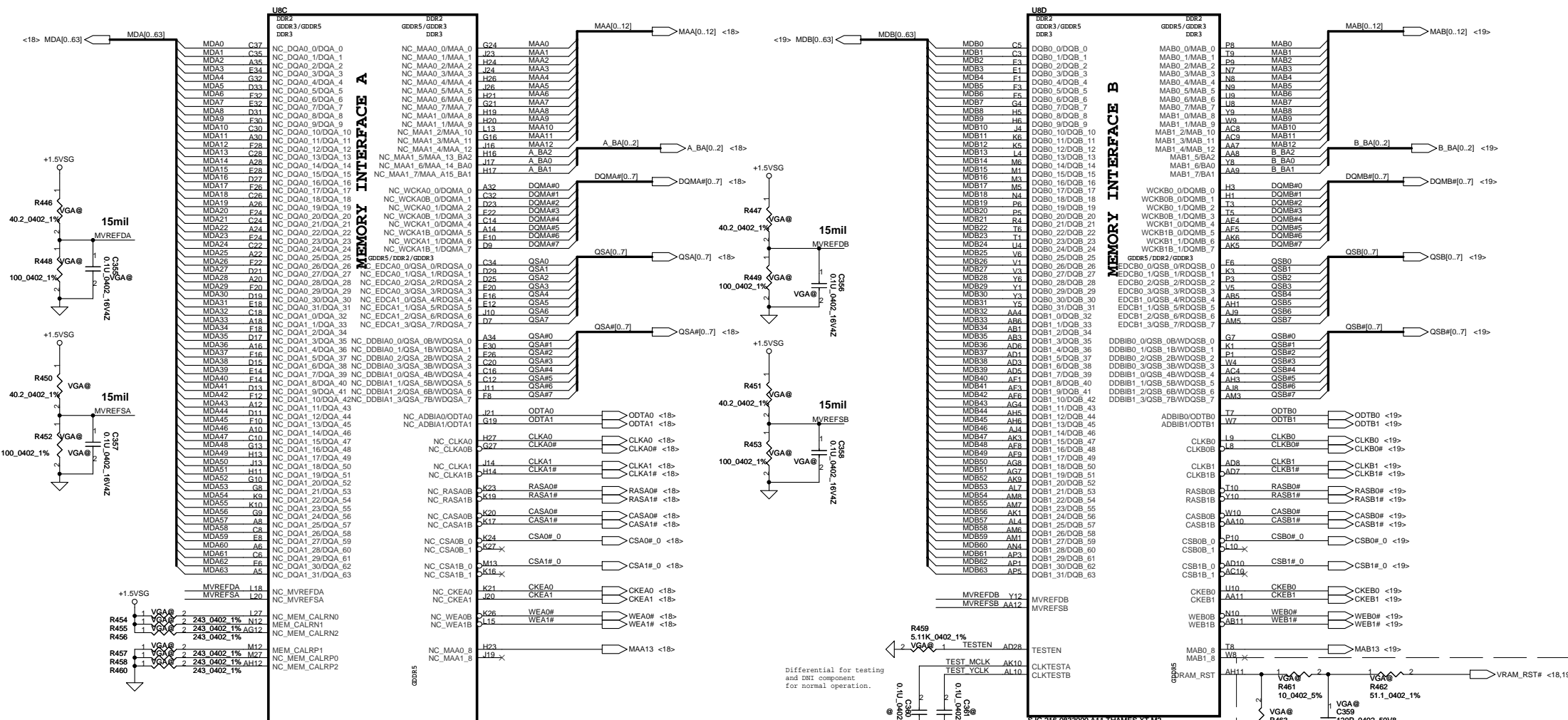
VGA@ L98

VGA@ L99

VGA@ L100

DVDPDATA	ID3ID2ID1ID0	Van SPD Name
001h	0 0 0 0	SAM 933 K4W1G1646G-BC11 64Mx16
011h	0 0 0 1	SAM 933 K4W2G1646G-BC11 128Mx16
02h	0 0 1 0	
03h	0 0 1 1	
04h	0 1 0 0	AMD 900 23EY2387MB11 64Mx16
05h	0 1 0 1	AMD 900 23EY4187M11 128Mx16
06h	0 1 1 0	
07h	0 1 1 1	
08h	1 0 0 0	HYN 900 H5TQ1G63DFR-11C
09h	1 0 0 1	HYN 900 H5TQ2G63BFR-11C
0Ah	1 0 1 0	
0Bh	1 0 1 1	
0Ch	1 1 0 0	MIC 900 MT41J64M16JT-107G:G
0Dh	1 1 0 1	MIC 900 MT41J128M16HA-107G:D
0Eh	1 1 1 0	
0Fh	1 1 1 1	





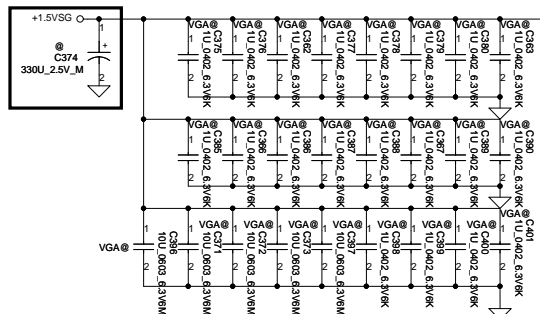
SC1216-0833000 A11 THAMES XT M2 THA

Place all these components very close to GPU (within 25mm) and keep all component close to each other (within 5mm) except Rser2

The suggested components are tested on the AMD reference board only. Customers must measure the slew on each memory part to ensure that the slew rate meets the DRAM specification.

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R04 Modify BOM



SM010030010

300ma 120ohm@100mhz DCR 0.3



120ohm/0.3A

Ref137-12- remove Bead



SM010030010

300ma 120ohm@100mhz DCR 0.3



120ohm/0.3A

470ohm/1A

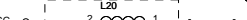
SM010030010

200ma 120ohm@100mhz DCR 0.2



SM010030010

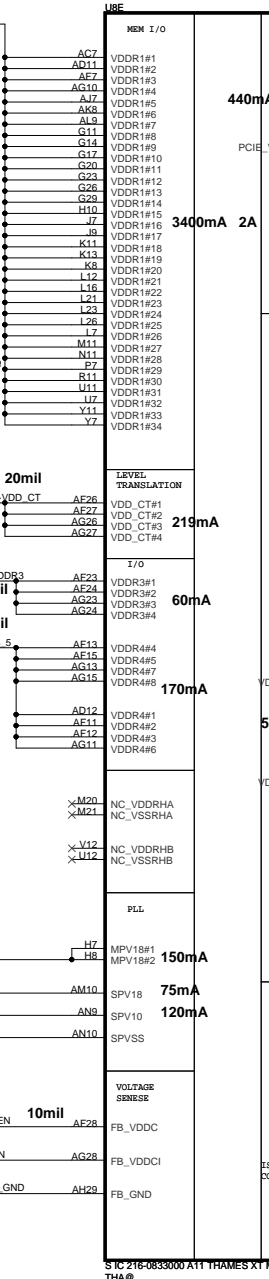
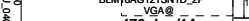
200ma 120ohm@100mhz DCR 0.2



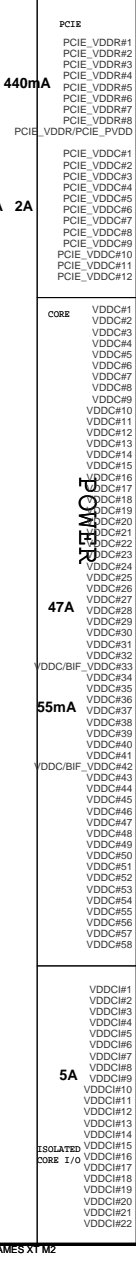
SM010030010

470ohm/1A

200ma 120ohm@100mhz DCR 0.2



3 IC 216-0833000 A11 THAMES XT M2 THA@



BIF\_VDDC  
Park/Madison: Connect to VDDC  
Seymour/Whisler:  
dGPU operating: VDDC  
BACO mode: +1.0V

2010/04/27  
non-BACO design, N27, T27  
connect BIF\_VDDC to VDDC  
For BACO design

VDDCI and VDDC should have separate regulators with a merge option on PCB  
For Madison and Park, VDDCI and VDDC can share one common regulator  
(GDDR3/DDR3 1.12V@4A VDDCI)

Granville VDDCI: 4.6A

SM01000BY00 5000ma 120ohm@100mhz DCR 0.02

No Pop for Heathrow and Chelsea

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AB39  
F39  
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F39  
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H31  
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H39  
J31  
J34  
K31  
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R34  
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GND#98

VSS\_MECH#1  
VSS\_MECH#2  
VSS\_MECH#3

A39 x  
A45 x  
AW38 x

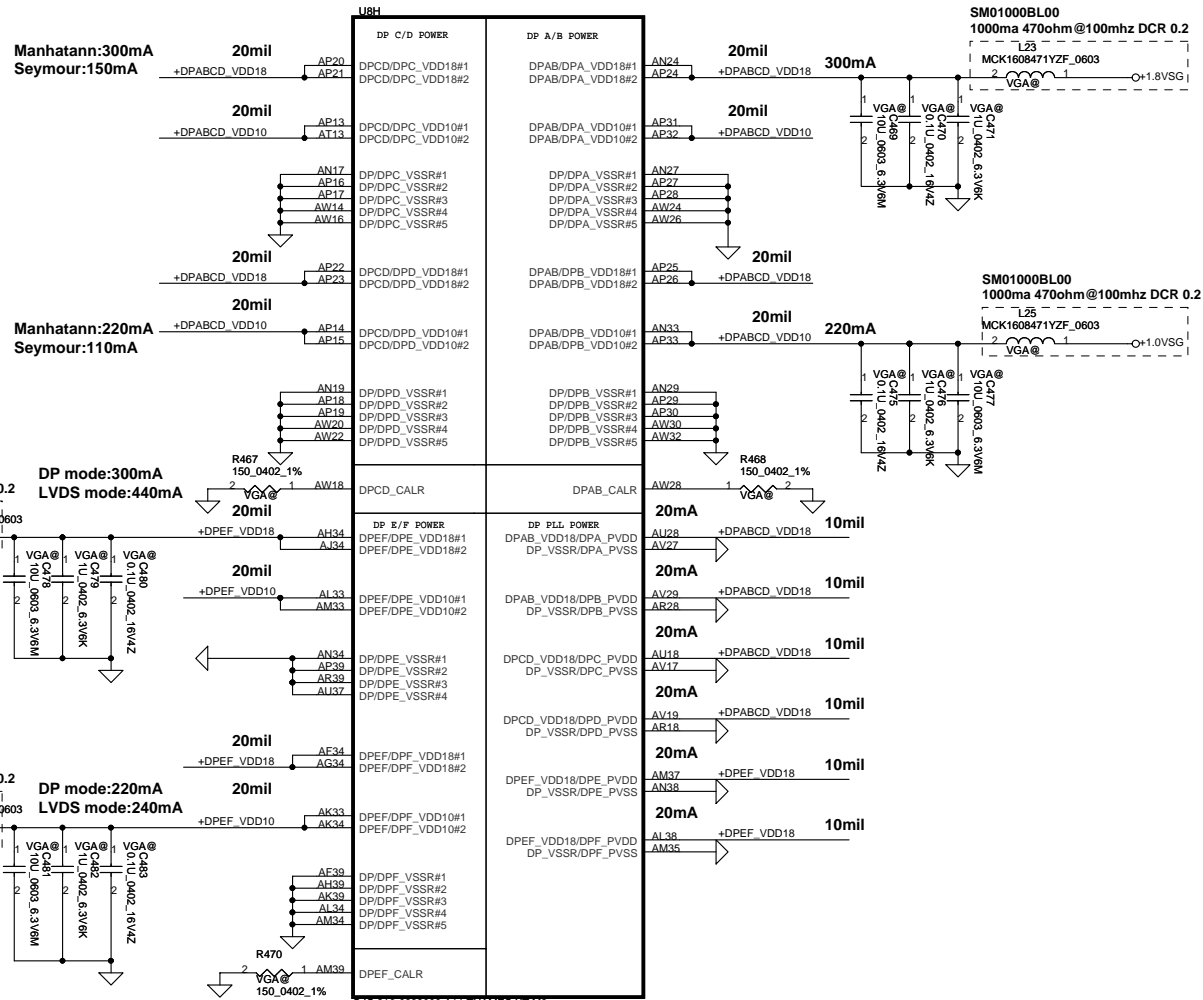
DPA\_VDD18,DPA\_PVDD,DPB\_VDD18,DPB\_PVDD  
can combian to DPAB\_VDD18  
DPC\_VDD18,DPC\_PVDD,DPD\_VDD18,DPD\_PVDD  
can combian to DPCD\_VDD18  
(DPD\_VDD18,DPD\_PVDD not applicable on Robson/Park)  
DPE\_VDD18,DPE\_PVDD,DPF\_VDD18,DPF\_PVDD  
can combian to DPEF\_VDD18

Seymour/Whistler :  
DPA\_VDD10,DPB\_VDD10  
can combian to DPAB\_VDD10  
DPC\_VDD10,DPD\_VDD10  
can combian to DPCD\_VDD10  
DPE\_VDD10,DPD\_VDD10  
can combian to DPEF\_VDD10

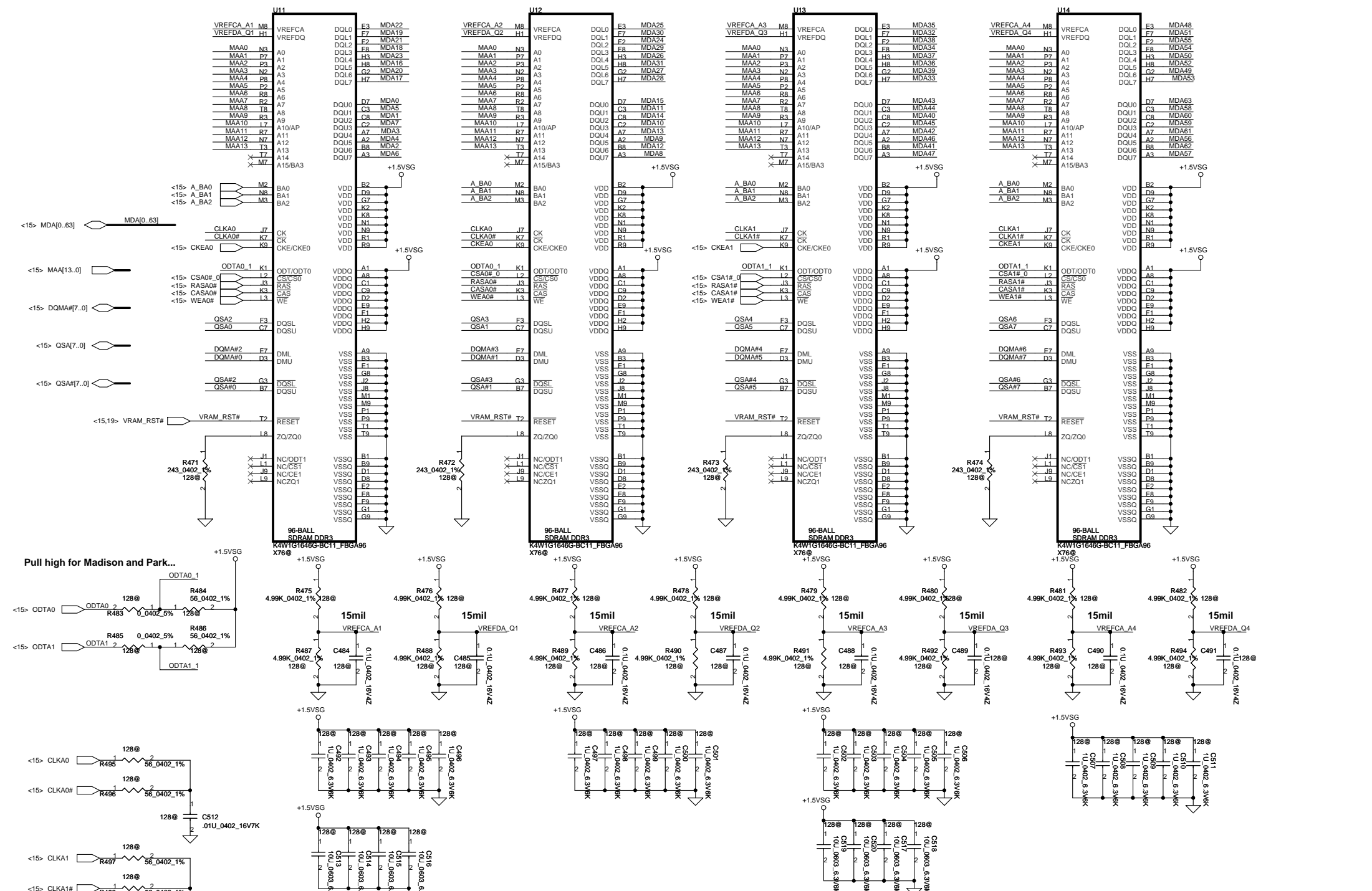
DPx-VSSR,DPx\_PVSS can combian to DP\_VSSR  
(Manhattan should have individual GND)  
where x is A,B,C,D,E,F

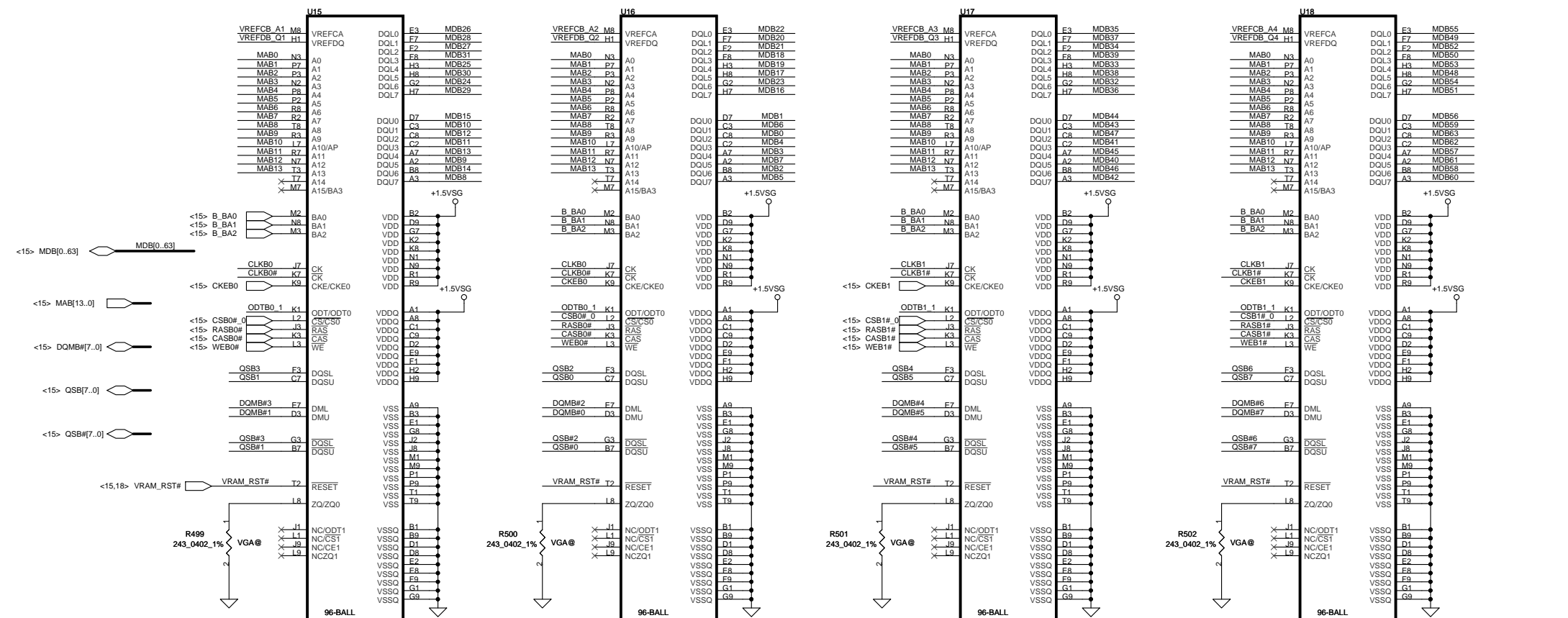
PX\_EN <-> PX\_EN <-20>  
PX\_EN: PU at P.20  
SBIOS will control VGA power on/off.  
High :BACO mode enable  
LOW:BACO disable

Park/Madison :AL21:left NC  
Seymour/Whistler:  
AL21:PX\_EN  
use to control discreate GPU regulators  
for power express BACO mode  
Support BACO:  
output High3.3V:turn off regulators (BACO mode on)  
output Low0V:turn on regulators (BACO mode off)  
need PD resistor  
No support BACO:  
left NC

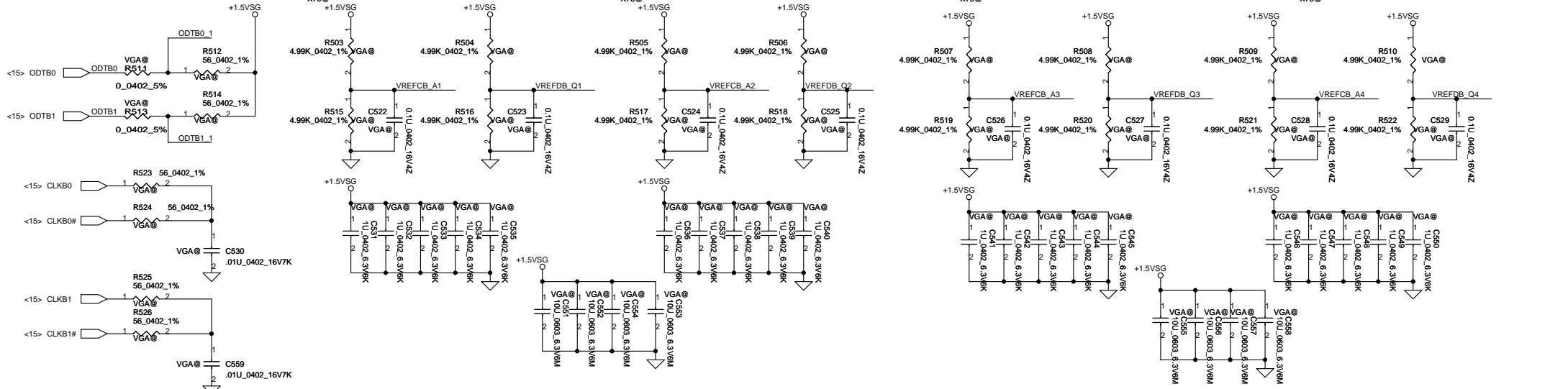


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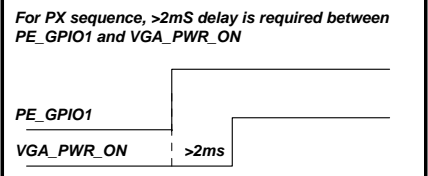
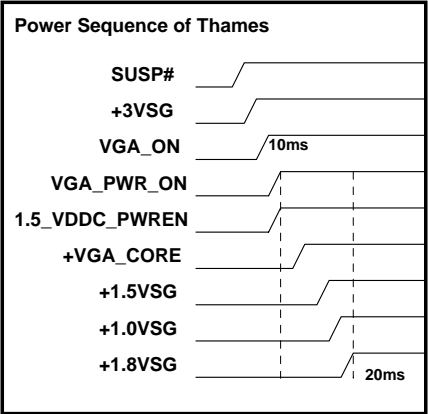




Pull high for Madison and Park...



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### VGA Muxless and Dis only Status Mapping table

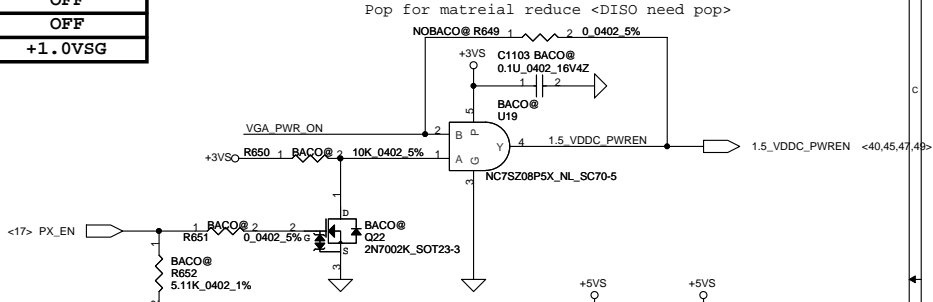
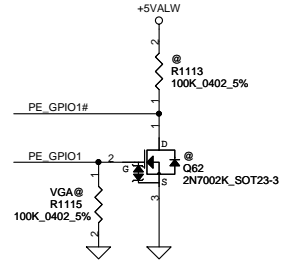
	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

### VGA Muxless with BACO Status Mapping table

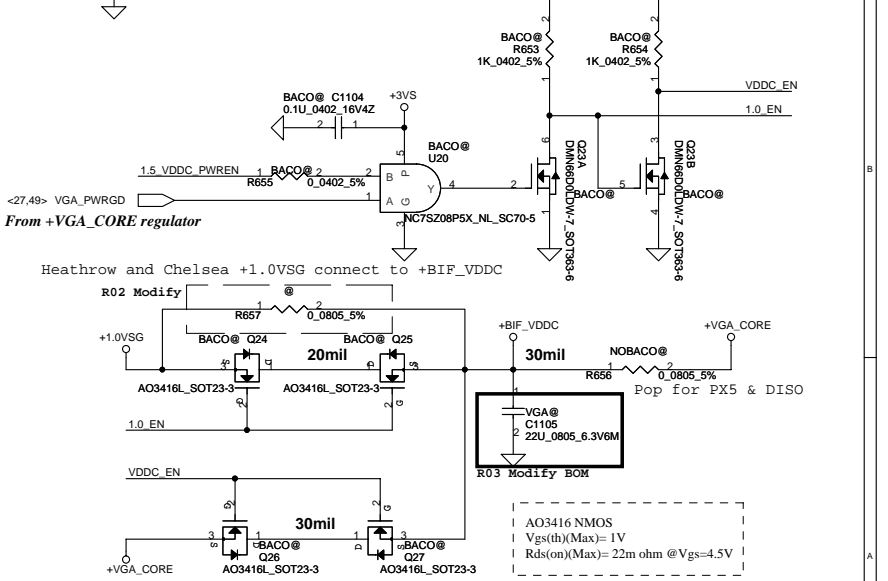
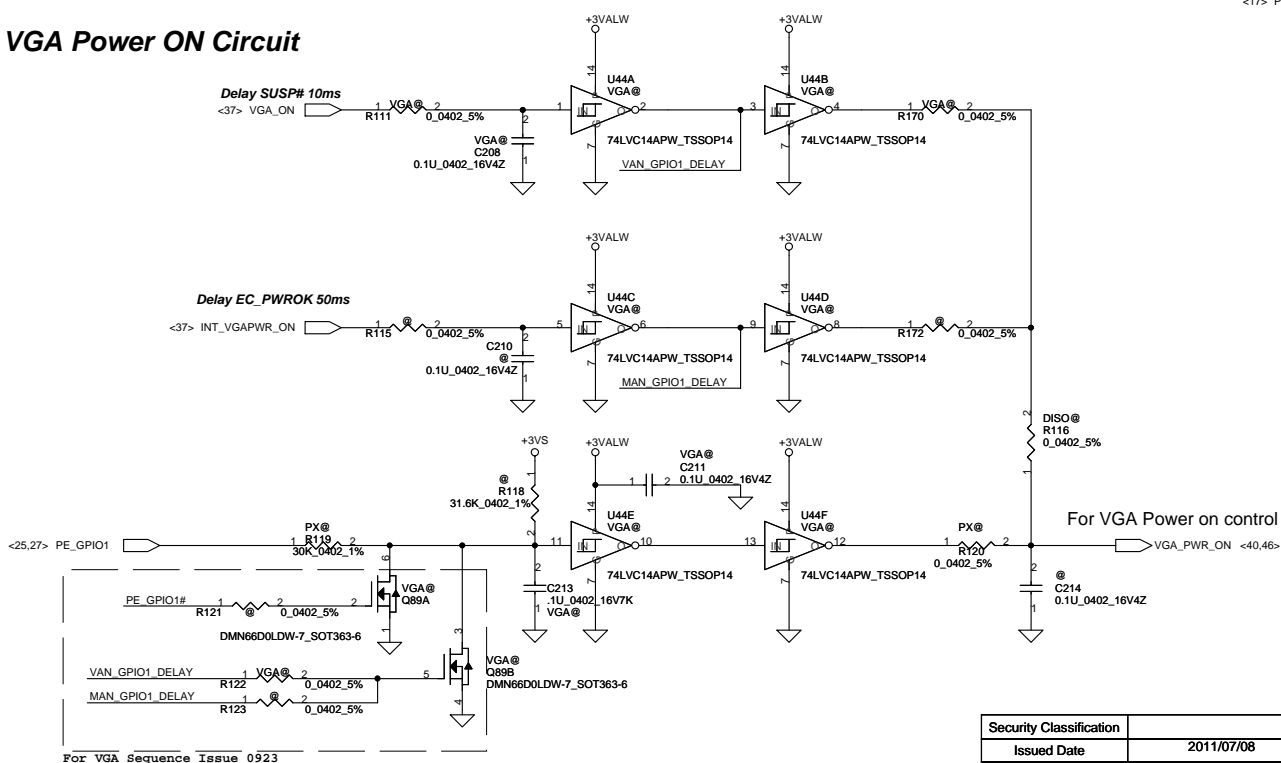
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

### VGA Power Enable Signal Mapping table

	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN



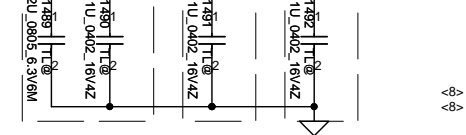
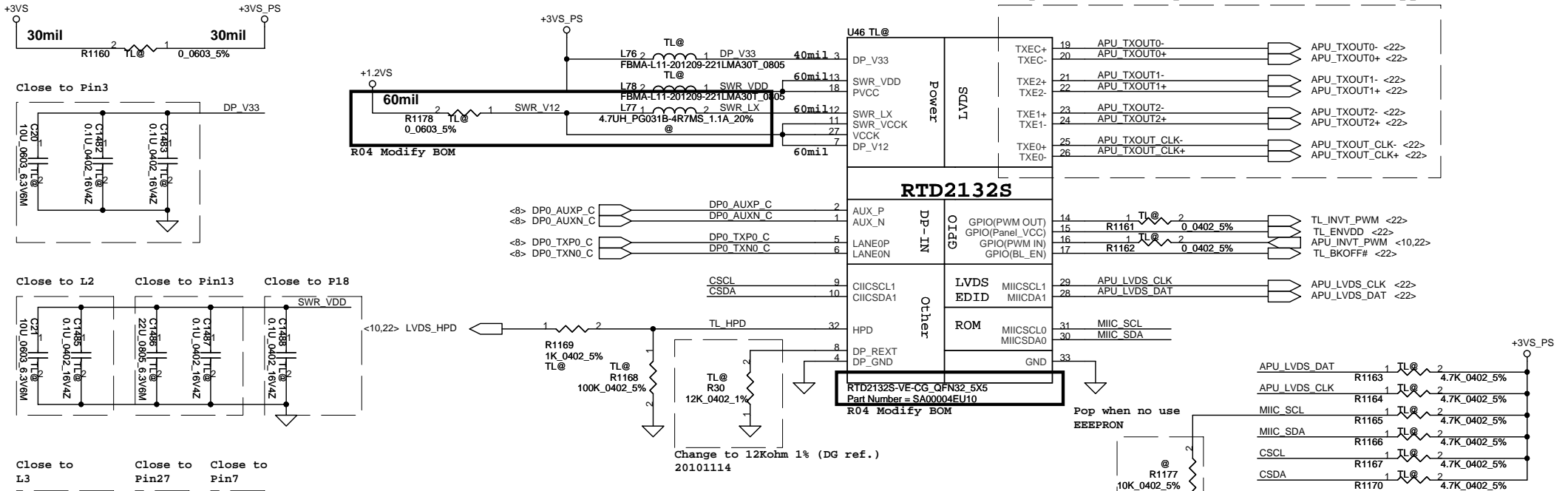
## VGA Power ON Circuit



For VGA Sequence Issue 0923

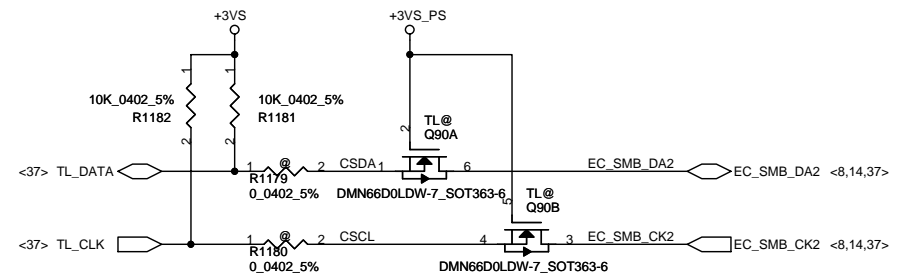
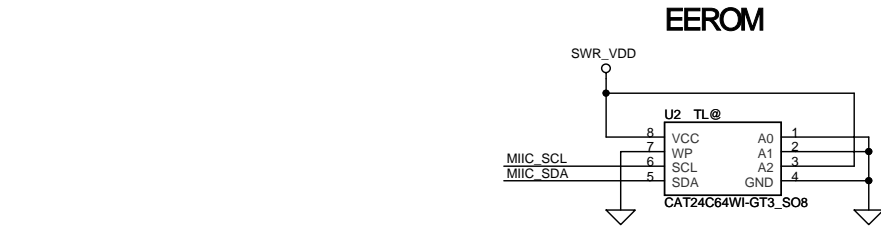
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Swap for Meet 40 pin LVDS define (FW Support)



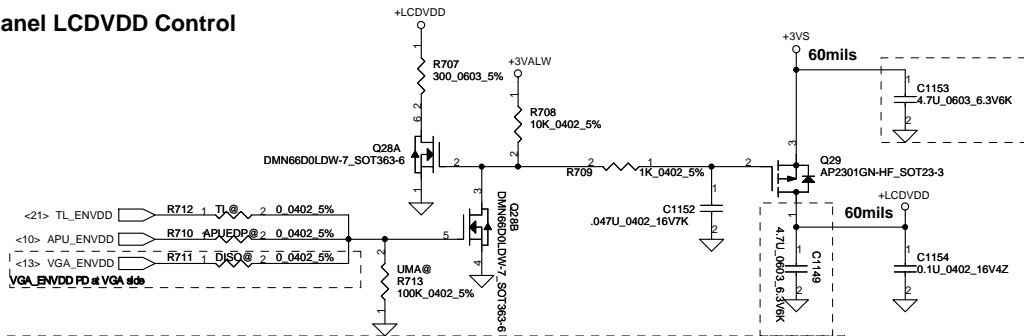
APU Co-layer eDP function

DP0_TXP0_C	R1171	1	2	APUEDP@	0.0402_5%	APU_TXOUT2+
DP0_TXN0_C	R1172	1	2	APUEDP@	0.0402_5%	APU_TXOUT2-
DP0_TXP1_C	R1173	1	2	APUEDP@	0.0402_5%	APU_TXOUT1+
DP0_TXN1_C	R1174	1	2	APUEDP@	0.0402_5%	APU_TXOUT1-
DP0_AUXP_C	R1175	1	2	APUEDP@	0.0402_5%	APU_LVDS_CLK
DP0_AUXN_C	R1176	1	2	APUEDP@	0.0402_5%	APU_LVDS_DAT

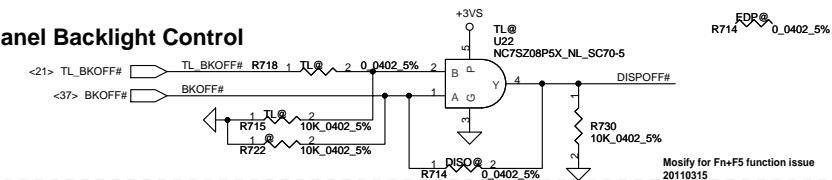


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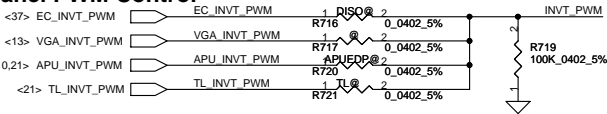
### Panel LCDVDD Control



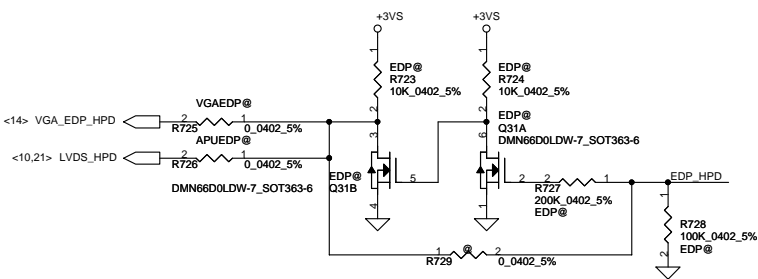
### Panel Backlight Control



### Panel PWM Control



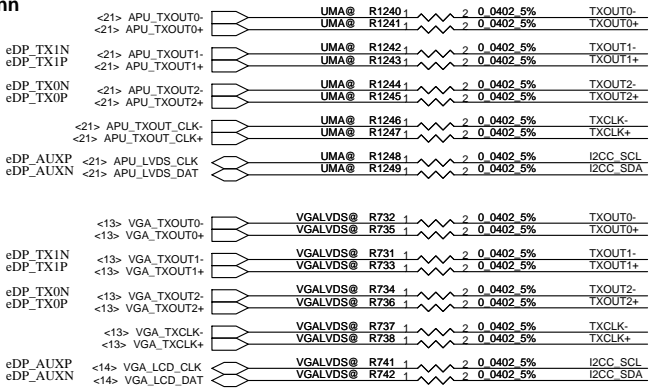
### eDP HDP for APU and VGA



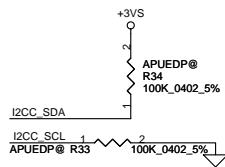
### Place near LVDS Conn

#### Translator LVDS Output

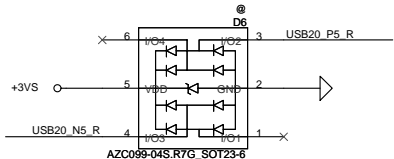
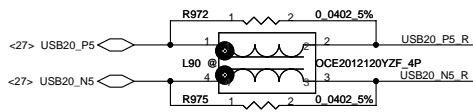
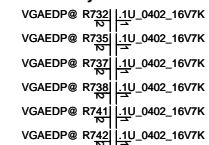
#### VGA LVDS Output



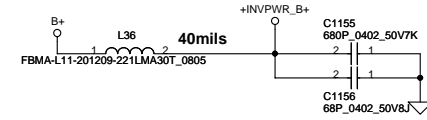
DG ref. Need close to eDP Conn.  
201011251400



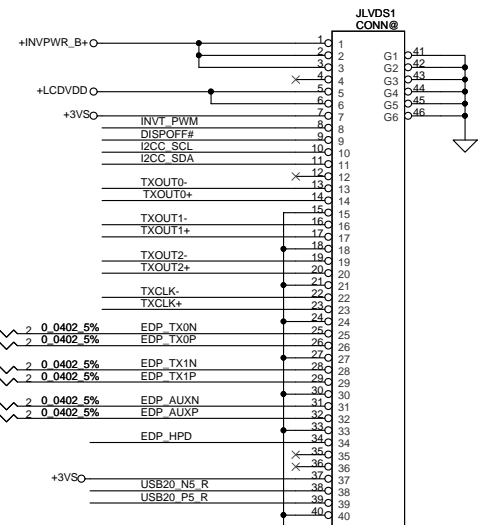
#### VGA Co-lay eDP function



UMA/DIS LVDS/eDP Mapping table				
UMA		DIS		Panel
LVDS	eDP	LVDS	eDP	Conn.
APU_TXOUT0+		VGA_TXOUT0+		TXOUT0+
APU_TXOUT0-		VGA_TXOUT0-		TXOUT0-
APU_TXOUT1+	DP0_TXP1_R	VGA_TXOUT1+	eDP_TX1P	TXOUT1+
APU_TXOUT1-	DP0_TXN1_R	VGA_TXOUT1-	eDP_TX1N	TXOUT1-
APU_TXOUT2+	DP0_TXP0_R	VGA_TXOUT2+	eDP_TX0P	TXOUT2+
APU_TXOUT2-	DP0_TXN0_R	VGA_TXOUT2-	eDP_TX0N	TXOUT2-
APU_TXOUT_CLK+		VGA_TXCLK+		TXCLK+
APU_TXOUT_CLK-		VGA_TXCLK-		TXCLK-
APU_TZOUT0+		VGA_TZOUT0+		TZOUT0+
APU_TZOUT0-		VGA_TZOUT0-		TZOUT0-
APU_TZOUT1+		VGA_TZOUT1+		TZOUT1+
APU_TZOUT1-		VGA_TZOUT1-		TZOUT1-
APU_TZOUT2+		VGA_TZOUT2+		TZOUT2+
APU_TZOUT2-		VGA_TZOUT2-		TZOUT2-
APU_TZOUT_CLK+		VGA_TZCLK+		TZCLK+
APU_TZOUT_CLK-		VGA_TZCLK-		TZCLK-
APU_LVDS_CLK	DP0_AUXP_R	VGA_LCD_CLK	eDP_AUXN	I2CC_SCL
APU_LVDS_DAT	DP0_AUXN_R	VGA_LCD_DATA	eDP_AUXN	I2CC_SDA

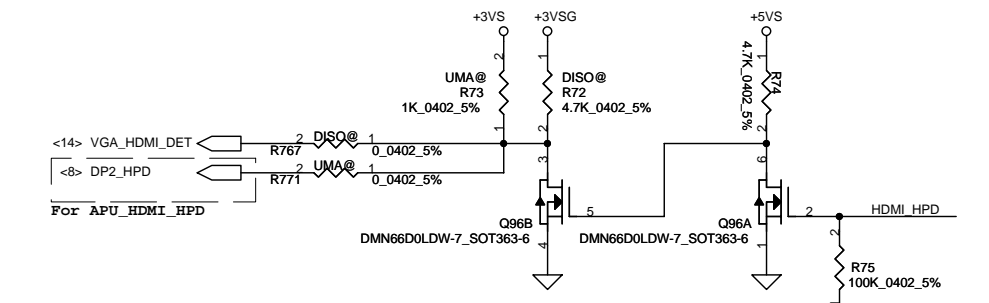
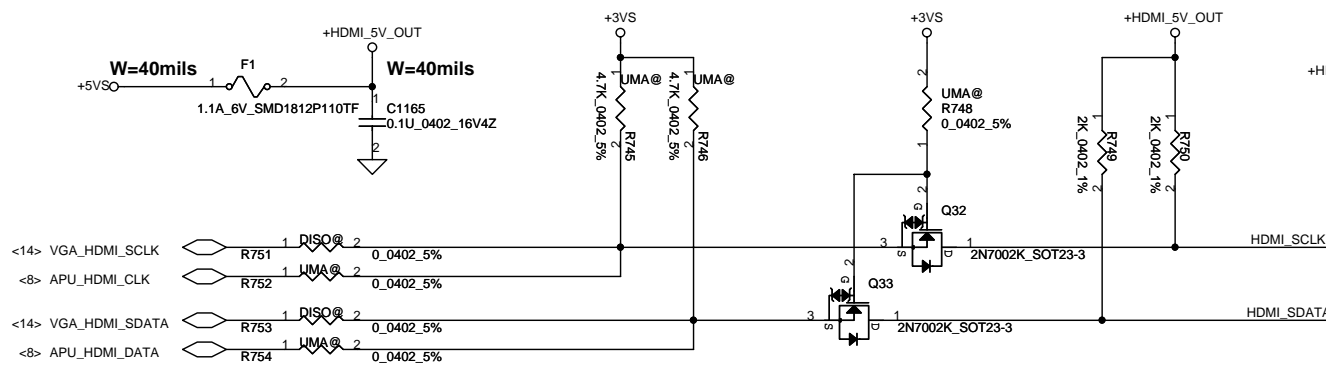


### LCD/LED PANEL Conn.



I-PEX\_20143-040E-20F  
Part Number = SP010016810  
PCB Footprint = I-PEX\_20143-040E-20F\_40P

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**From VGA**

<14> VGA_HDMI_TXD2-	DISO@R757	1	2	0.0402_5%	HDMI C TX2- R
<14> VGA_HDMI_TXD2+	DISO@R758	1	2	0.0402_5%	HDMI C TX2+ R
<14> VGA_HDMI_TXD1-	DISO@R759	1	2	0.0402_5%	HDMI C TX1- R
<14> VGA_HDMI_TXD1+	DISO@R760	1	2	0.0402_5%	HDMI C TX1+ R
<14> VGA_HDMI_TXD0-	DISO@R761	1	2	0.0402_5%	HDMI C TX0- R
<14> VGA_HDMI_TXD0+	DISO@R762	1	2	0.0402_5%	HDMI C TX0+ R
<14> VGA_HDMI_TXC-	DISO@R763	1	2	0.0402_5%	HDMI C TXC- R
<14> VGA_HDMI_TXC+	DISO@R764	1	2	0.0402_5%	HDMI C TXC+ R
<14> VGA_HDMI_TXD2-	DISO@R757	1	2	0.0402_5%	HDMI C TX2- R
<14> VGA_HDMI_TXD2+	DISO@R758	1	2	0.0402_5%	HDMI C TX2+ R
<14> VGA_HDMI_TXD1-	DISO@R759	1	2	0.0402_5%	HDMI C TX1- R
<14> VGA_HDMI_TXD1+	DISO@R760	1	2	0.0402_5%	HDMI C TX1+ R
<14> VGA_HDMI_TXD0-	DISO@R761	1	2	0.0402_5%	HDMI C TX0- R
<14> VGA_HDMI_TXD0+	DISO@R762	1	2	0.0402_5%	HDMI C TX0+ R
<14> VGA_HDMI_TXC-	DISO@R763	1	2	0.0402_5%	HDMI C TXC- R
<14> VGA_HDMI_TXC+	DISO@R764	1	2	0.0402_5%	HDMI C TXC+ R

**From APU**

<8> APU_HDMI_TXD2-	UMA@R770	1	2	0.0402_5%	HDMI C TX2- R
<8> APU_HDMI_TXD2+	UMA@R772	1	2	0.0402_5%	HDMI C TX2+ R
<8> APU_HDMI_TXD1-	UMA@R773	1	2	0.0402_5%	HDMI C TX1- R
<8> APU_HDMI_TXD1+	UMA@R774	1	2	0.0402_5%	HDMI C TX1+ R
<8> APU_HDMI_TXD0-	UMA@R776	1	2	0.0402_5%	HDMI C TX0- R
<8> APU_HDMI_TXD0+	UMA@R777	1	2	0.0402_5%	HDMI C TX0+ R
<8> APU_HDMI_TXC-	UMA@R778	1	2	0.0402_5%	HDMI C TXC- R
<8> APU_HDMI_TXC+	UMA@R780	1	2	0.0402_5%	HDMI C TXC+ R

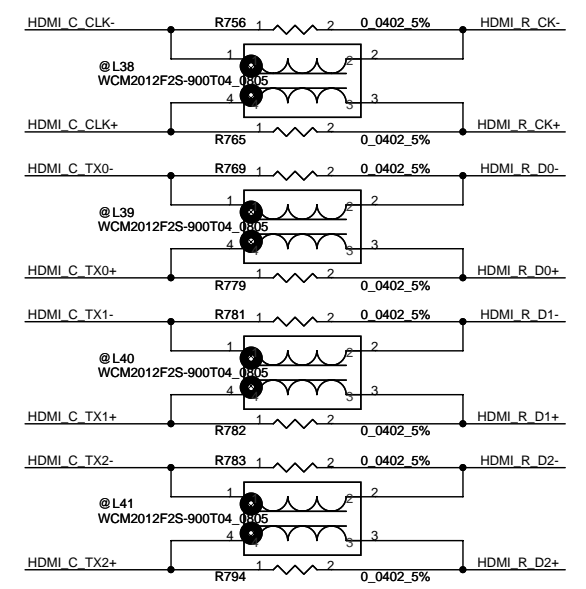
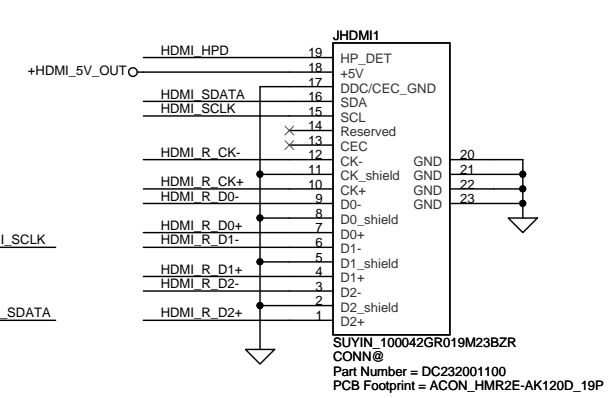
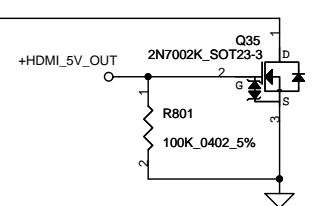
**UMA use 604 ohm SCL v1.01  
VGA use 499 ohm**

**For UMA HDMI  
termination BOM option**

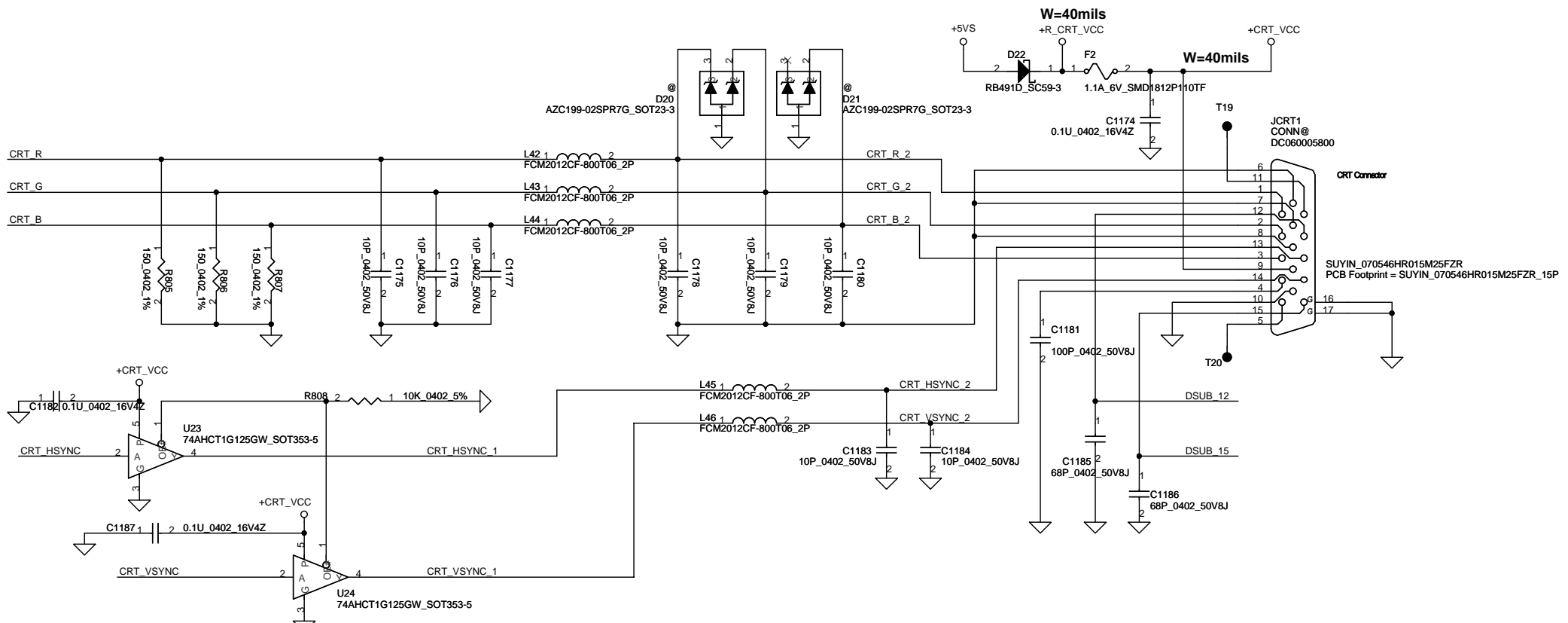
R784	2	UMA@1	604_0402_1%
R786	2	UMA@1	604_0402_1%
R788	2	UMA@1	604_0402_1%
R790	2	UMA@1	604_0402_1%
R792	2	UMA@1	604_0402_1%
R795	2	UMA@1	604_0402_1%
R797	2	UMA@1	604_0402_1%
R799	2	UMA@1	604_0402_1%

**Near the connector**

HDMI C TX2- R C1166	1	.1U_0402_16V	HDMI C TX2-DISO@R784	1	2	499_0402_1%
HDMI C TX2+ R C1167	1	.1U_0402_16V	HDMI C TX2-DISO@R786	1	2	499_0402_1%
HDMI C TX1- R C1168	1	.1U_0402_16V	HDMI C TX1-DISO@R788	1	2	499_0402_1%
HDMI C TX1+ R C1169	1	.1U_0402_16V	HDMI C TX1-DISO@R790	1	2	499_0402_1%
HDMI C TX0- R C1170	1	.1U_0402_16V	HDMI C TX0-DISO@R792	1	2	499_0402_1%
HDMI C TX0+ R C1171	1	.1U_0402_16V	HDMI C TX0-DISO@R795	1	2	499_0402_1%
HDMI C CLK- R C1172	1	.1U_0402_16V	HDMI C CLK-DISO@R797	1	2	499_0402_1%
HDMI C CLK+ R C1173	1	.1U_0402_16V	HDMI C CLK-DISO@R799	1	2	499_0402_1%



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**Use common via**

<26>	FCH_CRT_R	FCH_CRT_R	R809	2	JMA@	1	0.0402_5%	CRT_R
<26>	FCH_CRT_G	FCH_CRT_G	R810	2	JMA@	1	0.0402_5%	CRT_G
<26>	FCH_CRT_B	FCH_CRT_B	R811	2	JMA@	1	0.0402_5%	CRT_B

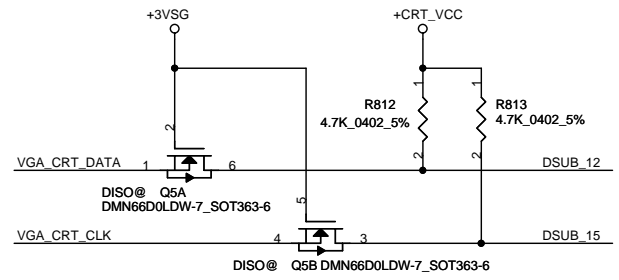
**From FCH**

<26>	FCH_CRT_HSYNC	FCH_CRT_HSYNC	R814	2	JMA@	1	0.0402_5%	CRT_HSYNC
<26>	FCH_CRT_VSYNC	FCH_CRT_VSYNC	R815	2	JMA@	1	0.0402_5%	CRT_VSYNC
<26>	FCH_CRT_DDC_SDA	FCH_CRT_DDC_SDA	R816	2	JMA@	1	0.0402_5%	DSUB_12
<26>	FCH_CRT_DDC_SCL	FCH_CRT_DDC_SCL	R817	2	JMA@	1	0.0402_5%	DSUB_15

**From VGA**

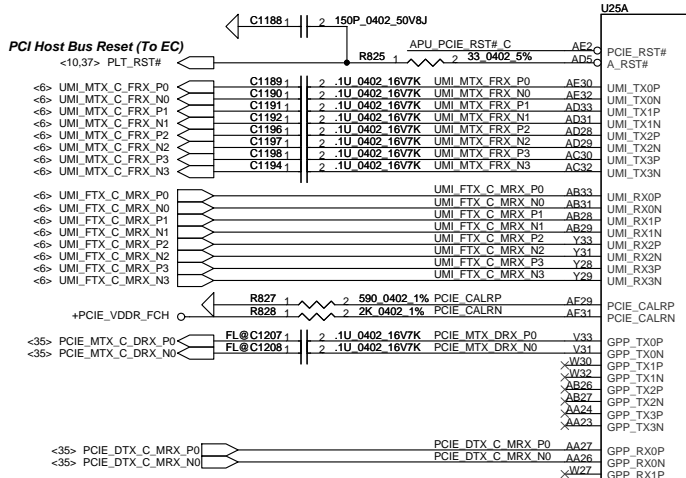
<14>	VGA_CRT_R	VGA_CRT_R	R818	2	DISO@	1	0.0402_5%	CRT_R
<14>	VGA_CRT_G	VGA_CRT_G	R819	2	DISO@	1	0.0402_5%	CRT_G
<14>	VGA_CRT_B	VGA_CRT_B	R820	2	DISO@	1	0.0402_5%	CRT_B
<14>	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R821	2	DISO@	1	0.0402_5%	CRT_HSYNC
<14>	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R822	2	DISO@	1	0.0402_5%	CRT_VSYNC
<14>	VGA_CRT_DATA	VGA_CRT_DATA						
<14>	VGA_CRT_CLK	VGA_CRT_CLK						

**Close to Conn side**

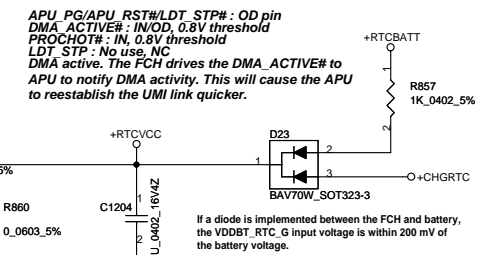
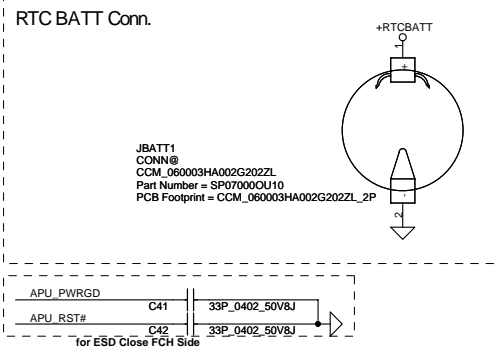
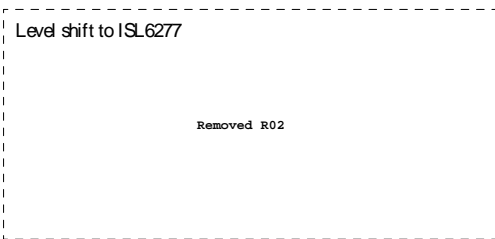
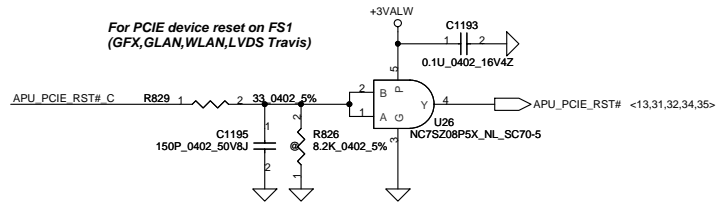
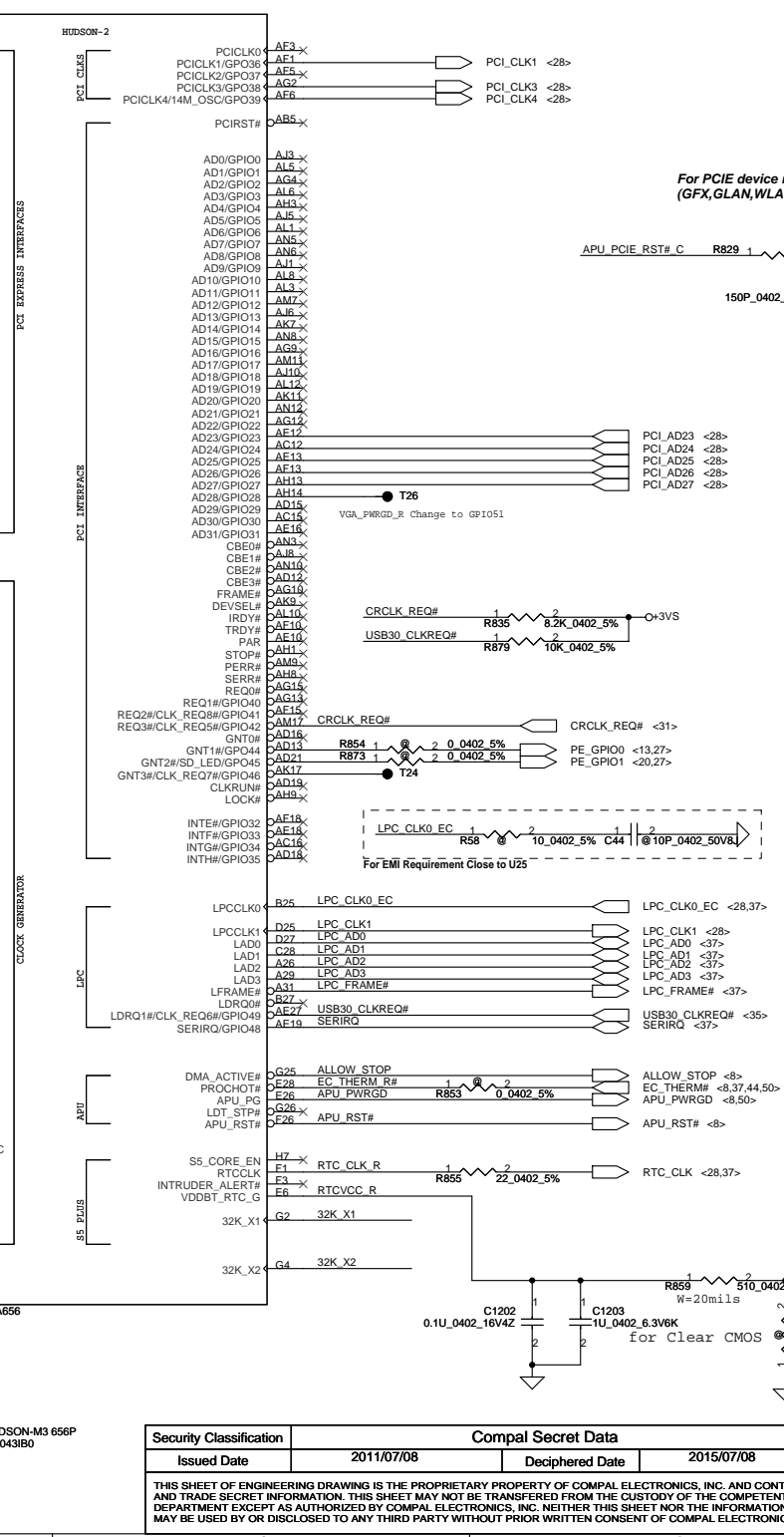
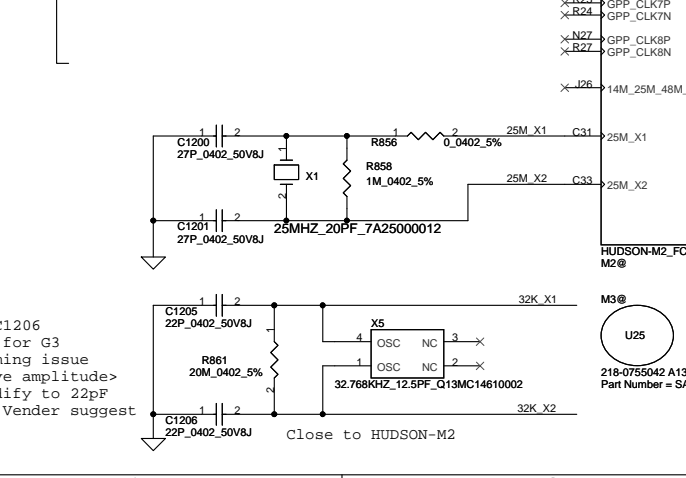
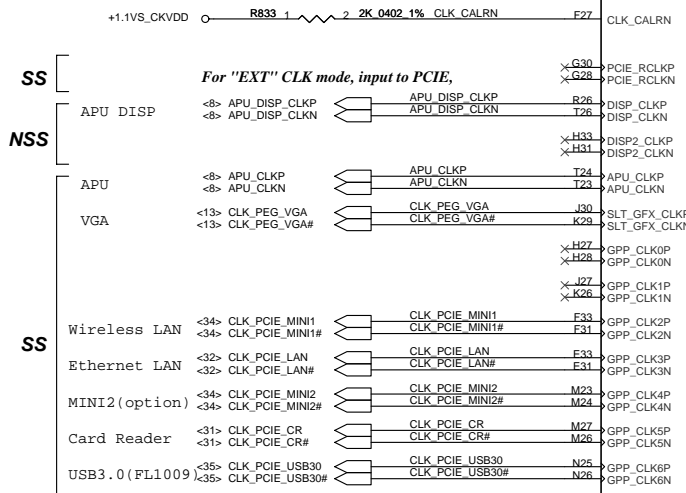


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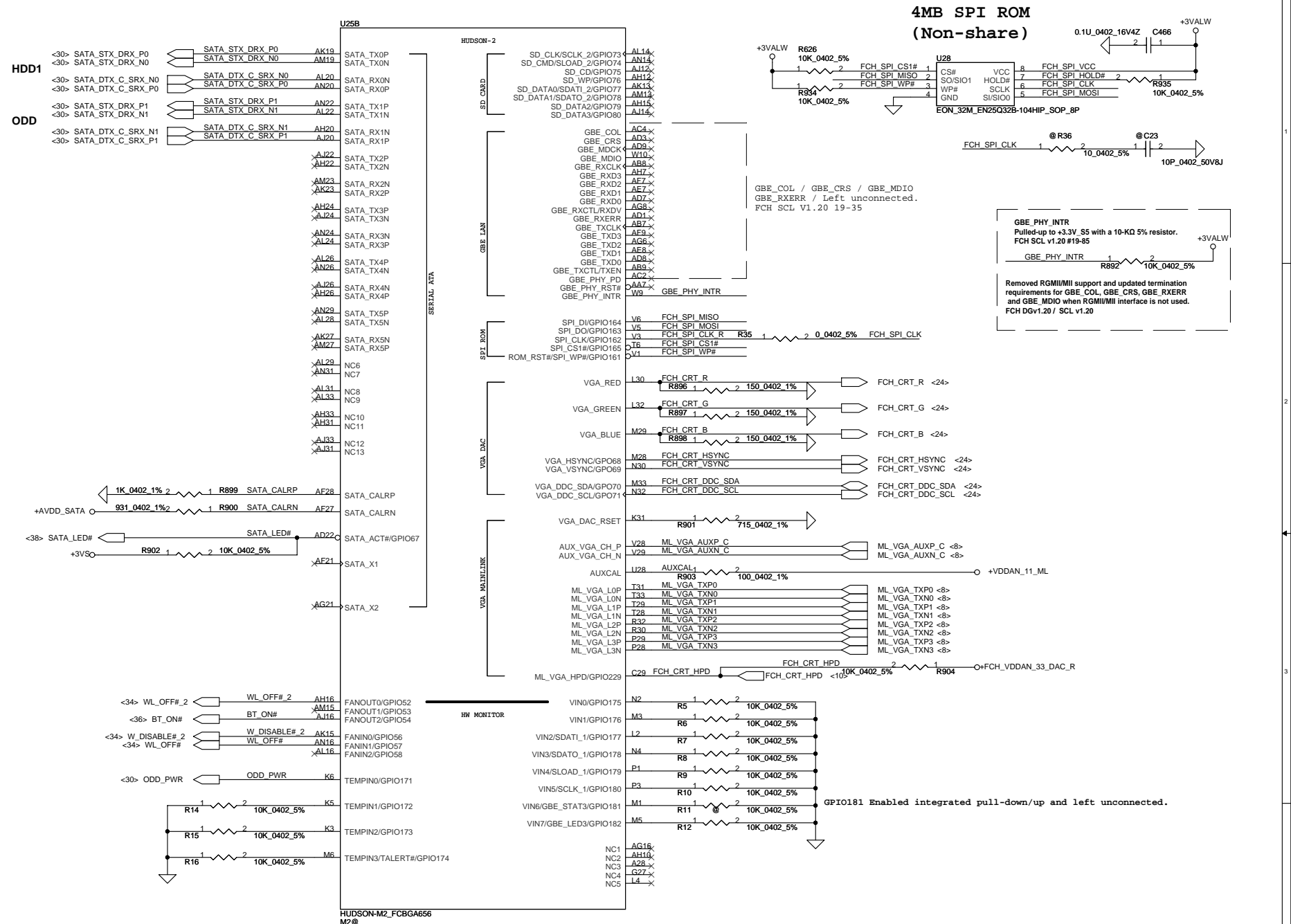




**GPP Port 0 For USB30 on S/SUB**  
**GPP Port 1 For USB30 on M/B 20101103**



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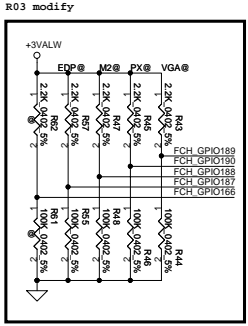
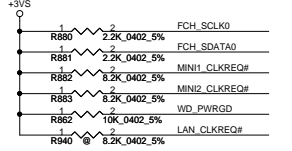
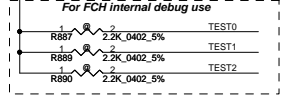
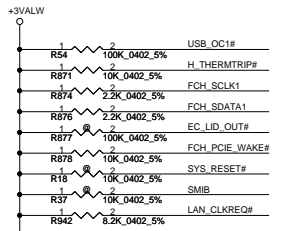
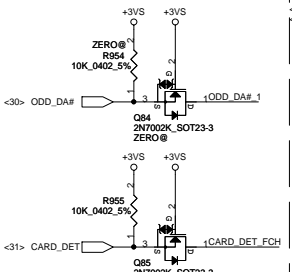
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FCH\_PCIE\_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

**THERMTRIP:**  
Need level shift from +3VALW to +1.5V  
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

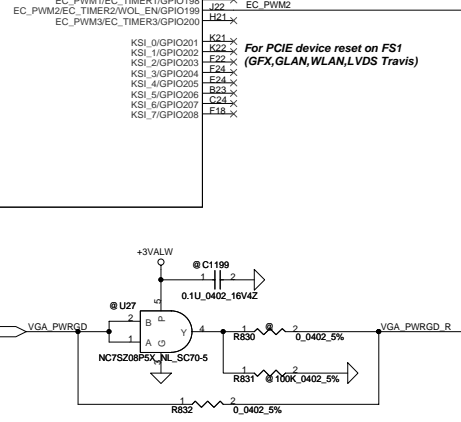
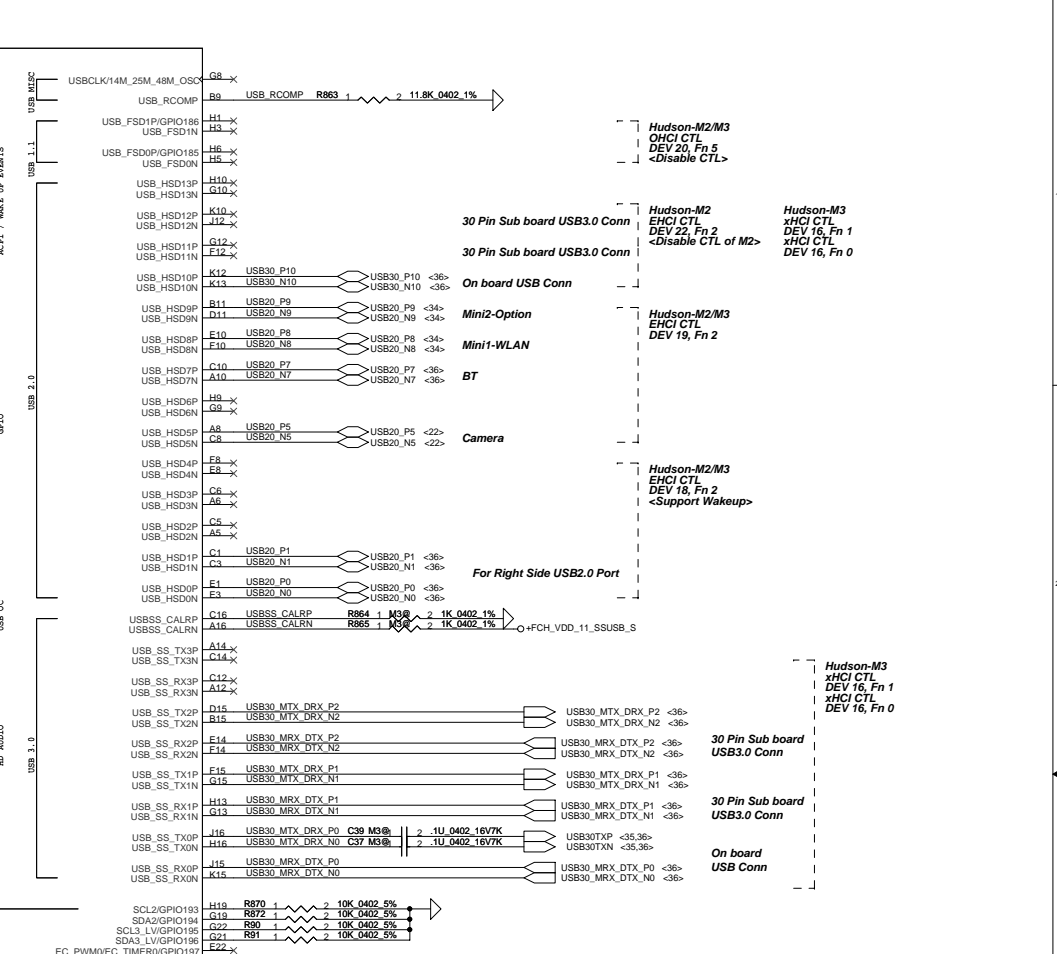
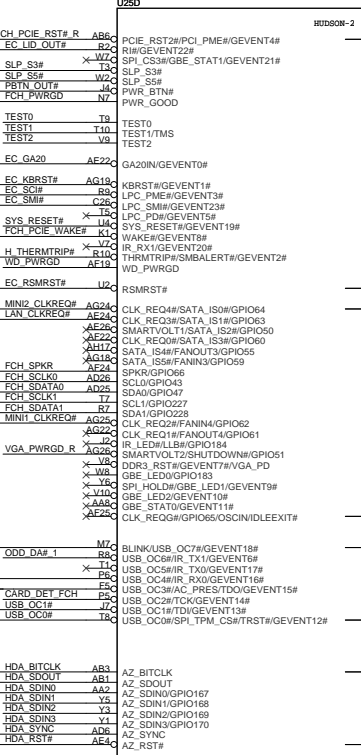
SM bus 0 -> S0 PWR domain  
SM bus 1 -> S5 PWR domain

FCH GEVENT (S5 domain) with isolation circuit to avoid leakage



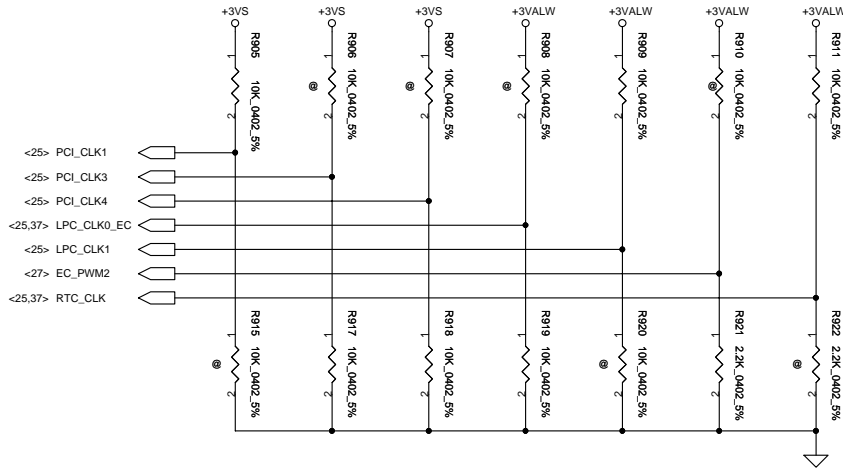
Project SKU ID	Value
GPIO189 (use VGA)	Low (UMA) High (VGA)
GPIO190 (use PX)	Low (noPX) High (PX)
GPIO188 (USBZ3)	High (Z.0) Low (3.0)
GPIO187 (LVDS/nDP)	Low (LVDS) High (nDP)
GPIO166 (Reservd)	

**R03 modify**  
Update BOM Structure



# STRAP PINS

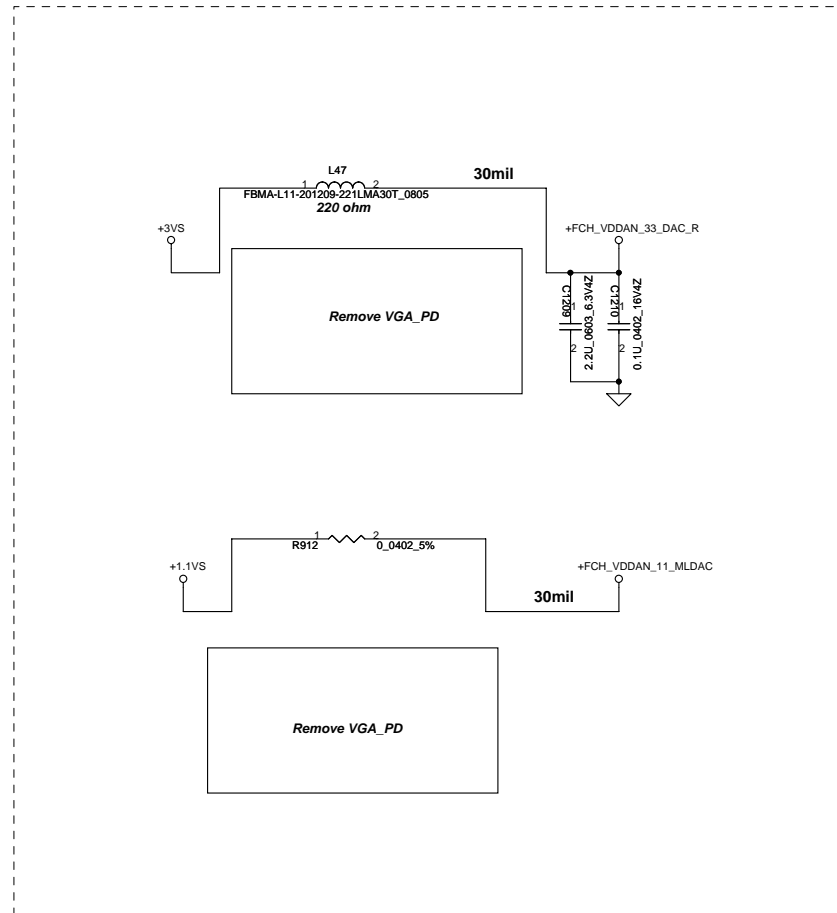
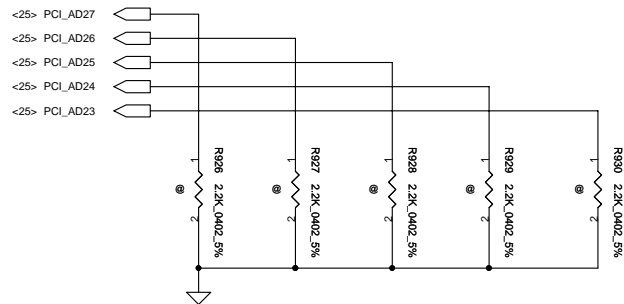
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
<b>PULL HIGH</b>	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
<b>PULL LOW</b>	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



# DEBUG STRAPS

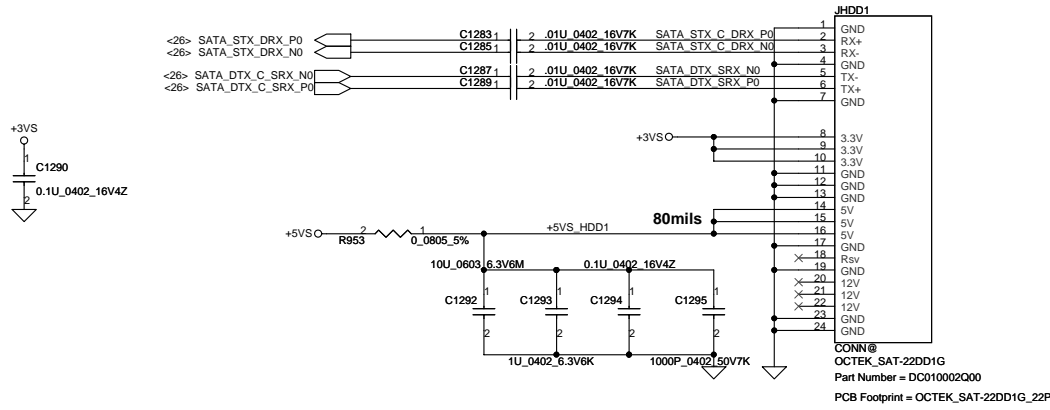
FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

PCI_AD26	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

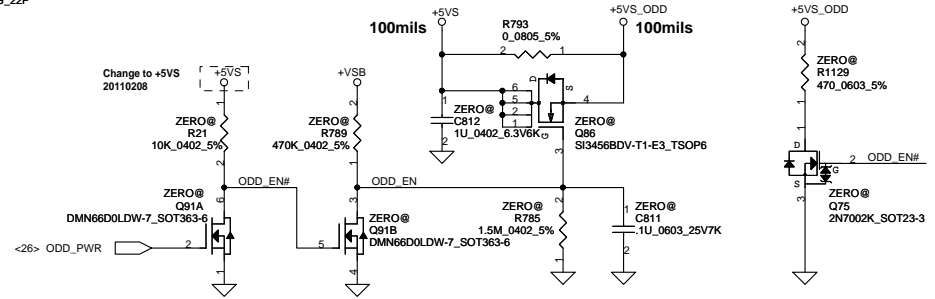
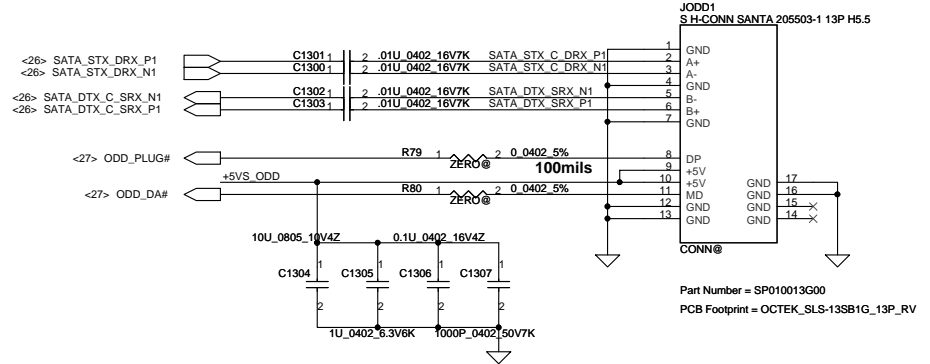




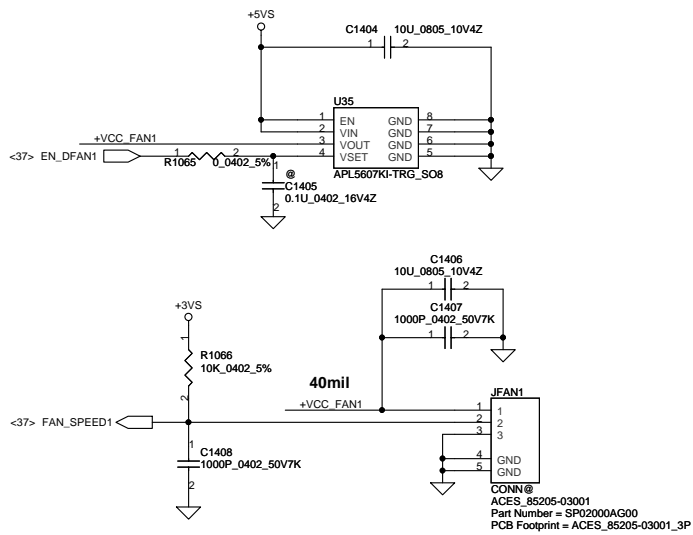
SATA HDD1 Conn.



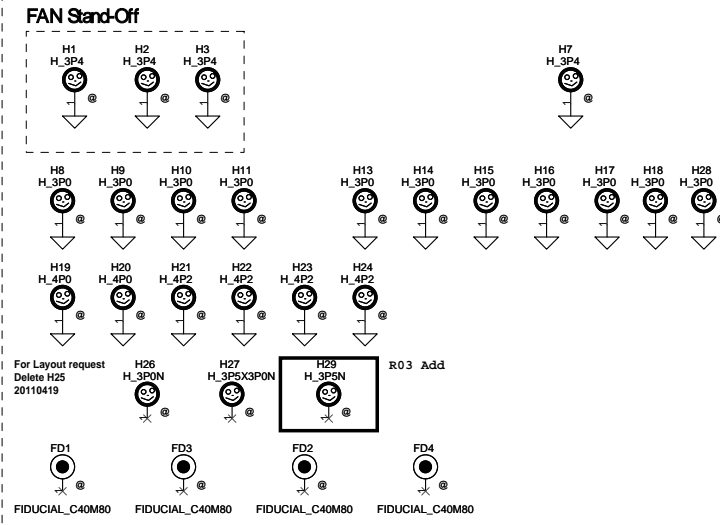
SATA ODD Conn.



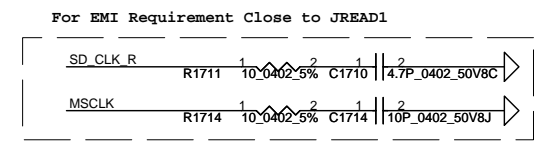
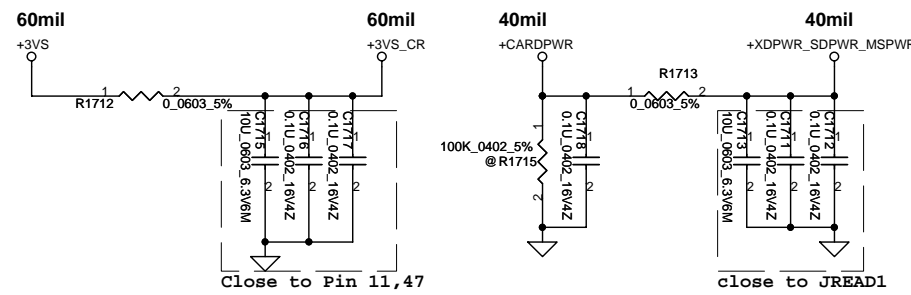
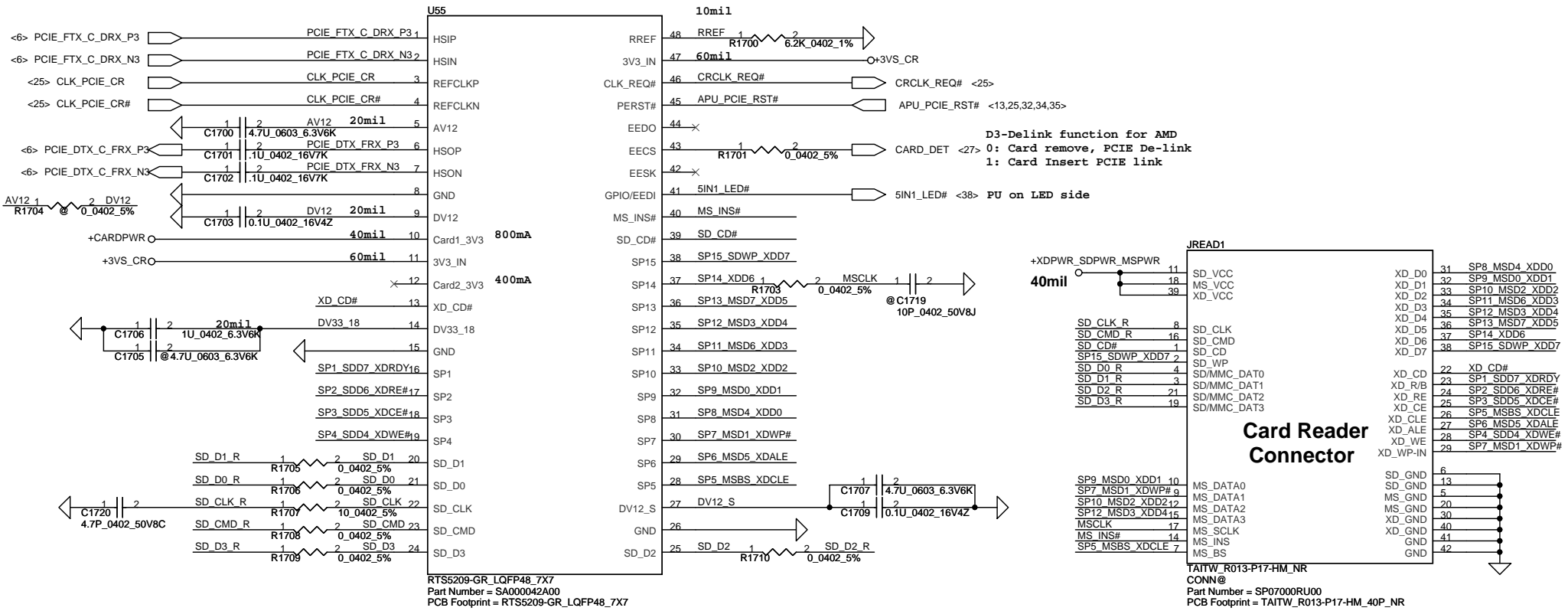
FAN



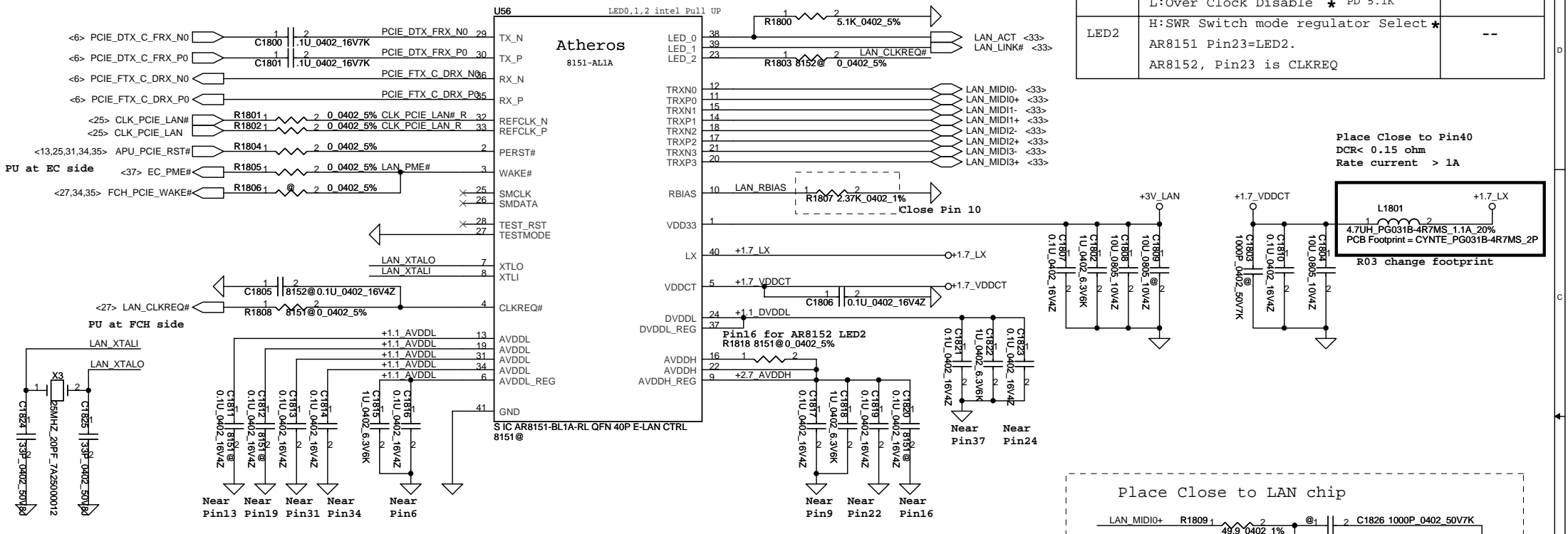
Screw Hole Follow P5WE0



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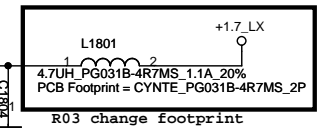
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Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable * PD 5.1K	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

Place Close to Pin40  
DCR< 0.15 ohm  
Rate current > 1A



PU at EC side <37> EC\_PME#

<27,34,35> FCH\_PCIE\_WAKE#

PU at FCH side

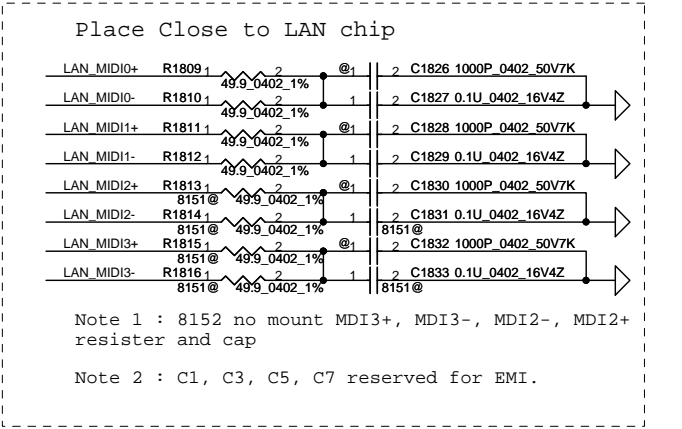
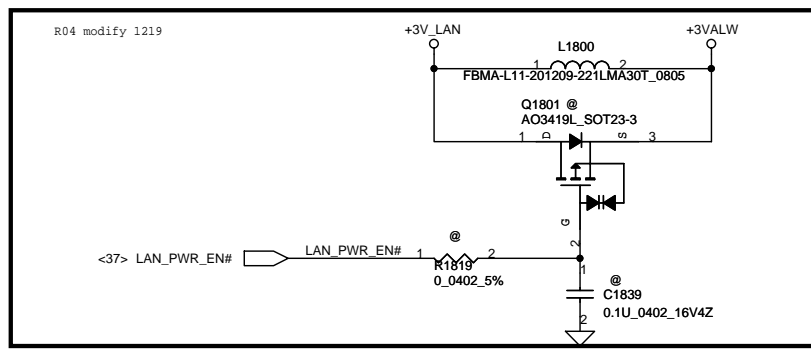
LAN\_XTALO

LAN\_XTALI

Pin13 Pin19 Pin31 Pin34

Pin6

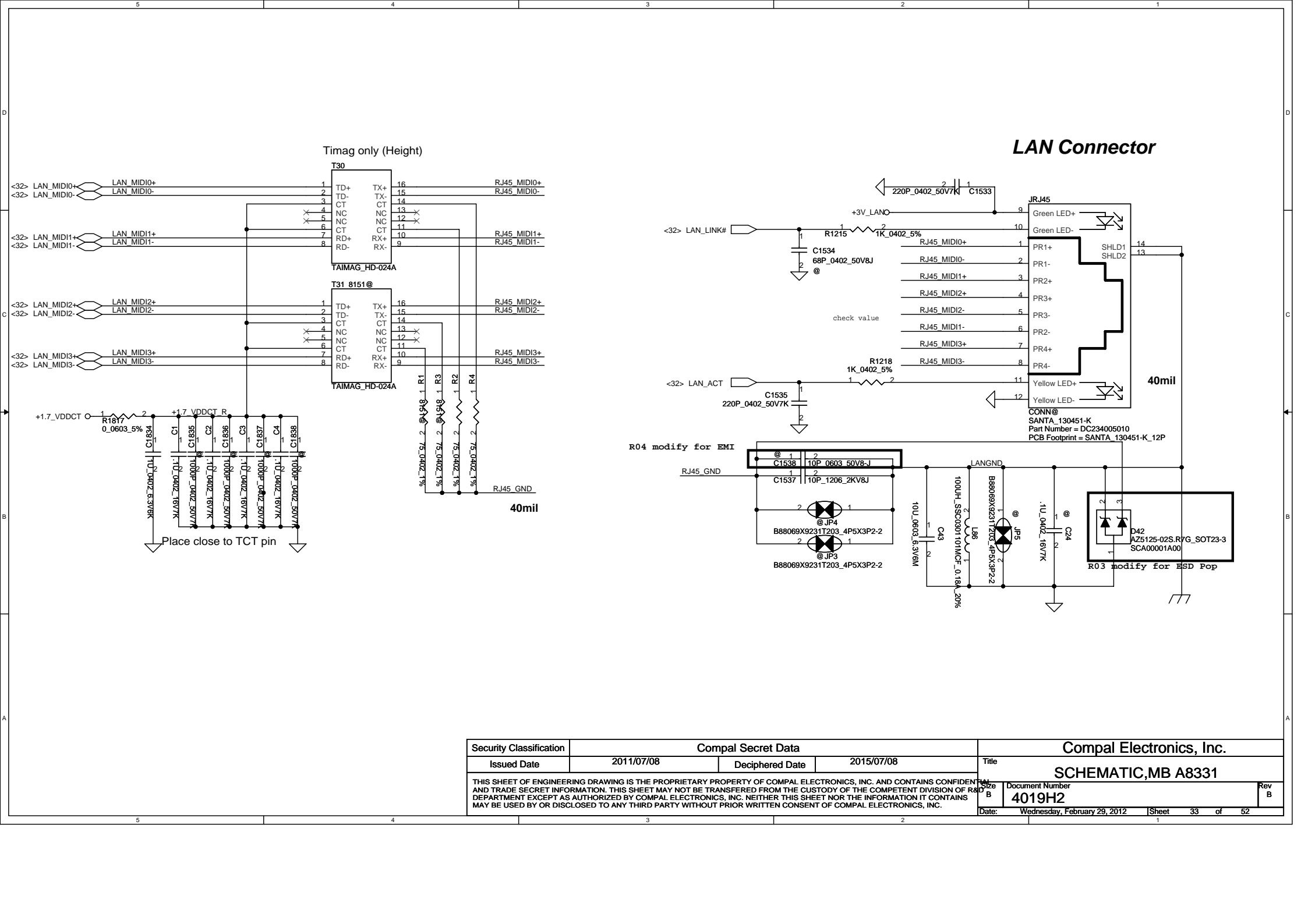
Pin9 Pin22 Near Pin16



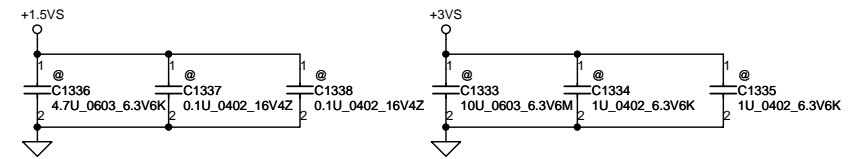
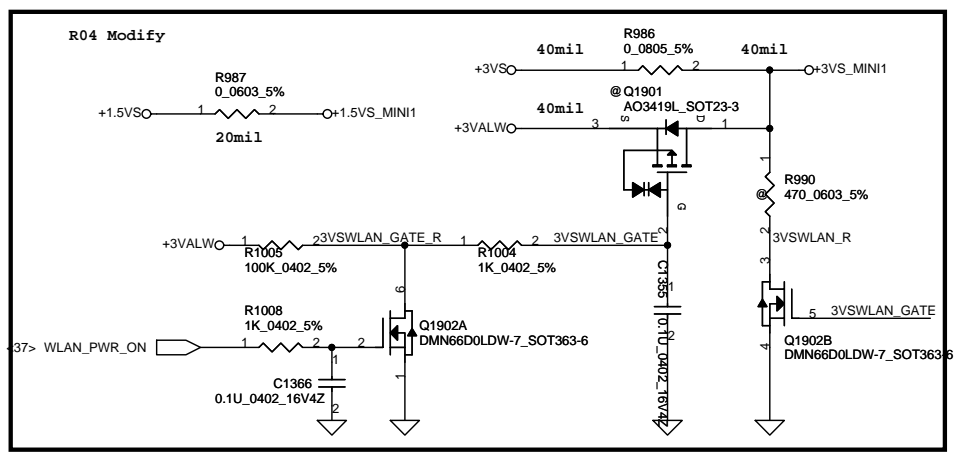
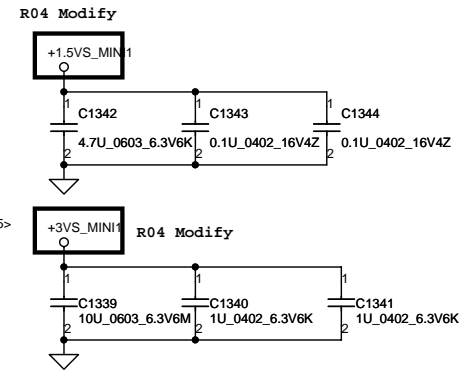
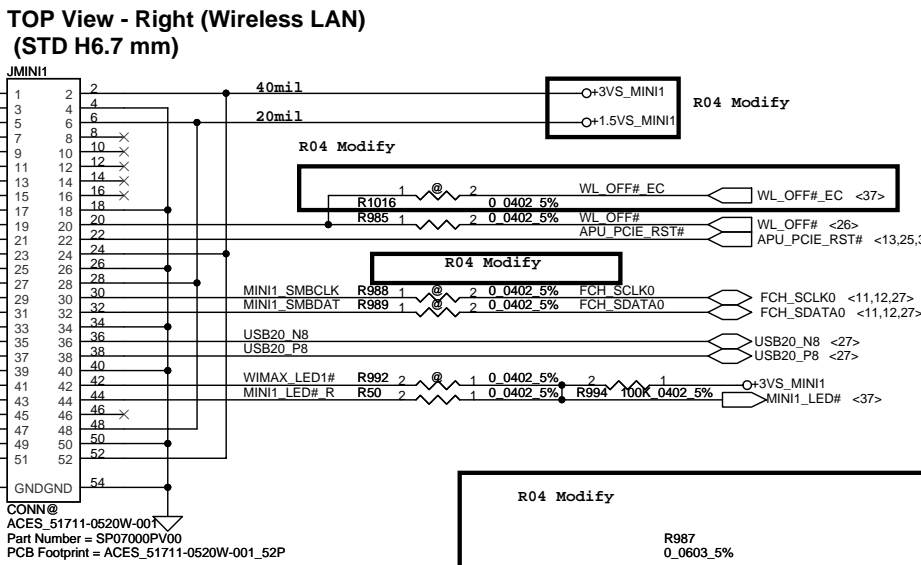
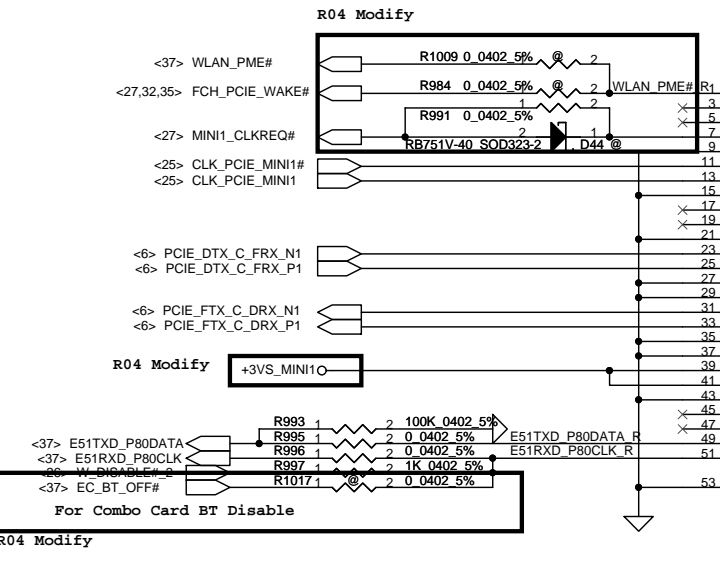
	Pin4	Configure		Pin23	Configure
		R1808	C1805		R1803
AR8152	VDDCT_REG		*	CLKREQn	*
AR8151	CLKREQn	*		LED[ 2 ]	

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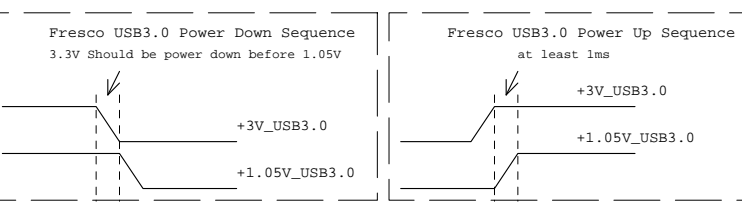
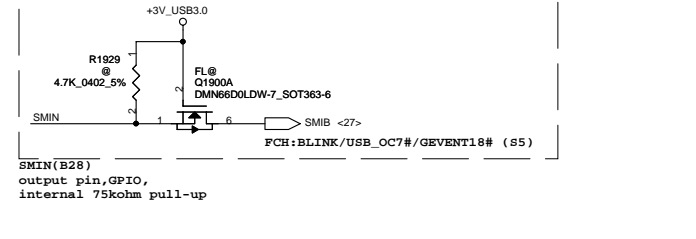
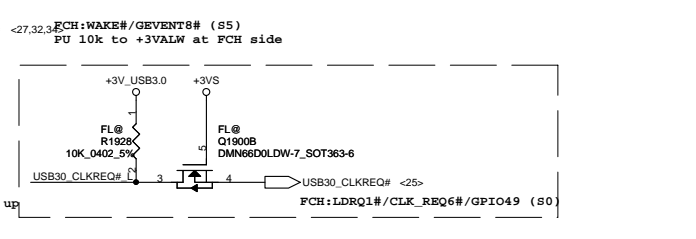
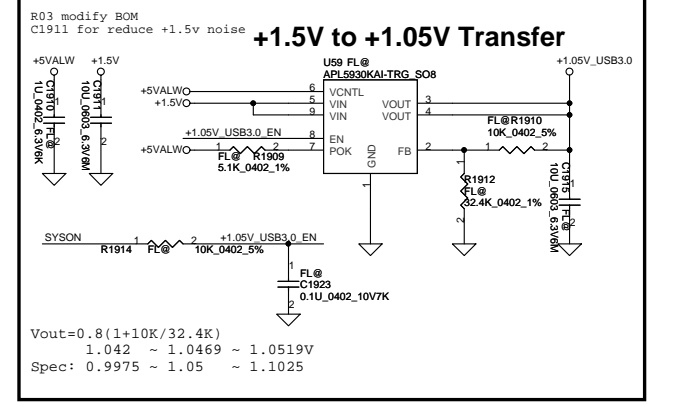
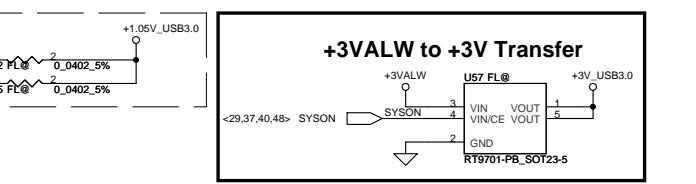
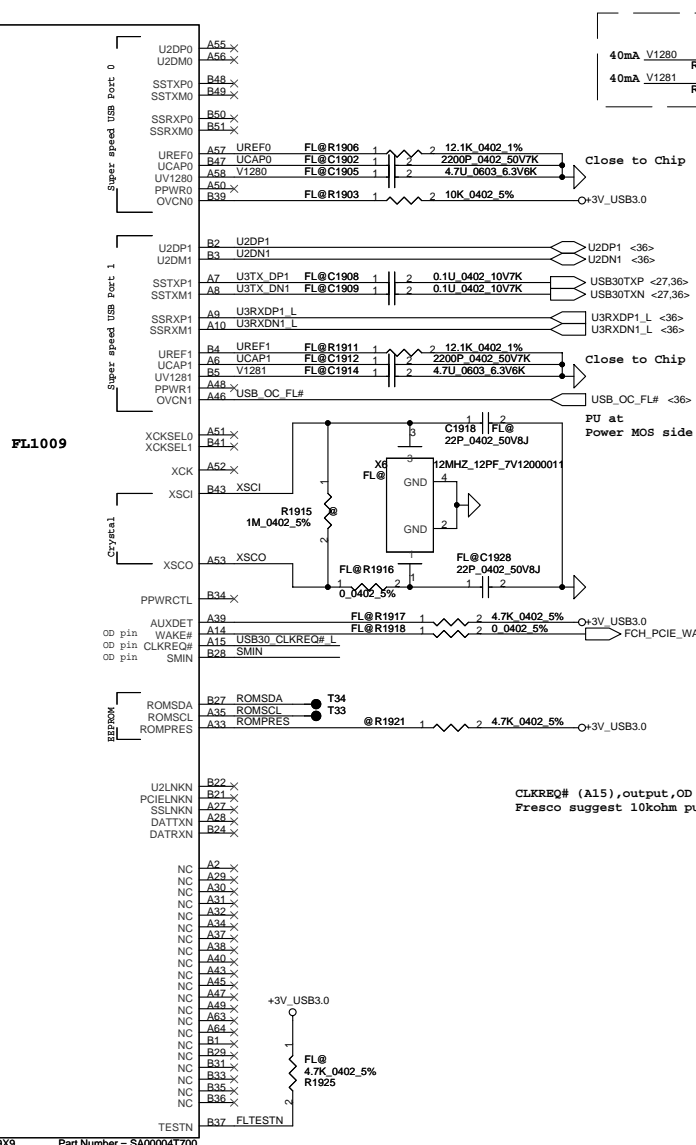
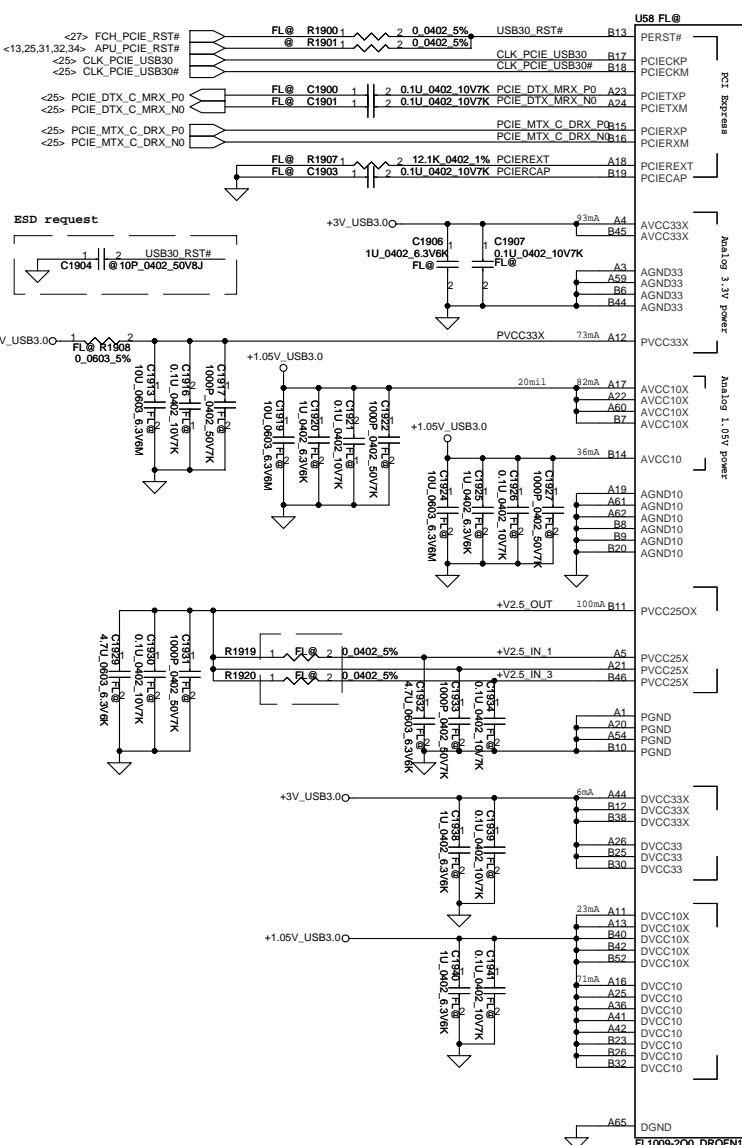




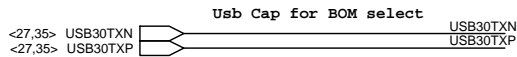
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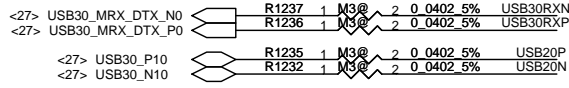
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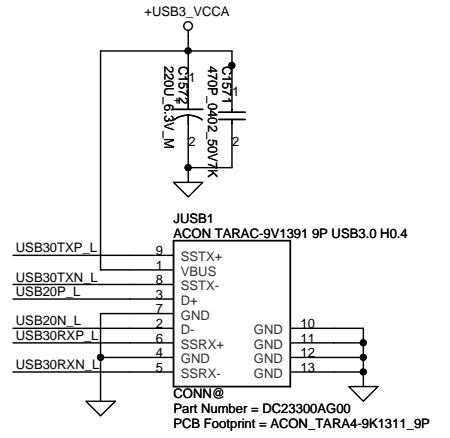
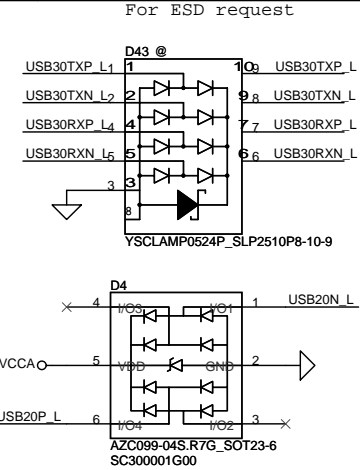
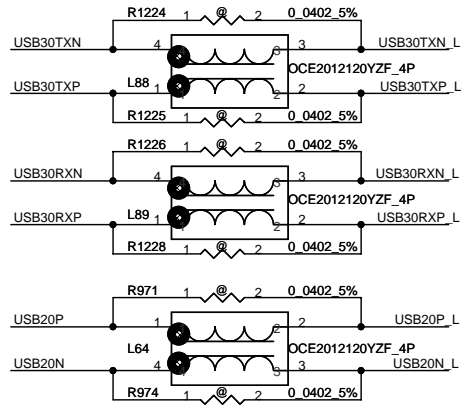
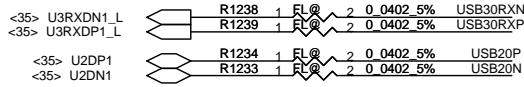
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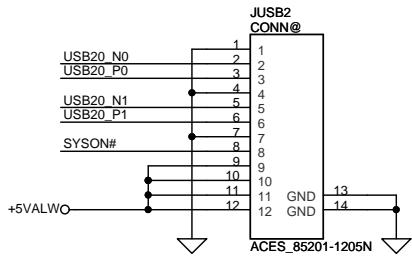
**From FCH**



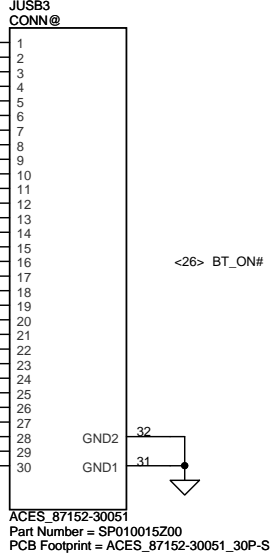
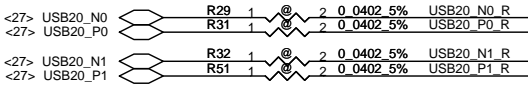
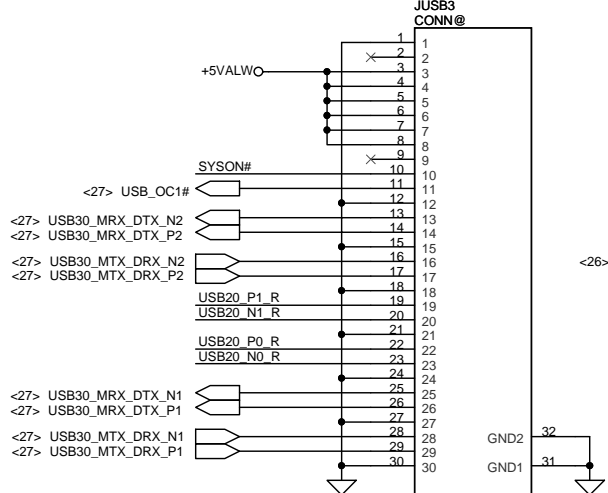
**From Fresco**



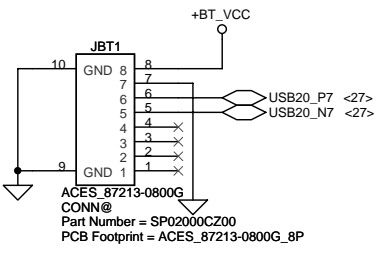
**12 Pin USB20/B Conn**



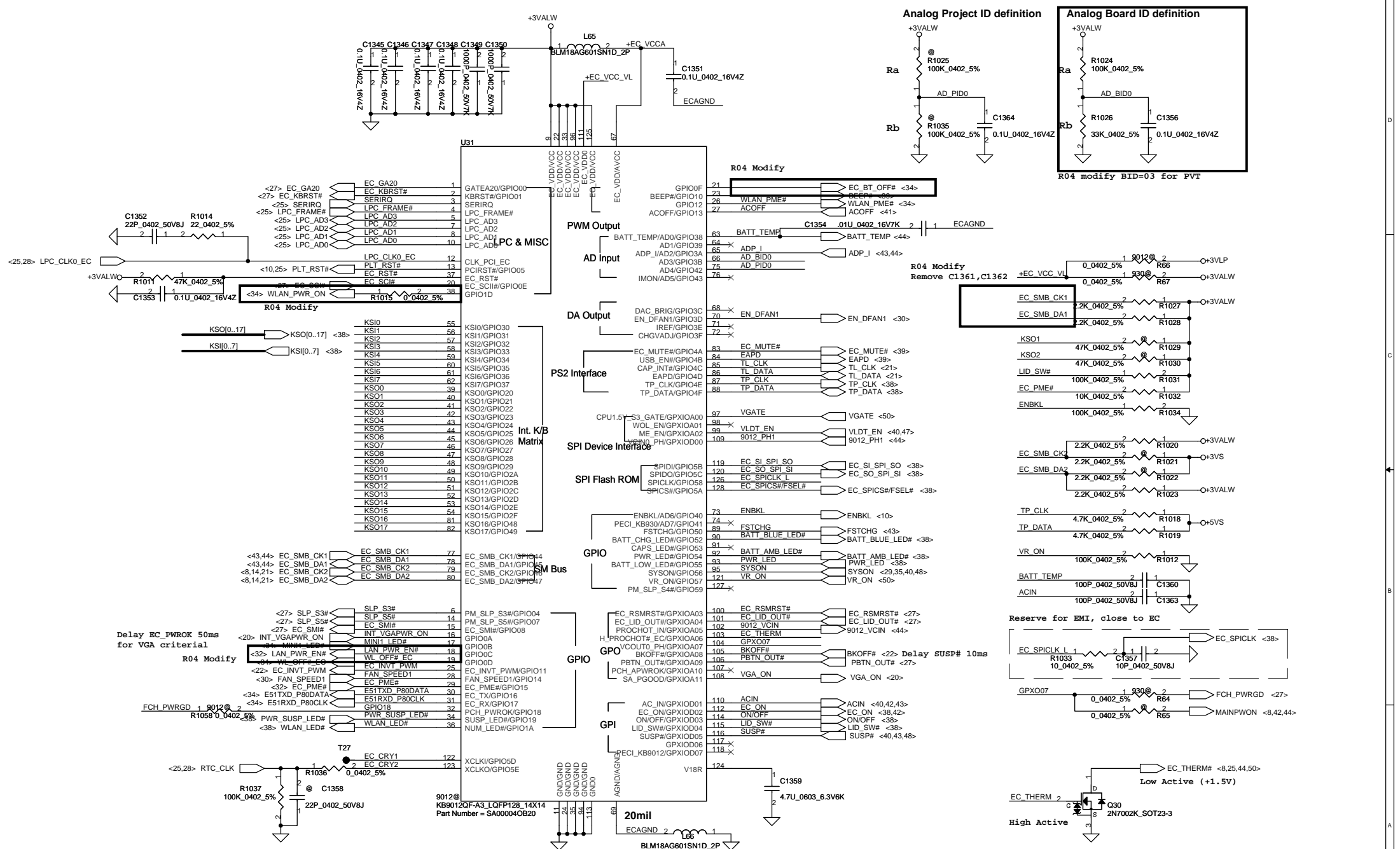
**30 Pin USB30/B Zif Conn.**



**Bluetooth Conn.**

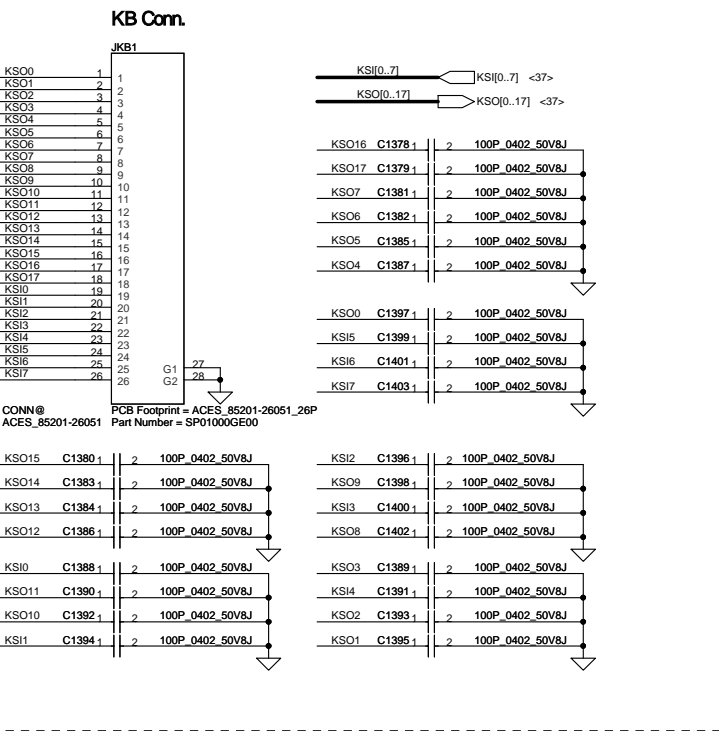
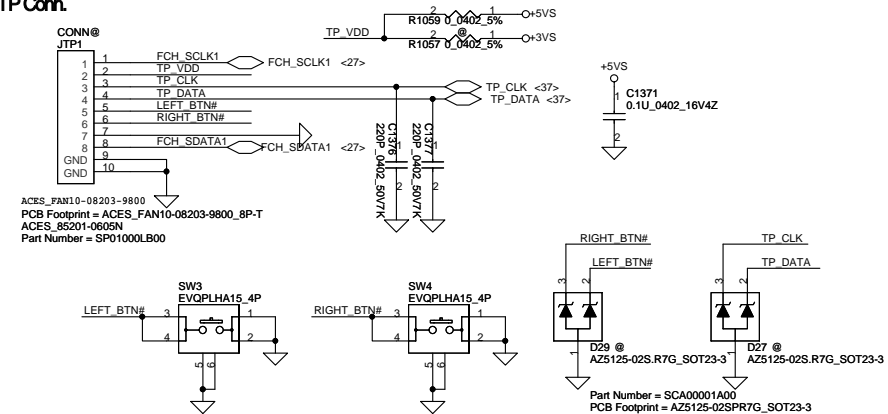
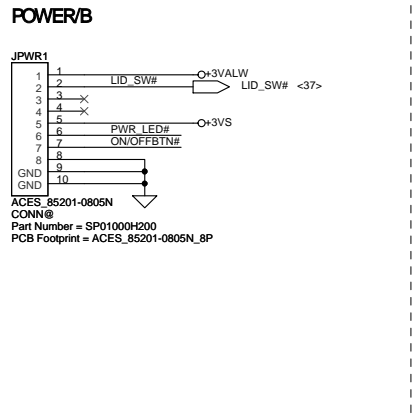
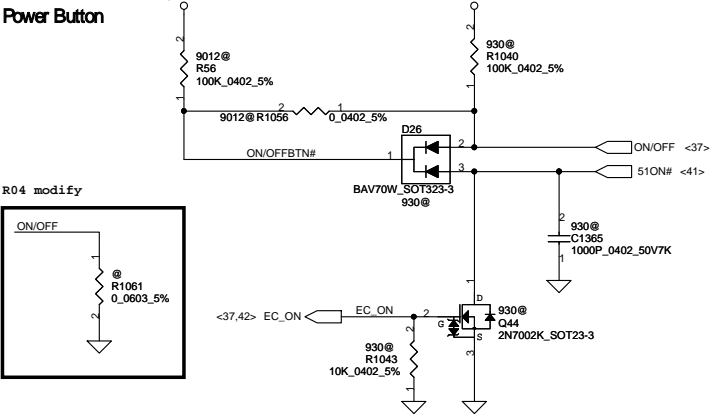


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Part Number = SP010015Z00 PCB Footprint = ACES_87152-30051_30P-S				Document Number
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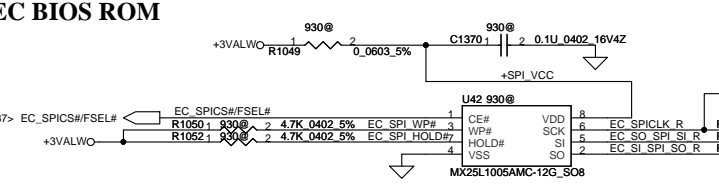
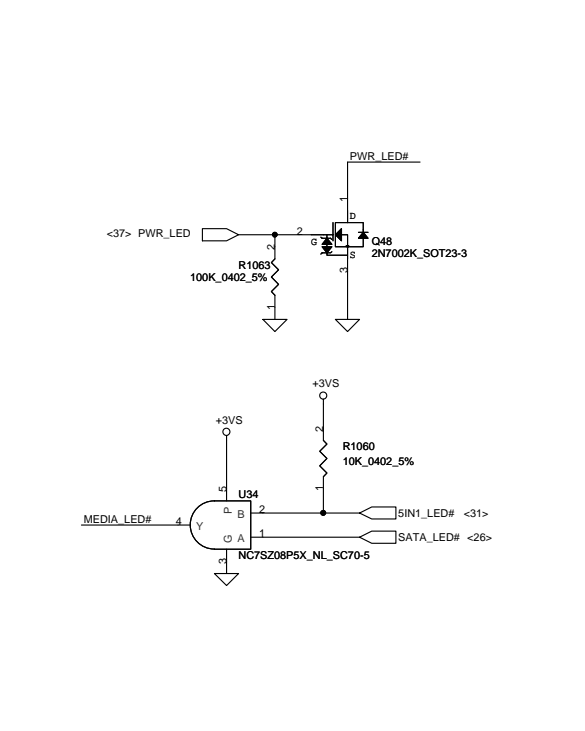
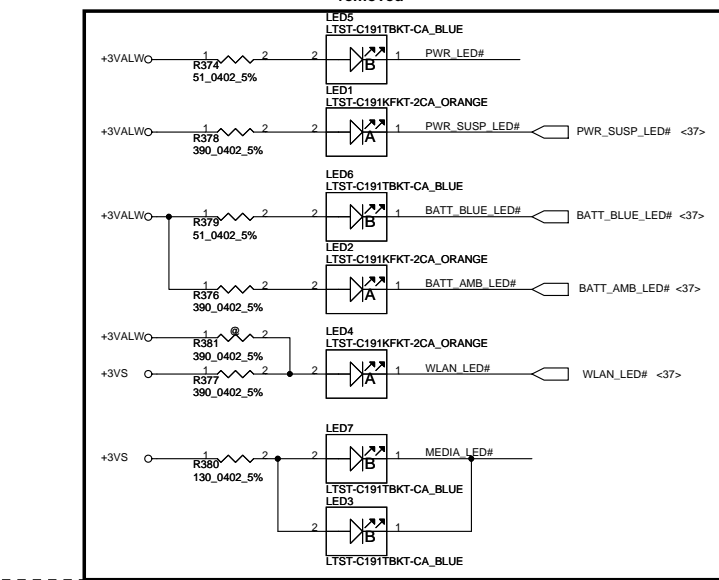
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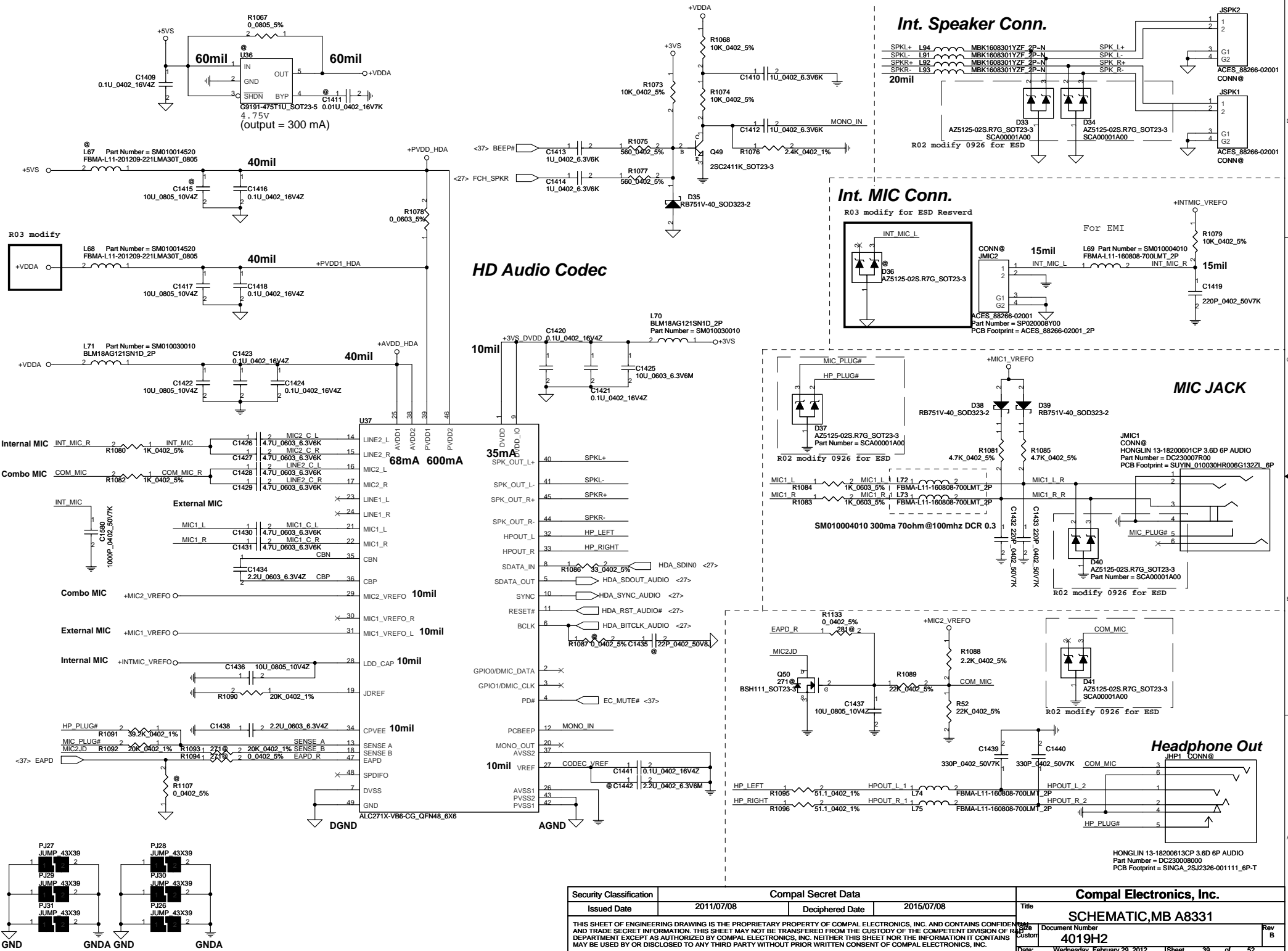
Document Number: 4019H2



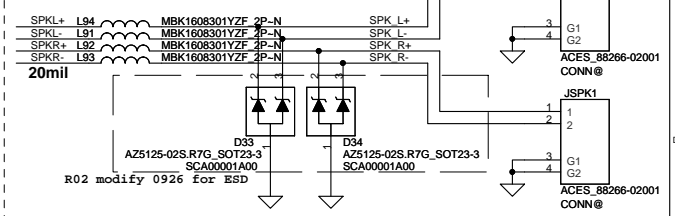
### LED

LED Status	Power/SUS		Battery		3G / WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber		Amber		

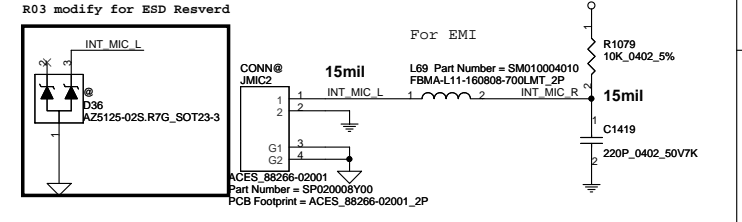




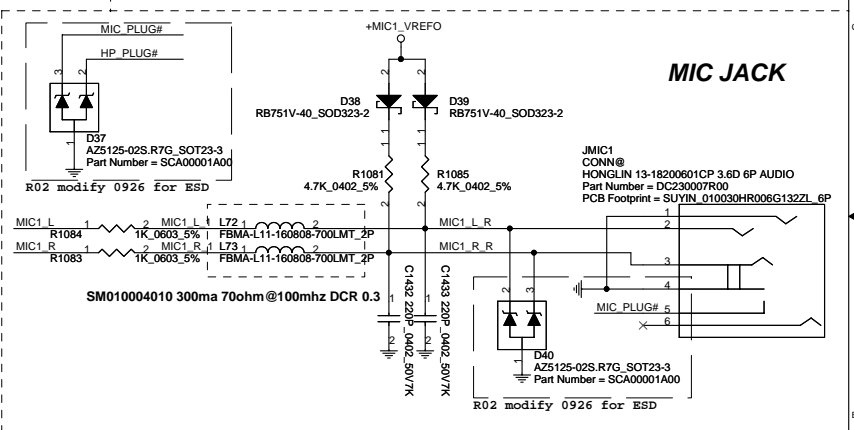
**Int. Speaker Conn.**



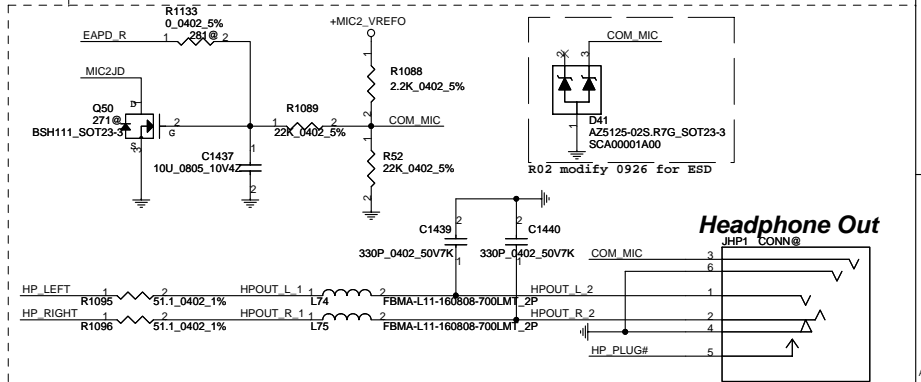
**Int. MIC Conn.**



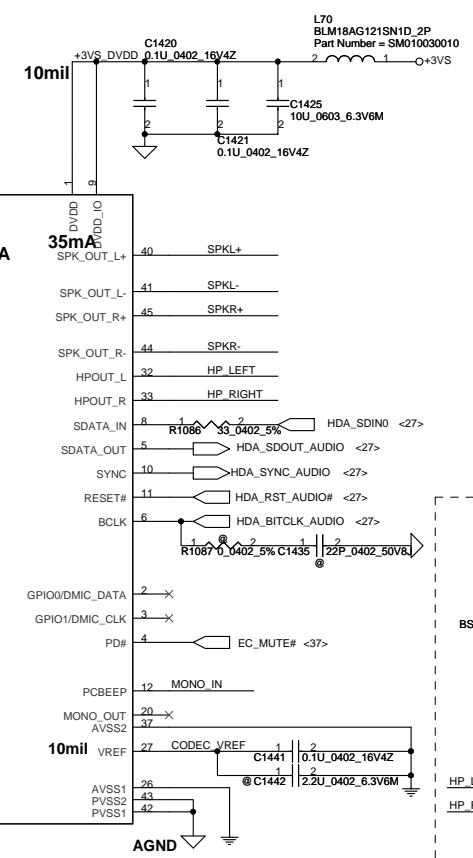
**MIC JACK**



**Headphone Out**



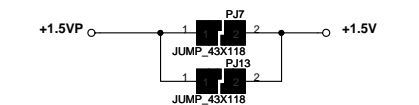
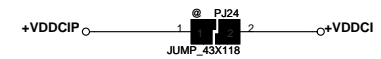
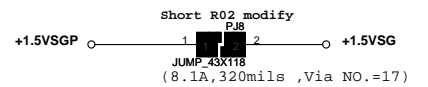
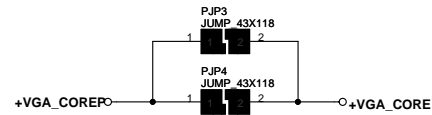
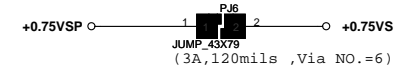
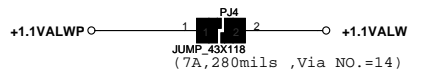
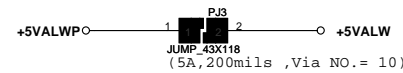
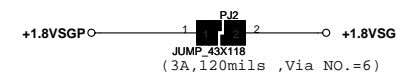
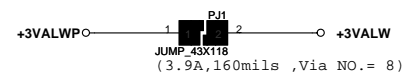
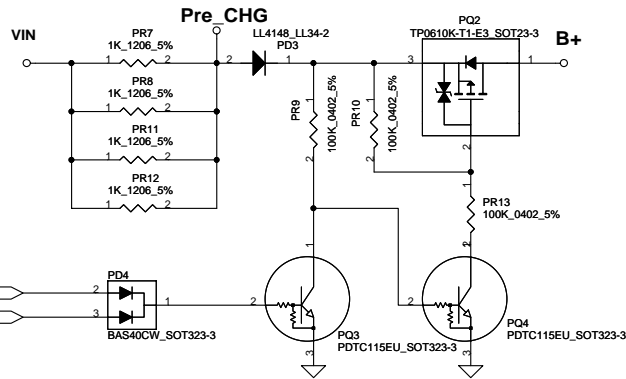
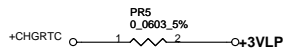
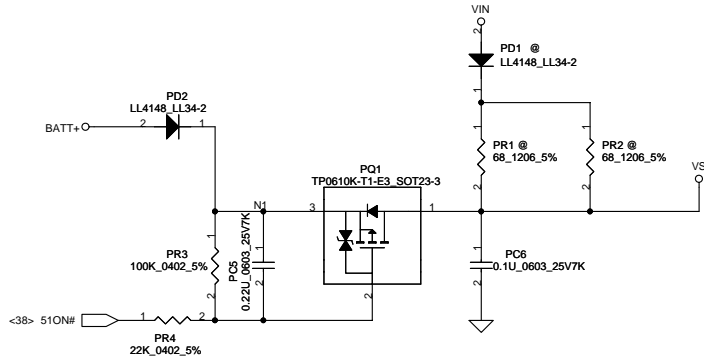
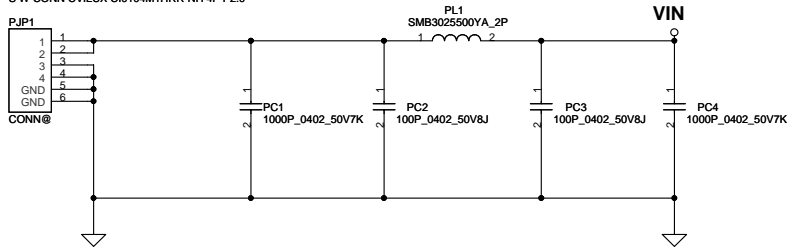
**HD Audio Codec**



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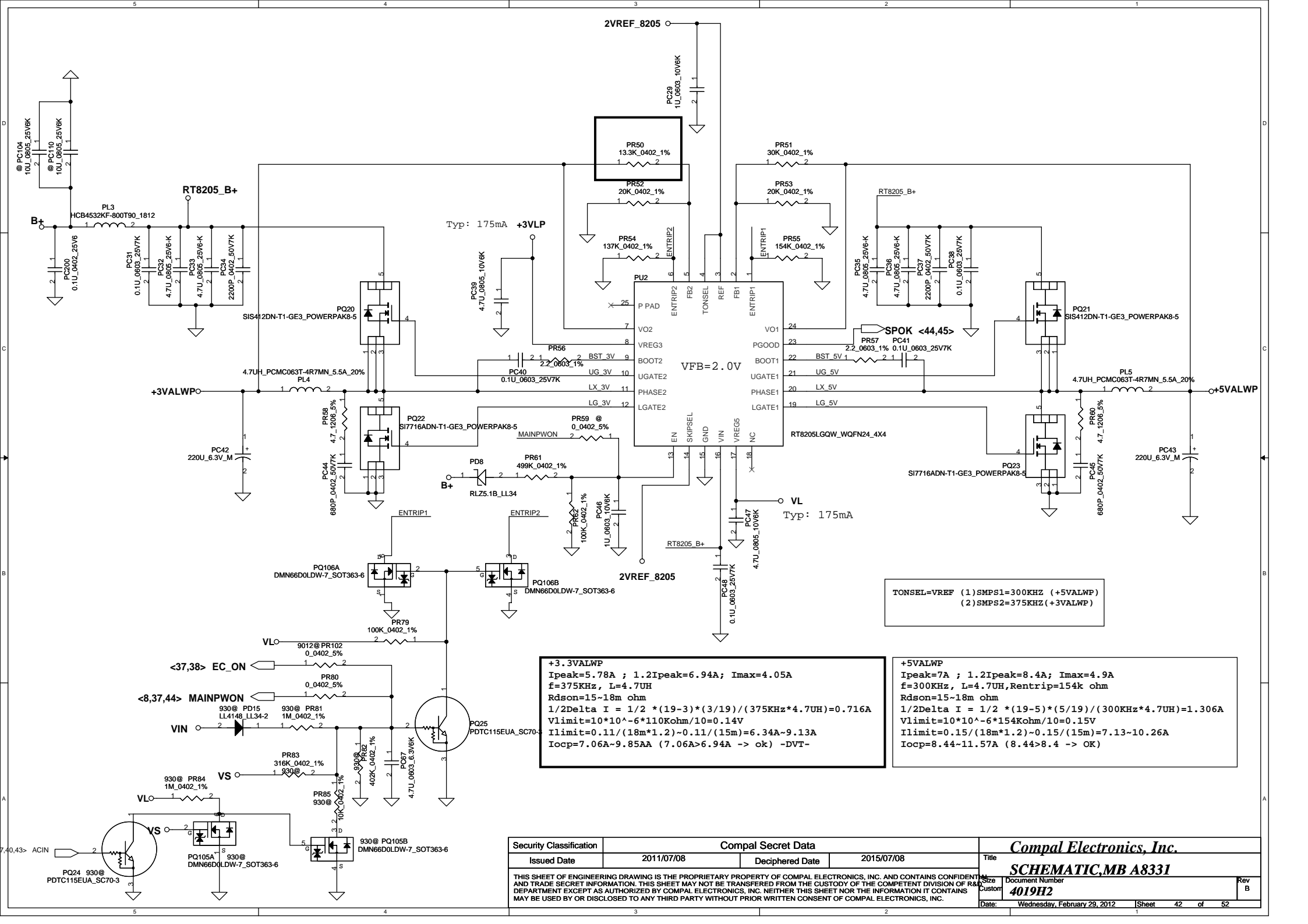






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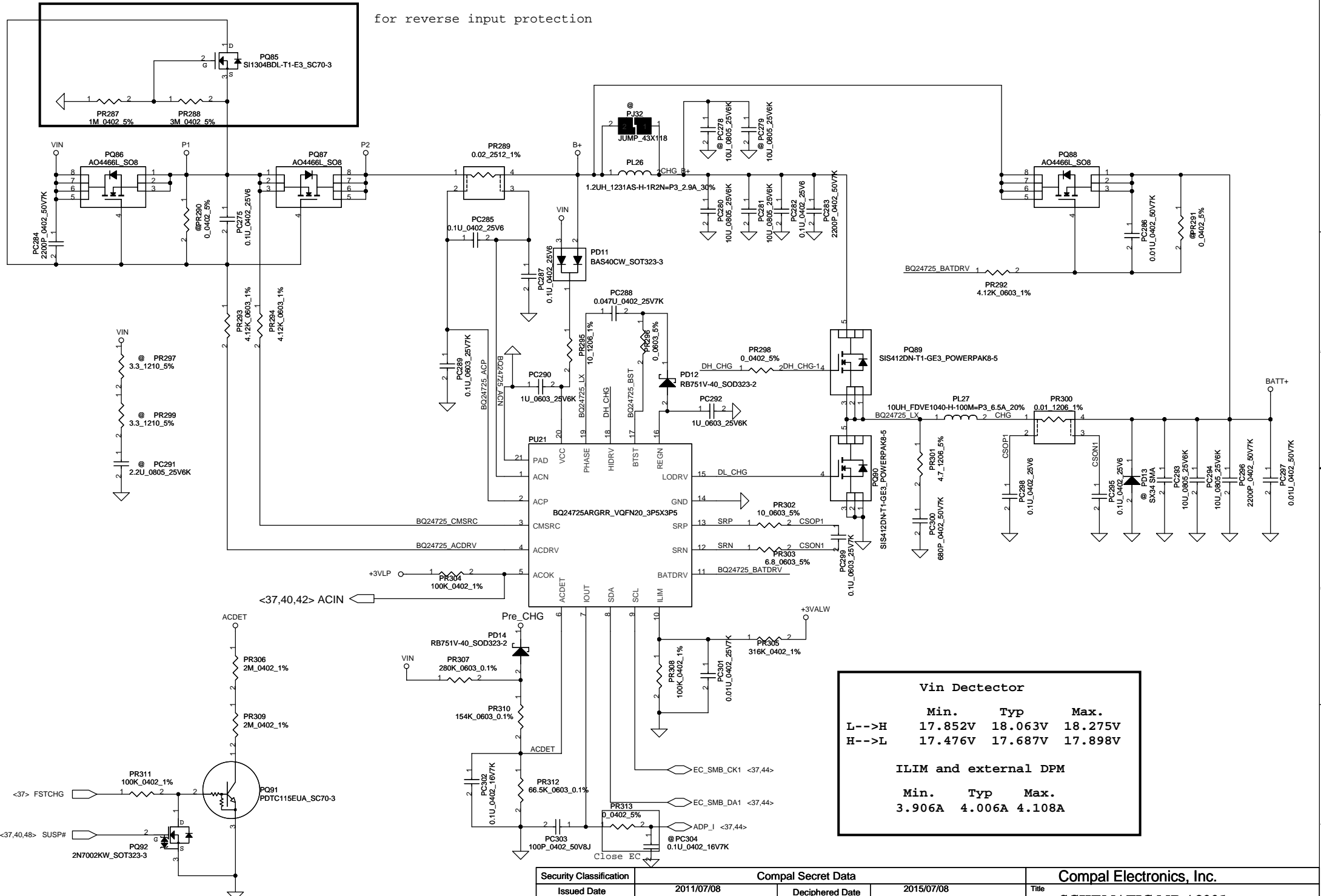
**+3.3VALWP**  
 Ipeak=5.78A ; 1.2Ipeak=6.94A; Imax=4.05A  
 f=375KHz, L=4.7UH  
 Rdsn=15~18m ohm  
 $1/2\Delta I = 1/2 * (19-3) * (3/19) / (375KHz * 4.7UH) = 0.716A$   
 $Vlimit = 10 * 10^{-6} * 110Kohm / 10 = 0.14V$   
 $Ilimit = 0.11 / (18m * 1.2) * 0.11 / (15m) = 6.34A \sim 9.13A$   
 $Iocp = 7.06A \sim 9.85A (7.06A > 6.94A \rightarrow ok) -DVT-$

**+5VALWP**  
 Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A  
 f=300KHz, L=4.7UH, Rentrip=154k ohm  
 Rdsn=15~18m ohm  
 $1/2\Delta I = 1/2 * (19-5) * (5/19) / (300KHz * 4.7UH) = 1.306A$   
 $Vlimit = 10 * 10^{-6} * 154Kohm / 10 = 0.15V$   
 $Ilimit = 0.15 / (18m * 1.2) * 0.15 / (15m) = 7.13 \sim 10.26A$   
 $Iocp = 8.44 \sim 11.57A (8.44 > 8.4 \rightarrow OK)$

TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)  
 (2) SMPS2=375KHZ (+3VALWP)

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for reverse input protection



Vin Detector			
	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

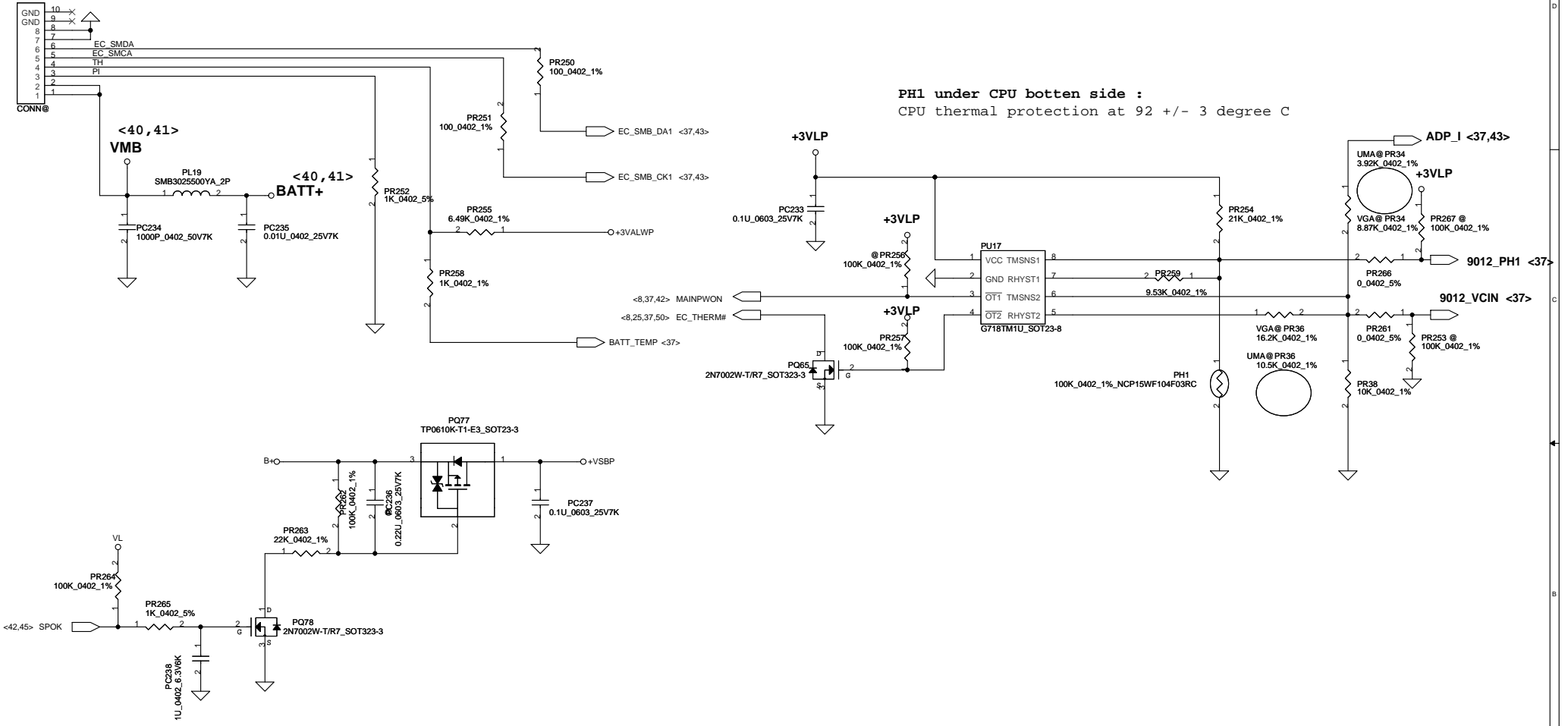
  

ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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Part Number = DC040008G00  
 PCB Footprint = SUYIN\_200275GR008G13GZR\_8P-T

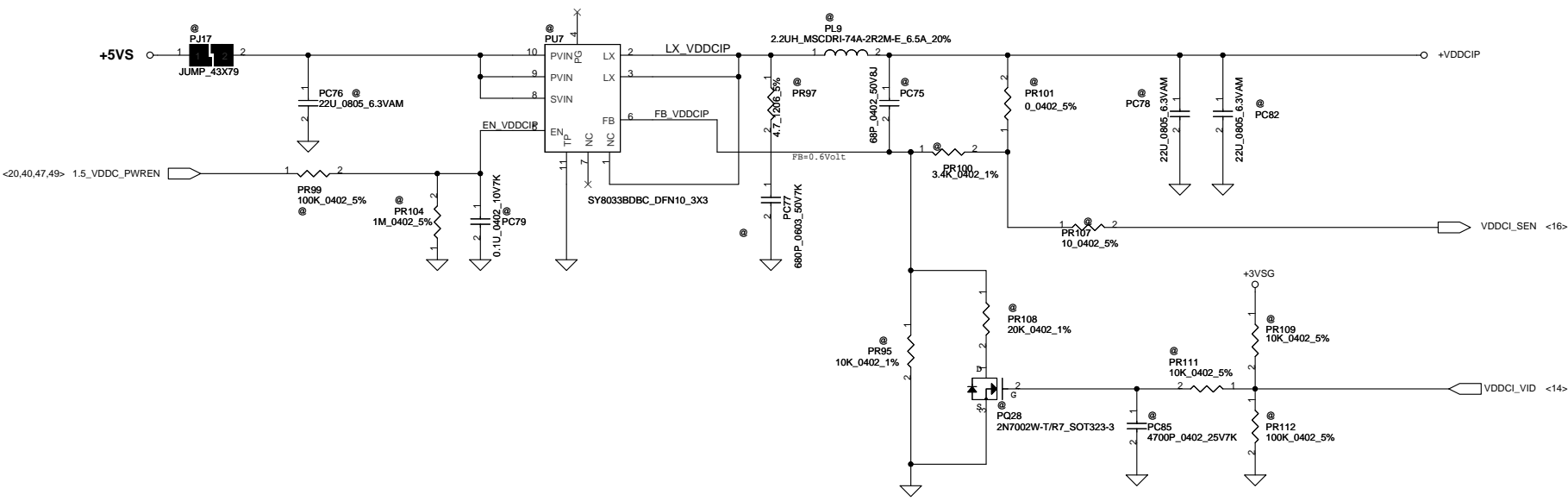
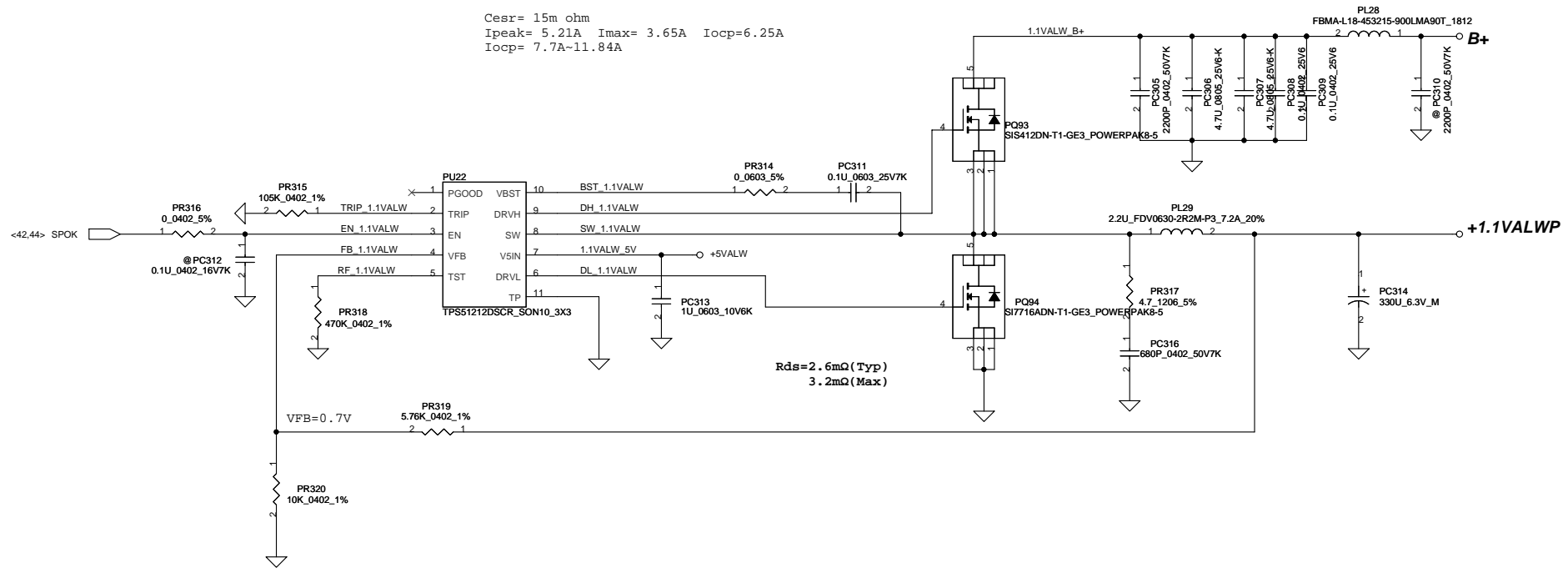
PJP2  
 SUYIN\_200275GR008G16BZR 8P



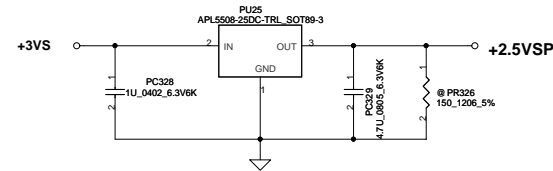
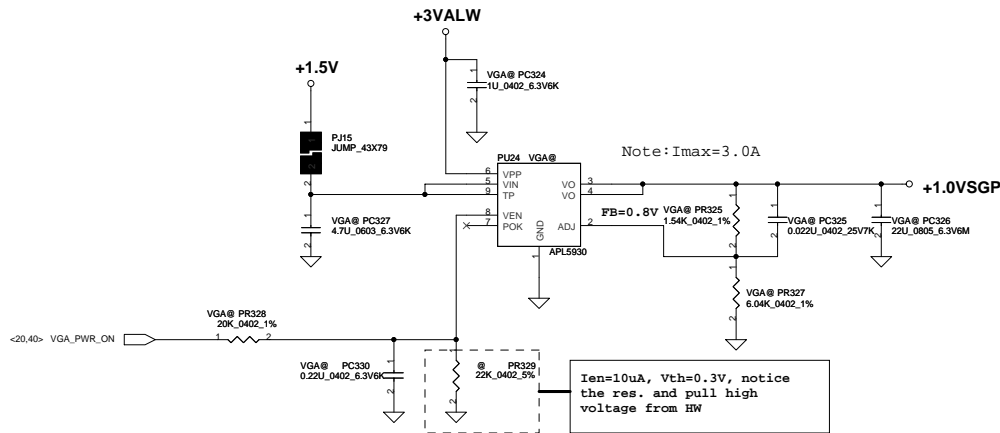
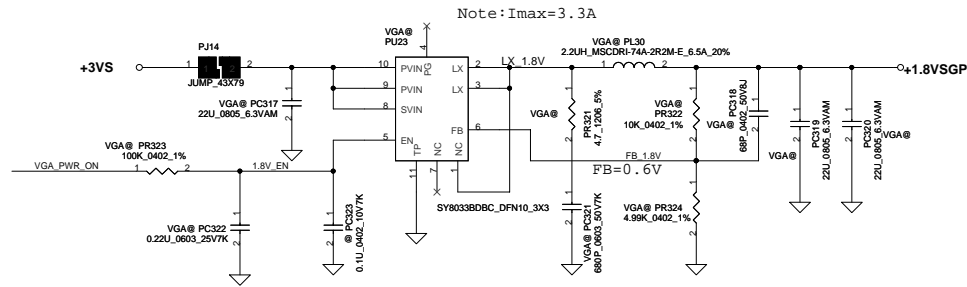
PH1 under CPU bottom side :  
 CPU thermal protection at 92 +/- 3 degree C

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VFB= 0.7V  
 $V_0 = V_{FB} * (1 + 5.76K / 10K) = 1.1V$   
 Freq= 266-314KHz , 290KHz(typ)  
 Cesr= 15m ohm  
 Ipeak= 5.21A I<sub>max</sub>= 3.65A I<sub>ocp</sub>=6.25A  
 Iocp= 7.7A-11.84A



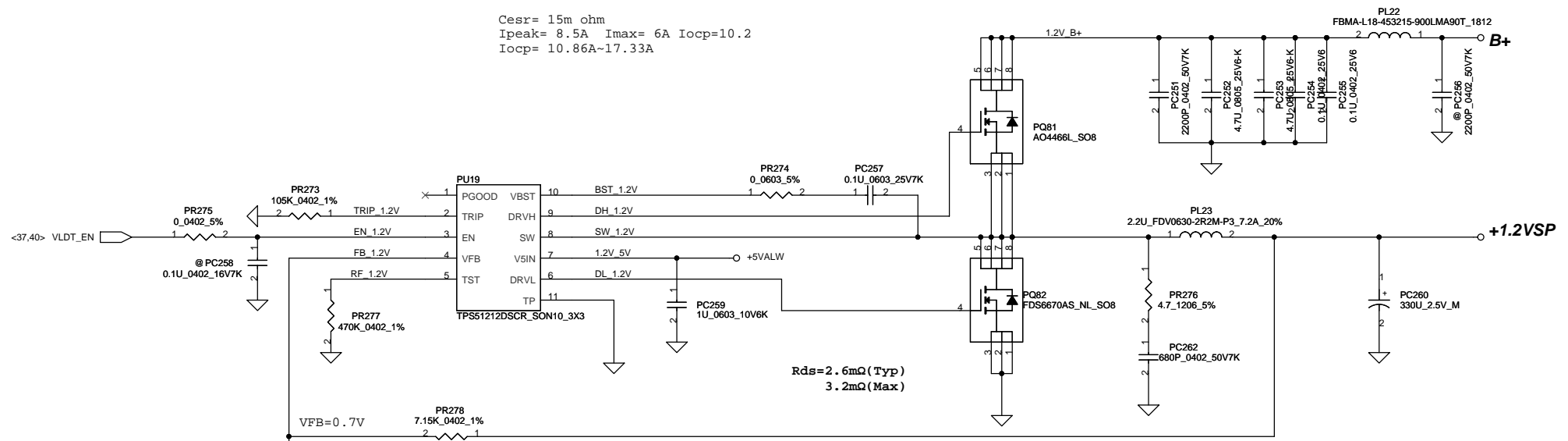
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VFB= 0.7V  
 $V_o = VFB * (1 + 7.15K/10K) = 1.2V$   
 Freq= 266~314KHz , 290KHz(typ)

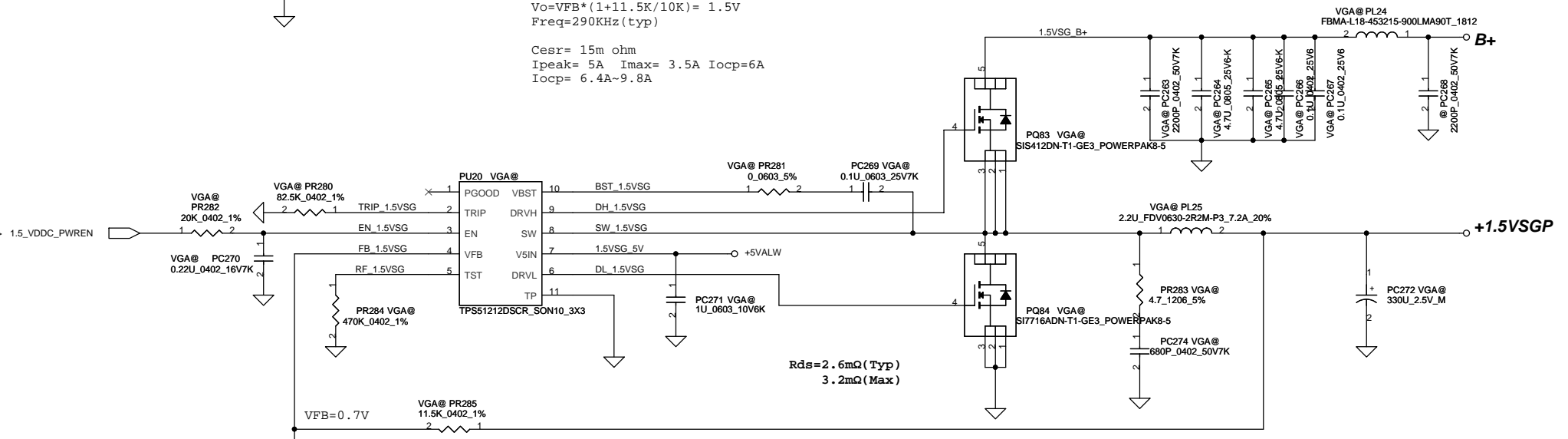
Cesr= 15m ohm  
 $I_{peak} = 8.5A$   $I_{max} = 6A$   $I_{ocp} = 10.2$   
 $I_{ocp} = 10.86A \sim 17.33A$



$R_{ds} = 2.6m\Omega$  (Typ)  
 $3.2m\Omega$  (Max)

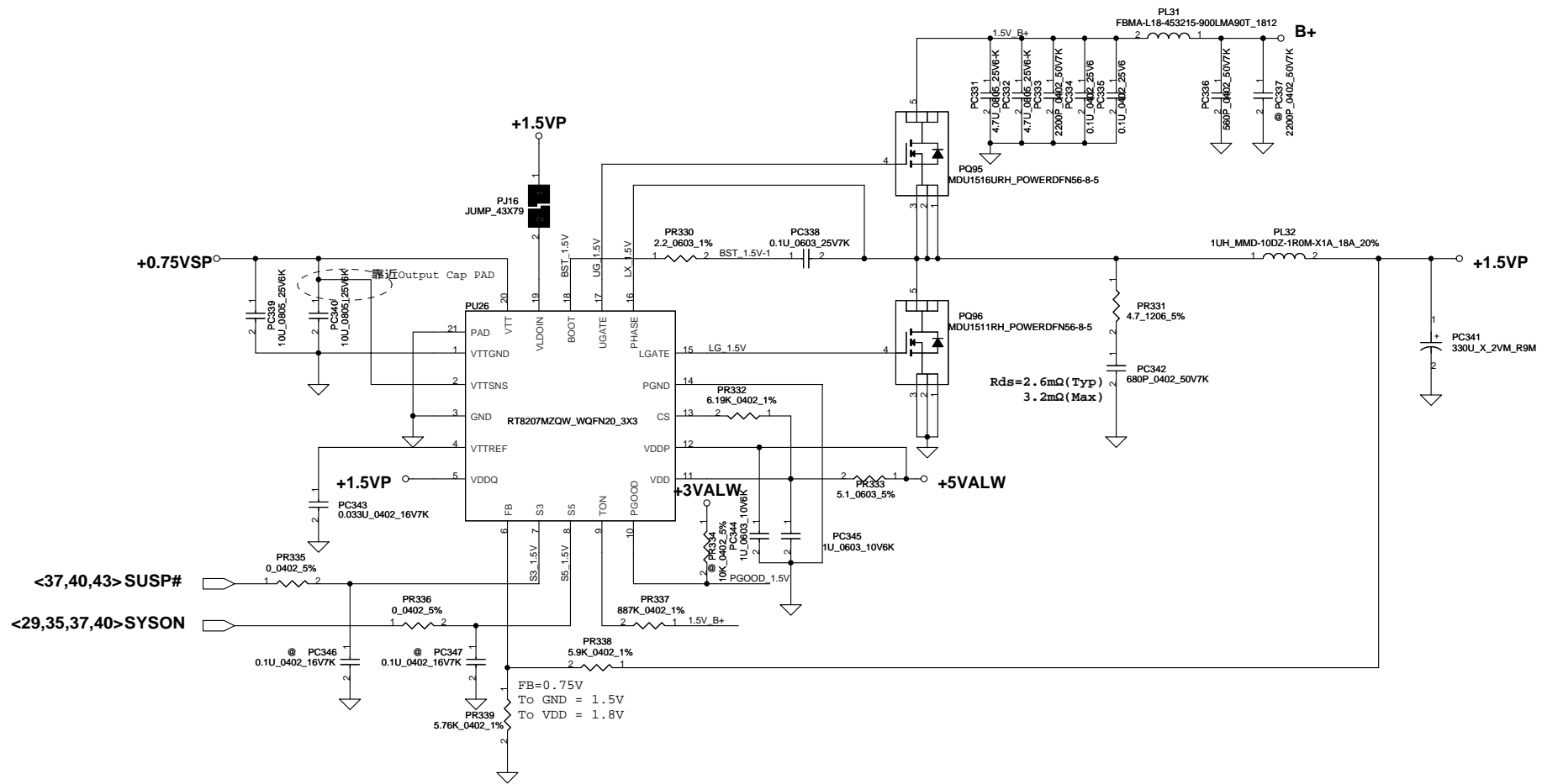
VFB= 0.704V  
 $V_o = VFB * (1 + 11.5K/10K) = 1.5V$   
 Freq=290KHz (typ)

Cesr= 15m ohm  
 $I_{peak} = 5A$   $I_{max} = 3.5A$   $I_{ocp} = 6A$   
 $I_{ocp} = 6.4A \sim 9.8A$



$R_{ds} = 2.6m\Omega$  (Typ)  
 $3.2m\Omega$  (Max)

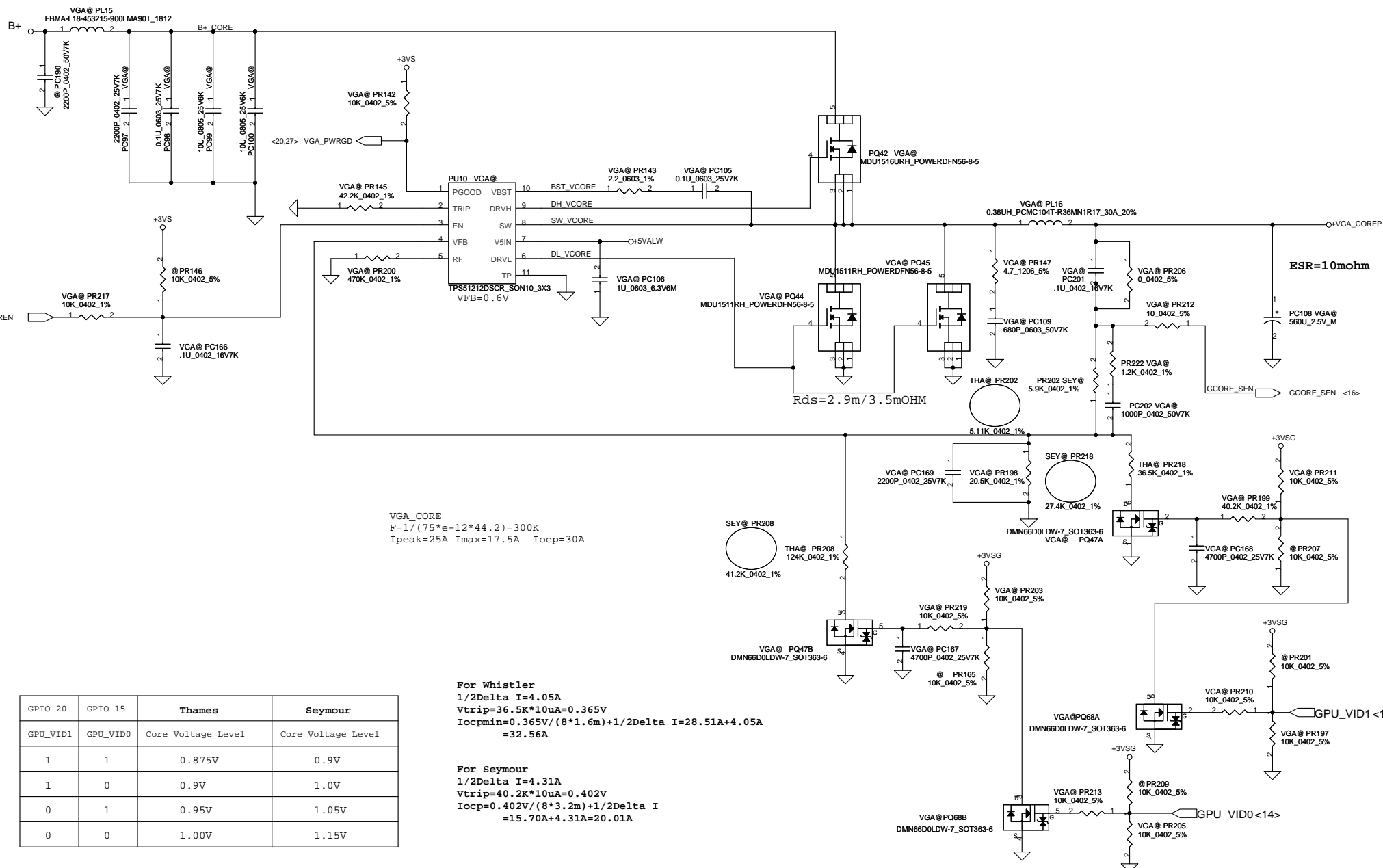
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VFB= 0.75V  
 Ipeak= 15A I<sub>max</sub>= 10.5A I<sub>ocp</sub>=18A  
 I<sub>ocp</sub>= 17.24A~25.47A

STATE	S3	S5	1.5VP	0.75VSP
S0	Hi	Hi	On	On
S3	Lo	Hi	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off				





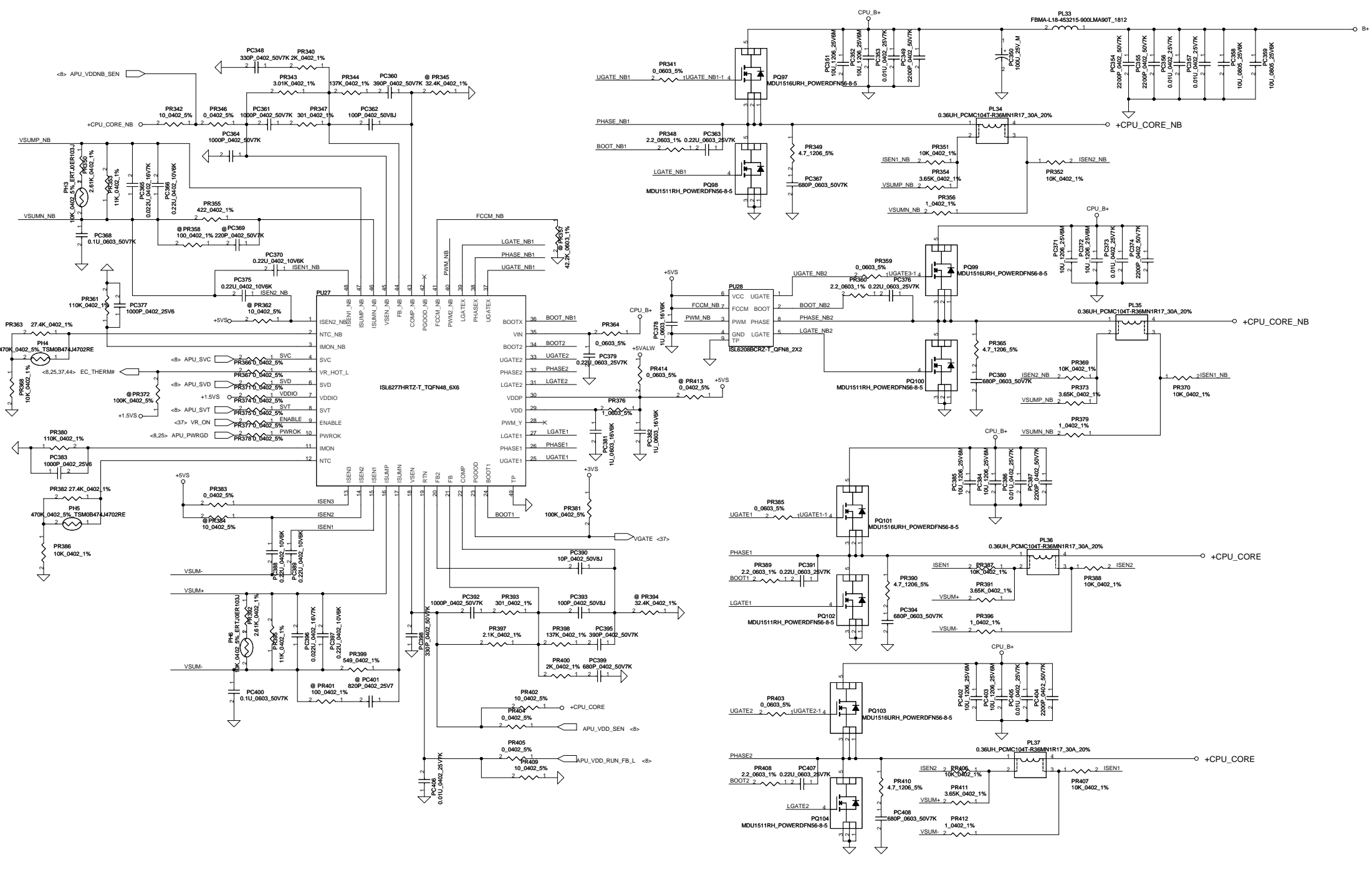
VGA\_CORE  
 $F=1/(75 \times e^{-12 \times 44.2})=300K$   
 $I_{peak}=25A$   $I_{max}=17.5A$   $I_{ocp}=30A$

For Whistler  
 $1/2\Delta I=4.05A$   
 $V_{trip}=36.5K \times 10\mu A=0.365V$   
 $I_{ocpmin}=0.365V/(8 \times 1.6m)+1/2\Delta I=28.51A+4.05A=32.56A$

For Seymour  
 $1/2\Delta I=4.31A$   
 $V_{trip}=40.2K \times 10\mu A=0.402V$   
 $I_{ocp}=0.402V/(8 \times 3.2m)+1/2\Delta I=15.70A+4.31A=20.01A$

GPIO 20	GPIO 15	Thames	Seymour
GPU_VID1	GPU_VID0	Core Voltage Level	Core Voltage Level
1	1	0.875V	0.9V
1	0	0.9V	1.0V
0	1	0.95V	1.05V
0	0	1.00V	1.15V

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
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# Version change list (P.I.R. List)

## EVT Stage (0.1~0.2)

- 0817 Pop C1025 180p for VDDIO (SCL v1.02)  
Change D16,D17 to SCS00000Z00
- 0818 Change Q50 from BSH138 to BSH111  
Unpop R1100 for +1.1VALW  
Add D26 BOM Structure for 930@  
unpop D4 for USB issue
- 0903 1.Change Card Reader Controller to RTS5209  
2.Change LAN to Atheros AR8151  
3.Removed D17
- 0904 Add Mini2 Debug Port
- 0905 1.Add Fresco FL1009 USB3.0 Controller  
P20. BACO BIFVDDC update  
P25. remove Q25 APU power ok
- 0915 1.Remove EC X2
- 0916 1.Add C1361/C1362 10pF for EMI  
2.Change D27/D29 footprint to AZ5125  
3.Add R402 10k for reserved  
4.Add R469/R527 for VGA Internal Thermal Senser
- 0926 1.Change D4 to SC300001G00 for ESD request  
2.Change D33/D34/D37/D40/D41 to SCA00001A00 for ESD request

## DVT Stage (0.2~0.3)

- 1.Unpop C954, C955 for Mini2 reserved.
- 2.Remove R587, R588, Q11 for no need level shift.
- 3.Pop R469, R527  
Unpop U9, R391, C352, C324  
for VGA Internal Thermal Interface.
- 4.Unpop C374 330uF for Use discrete +1.5VSG circuit.
- 5.Add R1169 1k for RTS2132 Vender suggestion.
- 6.Reserved R1177 for option EEPROM.
- 7.Add R1178 for RTS2132 discrete +1.2VS power.
- 8.Reserved SMBUS(TL\_CLK/TL\_DATA) to EC for EEPROM option.
- 9.Reserved BACO circuit and pop C1105.
- 10.Change D4, D6 to AZC099 for ESD reserved.
- 11.Change D20, D21 to AZC199-02SPR7G for ESD reserved.
- 12.Remove D44, D45 for no need.
- 13.Change C1211, R837 BOM to TL@.
- 14.Change JTP1 to 6P/8P co-lay footprint for WIN8.
- 15.Add SMBUS(FCH\_SCLK1/FCH\_SDAT1) for JTP1.
- 16.Reserved GPIO166 for future used.
- 17.Add H29 for ME update.
- 18.Add C1719, C1720 10pF for RTD5209 EMI request.
- 19.Change L1801 footprint.
- 20.Pop D42 and change to SCA00001A00 for ESD.
- 21.Change C1537 to 10pF 2KV for EMI/ESD.
- 22.Unpop C1336, C1337, C1338, C1333, C1334, C1335  
for MINI2 Reserved.
- 23.Modify C1911 always pop for noise reduce.
- 24.Modify R60 to M3@.
- 25.Change Board ID to "02" for DVT.
- 26.Add Q30 for EC\_THERM reverse for EC common code.
- 27.Change 9012\_PH2 netname to 9012\_VCIN for VC function.
- 28.Unpop R65 for External OTP.
- 29.Change L68 +5VS to +VDDA.
- 30.Chnage R1124 to 200k, R1130 to 10k for VGA Power Sequence.
- 31.Pop R997 for W/L BT combo card BT ON/OFF
- 32.Change U28 SPI ROM from MXIC to EON

## PVT Stage

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