

Compal Confidential

HBL50 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M
(With nVIDIA G73M/G72MV/NB7P-SE)

2006-10-04

REV: 4.0

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File Name : LA-2921

Fan Control
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uPGA-478 Package
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Thermal Sensor
F75383M
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Clock Generator
ICS9LPRS325
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CH7307C page 25
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DVI
CRT & TV-out page 24
LVDS
SDVO

PSB
533/667MHz
H_A#(3..31) H_D#(0..63)

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uFCBGA-1466
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Memory BUS(DDRII)
Dual Channel
1.8V DDRII 400/533

200pin DDRII-SO-DIMM X2
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nVidia G73M/(72M)/72MV
with 64/128/256MB VRAM
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MINI CARD x2
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USB conn x4
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Intel ICH7-M
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PCI Express

3.3V 48MHz

USB port 1

USB port 3, 7

USB port 0, 2

USB port 5

IDSEL:AU16
(PIRQ#1,
GNT#2,
REQ#2)

IDSEL:AU18
(PIRQ#1#,
GNT#3,
REQ#3)

IDSEL:AU17
(PIRQ#3,
GNT#3,
REQ#3)

IDSEL:AU20
(PIRQ#4,
GNT#2,
REQ#2)

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Mini PCI
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(WLAN)
(TV-Tuner)
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BCM4401E
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RJ45
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CardBus
ENE CB714
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Slot 0
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6 in 1
socket
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3.3V 48MHz

USB port 1

3.3V 24.576MHz/48MHz

3.3V ATA-100

IDE

S-ATA

port 0
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port 0
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Power On/Off CKT.
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DC/DC Interface CKT.
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MEDIA/B Conn.
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Touch Pad
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Int.KBD
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EC I/O Buffer
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BIOS
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CIR
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Super I/O
SMsC LPC47N207
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FIR
TFDU6102-TR3
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TPM1.2
SLB9635 TT 1.2
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

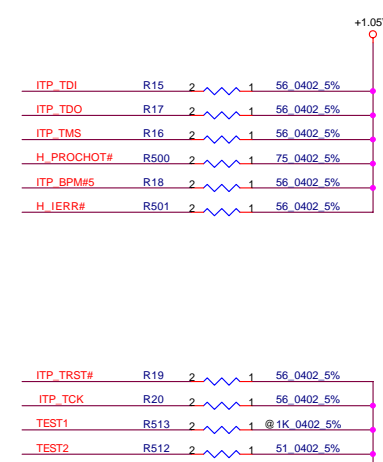
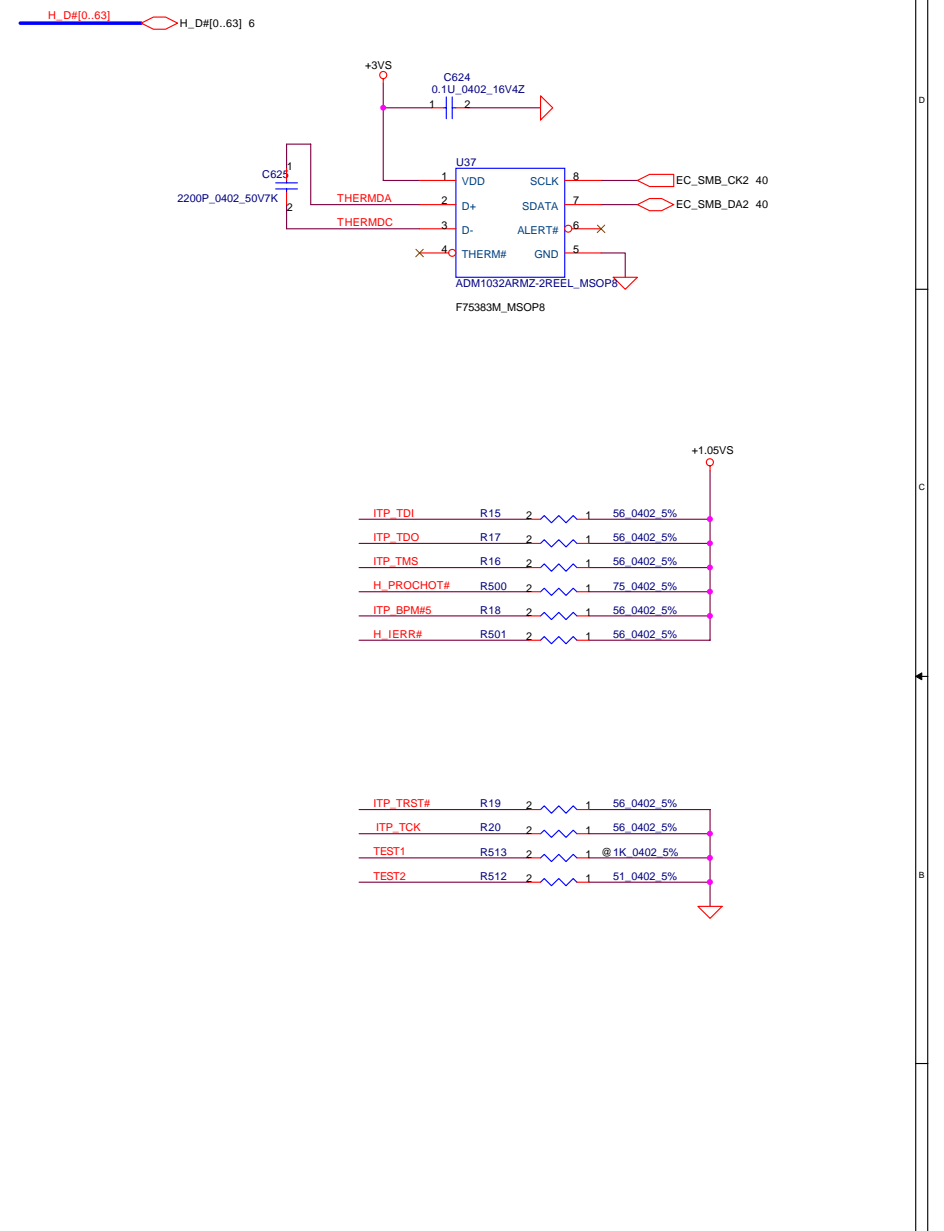
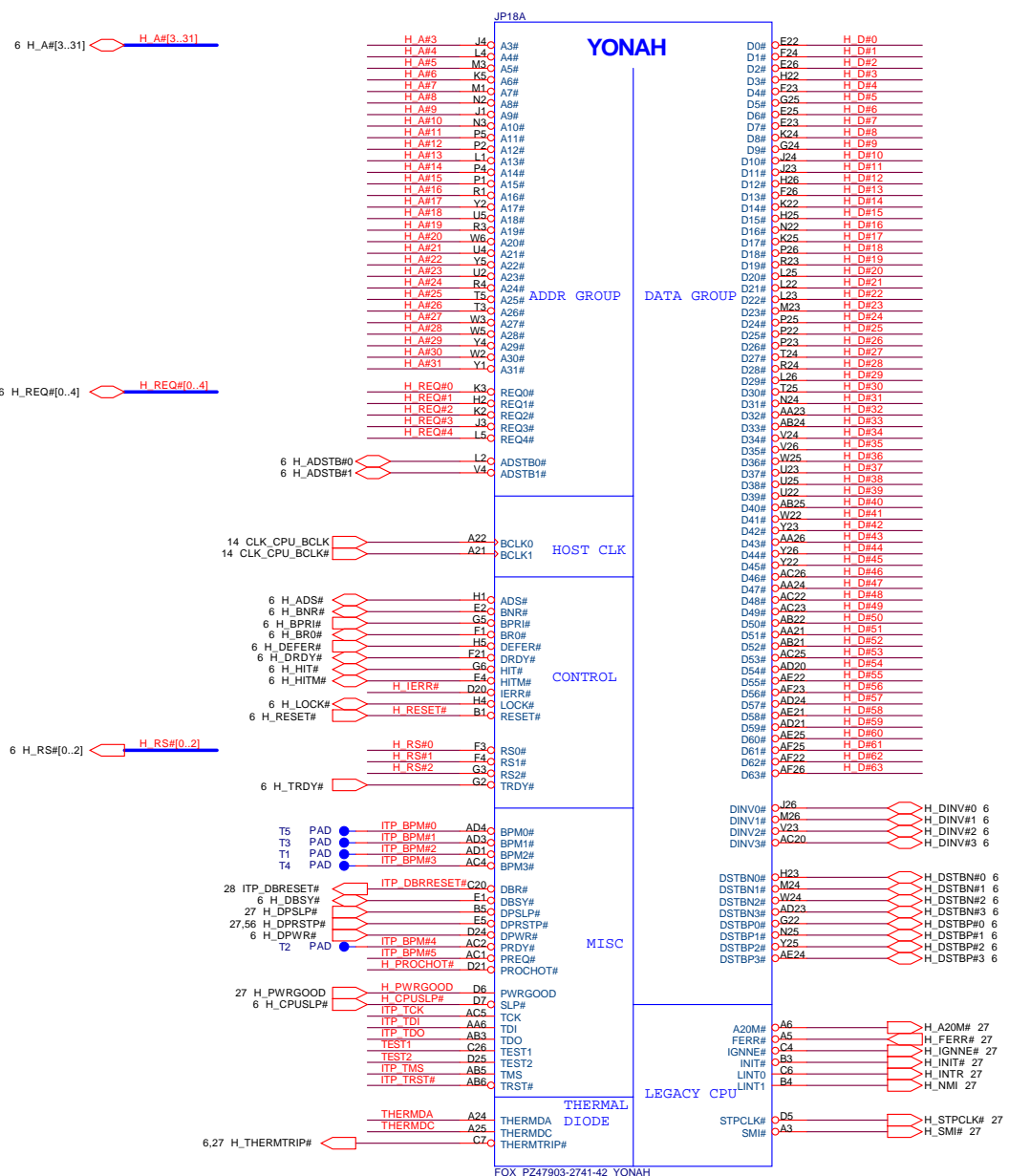
SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

G72MV	G72MV@
	G72MV64@
	G72MV128@
G72MZ	G72MZ@
G73	G73M128@

BTO Option Table

BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@
DVI	DVI@
CardReader	4IN1@
New Card	EXP@
CB1410	1410@

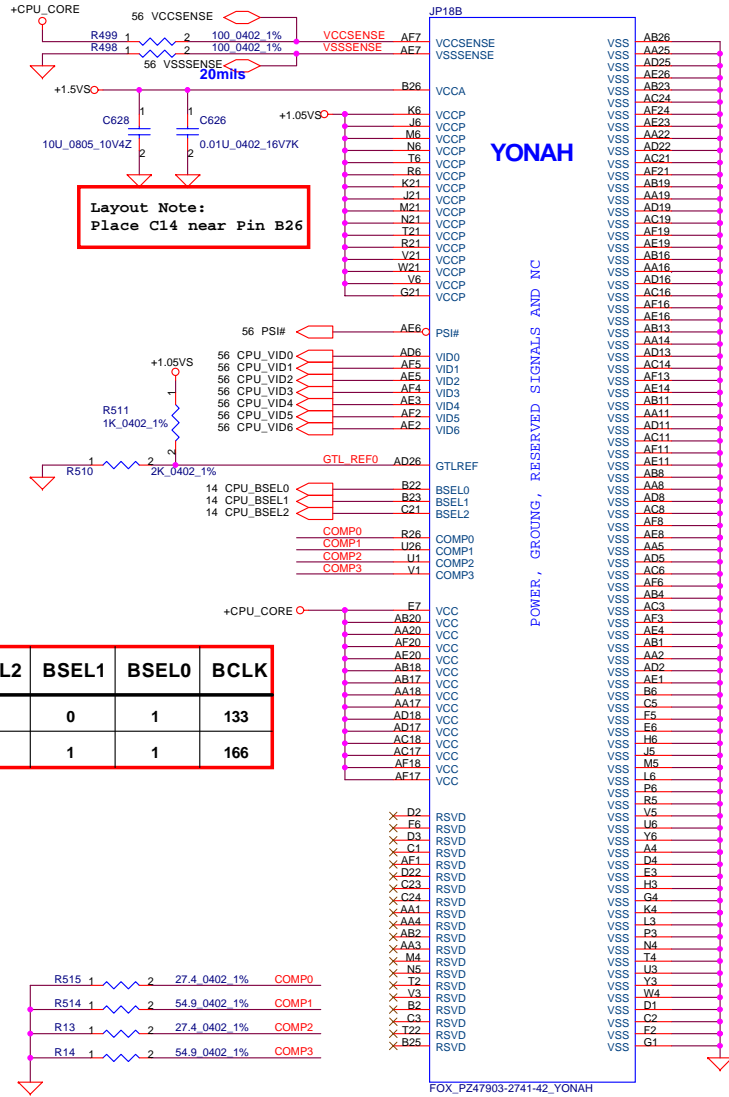
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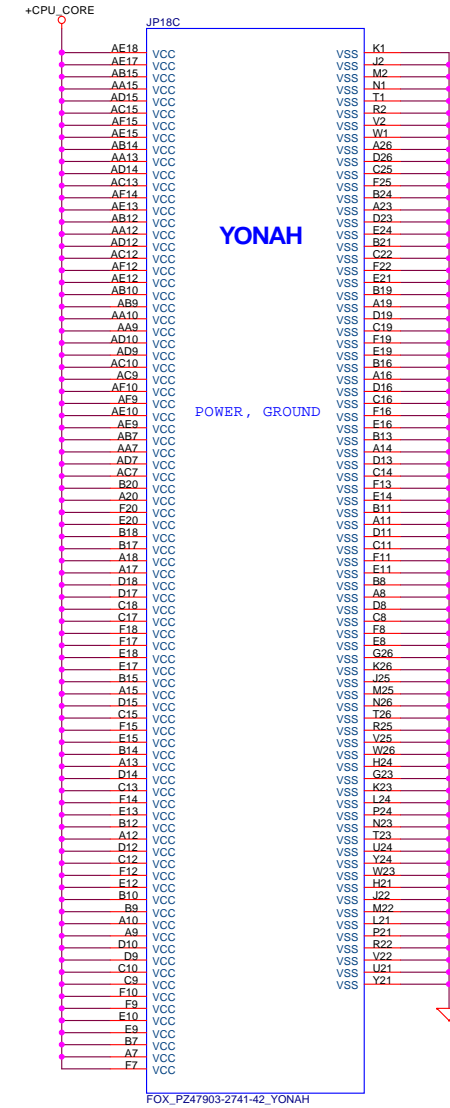
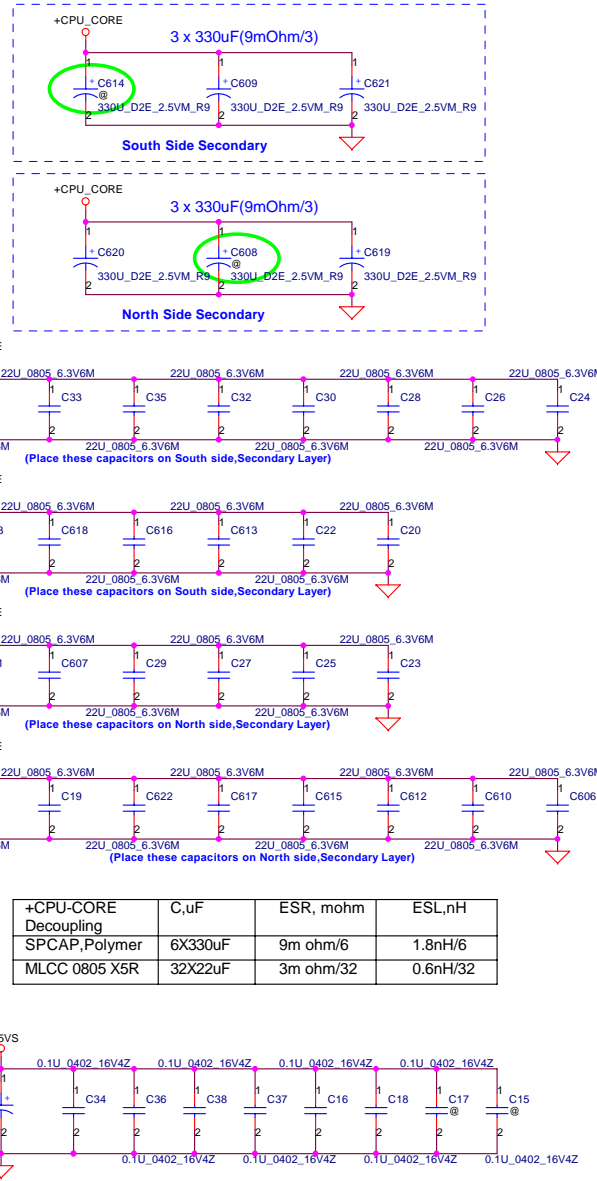
Layout Note:
THERMDA & THERMDC Trace / Space = 10 / 10 mil

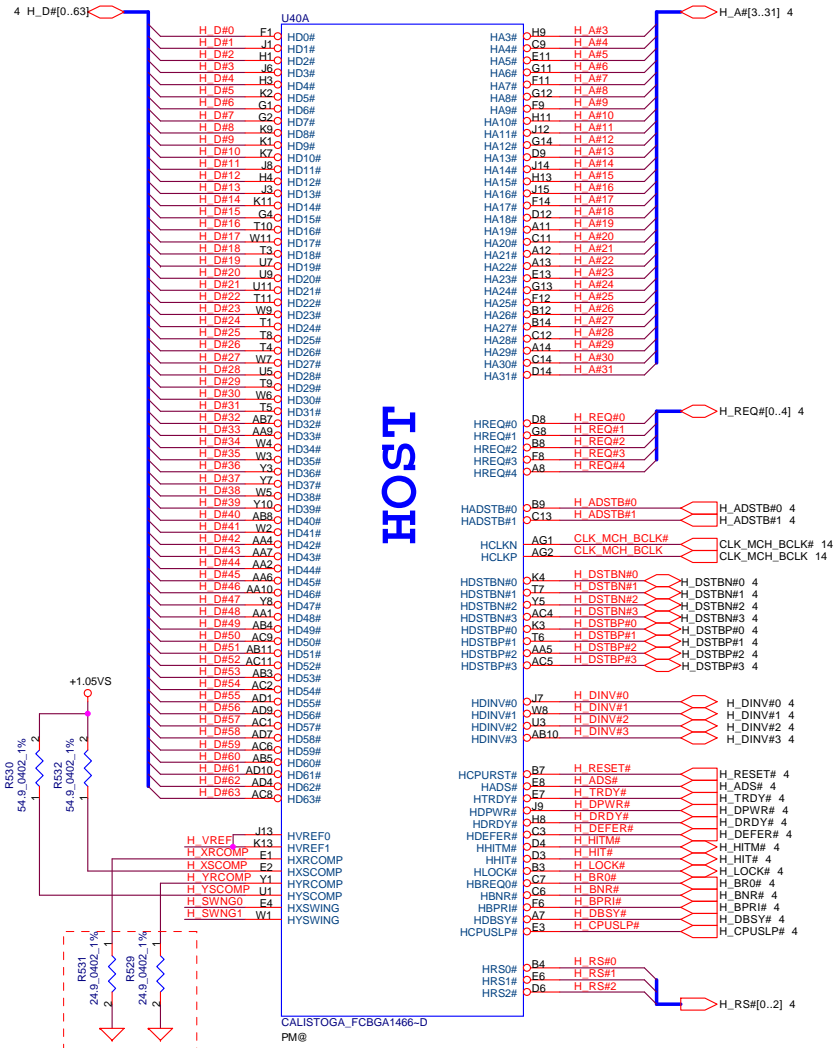
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Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.

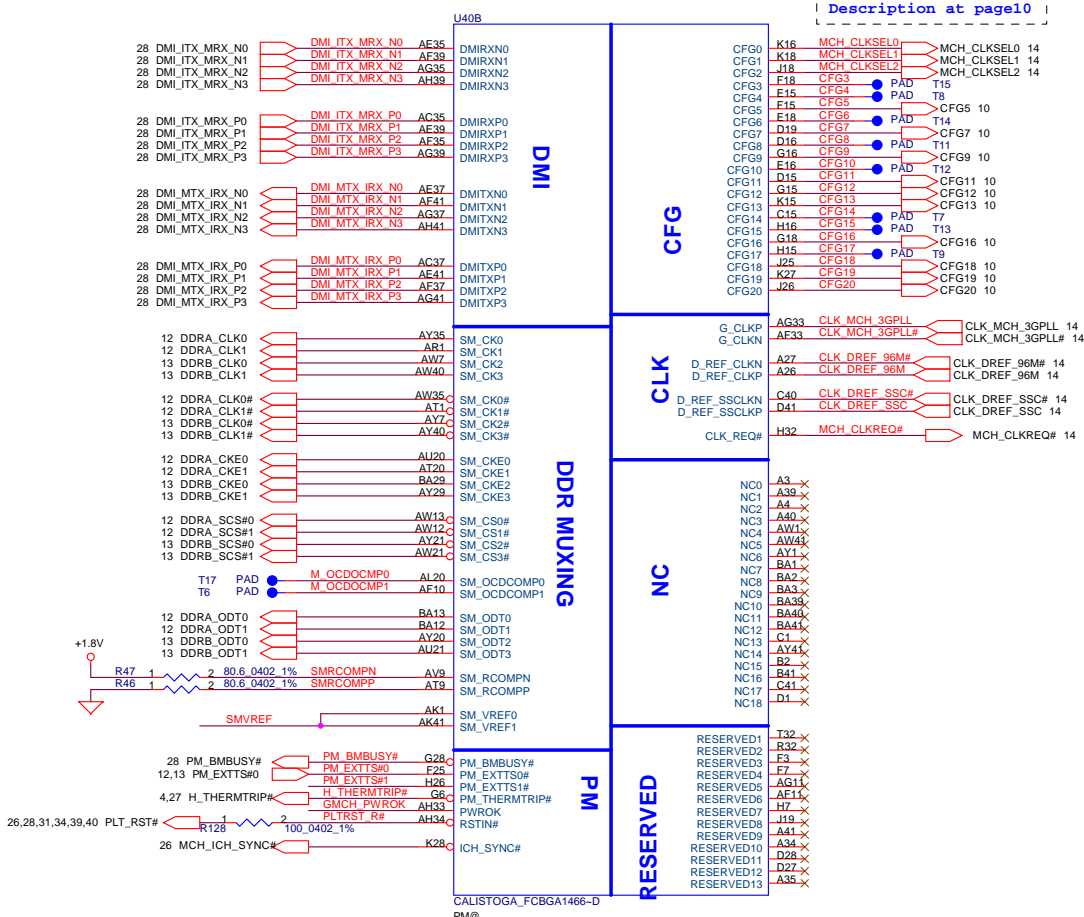
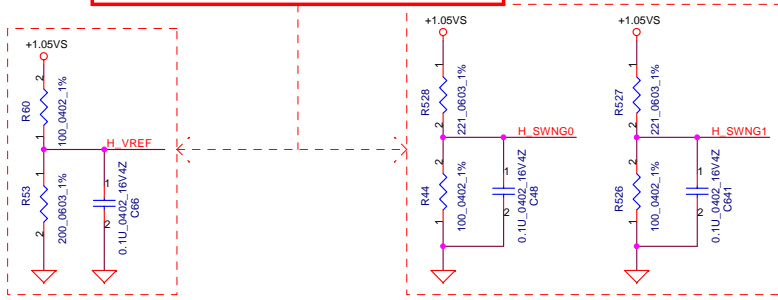


TRACE CLOSELY CPU < 0.5"
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4ohms)
COMP1, COMP3 layout : Space 25mils (55ohms)

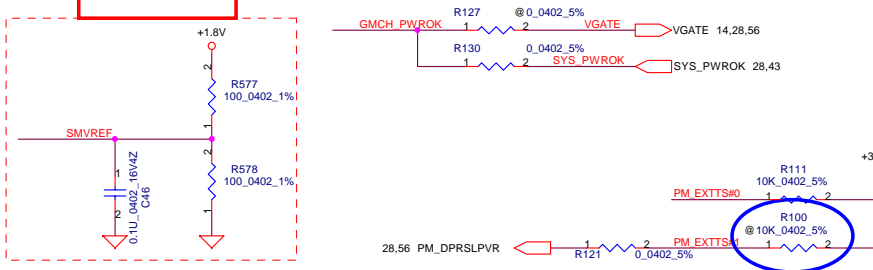




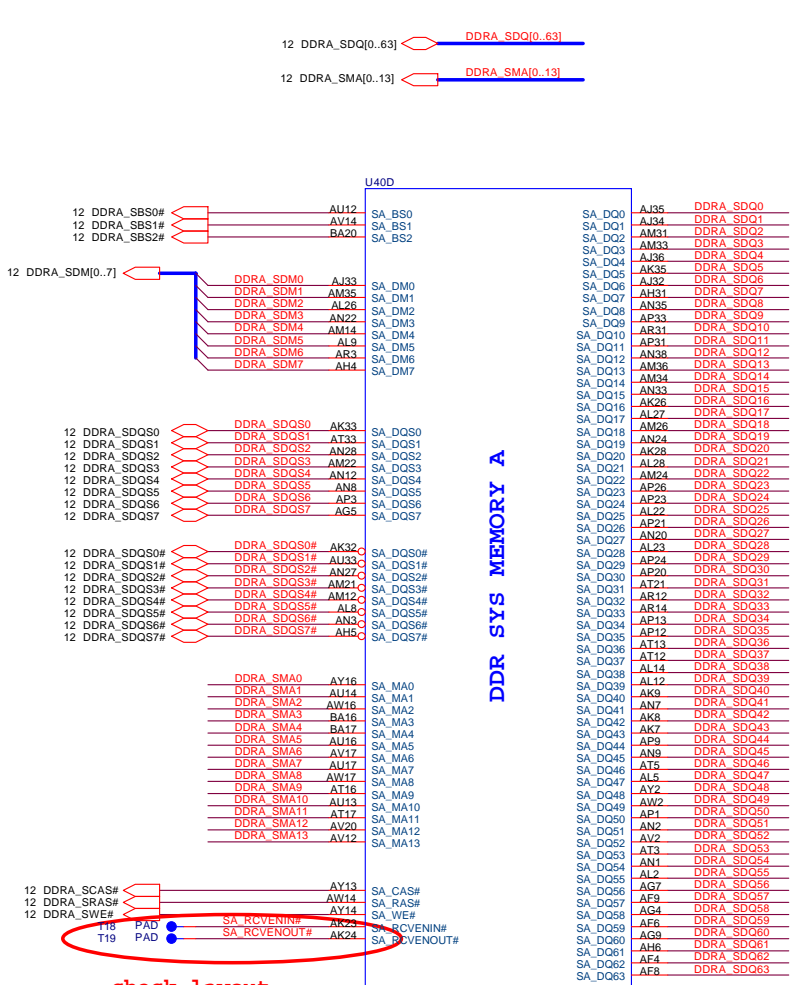
Layout Note:
 H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 /
 H_SWNG1 trace width and spacing is 10/20.



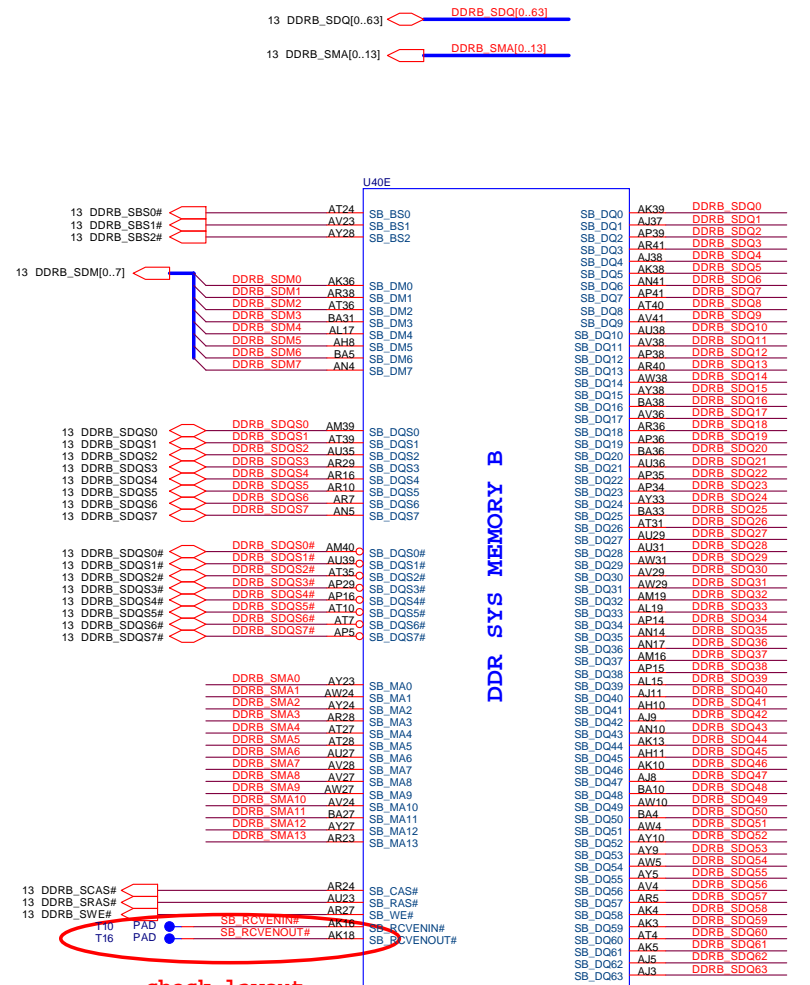
Layout Note:
 SMVREF trace
 width and spacing
 is 20/20.



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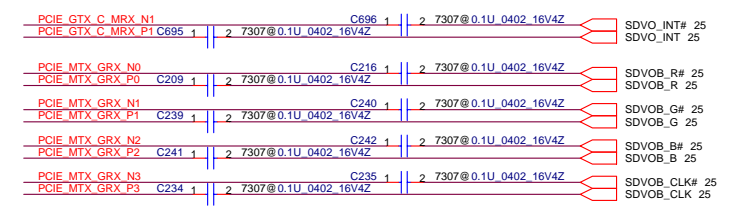
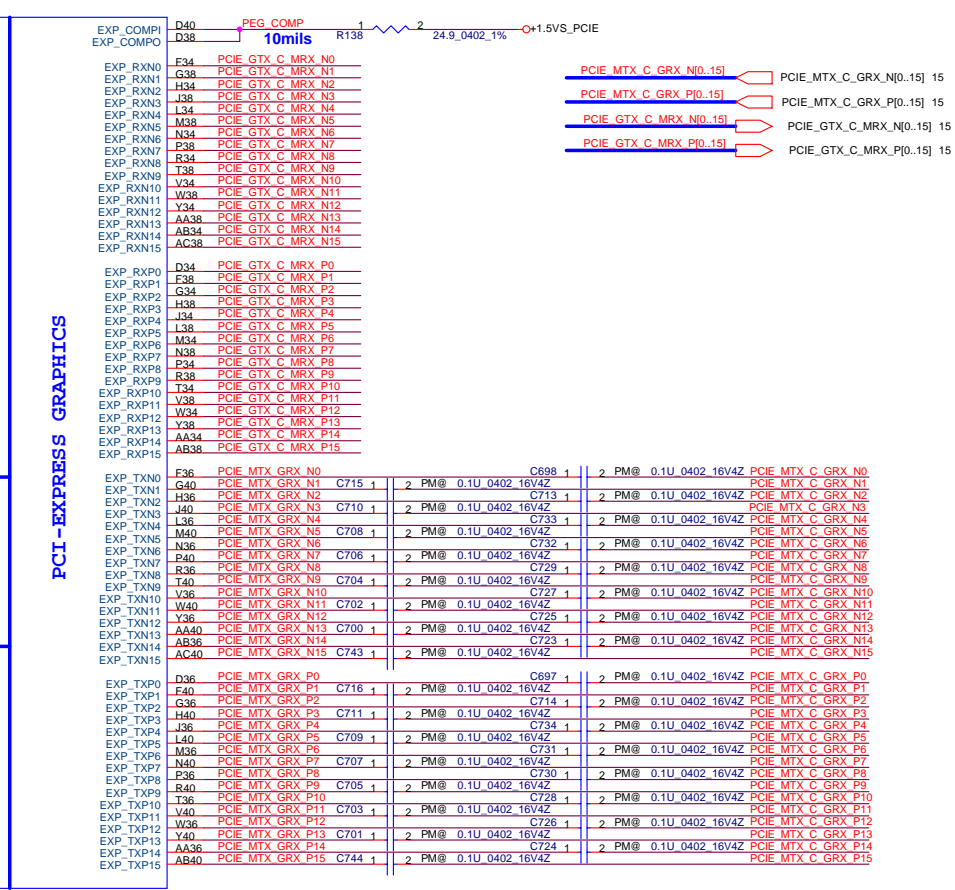
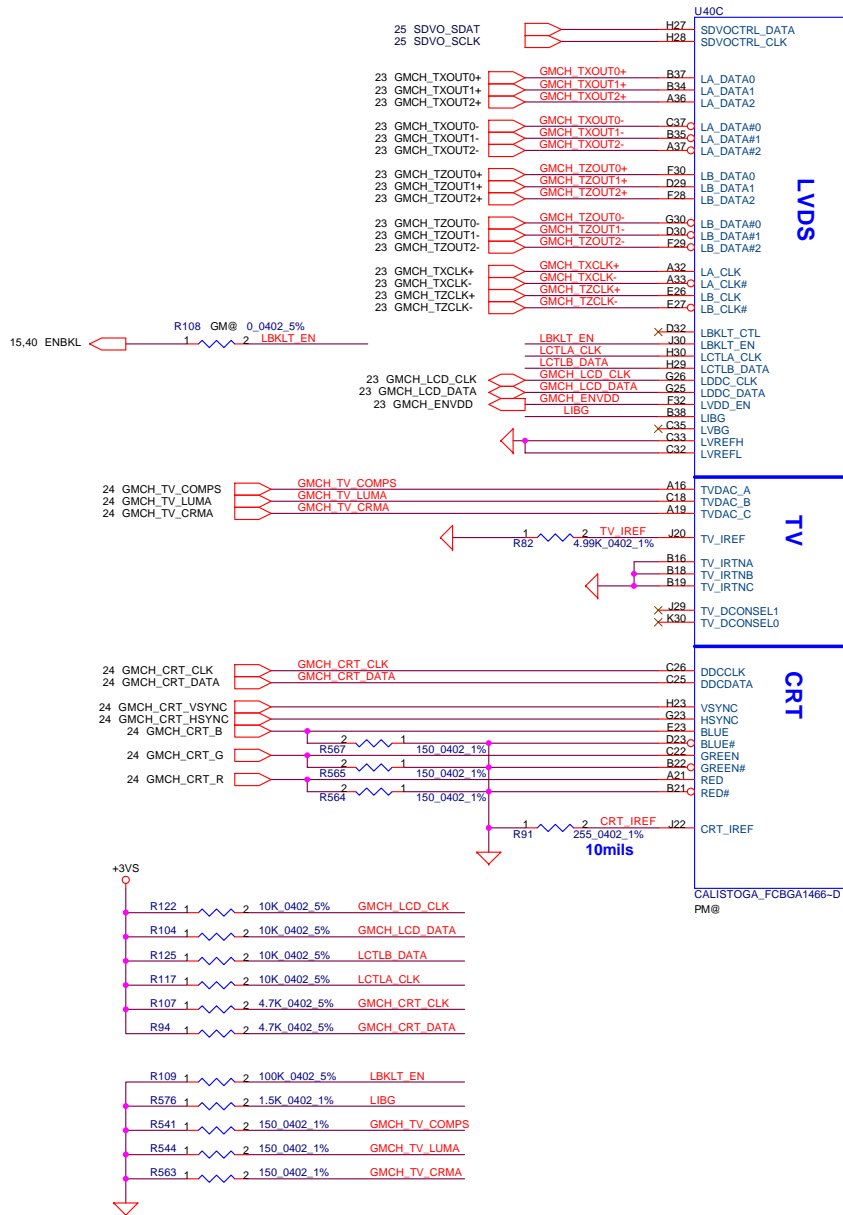


check layout
CALISTOGA_FCBGA1466-D
PM@

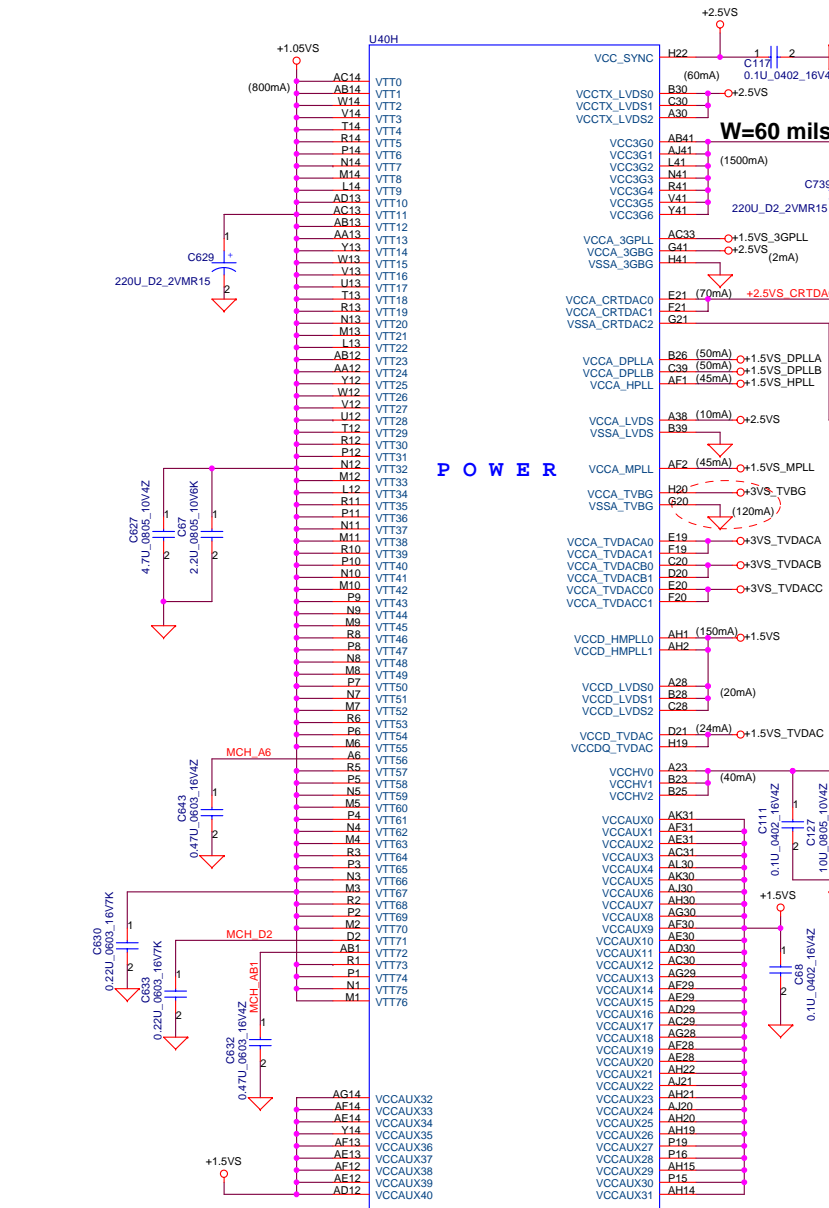
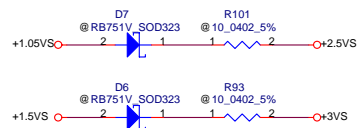


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PM@

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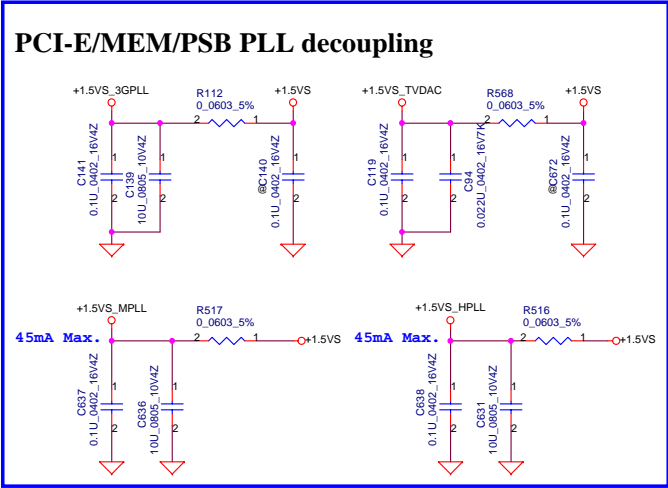
POWER

W=60 mils

CR/DAC: Route caps within 25mil of Alviso. Route FB within 3" of Calistoga

close pin A38

2005/09/19



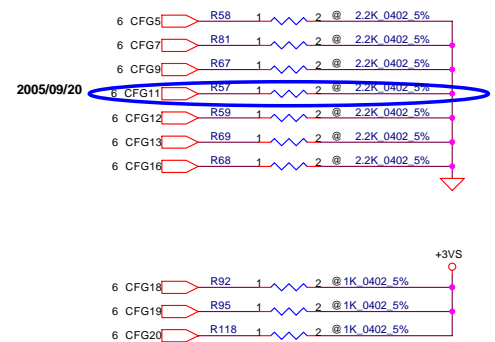
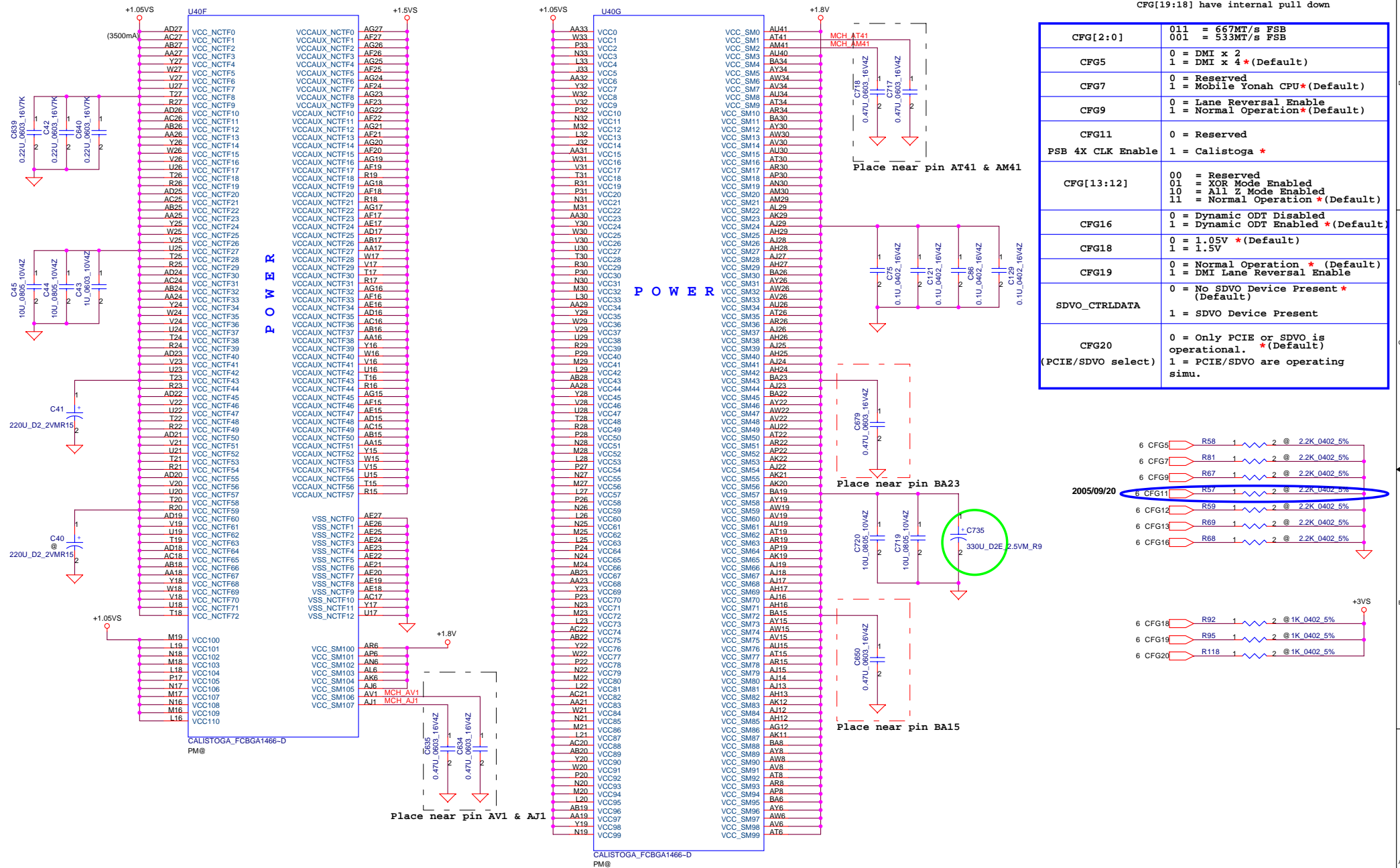
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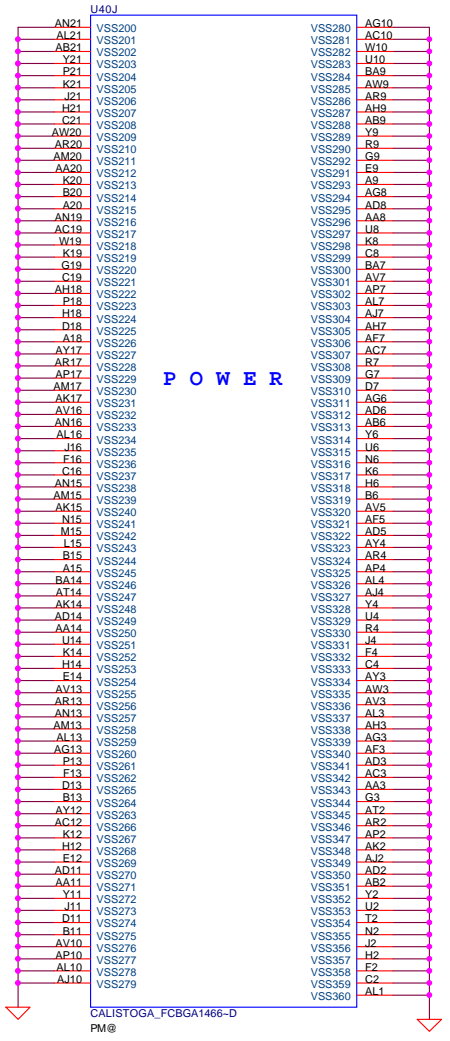
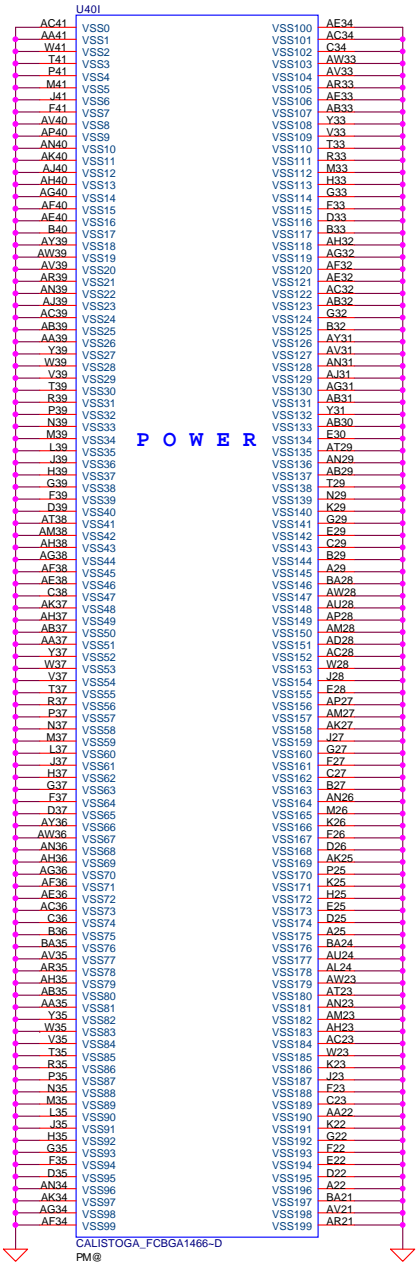
Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG6	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG8	0 = 1.05V *(Default) 1 = 1.5V
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

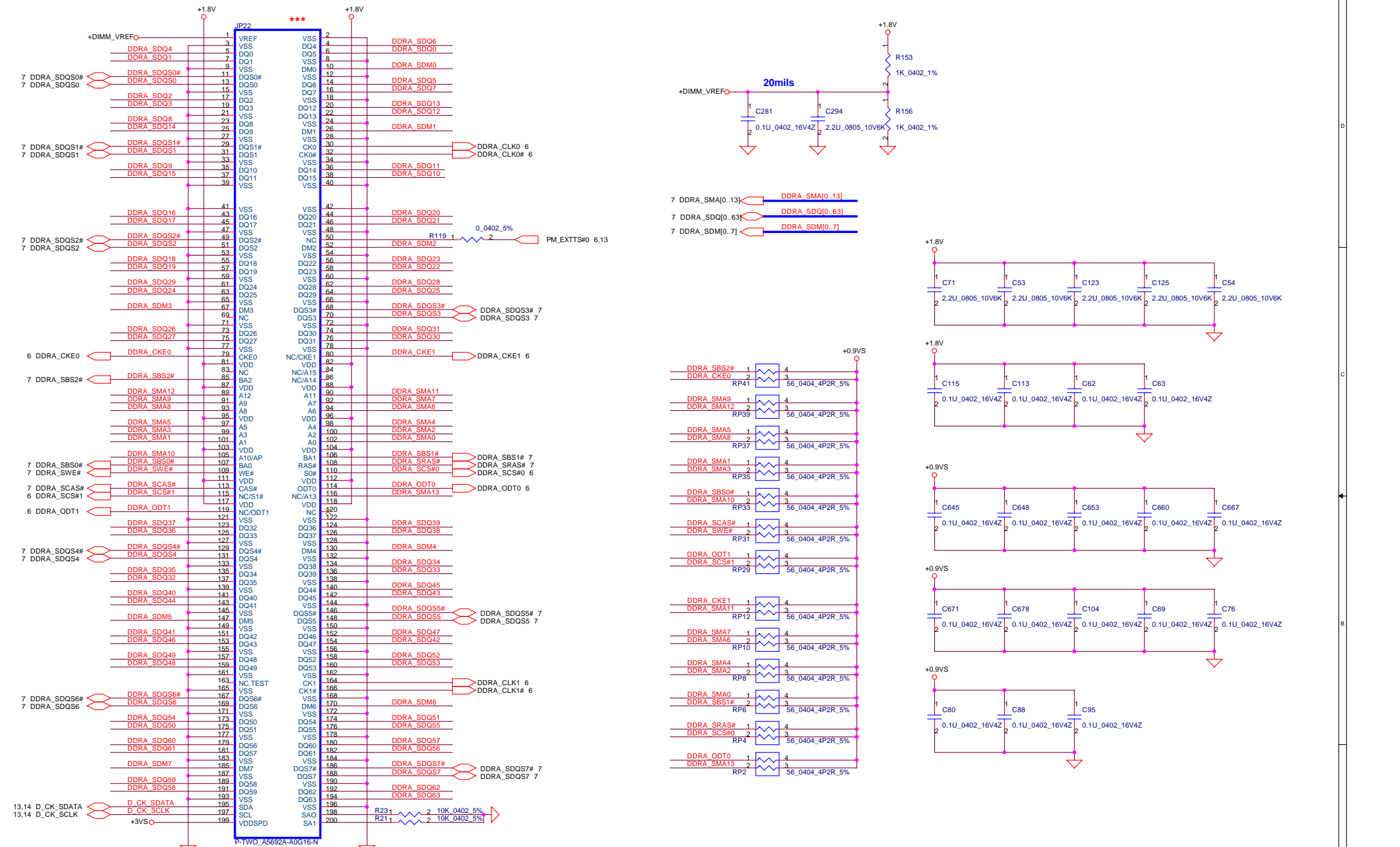


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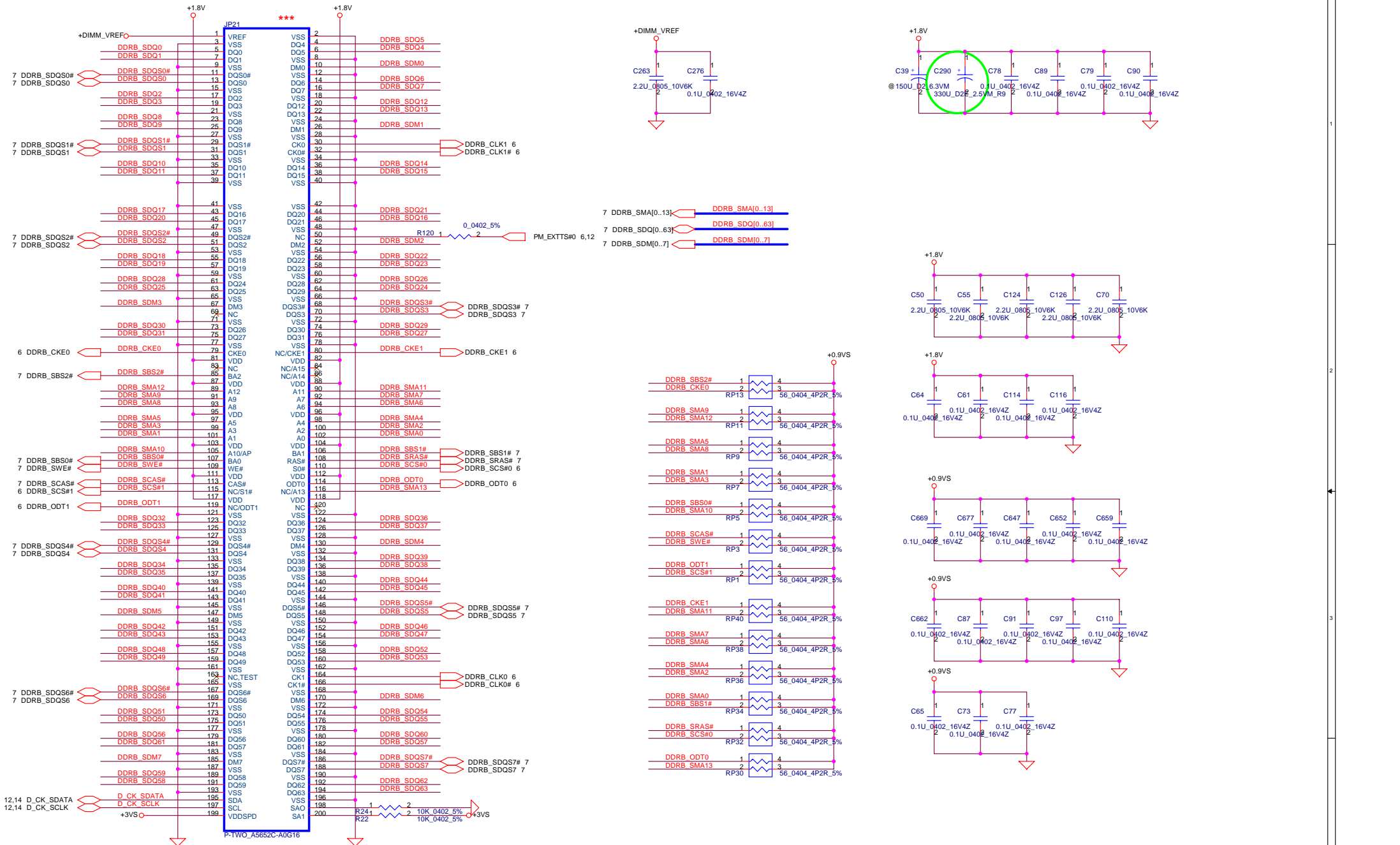


POWER

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DIMM1 STD H:5.2mm (BOT)

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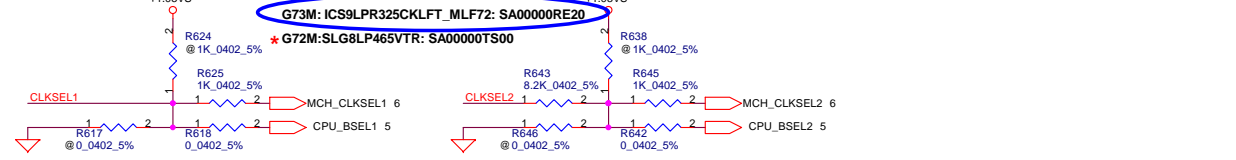
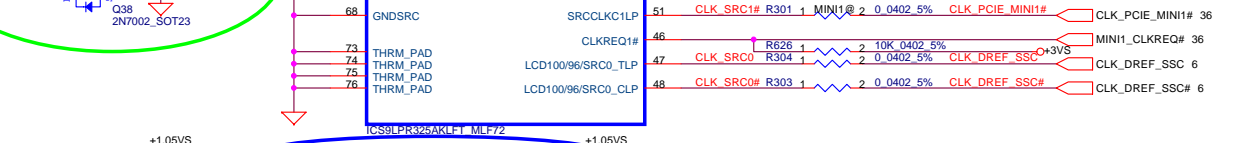
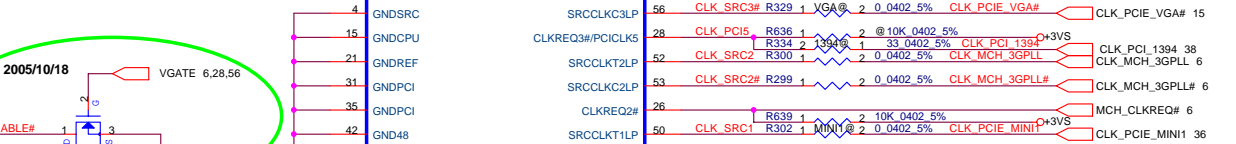
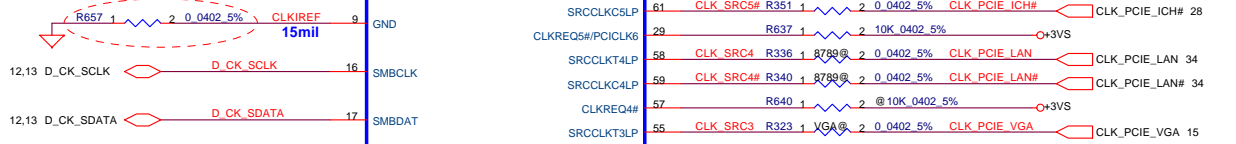
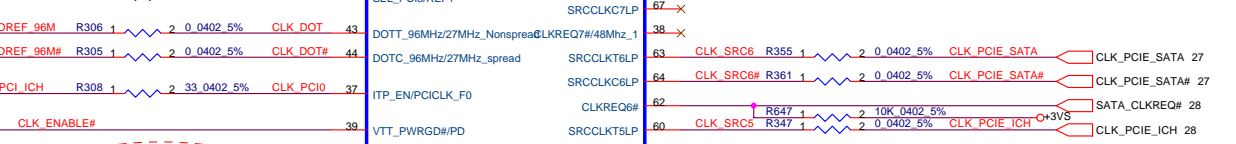
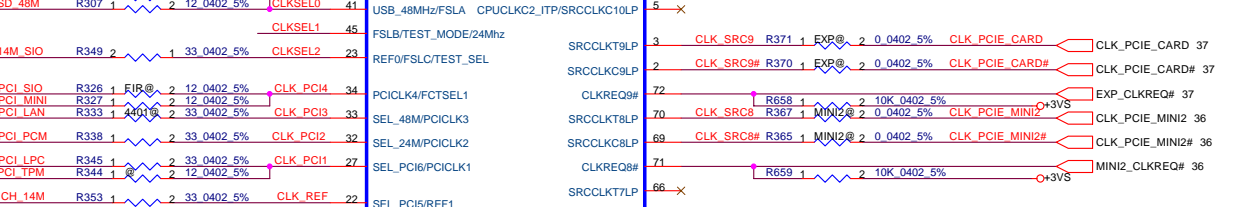
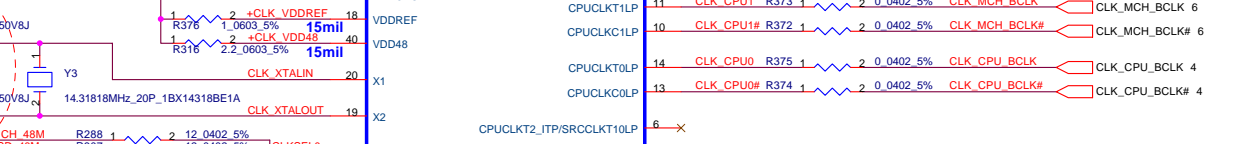
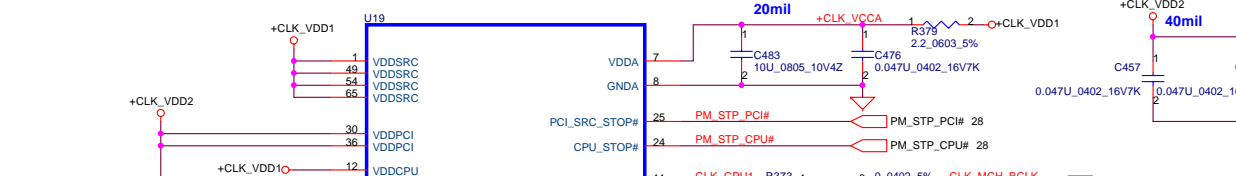
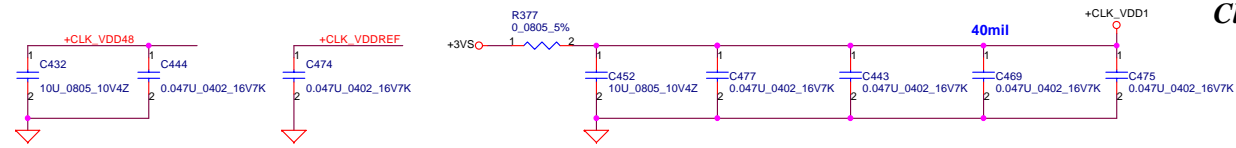
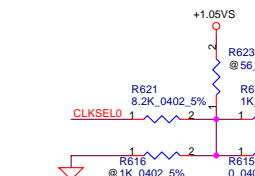
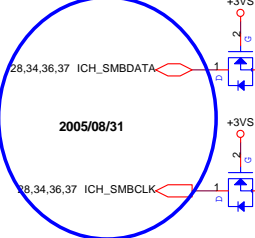
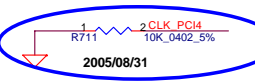
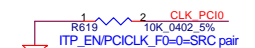
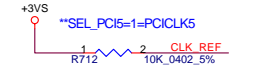
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

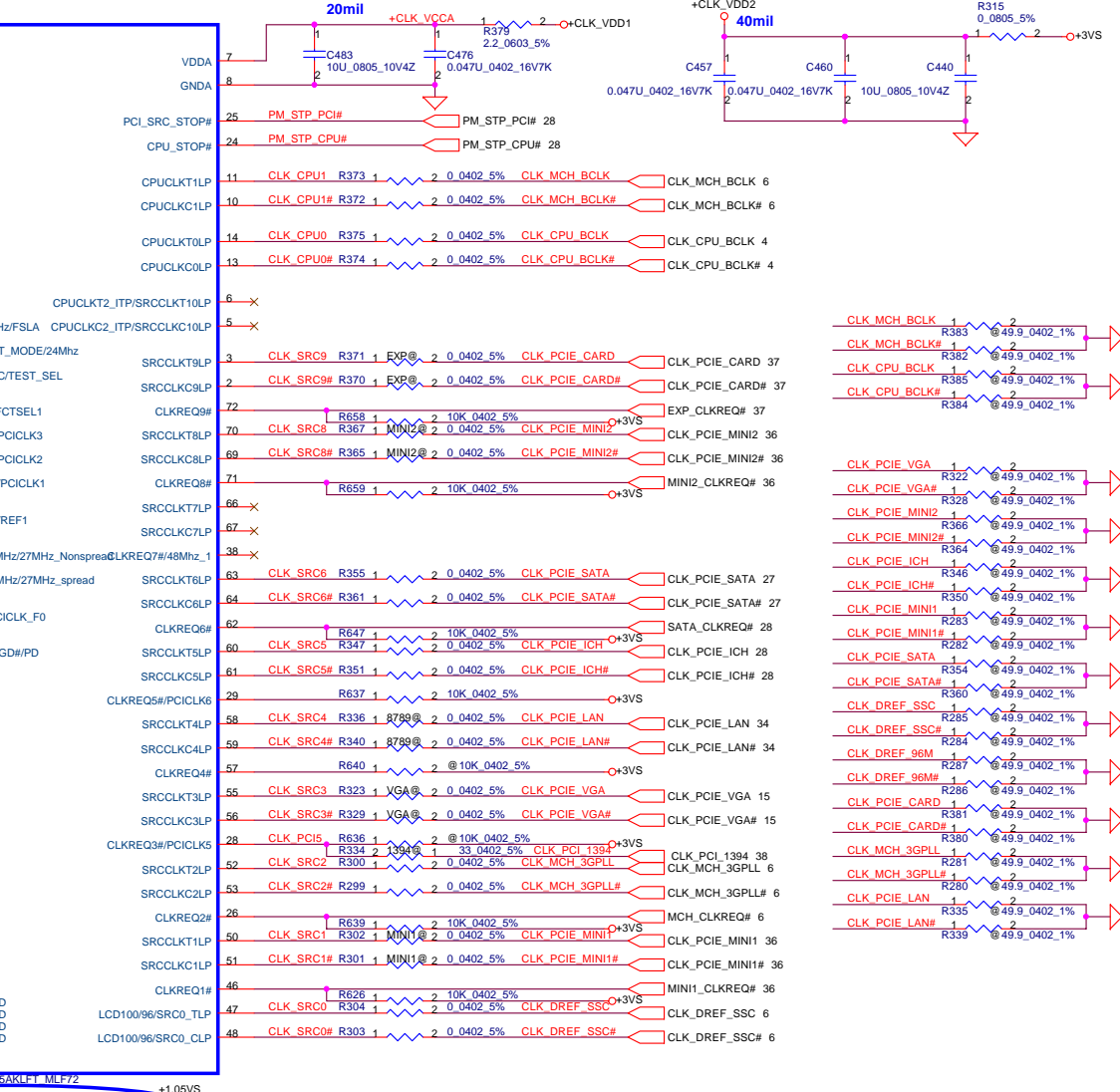
	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz 1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

**SEL_24M/PCICLK2=0=TESTMODE
**SEL_PCI6/PCICLK1=0=CLKREQ5#

**SEL_PCI5=1=PCICLK5
ITP_EN/PCICLK_F0=0=SRC pair



Clock Generator

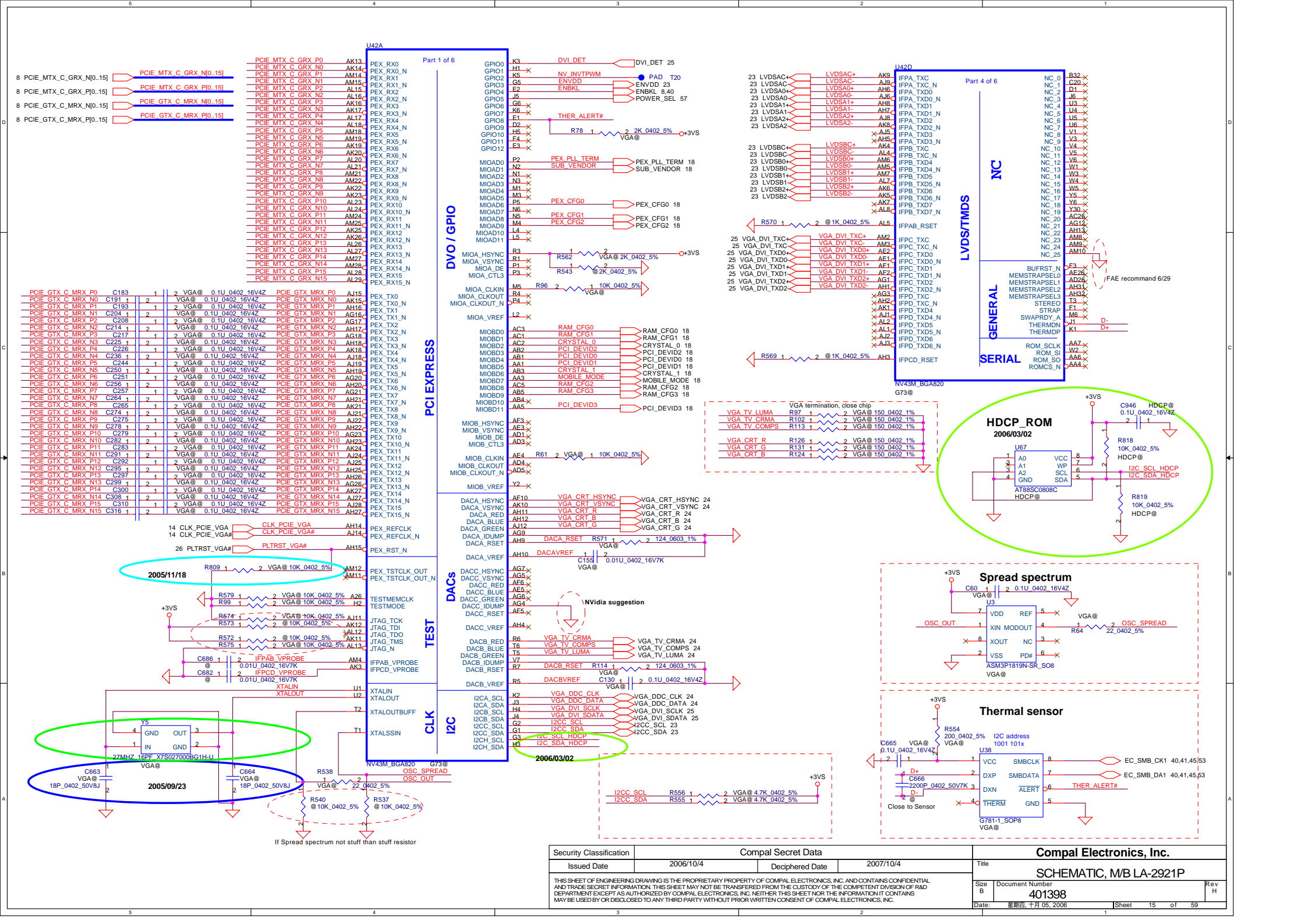


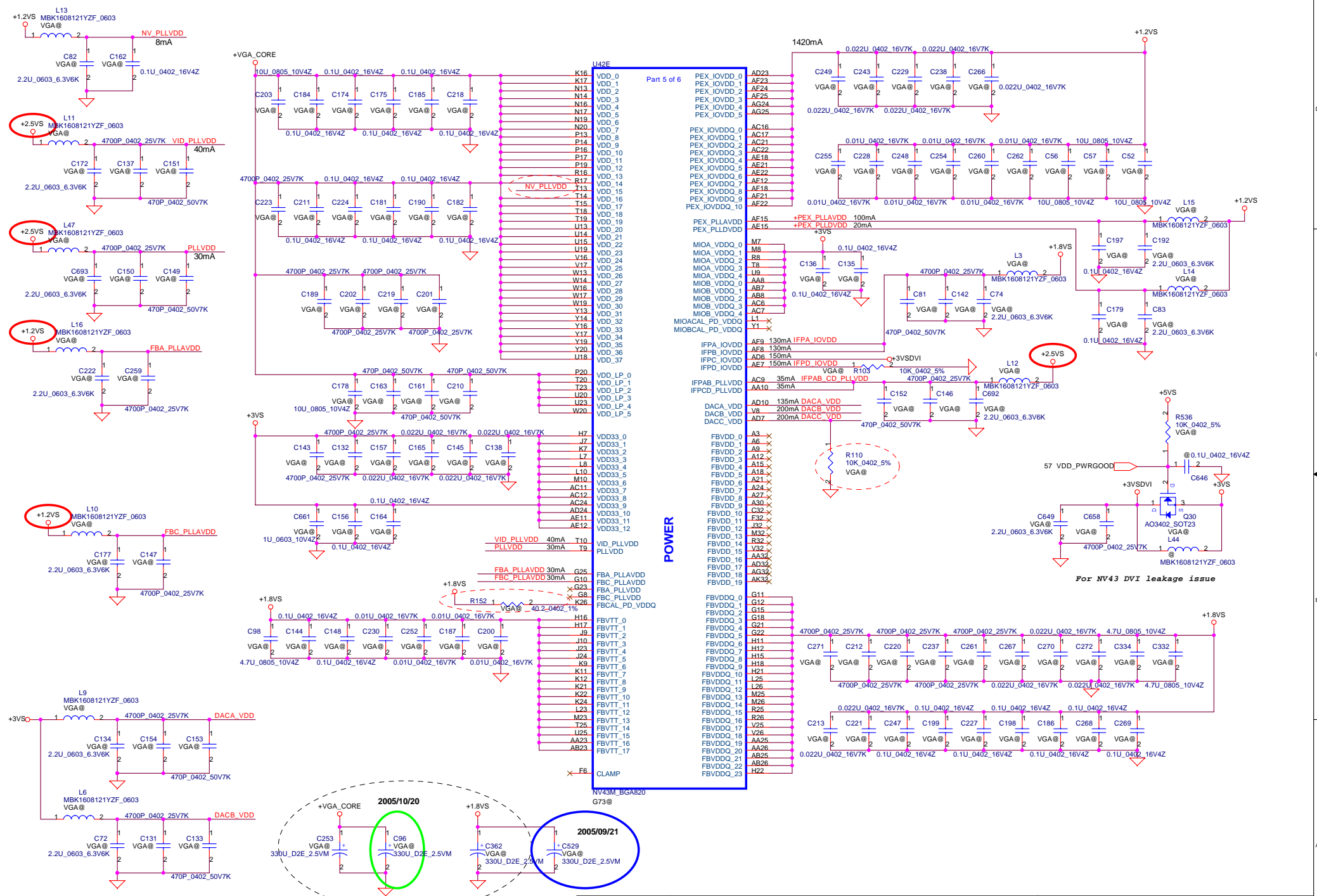
G73M: ICS9LPR325CKLFT_MLF72: SA00000RE20
* G72M: SLG8LP465VTR: SA00000T500

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		2007/10/4

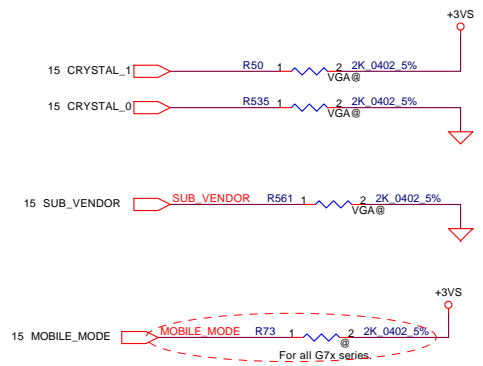
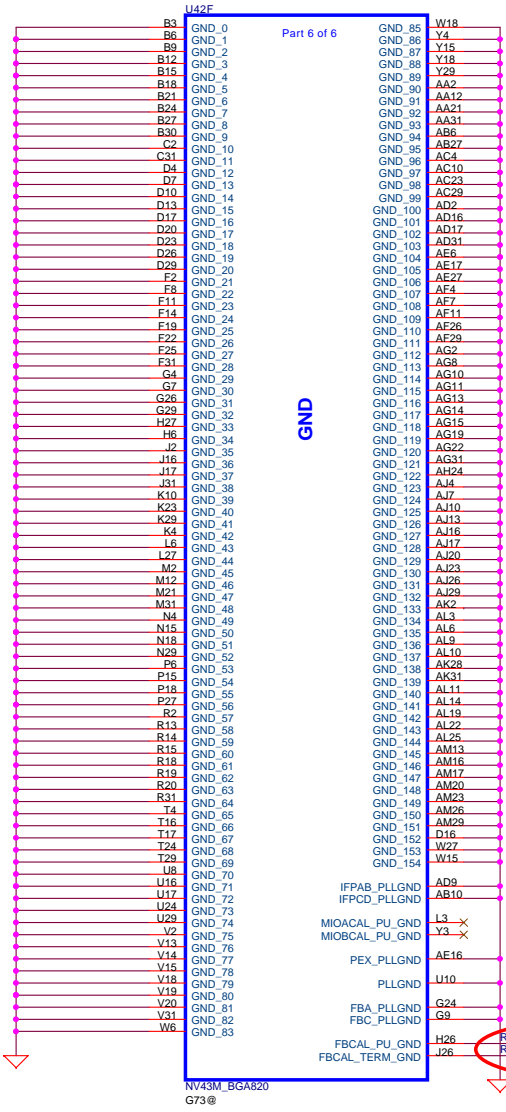
Compal Electronics, Inc.		
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G73M : SA00000QZ00 (A1)
G72M : SA00000QY00
G72MV : SA00000QY20
G73M : SA00000QZ10 (A2)

G72MZ : SA00001BL00
 If used G72MZ RAM_CFG[0..3]=0000
 PCI_DEVID[3..2..1..0]=0110
 No stuff all VRAM.

GF-G07600-SE-N-B1 : SA00000QZ30
GF-G07600SEHN-B1/H : SA00000QZ40

R148=30.1_0402_1% (For G72MV) P/N:SD00000B400
R148=40.2_0402_1% (For G73M) P/N:SD034402A80

 R148 1 G72@ 2 30.1 0402 1%
 R150 1 @ 2 0.0402 5%
 Nvidia suggestion

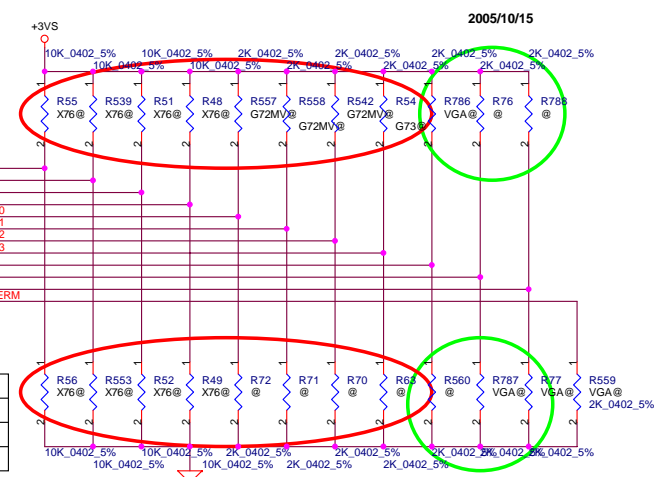
STRAPS	PIN	DESCRIPTION	Value	Value
CRYSTAL[1:0]	MIOBD[6,2]	27MHz=10, 14.318MHz=01, 13.5MHz=00	10	
ROM_TYPE[1:0]	MIOBD [11:10]	Parallel=00, SERIAL M25P10=01, Serial SST45VF=10	01	
SUB_VENDOR	MIOAD1	VBIOs on card (pull high) VBIOs with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Recommended for G7x	001	
RAM_CFG[3:0]	MIOAD[5:2]	RAM_CFG[3] (Bandwidth 0=Full, 1=Half) RAM_CFG[2] (0=16M or 1=32M) RAM_CFG[1:0] (Manufacture) (01=Sam, 10=Inf, 11=Hyn)		
PCI_DEVID[3:0]	VIPOD[5:3] MIOA_HSYNC	G73M-xxxxx8 G72M-0x01D8 G72MV-0x01D7 TBD/TBD	1000	0111
MOBILE_MODE	MIOBD7	For NV44M/G7x		0

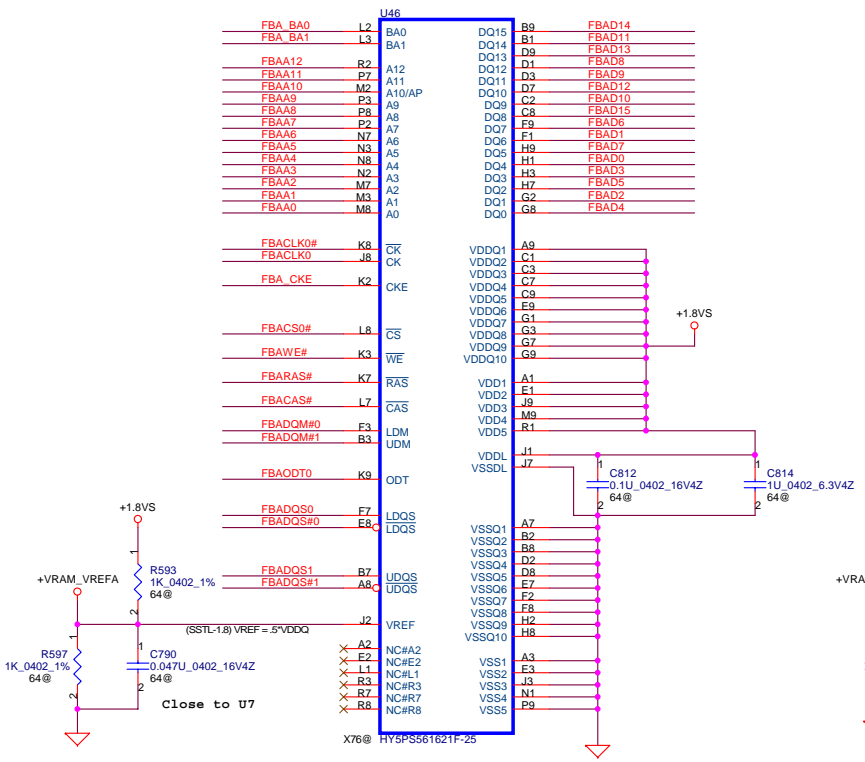
RAM_CFG[1:0] (Manufacture) (01=Sam, 10=Inf, 11=Hyn)
 RAM_CFG[2] (0=16M or 1=32M)
 RAM_CFG[3] (Bandwidth 0=Full, 1=Half)

Bandwidth	RAM Type	Vendor
FULL R49	32M R51	Samsung R553, R555
HALF R48	16M R52	Hynix R539, R555 Infineon R539, R556

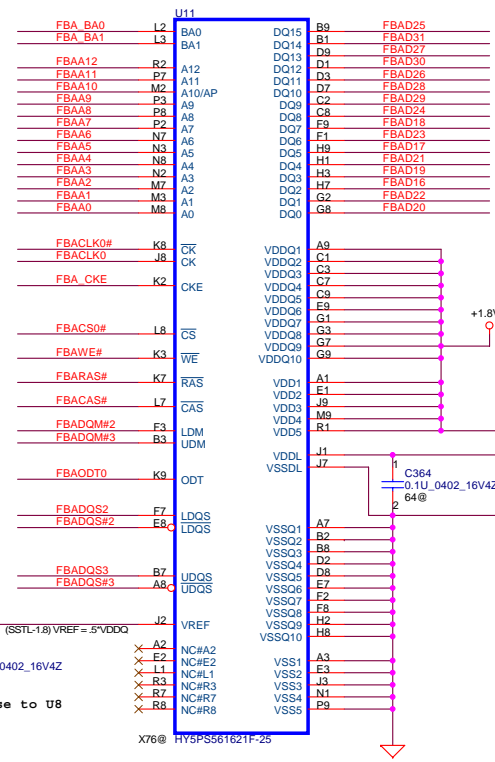
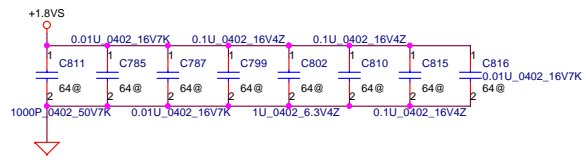
Package		
(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)

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Size B	Document Number	Rev H	Date: 星期四, 十月 05, 2006	
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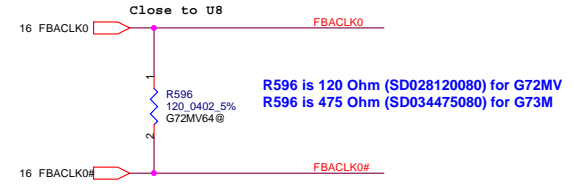
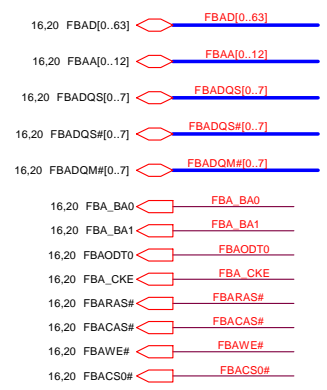
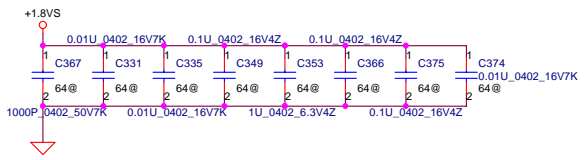




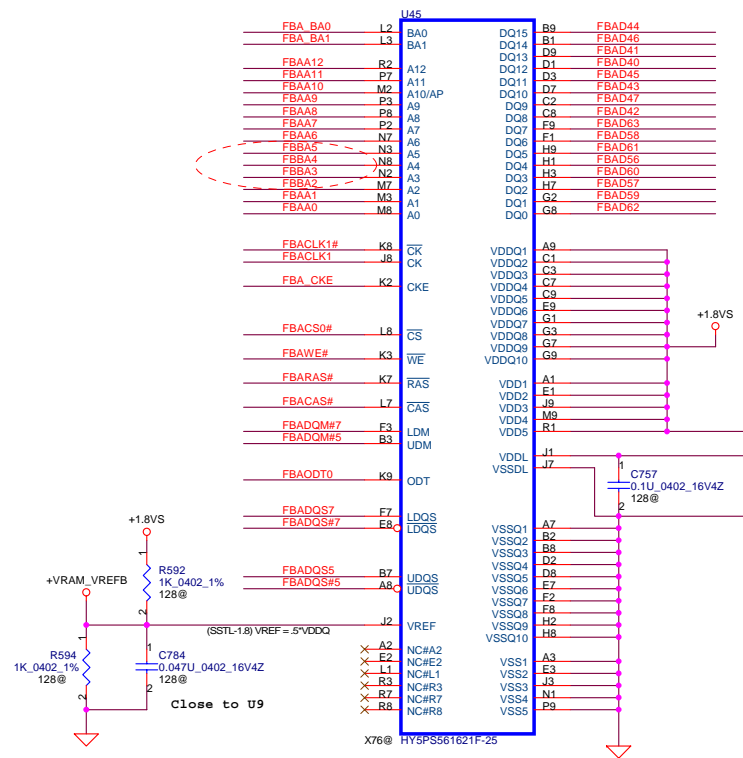
DDR2 BGA MEMORY



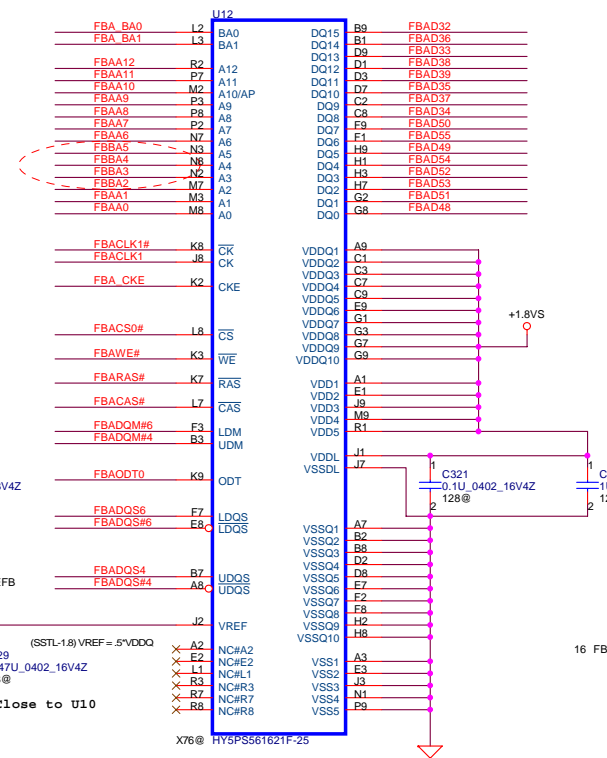
DDR2 BGA MEMORY



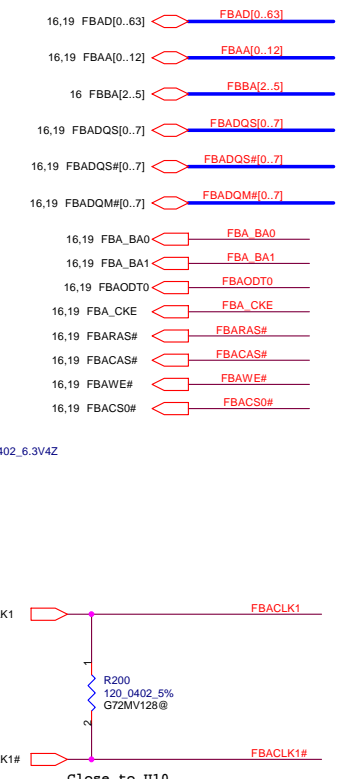
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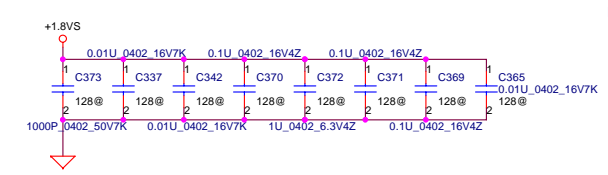
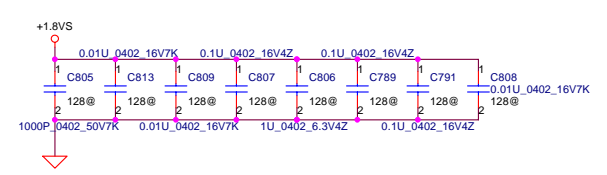
DDR2 BGA MEMORY



DDR2 BGA MEMORY

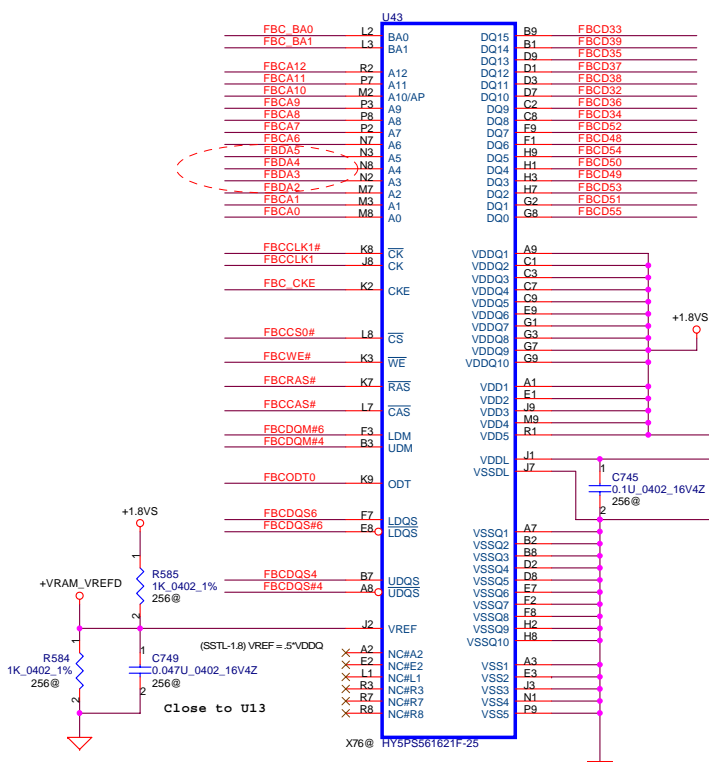


R200 is 120 Ohm (SD028120080) for G72MV
R200 is 475 Ohm (SD034475080) for G73M

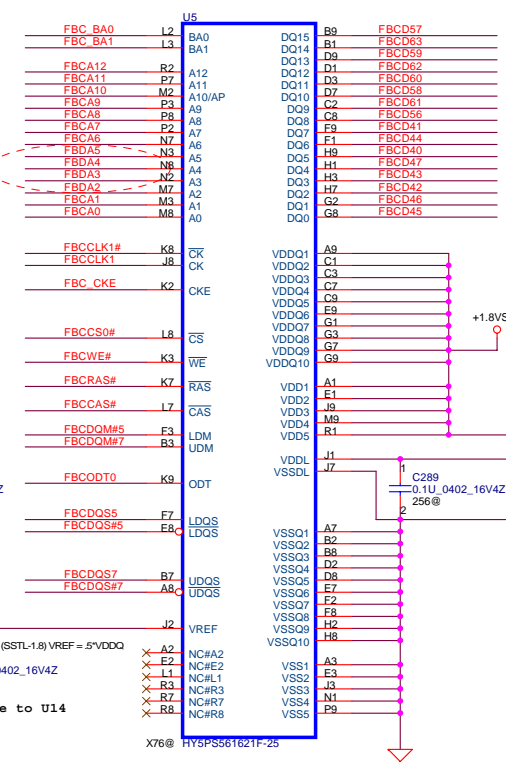
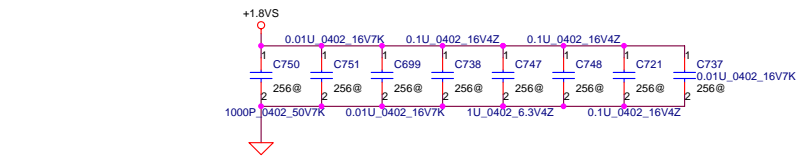


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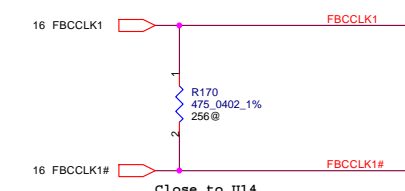
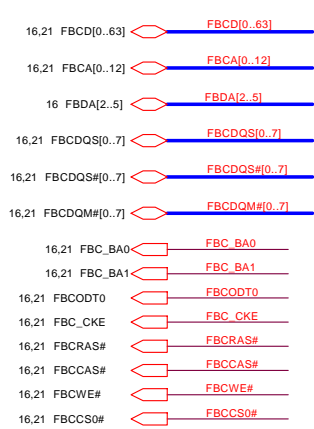
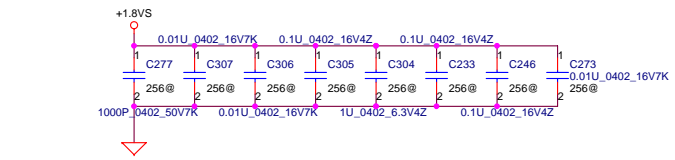
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DDR2 BGA MEMORY



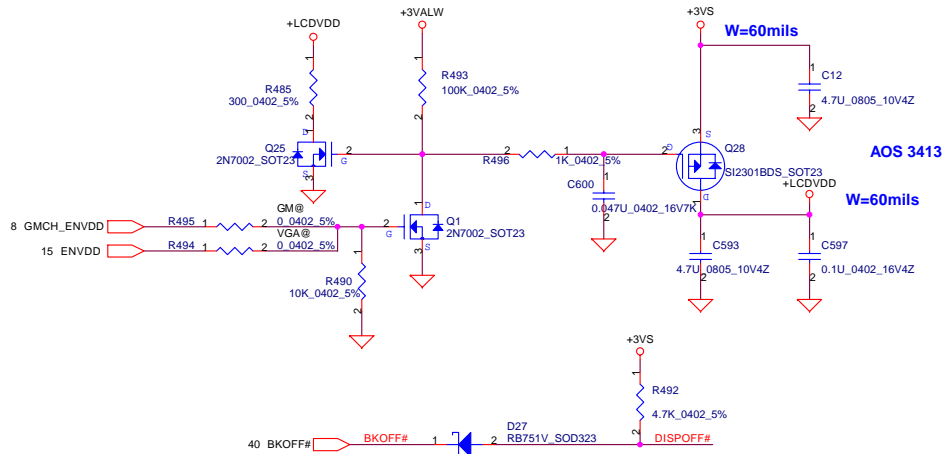
DDR2 BGA MEMORY



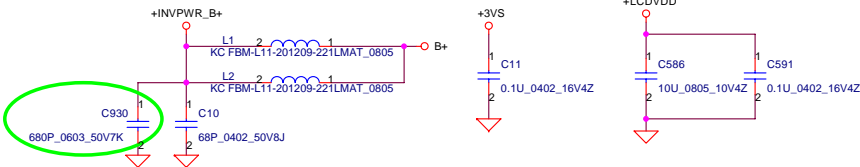
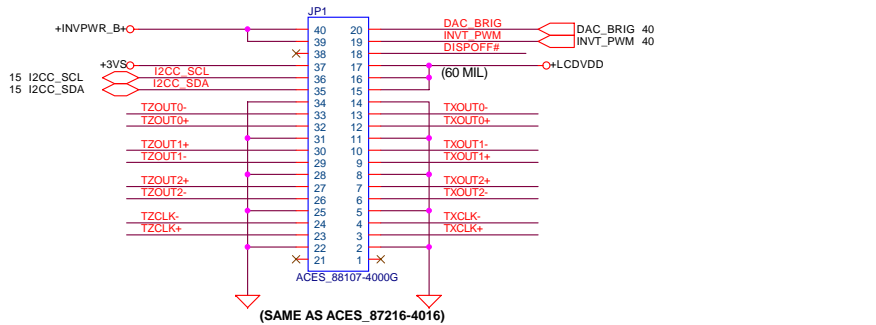
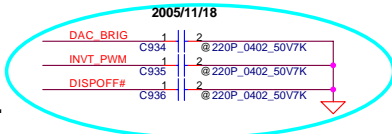
R170 is 120 Ohm (SD028120080) for G72MV
R170 is 475 Ohm (SD034475080) for G73M

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LCD POWER CIRCUIT



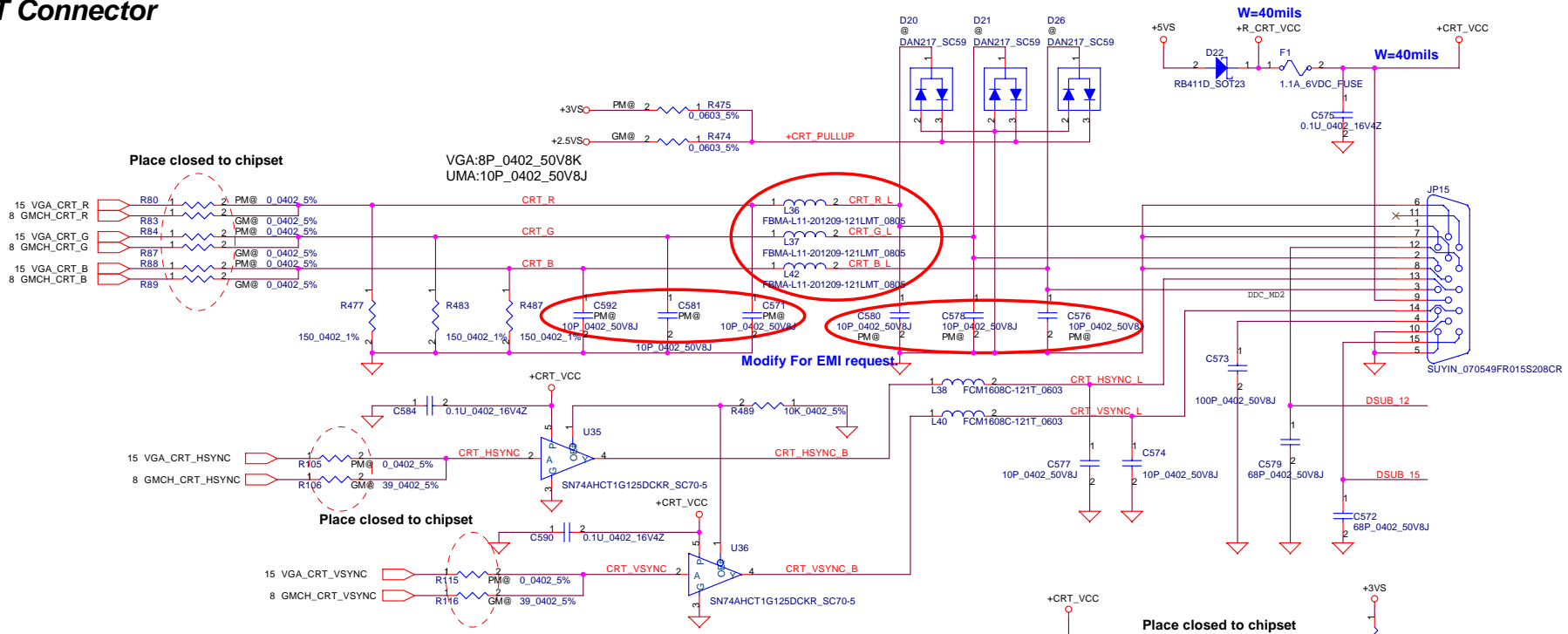
LCD/PANEL BD. Conn.



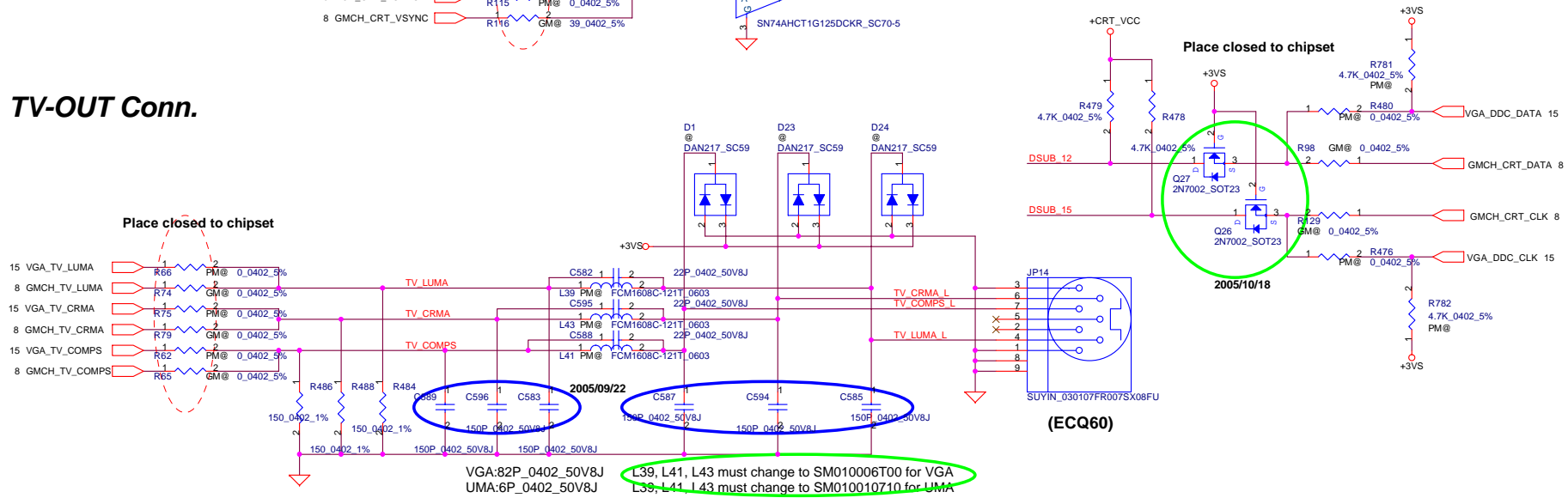
TXOUT0-	R25	1	2	VGA@ 0.0402 5%	LVDSA0-	LVDSA0-	15
TXOUT0+	R26	1	2	VGA@ 0.0402 5%	LVDSA0+	LVDSA0+	15
TXOUT1-	R27	1	2	VGA@ 0.0402 5%	LVDSA1-	LVDSA1-	15
TXOUT1+	R28	1	2	VGA@ 0.0402 5%	LVDSA1+	LVDSA1+	15
TXOUT2-	R29	1	2	VGA@ 0.0402 5%	LVDSA2-	LVDSA2-	15
TXOUT2+	R30	1	2	VGA@ 0.0402 5%	LVDSA2+	LVDSA2+	15
TXCLK-	R31	1	2	VGA@ 0.0402 5%	LVDSAC-	LVDSAC-	15
TXCLK+	R32	1	2	VGA@ 0.0402 5%	LVDSAC+	LVDSAC+	15
TZOUT0-	R33	1	2	VGA@ 0.0402 5%	LVDSB0-	LVDSB0-	15
TZOUT0+	R34	1	2	VGA@ 0.0402 5%	LVDSB0+	LVDSB0+	15
TZOUT1+	R35	1	2	VGA@ 0.0402 5%	LVDSB1+	LVDSB1+	15
TZOUT1-	R36	1	2	VGA@ 0.0402 5%	LVDSB1-	LVDSB1-	15
TZOUT2+	R37	1	2	VGA@ 0.0402 5%	LVDSB2+	LVDSB2+	15
TZOUT2-	R38	1	2	VGA@ 0.0402 5%	LVDSB2-	LVDSB2-	15
TZCLK-	R39	1	2	VGA@ 0.0402 5%	LVDSBC-	LVDSBC-	15
TZCLK+	R40	1	2	VGA@ 0.0402 5%	LVDSBC+	LVDSBC+	15
I2CC_SCL	R41	1	2	GM@ 0.0402 5%	GMCH_LCD_CLK	GMCH_LCD_CLK	8
I2CC_SDA	R42	1	2	GM@ 0.0402 5%	GMCH_LCD_DATA	GMCH_LCD_DATA	8
TXOUT0-	R509	1	2	GM@ 0.0402 5%	GMCH_TXOUT0-	GMCH_TXOUT0-	8
TXOUT0+	R508	1	2	GM@ 0.0402 5%	GMCH_TXOUT0+	GMCH_TXOUT0+	8
TXOUT1-	R507	1	2	GM@ 0.0402 5%	GMCH_TXOUT1-	GMCH_TXOUT1-	8
TXOUT1+	R506	1	2	GM@ 0.0402 5%	GMCH_TXOUT1+	GMCH_TXOUT1+	8
TXOUT2+	R505	1	2	GM@ 0.0402 5%	GMCH_TXOUT2+	GMCH_TXOUT2+	8
TXOUT2-	R504	1	2	GM@ 0.0402 5%	GMCH_TXOUT2-	GMCH_TXOUT2-	8
TXCLK-	R503	1	2	GM@ 0.0402 5%	GMCH_TXCLK-	GMCH_TXCLK-	8
TXCLK+	R502	1	2	GM@ 0.0402 5%	GMCH_TXCLK+	GMCH_TXCLK+	8
TZOUT0-	R525	1	2	GM@ 0.0402 5%	GMCH_TZOUT0-	GMCH_TZOUT0-	8
TZOUT0+	R524	1	2	GM@ 0.0402 5%	GMCH_TZOUT0+	GMCH_TZOUT0+	8
TZOUT1+	R523	1	2	GM@ 0.0402 5%	GMCH_TZOUT1+	GMCH_TZOUT1+	8
TZOUT1-	R522	1	2	GM@ 0.0402 5%	GMCH_TZOUT1-	GMCH_TZOUT1-	8
TZOUT2+	R521	1	2	GM@ 0.0402 5%	GMCH_TZOUT2+	GMCH_TZOUT2+	8
TZOUT2-	R520	1	2	GM@ 0.0402 5%	GMCH_TZOUT2-	GMCH_TZOUT2-	8
TZCLK-	R519	1	2	GM@ 0.0402 5%	GMCH_TZCLK-	GMCH_TZCLK-	8
TZCLK+	R518	1	2	GM@ 0.0402 5%	GMCH_TZCLK+	GMCH_TZCLK+	8

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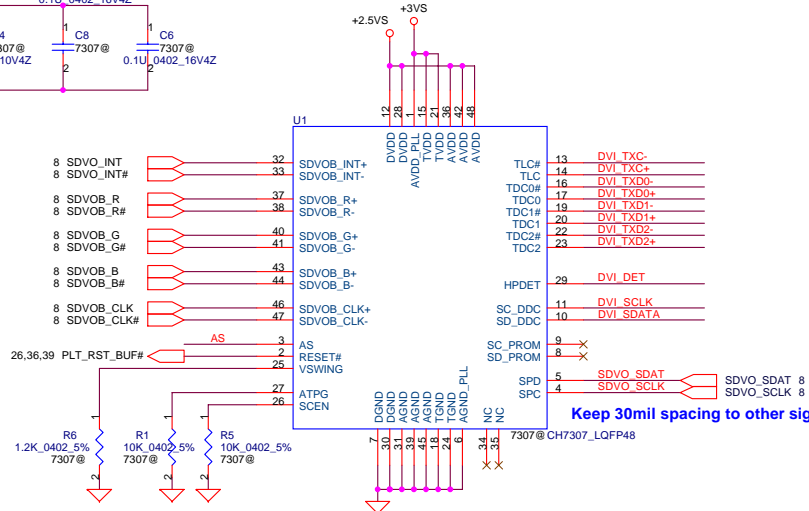
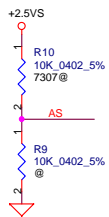
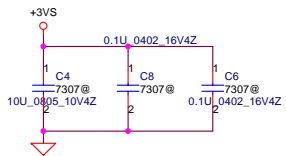
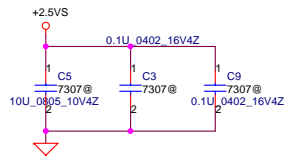
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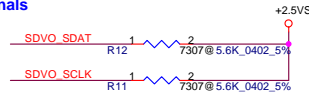
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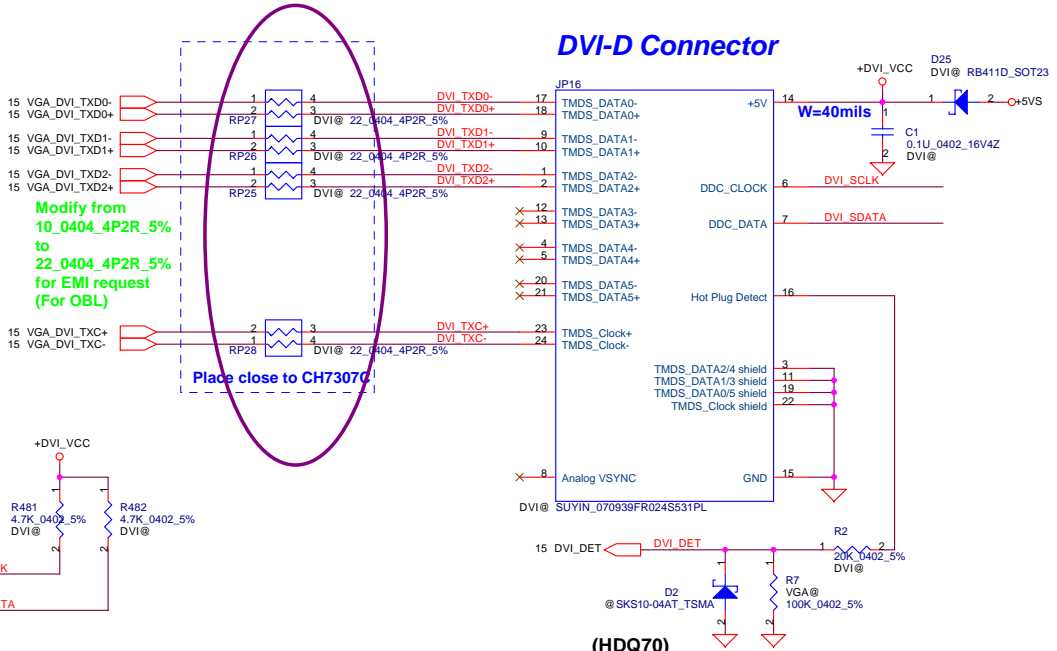
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BOM structure	DVI from SDVO	DVI from Discrete VGA
7307@	Stuff	No_Stuff
VGA@	No_Stuff	Stuff
@	No_Stuff	No_Stuff



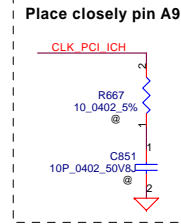
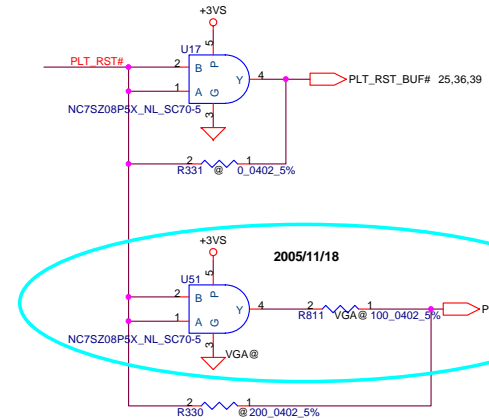
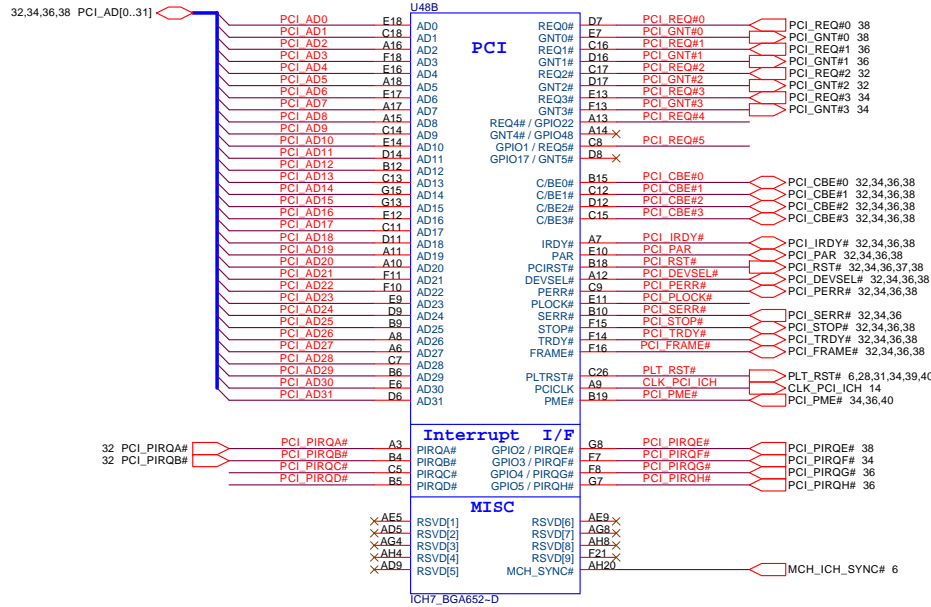
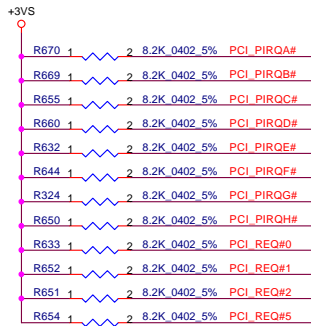
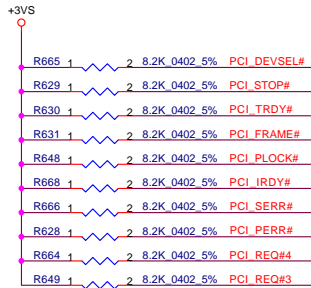
DVI-D Connector



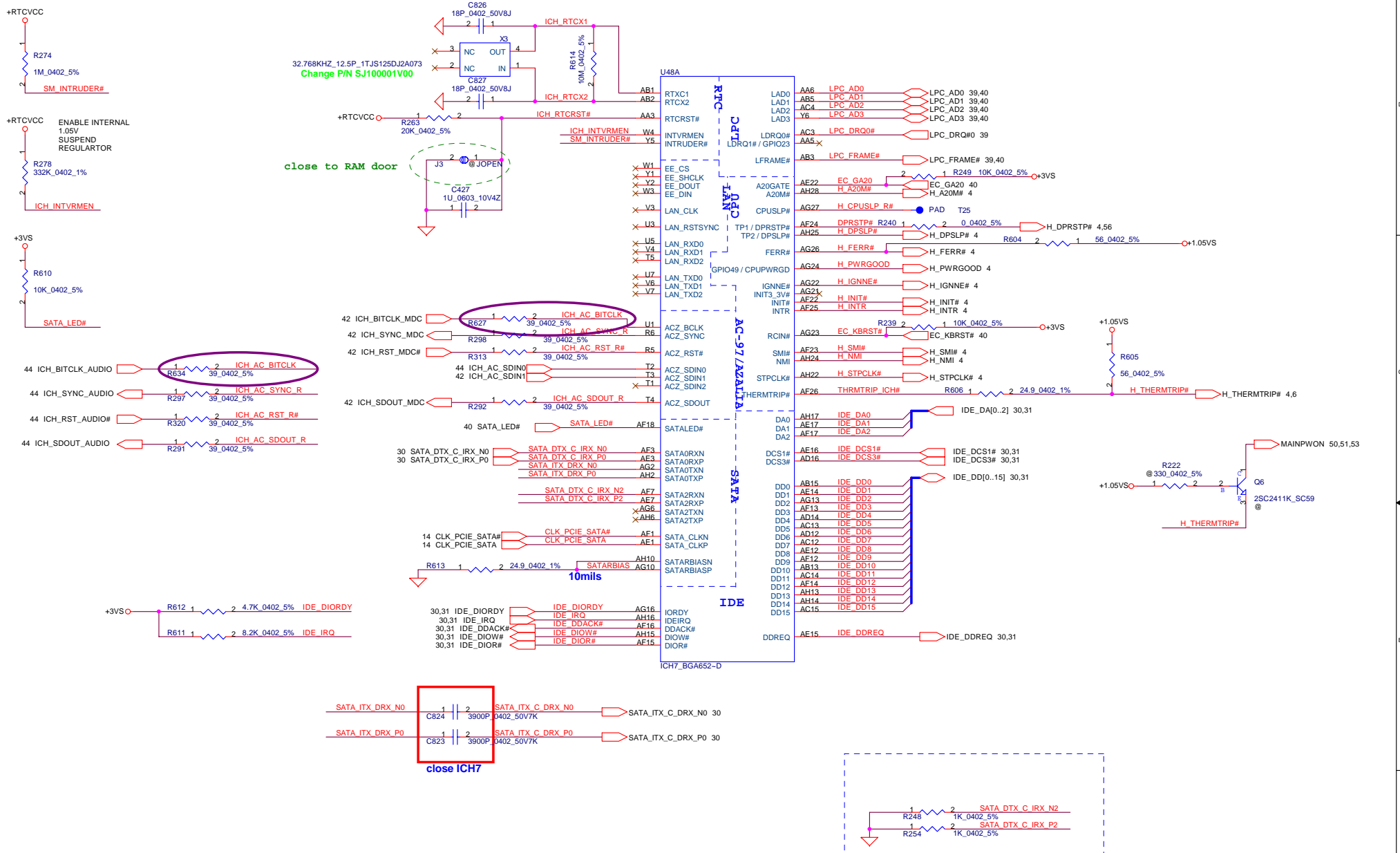
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ICH7M(SL8YB) [B-0]:SA0000V190 (ABO!)



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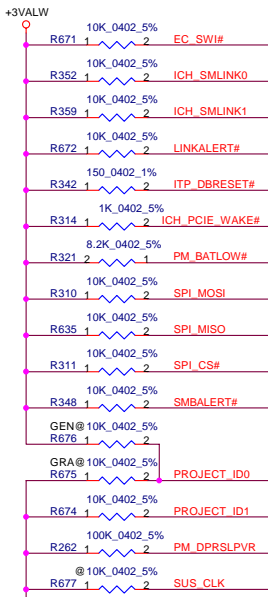
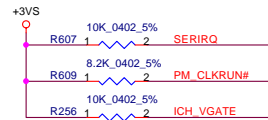


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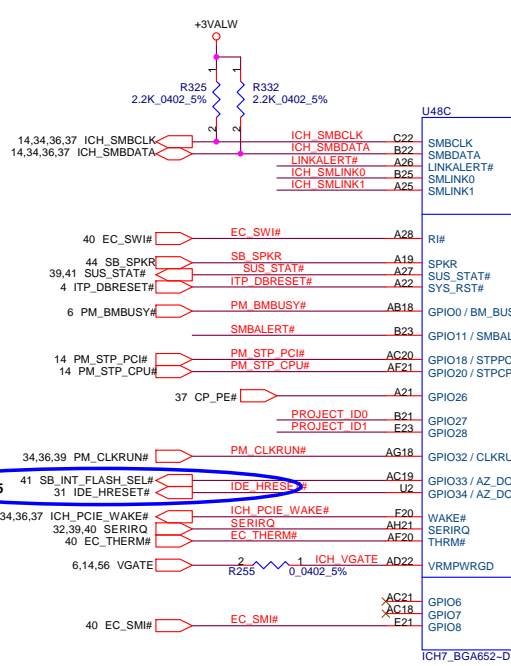
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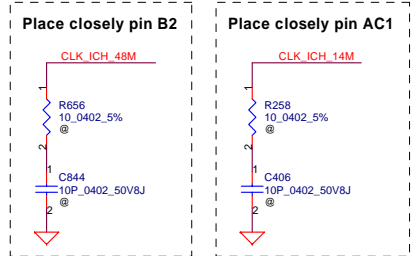
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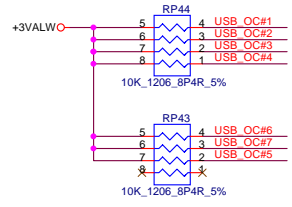
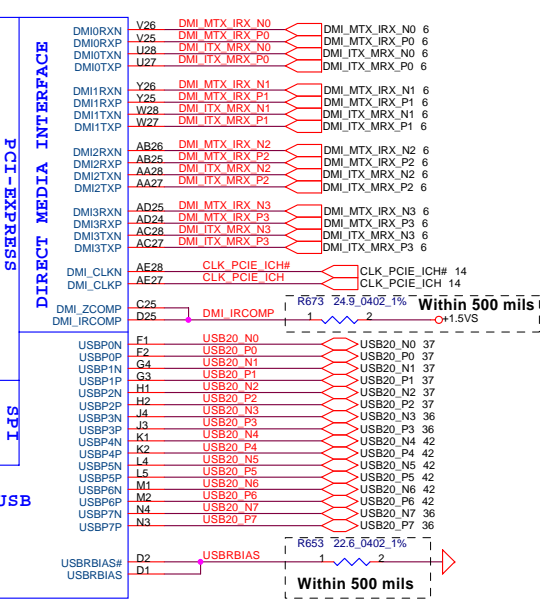
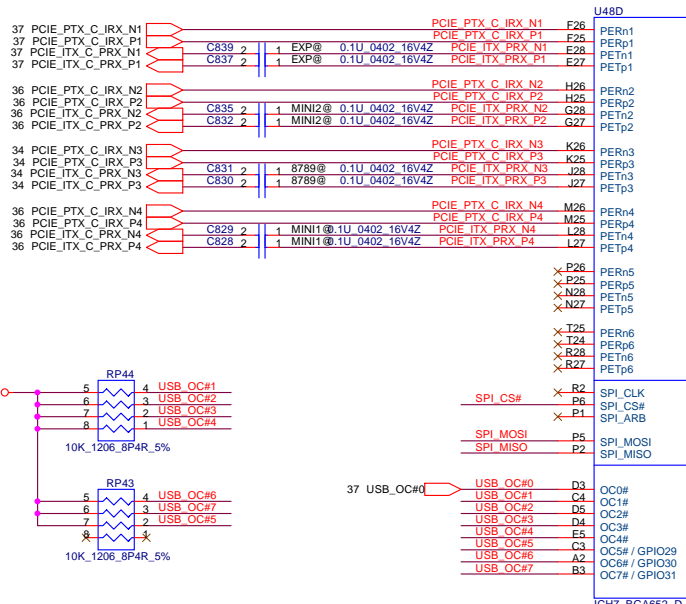
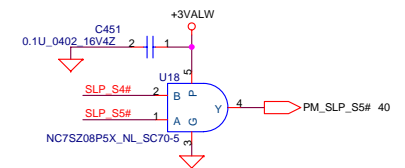
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01	= Geneva



Need update symbol



PM_DPRSPLVPR : Need to series a 500Ohm resistor to IMVP6

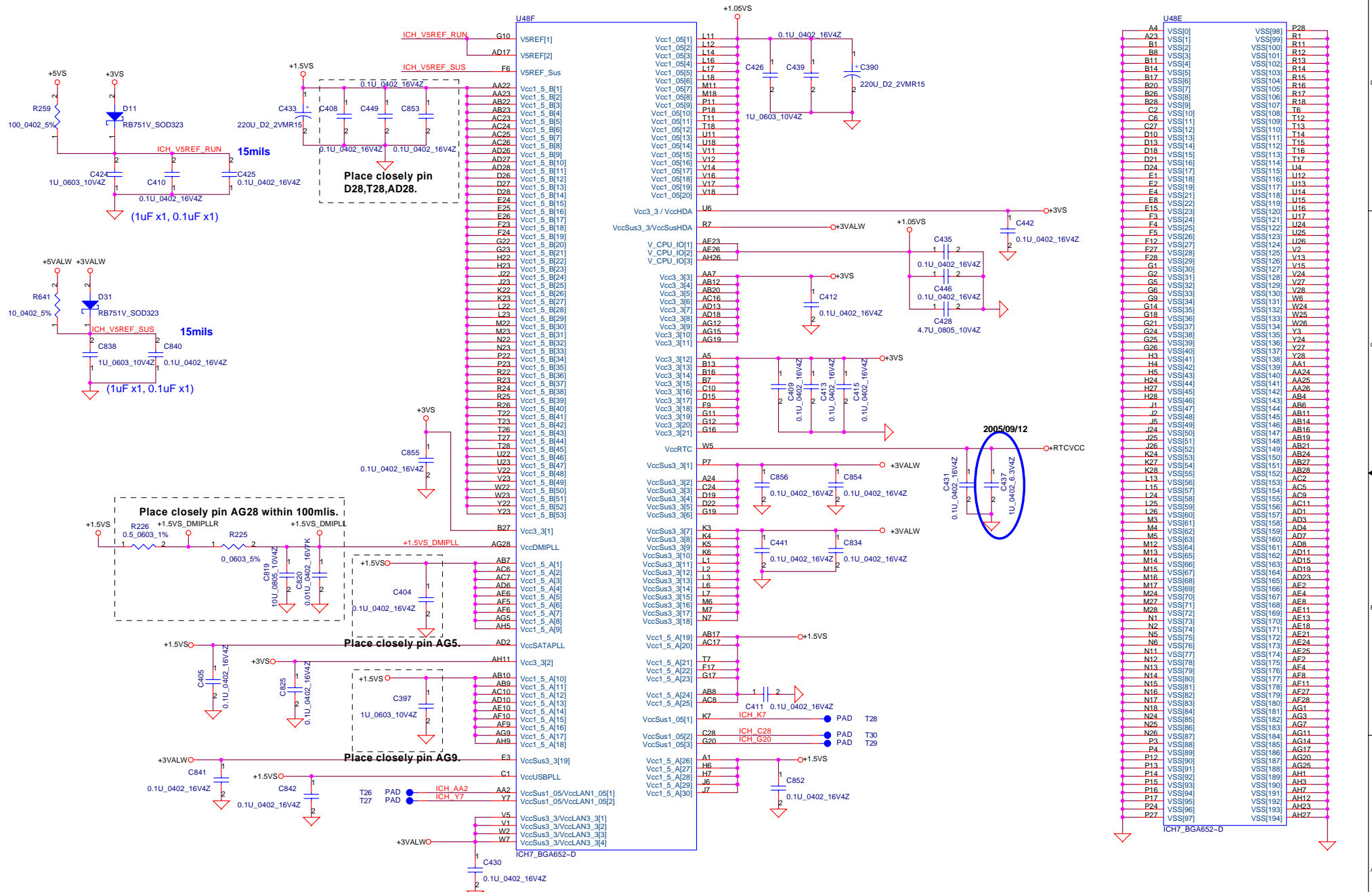


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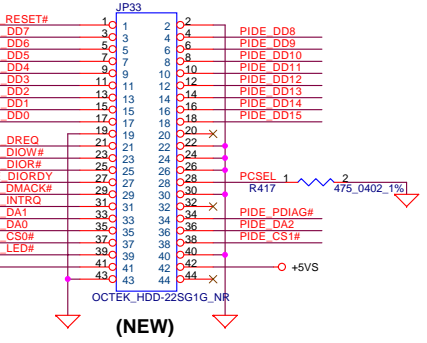
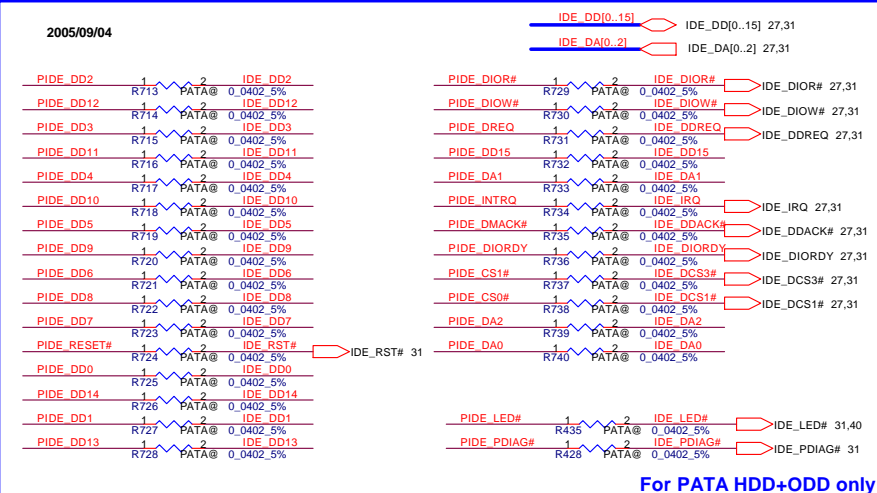
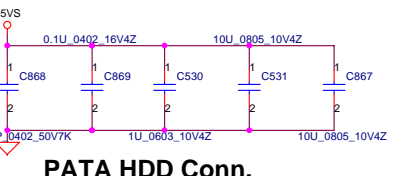
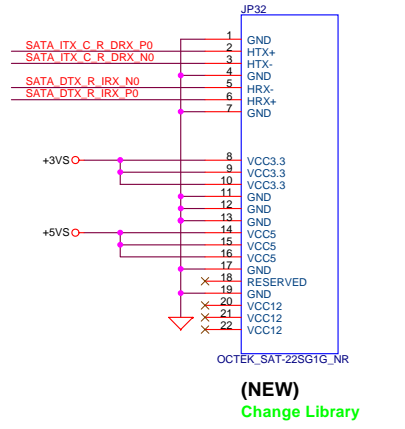
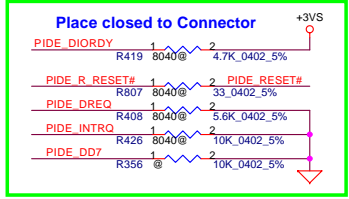
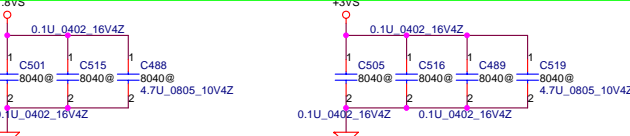
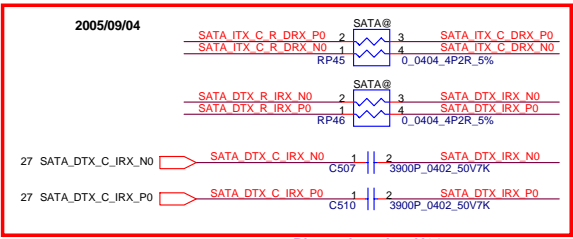
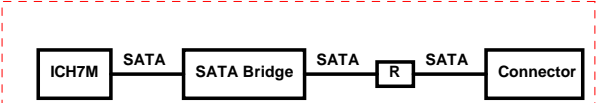
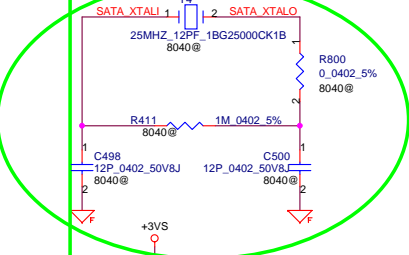
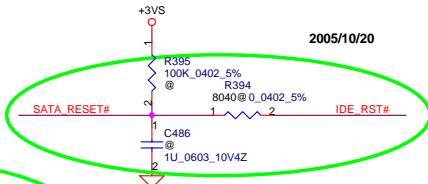
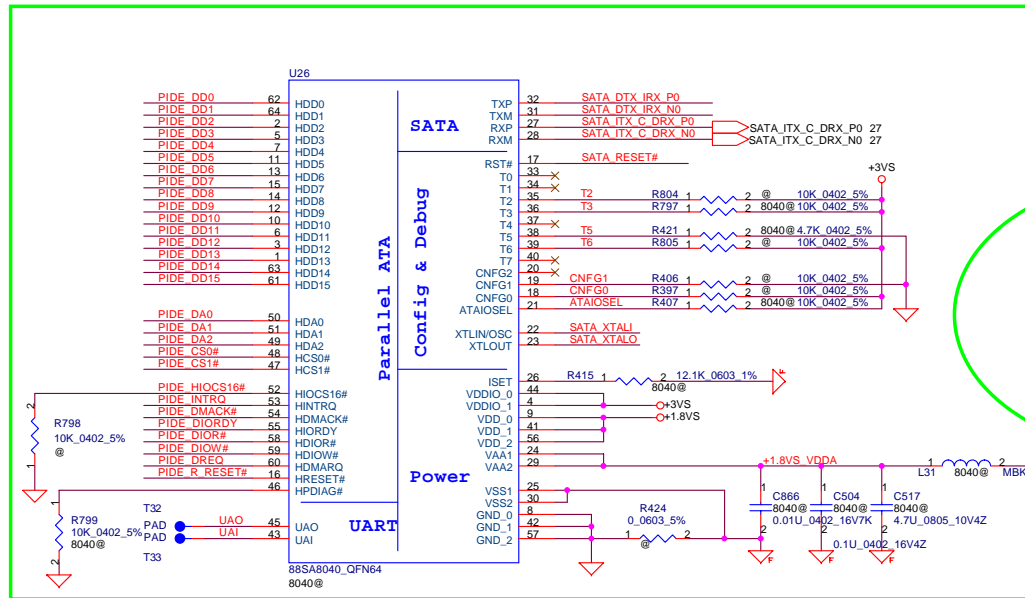
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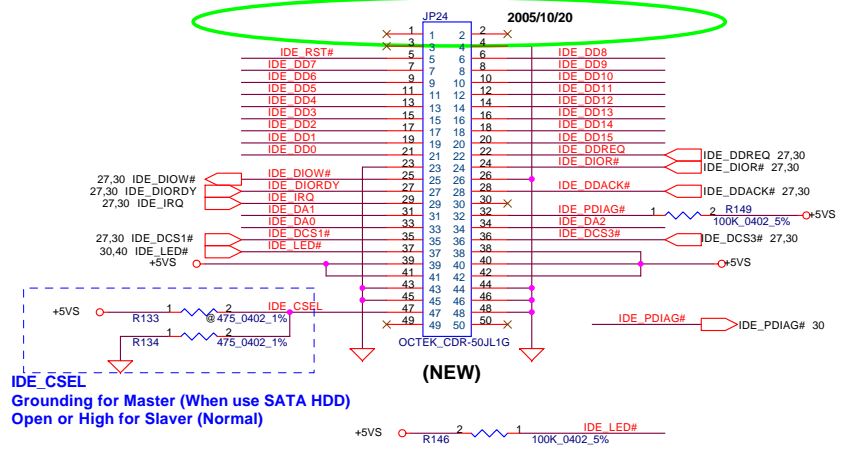
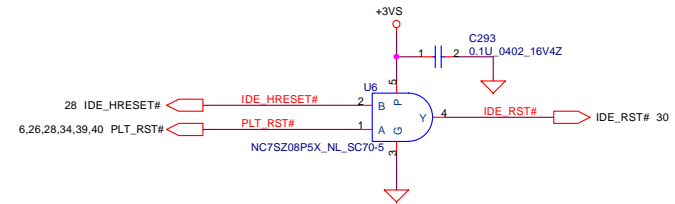
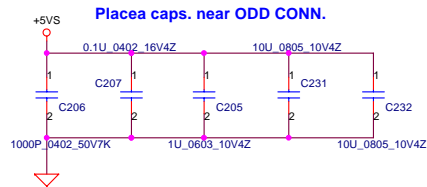
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SCHMATIC, M/B LA-2921P		
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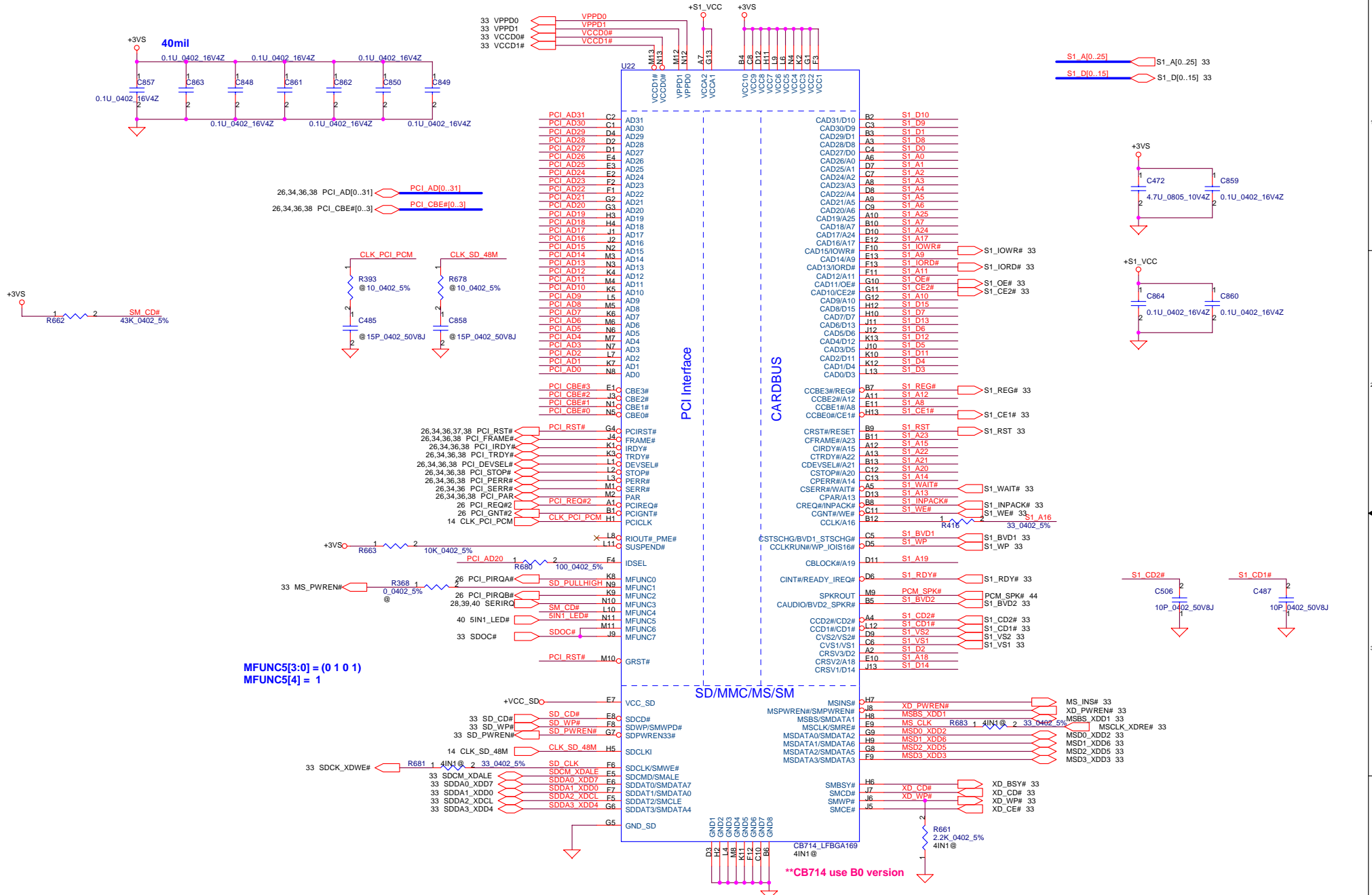
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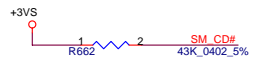
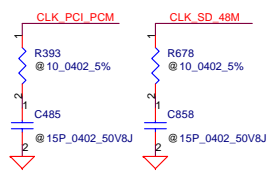
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26,34,36,38 PCI_AD[0..31] \leftrightarrow PCI_AD[0..31]
 26,34,36,38 PCI_CBE#[0..3] \leftrightarrow PCI_CBE#[0..3]



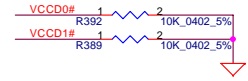
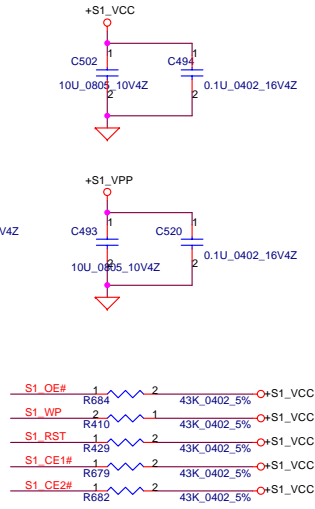
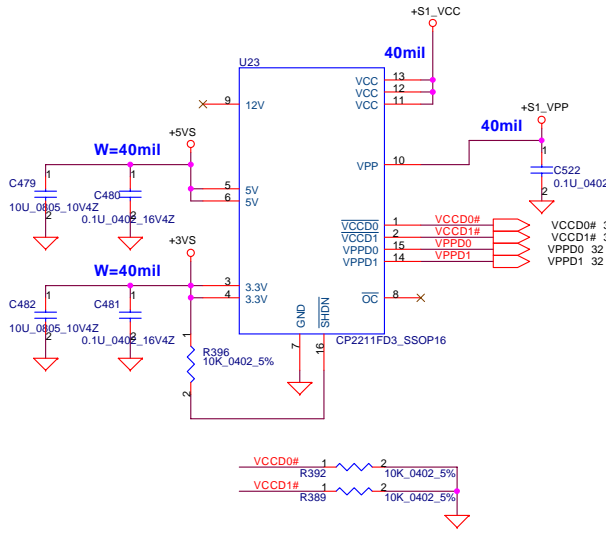
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CB1410 P/N: SA014100310

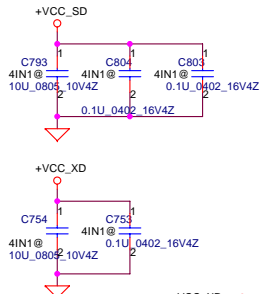
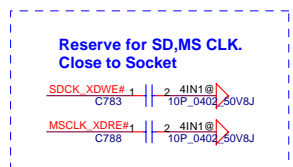
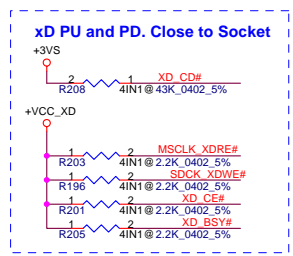
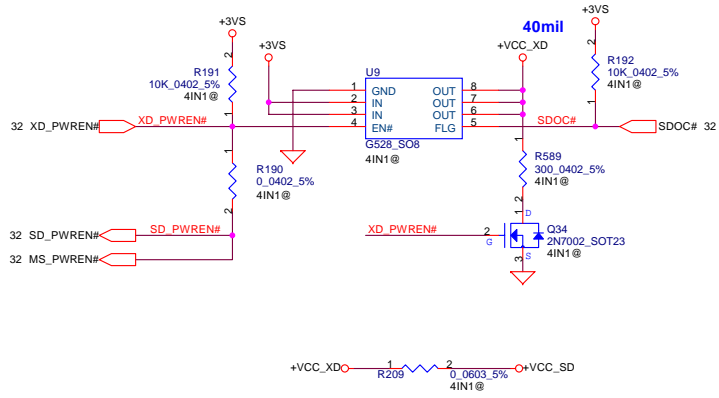
**CB714 use B0 version

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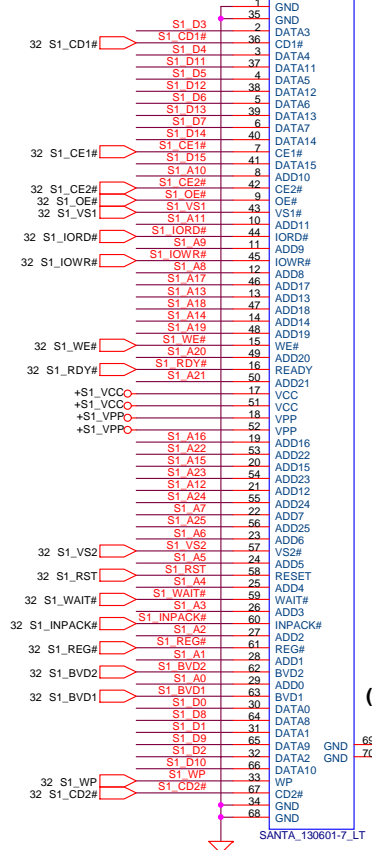
PCMCIA Power Control



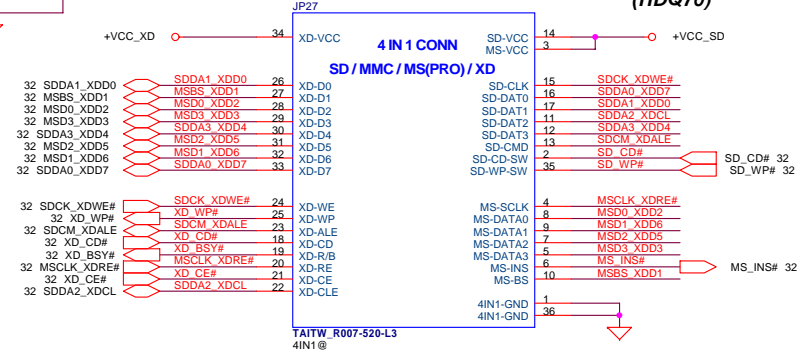
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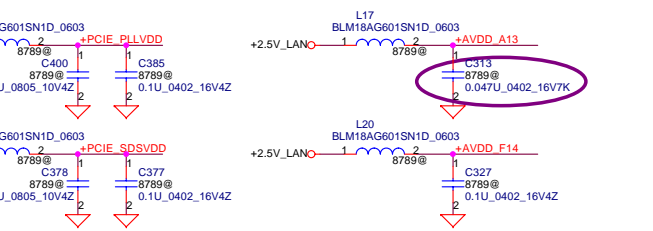
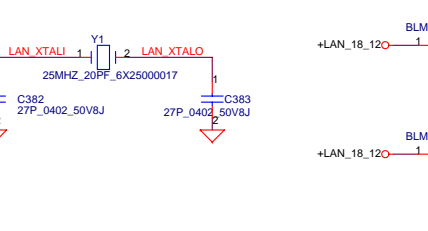
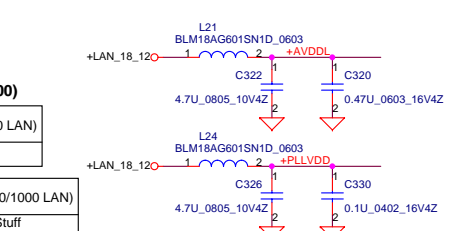
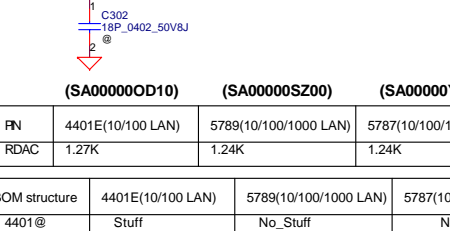
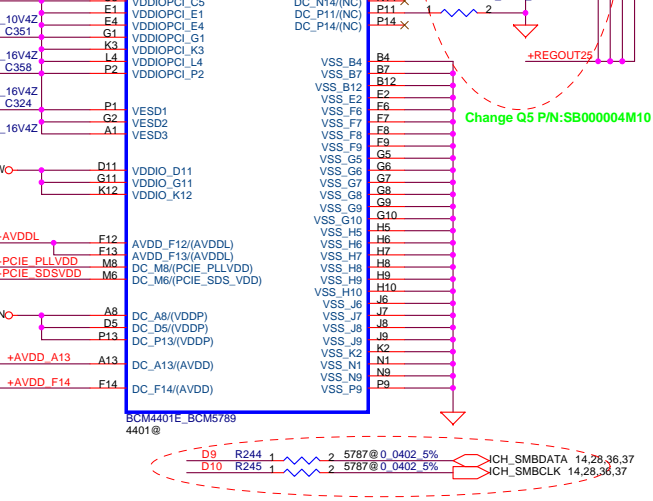
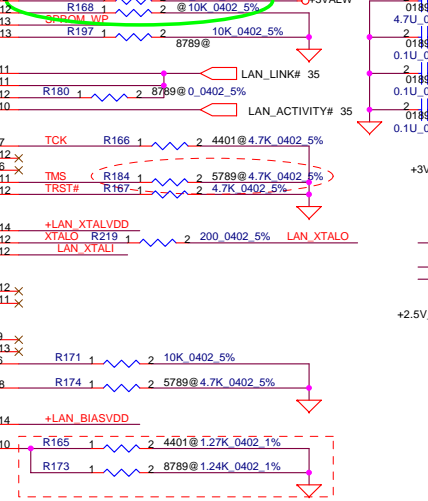
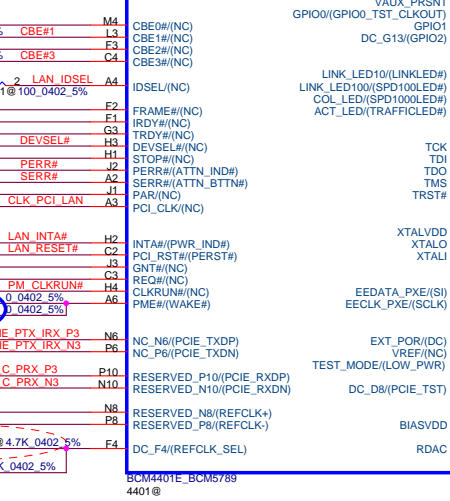
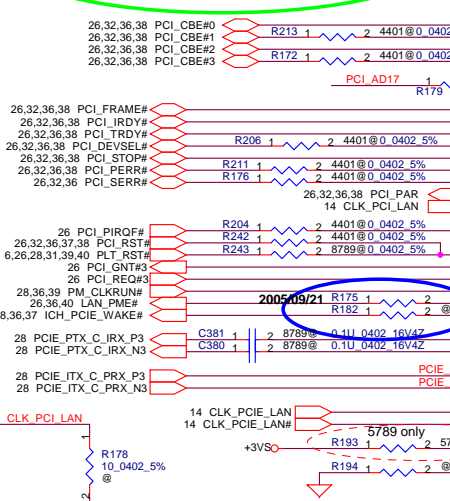
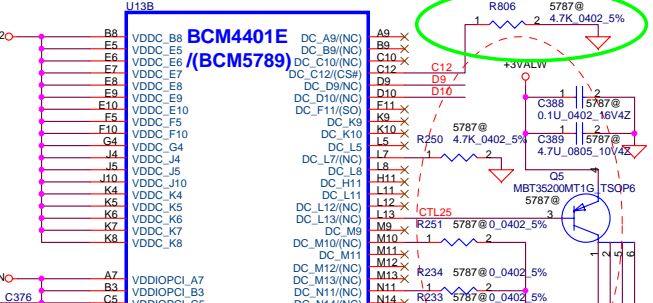
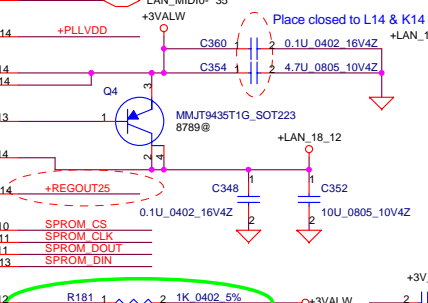
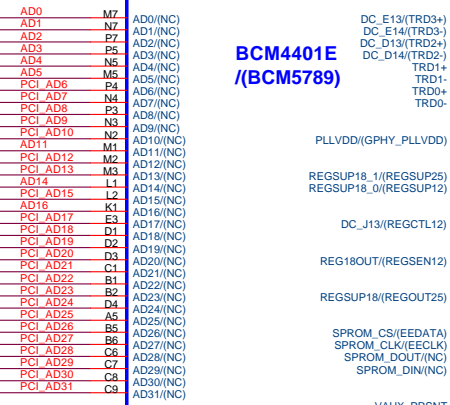
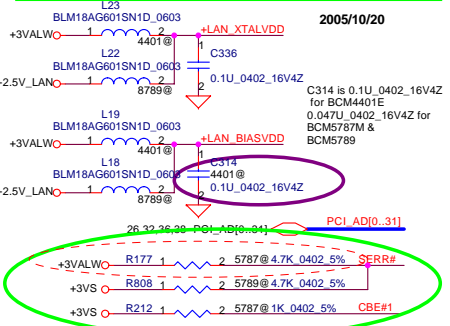
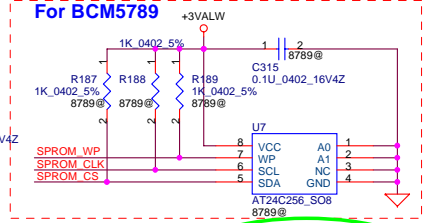
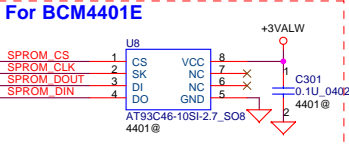
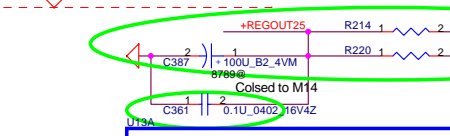
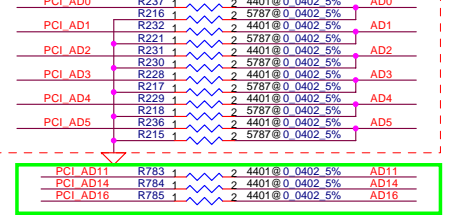
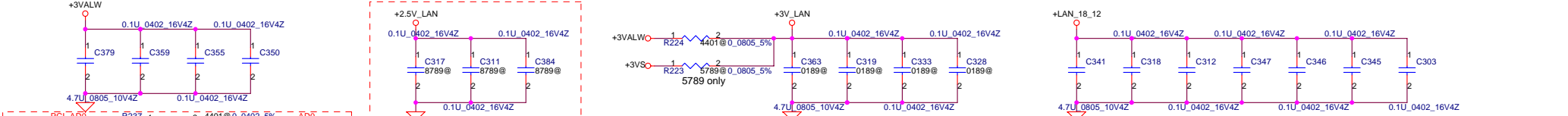
PCMCIA Socket



4 IN 1 Socket (HDQ70)



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	(SA00000D10)	(SA00000SZ00)	(SA00000YJ00)
FN	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
RDAC	1.27K	1.24K	1.24K

BOM structure	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
4401@	Stuff	No_Stuff	No_Stuff
5789@	No_Stuff	Stuff	No_Stuff
5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

Security Classification	Compal Secret Data	
Issued Date	2006/10/4	Deciphered Date
		2007/10/4

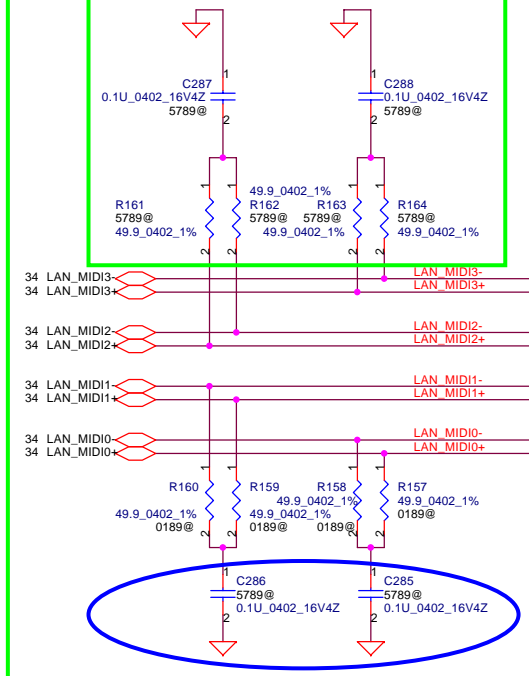
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LAN BCM4401E/ BCM5789

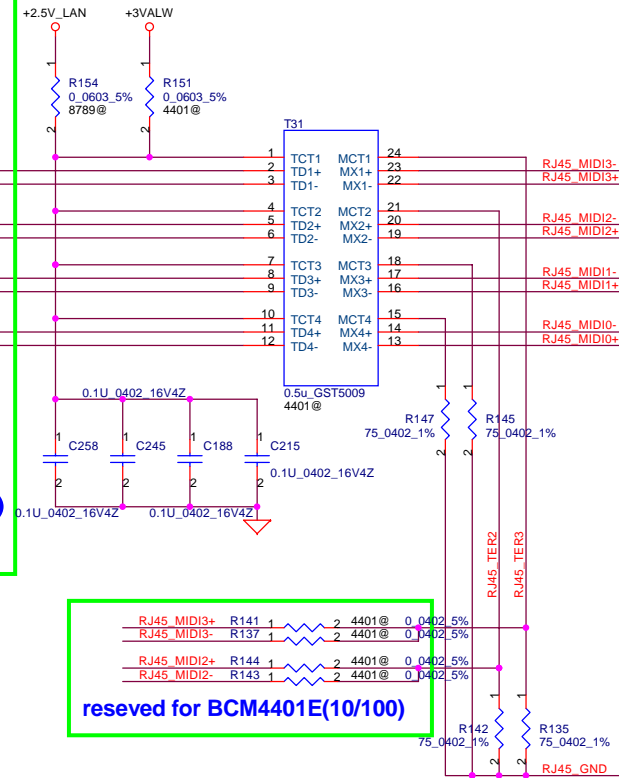
Place these components colsed to LAN chip

unpop when use BCM4401E(10/100)

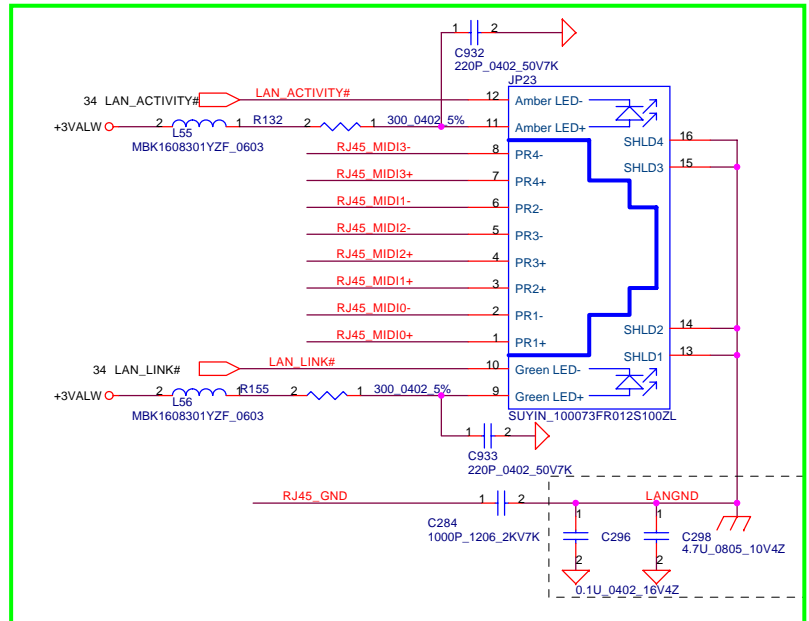


C285, C286 is 0.1uF for BCM5789.
C285, C286 is 0.01uF for BCM4401E.

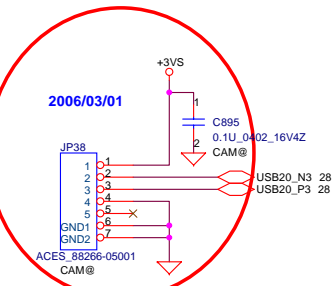
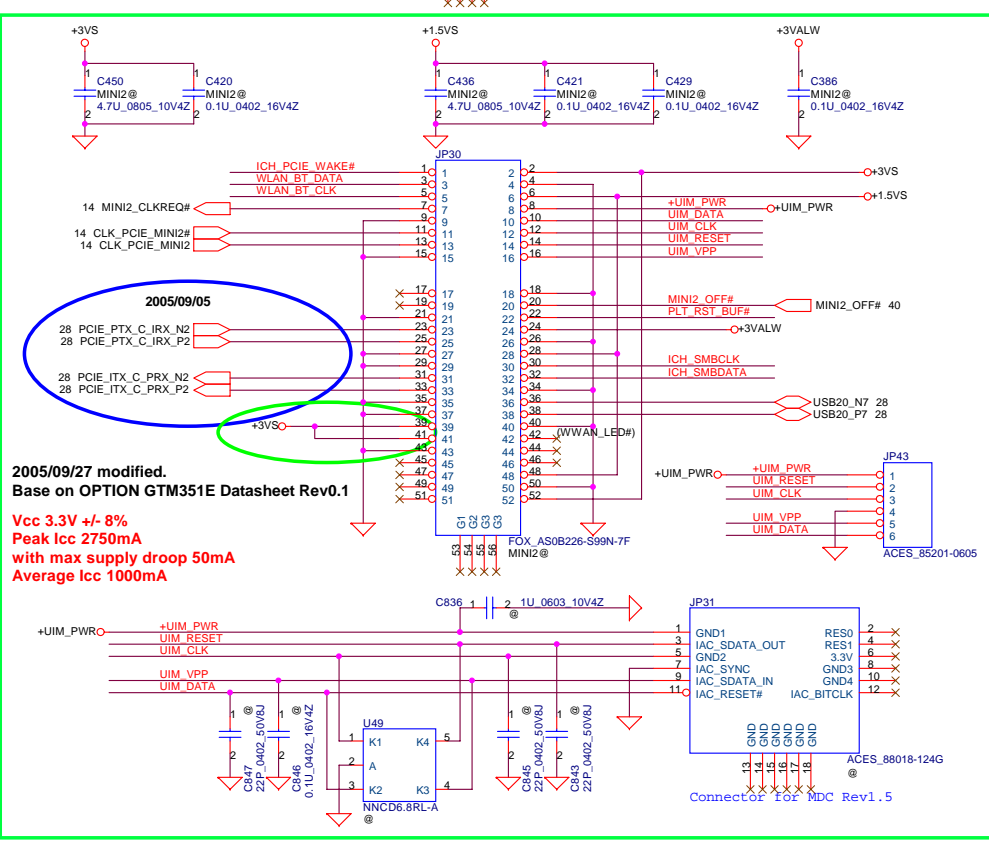
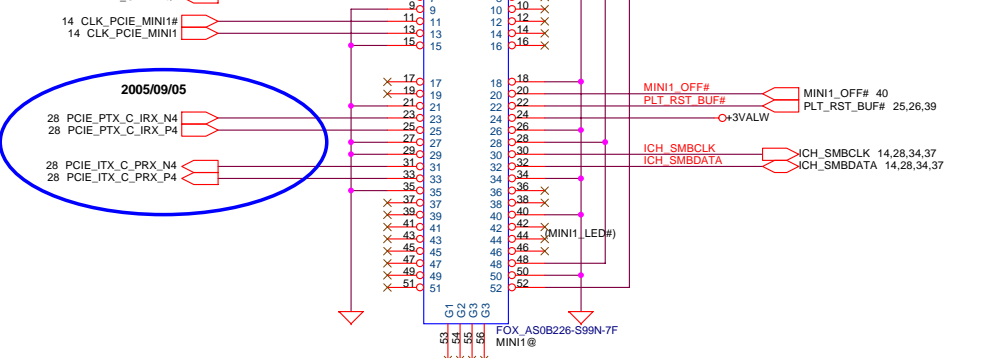
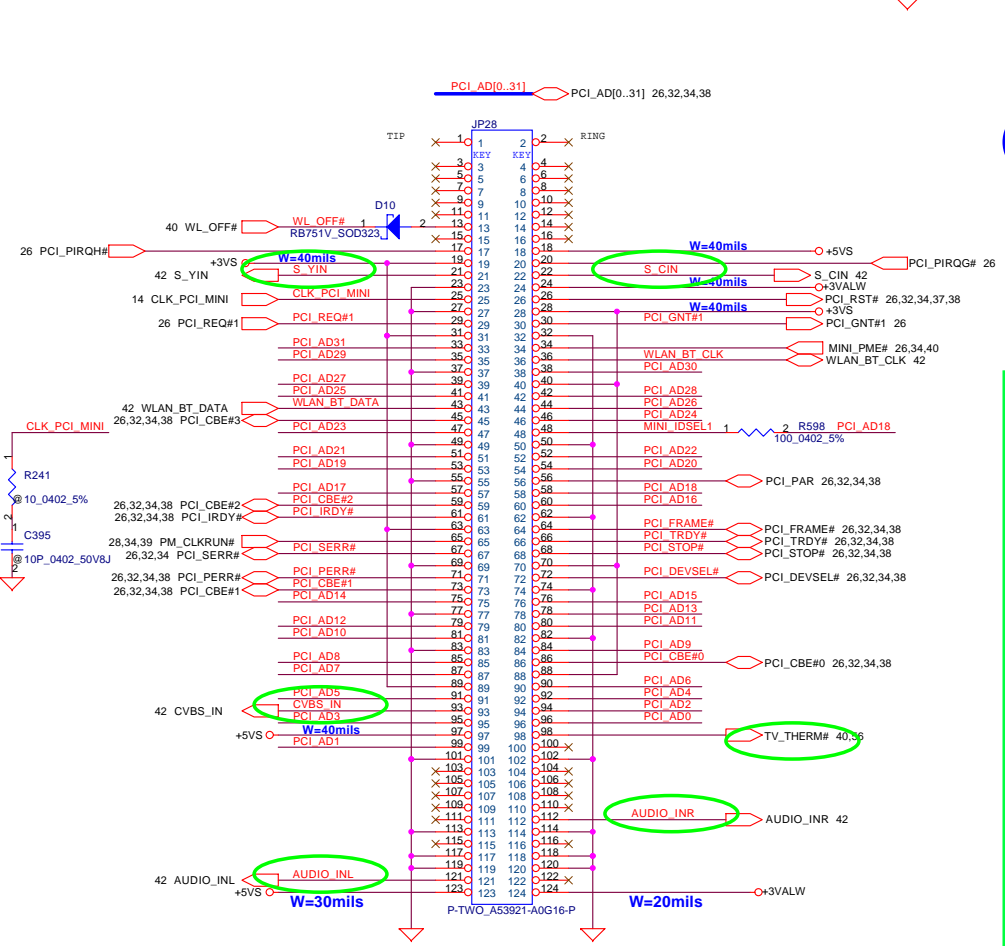
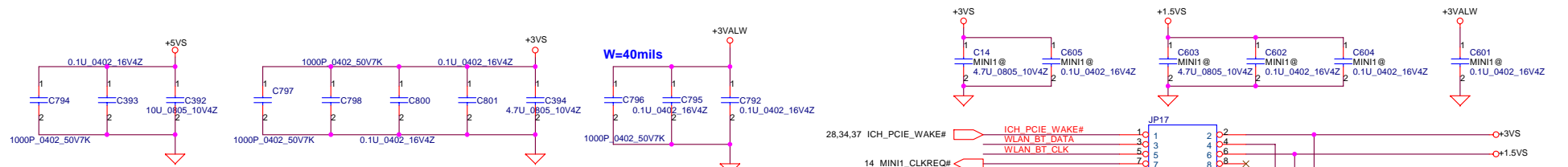
GbE Transformer: GST5009 (SP050005610)
10/100 Transformer : TST1284-LF (SP050001X10)



RJ45_MIDI3+ R141 1 2 4401@ 0.0402 5%
RJ45_MIDI3- R137 1 2 4401@ 0.0402 5%
RJ45_MIDI2+ R144 1 2 4401@ 0.0402 5%
RJ45_MIDI2- R143 1 2 4401@ 0.0402 5%
revised for BCM4401E(10/100)

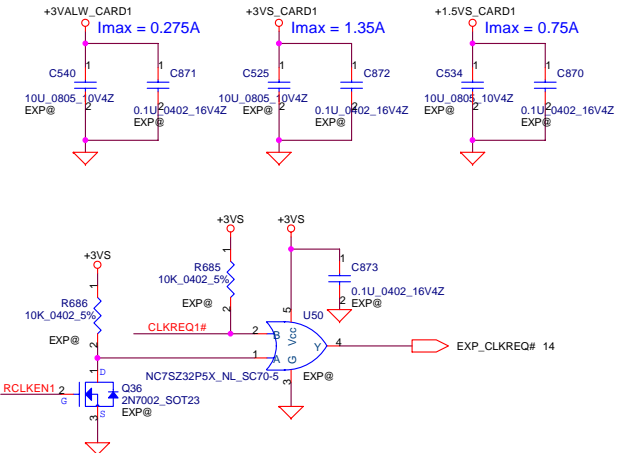
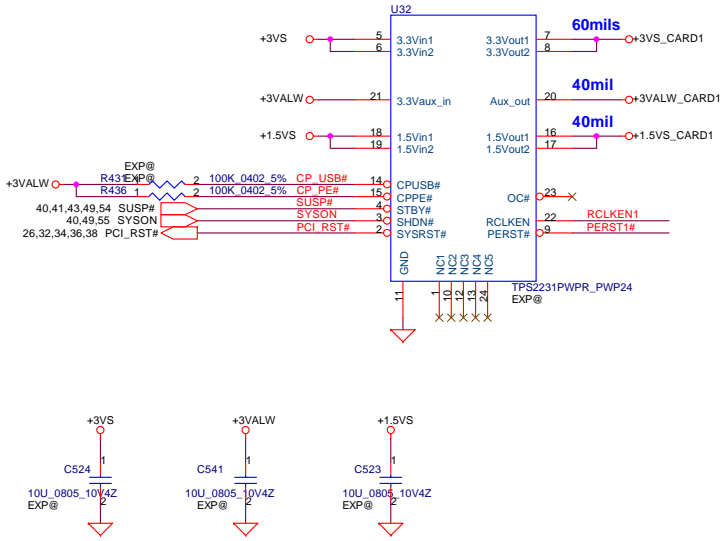


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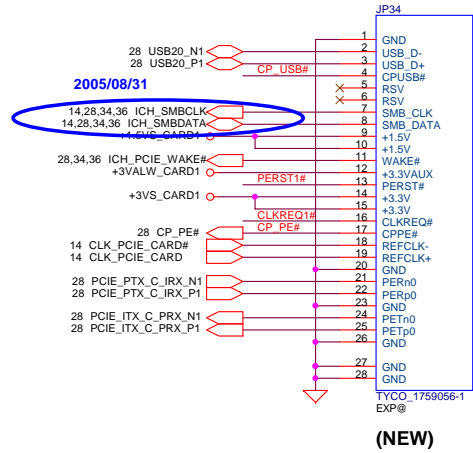


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

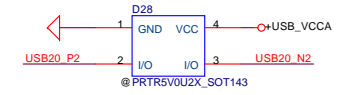
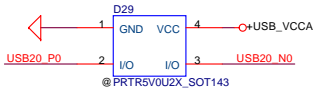
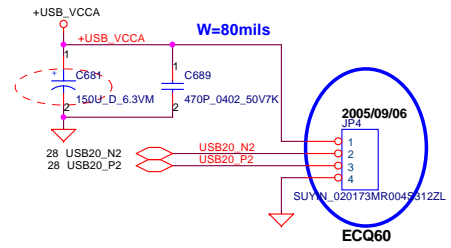
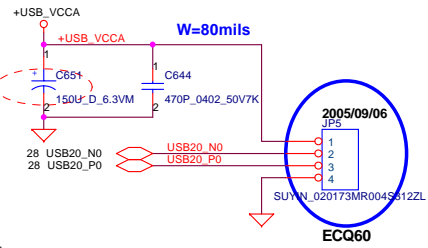
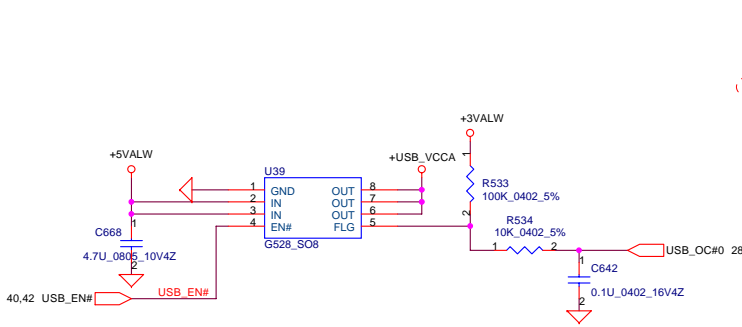
New Card Power Switch



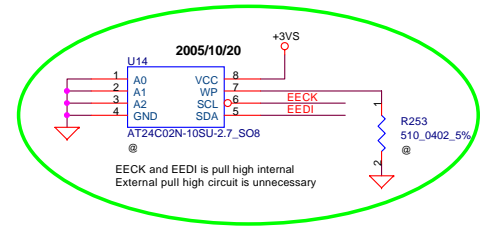
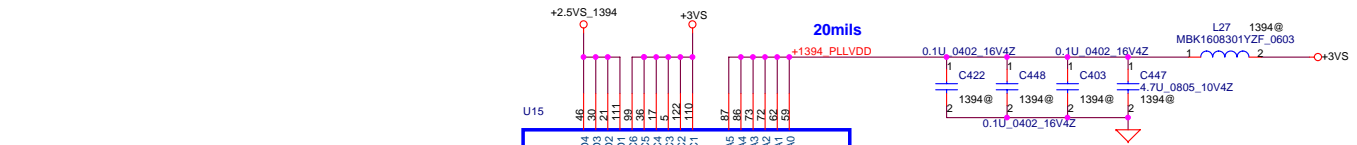
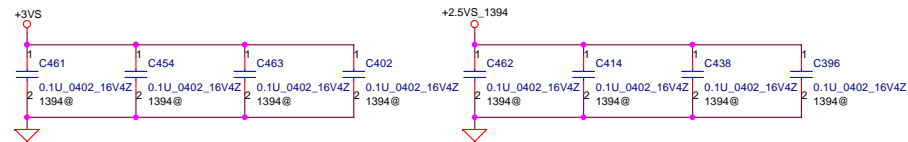
New Card Socket (Left)



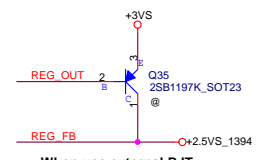
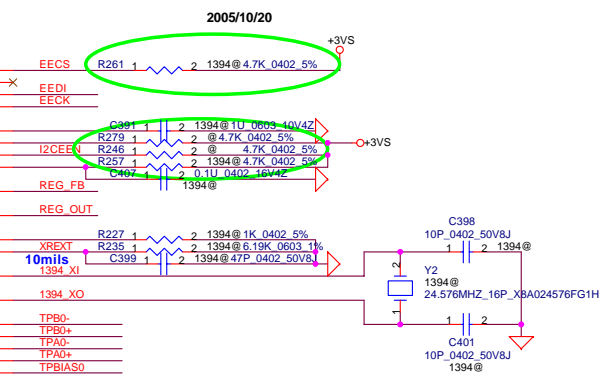
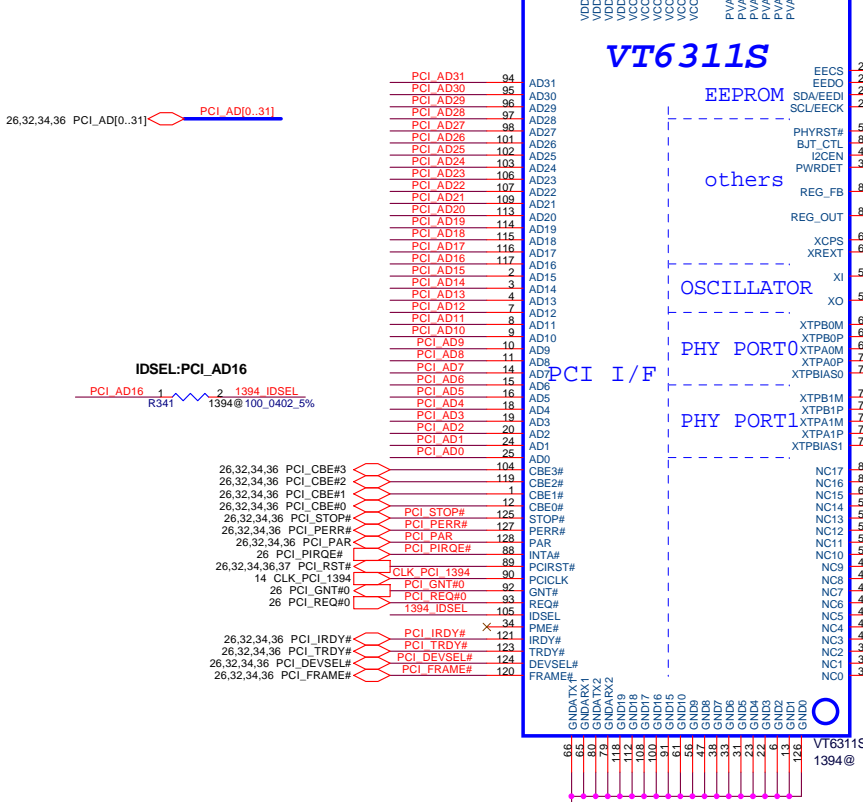
USB CONN. 1 & 2



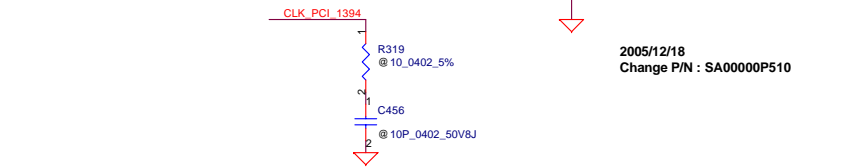
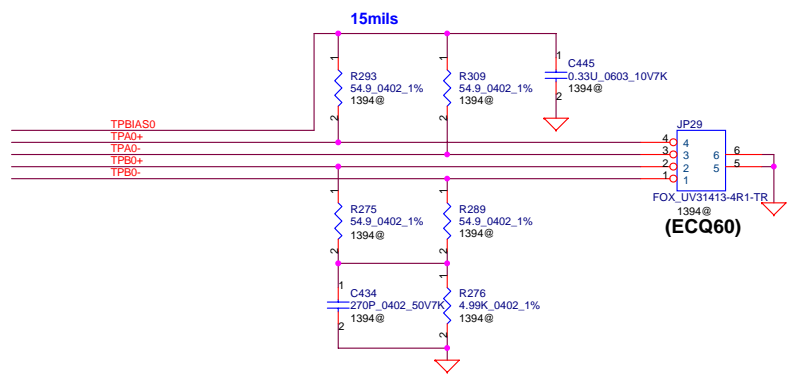
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When use external EEPROM
Populate U14, R246, R253
Un-populate R261



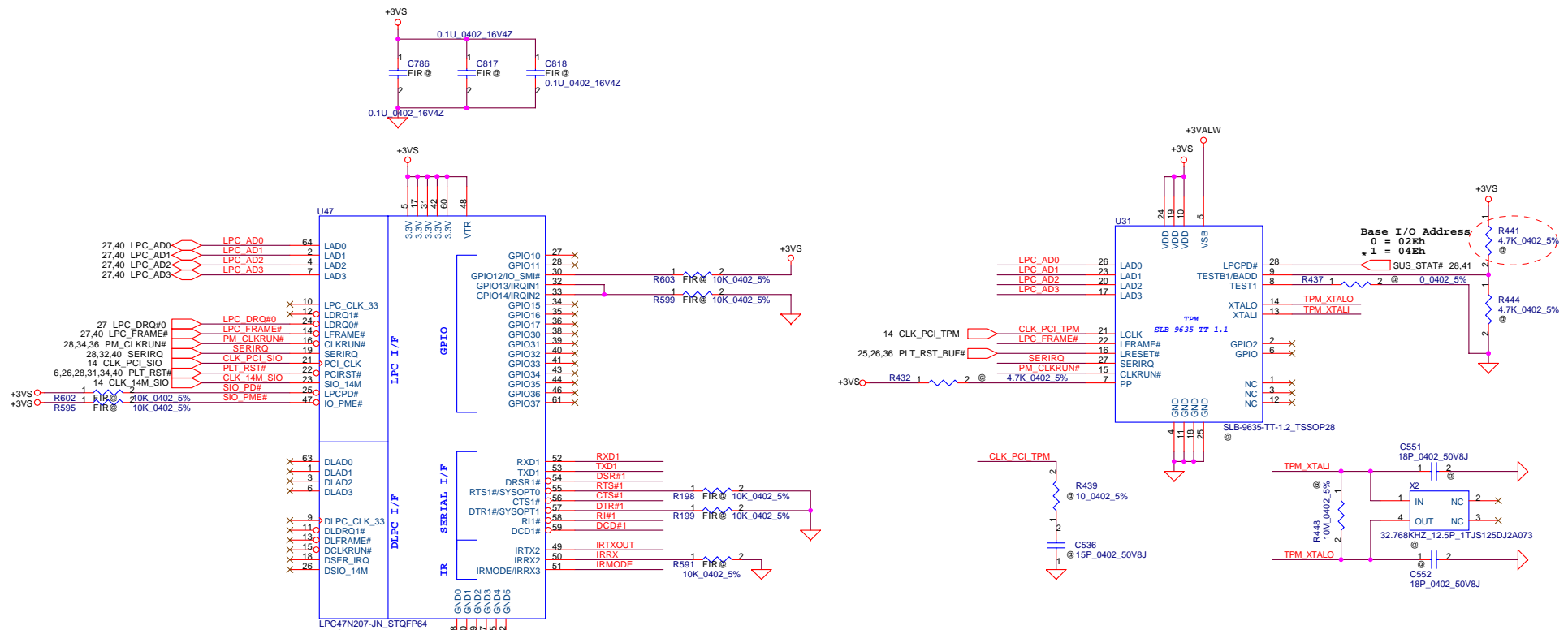
When use external BJT
Populate Q35, R279



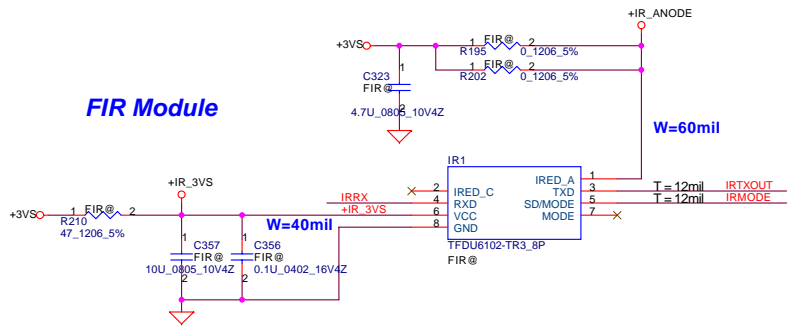
2005/12/18
Change P/N : SA00000P510

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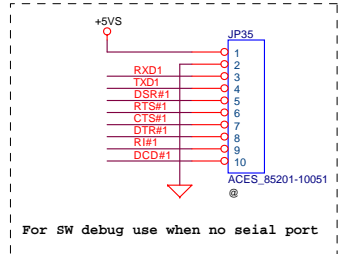
SUPER I/O SMsC LPC47N207



FIR Module

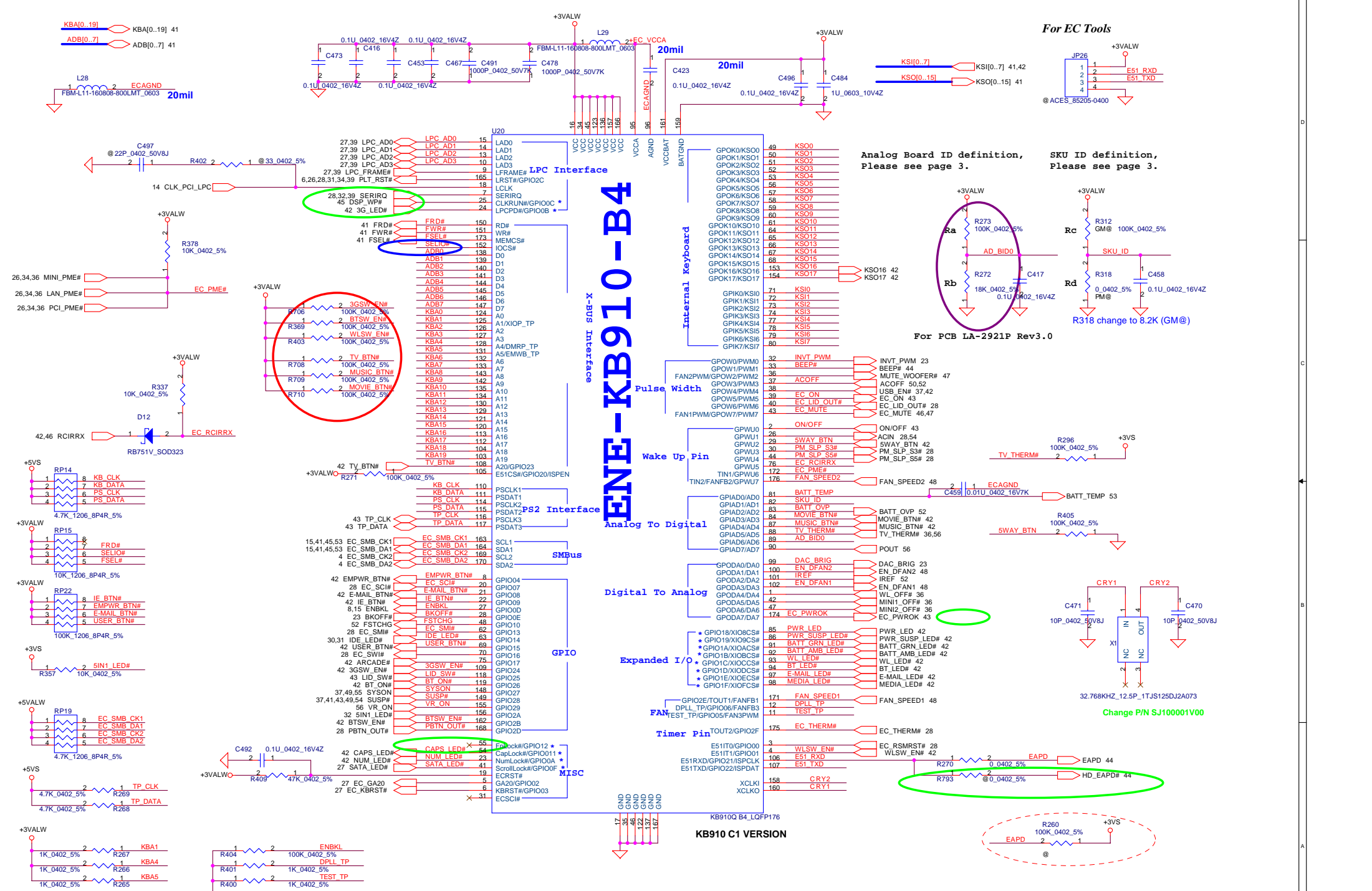


Place on the BOT side (near MINIPCI conn.)

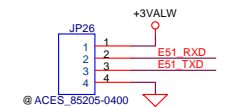


For SW debug use when no seial port

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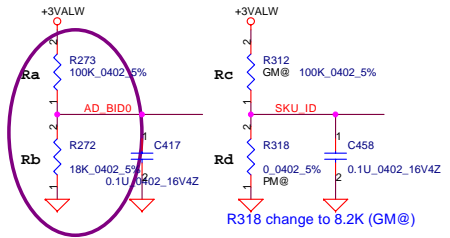


For EC Tools



Analog Board ID definition, Please see page 3.

SKU ID definition, Please see page 3.



For PCB LA-2921P Rev3.0

ENE-KB910-B4

X-USB Interface

Pulse Width

Wake Up Pin

Analog To Digital

Digital To Analog

Expanded I/O

FAN

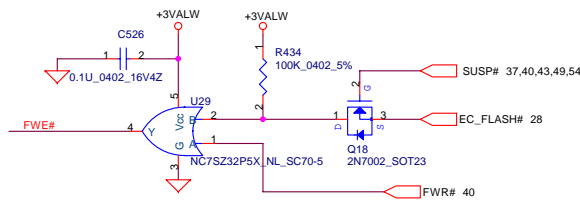
Timer Pin

MISC

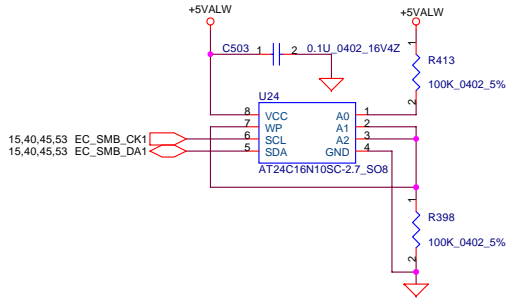
Internal Keyboard

KB910 C1 VERSION

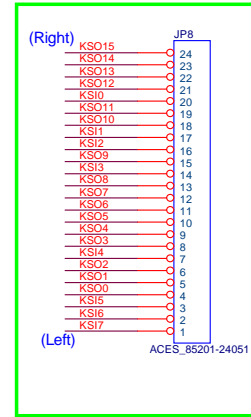
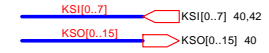
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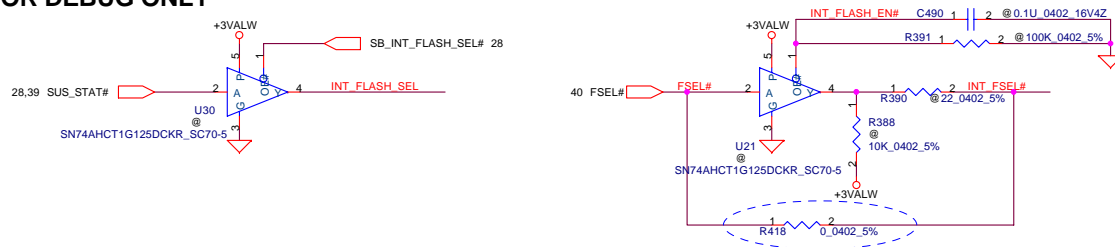
Check PCB Footprint



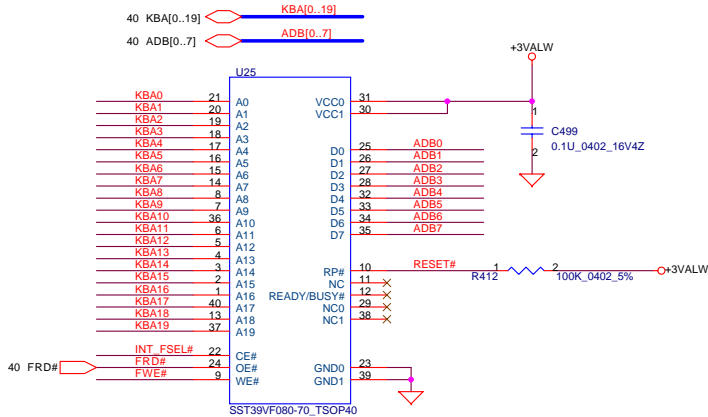
INT_KBD Conn.



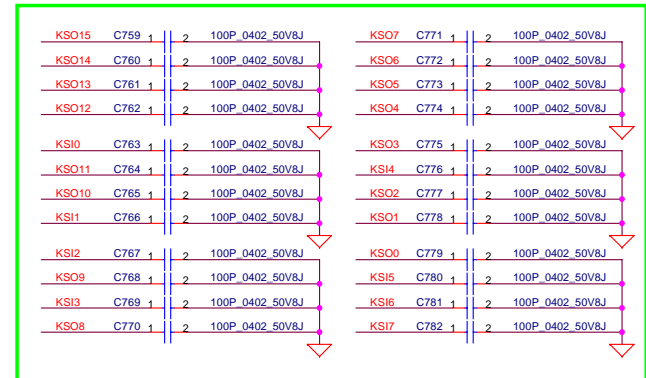
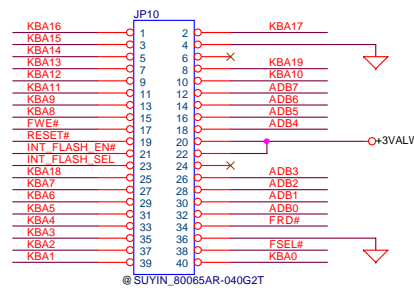
FOR DEBUG ONLY



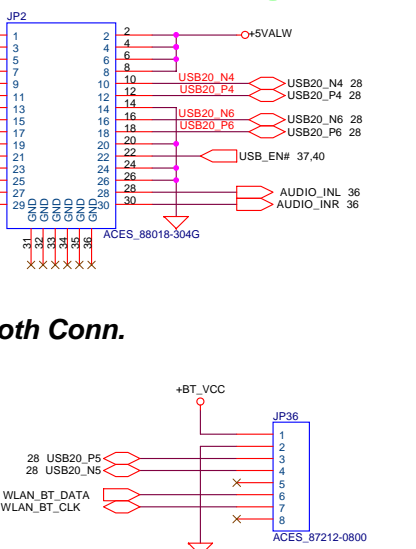
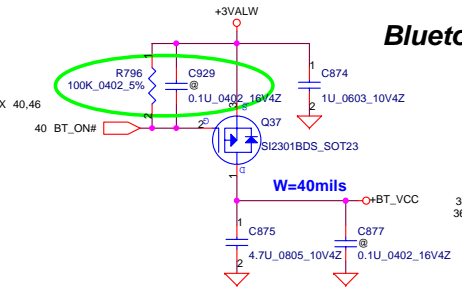
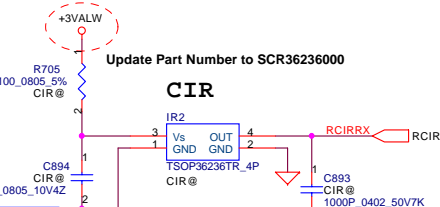
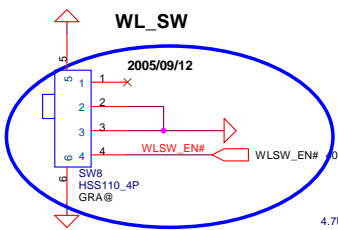
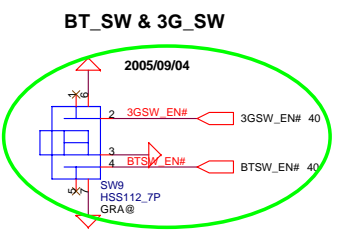
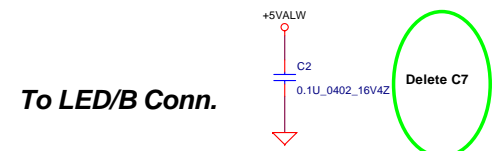
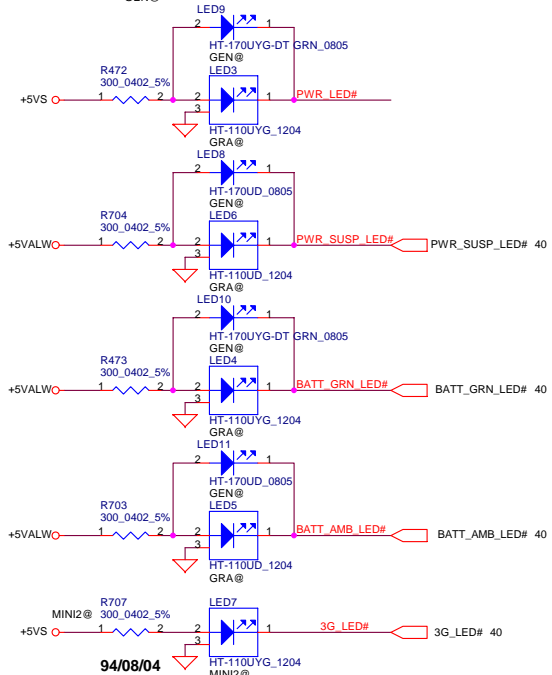
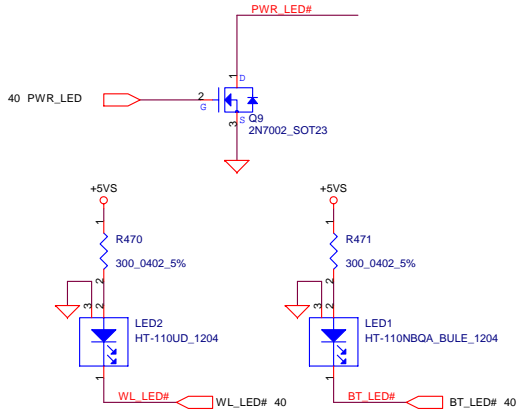
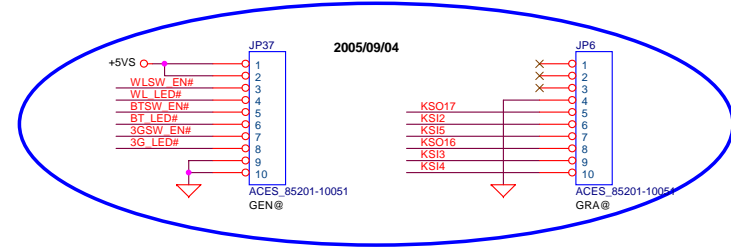
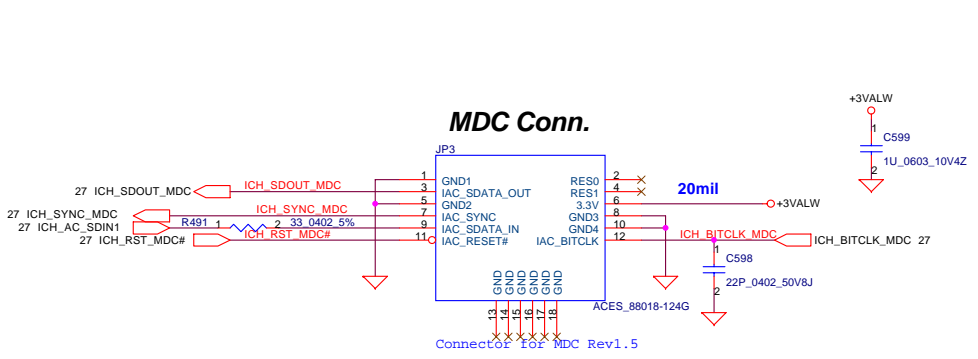
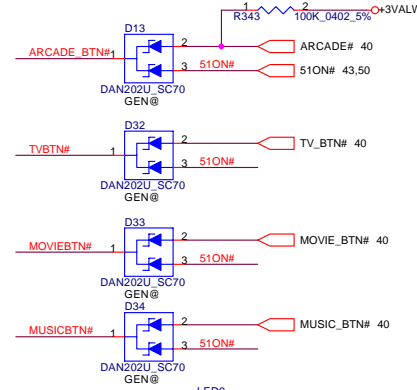
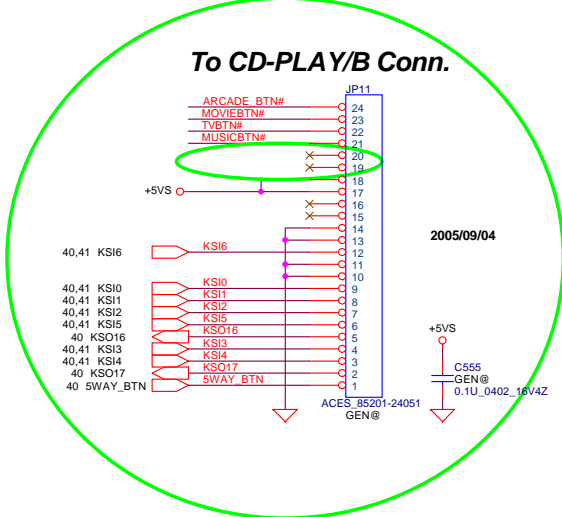
1MB Flash ROM



1MB ROM Socket

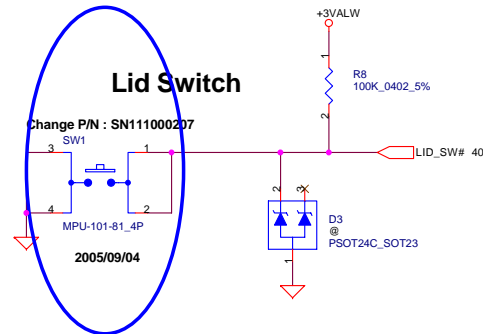
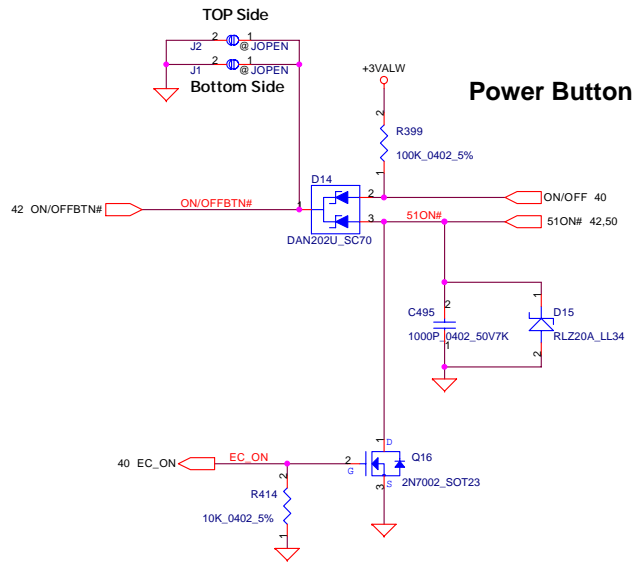


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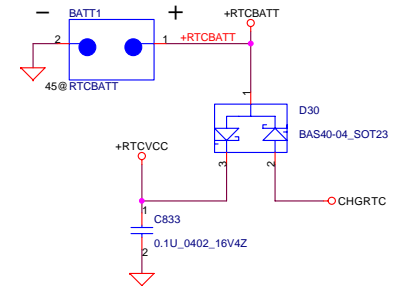
Geneva		Grapevine	
KSO10	KSO16	KSO16	KSO17
	VOL_UP		
KSI1	KSO17		
	VOL_RIGHT		
KSI2		KSI2	PLAY
	RIGHT	KSI3	STOP
KSI3	PLAY	KSI4	NEXT
	ENTER	KSI5	REV
KSI4	STOP		
	VOL_DOWN		
KSI5	NEXT		
	ENTER		
KSI6	REV		
	RECORD		

ON/OFF switch

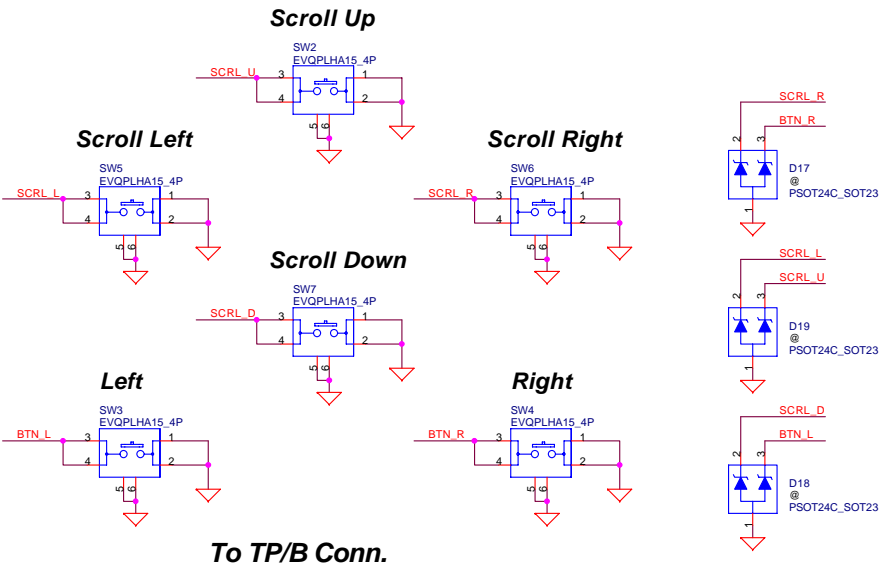
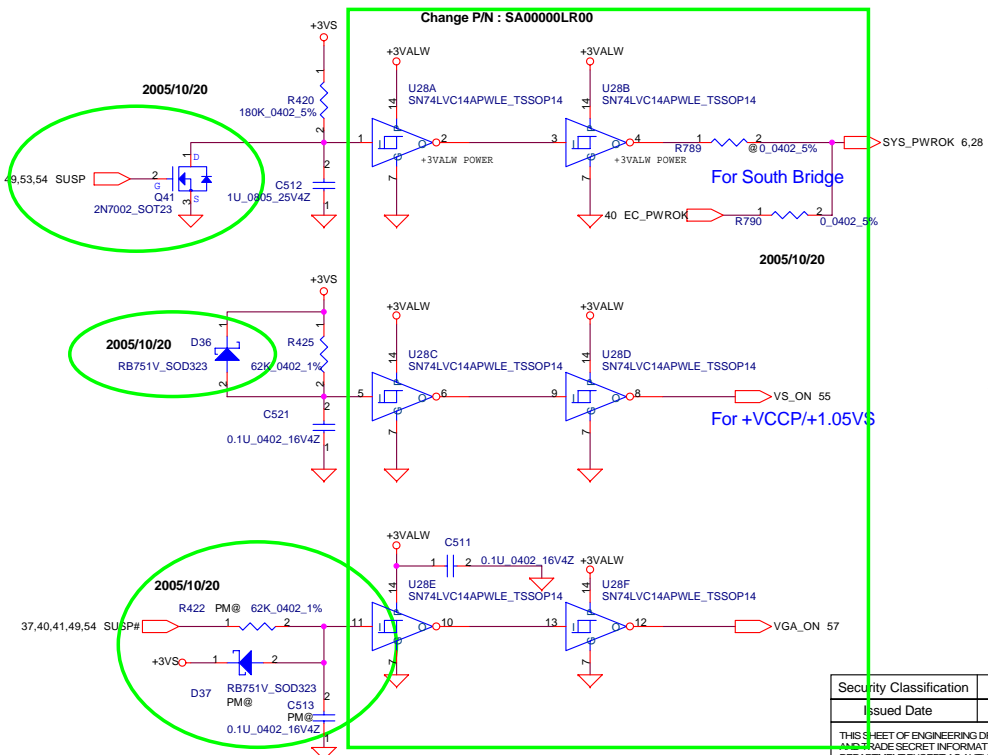


Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

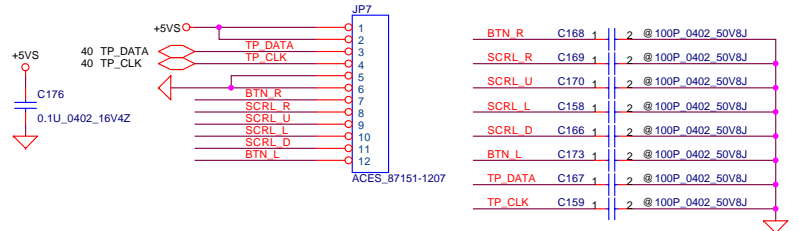
RTC Battery



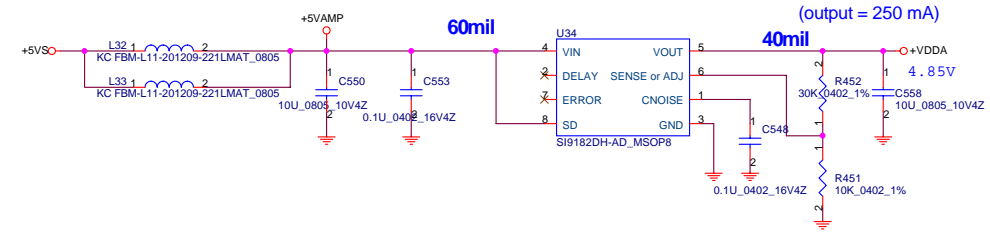
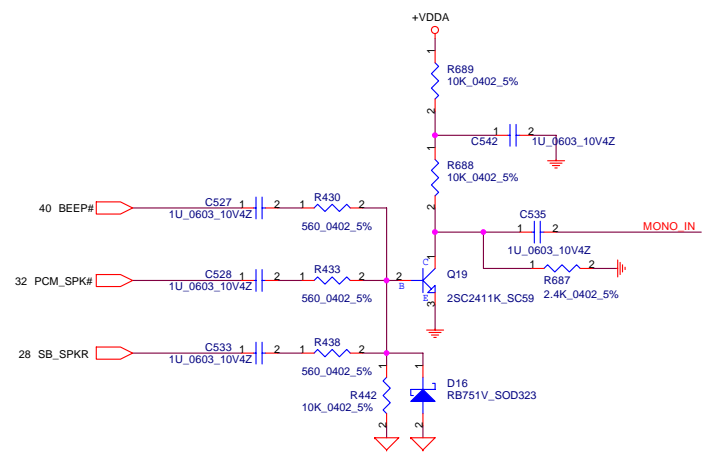
Power ON Circuit



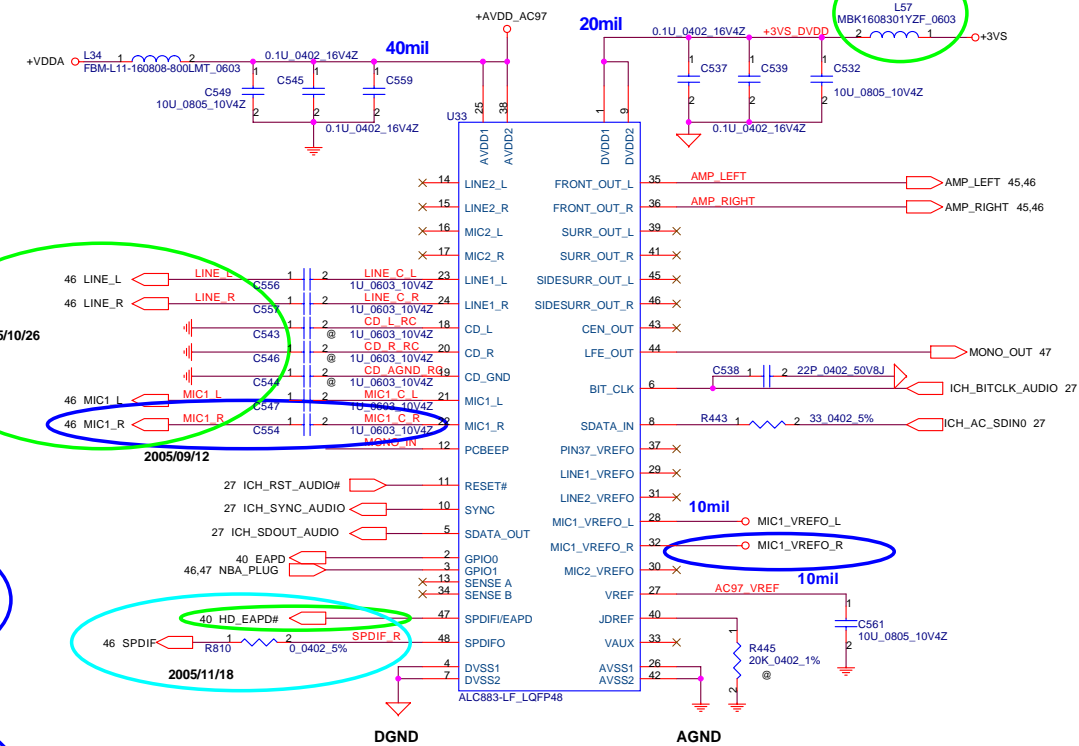
To TP/B Conn.



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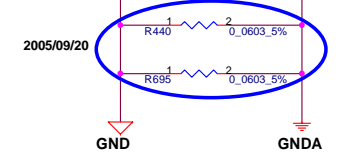
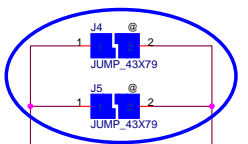
HD Audio Codec



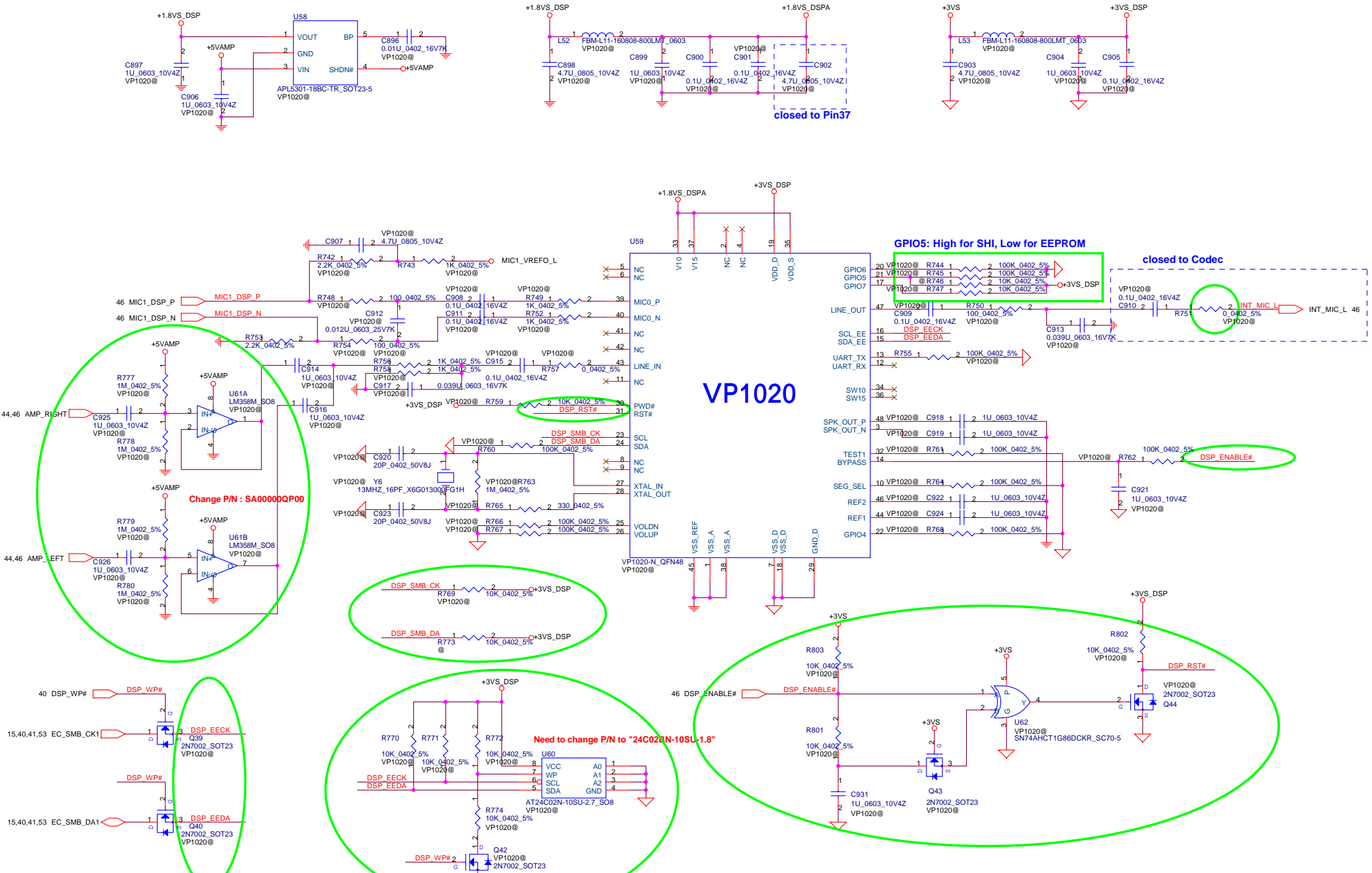
2005/10/26

2005/09/12

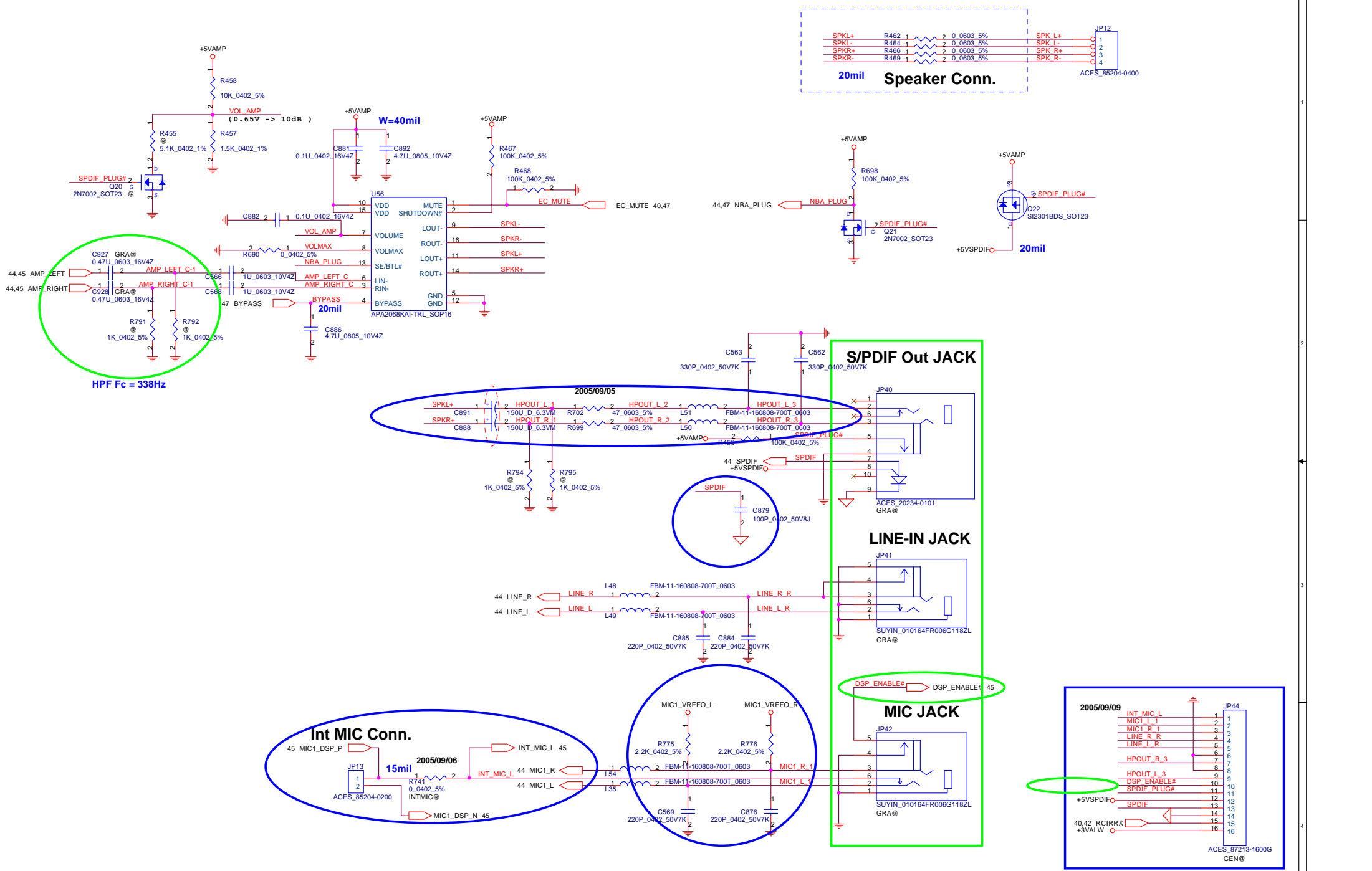
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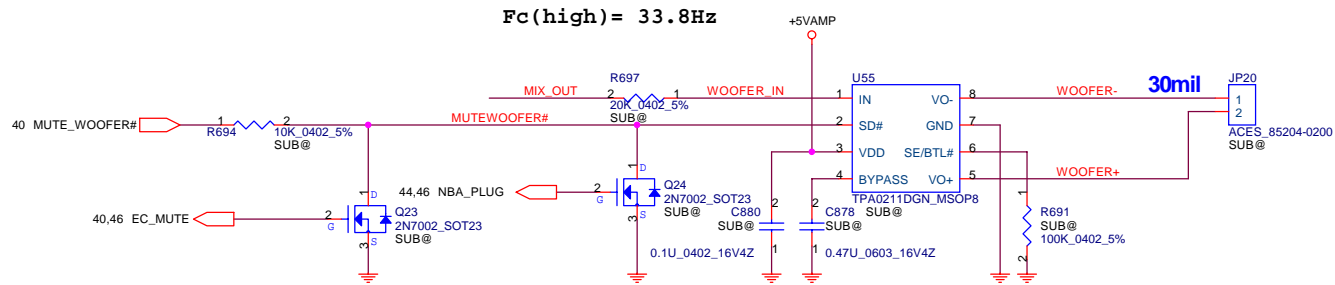
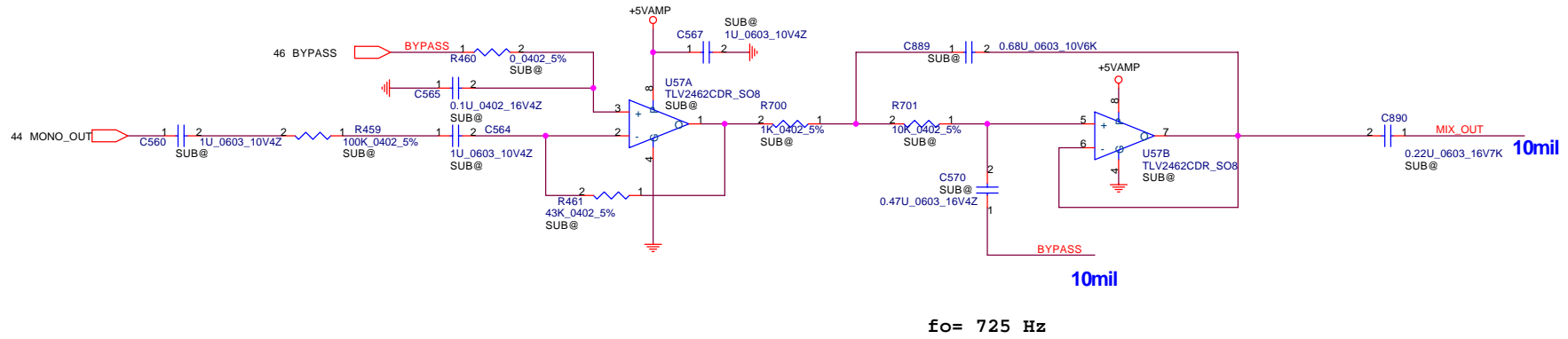


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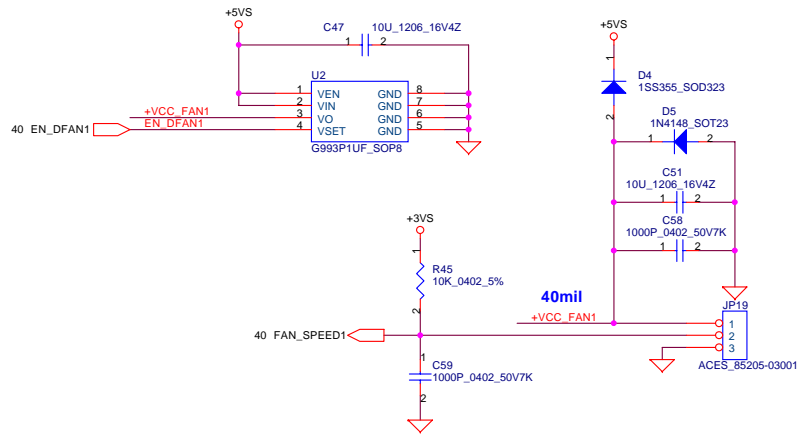
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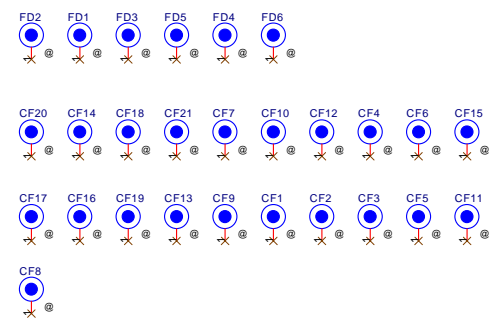
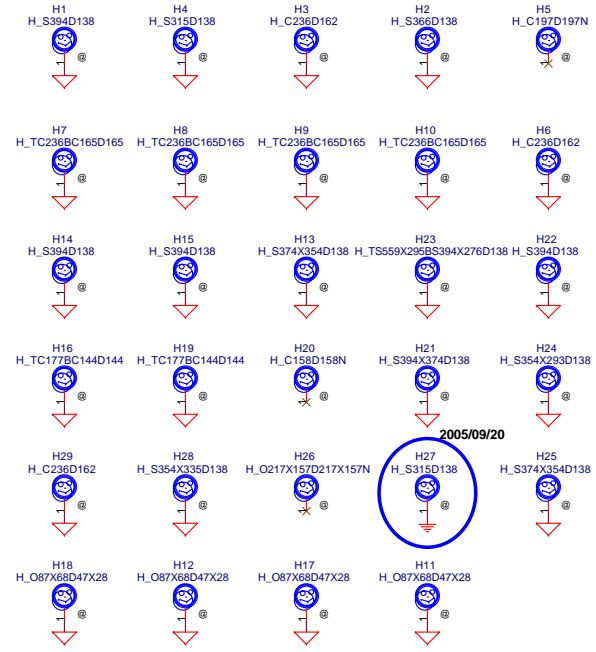
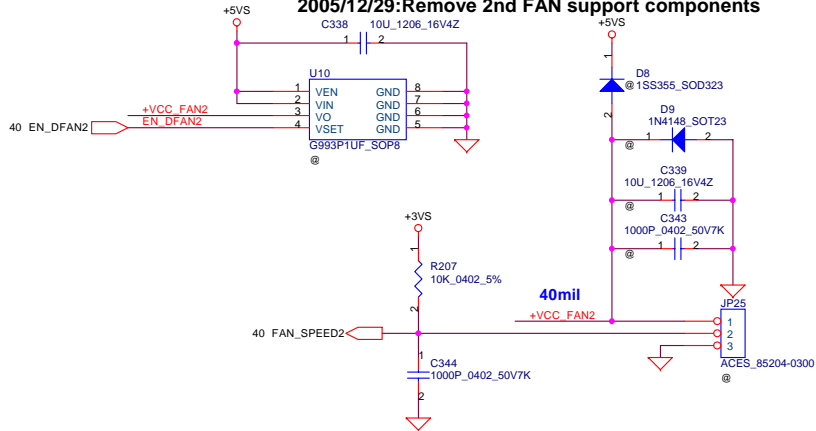
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FAN1 Conn

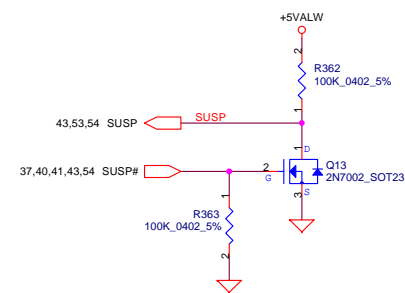
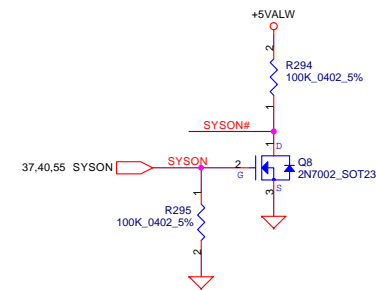
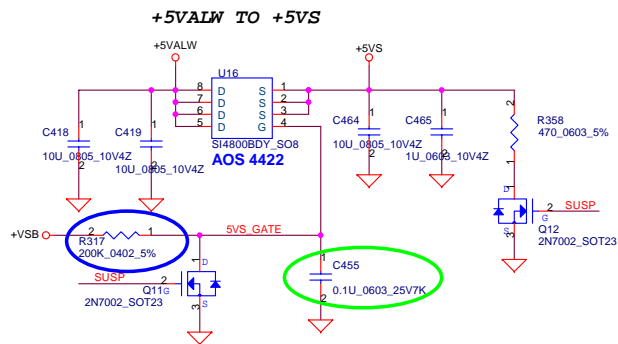


FAN2 Conn

2005/12/29: Remove 2nd FAN support components

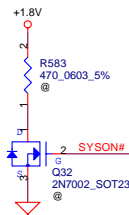
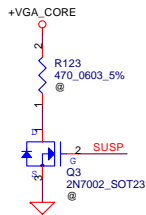
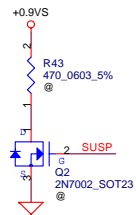
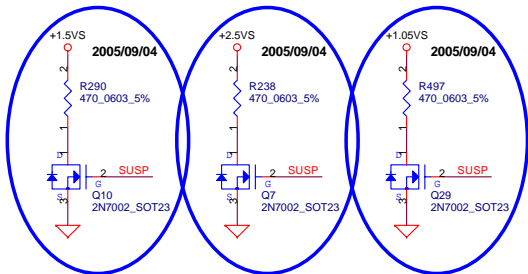
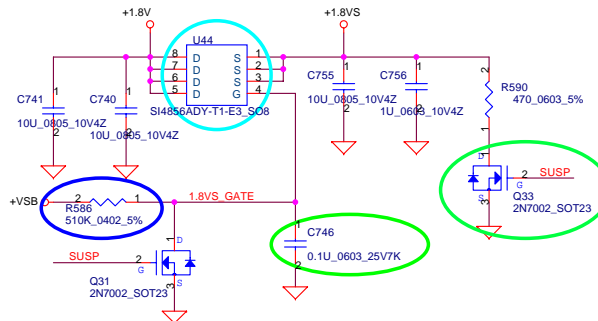
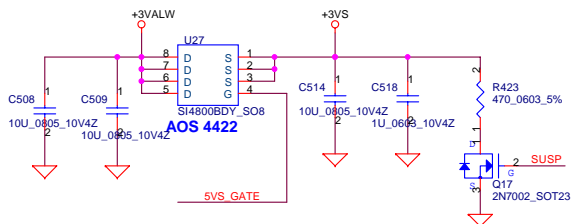


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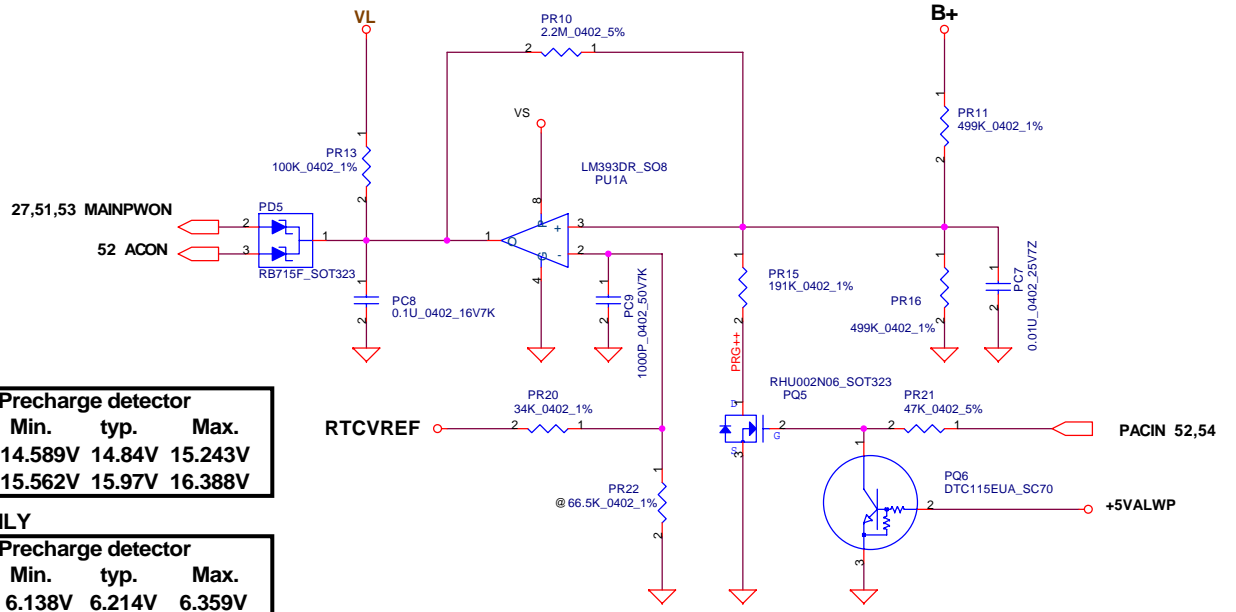
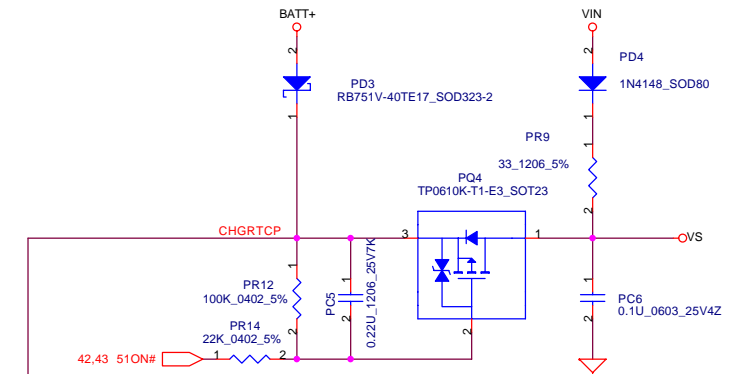
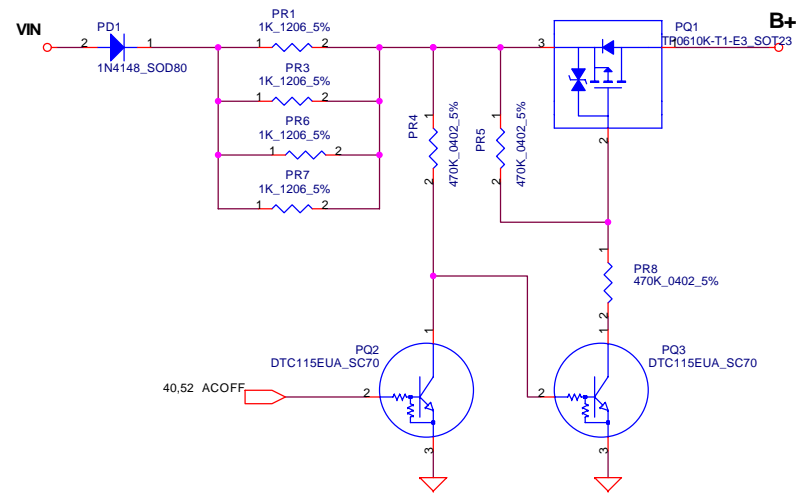
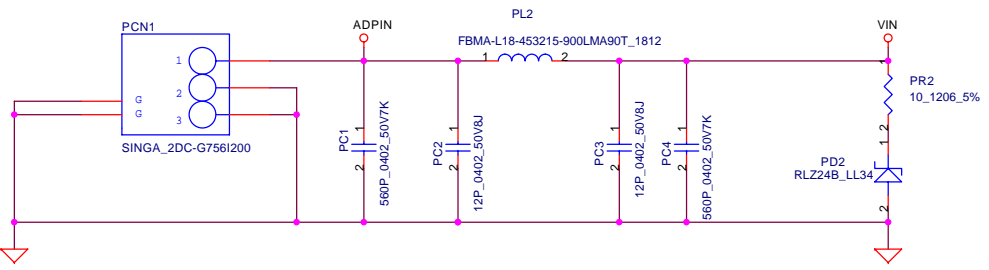


2005/12/18
 Change P/N : SB000001Y00(New) SI4856ADY
 SB548000310(Old)

+1.8V to +1.8VS



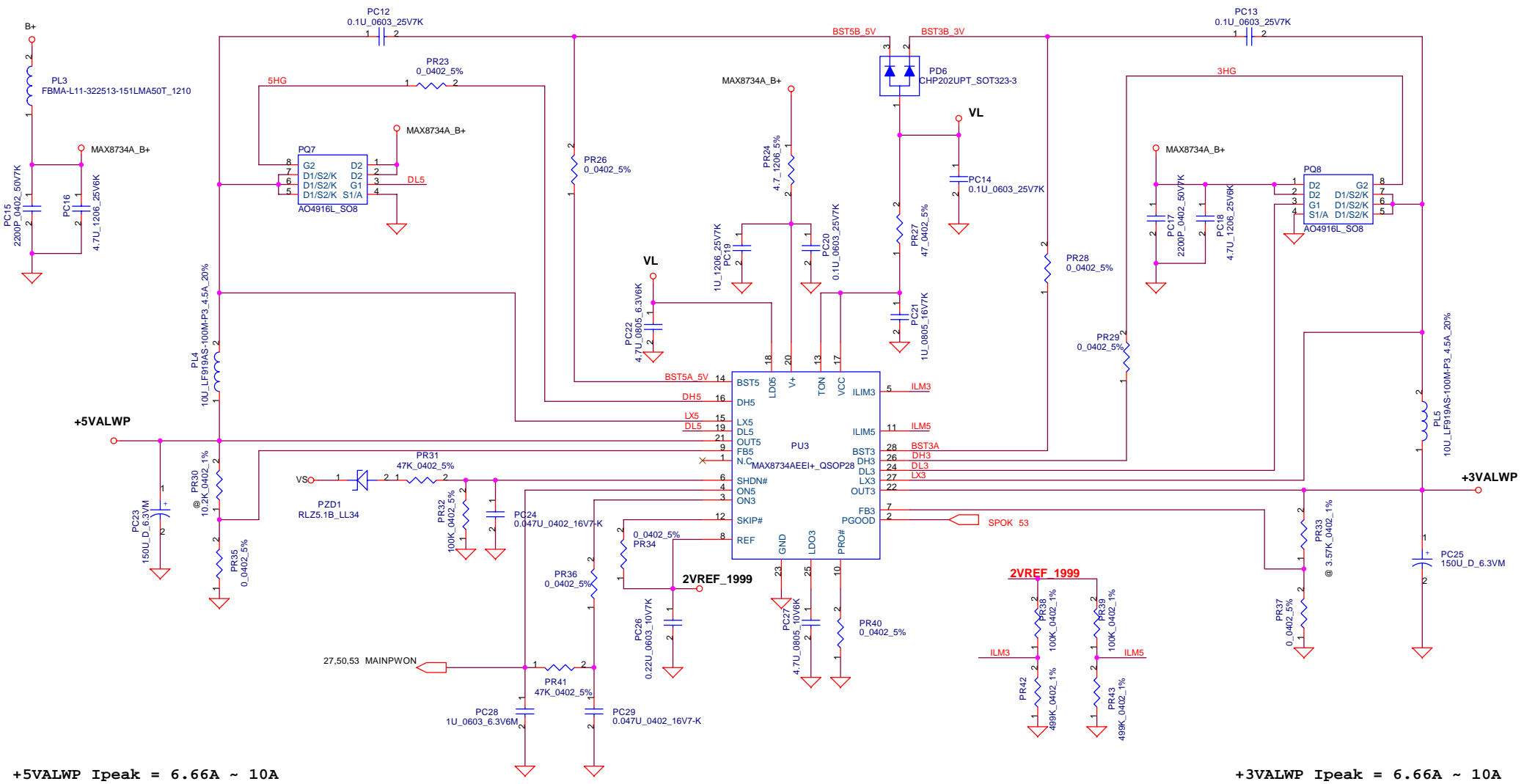
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ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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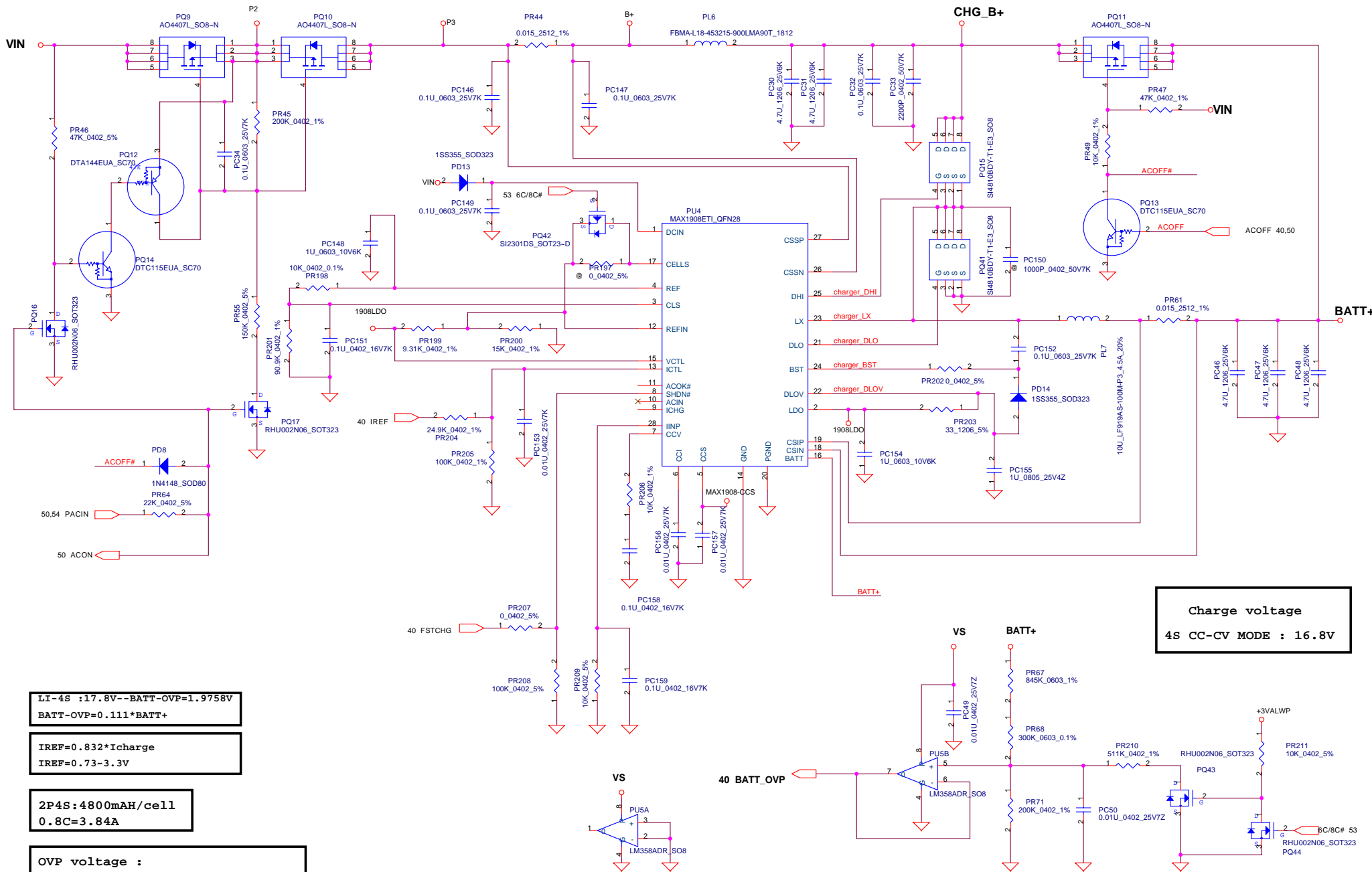


+5VALWP Ipeak = 6.66A ~ 10A

+3VALWP Ipeak = 6.66A ~ 10A

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I_{adp}=0~4.74A(90W)



Charge voltage
4S CC-CV MODE : 16.8V

LI-4S : 17.8V--BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

IREF=0.832*Icharge
IREF=0.73~3.3V

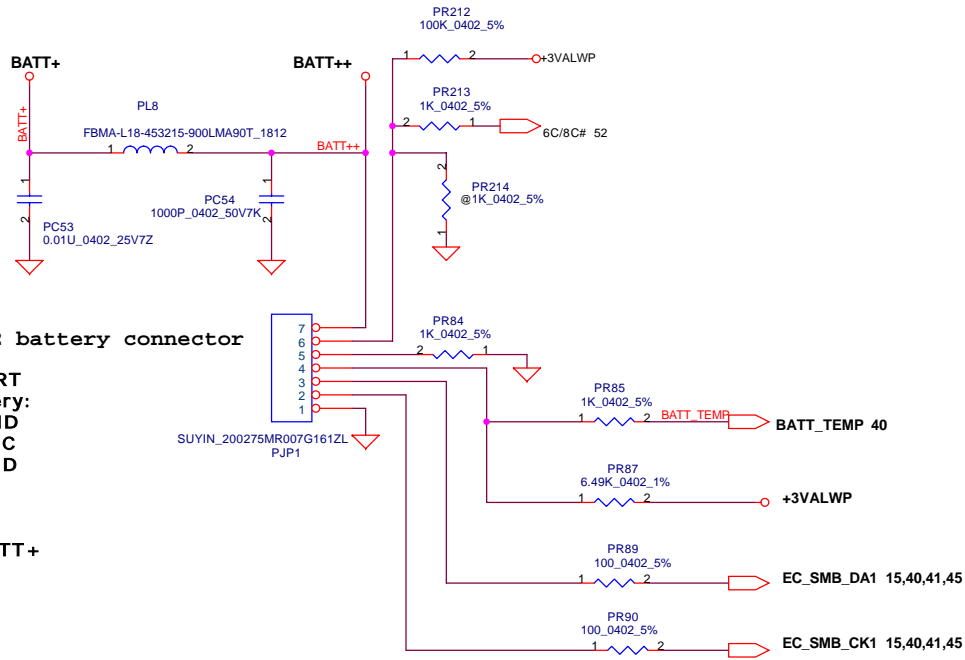
2P4S:4800mAh/cell
0.8C=3.84A

OVP voltage :
LI-3S : 17.8V---BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

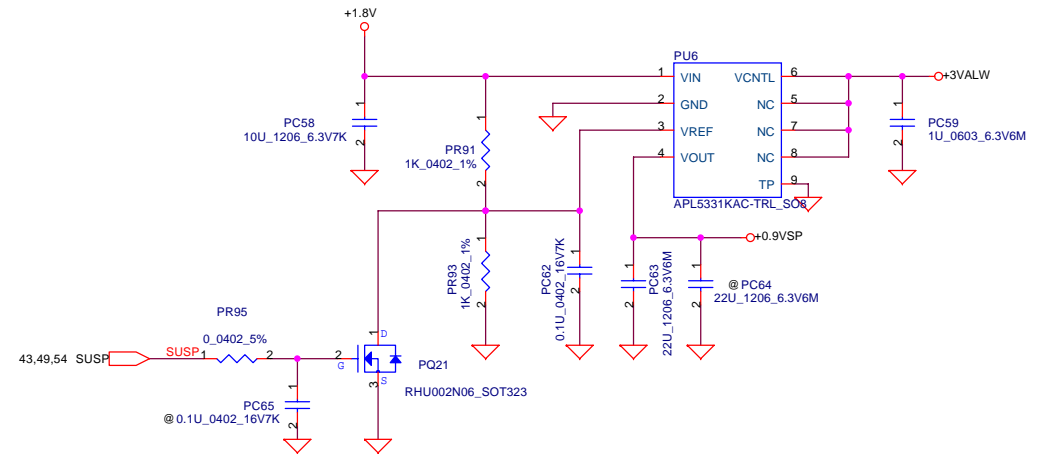
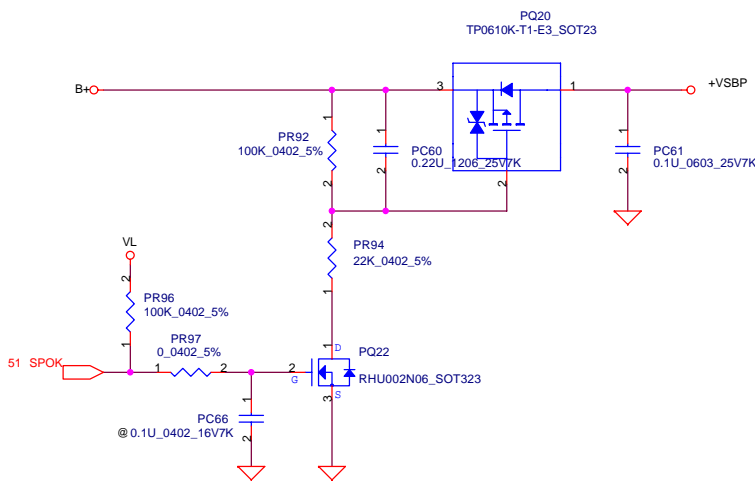
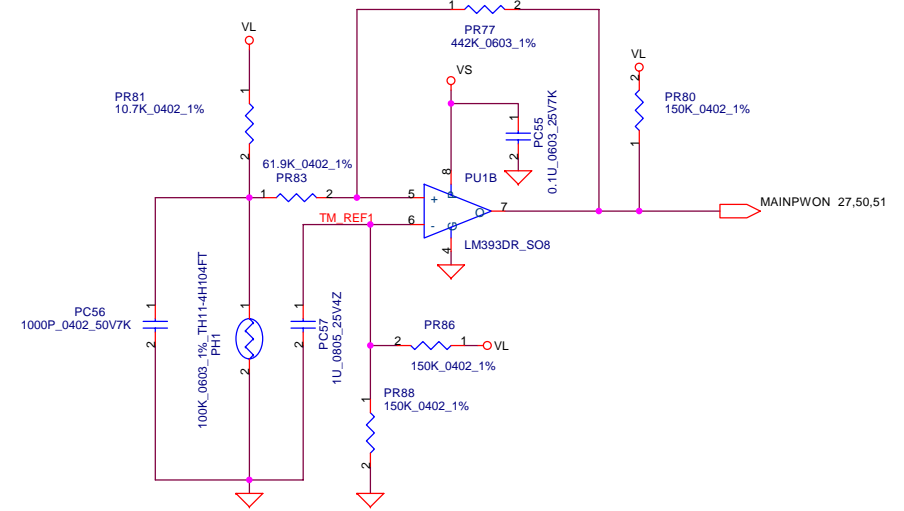
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PJP2 battery connector

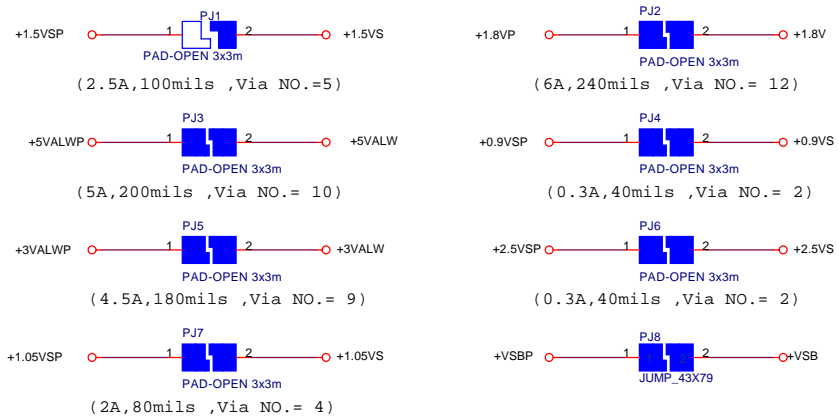
- SMART Battery:**
 1.GND
 2.SMC
 3.SMD
 4.TS
 5.B/I
 6.ID
 7.BATT+



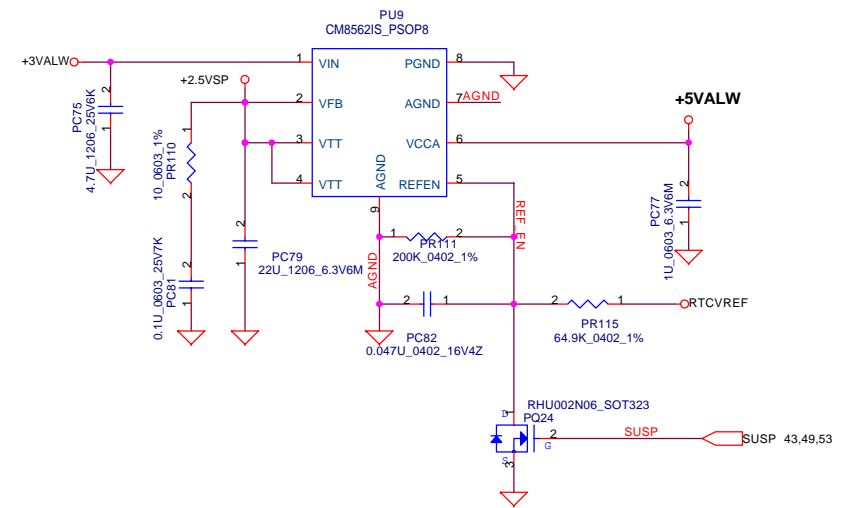
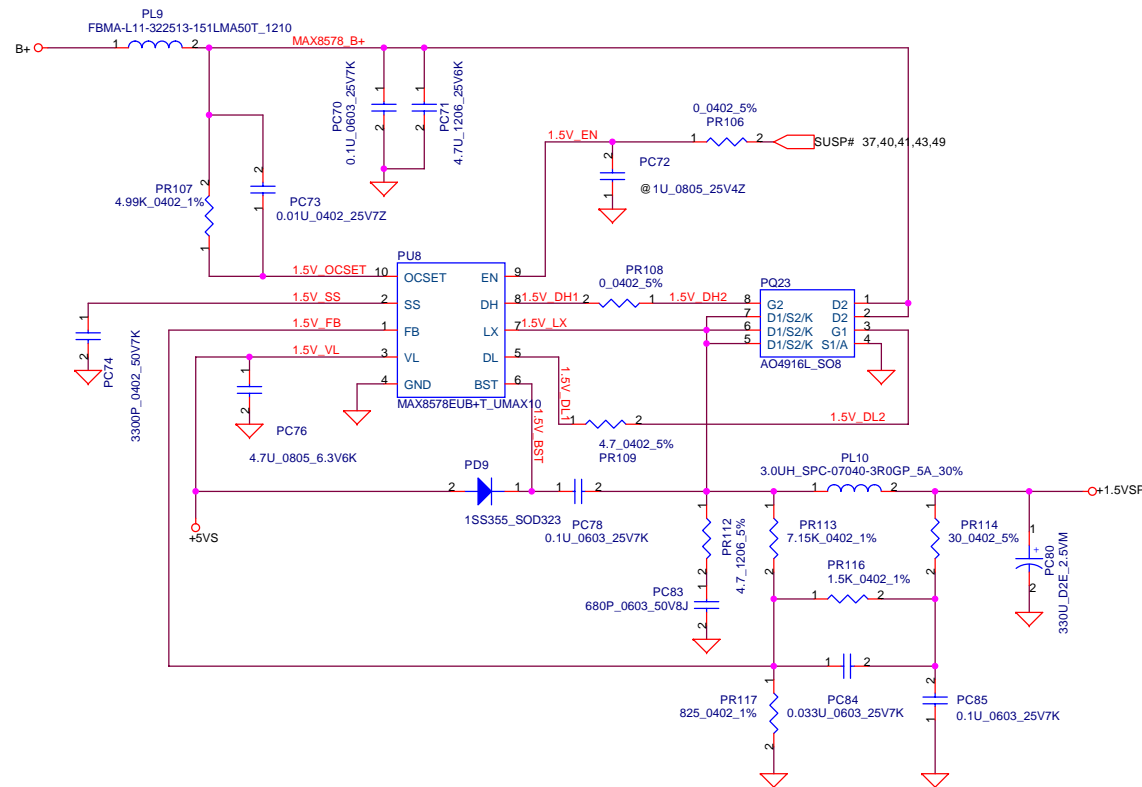
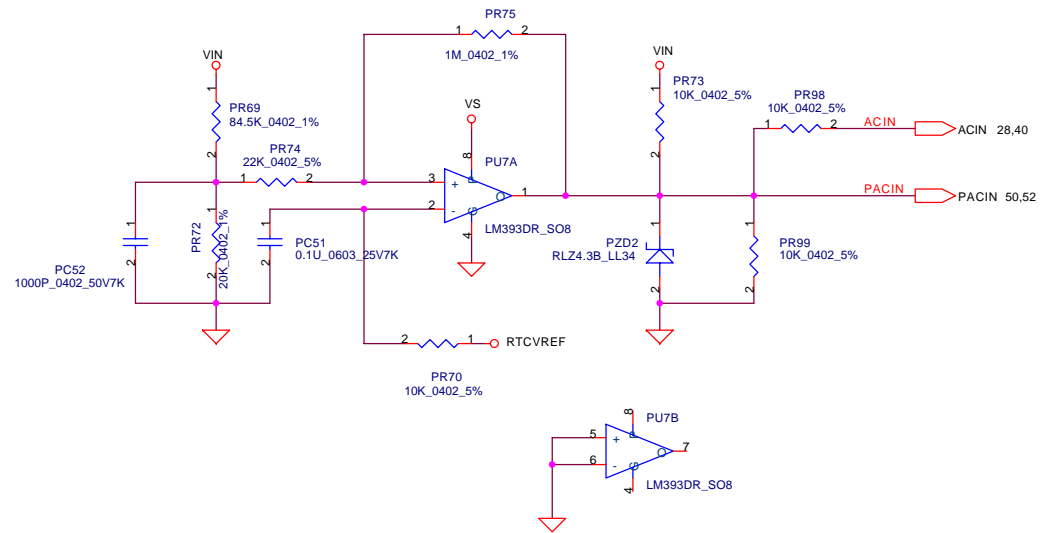
PH1 under CPU bottom side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C



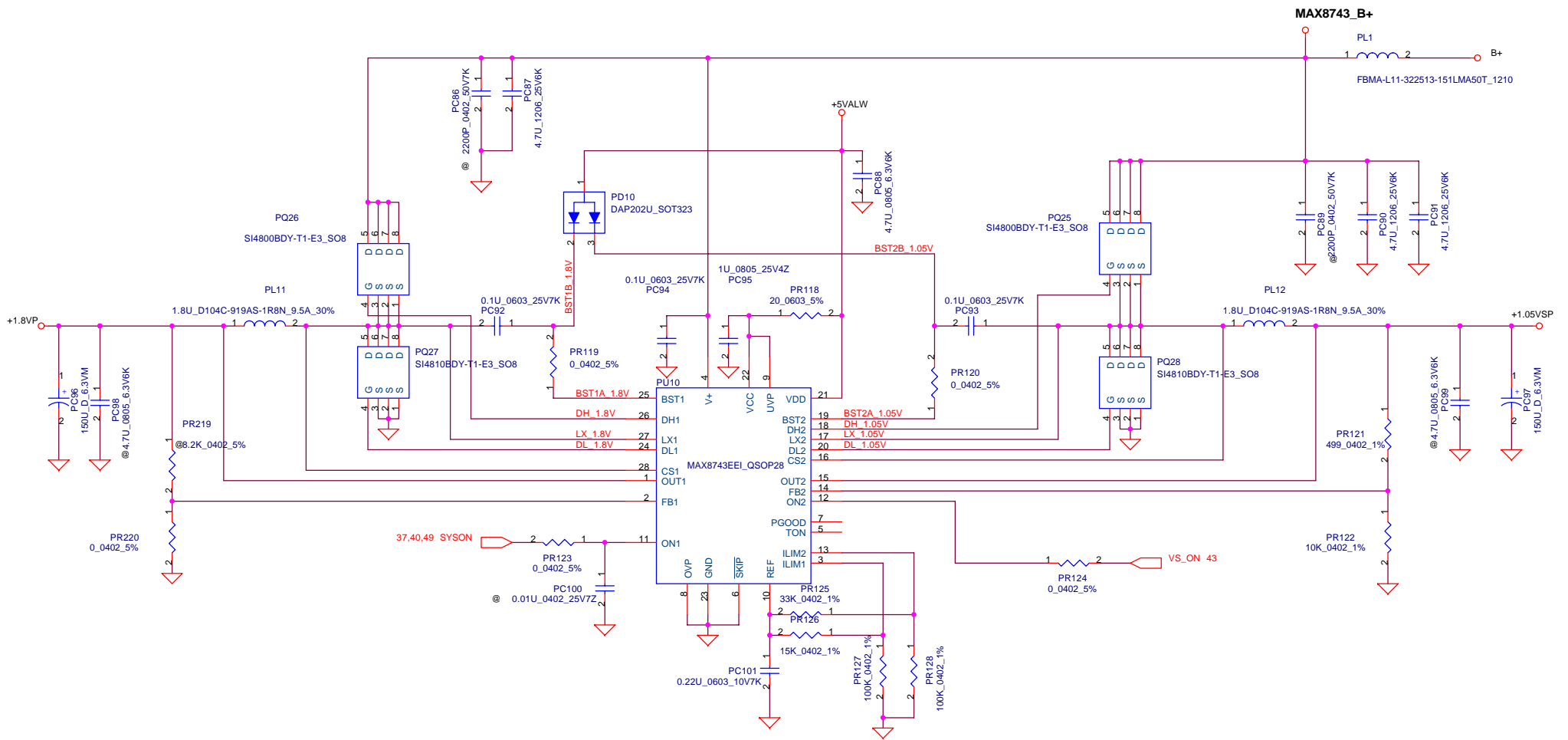
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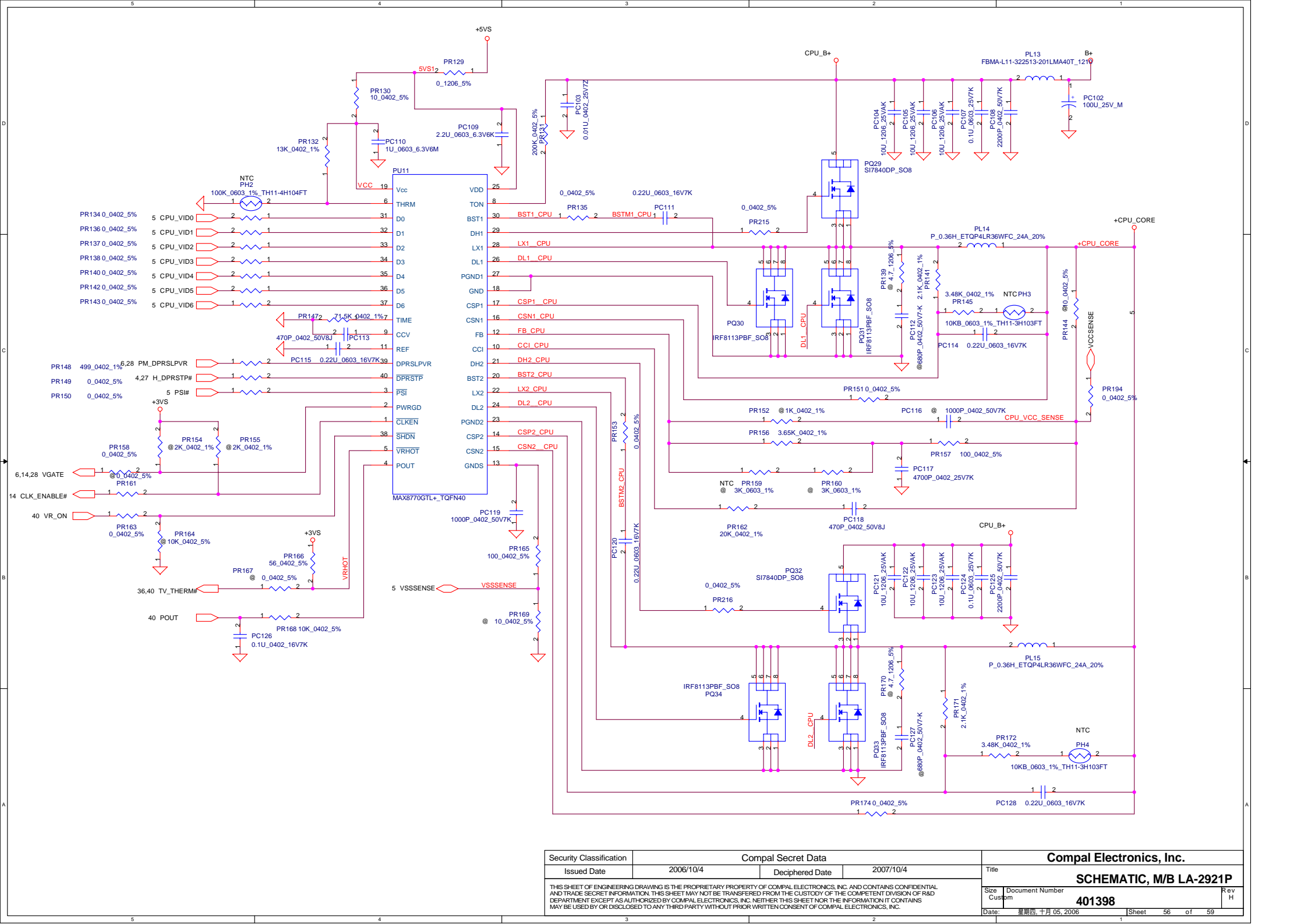
Vin Detector
17.90V/17.24V



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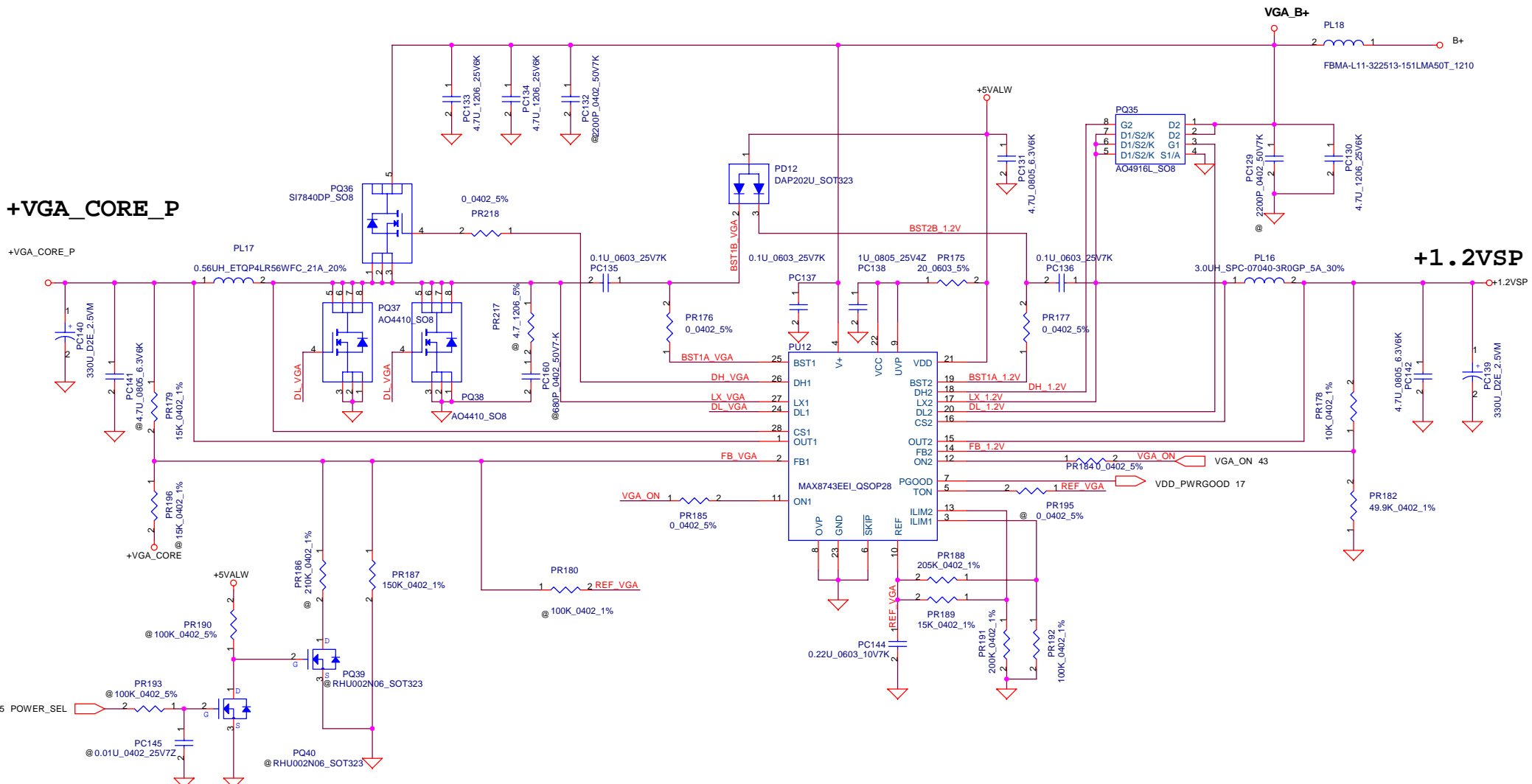


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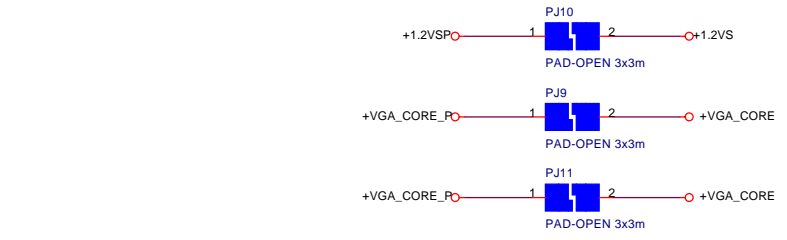
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POWER_SEL	H	L
+VGA_CORE FOR G73.	+0.95V(VGA@+G72@)	+1.025V
+VGA_CORE FOR G72.	+1.1V(VGA@)	



+VGA_CORE_P

+1.2VSP



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A --> B Change List

1. Page06 : No stuff R100 10K_0402_5%
2. Page09 : Add C49 & C887 220U_D2_4VM
3. Page10 : No stuff R57 2.2K_0402_5%
4. Page14 : Add R711 10K_0402_5% to set 96MHz output
Change Q14 & Q15 pin1 net name to connect to ICH7M
Change U19 ICS9LPRS325CKLFT part number to SA00000RE20
5. Page15 : Change C663, C664 from 22P_0402_50V8J to 18P_0402_50V8J.
6. Page18 : Modify VGA Device ID for G72MV & G73.
7. Page24 : Change VGA_DDC_CLK & VGA_DDC_DATA to Q26 & Q27 Level shift.
Add R781 & R782 4.7K_0402_5%
Change C589, C596, C583, C587, C594, C585 to 150P_0402_50V8J
8. Page28 : Change SB_INT_FLASH_SEL# from ICH7M GPIO38 to GPIO33.
9. Page29 : Change C437 from 0.1U_0402_16V4Z to 1U_0402_6.3V4Z
10. Page30 : Change PATA HDD+ODD select resistor form RP to R_0402 (0_0402_5%)
11. Page34 : Stuff R175 & no stuff R182 (0_0402_5%) for BCM4401E/BCM5789M/BCM5787M
12. Page35 : Modify LAN_ACTIVITY# & LAN_LINK# LED color
13. Page 36 : Add JP38 & C895 for CAMERA.
Swap JP17 PCIE TX & RX Signal.
Swap JP30 PCIE TX & RX Signal.
14. Page37 : Connect JP34 SMBus interface to ICH7M
Change JP4 & JP5 USB connector to BOTTOM.
15. Page38 : Add 1394 @ BOM Structure.
16. Page41 : Delete LCM interface Extension I/O.
No stuff R390 & Stuff R418 for Flash ROM interface.
17. Page42 : Change JP11 from 34 pin to 24 pin.
Change SW8 & SW9.
Add JP37.
18. Page43 : Change U28 Part Number.
Change SW1 Part Number.
Change R425 from 10K_0402_5% to 62K_0402_1%
Change R422 from 10K_0402_5% to 62K_0402_1% & add C513 0.1U_0402_16V4Z
19. Page44 : Add C554 for MIC_R
Add R440, R695 (0_0603_5%) & J4, J5 for EMI request.
20. Page45 : Add Echo Cancellation function.
21. Page46 : Correct Headphone L & R signal.
Reserved C879 for EMI request
Modify MIC Jack circuit. add R741, R775, R776, L54, C876
Change JP44 from 14 pin to 16 pin
22. Page48 : H27 connect to GNDA.
23. Page49 : Add R290, R238, R497, Q10, Q7, Q29
Change R317 to 200K_0402_5%
Change R586 to 510K_0402_5%

B --> C Change List

1. Page05 : No stuff C608, C614
2. Page12 : Change JP22 Footprint
3. Page14 : Change R620 from 2K_0402_5% to 10K_0402_5% & add Q38
4. Page15 : Delete DVI pull high resistor
5. Page17 : AddC96 330U for +VGA_CORE
6. Page18 : Modify PEX_CFG[0..2] setting from 02 to 01.
7. Page30 : Delete R395 & C486, add R394 for SATA bridge reset timing
Modify SATA HDD connector library
8. Page31 : Delete IDE_CD_L, IDE_CD_R & CD_GNDA
9. Page34 : Add R783, R784, R785 for BCM5787M, stuff R214 when use BCM4401E,
Del R168, change Q5 P/N
10. Page36 : Add +3VS, GND at JP30 for 3G device
11. Page38 : No stuff U14, R253, R246 & stuff R261
12. Page40 : Reserved R793 for ALC883 pin47 EAPD, & define KB910 Pin174 as EC_PWROK
13. Page41 : No stuff U21, U30, C490, R391, R390, R388 & stuff R418
14. Page42 : Modify SW9 Pin1, Pin5 as NC, no stuff C7
15. Page43 : Modify Power OK circuit. add R790 for EC_PWROK, reserved Q41, R420, C512
add D35, D37, Change BATT1 P/N to SP093PA0200
16. Page44 : Delete ALC883 CD input circuit, add HD_EAPD# signal
17. Page46 : Add C927, C928, reserved R791, R792
18. Page49 : Stuff Q33

Rev0.3 --> Rev0.4 Change List

1. Page15 : Add R809
2. Page23 : Reserved C934, C935, C936 for EMI
3. Page26 : Add U51, R811, Reserved R330
4. Page44 : Add R810 for EMI.

2005-12-19

1. Page 48: Delete 2nd Fan support components U10, D8, D9, C339, C343, JP25

2006-01-04

1. Page 16: Update VRAM Infineon strap setting.

2006-01-23

1. Change U42 part number from SA00000QZ00 to SA00000QZ10
2. Update C877 to no-stuff.

2006-02-06

1. Update R148 note as 30.1_0402_1% for G72MV & 40.2_0402_1% for G73M. (Not apply wait Nvidia document)

2006-03-02

1. Modify Camera power from +5VS to +3VS.
2. Add HDCP function. (U67, R818, R819, C946)

2006-03-28

1. Add R212 with 5787 @ BOM Structure property at Page 34 for S5 wake up function of BCM5787M.

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