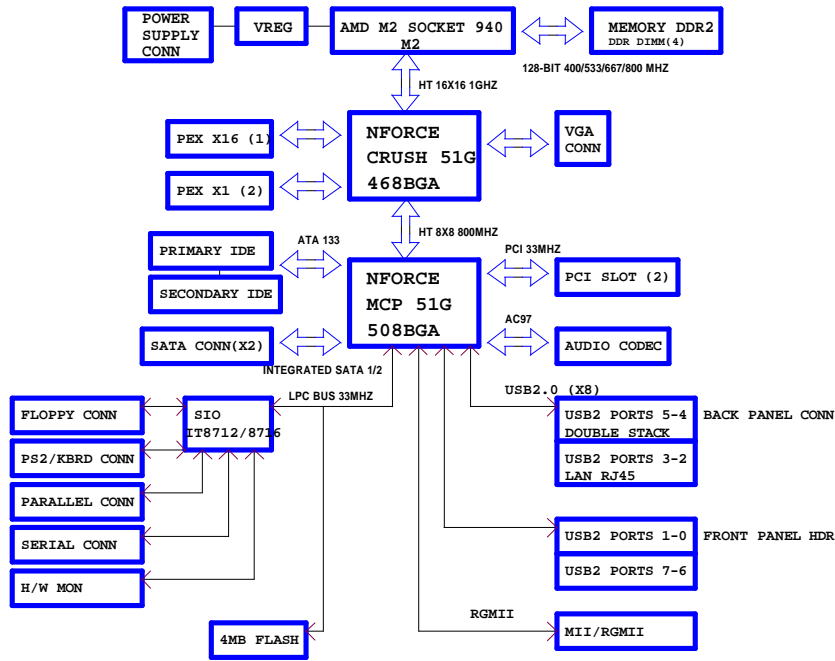



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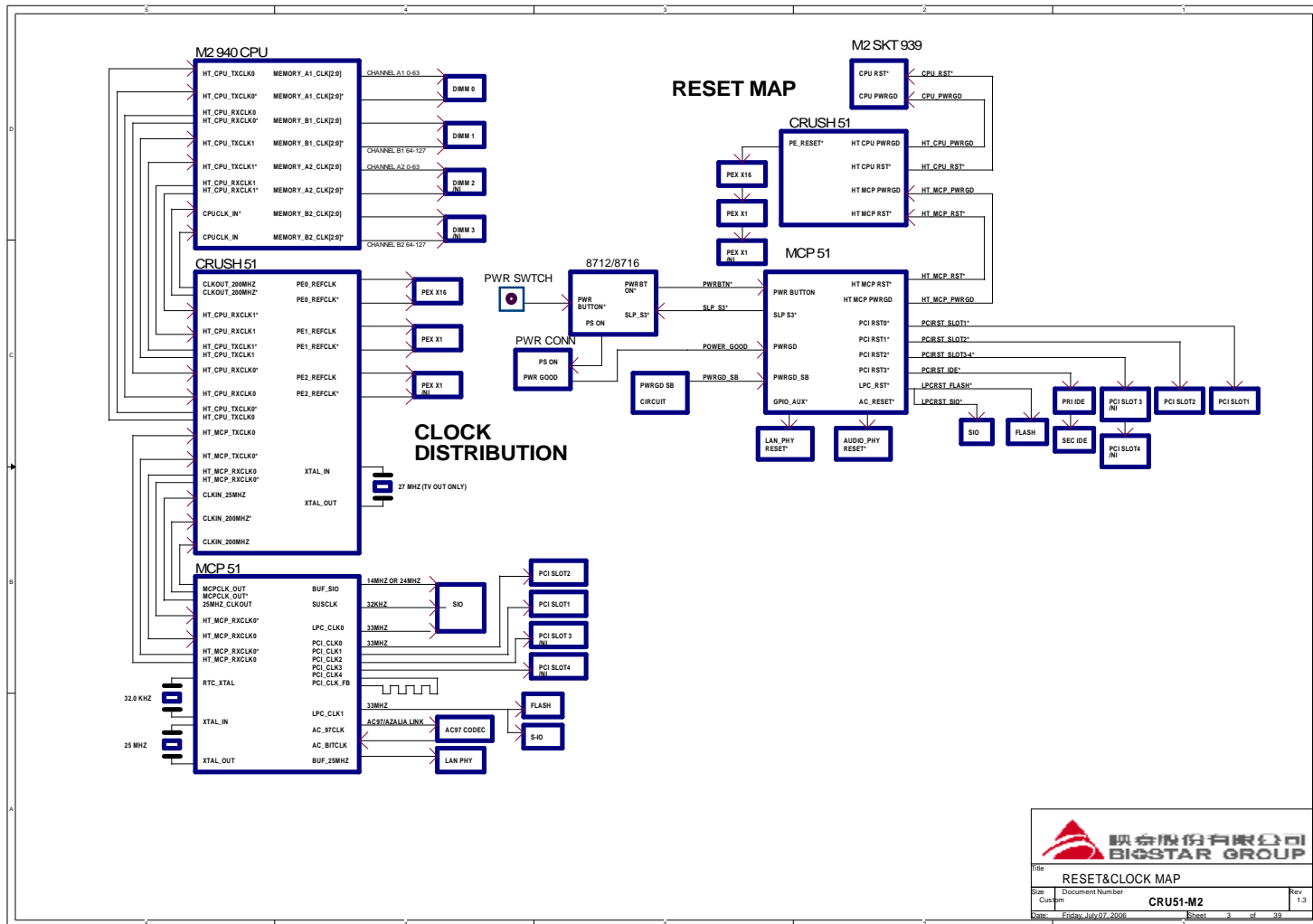
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RESET&CLOCK MAP	
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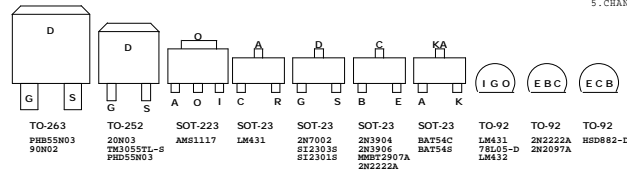
VID (4-9)	VDD	VID (4-9)	VDD
0X0000	1.550V	0X1000	1.150V
0X0001	1.525V	0X1001	1.125V
0X0010	1.500V	0X1010	1.100V
0X0011	1.475V	0X1011	1.075V
0X0100	1.450V	0X1100	1.050V
0X0101	1.425V	0X1101	1.025V
0X0110	1.400V	0X1110	1.000V
0X0111	1.375V	0X1111	0.975V
0X0100	1.350V	0X1100	0.950V
0X0101	1.325V	0X1101	0.925V
0X0110	1.300V	0X1110	0.900V
0X0111	1.275V	0X1111	0.875V
0X0100	1.250V	0X1100	0.850V
0X0101	1.225V	0X1101	0.825V
0X0110	1.200V	0X1110	0.800V
0X0111	1.175V	0X1111	0.775V

BACK PANEL	PCI BUS#	DEVICE#	IDSEL PIN	PCI SLOT	PCI SLOT	PCI SLOT	PCI SLOT	REQ/INT
SLOT				INTA*	INTB*	INTC*	INTD*	
1	01	0X05	22	P.INTX*	P.INTX*	P.INTX*	P.INTX*	1/1
2	01	0X06	24	P.INTW*	P.INTX*	P.INTY*	P.INTZ*	2/2
3	01	0X07						
4	01	0X08						
5	01	0X09						
6	01	0X0A						

DEVICE	PCI BUS#	FUNCTION	IDSEL PIN	DEVICE ID
MCP51	MCP51 LOGICAL PCI BUS#	0X01-0X0F
MAC/MAC	0	XA	0	0X5687
PCI/PCI BRIDGE	0	XB	0	0X000C
SATA1	0	X8	0	0X0005
SATA0	0	X8	0	0X0004
IDE	0	X6	0	0X0003
MODEM CODEC	0	X4	1	0X0008
AUDIO CODEC	0	X4	0	0X0009
USB 2.0	0	X2	1	0X0008
USB 1.1	0	X2	0	0X000A
SHARE TRIM	0	X1	2	0X000F
LDT	0	X0	0	0X000E
SMBUS2	0	X1	1	0X0002
LEGACY SLAVE	0	7	7	0X0003
LPC	0	X1	0	0X0000/0001
LOGICAL PCI BUS#	1	7	7	7
PCI SLOT 1				
PCI SLOT 2				
PCI SLOT 3				
PCI SLOT 4				
PCI SLOT 5				

DEVICE	SMBUS#	ADDRESS
SLOT		
DIMM 0	0	1010 000 - 0X50
DIMM 1	0	1010 001 - 0X51
DIMM 2	0	1010 010 - 0X52
DIMM 3	0	1010 011 - 0X53
SIO	1	0101 101 - 0X20
PCI SLOT 1	1	ARP
PCI SLOT 2	1	ARP
PCI SLOT 3	1	ARP
PCI SLOT 4	1	ARP
DDC BUS	A	7
DDC BUS	B	7

22U/25DE	97 mm
100U/16DE	63*11 mm
220U/16DE	63*11 mm
470U/16DE	87*11 mm
1000U/19DE	87*14 mm
1500U/19DE	107*25 mm
3300U/29DE	107*25 mm



CRU51-M9

1. CPU --- AMD Socket 939(3-Phase Power)
2. CHIPSET --- NF C51G IGP + NF MCP51
3. MEMORY --- Dual Channel DDR SDRAM X 2 (Max. 2GB)
4. SLOTS --- PEX X16 (x1), PEX X1 (x1), PCI (x2)
5. CODEC --- Realtek ALC655 5.1 Channel Audio
6. LAN PHY --- RTL8201
7. LPC/SIO --- IT8712F
8. SATA -- INTEGRATED(x2)
9. PCB Size --- 24.4cmx24.4cm, 4-Layer

CHANGE LIST

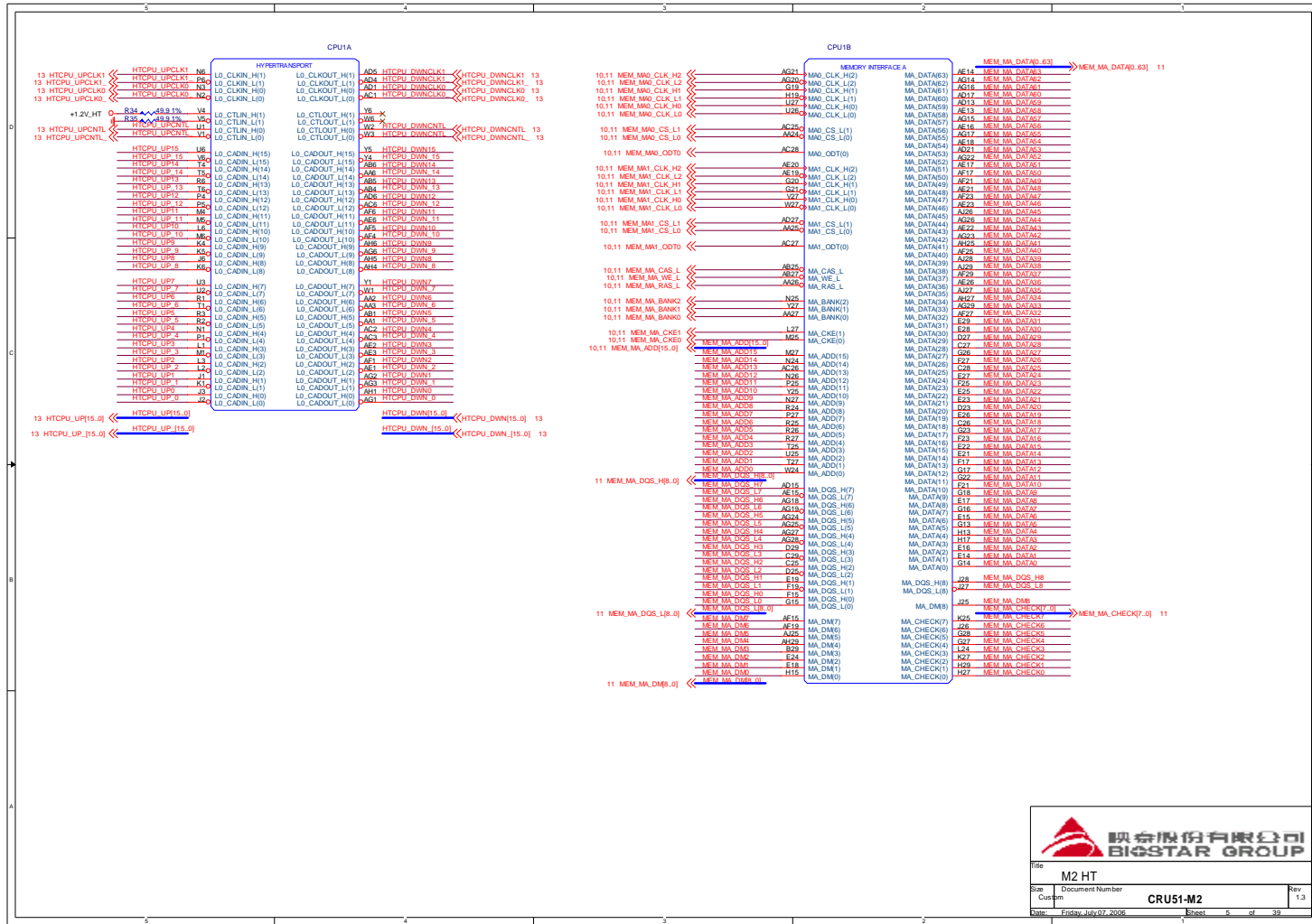
- 1.Q37 2N7002 CHANGE 2N3904 FOR POWER_SB TIMING
- 2.ADD C398 10U/10V FOR POWER_SB TIMING
- 3.PHY RST FOR S3 WAKE CAN WORK R134,C187 /NI, R136 0
- 4.DEL VID[0..5] TO MCP51.IT8712
- 5.ADD C45 1U/10V , R16 10K--> 100K FOR +2.6V
- 6.ADD U5,R83,R82(22) R84,R81(0)/NI FOR ON BOARD VGA PLUG INTO THE MONITOR CAN'T BOOT UP
- 7.ADD HEATSINK FOR S/B
- 8.R262,R264 20K --> 56K FOR KBRST,A20GATE BECOMING 3.3V
- 9.DEL R217,R222 SLEEPBTM CHANGE FROM S/B EXSMI PIN. R206 MOVE NEAR S/B
- 10.ADD OV-->R222,R281,R282,R283 /NI,R217
- 11.ADD LED-->D14,D15,D16,D17,R64,R66,R67,R74,R108,R149. SW-->PWRSM1,RSTS2,R62,R63
- 12.DEL CT31,PWRGD,C3,C4,C6,C7,C13,CTS,CT19,C209,C210,C230,C211,C212,C213,C227,C228,C229,C17(BOM)
- 13.AR19 0 /NI FOR AUDIO CLK TO 24KHz
- 14.ADD FOR EMI BC92,AR23,AL8,FB24
- 15.FOR EMI C9,C10,C12,C14-->447P
C8,C19,C196,AC32,C331-->104P
C395,C394,C393,C392,C391,C390,C389,C388,C383C387,C382,C386,C381,C385,C378,C384,C380-->100P
C116,C119,C123-->333P
AR22-->0
C343-->103P
C342-->102P
C316-->10P H1,H2-->COMMON CHOKE
- 16.DEL BOM FOR EMI FB6 /NI
- 5.CHANGE HEATSINK FOR N/B TO SHORT

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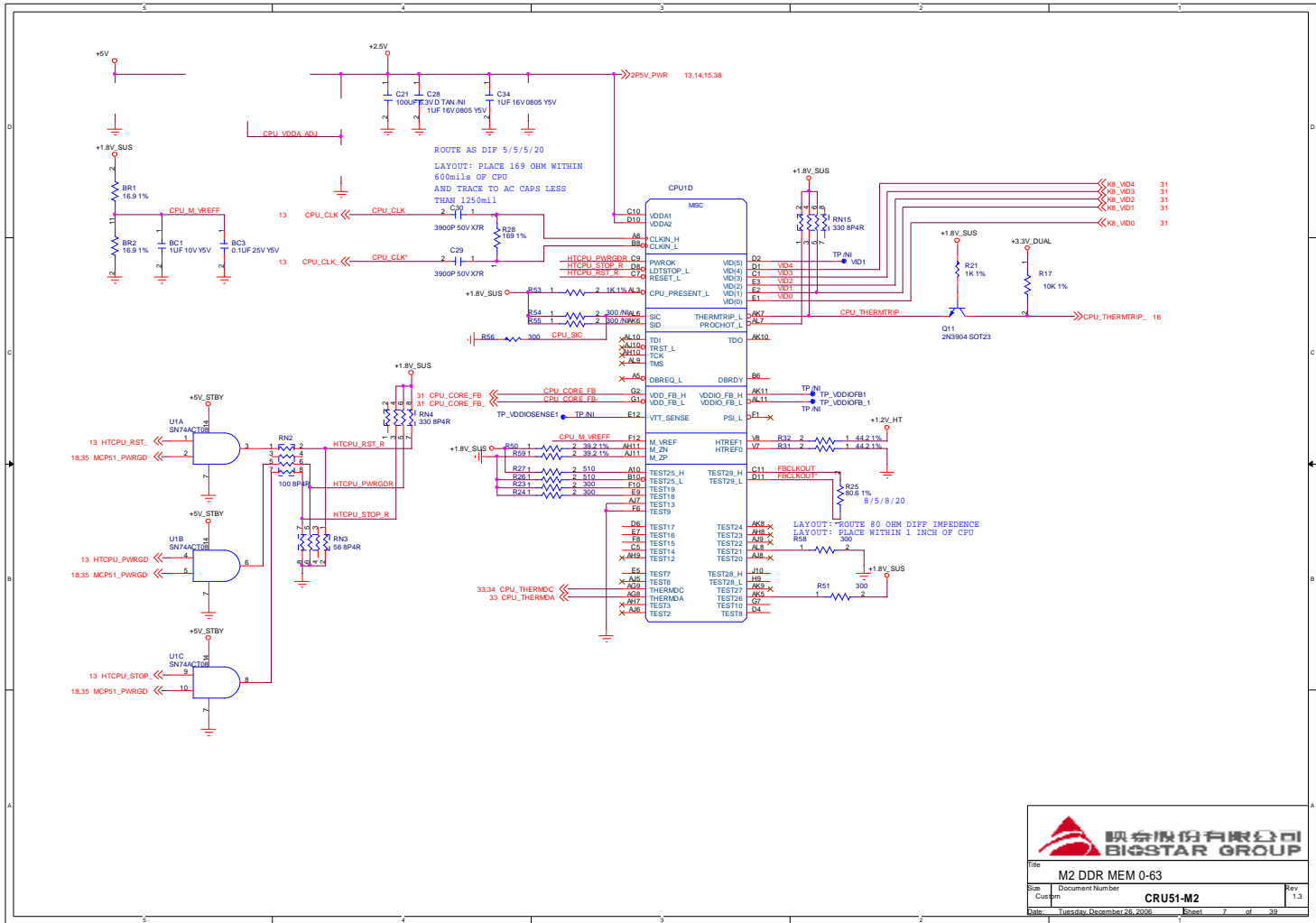
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CPU/C		MEMORY INTERFACE		MEM. MB. DATA[0..63]	
10.12 MEM_MB_CLK_H2	AK12	MB_CLK_H2(2)	MB_DATA(63)	AK13	MEM_MB_DATA[0..63]
10.12 MEM_MB_CLK_L2	AK13	MB_CLK_L2(2)	MB_DATA(62)	AK14	MEM_MB_DATA[62]
10.12 MEM_MB_CLK_H1	AK14	MB_CLK_H1(1)	MB_DATA(61)	AK15	MEM_MB_DATA[61]
10.12 MEM_MB_CLK_L1	AK15	MB_CLK_L1(1)	MB_DATA(60)	AK16	MEM_MB_DATA[60]
10.12 MEM_MB_CLK_H0	AK16	MB_CLK_H0(0)	MB_DATA(59)	AK17	MEM_MB_DATA[59]
10.12 MEM_MB_CLK_L0	AK17	MB_CLK_L0(0)	MB_DATA(58)	AK18	MEM_MB_DATA[58]
10.12 MEM_MB_CS_L1	AK18	MB_CS_L1(1)	MB_DATA(57)	AK19	MEM_MB_DATA[57]
10.12 MEM_MB_CS_L0	AK19	MB_CS_L0(0)	MB_DATA(56)	AK20	MEM_MB_DATA[56]
10.12 MEM_MB_ODT0	AK20	MB_ODT(0)	MB_DATA(55)	AK21	MEM_MB_DATA[55]
10.12 MEM_MB1_CLK_H2	AK21	MB1_CLK_H2(2)	MB_DATA(54)	AK22	MEM_MB_DATA[54]
10.12 MEM_MB1_CLK_L2	AK22	MB1_CLK_L2(2)	MB_DATA(53)	AK23	MEM_MB_DATA[53]
10.12 MEM_MB1_CLK_H1	AK23	MB1_CLK_H1(1)	MB_DATA(52)	AK24	MEM_MB_DATA[52]
10.12 MEM_MB1_CLK_L1	AK24	MB1_CLK_L1(1)	MB_DATA(51)	AK25	MEM_MB_DATA[51]
10.12 MEM_MB1_CLK_H0	AK25	MB1_CLK_H0(0)	MB_DATA(50)	AK26	MEM_MB_DATA[50]
10.12 MEM_MB1_CLK_L0	AK26	MB1_CLK_L0(0)	MB_DATA(49)	AK27	MEM_MB_DATA[49]
10.12 MEM_MB1_CS_L1	AK27	MB1_CS_L1(1)	MB_DATA(48)	AK28	MEM_MB_DATA[48]
10.12 MEM_MB1_CS_L0	AK28	MB1_CS_L0(0)	MB_DATA(47)	AK29	MEM_MB_DATA[47]
10.12 MEM_MB1_ODT0	AK29	MB1_ODT(0)	MB_DATA(46)	AK30	MEM_MB_DATA[46]
10.12 MEM_MB_CAS_L	AK30	MB_CAS_L	MB_DATA(45)	AK31	MEM_MB_DATA[45]
10.12 MEM_MB_WE_L	AK31	MB_WE_L	MB_DATA(44)	AK32	MEM_MB_DATA[44]
10.12 MEM_MB_RAS_L	AK32	MB_RAS_L	MB_DATA(43)	AK33	MEM_MB_DATA[43]
10.12 MEM_MB_BANK2	AK33	MB_BANK(2)	MB_DATA(42)	AK34	MEM_MB_DATA[42]
10.12 MEM_MB_BANK1	AK34	MB_BANK(1)	MB_DATA(41)	AK35	MEM_MB_DATA[41]
10.12 MEM_MB_BANK0	AK35	MB_BANK(0)	MB_DATA(40)	AK36	MEM_MB_DATA[40]
10.12 MEM_MB_CKE1	AK36	MB_CKE(1)	MB_DATA(39)	AK37	MEM_MB_DATA[39]
10.12 MEM_MB_CKE0	AK37	MB_CKE(0)	MB_DATA(38)	AK38	MEM_MB_DATA[38]
10.12 MEM_MB_ADD[15..0]	AK38	MEM_MB_ADD[15..0]	MB_DATA(37)	AK39	MEM_MB_DATA[37]
MEM_MB_ADD16	AK39	MB_ADD(16)	MB_DATA(36)	AK40	MEM_MB_DATA[36]
MEM_MB_ADD17	AK40	MB_ADD(17)	MB_DATA(35)	AK41	MEM_MB_DATA[35]
MEM_MB_ADD18	AK41	MB_ADD(18)	MB_DATA(34)	AK42	MEM_MB_DATA[34]
MEM_MB_ADD19	AK42	MB_ADD(19)	MB_DATA(33)	AK43	MEM_MB_DATA[33]
MEM_MB_ADD20	AK43	MB_ADD(20)	MB_DATA(32)	AK44	MEM_MB_DATA[32]
MEM_MB_ADD21	AK44	MB_ADD(21)	MB_DATA(31)	AK45	MEM_MB_DATA[31]
MEM_MB_ADD22	AK45	MB_ADD(22)	MB_DATA(30)	AK46	MEM_MB_DATA[30]
MEM_MB_ADD23	AK46	MB_ADD(23)	MB_DATA(29)	AK47	MEM_MB_DATA[29]
MEM_MB_ADD24	AK47	MB_ADD(24)	MB_DATA(28)	AK48	MEM_MB_DATA[28]
MEM_MB_ADD25	AK48	MB_ADD(25)	MB_DATA(27)	AK49	MEM_MB_DATA[27]
MEM_MB_ADD26	AK49	MB_ADD(26)	MB_DATA(26)	AK50	MEM_MB_DATA[26]
MEM_MB_ADD27	AK50	MB_ADD(27)	MB_DATA(25)	AK51	MEM_MB_DATA[25]
MEM_MB_ADD28	AK51	MB_ADD(28)	MB_DATA(24)	AK52	MEM_MB_DATA[24]
MEM_MB_ADD29	AK52	MB_ADD(29)	MB_DATA(23)	AK53	MEM_MB_DATA[23]
MEM_MB_ADD30	AK53	MB_ADD(30)	MB_DATA(22)	AK54	MEM_MB_DATA[22]
MEM_MB_ADD31	AK54	MB_ADD(31)	MB_DATA(21)	AK55	MEM_MB_DATA[21]
MEM_MB_ADD32	AK55	MB_ADD(32)	MB_DATA(20)	AK56	MEM_MB_DATA[20]
MEM_MB_ADD33	AK56	MB_ADD(33)	MB_DATA(19)	AK57	MEM_MB_DATA[19]
MEM_MB_ADD34	AK57	MB_ADD(34)	MB_DATA(18)	AK58	MEM_MB_DATA[18]
MEM_MB_ADD35	AK58	MB_ADD(35)	MB_DATA(17)	AK59	MEM_MB_DATA[17]
MEM_MB_ADD36	AK59	MB_ADD(36)	MB_DATA(16)	AK60	MEM_MB_DATA[16]
MEM_MB_ADD37	AK60	MB_ADD(37)	MB_DATA(15)	AK61	MEM_MB_DATA[15]
MEM_MB_ADD38	AK61	MB_ADD(38)	MB_DATA(14)	AK62	MEM_MB_DATA[14]
MEM_MB_ADD39	AK62	MB_ADD(39)	MB_DATA(13)	AK63	MEM_MB_DATA[13]
MEM_MB_ADD40	AK63	MB_ADD(40)	MB_DATA(12)	AK64	MEM_MB_DATA[12]
MEM_MB_ADD41	AK64	MB_ADD(41)	MB_DATA(11)	AK65	MEM_MB_DATA[11]
MEM_MB_ADD42	AK65	MB_ADD(42)	MB_DATA(10)	AK66	MEM_MB_DATA[10]
MEM_MB_ADD43	AK66	MB_ADD(43)	MB_DATA(9)	AK67	MEM_MB_DATA[9]
MEM_MB_ADD44	AK67	MB_ADD(44)	MB_DATA(8)	AK68	MEM_MB_DATA[8]
MEM_MB_ADD45	AK68	MB_ADD(45)	MB_DATA(7)	AK69	MEM_MB_DATA[7]
MEM_MB_ADD46	AK69	MB_ADD(46)	MB_DATA(6)	AK70	MEM_MB_DATA[6]
MEM_MB_ADD47	AK70	MB_ADD(47)	MB_DATA(5)	AK71	MEM_MB_DATA[5]
MEM_MB_ADD48	AK71	MB_ADD(48)	MB_DATA(4)	AK72	MEM_MB_DATA[4]
MEM_MB_ADD49	AK72	MB_ADD(49)	MB_DATA(3)	AK73	MEM_MB_DATA[3]
MEM_MB_ADD50	AK73	MB_ADD(50)	MB_DATA(2)	AK74	MEM_MB_DATA[2]
MEM_MB_ADD51	AK74	MB_ADD(51)	MB_DATA(1)	AK75	MEM_MB_DATA[1]
MEM_MB_ADD52	AK75	MB_ADD(52)	MB_DATA(0)	AK76	MEM_MB_DATA[0]
MEM_MB_DQS_H7	AK13	MB_DQS_H(7)	MB_DATA(10)	AK77	MEM_MB_DATA[10]
MEM_MB_DQS_L7	AK14	MB_DQS_L(7)	MB_DATA(9)	AK78	MEM_MB_DATA[9]
MEM_MB_DQS_H6	AK15	MB_DQS_H(6)	MB_DATA(8)	AK79	MEM_MB_DATA[8]
MEM_MB_DQS_L6	AK16	MB_DQS_L(6)	MB_DATA(7)	AK80	MEM_MB_DATA[7]
MEM_MB_DQS_H5	AK17	MB_DQS_H(5)	MB_DATA(6)	AK81	MEM_MB_DATA[6]
MEM_MB_DQS_L5	AK18	MB_DQS_L(5)	MB_DATA(5)	AK82	MEM_MB_DATA[5]
MEM_MB_DQS_H4	AK19	MB_DQS_H(4)	MB_DATA(4)	AK83	MEM_MB_DATA[4]
MEM_MB_DQS_L4	AK20	MB_DQS_L(4)	MB_DATA(3)	AK84	MEM_MB_DATA[3]
MEM_MB_DQS_H3	AK21	MB_DQS_H(3)	MB_DATA(2)	AK85	MEM_MB_DATA[2]
MEM_MB_DQS_L3	AK22	MB_DQS_L(3)	MB_DATA(1)	AK86	MEM_MB_DATA[1]
MEM_MB_DQS_H2	AK23	MB_DQS_H(2)	MB_DATA(0)	AK87	MEM_MB_DATA[0]
MEM_MB_DQS_L2	AK24	MB_DQS_L(2)	MB_DQS_H(8)	AK88	MEM_MB_DQS_H8
MEM_MB_DQS_H1	AK25	MB_DQS_H(1)	MB_DQS_L(8)	AK89	MEM_MB_DQS_L8
MEM_MB_DQS_L1	AK26	MB_DQS_L(1)	MB_DQS_H(9)	AK90	MEM_MB_DQS_H9
MEM_MB_DQS_H0	AK27	MB_DQS_H(0)	MB_DQS_L(9)	AK91	MEM_MB_DQS_L9
MEM_MB_DQS_L0	AK28	MB_DQS_L(0)	MB_DM(8)	AK92	MEM_MB_DM8
MEM_MB_DM7	AK14	MB_DM(7)	MB_CHECK(7)	AK93	MEM_MB_CHECK7
MEM_MB_DM6	AK15	MB_DM(6)	MB_CHECK(6)	AK94	MEM_MB_CHECK6
MEM_MB_DM5	AK16	MB_DM(5)	MB_CHECK(5)	AK95	MEM_MB_CHECK5
MEM_MB_DM4	AK17	MB_DM(4)	MB_CHECK(4)	AK96	MEM_MB_CHECK4
MEM_MB_DM3	AK18	MB_DM(3)	MB_CHECK(3)	AK97	MEM_MB_CHECK3
MEM_MB_DM2	AK19	MB_DM(2)	MB_CHECK(2)	AK98	MEM_MB_CHECK2
MEM_MB_DM1	AK20	MB_DM(1)	MB_CHECK(1)	AK99	MEM_MB_CHECK1
MEM_MB_DM0	AK21	MB_DM(0)	MB_CHECK(0)	AK100	MEM_MB_CHECK0
MEM_MB_CHECK[7..0]	AK100	MEM_MB_CHECK[7..0]	MEM_MB_CHECK[7..0]	AK101	MEM_MB_CHECK[7..0]

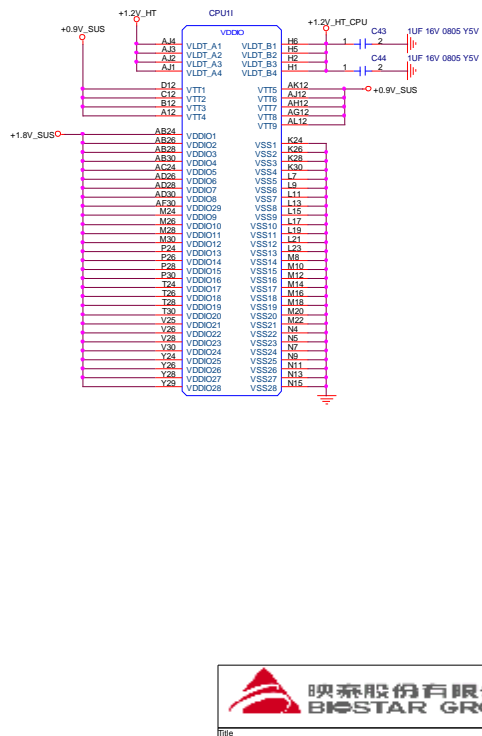
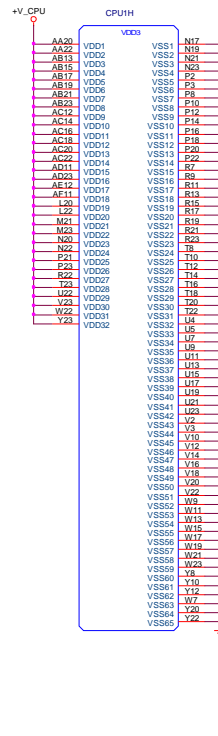
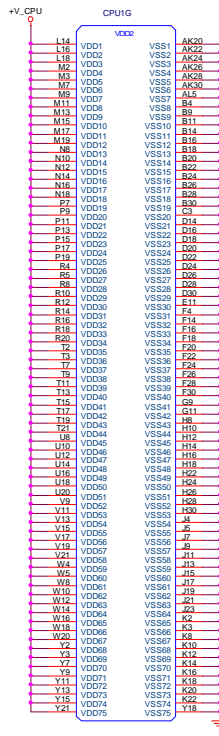
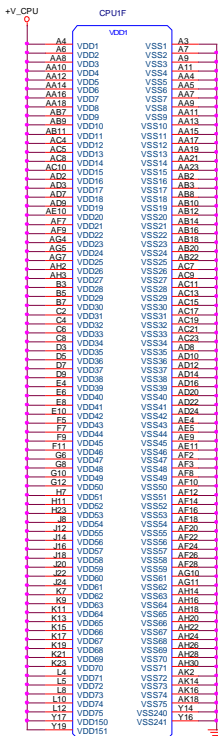
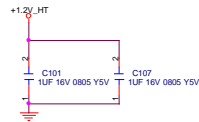
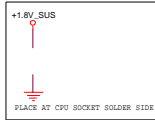
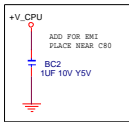
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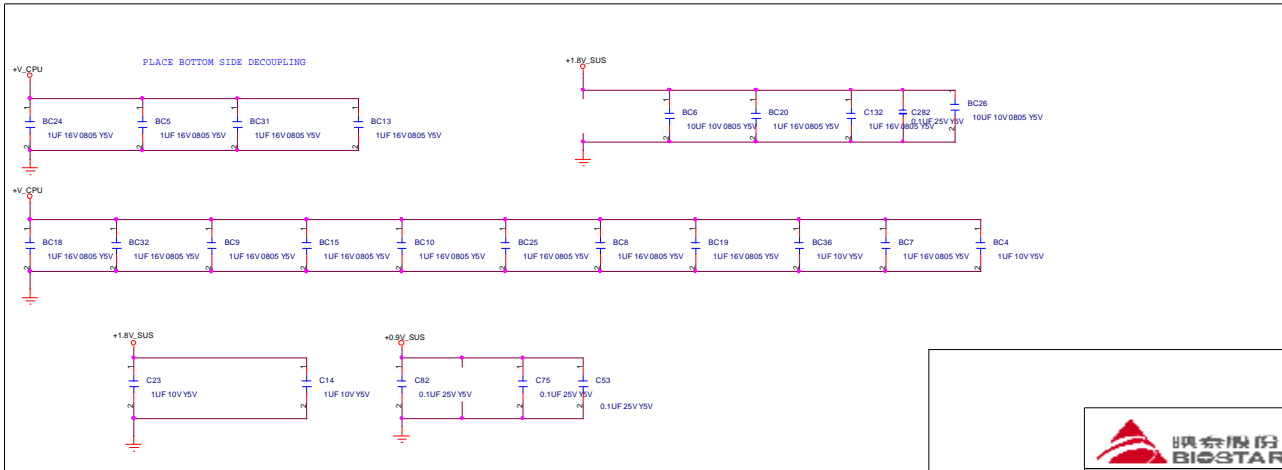
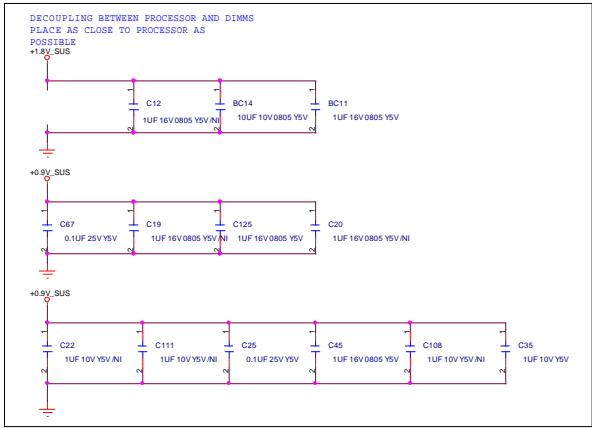


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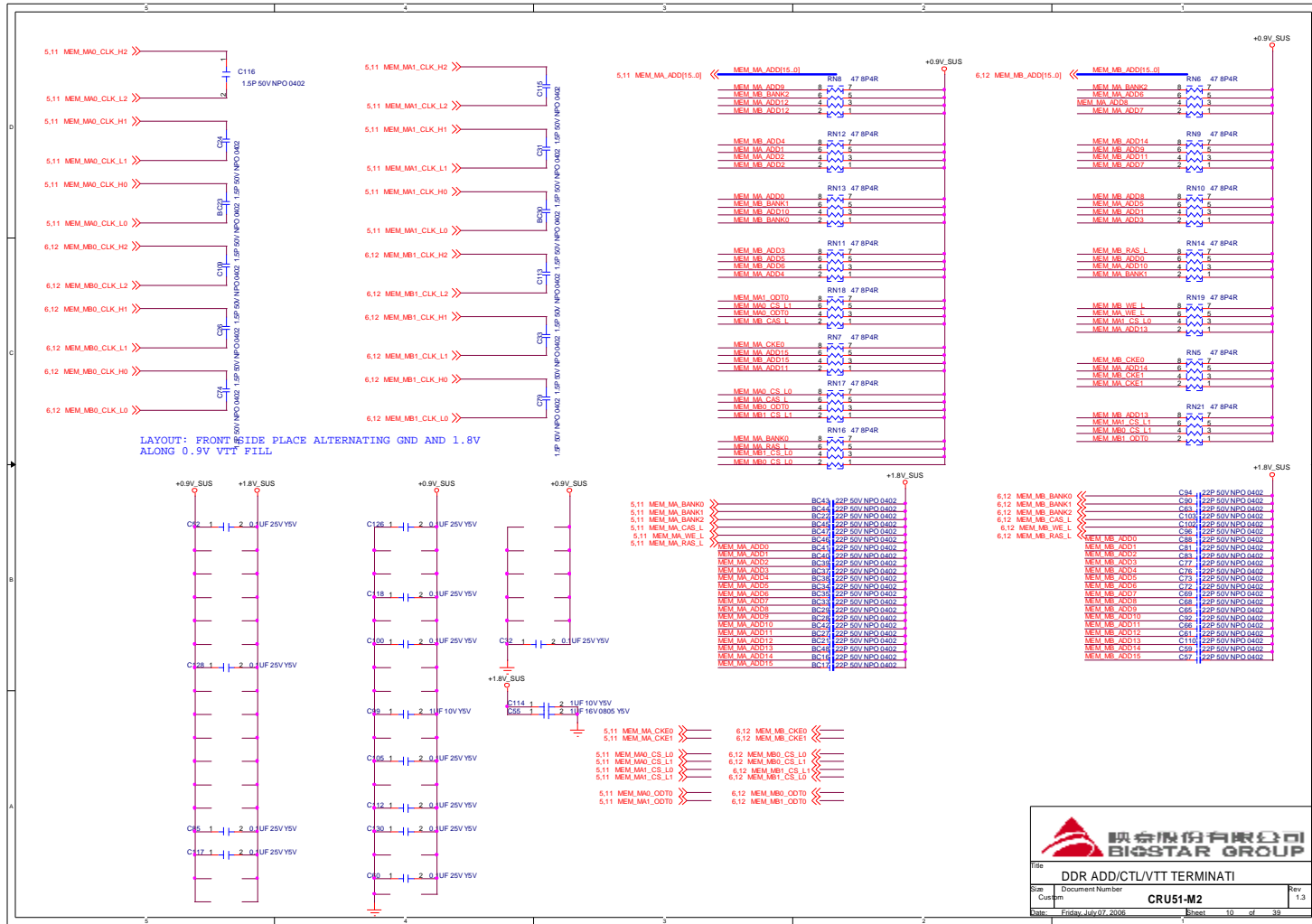
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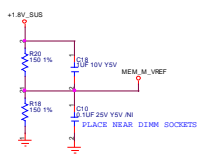
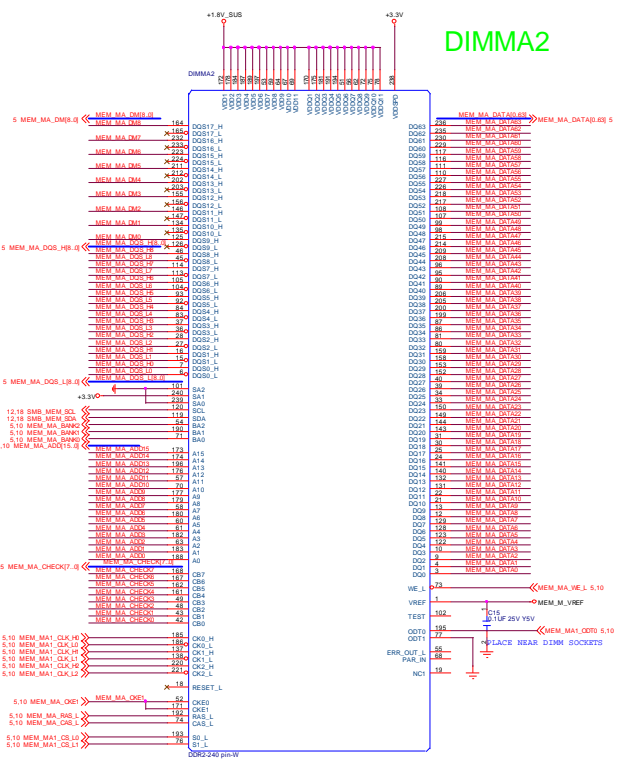
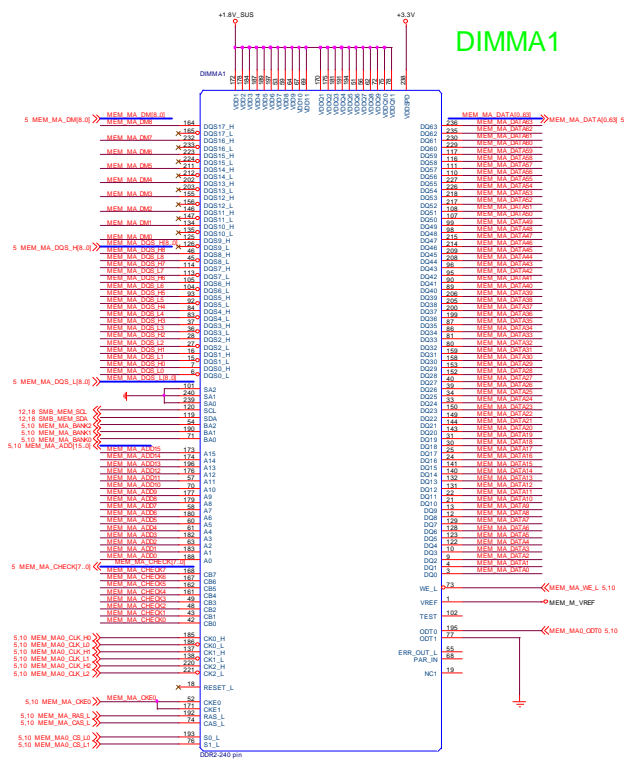
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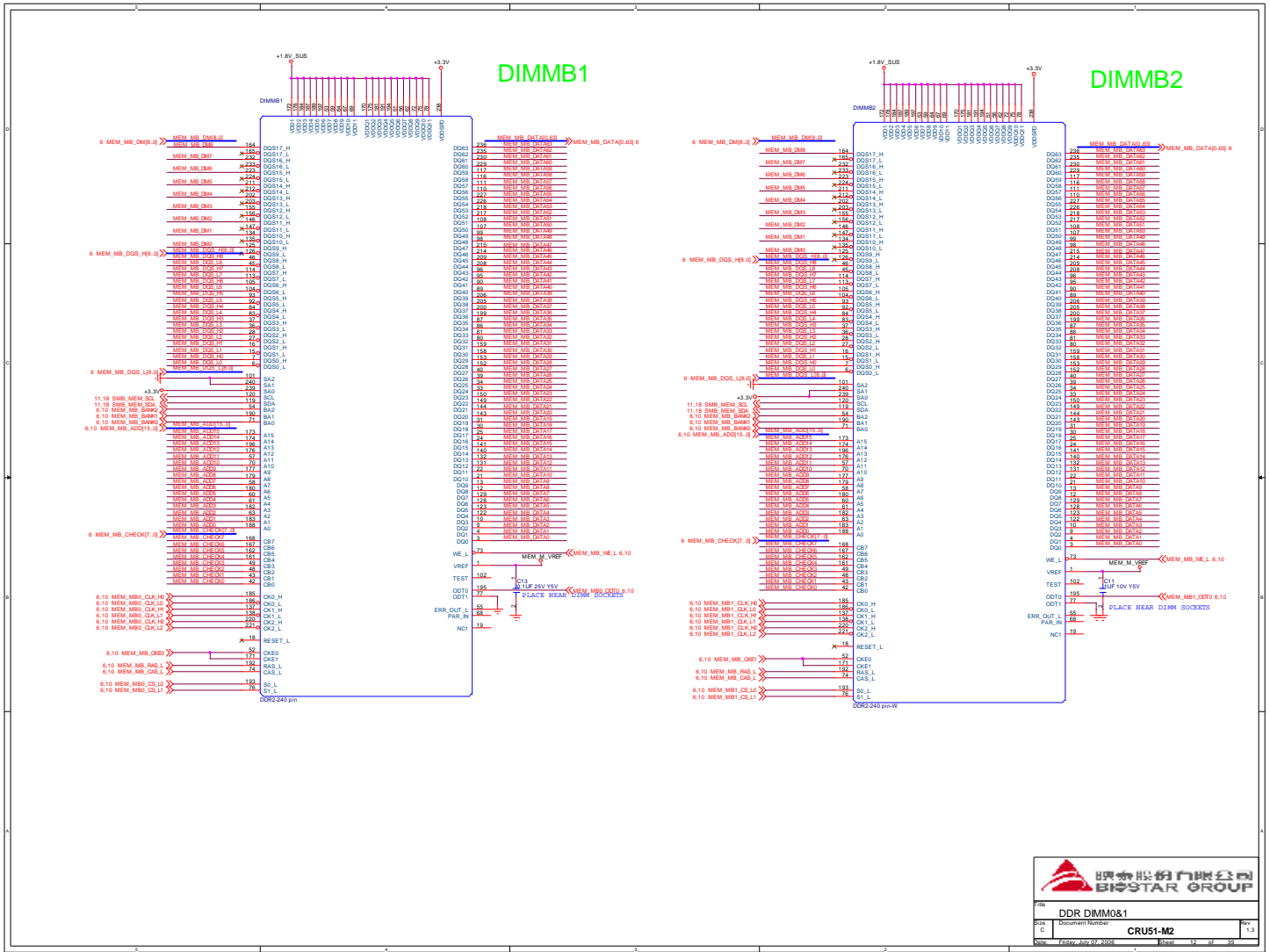
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DIMMA1

DIMMA2



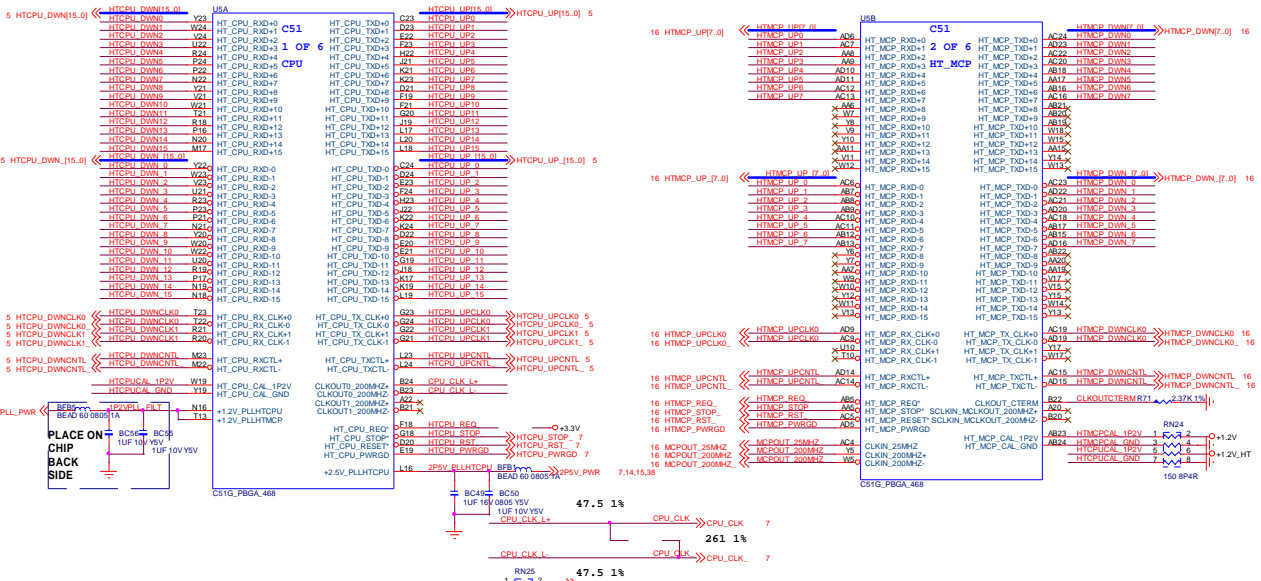
		DDR DIMM0&1	
Doc C	Document Number	CRU51-M2	
Date	Friday, July 27, 2006	Page	11 of 31





DDR DIMM0&1

 CRU51-M2



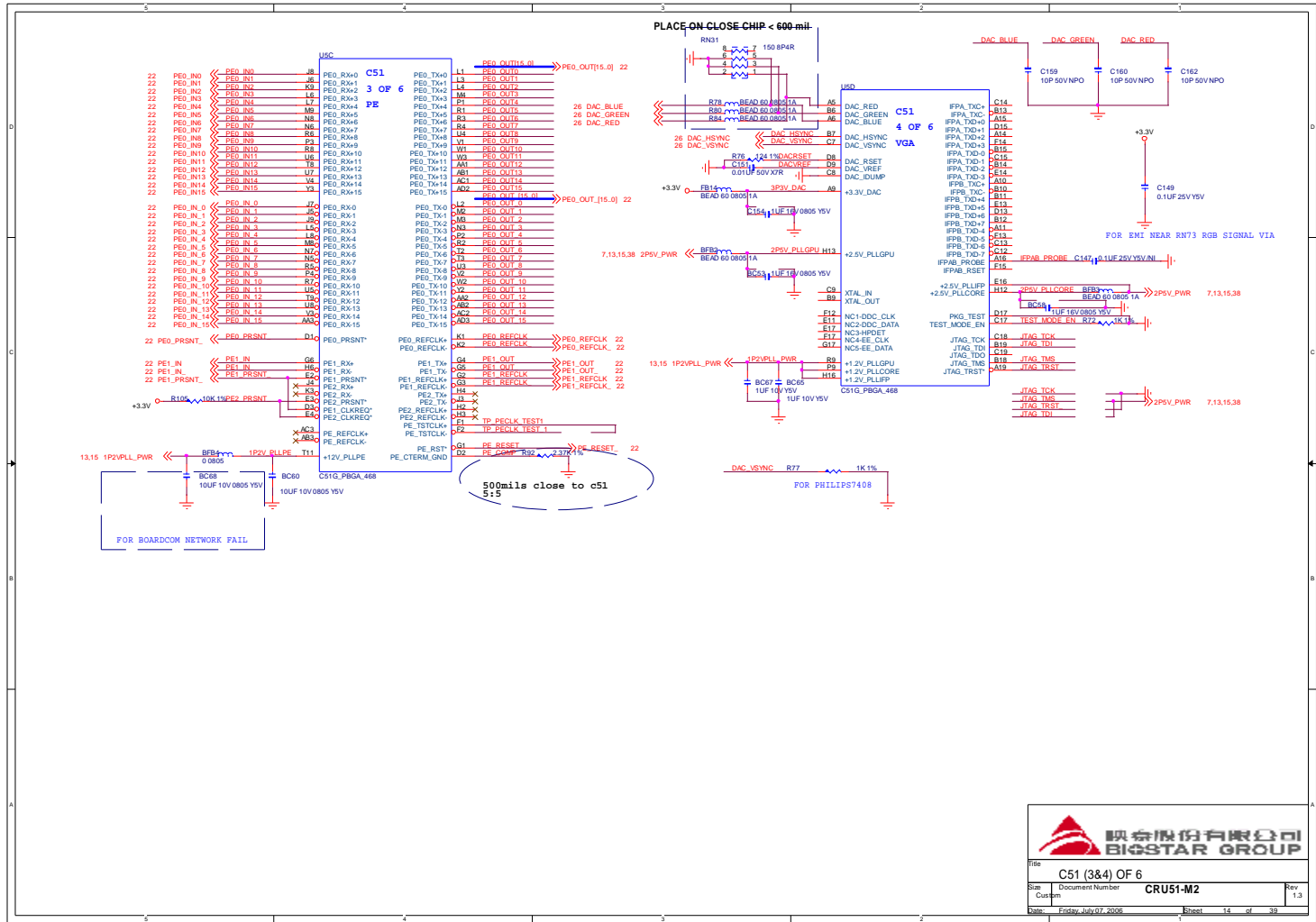
映泰股份有限公司
BIGSTAR GROUP

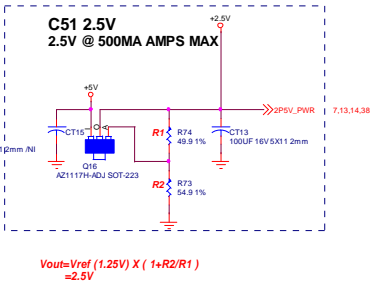
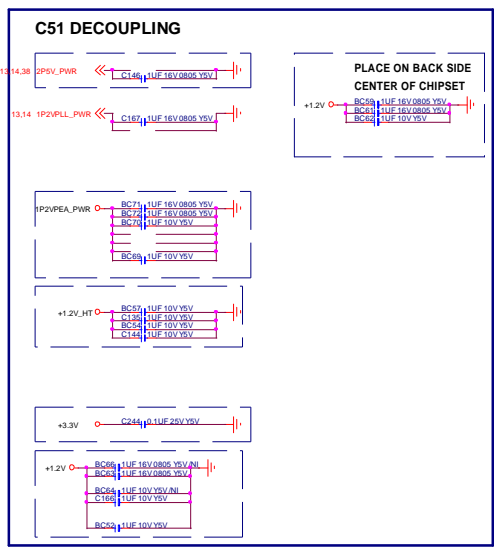
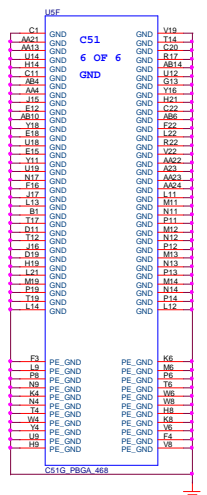
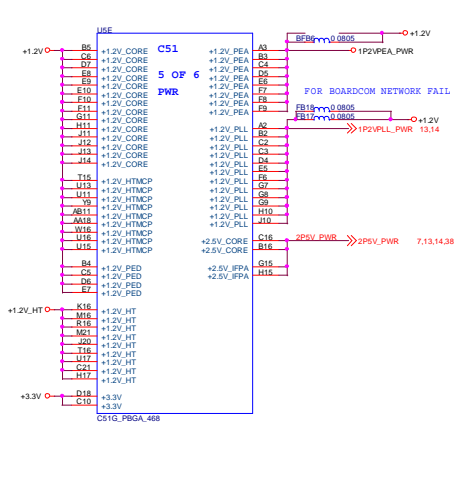
File: C51 (1&2) OF 6

Site: Document Number

Distm: CRU51-M2

Date: Thursday, November 30, 2006 Sheet: 13 of 39



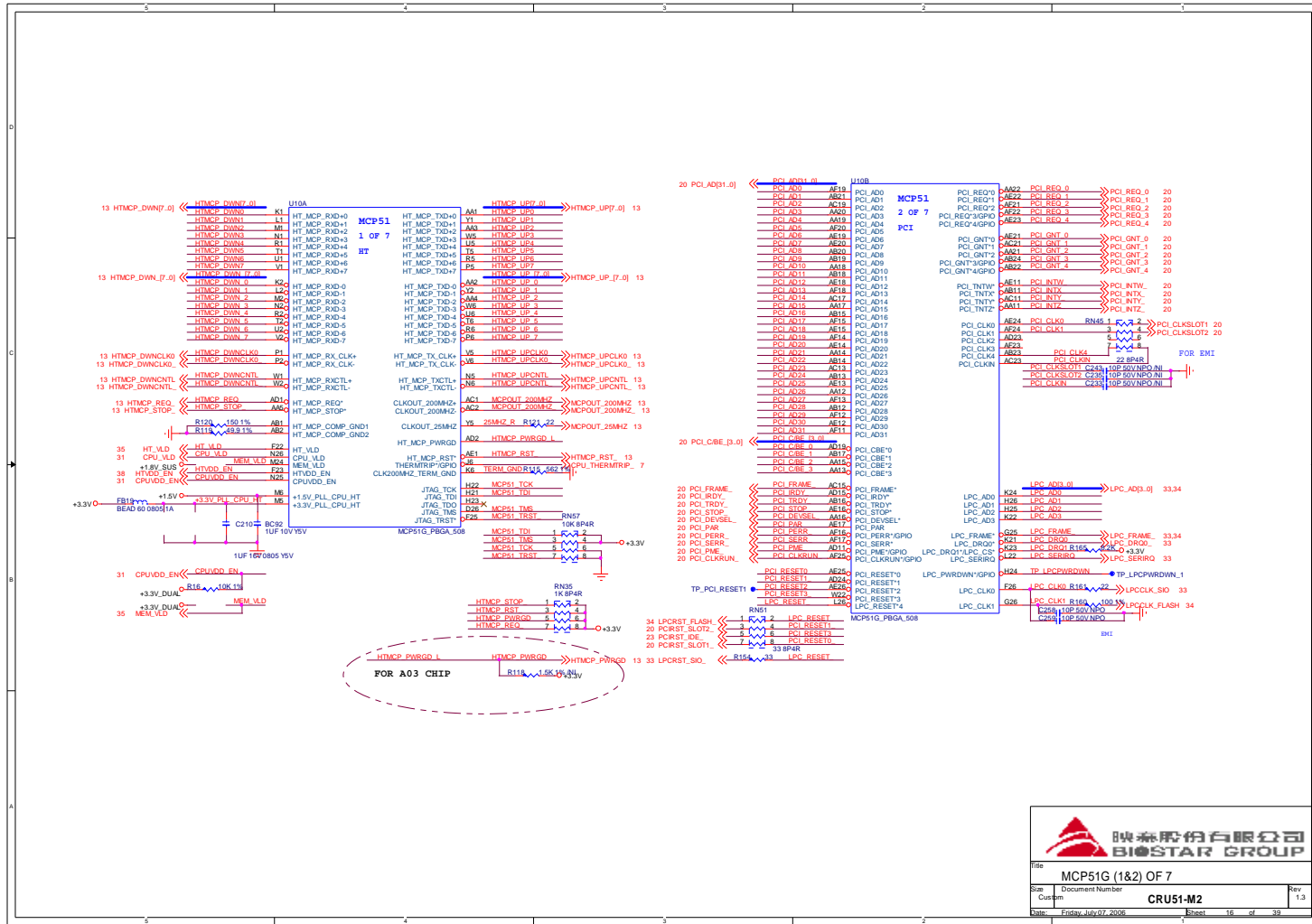


$$V_{out} = V_{ref} (1.25V) \times (1 + R2/R1) = 2.5V$$

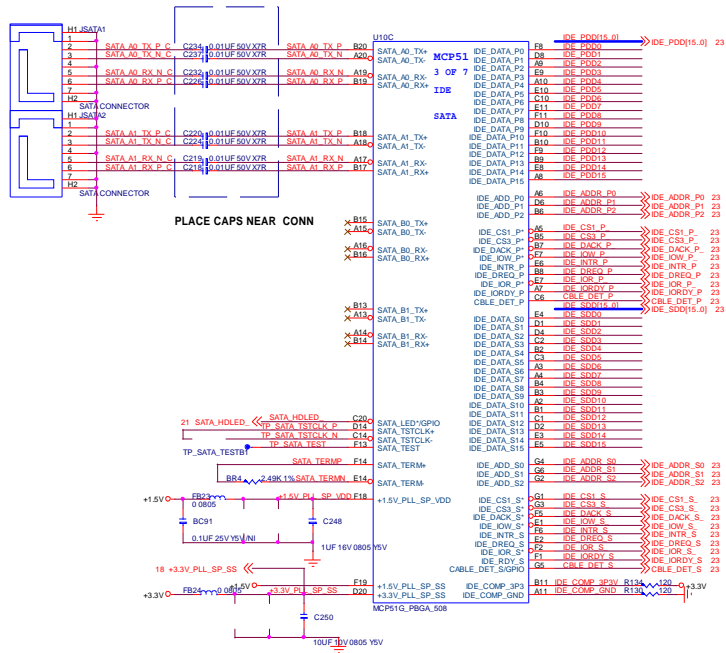


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Title		C51 (5&6) OF 6	
Spec		Document Number	
Custom		CRU51-M2	
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Title: MCP51G (1&2) OF 7
 Date: Friday, July 07, 2006
 Sheet: 16 of 39
 Rev: 1.3
 Document Number: CRU51-M2

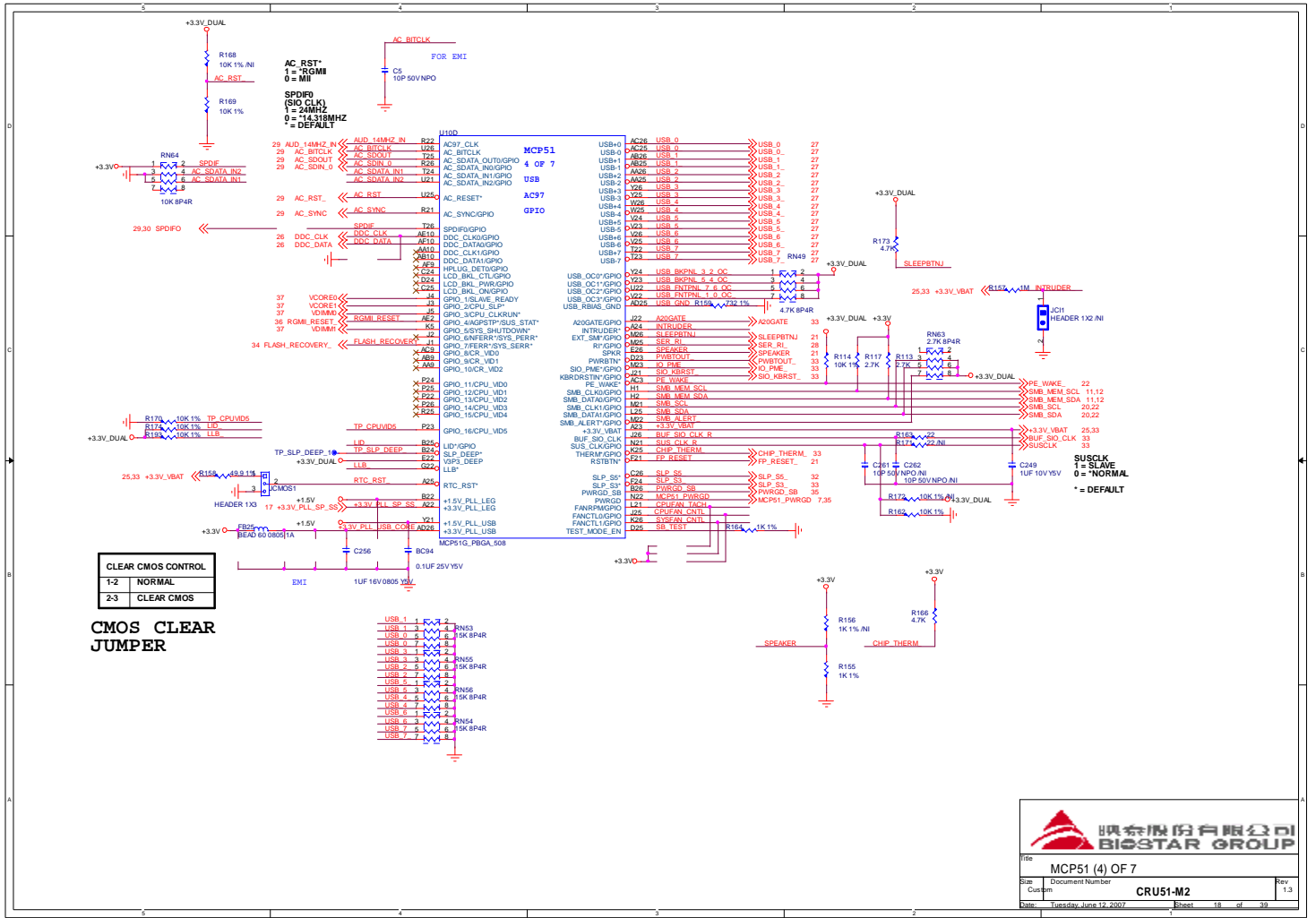



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BIOSSTAR GROUP

File: MCP51 (3) OF 7

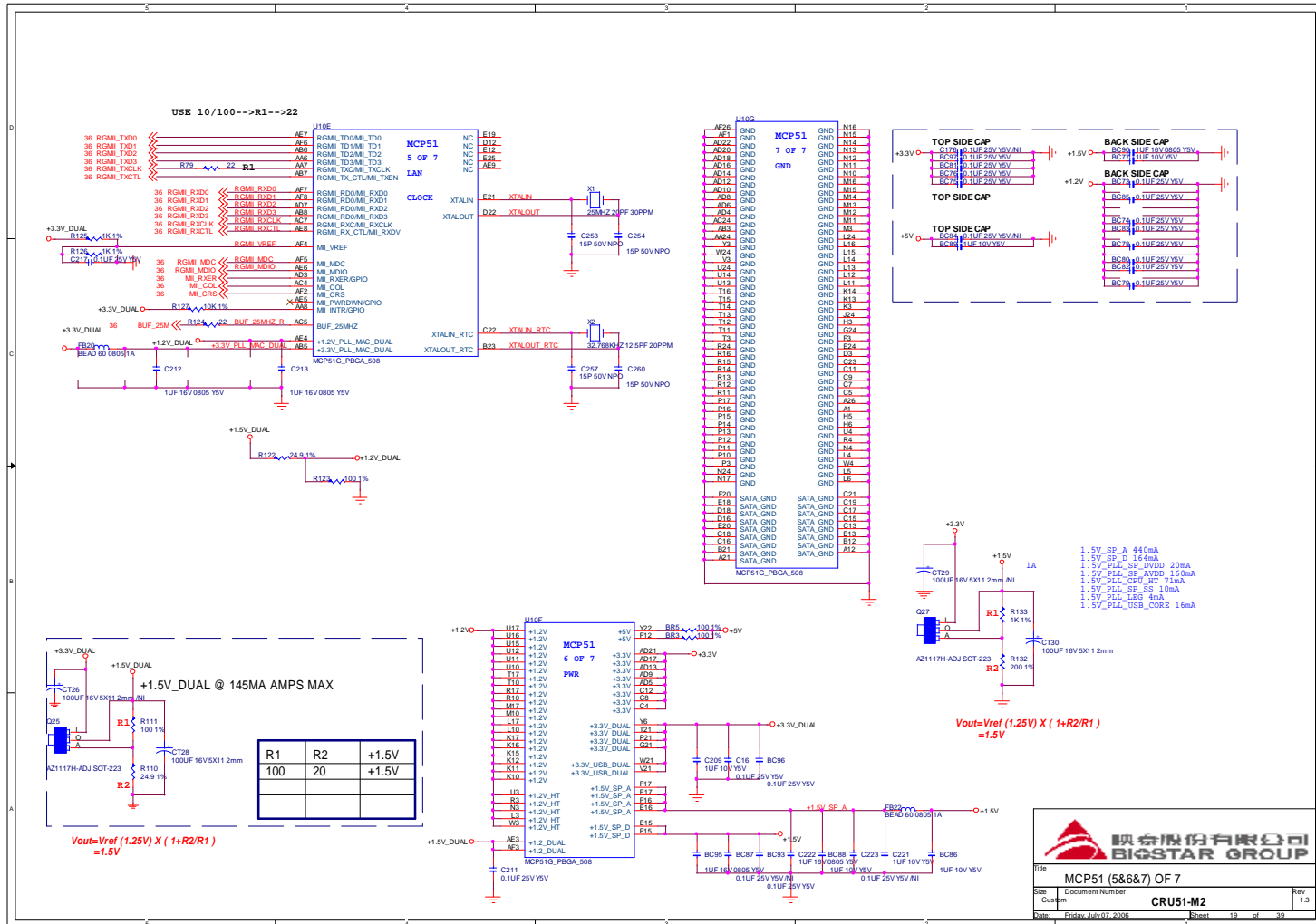
Sheet: Document Number: CRU51-M2

Date: Tuesday, October 17, 2006 Sheet: 17 of 39 Rev: 1.3



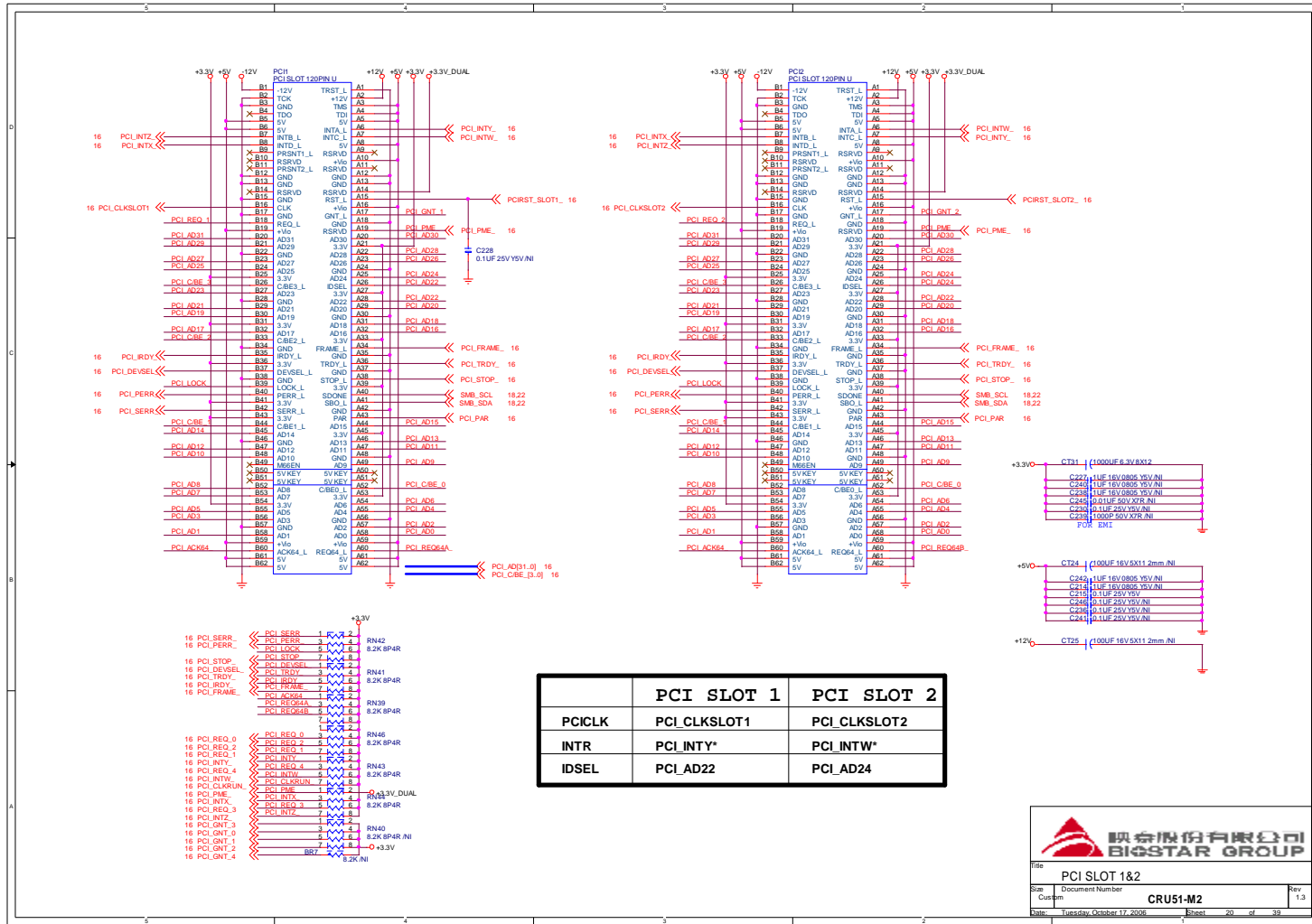

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BIOSTAR GROUP

File: MCP51 (4) OF 7
 Size: Document Number
 Custom: CRU51-M2
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BITSTAR GROUP

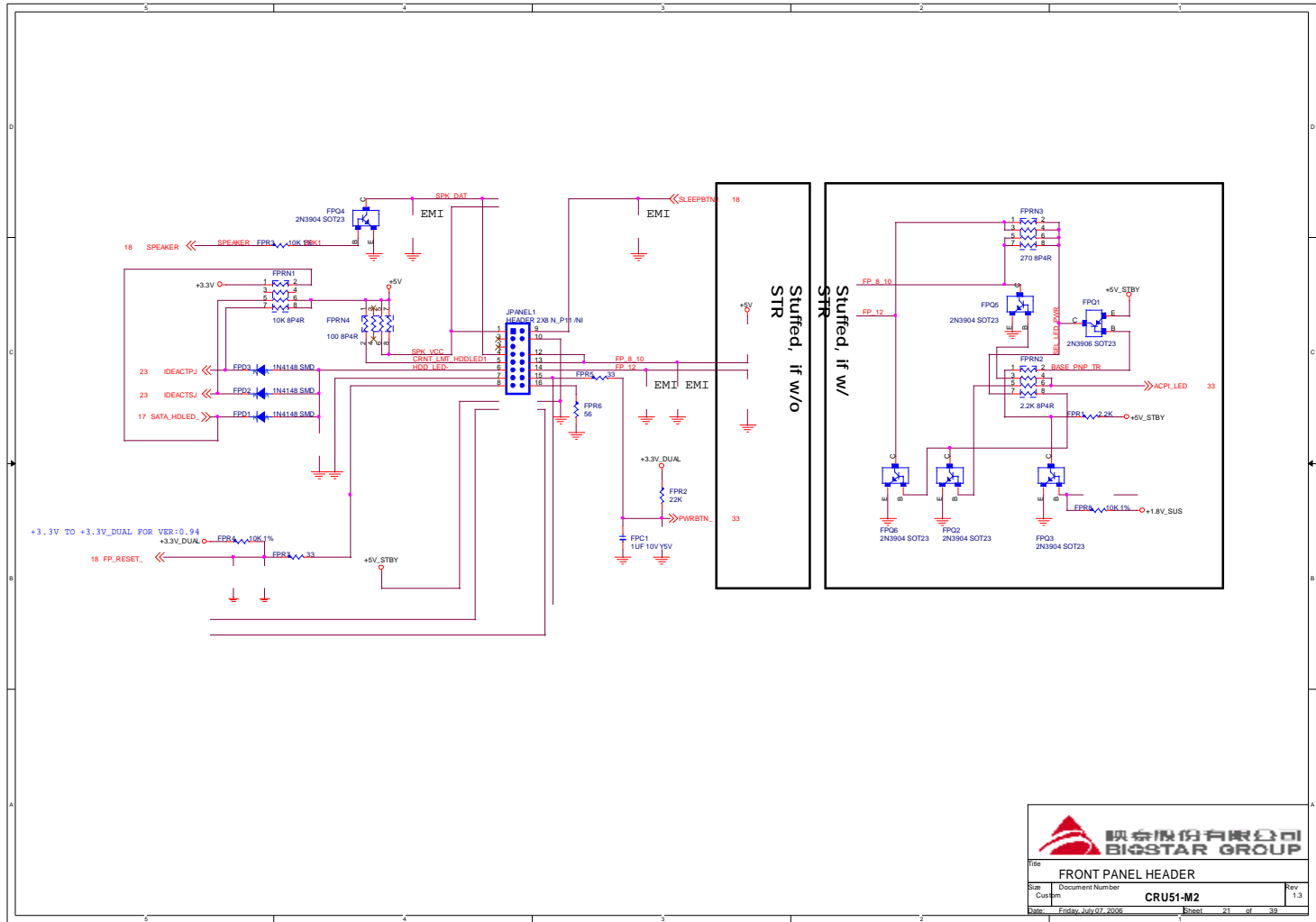
File: MCP51 (5&6&7) OF 7
 Size: Document Number
 Custom: CRU51-M2
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	PCI SLOT 1	PCI SLOT 2
PCICLK	PCI_CLKSLOT1	PCI_CLKSLOT2
INTR	PCI_INTY*	PCI_INTW*
IDSEL	PCI_AD22	PCI_AD24

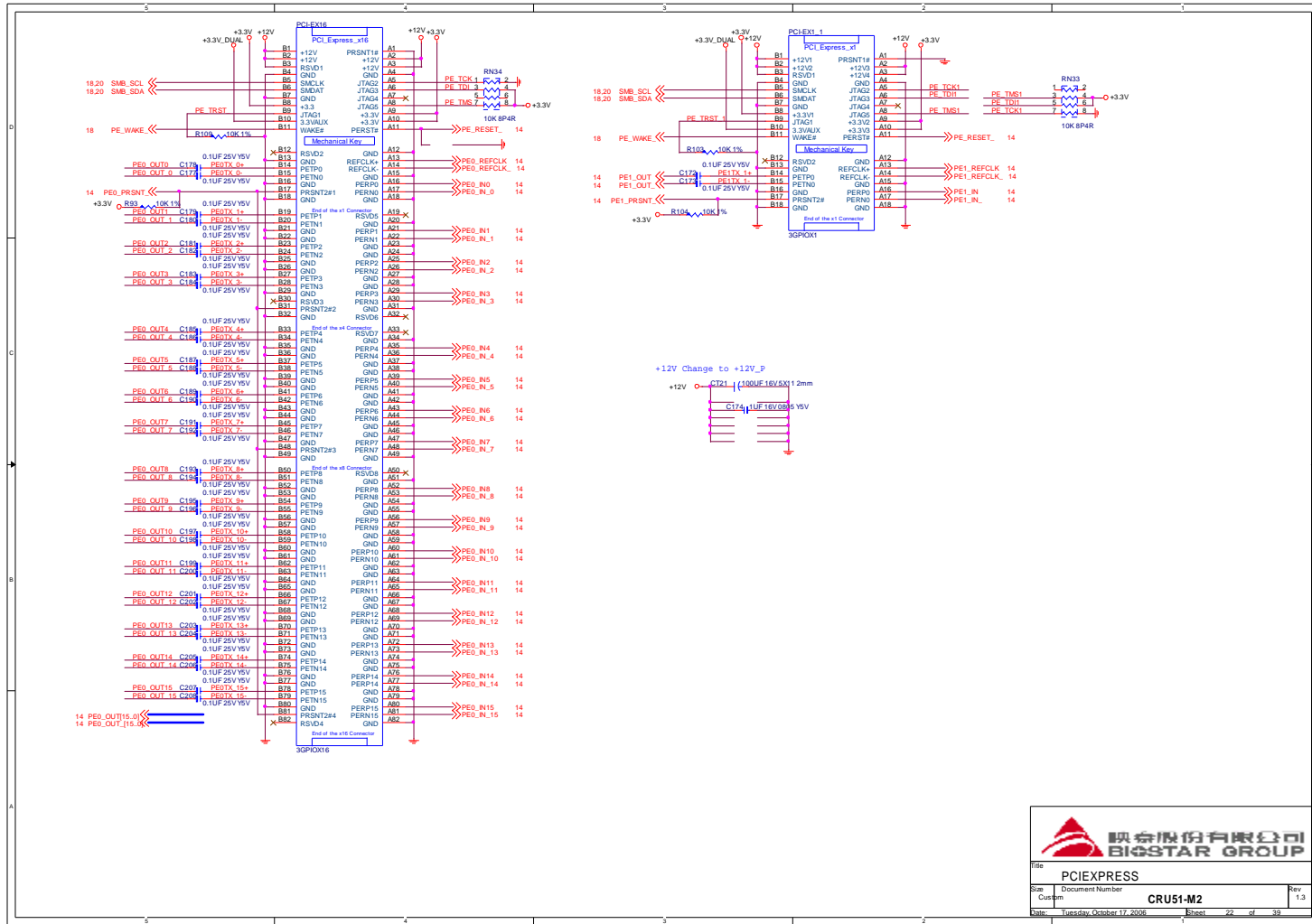
映泰股份有限公司
BIOSSTAR GROUP

File: PCI SLOT 1&2
 Title: Document Number
 Custom: CRU51-M2
 Date: Tuesday, October 17, 2006
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Title		Rev
FRONT PANEL HEADER		1.3
Size		Document Number
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Date:	Friday, July 07, 2006	Sheet 21 of 39



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Title: **PCIEXPRESS**

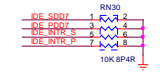
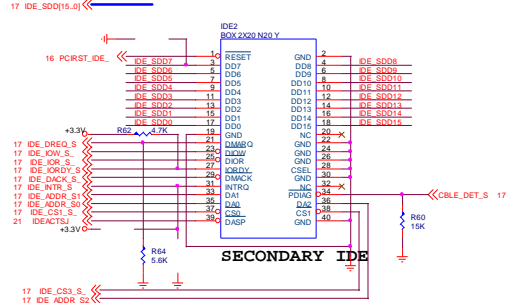
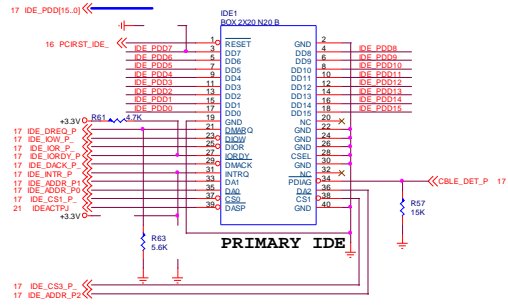
Size: Document Number

Custom: **CRU51-M2**

Date: Tuesday, October 17, 2006

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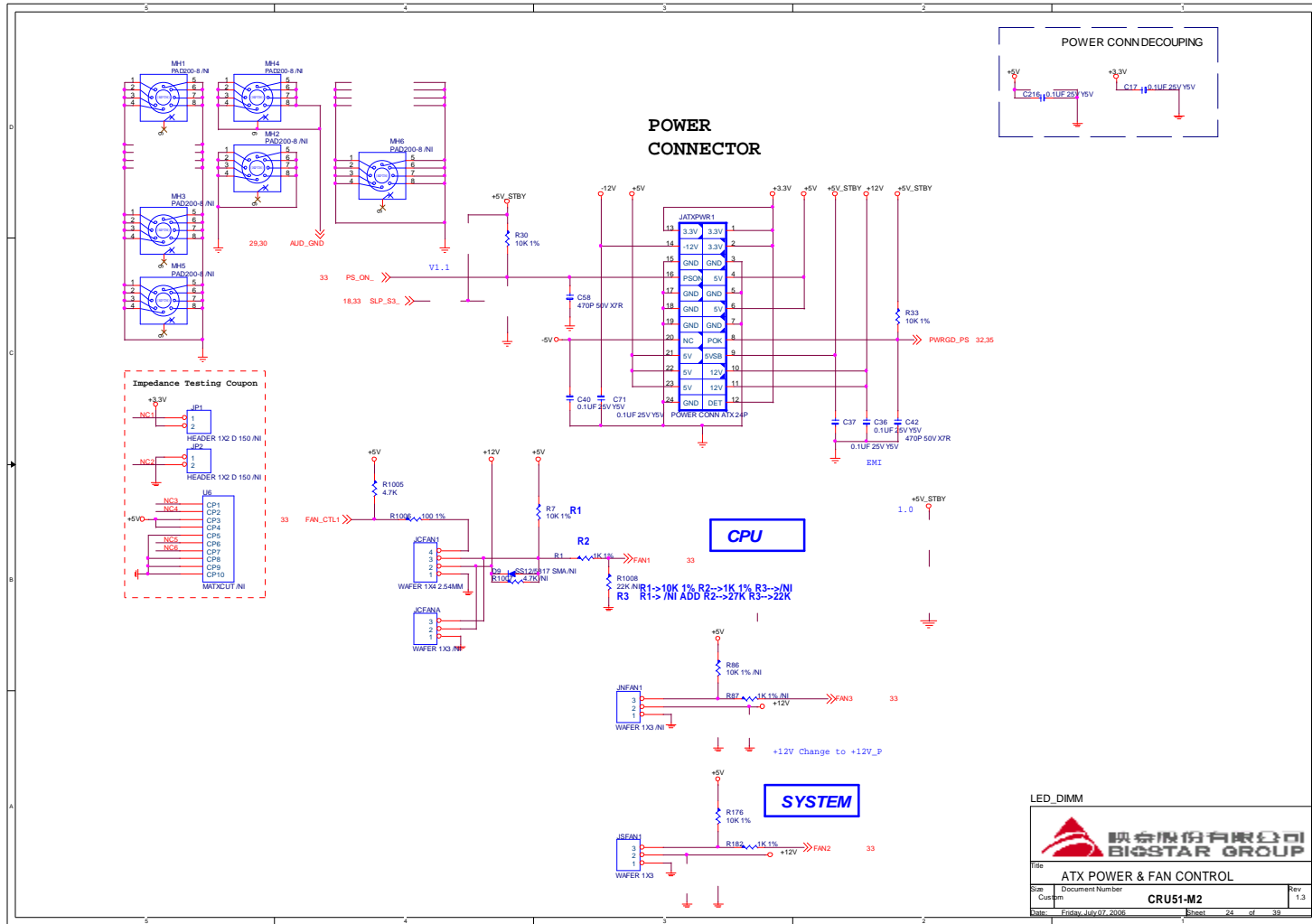
Rev: 1.3

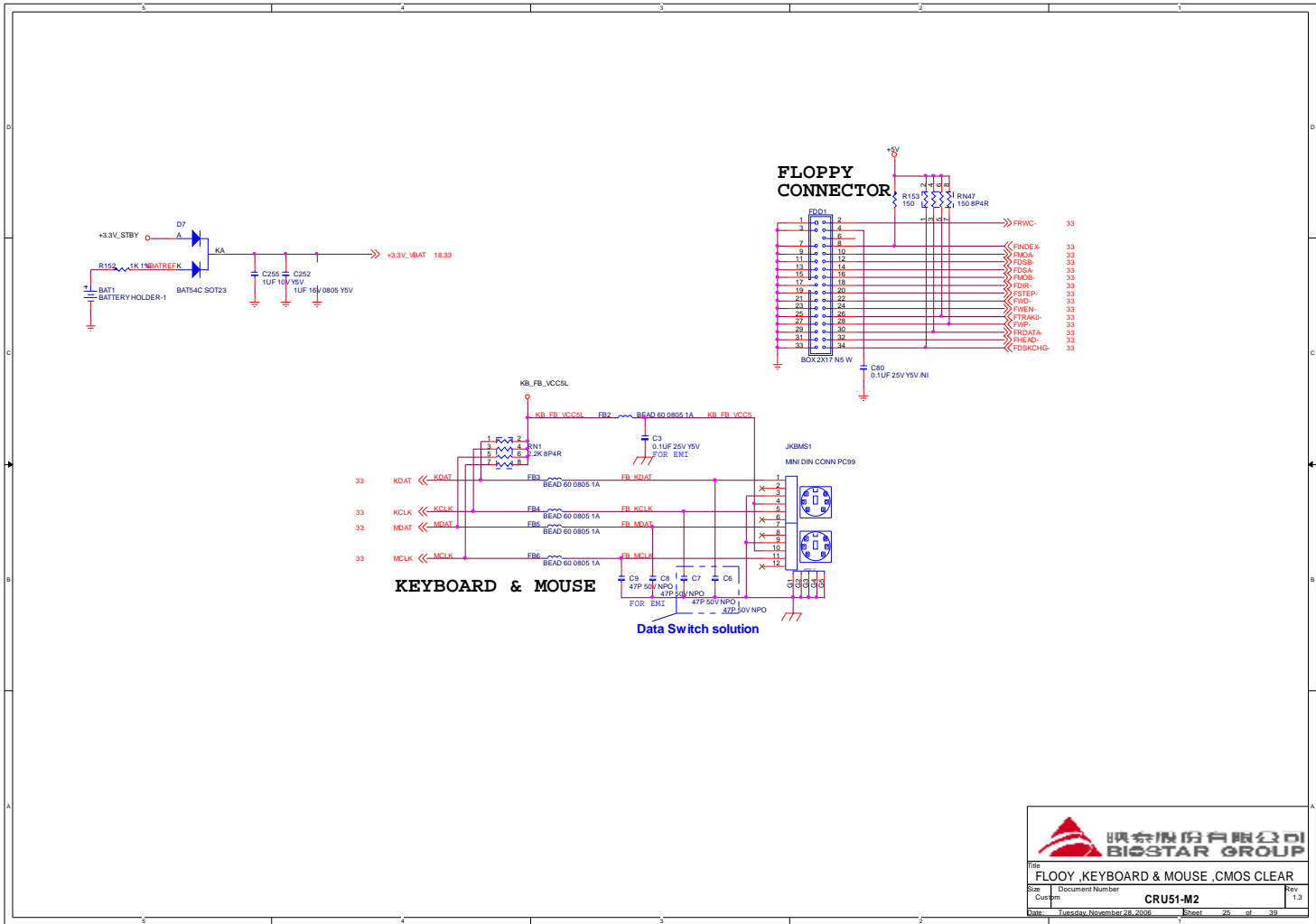


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BIGSTAR GROUP

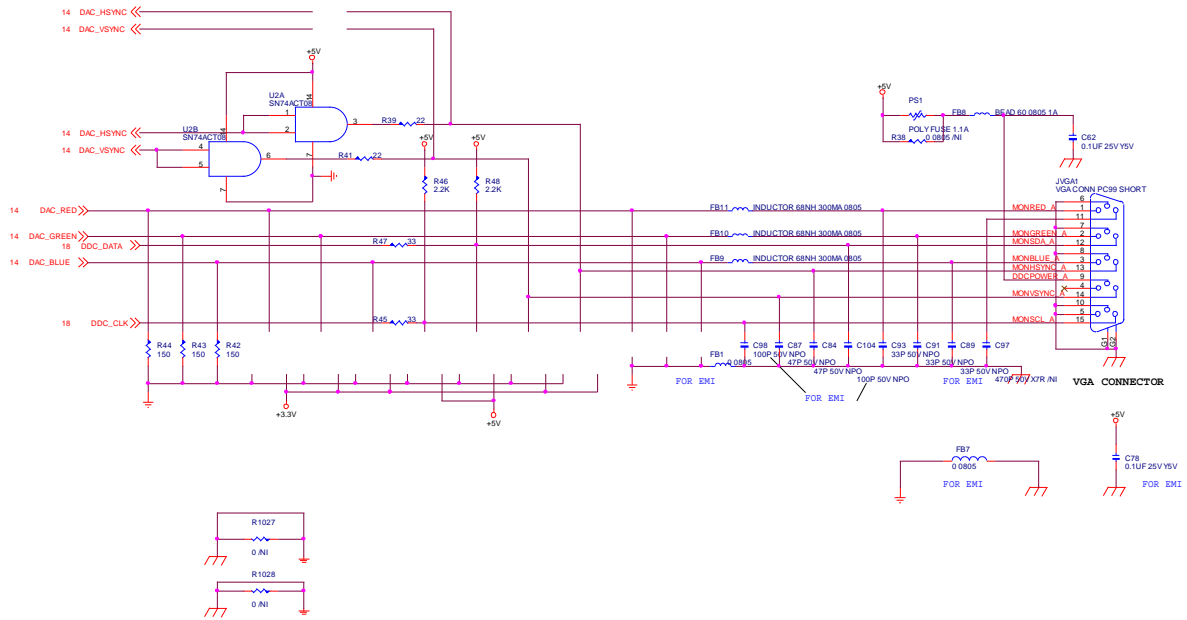
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Size:	Document Number	Rev:
Custom:	CRU51-M2	1.3
Date:	Friday, July 07, 2006	Sheet: 23 of 39



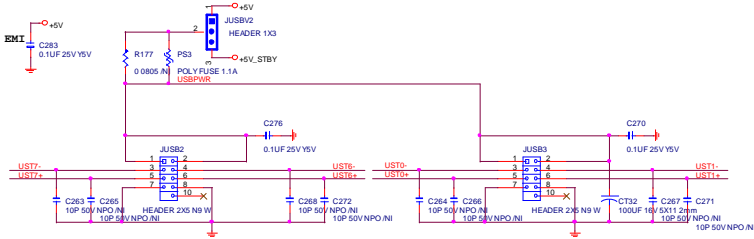
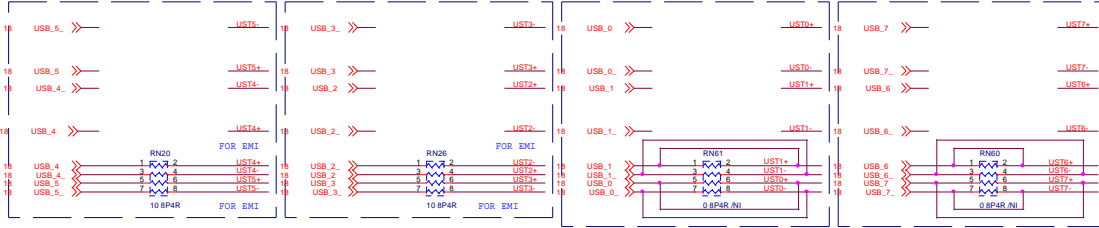
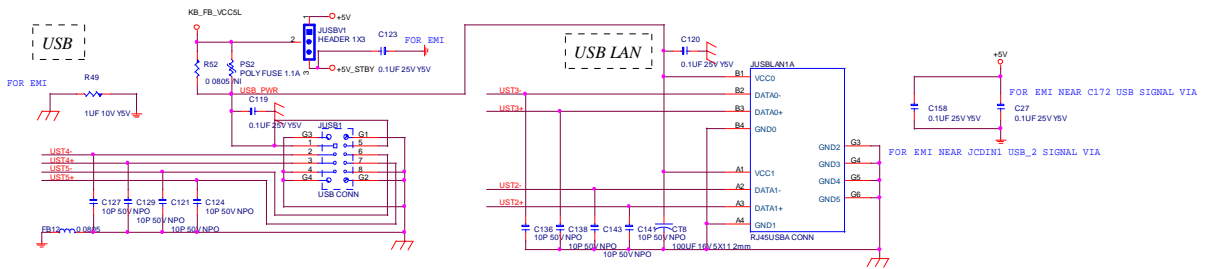



映泰股份有限公司 BIOSTAR GROUP	
Title: FLOOPY ,KEYBOARD & MOUSE ,CMOS CLEAR	
Size: Document Number	Rev: 1.3
Size: Custom	CRU51-M2
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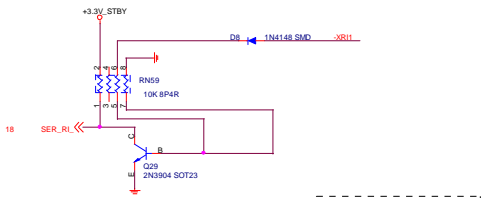

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BIGSTAR GROUP

Title		VGA CONNECTOR	
Size	Document Number	Customer	CRU51-M2
Date	Friday, July 07, 2006	Sheet	26 of 39
		Rev	1.3

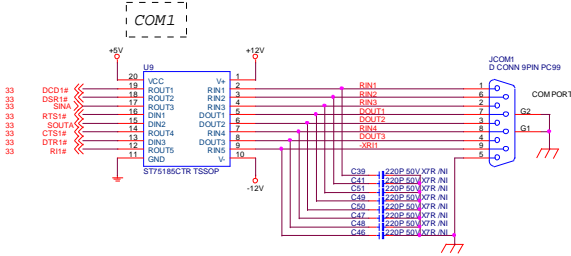



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BIGSTAR GROUP

USB INTERFACE	
Title	Document Number
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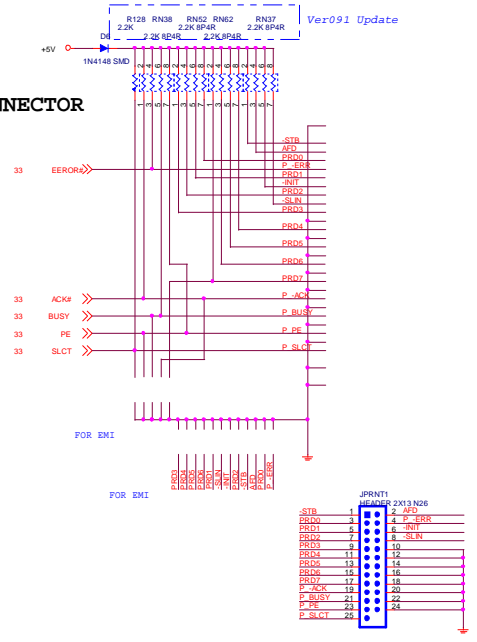


WAKE ON LAN



PARALLEL - CONNECTOR

33	PD3	P_PDD3	1	2	PDD3
33	PD2	P_PDD2	3	4	PDD2
33	PD1	P_PDD1	5	6	PDD1
33	PD0	P_PDD0	7	8	PDD0
33	PD7	P_PDD7	1	2	PDD7
33	PD6	P_PDD6	3	4	PDD6
33	PD5	P_PDD5	5	6	PDD5
33	PD4	P_PDD4	7	8	PDD4
33	STB#	P_STB	1	2	STB
33	ALF#	P_ALF	3	4	ALF
33	INT#	P_INT	5	6	INT
33	SLECTN	P_SLN	7	8	SLN
		RN48			33 BP4R



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Doc: SERIAL & PARALLEL

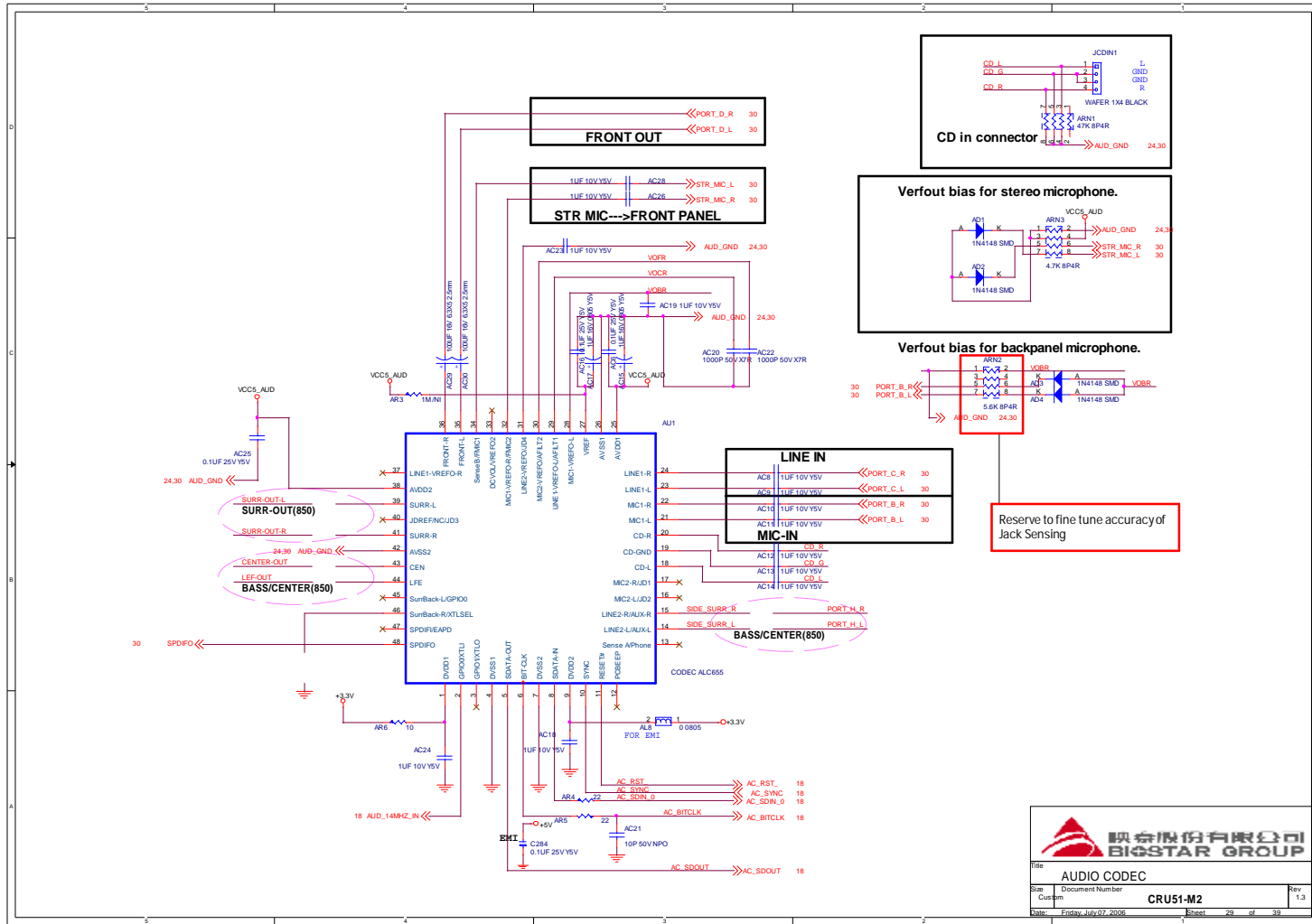
Site: Document Number

Custom: CRU51-M2

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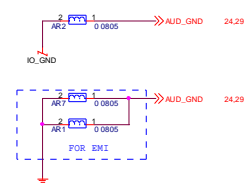
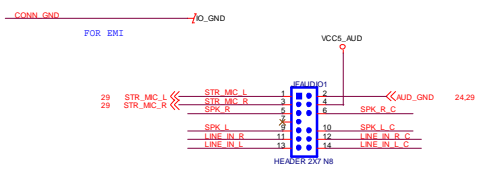
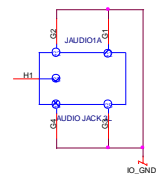
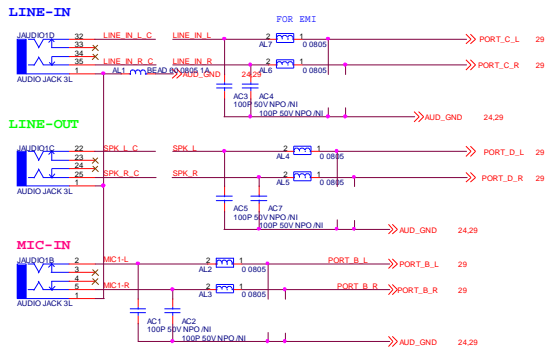
Rev: 1.3



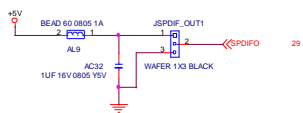
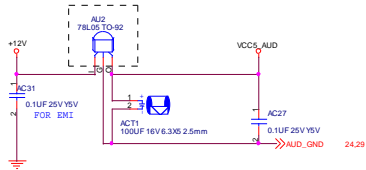
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Title		Rev
AUDIO CODEC		1.3
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AUDIO ANALOG POWER

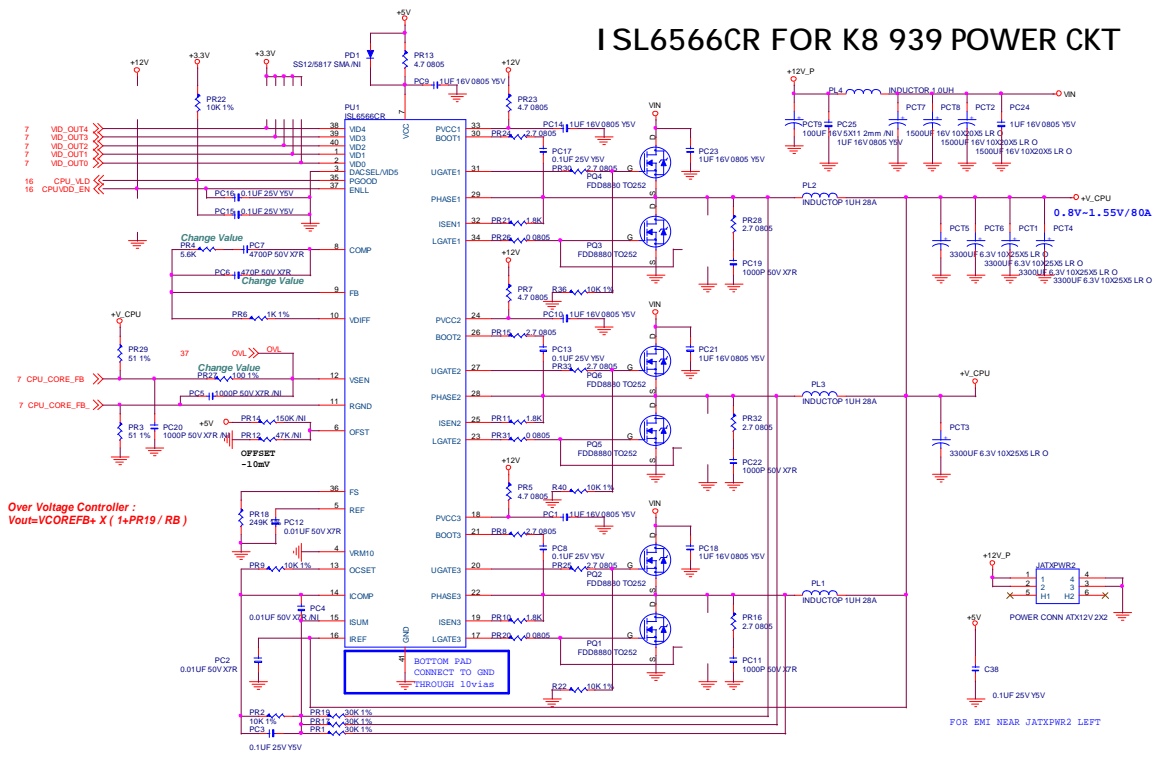




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BIGSTAR GROUP

Title: **AUDIO PORT**
 Size: Document Number
 Custom: **CRU51-M2**
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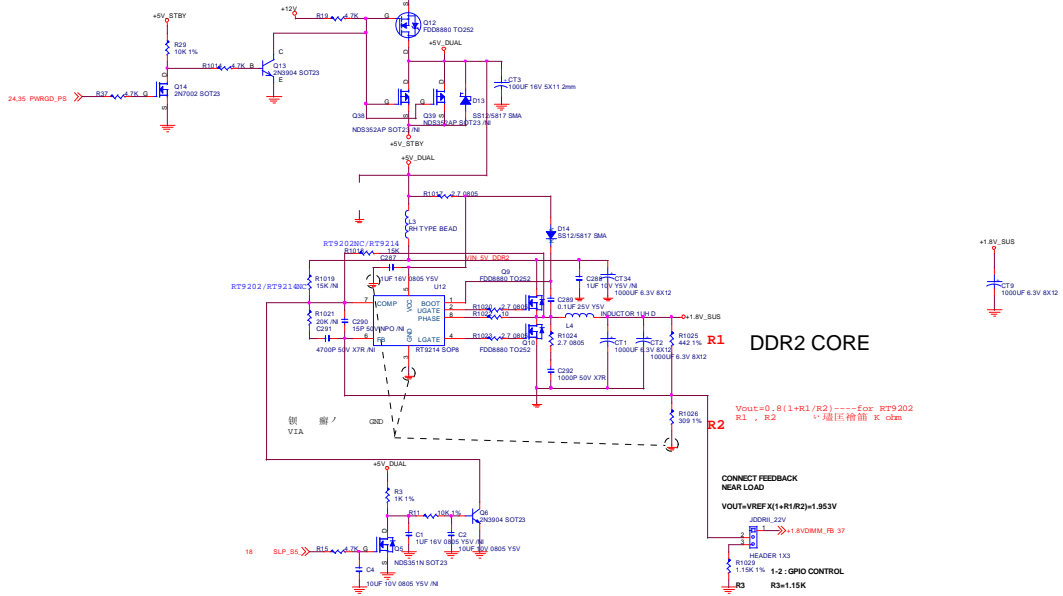
ISL6566CR FOR K8 939 POWER CKT




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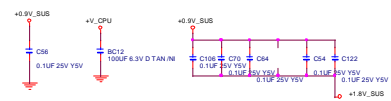
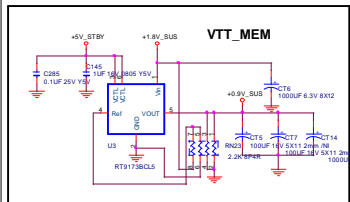
Title		VCORE POWER SUPPLY	
Size	Document Number	CRU51-M2	
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MEM_VDD
MEM_STR

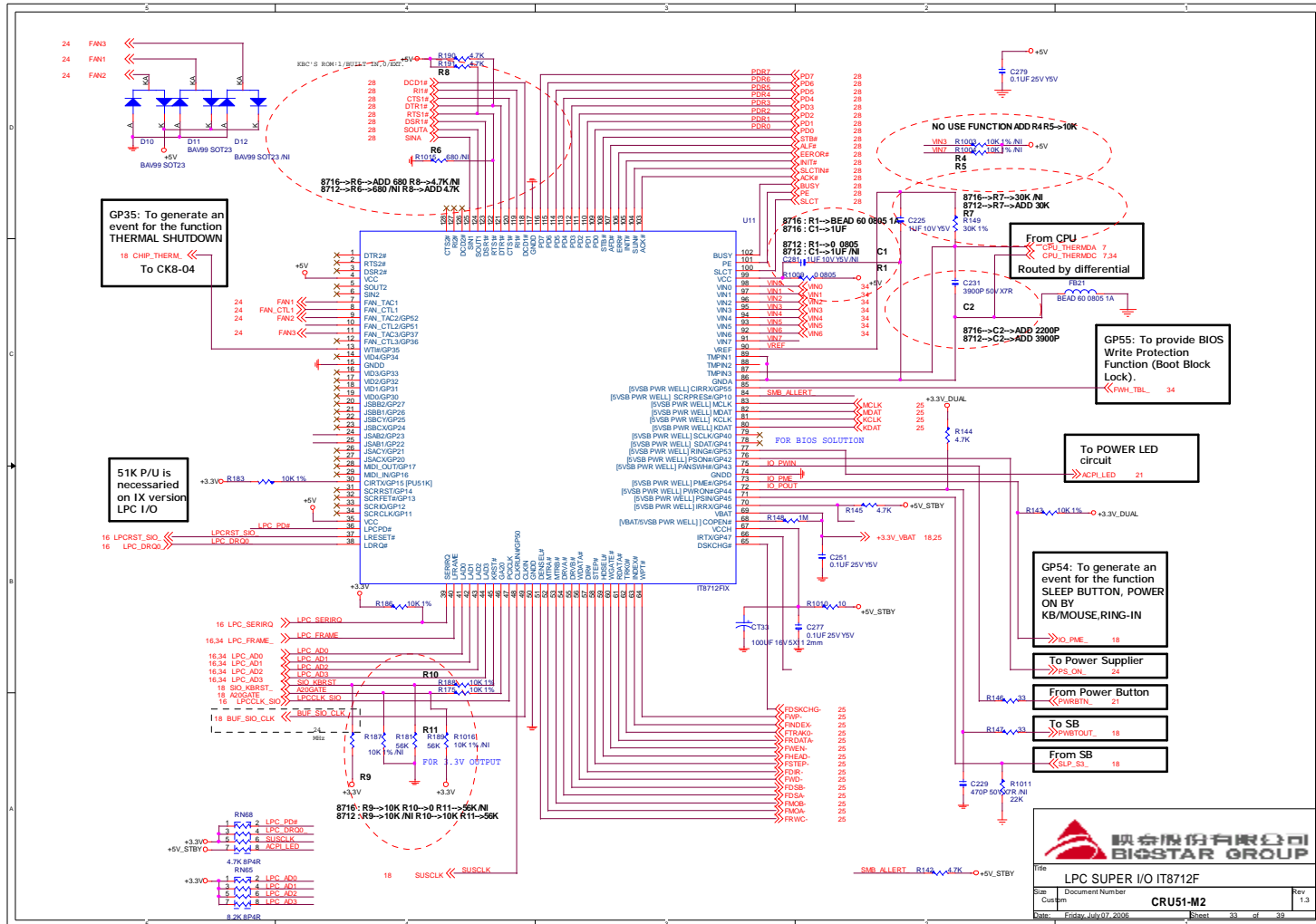


DDR2 CORE

$V_{out} = 0.8(1 + R1/R2)$ --- For RT9202
 $R1, R2$ 电阻比例
 CONNECT FEEDBACK NEAR LOAD
 $V_{OUT} = V_{REF} \times (1 + R1/R2) = 1.95V$
 JDDR1_2V
 R3=1.15K
 R3=1.15K



PLL_DELAY / PWRGD / MEM_VREG
 Document Number: CRU51-M2
 Rev: 1.3
 Date: 10/16/2017

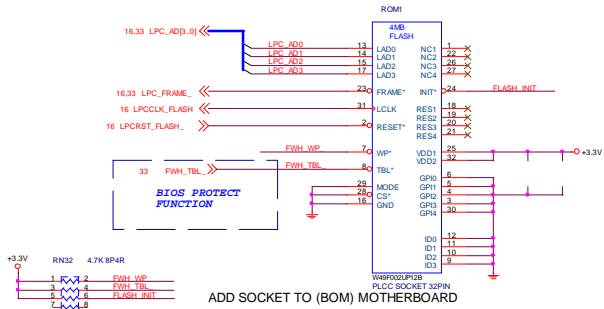


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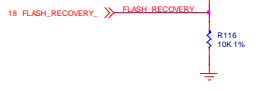
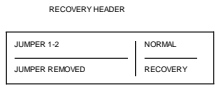
File: **LPC SUPER I/O IT8712F**

Size: Document Number **CRU51-M2** Rev: 1.3

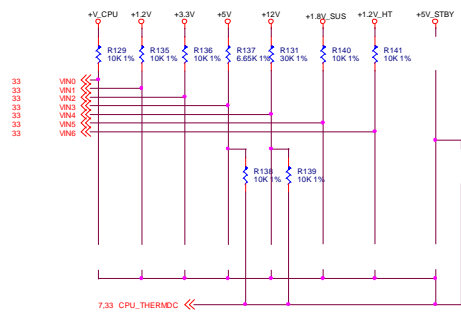
Date: Friday, July 07, 2006 Sheet: 33 of 39



ADD SOCKET TO (BOM) MOTHERBOARD



Voltage Sensing



hardware monitor

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Title: FLASH ROM & H/W MON

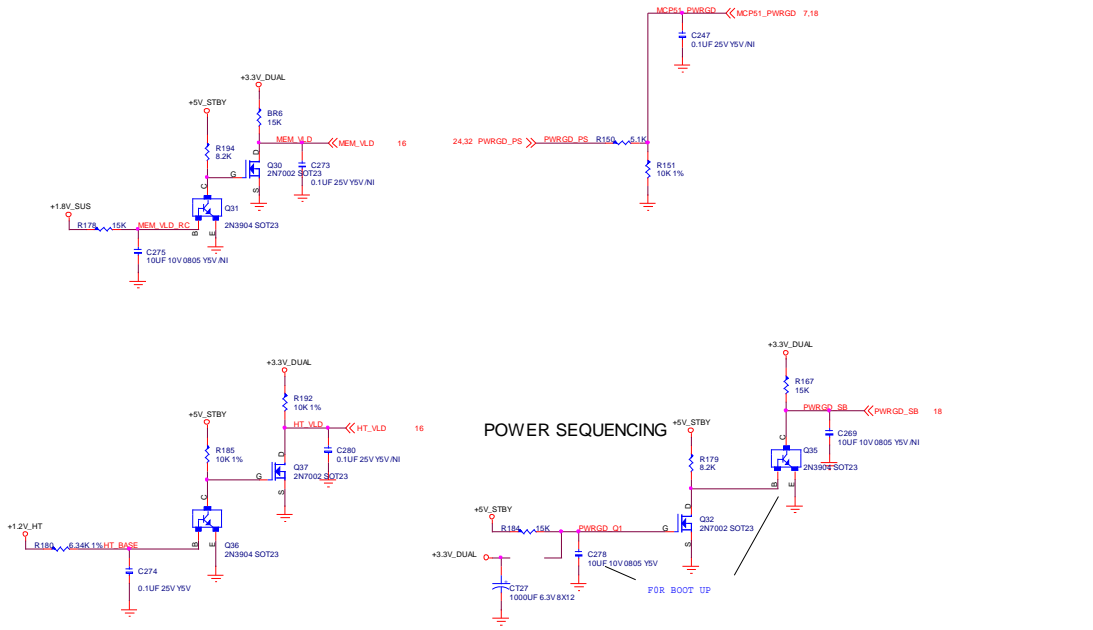
Size: Document Number

Date: Friday, July 07, 2006


Sheet: 34 of 39

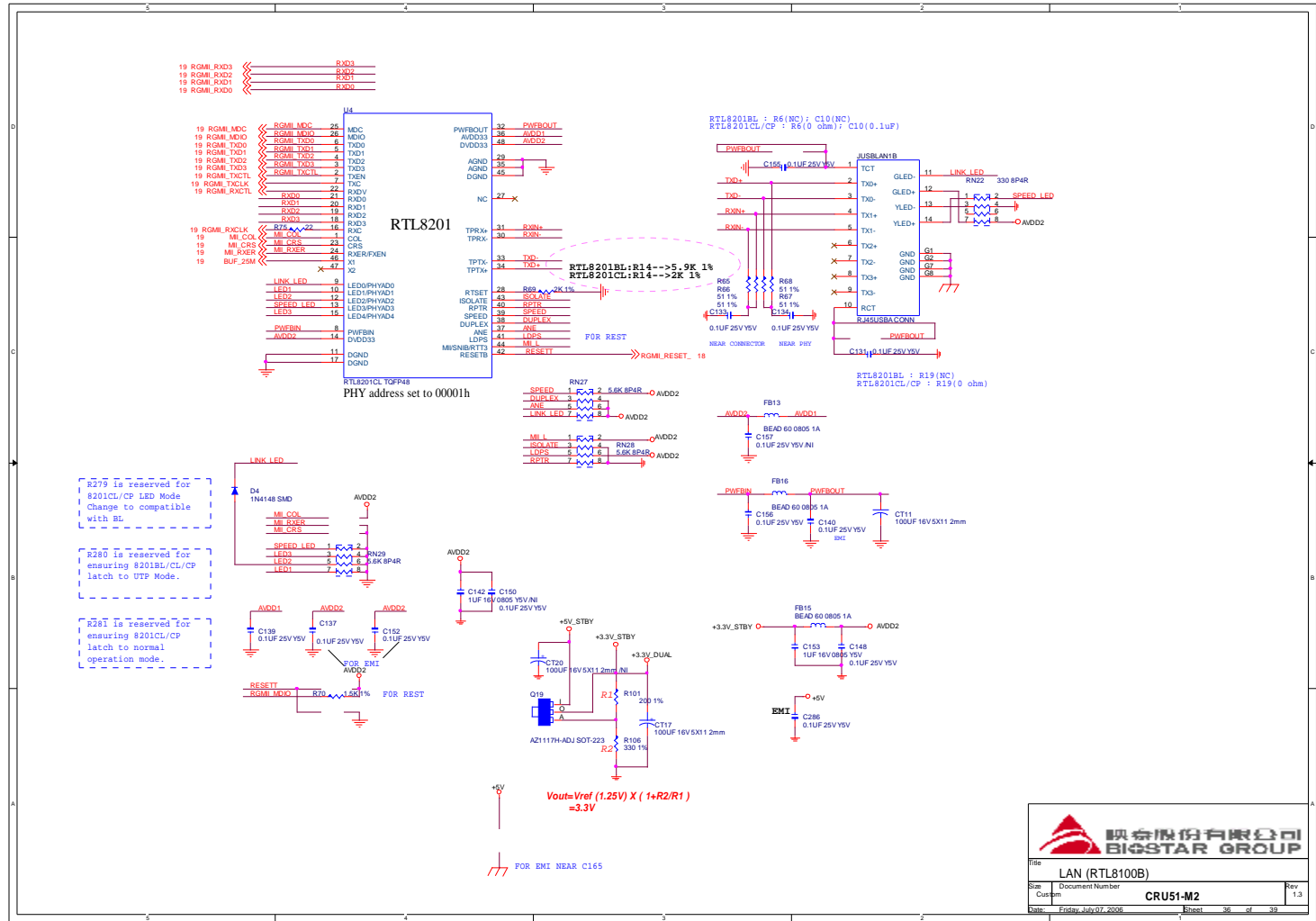
Rev: 1.3

CRU51-M2



POWER SEQUENCING

 映泰股份有限公司 BIGSTAR GROUP	
Title: POWER SEQUENCING	
Size: Custom	Document Number: CRU51-M2
Date: Friday, July 07, 2006	Rev: 1.3
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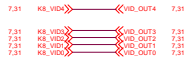
R279 is reserved for 8201CL/CP LED Mode Change to compatible with BL

R280 is reserved for ensuring 8201B/CL/CP latch to UTP Mode.

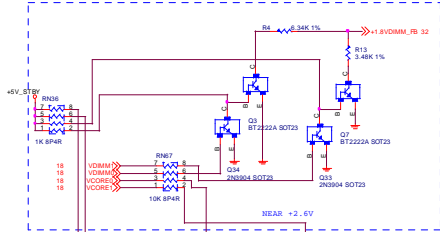
R281 is reserved for ensuring 8201B/CL/CP latch to normal operation mode.

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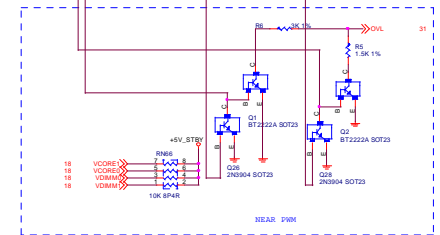
Title	LAN (RTL8100B)	
Size	Document Number	Rev
Customer	CRU51-M2	1.3
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Dimmer output	DIM0 GPIO3	DIM1 GPIO4
Output	1	1
2.22V	1	1
2.82V	1	1
2.92V	1	1



+1.8VVDIMM_FB	VDIMM0	VDIMM1
Default 1.844V	1	1
2.00V	0	1
2.045V	1	0
2.100V	0	0



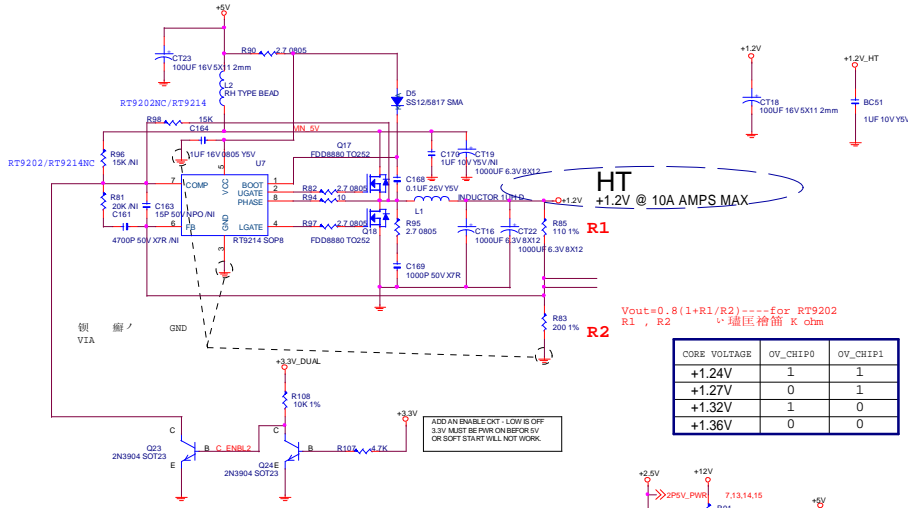
VCORE_OVL	VCORE0	VCORE1
Default 1.560V	1	1
1.602V	0	1
1.653V	1	0
1.705V	0	0


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OVER VOLTAGE

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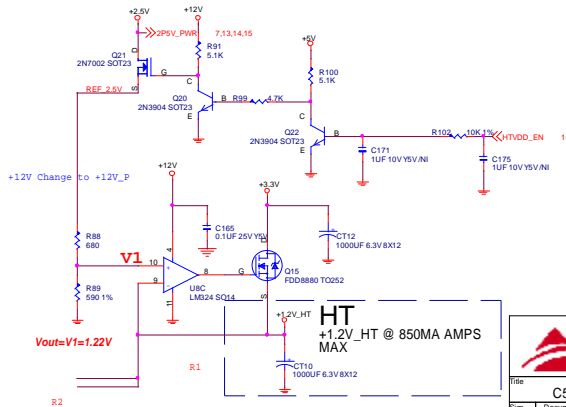
CK51 CORE



CORE VOLTAGE	OV_CHIP0	OV_CHIP1
+1.24V	1	1
+1.27V	0	1
+1.32V	1	0
+1.36V	0	0

+1.2V_HT	OV_HT0	OV_HT1
+1.2V	1	1
+1.25V	0	1
+1.3V	1	0
+1.35V	0	0

$V_{out} = 1.22X(1 + R1/R2)$



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File: C51 CORE
Size: Custom
Date: Friday, July 07, 2006
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JUSBV1(1_2)
JUMPER 2P R

JUSBV2(1_2)
JUMPER 2P R

JFAUDIO1(5_6)
JUMPER 2P B

JFAUDIO1(9_10)
JUMPER 2P B


JFAUDIO1(11_12)
JUMPER 2P B

JFAUDIO1(13_14)
JUMPER 2P B

JCMOS1(1_2)
JUMPER 2P B

JDDR11_22V(1_2)
JUMPER 2P R

(BAT1)



3V BATTERY SONY

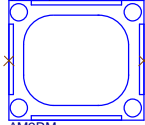
(ROM1)



FLASH ROM

PLCC 4M LPC

(CPU1)



AM2RM

(U5)



SBNP SMALL P


(U10)



SBNP SMALL


New JPANEL1
JPANEL1 2*11

JPANEL1(9_10) JPANEL1(15_16)
HEADER 1X2 HEADER 1X2
JPANEL1(11_14)
PLED



JPANEL1(1_4) JPANEL1(5_6) JPANEL1(7_8)
SPK HLED RST

PCB



CRU51-M2 1.3

(PCB)



POLON 245x220

Title		
<Title>		
Size	Document Number	Rev
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