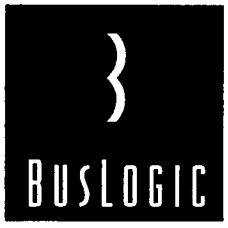
Technical Reference Manual



BA-81C15 High Performance PCI to SCSI Host Adapter Chip

P/N 3001013, Rev. B

Revision History

Revision	Change Activity	Date
A	Release	1/31/96
B	Changes reflect BA-81C15 Rev. F and above	3/22/96

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Functional Definition

About This Chapter

Read this chapter to find out

- Features of the BA-81C15 PCI host adapter chip
- A general overview of the BA-81C15 to SCSI host adapter chip

1

Functional Definition

Key Features

- 10 MB/sec FAST SCSI synchronous 8-bit data transfers
- 20 MB/sec FAST20 SCSI synchronous 8-bit data transfers
- 20 MB/sec FAST/WIDE SCSI synchronous 16-bit data transfers
- 40 MB/sec FAST20/WIDE SCSI synchronous 16-bit data transfers
- 14 MB/sec SCSI asynchronous 16-bit data transfers
- 132 MB/sec PCI host bus transfers
- 32-byte SCSI FIFO
- 128-byte host FIFO
- 128-byte program RAM for SCSI automation
- 128-byte host automation RAM
- Intelligent initiator control reduces host processor overhead
- Connects to up to fifteen SCSI peripherals in wide mode
- Differential SCSI support
- Support for SCAM Level 2
- Support for PCI Sub-System ID
- Low power CMOS technology

Overview

The BA-81C15 chip is an integrated PCI to SCSI host adapter chip. The BA-81C15 has been designed to perform 20 MB/sec Fast20 SCSI data transfers in 8-bit mode or 40 MB/sec Fast/Wide SCSI data transfers in 16-bit mode with an UltraSCSI bus. Using its low-level operating mode and automation commands, the BA-81C15 is able to handle normal SCSI protocol with a minimum of processor intervention. The low-level operations quickly hand operations directly to the SCSI bus under the control of the host processor. The user can also program commands or instructions to the automation RAM, which enables the BA-81C15 SCSI to handle the SCSI protocol. The program automation RAM can control most initiator operations.

Host automation can handle up to sixteen commands, which include address and count for a Scatter/Gather list. This RAM, which is 32x32 bits, could be shared with the onboard BIOS[1]. On the host bus, burst transfers can be handled at up to the maximum PCI transfer rate. The host FIFO will operate in 8-, 16- or 32-bit modes to or from the host side and in 8- or 16-bit modes to or from the SCSI side.

[1] There is a 32x8 stack that the BIOS can use without having to share the Scatter/Gather RAM.

Initiator/Disconnected Modes

When the BA-81C15 completes an "arbitrate and select a target" or if it successfully responds to "re-selection as an initiator," it automatically puts itself into Initiator mode. These operations are enabled by means of a bit in SCSI Control 0 Register 45h, R/W. When the BA-81C15 is not in Initiator mode, it is said to be in Disconnected mode (even if the SCSI bus is not in Bus-Free phase; another connection involving the BA-81C15 may be ongoing). The Initiator Mode Bit (R/W) is available in Reset Register 47h Bit 7, R/W.

Arbitration, Selection, and Re-Selection Control

The BA-81C15 can automatically perform all of the functions to arbitrate, select, or be re-selected. When the BA-81C15 is enabled to perform the Select Target operation (by those bits in SCSI Control 0 Register 45h), it will wait for bus free, then arbitrate for the SCSI bus (using the ID specified in the Arbitration ID Register 52h [3:0]). If the BA-81C15 wins arbitration, it will then select the appropriate Target (specified in the SCSI Select ID Register 53h [3:0]).

In addition, if the SCSI Interface Control Register 45h Bit 2 is set, the BA-81C15 will respond to re-selection by another device on the SCSI bus. The successful completion of this operation will cause the ReSel Comp Bit (Interrupt Status Register 42h Bit 3) to be set, which can result in the external interrupt signal asserting (if that particular interrupt source is enabled). The SCSI ID of the device re-selecting the BA-81C15 will be stored into the Selected ID (Reg 53h [7:4]). The BA-81C15's current SCSI ID will be stored in Current ID (Reg 52h [7:4]). This is useful if multiple bits are set in the Wait for Self ID Registers (Reg 50h, 51h [7:0]).

SCSI Bus Phase Changes and Data Transfer

An Information phase is defined by the state of the C/D, MSG, and I/O signals (the "SCSI bus phase control signals set by the target") only if the REQ signal is asserted. SCSI has several bus phases to handle the different types of information transfers between the Initiator and the Target.

While in Initiator mode, the BA-81C15 will not automatically assert the ACK signal to handshake or transfer data on the SCSI bus if a "phase-mismatch" occurs. A phase-mismatch is defined as the assertion of REQ (by the Target) when the SCSI bus phase control signals (also driven by the Target) do not match the corresponding values in SCSI Signal Register 44h [2:0]. If a phase-mismatch occurs, a SCSI Phase Change Status and Interrupt (if enabled) is generated to the host CPU, and the low-level driver must take appropriate action. Once enabled, the BA-81C15 will continue to transfer data (and keep generating ACK pulses) until a new phase-mismatch occurs or the SCSI bus reset occurs. Data will continue to transfer even if the SCSI block transfer counter is zero; therefore the transfer counter is used to keep track of large blocks of data when the BA-81C15 is in Initiator mode and not to control the operation. In Initiator mode, the transfer counter is decremented on reads from the FIFO so that the transfer counter can be loaded after the SCSI transfer has started on reads; therefore, on writes, the transfer counter will reflect the amount of data the Target has accepted. The data transfer is controlled by the Bus-Master transfer counter.

Synchronous Transfer Support

Per SCSI specification, the only SCSI bus phases that can utilize synchronous transfers are the two data phases (Data In and Data Out). The BA-81C15 automatically detects when the current bus phase is equal to the Data In phase and receives synchronous data without the need to match the SCSI phase. The BA-81C15 also automatically enables the SCSI FIFO port. The Data Out phase is started by matching the phase. The target REQ(s) are stored by the offset counter prior to the phase being matched so that the offset is preserved.

Most of the time the synchronous control logic is automatically set up at the time the Initiator is connected to the SCSI Target. The Selected ID is stored at the time of selection or re-selection. The Selected ID is used to point to one of sixteen Target Registers. The Target Registers store the sync rate, the SCSI bus width, and the maximum sync offset. These are assigned by the driver during sync negotiation. In this way the SCSI Sync Registers are addressed by the Selected ID, which is loaded every time a selection or re-selection occurs.

Whenever the BA-81C15 is transferring data in a non-data information transfer phase, it uses async transfer mode, *regardless of the values in the SCSI Synchronous Control Register.*

32-Byte SCSI FIFO

The BA-81C15 has two 16x9 bit FIFOs which can be configured for either 8-bit or 16-bit mode, depending on the width of the SCSI device. Two channels can simultaneously access the FIFO: a read channel and a write channel. The SCSI FIFO is used mostly for data, but other information can go through it. It has a dual port memory, separate read and write address counters, and a synchronous up-down counter which keeps track of the status of the SCSI FIFOs.

Timeout

The BA-81C15 provides a "load and forget" timeout interrupt-generation mechanism. This mechanism is built around a 20-bit counter clocked at approximately 2.5 MHz, depending on the OCS frequency and the value in SCSI CNTL (Register 6Dh [2:0]). There is an 8-bit Compare (Timeout Value Register 6Ch [7:0]) and a general purpose "START_TIMEOUT" bit (Port Control Register 46h Bit 0). The timeout is used automatically during selection. The magnitude of the timeout can be adjusted using Reg 4Eh Bit 7. This bit allows the use of much shorter timeout conditions, such as those required by SCAM. Manual use of the timer is covered in Chapter 6, Register Definition.

SCSI Three-State Drivers

The BA-81C15's SCSI buffers are programmable to be either open collector (open drain) or three-state. The open collector buffers are the standard 48mA drivers. (Note that SCSI-3 will require active terminations.)

Note: For applications needing higher speeds, there is the option to add active deassertion (see bit "ENABLE Active Deassertion" in SCSI CLK Control, 65h, Bit 4). The BA-81C15 is equipped with an active pull-up consisting of an N-channel transistor to Vdd. This weak N-channel device will not cause a problem with the operation of the SCSI bus when the BA-81C15 is powered down. The weak N-channel will not overdrive the standard or active terminators, causing term power problems. The weak N-channel will allow the SCSI device to be hot-plugged as long as the bus is quiescent.

Parity Logic

The BA-81C15 can generate or check parity. In addition, there is an option to invert parity information on *data being written to the FIFO* (from any source). There is one bit of parity per byte of data. Parity errors can optionally generate interrupts.

Automation Logic

The automation logic is used to reduce the number of interrupts. There is an automation instruction RAM (64x 6 bits) which can be programmed to hold normal messages, commands, check the SCSI phases, and control signals automatically responding to the Target. The method used is first to decide on the sequence needed. Program the automation RAM, enable the automation logic (using the desired start condition in Regs 64–67h, R/W), and then enable the Select Target (Reg 45h Bit 6, R/W) usually with ATN (Reg 45h Bit 4, R/W). After the BA-81C15 has gained access to the target and once the starting condition is met, the automation logic will begin executing instructions. These instructions include waiting for a particular phase, transferring a message or status byte into one of the general purpose registers (Regs 68h-6Bh), generating interrupts and the like.

The automation logic will halt once it encounters a Stop and Set Interrupt command (SSI) (Reg 43h [0:4]) or when a phase is encountered that has not been anticipated (Reg 42h Bit 6). The automation program counter will contain the offset into the automation RAM where the automation stopped execution. The automation RAM will be loaded at initialization time with a generic script or map and then can be modified for each specific command. This allows about 85 percent of the map to remain constant and only requires such commands as the CDB or the identify message to be loaded for each operation.

Multiple starting conditions can be enabled simultaneously, but only one of these can start the automation at a time. Once one condition does start the automation, the other starting condition will remain active and will restart the automation once it has stopped and the condition is met.

Automation is covered in detail in Chapter 7.

DMA Interface

The DMA interface transfers 8 -bit data internal to the BA-81C15 between the PCI block and the SCSI block. In the DMA mode the SCSI block asserts the DMA_REQ signal and the PCI block receives it. The SCSI block expects to send/receive data when the DMA_ACK signal is asserted by the PCI block.

BIOS PROM Interface

The BA-81C15 requires a BIOS PROM to aid the operating system in configuring and using the I/O card. The code contained within the BIOS PROM is executed by the operating system to initialize the BA-81C15 and the I/O card, and to inform the operating system of the I/O card's presence. It may also provide the interface routines which communicate between an I/O driver and the I/O card (BA-81C15). It should be noted that when the BIOS PROM interface is 8 data bits wide, any code run directly from this PROM will execute slowly. The BIOS is read 4 bytes at a time and then given to the PCI interface in 32-bit format. For higher performance systems, the BIOS code should be copied into and executed from system RAM.

The method used to address the BIOS PROM is a 14-bit memory address bus and an 8-bit data bus, plus a ROM chip select. There is an Address Bit 15 provided under driver control to allow 64K ROM space.

Automated Scatter/Gather Handling

The BA-81C15 provides the ability to handle up to sixteen Scatter/Gather 8-byte segments at one time. This is accomplished by using the 128 bytes of Scatter/Gather RAM (SGRAM). The SGRAM is broken up into sixteen 8-byte chunks or segments and are numbered 0–15. Each segment is written into the SGRAM using 32-bit accesses. Once this SGRAM has been initialized, the starting and ending segment numbers, or pointers, are written into Reg 28h. This register tells the BA-81C15 where to start and end processing of the Scatter/Gather segments. Finally, Bit 0 of Reg 29h is enabled and the Scatter/Gather operation commences. The first 8-byte packet is copied into Scatter/Gather Instruction registers (Transfer Command Register 1Bh, Count Register 1Ah~18h, and Host Address 1Fh~1Ch), which start the transfer of the first Scatter/Gather elements data. The BA-81C15 allows the flexibility of selectively generating interrupts at the completion of each Scatter/Gather element by setting Bit 7 of the Transfer Command Register 1Bh. This way, the interrupt can be inhibited on all Scatter/Gather elements, except for the last, when the entire list has been processed.

SEEPROM Download at Power On Reset

The BA-81C15 supports PCI Configuration at power on reset by downloading values from the SEEPROM. The following table shows a description of the register, the PCI register address, and the SEEPROM address for each of the values which are loaded:

Table 1-1. Format of the SEEPROM Space

Description	PCI Configuration Register	SEEPROM Address
Sub-sys Vendor ID:	Reg. 0x2C-2D	Word Address 0x28
Sub-sys Device ID:	Reg. 0x2E-2F	Word Address 0x29
Configuration Key:	N/A	Word Address 0x2A (value = 0x424C)
Interrupt Pin: BIOS Size	Reg.0x3D bits (2-0) If bit 7- is cleared 32KB BIOS is used or if bit 7- is set then 64KB BIOS is used at POR.	Word Address 0x2B (low byte)
Available: bits 15-8		Word Address 0x2B (hi byte)
Min Grant	Reg. 0x3E	Word Address 0x2C (low byte)
Max Latency	Reg. 0x3F	Word Address 0x2C (hi byte)
Card Bus CIS Pointer:	Reg. 0x28-29	Word Address 0x2D
Card Bus CIS Pointer:	Reg. 0x2A-2B	Word Address 0x2E

The Sub-system ID will always be loaded into the appropriate registers at power-up. In addition, if the Configuration Key contains the proper value ("BL"), then the remaining registers will be loaded with the values stored in the SEEPROM. The Configuration Key has been added to prevent accidental loading of critical registers in the event a part is installed on a board containing a SEEPROM with old data. If the Configuration Key does not match, then the power on reset values inside the chip would be used.

The BIOS Size Register is one bit (bit 7), of Word Address 0x2B. FlashPoint currently requests a 32K ROM space and in the future, we may need to request 64K. If the byte in the SEEPROM contains 0x00, then ROM address bit 15 is writable and PCI Configuration will assign 32K. If the SEEPROM contains 0x8X, then bit 15 of the ROM address is not writable and PCI Configuration will assign 64K. The values of the SEEPROM register will not affect bit 2 of the Feature Ctrl (Reg. 0x29) BIOS SHADOW (0 = 32K, 1 = 64K), but in the case of 64K it will have no effect.

The Minimum Grant and Maximum Latency, Registers 3Eh, and 3Fh are both preset with 08h and can be downloaded with values from the SEEPROM. The values do not affect any logic in the BA-81C15 and they are used by the system in optimizing the PCI performance for the BA-81C15.

The Card Bus CIS Pointer, Register 28h-2Bh are preset to 00h and if the Configuration Key is correct, they are donwloaded from the SEEPROM. The Card Bus CIS Pointer is part of Card Information Structure. Refer to the PCMCIA v2.10 specification for details. It can be used to communicate an address to the BIOS or Software Driver as to the address of any code or parameter lists during initialization.

2

Pin Definitions

About This Chapter

Read this chapter to find out

- A summary of the pin pad type and signal assignment
- Pin layout of the BA-81C15

2

Pin Definitions

BA-81C15 pins are described here in tables listing the name (or symbol), number, type, and funtion. In these tables, the following abbreviations are used:

I/O	-	Input and output pin
I	-	Input pin only
O	-	Output pin only; push-pull driver
TS	-	Three-state output pin
OC	-	Open collector output pin

In addition, a diagram of the BA-81C15 pin layout is presented in Figure 2-1.

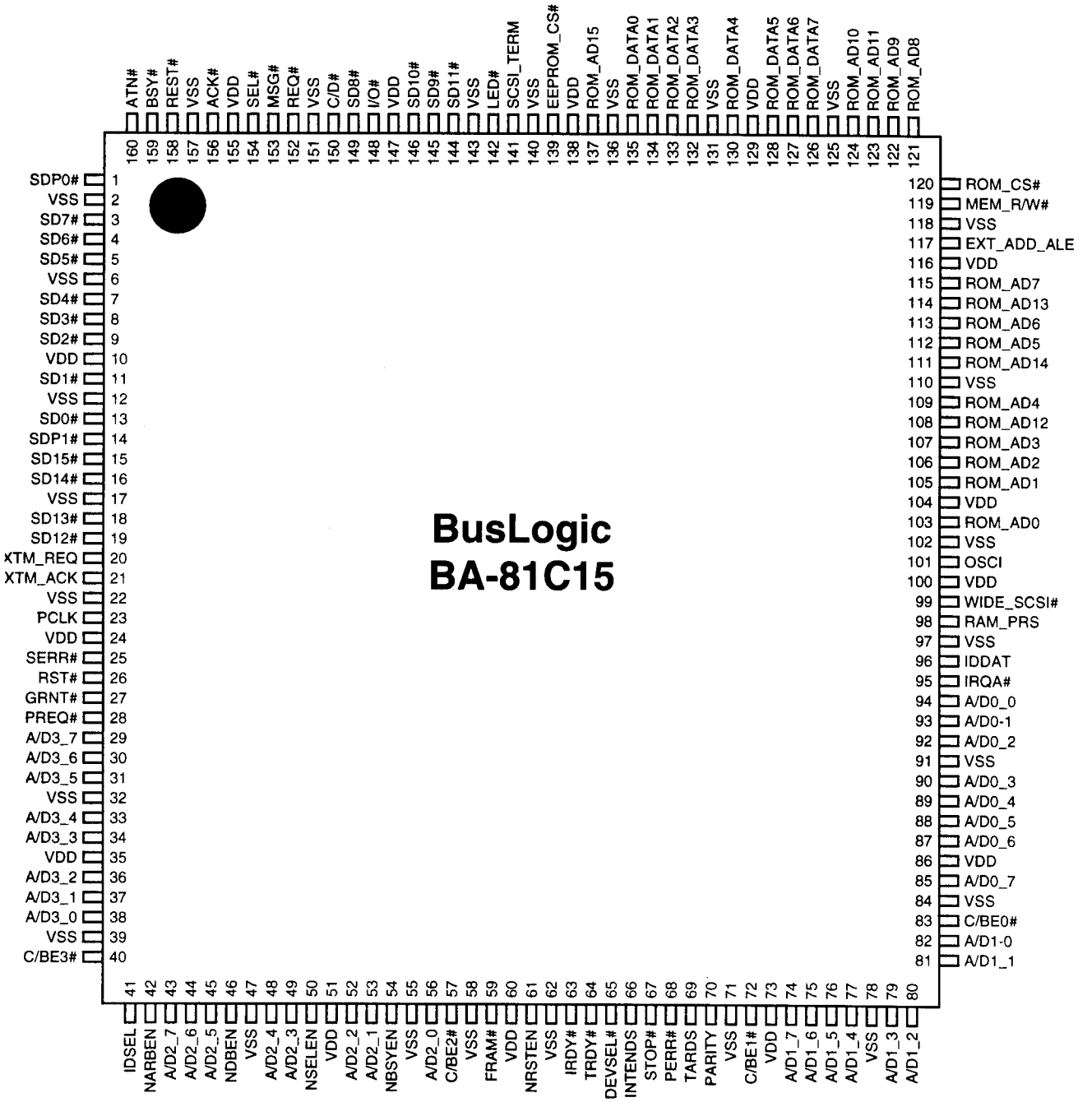


Figure 2-1. BA-81C15 Pin Layout

PCI Interface Pins

Table 2-1. PCI Interface Pins

Symbol	*Pin Number*	*I/O*	*Function*
PCLK	23	I	**PCI CLK:** Used to drive host logic.
IDSEL	41	I	**Initialization Device Select:** Used as a chip select during configuration read and write transactions.
GRNT#	27	I	**GRANT#:** GRNT as designated in the PCI Specification. This active low input from the PCI arbitration logic indicates that the master is granted the bus.
PREQ#	28	O	**PCI Request:** PREQ# indicates to the arbiter that this device desires use of the bus.
DEVSEL#	65	I/O	**PCI Device Select:** DEVSEL# is used as a chip select during configuration read and write transactions.
FRAME#	59	I/O	**PCI Frame:** FRAME# starts the PCI bus cycle.
STOP#	67	I/O	**PCI Stop:** STOP# stops the PCI bus cycle.
IRDY#	63	I/O	**Initiator Ready#:** IRDY# signal as designated in the PCI Specification.
TRDY#	64	I/O	**Target Ready#:** TRDY# signal as designated in the PCI Specification.
PAR	70	I/O	**Parity Error*: PERR*** signal as designated in the PCI Specification.
PERR#	68	I/O	**Parity Error#: PERR#** signal as designated in the PCI Specification.
SERR#	25	I/O	**System Error#: SERR#** signal as designated in the PCI Specification.
IRQA# (16mA)	95	TS	**Interrupt A#: IRAQ#** signal as designated in the PCI Specification.
A/D3 [7:0] (20 mA)	29-31, 33,34, 36-38	I/O	**Host Address/Data Byte 3 [7:0]:** Bidirectional active high host multiplexed address and data bus.
A/D2 [7:0] (24mA)	43-45, 48,49, 52-53, 56	I/O	**Host Address/Data Byte 2 [7:0]:** Bidirectional active high host multiplexed address and data bus.
A/D1 [7:0] (24mA)	74-77, 79-82	I/O	**Host Address/Data Byte 1 [7:0]:** Bidirectional active high host multiplexed address and data bus.
A/D0 [7:0] (24mA)	85, 87-90, 92-94	I/O	**Host Address/Data Byte 0 [7:0]:** Bidirectional active high host multiplexed address and data bus.
C/BE [3:0] (24mA)	40,57, 72,83	I/O	**Command/Byte Enables [3:0]:** These determine the data paths that will be used by the current cycle of the PCI bus.
RST#	26	I	**Reset#:** This active *low* input signal resets the BA-81C15. It puts the BA-81C15 into a power reset condition with all controllers and registers in the reset condition. The condition of resisters after reset is found in Chapter 5, Register Summary. This signal must be asserted for a minimum of two clocks after the Vdd pins have reached Vdd-min.

External Memory Interface Pins

Table 2-2. External Memory Interface Pins

Symbol	*Pin Number*	*I/O*	*Function*
ROM_AD [15:0]	137, 111, 114, 108, 123, 124, 122, 121, 115, 113, 112, 109, 107, 106 105, 103	I/O	**ROM Address [15:0]:** BIOS and external RAM address for BA-81C15 board product. BIOS is assumed to be fixed 32K x 8 EPROM or Flash. BIOS Shadow Bit (Reg 29h Bit 2) is used to address 64K x 8 memories.
ROM_DATA [7:0]	126-128, 130, 132-135	I/O	**ROM Data [7:0]:** BIOS and external RAM data for BA-81C15 board product.
ROM_CS#	120	TS	**ROM Chip Select:** Chip Select for the BIOS ROM.
MEM_R/W#	119	TS	**Memory Read/Write#:** Signal which determines whether the memory is read or written. Active high for Reads and active low for Writes.
WIDE#	99	I	**Wide SCSI Bus:** Used as strapping pin for narrow/wide SCSI applications.
RAM_PRS	98	I	**RAM_PRS:** User Defined Input, connected to Feature Control Register, 29h, bit 5.
IDDAT	96	I/O	**ID of the Board:** This value is used for Plug and Play and is shifted in at power on reset from external logic.
TARDS	69	O	**TARDS:** Used as SCSI differential control signal indicating Target mode.
INTENDS	66	O	**INTENDS:** Used as SCSI differential control signal indicating Initiator mode.
NRSTEN	61	O	**NRSTEN:** Used as SCSI differential control signal indicating NRST is asserted.
NBSYEN	54	O	**NBSYEN:** Used as SCSI differential control signal indicating NBSY is asserted
NSELEN	50	O	**NSELEN:** Used as SCSI differential control signal indicating NSEL is asserted.
NDBEN	46	O	**NDBEN:** Used as SCSI differential control signal indicating output data to bus.
NARBEN	42	O	**NARBEN:** Used as SCSI differential control signal indicating arbitrate in process.
SCSI_TERM	141	TS	**SCSI Termination:** Signal which can be used to enable the SCSI Termination under program control.
EEPROM_CS	139	TS	**EEPROM Chip Select:** Chip Select to control the EEPROM. The other pins necessary are multiplexed with the EPROM and RAM.
LED#	142	OC	**LED:** LED is used to drive the LED connector, sending Device Select information to the front panel. The LED will be active when the SCSI Busy signal is active.
#EXTM_ACK	21	I	**External Memory Acknowledge:** This signal is a general purpose input (Reg 22h Bit 7).
#EXTM_REQ	20	TS	**External Memory Request:** This signal is a general purpose output (Reg 22h Bit 6).

SCSI Interface Pins

Table 2-3. SCSI Interface Pins

Symbol	*Pin Number*	*I/O*	*Function*
BSY# (48mA)	159	I/O OC	**Busy#:** The SCSI Busy signal. Indicates that the SCSI bus is in use, and is also used to gain control of the bus. This signal does not have a programmable active internal pull-up. The input is Schmitt triggers input with nominal hysteresis of 400mV.
SEL# (48mA)	154	I/O OC	**Select#:** The SCSI Select Device signal. Driven by the Initiator to select a Target and driven by a Target to Re-Select an Initiator. This signal does not have a programmable active internal pull-up. The input is Schmitt triggers input with nominal hysteresis of 400mV.
RSET# (48mA)	158	I/O OC	**Reset#:** The SCSI Bus Device Reset signal. This can be driven by any device to clear all devices from the bus. This signal does not have a programmable active internal pull-up. The input is Schmitt triggers input with nominal hysteresis of 400mV.
ATN# (48mA)	160	I/O OC TS	**Attention#:** Used by the Initiator to get the Target to respond and change the bus phase to Message Out. It has a 48mA N-channel pull-down and a programmable 4mA N-channel pull-up. The input is Schmitt triggers input with nominal hysteresis of 400mV.
MSG# (48mA)	153	I/O OC TS	**Message Phase#:** Driven by the Target to indicate the Bus phase (refer to the SCSI Bus Phase Table in the SCSI Block Description). It has a 48mA N-channel pull-down and a programmable 4mA N-channel pull-up. The input is Schmitt triggers input with nominal hysteresis of 400mV.
C/D# (48mA)	150	I/O OC TS	**Command/Data#:** Driven by the Target to indicate the Bus phase (refer to the SCSI Bus Phase Table in the SCSI Block Description). It has a 48mA N-channel pull-down and a programmable 4mA N-channel pull-up. The input is Schmitt triggers input with nominal hysteresis of 400mV.
I/O# (48mA)	148	I/O OC TS	**Input/Output#:** Driven by the Target to indicate the Bus phase (refer to the SCSI Bus Phase Table in the SCSI Block Description). It has a 48mA N-channel pull-down and a programmable 4mA N-channel pull-up. The input is Schmitt triggers input with nominal hysteresis of 400mV.
REQ# (48mA)	152	I/O OC TS	**Request#:** Driven by the Target to transfer data to or request data from the Initiator. It has a 48mA N-channel pull-down and a programmable 4mA N-channel pull-up. The input is Schmitt triggers input with nominal hysteresis of 400mV.
ACK# (48mA)	156	I/O OC TS	**Acknowledge#:** Driven by the Initiator to acknowledge the receipt of data or to signal the Initiator that the requested data is available. It has a 48mA N-channel pull-down and a programmable 4mA N-channel pull-up. The input is Schmitt triggers input with nominal hysteresis of 400mV.
SD[15:8]# (48mA)	15,16, 18,19, 144-146, 149	I/O OC TS	**SCSI Data [15:8]#:** These bidirectional active low signals are the SCSI Data signals. They have 48mA N-channel pull-downs and a programmable 4mA N-channel pull-up. The inputs are Schmitt triggers inputs with nominal hysteresis of 400mV. Logically they function the same in both single-ended and differential modes. Note: Must be deasserted when not in use.
SD[7:0]# (48mA)	3-5, 7-9, 11, 13	I/O OC TS	**SCSI Data [7:0]#:** These bidirectional active low signals are the SCSI Data signals. They have 48mA N-channel pull-downs and a programmable 4mA N-channel pull-up. The inputs are Schmitt triggers inputs with nominal hysteresis of 400mV. Logically they function the same in both single-ended and differential modes.
SDP1# (48mA)	14	I/O OC TS	**SCSI Parity 1#:** Odd parity for SCSI Data 15-8. Same buffer as the data.
SDP0# (48mA)	1	I/O OC TS	**SCSI Parity 0#:** Odd parity for SCSI Data 7-0. Same buffer as the data.

Miscellaneous Pins

Table 2-4. Miscellaneous Pins

Symbol	*Pin Number*	*I/O*	*Function*
OSCI	101	I	**Oscillator In:** This free-running or gated clock signal is used to generate timing and synchronize transfers with the BA-81C15. It also is used for internal chip timing and is divided to produce external timing for the SCSI bus.
EXT_ADD_ALE	117	O	**External Address ALE:** Active high signal to latch the ROM Data Signals through I/O or Memory Register 27h.

Power/Ground Pins

Table 2-5. Power/Ground Pins

Symbol	*Pin Number*	*Function*
VDD	10, 24, 35, 51, 60, 73, 86, 101, 104, 116, 129, 138, 147, 155	+5 Volt Power Pins (14 pins)
VSS	2, 6, 12, 17, 22, 32, 39, 47, 55, 58, 62, 71, 78, 84, 91, 97, 102, 110, 118, 125, 131, 136, 140, 143, 151, 157,	VSS—Ground Pins (26 pins)

3

Address Space

About This Chapter

Read this chapter to find out

- A summary of the address space for BA-81C15 I/O space

3

Address Space

The following is a summary of the address space for BA-81C15 I/O space.

00–3F	BUS MASTER REGISTER FILE
40–77	SCSI REGISTER FILE
80–FF	SCATTER/GATHER INSTRUCTION RAM ADDRESSABLE AS DOUBLE WORDS ONLY
80–FF	SHADOWED SCSI AUTOMATION RAM ADDRESSABLE AS BYTES OR WORD ONLY

Note: *Shadowed area is only addressable if the shadow bit is set in the Feature Control Register 29h Bit 1.*

4

Register Reset Condition Description

About This Chapter

Read this chapter to find out

- PCI Configuration Space Register reset conditions
- Host Register File reset conditions
- Block Register reset conditions

4

Register Reset Condition Description

PCI Configuration Space Register Reset Condition

REGISTER NUMBER	POWER ON RESET	CHIP RESET	DRIVER RESET	REGISTER VALUE 7 6 5 4 3 2 1 0
00				0 1 0 0 1 0 1 1
01				0 0 0 1 0 0 0 0
02				0 0 1 1 0 0 0 0
03				1 0 0 0 0 0 0 1
04	*	*		1 0 0 0 0 0 0 0
05	*	*		0 0 0 0 0 0 0 0
06	*	*		0 0 0 0 0 0 0 0
07	*	*		0 0 0 0 0 0 0 0
08	*	*		0 0 0 0 0 0 1 0
09	*	*		0 0 0 0 0 0 0 0
0A	*	*		0 0 0 0 0 0 0 0
0B	*	*		0 0 0 0 0 0 0 1
0C	*	*		0 0 0 0 0 0 0 0
0D	*	*		0 0 0 0 0 0 0 0
0E	*	*		0 0 0 0 0 0 0 0
0F	*	*		0 0 0 0 0 0 0 0
10	*	*		0 0 0 0 0 0 0 1
11	*	*		0 0 0 0 0 0 0 0
12	*	*		0 0 0 0 0 0 0 0
13	*	*		0 0 0 0 0 0 0 0
14	*	*		0 0 0 0 0 0 0 0
15	*	*		0 0 0 0 0 0 0 0
16	*	*		0 0 0 0 0 0 0 0
17	*	*	*	0 0 0 0 0 0 0 0
18	*	*		0 0 0 0 0 0 0 0
19	*	*		0 0 0 0 0 0 0 0
1A	*	*		0 0 0 0 0 0 0 0
1B	*	*	*	0 0 0 0 0 0 0 0

REGISTER NUMBER	POWER ON RESET	CHIP RESET	DRIVER RESET	REGISTER VALUE 7 6 5 4 3 2 1 0
1C				0 0 0 0 0 0 0 0
1D				0 0 0 0 0 0 0 0
1E				0 0 0 0 0 0 0 0
1F				0 0 0 0 0 0 0 0
20				0 0 0 0 0 0 0 0
21	*	*		0 0 0 0 0 0 0 0
22	*	*		0 0 0 0 0 0 0 0
23	*	*		0 0 0 0 0 0 0 0
24	*	*		0 0 0 0 0 0 0 0
25	*	*		0 0 0 0 0 0 0 0
26	*	*		0 0 0 0 0 0 0 0
27	*	*		0 0 0 0 0 0 0 0
28	*	*		0 0 0 0 0 0 0 0
29	*	*		0 0 0 0 0 0 0 0
2A	*	*		0 0 0 0 0 0 0 0
2B				0 0 0 0 0 0 0 0
2C	*	*		0 0 0 0 0 0 0 0
2D	*	*	*	0 0 0 0 0 0 0 0
2E	*	*		0 0 0 0 0 0 0 0
2F	*	*		0 0 0 0 0 0 0 0
30	*	*		0 0 0 0 0 0 0 0
31	*	*		0 0 0 0 0 0 0 0
32	*	*		0 0 0 0 0 0 0 0
33				0 0 0 0 0 0 0 0
34				0 0 0 0 0 0 0 0
35				0 0 0 0 0 0 0 0
36				0 0 0 0 0 0 0 0
37				0 0 0 0 0 0 0 0
38	*	*		0 0 0 0 0 0 0 0
39	*	*		0 0 0 0 0 0 0 0
3A	*	*		0 0 0 0 0 0 0 0
3B	*	*		0 0 0 0 0 0 0 0
3C	*	*		0 0 0 0 0 0 0 0
3D	*	*		0 0 0 0 0 0 0 1
3E	*	*		0 0 0 0 1 0 0 0
3F	*	*		0 0 0 0 1 0 0 0

Host Register File Reset Condition

REGISTER NUMBER	POWER ON RESET	CHIP RESET	DRIVER RESET	REGISTER VALUE 7 6 5 4 3 2 1 0
00				0 1 0 0 1 0 1 1
01				0 0 0 1 0 0 0 0
02				0 0 1 1 0 0 0 0
03				1 0 0 0 0 0 0 1
04	*	*		0 0 0 0 0 0 0 0
05	*	*		0 0 0 0 0 0 0 0
06	*	*		0 0 0 0 0 0 0 0
07	*	*		0 0 0 0 0 0 0 0
08	*	*		0 0 0 0 0 0 0 0
09	*	*		0 0 0 0 0 0 0 0
0A	*	*		0 0 0 0 0 0 0 0
0B	*	*		0 0 0 0 0 0 0 0
0C	*	*		0 0 0 0 0 0 0 0
0D	*	*		0 0 0 0 0 0 0 0
0E	*	*		0 0 0 0 0 0 0 0
0F	*	*		0 0 0 0 0 0 0 0
10	*	*		0 0 0 0 0 0 0 0
11	*	*		0 0 1 0 0 0 0 0
12	*	*		0 0 0 0 0 0 0 0
13	*	*		0 0 0 0 0 0 0 0
14	*	*		0 0 0 0 0 0 0 0
15	*	*		0 0 0 0 0 0 0 0
16	*	*		0 0 0 0 0 0 0 0
17	*	*	*	0 0 0 0 0 0 0 0
18	*	*		0 0 0 0 0 0 0 0
19	*	*		0 0 0 0 0 0 0 0
1A	*	*		0 0 0 0 0 0 0 0
1B	*	*	*	0 0 0 0 0 0 0 0
1C				x x x x x x x x
1D				x x x x x x x x
1E				x x x x x x x x
1F				x x x x x x x x
20				x x x x x x x x
21	*	*		0 0 0 0 0 0 0 0
22	*	*		x 0 0 0 0 0 0 x
23	*	*		0 0 0 0 0 0 0 0
24	*	*		0 0 0 0 0 0 0 0

REGISTER NUMBER	POWER ON RESET	CHIP RESET	DRIVER RESET	REGISTER VALUE 7 6 5 4 3 2 1 0
25	*	*		00000000
26	*	*		000000xx
27	*	*		00000000
28	*	*		00000000
29	*	*		000x0000
2A	*	*		00000000
2B				10000000
2C	*	*		00000000
2D	*	*	*	00000000
2E	*	*		00000000
2F	*	*		0000000x
30	*	*		00000000
31	*	*		xxx00000
32	*	*		00000000
33				00001110
34				xxxxxxxx
35				xxxxxxxx
36				00001000
37				00000010
38	*	*		00000000
39	*	*		00000000
3A	*	*		00000000
3B	*	*		00000000
3C	*	*		00000000
3D	*	*		00000000
3E	*	*		00000000
3F	*	*		00000000

SCSI Block Register Reset Condition

REGISTER NUMBER	POWER ON RESET	RESET DMA BK	RESET SCSI BK	RESET PROG BK	CLEAR FIFO	CHIP RESET	DRIVER RESET	REGISTER VALUE 7 6 5 4 3 2 1 0
40	*					*	*	0 0 0 0 0 0 0 0
41	*	*	*	*	*	*	*	0 0 0 0 0 0 0 0
42	*	*	*	*	*	*	*	0 0 0 1 0 0 0 0
43								1 0 0 0 0 0 0 0
44	*	*	*	*	*	*	*	1 1 0 0 0 0 0 0
45	*	*	*	*	*	*	*	0 0 0 0 0 0 0 0
46	*	*	*	*	*	*	*	0 0 0 0 0 0 0 0
47					*			0 0 0 0 1 1 1 0
48	*	*	*	*	*	*	*	0 0 0 0 0 0 0 0
49	*	*	*	*	*	*	*	0 0 0 0 0 0 0 0
4A	*	*	*	*	*	*	*	0 0 0 0 0 0 0 0
4B								x x 0 0 0 0 0 0
4C								x x x x x x x x
4D								x x x x x x x x
4E	*					*	*	0 0 0 0 0 0 0 0
4F	*	*	*	*		*	*	0 0 0 0 0 0 0 0
50								x x x x x x x x
51								x x x x x x x x
52								0 0 0 0 x x x x
53	*	*	*	*	*	*	*	0 0 0 0 0 0 0 0
54								x x x x x x x x
55								x x x x x x x x
56								x x x x x x x x
57								x x x x x x x x
58								x x x x x x x x
59								x x x x x x x x
5A								x x x x x x x x
5B								x x x x x x x x
5C								x x x x x x x x
5D								x x x x x x x x
5E								x x x x x x x x
5F								x x x x x x x x
60								x x x x x x x x
61								x x x x x x x x
62								x x x x x x x x

REGISTER NUMBER	POWER ON RESET	RESET DMA BK	RESET SCSI BK	RESET PROG BK	CLEAR FIFO	CHIP RESET	DRIVER RESET	REGISTER VALUE 7 6 5 4 3 2 1 0
63								xxxxxxxx
64								00011111
65								00011111
66								00011111
67								00011111
68	*	*	*	*	*	*	*	00000000
69	*	*	*	*	*	*	*	00000000
6A	*	*	*	*	*	*	*	00000000
6B	*	*	*	*	*	*	*	00000000
6C								10011001
6D	*	*	*	*	*	*	*	00000000
6E	*	*	*	*	*	*	*	00000000
6F	*	*	*	*	*	*	*	00000000
70								00000000
71								01000000
72	*	*	*	*	*	*	*	00000000
73	*	*	*	*	*	*	*	00000000
74	*	*	*	*	*	*	*	00000000
75	*	*	*	*	*	*	*	00000000
76	*	*	*	*	*	*	*	00000000
77	*	*	*	*	*	*	*	00000000

5

Register Summary

About This Chapter

Read this chapter to find out

- A summary of each register in the BA-81C15

5

Register Summary

This chapter summarizes each BA-81C15 register in tabular form. Covered registers include those used for PCI Configuration Space, Host Register File, and SCSI File Registers.

PCI Configuration Space

03h Device ID 1 R ADD 00/BE 3	02h Device ID 0 R ADD 00/BE 2	01h Vendor ID 1 R ADD 00/BE 1	00h Vendor ID 0 R ADD 00/BE 0
7 Dev ID 15	7 Dev ID 7	7 Vendor ID 15	7 Vendor ID 7
6 Dev ID 14	6 Dev ID 6	6 Vendor ID 14	6 Vendor ID 6
5 Dev ID 13	5 Dev ID 5	5 Vendor ID 13	5 Vendor ID 5
4 Dev ID 12	4 Dev ID 4	4 Vendor ID 12	4 Vendor ID 4
3 Dev ID 11	3 Dev ID 3	3 Vendor ID 11	3 Vendor ID 3
2 Dev ID 10	2 Dev ID 2	2 Vendor ID 10	2 Vendor ID 2
1 Dev ID 9	1 Dev ID 1	1 Vendor ID 9	1 Vendor ID 1
0 Dev ID 8	0 Dev ID 0	0 Vendor ID 8	0 Vendor ID 0

Dev ID [15:8] = Config Reg 03h = Option # = 1XXXXXX1h X loaded from external logic
Dev ID [7:0] = Config Reg 02h = PRODUCT # = 30h
PCI Vendor ID [15:0] = 10 4Bh

07h Status 1 R/W ADD 01/BE 3	06h Status 0 R/W ADD 01/BE 2	05h Command 1 R/W ADD 01/BE 1	04h Command 0 R/W ADD 01/BE 0
7 Detected Par Err	7 Reserved	7 Reserved	7 Wait Cyc Cntl
6 Signaled System Err	6 Reserved	6 Reserved	6 Par Err Response
5 Rec Master Abort	5 Reserved	5 Reserved	5 VGA PAL Snoop
4 Rec Target Abort	4 Reserved	4 Reserved	4 Memory W/I Enable
3 Sig Target Abort	3 Reserved	3 Reserved	3 Special Cycles
2 DEVSEL TM 1	2 Reserved	2 Reserved	2 Bus Master
1 DEVSEL TM 0	1 Reserved	1 Fast B to B Ena	1 Memory Space
0 Data Par Detected	0 Reserved	0 SERR# Enable	0 I/O Space

Sig Target Abort = 0
DEVSEL TM 1 = 0
DEVSEL TM 0 = 0

0Bh Class Code 2 R/W ADD 02/BE 3	0Ah Class Code 1 R/W ADD 02/BE 2	09h Class Code 0 R/W ADD 02/BE 1	08h Revision ID R/W ADD 02/BE 0
7 Base Class 7	7 Sub Class 7	7 Prog. Interface 7	7 Revision
6 Base Class 6	6 Sub Class 6	6 Prog. Interface 6	6 Revision
5 Base Class 5	5 Sub Class 5	5 Prog. Interface 5	5 Revision
4 Base Class 4	4 Sub Class 4	4 Prog. Interface 4	4 Revision
3 Base Class 3	3 Sub Class 3	3 Prog. Interface 3	3 Revision
2 Base Class 2	2 Sub Class 2	2 Prog. Interface 2	2 Revision
1 Base Class 1	1 Sub Class 1	1 Prog. Interface 1	1 Revision
0 Base Class 0	0 Sub Class 0	0 Prog. Interface 0	0 Revision

0Fh Reserved R ADD 02/BE 3	0Eh Reserved R ADD 02/BE 2	0Dh Latency Timer R/W ADD 02/BE 1	0Ch Cache Line Size R/W ADD 02/BE 0
7 Reserved	7 Reserved	7 Timer 5	7 Cache Line 7
6 Reserved	6 Reserved	6 Timer 4	6 Cache Line 6
5 Reserved	5 Reserved	5 Timer 5	5 Cache Line 5
4 Reserved	4 Reserved	4 Timer 4	4 Cache Line 4
3 Reserved	3 Reserved	3 Timer 3	3 Cache Line 3
2 Reserved	2 Reserved	2 Timer 2	2 Cache Line 2
1 Reserved	1 Reserved	1 GND	1 Cache Line 1
0 Reserved	0 Reserved	0 GND	0 Cache Line 0

13h Base Address 3 R/W ADD 10/BE 3	12h Base Address 2 R/W ADD 10/BE 2	11h Base Address 1 R/W ADD 10/BE 1	10h Base Address 0 R/W ADD 10/BE 0
7 Base Addr 31	7 Base Addr 23	7 Base Addr 15	7 Base Addr 7
6 Base Addr 30	6 Base Addr 22	6 Base Addr 14	6 Base Addr 6
5 Base Addr 29	5 Base Addr 21	5 Base Addr 13	5 Base Addr 5
4 Base Addr 28	4 Base Addr 20	4 Base Addr 12	4 Base Addr 4
3 Base Addr 27	3 Base Addr 19	3 Base Addr 11	3 Base Addr 3
2 Base Addr 26	2 Base Addr 18	2 Base Addr 10	2 Base Addr 2
1 Base Addr 25	1 Base Addr 17	1 Base Addr 9	1 Reserved
0 Base Addr 24	0 Base Addr 16	0 Base Addr 8	0 I/O Space Ind.

17h Base Address 3 R/W ADD 14/BE 3	16h Base Address 2 R/W ADD 14/BE 2	15h Base Address 1 R/W ADD 14/BE 1	14h Base Address 0 R/W ADD 14/BE 0
7 Base Addr 31	7 Base Addr 23	7 Base Addr 15	7 Base Addr 7
6 Base Addr 30	6 Base Addr 22	6 Base Addr 14	6 Base Addr 6
5 Base Addr 29	5 Base Addr 21	5 Base Addr 13	5 Base Addr 5
4 Base Addr 28	4 Base Addr 20	4 Base Addr 12	4 Base Addr 4
3 Base Addr 27	3 Base Addr 19	3 Base Addr 11	3 Base Addr 3
2 Base Addr 26	2 Base Addr 18	2 Base Addr 10	2 Base Addr 2
1 Base Addr 25	1 Base Addr 17	1 Base Addr 9	1 Reserved
0 Base Addr 24	0 Base Addr 16	0 Base Addr 8	0 Memory Space Ind.

1Bh Reserved R/W ADD 18/BE 3	1Ah Reserved R/W ADD 18/BE 2	19h Reserved R/W ADD 18/BE 1	18h Reserved R/W ADD 18/BE 0
7 Reserved 31	7 Reserved 23	7 Reserved 15	7 Reserved
6 Reserved 30	6 Reserved 22	6 Reserved 14	6 Reserved
5 Reserved 29	5 Reserved 21	5 Reserved 13	5 Reserved
4 Reserved 28	4 Reserved 20	4 Reserved 12	4 Reserved
3 Reserved 27	3 Reserved 19	3 Reserved 11	3 Reserved
2 Reserved 26	2 Reserved 18	2 Reserved 10	2 Reserved
1 Reserved 25	1 Reserved 17	1 Reserved 9	1 Reserved
0 Reserved 24	0 Reserved 16	0 Reserved 8	0 Reserved

1Fh Reserved R/W ADD 1C/BE 3	1Eh Reserved R/W ADD 1C/BE 2	1Dh Reserved R/W ADD 1C/BE 1	1Ch Reserved R/W ADD 1C/BE 0
7 Reserved 31	7 Reserved 23	7 Reserved 15	7 Reserved
6 Reserved 30	6 Reserved 22	6 Reserved 14	6 Reserved
5 Reserved 29	5 Reserved 21	5 Reserved 13	5 Reserved
4 Reserved 28	4 Reserved 20	4 Reserved 12	4 Reserved
3 Reserved 27	3 Reserved 19	3 Reserved 11	3 Reserved
2 Reserved 26	2 Reserved 18	2 Reserved 10	2 Reserved
1 Reserved 25	1 Reserved 17	1 Reserved 9	1 Reserved
0 Reserved 24	0 Reserved 16	0 Reserved 8	0 Reserved

23h Reserved R/W ADD 20/BE 3	22h Reserved R/W ADD 20/BE 2	21h Reserved R/W ADD 20/BE 1	20h Reserved R/W ADD 20/BE 0
7 Reserved 31	7 Reserved 23	7 Reserved 15	7 Reserved
6 Reserved 30	6 Reserved 22	6 Reserved 14	6 Reserved
5 Reserved 29	5 Reserved 21	5 Reserved 13	5 Reserved
4 Reserved 28	4 Reserved 20	4 Reserved 12	4 Reserved
3 Reserved 27	3 Reserved 19	3 Reserved 11	3 Reserved
2 Reserved 26	2 Reserved 18	2 Reserved 10	2 Reserved
1 Reserved 25	1 Reserved 17	1 Reserved 9	1 Reserved
0 Reserved 24	0 Reserved 16	0 Reserved 8	0 Reserved

27h Reserved R/W ADD 24/BE 3	26h Reserved R/W ADD 24/BE 2	25h Reserved R/W ADD 24/BE 1	24h Reserved R/W ADD 24/BE 0
7 Reserved 31	7 Reserved 23	7 Reserved 15	7 Reserved
6 Reserved 30	6 Reserved 22	6 Reserved 14	6 Reserved
5 Reserved 29	5 Reserved 21	5 Reserved 13	5 Reserved
4 Reserved 28	4 Reserved 20	4 Reserved 12	4 Reserved
3 Reserved 27	3 Reserved 19	3 Reserved 11	3 Reserved
2 Reserved 26	2 Reserved 18	2 Reserved 10	2 Reserved
1 Reserved 25	1 Reserved 17	1 Reserved 9	1 Reserved
0 Reserved 24	0 Reserved 16	0 Reserved 8	0 Reserved

2Bh Card Bus/CIS R ADD 28/BE 3	2Ah Card Bus/CIS R ADD 28/BE 2	29h Card Bus/CIS R ADD 28/BE 1	28h Card Bus/CIS R ADD 28/BE 0
7 CIS 31	7 CIS 23	7 CIS 15	7 CIS 7
6 CIS 30	6 CIS 22	6 CIS 14	6 CIS 6
5 CIS 29	5 CIS 21	5 CIS 13	5 CIS 5
4 CIS 28	4 CIS 20	4 CIS 12	4 CIS 4
3 CIS 27	3 CIS 19	3 CIS 11	3 CIS 3
2 CIS 26	2 CIS 18	2 CIS 10	2 CIS 2
1 CIS 25	1 CIS 17	1 CIS 9	1 CIS 1
0 CIS 24	0 CIS 16	0 CIS 8	0 CIS 0

2Fh Sub-System ID R ADD 2C/BE 3	2Eh Sub-System ID R ADD 2C/BE 2	2Dh Sub-Sys Vendor ID R ADD 2C/BE 1	2Ch Sub-Sys Vendor ID R ADD 2C/BE 0
7 Sub-System ID 31	7 Sub-System ID 23	7 Sub-System ID 15	7 Sub-System ID 7
6 Sub-System ID 30	6 Sub-System ID 22	6 Sub-System ID 14	6 Sub-System ID 6
5 Sub-System ID 29	5 Sub-System ID 21	5 Sub-System ID 13	5 Sub-System ID 5
4 Sub-System ID 28	4 Sub-System ID 20	4 Sub-System ID 12	4 Sub-System ID 4
3 Sub-System ID 27	3 Sub-System ID 19	3 Sub-System ID 11	3 Sub-System ID 3
2 Sub-System ID 26	2 Sub-System ID 18	2 Sub-System ID 10	2 Sub-System ID 2
1 Sub-System ID 25	1 Sub-System ID 17	1 Sub-System ID 9	1 Sub-System ID 1
0 Sub-System ID 24	0 Sub-System ID 16	0 Sub-System ID 8	0 Sub-System ID 0

33h ROM Base Ad 3 R/W ADD 30/BE 3	32h ROM Base Ad 2 R/W ADD 30/BE 2	31h ROM Base Ad 1 R/W ADD 30/BE 1	30h ROM Base Ad 0 R/W ADD 30/BE 0
7 Base Addr 31	7 Base Addr 23	7 Base Addr 15	7 Reserved
6 Base Addr 30	6 Base Addr 22	6 Base Addr 14	6 Reserved
5 Base Addr 29	5 Base Addr 21	5 Base Addr 13	5 Reserved
4 Base Addr 28	4 Base Addr 20	4 Base Addr 12	4 Reserved
3 Base Addr 27	3 Base Addr 19	3 Base Addr 11	3 Reserved
2 Base Addr 26	2 Base Addr 18	2 Reserved	2 Reserved
1 Base Addr 25	1 Base Addr 17	1 Reserved	1 Reserved
0 Base Addr 24	0 Base Addr 16	0 Reserved	0 Addr Decode Ena.

37h Reserved R/W ADD 34/BE 3	36h Reserved R/W ADD 34/BE 2	35h Reserved R/W ADD 34/BE 1	34h Reserved R/W ADD 34/BE 0
7 Reserved 31	7 Reserved 23	7 Reserved 15	7 Reserved
6 Reserved 30	6 Reserved 22	6 Reserved 14	6 Reserved
5 Reserved 29	5 Reserved 21	5 Reserved 13	5 Reserved
4 Reserved 28	4 Reserved 20	4 Reserved 12	4 Reserved
3 Reserved 27	3 Reserved 19	3 Reserved 11	3 Reserved
2 Reserved 26	2 Reserved 18	2 Reserved 10	2 Reserved
1 Reserved 25	1 Reserved 17	1 Reserved 9	1 Reserved
0 Reserved 24	0 Reserved 16	0 Reserved 8	0 Reserved

3Bh Reserved R/W ADD 38/BE 3	3Ah Reserved R/W ADD 38/BE 2	39h Reserved R/W ADD 38/BE 1	38h Reserved R/W ADD 38/BE 0
7 Reserved 31	7 Reserved 23	7 Reserved 15	7 Reserved
6 Reserved 30	6 Reserved 22	6 Reserved 14	6 Reserved
5 Reserved 29	5 Reserved 21	5 Reserved 13	5 Reserved
4 Reserved 28	4 Reserved 20	4 Reserved 12	4 Reserved
3 Reserved 27	3 Reserved 19	3 Reserved 11	3 Reserved
2 Reserved 26	2 Reserved 18	2 Reserved 10	2 Reserved
1 Reserved 25	1 Reserved 17	1 Reserved 9	1 Reserved
0 Reserved 24	0 Reserved 16	0 Reserved 8	0 Reserved

3Fh Max Lat R ADD 3C/BE 3	3Eh Min Grant R ADD 3C/BE 2	3Dh Interrupt Pin R ADD 3C/BE 1	3Ch Interrupt Line R/W ADD 3C/BE 0
7 Max Lat 7 = 0	7 Min Gnt 7 =0	7 Reserved	7 Line 7
6 Max Lat 6 = 0	6 Min Gnt 6 =0	6 Reserved	6 Line 6
5 Max Lat 5 = 0	5 Min Gnt 5 =0	5 Reserved	5 Line 5
4 Max Lat 4 = 0	4 Min Gnt 4 = 0	4 Reserved	4 Line 4
3 Max Lat 3 = 1	3 Min Gnt 3 = 1	3 Reserved	3 Line 3
2 Max Lat 2 = 0	2 Min Gnt 2 = 0	2 Pin 2 = 0	2 Line 2
1 Max Lat 1 = 0	1 Min Gnt 1 = 0	1 Pin 1 = 0	1 Line 1
0 Max Lat 0 = 0	0 Min Gnt 0 = 0	0 Pin 0 = 1	0 Line 0

Host Register File

The following are the BusMaster I/O registers:

03h Config - REV # R ADD 00/BE 3	02h Config - PROD # R ADD 00/BE 2	01h Vendor ID 1 R ADD 00/BE 1	00h Vendor ID 0 R ADD 00/BE 0
7 Mirr of Dev ID 15	7 Mirr of Dev ID 7	7 Mirr Vendor ID 15	7 Mirr Vendor ID 7
6 Mirr of Dev ID 14	6 Mirr of Dev ID 6	6 Mirr Vendor ID 14	6 Mirr Vendor ID 6
5 Mirr of Dev ID 13	5 Mirr of Dev ID 5	5 Mirr Vendor ID 13	5 Mirr Vendor ID 5
4 Mirr of Dev ID 12	4 Mirr of Dev ID 4	4 Mirr Vendor ID 12	4 Mirr Vendor ID 4
3 Mirr of Dev ID 11	3 Mirr of Dev ID 3	3 Mirr Vendor ID 11	3 Mirr Vendor ID 3
2 Mirr of Dev ID 10	2 Mirr of Dev ID 2	2 Mirr Vendor ID 10	2 Mirr Vendor ID 2
1 Mirr of Dev ID 9	1 Mirr of Dev ID 1	1 Mirr Vendor ID 9	1 Mirr Vendor ID 1
0 Mirr of Dev ID 8	0 Mirr of Dev ID 0	0 Mirr Vendor ID 8	0 Mirr Vendor ID 0

Dev ID [15:8] = Config Reg 03h = REV # = 1XXXXXXXh X loaded from external logic
Dev ID [7:0] = Config Reg 02h = PRODUCT # = 30h
PCI Vendor ID [15:0] = 10 4Bh

07h Sub-System ID R/W ADD 2C/BE 3	06h Sub-System ID R/W ADD 2C/BE 2	05h Sub-Sys Vendor ID R/W ADD 2C/BE 1	04h Sub-Sys Vendor ID R/W ADD 2C/BE 0
7 Sub-System ID 15	7 Sub-System ID 7	7 Sub-Sys Vendor ID 15	7 Sub-Sys Vendor ID 7
6 Sub-System ID 14	6 Sub-System ID 6	6 Sub-Sys Vendor ID 14	6 Sub-Sys Vendor ID 6
5 Sub-System ID 13	5 Sub-System ID 5	5 Sub-Sys Vendor ID 13	5 Sub-Sys Vendor ID 5
4 Sub-System ID 12	4 Sub-System ID 4	4 Sub-Sys Vendor ID 12	4 Sub-Sys Vendor ID 4
3 Sub-System ID 11	3 Sub-System ID 3	3 Sub-Sys Vendor ID 11	3 Sub-Sys Vendor ID 3
2 Sub-System ID 10	2 Sub-System ID 2	2 Sub-Sys Vendor ID 10	2 Sub-Sys Vendor ID 2
1 Sub-System ID 9	1 Sub-System ID 1	1 Sub-Sys Vendor ID 9	1 Sub-Sys Vendor ID 1
0 Sub-System ID 8	0 Sub-System ID 0	0 Sub-Sys Vendor ID 8	0 Sub-Sys Vendor ID 0

0Bh Dual Add 3 R/W ADD 08/BE 3	0Ah Dual Add 2 R/W ADD 08/BE 2	09h Dual Add 1 R/W ADD 08/BE 1	08h Dual Add 0 R/W ADD 08/BE 0
7 Dual - Add 63	7 Dual - Add 55	7 Dual - Add 47	7 Dual - Add 39
6 Dual - Add 62	6 Dual - Add 54	6 Dual - Add 46	6 Dual - Add 38
5 Dual - Add 61	5 Dual - Add 53	5 Dual - Add 45	5 Dual - Add 37
4 Dual - Add 60	4 Dual - Add 52	4 Dual - Add 44	4 Dual - Add 36
3 Dual - Add 59	3 Dual - Add 51	3 Dual - Add 43	3 Dual - Add 35
2 Dual - Add 58	2 Dual - Add 50	2 Dual - Add 42	2 Dual - Add 34
1 Dual - Add 57	1 Dual - Add 49	1 Dual - Add 41	1 Dual - Add 33
0 Dual - Add 56	0 Dual - Add 48	0 Dual - Add 40	0 Dual - Add 32

0Fh System Cntl R/W ADD 0C/BE 3	0Eh Reserved R ADD 0C/BE 2	0Dh User Defined R/W ADD 0C/BE 1	0Ch User Defined R/W ADD 0C/BE 0
7 Reserved	7 Reserved	7 User Def Bit	7 User Def Bit
6 Reserved	6 Reserved	6 User Def Bit	6 User Def Bit
5 Diagnostic Bit	5 Reserved	5 User Def Bit	5 User Def Bit
4 Hard Abort	4 Reserved	4 User Def Bit	4 User Def Bit
3 Halt State Mach.	3 Reserved	3 User Def Bit	3 User Def Bit
1 Reserved	2 Reserved	2 User Def Bit	2 User Def Bit
2 Driver Reset (W)	1 Reserved	1 User Def Bit	1 User Def Bit
0 Stop Clk (W)	0 Reserved	0 User Def Bit	0 User Def Bit

13h Host Block Count R/W ADD 10/BE 3	12h Reserved R/W ADD 10/BE 2	11h Host Control 0 R/W ADD 10/BE 1	10h Reserved R/W ADD 10/BE 0
7 Reserved	7 Reserved	7 Don't Reset FIFO	7 Reserved
6 Reserved	6 Reserved	6 DMA Odd Parity	6 Reserved
5 Reserved	5 Reserved	5 Add Local Wait States	5 Reserved
4 Reserved	4 Reserved	4 Host Int. Edge/Level	4 Reserved
3 Reserved	3 Reserved	3 Ignore Access Err	3 Reserved
2 Host Block Count 2	2 Reserved	2 EN PCI REQ	2 Reserved
1 Host Block Count 1	1 Reserved	1 I/O or Memory Space	1 Reserved
0 Host Block Count 0	0 Reserved	0 Dual Add Cyc.	0 Reserved

17h Int Enable Register R/W ADD 14/BE 3	16h Reserved R/W ADD 14/BE 2	15h Reserved R/W ADD 14/BE 1	14h Reserved R/W ADD 14/BE 0
7 New Host CMD	7 Reserved	7 Reserved	7 Reserved
6 SG Transfer Done	6 Reserved	6 Reserved	6 Reserved
5 Global INT Status	5 Reserved	5 Reserved	5 Reserved
4 MFIFO_RDY	4 Reserved	4 Reserved	4 Reserved
3 User Defined bit	3 Reserved	3 Reserved	3 Reserved
2 SCSI INT Status	2 Reserved	2 Reserved	2 Reserved
1 Extended Status	1 Reserved	1 Reserved	1 Reserved
0 Command Complete	0 Reserved	0 Reserved	0 Reserved

1Bh Command R/W ADD 18/BE 3	1Ah Host Xfer Counter 2 R/W ADD 18/BE 2	19h Host Xfer Counter 1 R/W ADD 18/BE 1	18h Host Xfer Counter 0 R/W ADD 18/BE 0
7 Disable Interrupt	7 Xfer Cnt 23	7 Xfer Cnt 15	7 Xfer Cnt 7
6 DMA Trans Size 1	6 Xfer Cnt 22	6 Xfer Cnt 14	6 Xfer Cnt 6
5 DMA Trans Size 0	5 Xfer Cnt 21	5 Xfer Cnt 13	5 Xfer Cnt 5
4 Host Trans Size 1	4 Xfer Cnt 20	4 Xfer Cnt 12	4 Xfer Cnt 4
3 Host Trans Size 0	3 Xfer Cnt 19	3 Xfer Cnt 11	3 Xfer Cnt 3
2 Trans Dir 2	2 Xfer Cnt 18	2 Xfer Cnt 10	2 Xfer Cnt 2
1 Trans Dir 1	1 Xfer Cnt 17	1 Xfer Cnt 9	1 Xfer Cnt 1
0 Trans Dir 0	0 Xfer Cnt 16	0 Xfer Cnt 8	0 Xfer Cnt 0

1Fh Host Address 3 R/W ADD 1C/BE 3	1Eh Host Address 2 R/W ADD 1C/BE 2	1Dh Host Address 1 R/W ADD 1C/BE 1	1Ch Host Address 0 R/W ADD 1C/BE 0
7 Host Addr 31	7 Host Addr 23	7 Host Addr 15	7 Host Addr 7
6 Host Addr 30	6 Host Addr 22	6 Host Addr 14	6 Host Addr 6
5 Host Addr 29	5 Host Addr 21	5 Host Addr 13	5 Host Addr 5
4 Host Addr 28	4 Host Addr 20	4 Host Addr 12	4 Host Addr 4
3 Host Addr 27	3 Host Addr 19	3 Host Addr 11	3 Host Addr 3
2 Host Addr 26	2 Host Addr 18	2 Host Addr 10	2 Host Addr 2
1 Host Addr 25	1 Host Addr 17	1 Host Addr 9	1 Host Addr 1
0 Host Addr 24	0 Host Addr 16	0 Host Addr 8	0 Host Addr 0

23h Reserved R ADD 20/BE 3	22h SEE Control R/W ADD 20/BE 2	21h Reserved R/W ADD 20/BE 1	20h Host PIO FIFO Data R/W ADD 20/BE 0
7 Reserved	7 EXT_ARB_ACK(RO)	7 Reserved	7 PIO FIFO Port 7
6 Reserved	6 EXT_ARB_REQ	6 Reserved	6 PIO FIFO Port 6
5 Reserved	5 SEE_MS (R/W)	5 Reserved	5 PIO FIFO Port 5
4 Reserved	4 Reserved = 0	4 Reserved	4 PIO FIFO Port 4
3 Reserved	3 SEE_CS (R/W)	3 Reserved	3 PIO FIFO Port 3
2 Reserved	2 SEE_CLK (R/W)	2 Reserved	2 PIO FIFO Port 2
1 Reserved	1 SEE_DO (R/W)	1 Reserved	1 PIO FIFO Port 1
0 Reserved	0 SEE_DI (RO)	0 Reserved	0 PIO FIFO Port 0

27h EXT ROM ADD W ADD 24/BE 3	26h BusMaster CNTL R/W ADD 24/BE 2	25h ROM POI ADDR R ADD 24/BE 1	24h ROM POI ADDR R/W ADD 24/BE 0
7 EXT ROM ADD 23	7 Reserved	7 ROM POI ADDR 15	7 ROM POI ADDR 7
6 EXT ROM ADD 22	6 FAST_SINGLE	6 ROM POI ADDR 14	6 ROM POI ADDR 6
5 EXT ROM ADD 21	5 Force One Xfer	5 ROM POI ADDR 13	5 ROM POI ADDR 5
4 EXT ROM ADD 20	4 Reserved	4 ROM POI ADDR 12	4 ROM POI ADDR 4
3 EXT ROM ADD 19	3 BIOS Flash Ena.	3 ROM POI ADDR 11	3 ROM POI ADDR 3
2 EXT ROM ADD 18	2 Reserved=0	2 ROM POI ADDR 10	2 ROM POI ADDR 2
1 EXT ROM ADD 17	1 Flush Xfer CNT	1 ROM POI ADDR 9	1 ROM POI ADDR 1
0 EXT ROM ADD 16	0 SCSI Termination	0 ROM POI ADDR 8	0 ROM POI ADDR 0

2Bh PCI Conf Mirror R/ ADD 28/BE 3	2Ah PIO ROM DATA R/W ADD 28/BE 2	29h FEATURE CNTL R/W ADD 28/BE 1	28h S/G ADDRESS R/W ADD 28/BE 0
7 PCI Wait State	7 PIO ROM DATA 7	7 Reserved	7 Scatter End Addr 3
6 Par Err Response	6 PIO ROM DATA 6	6 Reserved	6 Scatter End Addr 2
5 SERR#	5 PIO ROM DATA 5	5 RAM_PRS	5 Scatter End Addr 1
4 Memory W/I Enable	4 PIO ROM DATA 4	4 WIDE_SCSI	4 Scatter End Addr 0
3 Reserved	3 PIO ROM DATA 3	3 G_INT_DISABLE	3 Scatter Start Addr 3
2 Bus Master	2 PIO ROM DATA 2	2 BIOS SHARDOW	2 Scatter Start Addr 2
1 Memory Space	1 PIO ROM DATA 1	1 SHADOW RAM	1 Scatter Start Addr 1
0 I/O Space	0 PIO ROM DATA 0	0 SCATTER ENA	0 Scatter Start Addr 0

2Fh SYSTEM STATUS R ADD 2C/BE 3	2Eh Reserved R/W ADD 2C/BE 2	2Dh PCI Status Conf R/W ADD 2C/BE 1	2Ch Reserved R/W ADD 2C/BE 0
7 Power On Flag	7 Reserved	7 Detected Parity Err	7 Reserved
6 Slave Oper Done	6 Reserved	6 Signaled Sys Error	6 Reserved
5 DMA Oper Done	5 Reserved	5 Rec Master Abort	5 Reserved
4 Host Oper Done	4 Reserved	4 Rec Target Abort	4 Reserved
3 FIFO Full	3 Reserved	3 Reserved	3 Reserved
2 FIFO Empty	2 Reserved	2 Reserved	2 Reserved
1 Xfer Cnt = 0	1 Reserved	1 Reserved	1 Reserved
0 MFIFO Rdy	0 Reserved	0 Data Parity Detected	0 Reserved

33h Product Code R ADD 30/BE 3	32h Reserved R ADD 30/BE 2	31h Host Cntl R ADD 30/BE 1	30h Reserved R ADD 30/BE 0
7 Code =0	7 Reserved	7 Connected to Host	7 Reserved
6 Code =0	6 Reserved	6 Host Threshold	6 Reserved
5 Code =0	5 Reserved	5 Host Term Count	5 Reserved
4 Code =0	4 Reserved	4 Reserved	4 Reserved
3 Code =1	3 Reserved	3 Reserved	3 Reserved
2 Code =1	2 Reserved	2 Reserved	2 Reserved
1 Code =1	1 Reserved	1 Reserved	1 Reserved
0 Code =1	0 Reserved	0 Reserved	0 Reserved

37h Interrupt Status R ADD 34/BE 3	36h Extended Status R ADD 34/BE 2	35h STACK_ADD R/W ADD 34/BE 1	34h STACK_ DATA R/W ADD 34/BE 0
7 Command Reg Busy	7 Command Busy	7 User Def Bit	7 STK DT 7
6 SC/GA RAM Busy	6 PIO Over Run	6 User Def Bit	6 STK DT 6
5 Interrupt Asserted	5 Parity Error	5 User Def Bit	5 STK DT 5
4 FIFO RDY	4 Command Aborted	4 User Def Bit	4 STK DT 4
3 Reserved	3 Chip Reset Occurred	3 STK_ADD 3	3 STK DT 3
2 SCSI G_INT	2 FIFOorTC Contains Data	2 STK_ADD 2	2 STK DT 2
1 Extended Status	1 PCI Target Time Out	1 STK_ADD 1	1 STK DT 1
0 Command Complete	0 Target Abort	0 STK_ADD 0	0 STK DT 0

3Bh Host FIFO IN ADDR R/W ADD 38/BE 3	3Ah Reserved R/W ADD 38/BE 2	39h Current Host CNT R ADD 38/BE 1	38h Host FIFO CNT R/W ADD 38/BE 0
7 Reserved	7 Reserved	7 Current Host CNT 7	7 FIFO CNT 7
6 FIFO In Addr 6	6 Reserved	6 Current Host CNT 6	6 FIFO CNT 6
5 FIFO In Addr 5	5 Reserved	5 Current Host CNT 5	5 FIFO CNT 5
4 FIFO In Addr 4	4 Reserved	4 Current Host CNT 4	4 FIFO CNT 4
3 FIFO In Addr 3	3 Reserved	3 Current Host CNT 3	3 FIFO CNT 3
2 FIFO In Addr 2	2 Reserved	2 Current Host CNT 2	2 FIFO CNT 2
1 FIFO In Addr 1	1 Reserved	1 Current Host CNT 1	1 FIFO CNT 1
0 FIFO In Addr 0	0 Reserved	0 Current Host CNT 0	0 FIFO CNT 0

3Fh Reserved R/W ADD 3C/BE 3	3Eh Reserved R ADD 3C/BE 2	3Dh Reserved R ADD 3C/BE 1	3Ch Host FIFO OUT ADDR R/W ADD 3C/BE 0
7 Reserved	7 Reserved	7 Reserved	7 Reserved
6 Reserved	6 Reserved	6 Reserved	6 FIFO Out Addr 6
5 Reserved	5 Reserved	5 Reserved	5 FIFO Out Addr 5
4 Reserved	4 Reserved	4 Reserved	4 FIFO Out Addr 4
3 Reserved	3 Reserved	3 Reserved	3 FIFO Out Addr 3
2 Reserved	2 Reserved	2 Reserved	2 FIFO Out Addr 2
1 Reserved	1 Reserved	1 Reserved	1 FIFO Out Addr 1
0 Reserved	0 Reserved	0 Reserved	0 FIFO Out Addr 0

SCSI Register File

The following registers are used to control the SCSI module data path.

43h Interrupt Status 1 R ADD 40/BE 3	42h Interrupt Status 0 R ADD 40/BE 2	41h Interrupt Enable 1 R/W ADD 40/BE 1	40h Interrupt Enable 0 R/W ADD 40/BE 0
7 Bus Free	7 SCSI Reset Det.	7 EN Bus Free Int.	7 EN SCSI Rst Det Int.
6 XFER Count Zero	6 Auto Ph_missmatch	6 EN XFER CNT 0 Int.	6 EN Auto Ph miss Int.
5 Phase Change	5 Parity Error	5 EN PhChg Int.	5 EN Parity Error Int.
4 AUTOM STAT4	4 SCSI FIFO Error	4 EN AUTOM INT. 4	4 EN FIFO Error Int.
3 AUTOM STAT3	3 Sel Comp	3 EN AUTOM INT. 3	3 EN Sel Cmp Int.
2 AUTOM STAT2	2 SCAM Selection	2 EN AUTOM INT. 2	2 EN SCAM Selection
1 AUTOM STAT1	1 Re-selected	1 EN AUTOM INT. 1	1 EN Resel Int.
0 AUTOM STAT0	0 Timeout	0 EN AUTOM INT. 0	0 EN Timeout Int.

43h Clear Int. Status 1 W ADD 40/BE 3	42h Clear Int. Status 0 W ADD 40/BE 2
7 CLR Bus Free	7 CLR SCSI Rst Det.
6 CLR XFR CNT Zero	6 CLR Auto Ph misscomp
5 CLR Phase Ch.	5 CLR Parity Error
4 CLR AUTO STAT4	4 CLR FIFO Error
3 CLR AUTO STAT3	3 CLR SelCmp
2 CLR AUTO STAT2	2 CLR SCAM Selection
1 CLR AUTO STAT1	1 CLR Re-selected
0 CLR AUTO STAT0	0 CLR Timeout

47h RESET R/W ADD 44/BE 3	46h Port Control 0 R/W ADD 44/BE 2	45h SCSI Control 0 R/W ADD 44/BE 1	44h SCSI Signal R/W ADD 44/BE 0
7 Initiator CNTL(R/W)	7 EN SCSI Port	7 No Arbitration	7 SEL
6 Reserved must be 0	6 SCSI Port Direction	6 Select Target	6 BSY
5 SCAM_EN	5 EN DMA Port	5 Reserved must be 0	5 REQ
4 ACK_HOLD	4 EN DMA Direction	4 EN ATN* on Sel.	4 ACK
3 Reset DMA block	3 EN Host Port	3 Reserved must be 0	3 ATN
2 Reset SCSI block	2 Host Port Direction	2 EN ReSel as INIT.	2 C/D
1 Reset Prog. block	1 MP_SCSI_EN	1 RST	1 MSG
0 CLR FIFO(SELF CLR)	0 Start Timeout Cnt	0 SCAM_SEL_EN	0 I/O

4Bh Reserved ADD 48/BE 3	4Ah Byte/Xfr Count 2 R/W ADD 48/BE 2	49h Byte/Xfr Count 1 R/W ADD 48/BE 1	48h Byte/Xfr Count 0 R/W ADD 48/BE 0
7 Reserved	7 Byte Count 23	7 Byte Count 15	7 Byte Count 7
6 Reserved	6 Byte Count 22	6 Byte Count 14	6 Byte Count 6
5 Reserved	5 Byte Count 21	5 Byte Count 13	5 Byte Count 5
4 Reserved	4 Byte Count 20	4 Byte Count 12	4 Byte Count 4
3 Reserved	3 Byte Count 19	3 Byte Count 11	3 Byte Count 3
2 Reserved	2 Byte Count 18	2 Byte Count 10	2 Byte Count 2
1 Reserved	1 Byte Count 17	1 Byte Count 9	1 Byte Count 1
0 Reserved	0 Byte Count 16	0 Byte Count 8	0 Byte Count 0

4Fh Program Count0 R ADD 4C/BE 3	4Eh Additional Status R ADD 4C/BE 2	4Dh SCSI FIFO Data 1 R/W ADD 4C/BE 1	4Ch SCSI FIFO Data 0 R/W ADD 4C/BE 0
7 Reserved	7 SCAM TIME OUT EN	7 FIFO Data 15	7 FIFO Data 7
6 Reserved	6 AUTO EXEC	6 FIFO Data 14	6 FIFO Data 6
5 Automation PC 5	5 FAST SYNC R/W	5 FIFO Data 13	5 FIFO Data 5
4 Automation PC 4	4 Reserved	4 FIFO Data 12	4 FIFO Data 4
3 Automation PC 3	3 SCSI MODE 8 (global)	3 FIFO Data 11	3 FIFO Data 3
2 Automation PC 2	2 RESERVED	2 FIFO Data 10	2 FIFO Data 2
1 Automation PC 1	1 RESERVED	1 FIFO Data 9	1 FIFO Data 1
0 Automation PC 0	0 SCSI Parity Err	0 FIFO Data 8	0 FIFO Data 0

53h SCSI Select ID R/W ADD 50/BE 3	52h SCSI Self ID W ADD 50/BE 2	51h Wait Self ID 1 W ADD 50/BE 1	50h Wait Self ID 0 W ADD 50/BE 0
7 Selected ID 3(R/W)	7 Current ID 3 (RO)	7 Wait for SEL ID 15	7 Wait for SEL ID 7
6 Selected ID 2(R/W)	6 Current ID 2 (RO)	6 Wait for SEL ID 14	6 Wait for SEL ID 6
5 Selected ID 1(R/W)	5 Current ID 1 (RO)	5 Wait for SEL ID 13	5 Wait for SEL ID 5
4 Selected ID 0(R/W)	4 Current ID 0 (RO)	4 Wait for SEL ID 12	4 Wait for SEL ID 4
3 Select ID 3	3 Self ARB ID 3	3 Wait for SEL ID 11	3 Wait for SEL ID 3
2 Select ID 2	2 Self ARB ID 2	2 Wait for SEL ID 10	2 Wait for SEL ID 2
1 Select ID 1	1 Self ARB ID 1	1 Wait for SEL ID 9	1 Wait for SEL ID 1
0 Select ID 0	0 Self ARB ID 0	0 Wait for SEL ID 8	0 Wait for SEL ID 0

57h SCSI Syn Tar 15 W ADD 58/BE 3	56h SCSI Syn Tar 14 W ADD 58/BE 2	55h SCSI Syn Tar 13 W ADD 58/BE 1	54h SCSI Syn Tar 12 W ADD 58/BE 0
7 Sync Rate 2	7 Sync Rate 2	7 Sync Rate 2	7 Sync Rate 2
6 Sync Rate 1	6 Sync Rate 1	6 Sync Rate 1	6 Sync Rate 1
5 Sync Rate 0	5 Sync Rate 0	5 Sync Rate 0	5 Sync Rate 0
4 SCSI Mode 8	4 SCSI Mode 8	4 SCSI Mode 8	4 SCSI Mode 8
3 Offset 3	3 Offset 3	3 Offset 3	3 Offset 3
2 Offset 2	2 Offset 2	2 Offset 2	2 Offset 2
1 Offset 1	1 Offset 1	1 Offset 1	1 Offset 1
0 Offset 0	0 Offset 0	0 Offset 0	0 Offset 0

5Bh SCSI Syn Tar 11 W ADD 58/BE 3	5Ah SCSI Syn Tar 10 W ADD 58/BE 2	59h SCSI Syn Tar 9 W ADD 58/BE 1	58h SCSI Syn Tar 8 W ADD 58/BE 0
7 Sync Rate 2	7 Sync Rate 2	7 Sync Rate 2	7 Sync Rate 2
6 Sync Rate 1	6 Sync Rate 1	6 Sync Rate 1	6 Sync Rate 1
5 Sync Rate 0	5 Sync Rate 0	5 Sync Rate 0	5 Sync Rate 0
4 SCSI Mode 8	4 SCSI Mode 8	4 SCSI Mode 8	4 SCSI Mode 8
3 Offset 3	3 Offset 3	3 Offset 3	3 Offset 3
2 Offset 2	2 Offset 2	2 Offset 2	2 Offset 2
1 Offset 1	1 Offset 1	1 Offset 1	1 Offset 1
0 Offset 0	0 Offset 0	0 Offset 0	0 Offset 0

5Fh SCSI Syn Tar 7 W ADD 58/BE 3	5Eh SCSI Syn Tar 6 W ADD 58/BE 2	5Dh SCSI Syn Tar 5 W ADD 58/BE 1	5Ch SCSI Syn Tar 4 W ADD 58/BE 0
7 Sync Rate 2	7 Sync Rate 2	7 Sync Rate 2	7 Sync Rate 2
6 Sync Rate 1	6 Sync Rate 1	6 Sync Rate 1	6 Sync Rate 1
5 Sync Rate 0	5 Sync Rate 0	5 Sync Rate 0	5 Sync Rate 0
4 SCSI Mode 8	4 SCSI Mode 8	4 SCSI Mode 8	4 SCSI Mode 8
3 Offset 3	3 Offset 3	3 Offset 3	3 Offset 3
2 Offset 2	2 Offset 2	2 Offset 2	2 Offset 2
1 Offset 1	1 Offset 1	1 Offset 1	1 Offset 1
0 Offset 0	0 Offset 0	0 Offset 0	0 Offset 0

63h SCSI Syn Tar 3 W ADD 58/BE 3	62h SCSI Syn Tar 2 W ADD 58/BE 2	61h SCSI Syn Tar 1 W ADD 58/BE 1	60h SCSI Syn Tar 0 W ADD 58/BE 0
7 Sync Rate 2	7 Sync Rate 2	7 Sync Rate 2	7 Sync Rate 2
6 Sync Rate 1	6 Sync Rate 1	6 Sync Rate 1	6 Sync Rate 1
5 Sync Rate 0	5 Sync Rate 0	5 Sync Rate 0	5 Sync Rate 0
4 SCSI Mode 8	4 SCSI Mode 8	4 SCSI Mode 8	4 SCSI Mode 8
3 Offset 3	3 Offset 3	3 Offset 3	3 Offset 3
2 Offset 2	2 Offset 2	2 Offset 2	2 Offset 2
1 Offset 1	1 Offset 1	1 Offset 1	1 Offset 1
0 Offset 0	0 Offset 0	0 Offset 0	0 Offset 0

60h SCSI SYN ID Read R ADD 58/BE 0
7 Sync Rate 2
6 Sync Rate 1
5 Sync Rate 0
4 SCSI Mode 8
3 Offset 3
2 Offset 2
1 Offset 1
0 Offset 0

67h Start Execution 3 R/W ADD 5C/BE 3	66h Start Execution 2 R/W ADD 5C/BE 2	65h Start Execution 1 R/W ADD 5C/BE 1	64h Start Execution 0 R/W ADD 5C/BE 0
7 CNTL OPTION 2	7 CNTL OPTION 2	7 CNTL OPTION 2	7 CNTL OPTION 2
6 CNTL OPTION 1	6 CNTL OPTION 1	6 CNTL OPTION 1	6 CNTL OPTION 1
5 CNTL OPTION 0	5 CNTL OPTION 0	5 CNTL OPTION 0	5 CNTL OPTION 0
4 AutoStart Addr 4	4 AutoStart Addr 4	4 AutoStart Addr 4	4 AutoStart Addr 4
3 AutoStart Addr 3	3 AutoStart Addr 3	3 AutoStart Addr 3	3 AutoStart Addr 3
2 AutoStart Addr 2	2 AutoStart Addr 2	2 AutoStart Addr 2	2 AutoStart Addr 2
1 AutoStart Addr 1	1 AutoStart Addr 1	1 AutoStart Addr 1	1 AutoStart Addr 1
0 AutoStart Addr 0	0 AutoStart Addr 0	0 AutoStart Addr 0	0 AutoStart Addr 0

6Bh Gen Auto Reg. 2 R/W ADD 60/BE 3	6Ah Gen Auto Reg. 2 R/W ADD 60/BE 2	69h Gen Auto Reg. 1 R/W ADD 60/BE 1	68h Gen Auto Reg. 0 R/W ADD 60/BE 0
7 Data 7	7 Data 7	7 Data 7	7 Data 7
6 Data 6	6 Data 6	6 Data 6	6 Data 6
5 Data 5	5 Data 5	5 Data 5	5 Data 5
4 Data 4	4 Data 4	4 Data 4	4 Data 4
3 Data 3	3 Data 3	3 Data 3	3 Data 3
2 Data 2	2 Data 2	2 Data 2	2 Data 2
1 Data 1	1 Data 1	1 Data 1	1 Data 1
0 Data 0	0 Data 0	0 Data 0	0 Data 0

6Fh FIFO Write Addr R/W ADD 64/BE 3	6Eh FIFO Read Addr R/W ADD 64/BE 2	6Dh SCSI CLK Cntl 0 R/W ADD 64/BE 1	6Ch Timeout R/W ADD 64/BE 0
7 Reserved	7 Reserved	7 Reserved	7 Timeout 7
6 Reserved	6 Reserved	6 POWERDOWN	6 Timeout 6
5 Reserved	5 Reserved	5 Reserved	5 Timeout 5
4 FIFO Write 4	4 FIFO Read 4	4 EN Active Deassert	4 Timeout 4
3 FIFO Write 3	3 FIFO Read 3	3 EN ATN on Err	3 Timeout 3
2 FIFO Write 2	2 FIFO Read 2	2 SCSI Clock 2	2 Timeout 2
1 FIFO Write 1	1 FIFO Read 1	1 SCSI Clock 1	1 Timeout 1
0 FIFO Write 0	0 FIFO Read 0	0 SCSI Clock 0	0 Timeout 0

73h Spare Register R/W ADD 68/BE 3	72h Parity Control R/W ADD 68/BE 2	71h SCSI XFER Status R/W ADD 68/BE 1	70h Offset Counter R/W ADD 68/BE 0
7 Reserved	7 RESERVED	7 FIFO Full (R)	7 Reserved
6 Reserved	6 Timer Test Mode	6 FIFO Empty (R)	6 Reserved
5 INT_POL(0 for use)	5 Even Host Parity	5 FIFO Count 5	5 Reserved
4 LED	4 Invert SCSI Parity	4 FIFO Count 4	4 Offset Counter 4
3 ID_UNLOCK	3 EN SCSI Parity	3 FIFO Count 3	3 Offset Counter 3
2 SCSI Transfer Pad	2 User Defined Curr. SCSI	2 FIFO Count 2	2 Offset Counter 2
1 User Defined	Mode (RO)	1 FIFO Count 1	1 Offset Counter 1
0 User Defined	0 Host Mode 8 (FIFO)	0 FIFO Count 0	0 Offset Counter 0

77h Timer 1 R ADD 6C/BE 3	76h Timer 0 R ADD 6C/BE 2	75h SCSI Data 1 R/W ADD 6C/BE 1	74h SCSI Data 0 R/W ADD 6C/BE 0
7 Timer 19	7 Timer 11	7 SCSI Data 15	7 SCSI Data 7
6 Timer 18	6 Timer 10	6 SCSI Data 14	6 SCSI Data 6
5 Timer 17	5 Timer 9	5 SCSI Data 13	5 SCSI Data 5
4 Timer 16	4 Timer 8	4 SCSI Data 12	4 SCSI Data 4
3 Timer 15	3 Timer 7	3 SCSI Data 11	3 SCSI Data 3
2 Timer 14	2 Timer 6	2 SCSI Data 10	2 SCSI Data 2
1 Timer 13	1 Timer 5	1 SCSI Data 9	1 SCSI Data 1
0 Timer 12	0 Timer 4	0 SCSI Data 8	0 SCSI Data 0

Scatter/Gather Instruction RAM

Scatter/Gather Instruction RAM—80–FFh Address
(32 Bits by 32 Words) Addressable as Double Words Only

Command R/W	Transfer Count 2 R/W	Transfer Count 1 R/W	Transfer Count 0 R/W
Host Address 3 R/W	Host Address 2 R/W	Host Address 1 R/W	Host Address 0 R/W

SCSI Automation RAM

Program RAM—Shadowed in 80–FFh Address
(16 Bits by 64 Words) Addressable as Bytes and Words Only

Program Data 1 R/W	**Program Data 0 R/W**
7 Op code 7	7 Data 7
6 Op code 6	6 Data 6
5 Op code 5	5 Data 5
4 Op code 4	4 Data 4
3 Op code 3	3 Data 3
2 Op code 2	2 Data 2
1 Op code 1	1 Data 1
0 Op code 0	0 Data 0

6

Register Definition

About This Chapter

Read this chapter to find out

- A detailed description of each register in the BA-81C15 PCI

6

Register Definition

The registers in the BA-81C15 are described here in detail. These include PCI Configuration Space Registers, Host Register File Registers, and SCSI Register File Registers.

PCI Configuration Space

Register	Bits	R/W	Function
00h–VENDOR ID 0	7:0	(R/W)	**VENDOR ID 0:** Containing Byte 0 of the PCI Vendor ID, this register is hard-wired to the value of 4Bh. It is not affected by a low-level driver reset.
01h–VENDOR ID 1	7:0	(R/W)	**VENDOR ID 1:** Containing Byte 1 of the PCI Vendor ID, this register is hard-wired to the value of 10h. It is not affected by a low-level driver reset.
02h–DEVICE ID 0	7:0	(R/W)	**DEVICE ID 0:** Containing Byte 1 of the PCI Device ID. This register is always hard-wired to the value of 30h.
03h–DEVICE ID 1	7:0	(R/W)	**DEVICE ID 1:** Containing Byte 0 of the PCI Device ID, this register is loaded by external logic at power-up. For every clock after the RST# signal is released, the IDDAT is sampled and the value is shifted into the LSB of this register. The MSB is hard-wired to one. This register is not affected by a low-level driver reset.
04h–COMMAND 0	7	(R/W)	**WAIT CYC CNTL:** PCI SPECIFICATION—The default is one (power on reset) to provide a wait state should the motherboard need one. As the BA-81C15 does not need a wait state with most motherboards, the configuration routine should reset this bit.
	6	(R/W)	**PAR ERR RESPONSE:** PCI SPECIFICATION—The default is zero (power on reset), but on the BA-81C15 this bit is write-capable to a one.
	5	(R/W)	**VGA PAL SNOOP:** PCI SPECIFICATION—Not used in the BA-81C15.
	4	(R/W)	**MEMORY W/I ENABLE:** PCI SPECIFICATION—The default is zero (power on reset), but on the BA-81C15 this bit is write-capable to a one to enable Write and Invalidate.
	3	(R/W)	**SPECIAL CYCLES:** PCI SPECIFICATION—Not used in the BA-81C15.
	2	(R/W)	**BUS MASTER:** PCI SPECIFICATION—The default is zero (power on reset), but on the BA-81C15 this bit is write-capable to a one to BusMaster mode.
	1	(R/W)	**MEMORY SPACE:** PCI SPECIFICATION—The default is zero (power on reset), but on the BA-81C15 this bit is write-capable to a one to enable memory space.
	0	(R/W)	**I/O SPACE:** PCI SPECIFICATION—The default is zero (power on reset), but on the BA-81C15 this bit is write-capable to a one to enable I/O space.
05h–COMMAND 1	7:2	(R)	**RESERVED:**
	1	(R/W)	**FAST BACK TO BACK EN:** PCI SPECIFICATION—Setting this bit enables the Back-to-Back Request of the PCI bus (not implemented).
	0	(R/W)	**SERR# ENABLE:** PCI SPECIFICATION—Setting this bit enables the SERR signal on the PCI bus.

Register	Bits	R/W	Function
06h–STATUS 0	7:0	(R)	**RESERVED:**
07h–STATUS 1	7	(R/W)	**DETECTED PAR ERR:** PCI SPECIFICATION—The default is zero (power on reset). When set to one, this bit indicates a parity error.
	6	(R/W)	**SIGNALED SYSTEM ERR:** PCI SPECIFICATION—The default is zero (power on reset). When set to one, this bit indicates a system error.
	5	(R/W)	**REC MASTER ABORT:** PCI SPECIFICATION—The default is zero (power on reset). When set to one, this bit indicates a master abort.
	4	(R/W)	**REC TARGET ABORT:** PCI SPECIFICATION—The default is zero (power on reset). When set to one, this bit indicates the BusMaster received a target abort.
	3	(R/W)	**SIGNAL TARGET ABORT:** PCI SPECIFICATION—The default is zero (power on reset). When set to one, this bit indicates that the Target sent a target abort.
	2:1	(R/W)	**DEVSEL TM [1:0]:** PCI SPECIFICATION—These bits are hard-wired to zeros, to indicate *Fast* timing.
	0	(R/W)	**DATA PARITY DETECTED:** PCI SPECIFICATION—When set to one, this bit indicates that the PERR# signal is asserted and the BusMaster is active.
08h–REVISION ID	7:0	(R)	**REVISION ID [7.0]:** PCI SPECIFICATION—These bits are hard-wired to 02h to indicate revision of the BA-81C15.
09h–CLASS CODE 0	7:0	(R)	**CLASS CODE 0:** PCI SPECIFICATION—These bits are hard-wired to 0h.
0Ah–CLASS CODE 1	7:0	(R)	**CLASS CODE 1:** PCI SPECIFICATION—These bits are hard-wired to 0h.
0Bh–CLASS CODE 2	7:0	(R)	**CLASS CODE 2:** PCI SPECIFICATION—Hard-wired to 1h, these bits indicate that the BA-81C15 is a mass storage device.
0Ch–CACHE LINE SIZE	7:0	(R/W)	**CACHE LINE SIZE [7:0]:** PCI SPECIFICATION—These bits indicate the value that the BA-81C15 should use for bursting transfer count. The default is zero (power on reset). For the current application, it is highly recommended to use the value 4h.
0Dh–LATENCY TIMER	7:2	(R/W)	**LATENCY TIMER [7:2]:** PCI SPECIFICATION—These bits indicate the value that the BA-81C15 should use for latency time. The default is zero (power on reset).
	1:0	(R)	**LATENCY TIMER [1:0]:** PCI SPECIFICATION—Bits 1:0 are hard-wired to zero.
0Eh–RESERVED	7:0	(R)	**RESERVED:**
0Fh–RESERVED	7:0	(R)	**RESERVED:**
10–13h–I/O BASE ADDRESS 3–0	31:2	(R/W)	**BASE ADDRESS [31:2]:** PCI SPECIFICATION—These bits are used to assign the I/O base address to the BA-81C15. The default is zero (power on reset).
	1	(R/W)	**RESERVED:**
	0	(R/W)	**I/O SPACE INDICATED:** PCI SPECIFICATION—This bit is hard-wired to one to indicate that this register is used by the host to assign I/O base addresses to all local registers for R/W access.
14–17h–MEMORY BASE ADDRESS 3–0	31:2	(R/W)	**BASE ADDRESS [31:2]:** PCI SPECIFICATION—These bits are used to assign the memory base address to the BA-81C15. The default is zero (power on reset).
	1	(R/W)	**RESERVED:**
	0	(R/W)	**MEMORY SPACE INDICATED:** PCI SPECIFICATION—This bit is hard-wired to zero. It indicates that this register is used by the host to assign memory base addresses for memory mapped I/O access to all local registers.
18–1Bh–RESERVED	31:0	(R)	**RESERVED:**

Register	Bits	R/W	Function
1C–1Fh–RESERVED	31:0	(R)	**RESERVED:**
20–23h–RESERVED	31:0	(R)	**RESERVED:**
24–27h–RESERVED	31:0	(R)	**RESERVED:**
28–2Bh–CARD BUS - CIS	31:0	(R)	**CARD BUS - CIS [31:0]:** PCI SPECIFICATION—These bits indicate what value the BA-81C15 driver should be. To locate the Card Information Structure, refer to the PCMCIA v2.10 specification.
2C–2Dh–SUBSYSTEM VENDOR ID	15:0	(R)	**SUBSYSTEM VENDOR ID [15:0]:** PCI SPECIFICATION—These bits uniquely identify the add-in board or subsystem where the PCI device resides. This register allows the add-in card vendor to distinguish their cards even though the cards have the same PCI controller on them. This value is loaded automatically at POR from address 28h of the EEPROM.
2E–2Fh–SUBSYSTEM ID	15:0	(R)	**SUBSYSTEM ID [15:0]:** PCI SPECIFICATION—These bits uniquely identify the add-in board or subsystem where the PCI device resides. This register allows the add-in card vendor to distinguish their cards even though the cards have the same PCI controller on them. This value is loaded automatically at POR from address 29h of the EEPROM.
30–33h–ROM BASE ADDRESS 3–0	31:15	(R/W)	**ROM BASE ADDRESS [31:15]:** PCI SPECIFICATION—These bits are used to assign the ROM Base Address. The BA-81C15 supports a 32K BIOS space, but can address a 64K ROM by using a shadow bit. The default is zero (power on reset).
	14:1	(R/W)	**RESERVED:** This bit is hard-wired to zero.
	0	(R/W)	**ADDRESS DECODE ENABLE:** PCI SPECIFICATION—This bit is used to enable the BIOS address decode. The default is zero (power on reset). Zero disables the BIOS space.
34–37h–RESERVED	31:0	(R)	**RESERVED:**
38–3Bh–RESERVED	31:0	(R)	**RESERVED:**
3Ch–INTERRUPT LINE	7:0	(R/W)	**INTERRUPT LINE [7:0]:** PCI SPECIFICATION—These bits indicate the value that the BA-81C15 should use for the interrupt line. They must be programmed to the proper value which is determined by the user's system configuration. The default is zero (power on reset).
3Dh–INTERRUPT PIN	7:3	(R)	**RESERVED:**
	2:0	(R)	**INTERRUPT PIN [2:0]:** PCI SPECIFICATION—These bits indicate what value the BA-81C15 should use for Interrupt Line. This value is optionally loaded automatically at POR from address 2Bh of the EEPROM. See EEPROM loading for details. Currently only one Interrupt Line is supported, but the hardware engineer is free to connect that pin to any Interrupt Pin on the PCI Bus. If the register is not loaded from the EEPROM the value is preset to 01h, indicating Pin A.
3Eh–MINIMUM GRANT	7:0	(R)	**MINIMUM GRANT:** PCI SPECIFICATION—This value is optionally loaded automatically at POR from address 2Ch, lower byte of the EEPROM. See EEPROM loading for details. If the register is not loaded from the EEPROM, the value is preset to 08h.
3Fh–MAXIMUM LATENCY	7:0	(R)	**MAXIMUM LATENCY [7:0]:** PCI SPECIFICATION—This value is optionally loaded automatically at POR from address 2Ch, upper byte of the EEPROM. See EEPROM loading for details. If the register is not loaded from the EEPROM, the value is preset to 08h.

Host Register File

Register	Bits	R/W	Function
00h–MIRROR OF VENDOR ID 0	7:0	(R/W)	**VENDOR ID 0:** Containing Byte 0 of the PCI Vendor ID, this register is hard-wired to the value of 4Bh. It is not affected by a low-level driver reset.
01h–MIRROR OF VENDOR ID 1	7:0	(R/W)	**VENDOR ID 1:** Containing Byte 1 of the PCI Vendor ID, this register is hard-wired to the value of 10h. It is not affected by a low level driver reset.
02h–MIRROR OF DEVICE ID 0	7:0	(R/W)	**DEVICE ID 0:** Containing Byte 1 of the PCI Device ID, this register always contains a hard-coded value of 30h.
03h–MIRROR OF DEVICE ID 1	7:0	(R/W)	**DEVICE ID 0:** Containing Byte 0 of the PCI Device ID, this register is loaded by external logic at power-up. For every clock after RST# is released, the IDDAT is sampled and the value is shifted into the LSB of this register. The MSB is hard-wired to a one. This register is not affected by a low-level driver reset.
04h–05h–MIRROR OF SUBSYSTEM VENDOR ID	15:0	(R/W)	**MIRROR OF SUBSYSTEM VENDOR ID [15:0]:** PCI SPECIFICATION—These bits uniquely identify the add-in board or subsystem where the PCI device resides. This register allows the add-in card vendor to distinguish their cards even though the cards have the same PCI controller on them. This value is loaded automatically at POR from address 28h of the EEPROM. This register is writable from the I/O or Memory Space if needed by the BIOS.
06h–07h–MIRROR OF SUBSYSTEM ID	15:0	(R/W)	**MIRROR OF SUBSYSTEM ID [15:0]:** PCI SPECIFICATION—These bits uniquely identify the add-in board or subsystem where the PCI device resides. This register allows the add-in card vendor to distinguish their cards even though the cards have the same PCI controller on them. This value is loaded automatically at POR from address 29h of the EEPROM. This register is writable from the I/O or Memory Space if needed by the BIOS.
08–0Bh–DUAL ADDRESS/ USER DEFINED	31:0	(R)	**DUAL ADDRESS [63:32] or USER DEFINED:** This register holds the high 32-bit address for a 64-bit dual address cycle. (The enable for dual address cycle is located in Host Control 0 Register 11h Bit 0.) If this register is not being used for dual addressing, it can be used as a user-defined general purpose register.
0Ch–USER DEFINED	7:0	(R/W)	**USER DEFINED [7:0]:** This register can be used as a general purpose register.
0Dh–USER DEFINED	7:0	(R/W)	**USER DEFINED [7:0]:** This register can be used as a general purpose register.
0Eh–RESERVED	7:0		**RESERVED:**
0Fh–SYSTEM CONTROL	7	(R)	**RESERVED:**
	6	(R)	**RESERVED:**
	5	(R/W)	**Diagnostic Bit:** Must be set to zero.
	4	(R/W)	**HARD ABORT:** When this bit is asserted, the currently executing command is hard-aborted.
	3	(R/W)	**HALT STATE MACHINE:** When this bit is asserted the currently executing command is halted. This bit normally is set by the low-level driver prior to setting the hard-abort bit (Bit 4). It forces the chip to release the host bus, halt DMA activity and the like. Asserting this bit terminates execution of most commands. After setting this bit, the low-level driver must wait at least 50µsec before the currently executing command will abort.
	2	(R/W)	**RESERVED:**
	1	(W)	**DRIVER RESET:** This latched bit provides the BA-81C15 with a Driver Reset. This programmable reset is similar to a host or power-up reset except that most Configuration Registers are not affected.

Register	Bits	R/W	Function
	0	(R/W)	**STOP CLOCK BIT:** Setting this bit will synchronously stop the clocks in the BusMaster block. It has no effect on the SCSI clocks. **Note:** *Bits 3–4 of the System Control Register are cleared by a low-level driver or hard reset. Both bits must be set to one and a word write is required to enable the function. This is a special lock function for FIFO control.*
10h–RESERVED	7:0		**RESERVED:**
11h–HOST CONTROL 0	7	(R/W)	**DON'T RESET FIFO:** When a new BA-81C15 command is issued, the FIFO is reset and data contained within the FIFO is lost. If this bit is asserted, the BA-81C15 does not reset the FIFO when a new command is issued and so any data contained in the FIFO is processed. This bit usually is set only for error recovery.
	6	(R/W)	**DMA EVEN PARITY:** Setting this bit will cause the DMA parity generator to produce even parity. Parity is passed through the SCSI block and accordingly even parity will appear on the SCSI bus.
	5	(R/W)	**ADD LOCAL WAIT STATE:** For PCI bus operation the host PCI configuration utility writes directly to this bit. When this bit is asserted, the IRDY signal is toggled to insert a wait state for additional address and a wait state for additional write data set-up.
	4	(R/W)	**HOST INTERRUPT/LEVEL OR EDGE:** When asserted, this bit selects edge mode interrupt operation; when low, it selects level mode. Edge interrupts are always driven (totem pole output) and are high true. The low-to-high transition generates the interrupt request to the host processor. Level interrupts are driven by open collector drivers and are always low true. These interrupts can be shared by several I/O cards. The PCI bus should use level mode.
	3	(R/W)	**IGNORE ACCESS ERROR:** When this bit is asserted, the BA-81C15 does not halt the currently executing command if an access error occurs. The access error is still reported. An access error occurs when the -I/O CHCK signal is asserted.
	2	(R/W)	**ENABLE PCI REQUEST:** Setting this bit causes the PCI Request to be held active until the BusMaster is forced to give up the PCI Bus or the BusMaster voluntariy gives up the PCI Bus.
	1		**I/O MEMORY SPACE:** When this bit is set, the data is transferred to/from host I/O space. This bit allows the BA-81C15 to transfer data directly to/from an I/O card without using system memory. The default is zero for BusMaster data transfer with memory read/write cycles.
	0		**DUAL ADDRESS CYCLE ENABLE:** When this bit is asserted, the BA-81C15 is enabled to perform dual address bus cycle transfers to/from host memory. The upper 32-bit address can be programmed in Regs 08h-0Bh. **Note:** *This control register is cleared by a low level-driver or hard reset.*
12h–RESERVED	7:0	(R/W)	**RESERVED:**
13h–HOST BLOCK COUNT	7:3	(R/W)	**RESERVED:**

Register	Bits	R/W	Function
	2:0	(R/W)	**HOST BLOCK COUNT [2:0]:** The value written here sets the number of byte transfers to/from the PCI host when the BA-81C15 is BusMaster. For example, if the BA-81C15 is transferring data to the host and these bits equal b001b (see below), then the BA-81C15 waits until the FIFO contains at least eight bytes before arbitrating for host bus access. Once bus ownership is obtained, the BA-81C15 attempts to transfer the block count specified in this register before releasing the bus. The transfer terminates early if the BA-81C15 loses bus priority or is on the bus for too long (Register 14h). If Reg 17 Bit 7 is asserted, the BA-81C15 attempts to stay on the bus until the FIFO is empty/full. For current design version, values 0, 5, 6, and 7 are supported. **Note:** *These bits are cleared by a low-level driver or hard reset.*

BITS 2	1	0	NUMBER OF HOST TRANSFERS
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	64

14h–RESERVED	7:0	(R/W)	**RESERVED:**
15h–RESERVED	7:0	(R/W)	**RESERVED:**
16h–RESERVED	7:0	(R/W)	**RESERVED:**
17h–HOST INTERRUPT ENABLE			When the enable bit in this register is asserted and the corresponding status bit in the Interrupt Status Register 37h is a one, the BA-81C15 generates an interrupt to the host.
	7	(R/W)	**ENABLE NEW HOST COMMAND INT:** When this bit is set, the new host command interrupt is enabled.
	6	(R/W)	**ENABLE SG ADDRESS CHECK INT:** When this bit is set, the Scatter/Gather address check interrupt is enabled.
	5	(R/W)	**ENABLE GLOBAL INTERRUPT:** When this bit is set, the global interrupt is enabled.
	4	(R/W)	**MFIFO READY INT:** The corresponding status bit in Register 37h indicates the state of the MFIFO_RDY pin.
	3	(R/W)	**USER DEFINED:** Use of this bit does not affect interrupt logic.
	2	(R/W)	**SCSI GLOBAL INTERRUPT:** Setting this bit will allow any interrupt condition generated from enabled interrupts in Registers 40h and 41h to interrupt the host.
	1	(R/W)	**EXTENDED STATUS INT:** When this bit is asserted, the host receives an interrupt if any Extended Status Bit (Register 36h) is also asserted. The Extended Status Bit is cleared when Register 37h is read. The Extended Status Bit may be set before the transfer command completes. This bit should not be used to indicate Command Done status.
	0	(R/W)	**CMD COMPLETE INT:** Set this bit to receive a host interrupt when the currently executing command completes. The latched Command Complete Status Bit in Register 37h indicates that the command specified in the Transfer Command Register 1Bh has completed execution. The latched Command Complete Status Bit is cleared when Register 37h is read. **Note:** *This register is cleared by a low-level driver or hard reset.*

Register	Bits	R/W	Function
18–1Ah–HOST TRANSFER COUNTER	24:0	(R/W)	**HOST TRANSFER COUNTER [24:0]:** These registers contain the 24-bit data transfer count as shown below: Register 18h–Low Byte Register 19h–Middle Byte Register 1Ah–High Byte During data transfers this register is decremented on writes to the FIFO. It is used to control requests to transfer more data into the FIFO. When determining the number of bytes that have been transferred, the low-level driver should consider the transfer and FIFO counters (Register 38h). If the contents of these registers are read during a data transfer, they must be debounced. **Note:** *The 24-bit transfer counter is not affected by a low-level driver reset. It is set to zero by a hard reset.*
1Bh–HOST TRANSFER COMMAND	7	(R/W)	**DISABLE INTERRUPT:** Setting this bit will block the generation of Command Complete status (Reg 37h Bit 0) at the end of the operation. The low-level driver should set this bit when processing multiple Scatter/Gather segments. The bit should be set for all but the last Scatter/Gather segment, thus allowing a host interrupt to be generated only when the end of the Scatter/Gather list is reached.
	6:5	(R/W)	**DMA DATA TRANSFER SIZE [1:0]:** These bits indicate the width of the DMA interface data path. The current BA-81C15 supports only an 8-bit DMA width.

BITS 6	BITS 5	DMA DATA TRANSFER FILE
0	0	RESERVED
0	1	8 BIT
1	0	16 BIT
1	1	RESERVED

	4:3	(R/W)	**HOST DATA TRANSFER SIZE [1:0]:** These bits indicate the size of the host transfer.

BITS 4	BITS 3	HOST DATA TRANSFER SIZE
0	0	AUTOMATIC
0	1	8 BIT
1	0	16 BIT
1	1	32 BIT

If Bits 3 and 4 both equal zero, the BA-81C15 automatically performs odd byte count and odd address "clean-up" transfers. For example, if the host address is 0E0001h and the byte count is 21 (15h), the BA-81C15 chip performs three byte accesses to the host memory followed by four double-word (32-bit) accesses and then two byte-wide accesses. For the current design version, host 16-bit is not supported.

	2:0	(R/W)	**TRANSFER DIRECTION [2:0]:** When these bits are written, the command indicated below begins execution. The low-level driver must initialize all other registers (transfer count, etc.) before issuing a command to this register. The low-level driver can poll Register 36h for Command Complete or to receive an interrupt.

BITS 2	BITS 1	BITS 0	TRANSFER DIRECTION
0	0	0	HOST to DMA
0	0	1	DMA to HOST
0	1	0	HOST to PIO FIFO PORT
0	1	1	PIO FIFO PORT to HOST
1	0	0	DMA to PIO FIFO PORT
1	0	1	PIO FIFO PORT to DMA
1	1	0	RESERVED
1	1	1	NO OPERATION

Note: *In the current revision, Host to PIO FIFO Port does not work.*

Register	Bits	R/W	Function
1C–1Fh–HOST ADDRESS	31:0	(R/W)	**HOST ADDRESS [31:0]:** These registers contain the host bus address as shown below: Register 1Ch, Bits [0:7] Register 1Dh, Bits [8:15] Register 1Eh, Bits [16:23] Register 1Fh, Bits [24:31] The address placed in this register is incremented by 0, 1, 2, or 4 after each host bus access. The low-level driver may read (and debounce) these registers to monitor the progress of the data transfer. The contents of these registers are also useful for error recovery. **Note:** *The Host Address Register is not affected by a low-level driver or hard reset.*
20h–HOST PIO FIFO DATA	7:0	(R/W)	**HOST PIO FIFO PORT [7:0]:** When data is transferred between the host and the host FIFO using PIO, this register provides a buffer for the data. Data transfer size is 8 bits only. This register is not affected by a firmware or hard reset. **Note:** *Due to logic error the BusMaster FIFO is read only in the current revision.*
21h–RESERVED	7:0	(R/W)	**RESERVED:**
22h–EEPROM CONTROL	7	(R)	**EXT_ARB_ACK:** This bit reflects the status of the EXT_ARB_ARQ signal.
	6	(R/W)	**EXT_ARB_REQ:** Writing to this bit asserts the EXT_ARB_REQ signal.
	5	(R/W)	**SEE_MS:** This is the Master Select for the serial EEPROM, which must be enabled before any operations with the SEEPROM can be completed.
	4	(R/W)	**RESERVED:** This bit is reserved and is always set to zero.
	3	(W)	**SEE_CS:** This bit is connected to the output pin, which is connected to the chip select of the serial EPROM.
	2	(W)	**SEE_CLK:** This bit provides the access to the serial EEPROM clock line.
	1	(W)	**SEE_DO:** This bit is set to the desired value, which is then clocked to the serial EEPROM during write cycles.
	0	(R)	**SEE_DI:** This input bit is used to read data from the serial EEPROM.
23h–BRDCTL	7:0	(R)	**RESERVED:**
24h-25h– ROM PIO ADDRESS	15:0	(R/W)	**ROM PIO ADDRESS [15:0]:** This counter is used to address the ROM through the I/O or Memory Space. It will automatically increment on any read or write to Register 24h (PIO ROM Data Register). If the PIO port to the ROM is not being used, this could function as a user defined register.
26h–CONFIGUR-ATION	7	(R/W)	**RESERVED:**
	6	(R/W)	**FAST SINGLE:** Setting this bit to one enables the BusMaster to resume bus transfers (upon waiting two PCI clocks) after previously being pre-empted from the bus. It is recommended that this bit be set to one.
	5	(R/W)	**FORCE ONE TRANSFER:** Setting this to one is highly recommended for the case of host transfer starting address not at D-word boundary.
	4	(R/W)	**RESERVED:**
	3	(R/W)	**BIOS Flash Enable:** Setting this bit to one enables host write access to BIOS. This bit defaults to zero (power on reset).
	2	(R/W)	**RESERVED:**
	1	(R/W)	This bit provides an easy method to zero the transfer count for error recovery and command clean-up operation.
	0	(R/W)	**SCSI TERMINATION:** Setting this bit asserts the SCSI termination I/O pin to a high.
27h–EXTERNAL ROM ADDRESS	7:0	(W)	**EXTERNAL ROM ADDRESS [7:0]:** This register is used to address the ROM through the external hardware. The value written to this register will appear on the ROM Data Signals and EXT_ALE could be used to latch the data. EXT_ALE is high active and on the falling edge the address will be valid.

Register	Bits	R/W	Function
28h–SCATTER GATHER ADDRESS	7:4	(R/W)	**SCATTER/GATHER ENDING ADDRESS [3:0]:** These bits point to the ending Scatter/Gather element in Scatter/Gather RAM. The number, which indicates the address pointer to each 8-byte block for transfer command and transfer byte count, can be from 0h to 0Fh. After each Scatter/Gather element has been processed, this element number is compared against this value and if it is equal, the Scatter/Gather RAM halts operation and Bit 6 of Interrupt Status is cleared (Reg 37h).
	3:0	(R/W)	**SCATTER/GATHER STARTING ADDRESS [3:0]:** These bits are loaded with the starting Scatter/Gather element number of the Scatter/Gather RAM. The number can be programmed from 0h to 0Fh. When the Scatter/Gather RAM is turned on (Reg 29h Bit 0), this will be the first element to be executed. **Note:** *The total number of elements that can be programmed at one time is sixteen; this means the starting address can be equal to the ending address initially, and the next time when their value are equal, this condition will terminate Scatter/Gather transfer.*
29h–FEATURE CONTROL	7:5	(R/W)	**RESERVED:**
	4	(R)	**NARROW SCSI:** This bit initiates the status of WIDE# pin #99.
	3	(R/W)	**GLOBAL INTERRUPT DISABLE:** Setting this bit blocks the interrupt signal to the host. This blocks all sources of interrupt, whether BusMaster or SCSI. This allows the driver to disable all interrupts with one chip access.
	2	(R/W)	**BIOS SHADOW:** This bit is set when a 64K BIOS is being addressed; the bit is cleared when a 32K BIOS is being addressed.
	1	(R/W)	**SHADOW RAM:** Clearing this bit allows access to the Scatter/Gather RAM (Regs 80–FFh). Setting this bit allows access to the SCSI Automation RAM (Regs 80–FFh).
	0	(R/W)	**SCATTER/GATHER ENABLE:** Setting this bit to one starts Scatter/Gather automation and loads Registers 18h–1Fh with the first eight bytes of the Scatter/Gather RAM, which are pointed to by Reg 28h [3:0]. Once the transfer command completes (count=0), the next eight bytes are again loaded into Regs 18h–1Fh. This continues until the Scatter/Gather packet pointed to by Reg 28h [7:4]. The Scatter/Gather Enable Bit needs to be reset to zero every time the entire Scatter/Gather transfer is completed. The Scatter/Gather RAM may be accessed while the commands are being processed.
2Ah–PIO ROM DATA	7:0	(R/W)	**PIO ROM DATA [7:0]:** This register is used to send or receive data to the ROM. The value written to this register will appear on the ROM Data Signals along with the ROM_CS and MEM_RW to read or write the Flash Memory.
2BH–PCI COMMAND CONFIGURATION			**Note:** *This register is written to by the host PCI configuration utility. It provides coarse configuration control over the BA-81C15 chip. This register is cleared to zero by a hard reset and is not affected by a firmware reset.*
	7	(R/W)	**WAIT CYCLE CONTROL:** The BA-81C15 maps this bit to Register 11h Bit 5. When asserted, the BA-81C15 adds a wait state to the address and write data host transfer cycle. This bit is set by the PCI configuration utility.
	6	(R/W)	**PARITY ERROR RESPONSE:** Setting this bit allows parity errors to be reported to the host (PERR#) during PCI bus data phases. This bit is cleared by the generation of a chip reset condition RST#.
	5	(R/W)	**SERR#:** Mirror of Register 05h Bit 0 in the PCI configuration space. Setting this bit enables the SERR signal on the PCI bus.
	4	(R/W)	**MEMORY WRITE AND INVALIDATE ENABLE:** Enabling this bit allows the BA-81C15 to use Memory Write and Invalidate commands when it becomes BusMaster. Memory Write commands are used if this bit is disabled. This bit is cleared by an RST# condition.
	3	(R/W)	**RESERVED:**
	2	(R/W)	**ENABLE BUS MASTER OPERATION:** This bit does not control any hardware. The PCI configuration utility sets it to enable host bus master operation.
	1	(R/W)	**ENABLE MEMORY SPACE:** When set, this bit enables the BA-81C15 memory mapped I/O address decode logic. This bit mirrors Bit 1 of the PCI Configuration Command Register, which allows memory address selection on Configuration Register 14h to occur.

Register	Bits	R/W	Function
	0	(R/W)	**ENABLE I/O SPACE:** When asserted, this bit enables the BA-81C15 I/O address decode logic. This bit mirrors Bit 0 of the PCI Configuration Command Register, which allows I/O address selection on Configuration Register 10h to occur.
2Ch–PCI CACHE LINE SIZE	7:0	(R/W)	**CACHE LINE [7:0]:** These bits specify the system cache line size in 32–bit words. Based on the value stored in this register, the BA-81C15 will choose the optimal PCI command to use when accessing host data. During memory writes, Memory Write or Memory Write and Invalidate commands will be used. Memory read performance also benefits from use of the optimal command, Memory Read, or Memory Read Multiple. These bits are cleared by an RST# condition.
2DH–PCI STATUS CONFIGUR-ATION			**Note:** *This register is used to record status information for PCI-related events. PCI reads to this register behave normally. PCI writes are slightly different in that bits can be reset but not set. PCI Status Configuration bits are set by the firmware. They are cleared by a hard reset but are not affected by a firmware reset.*
	7	(R/W)	**DATA PARITY DETECTED:** This bit is set in response to detecting a parity error, regardless of the value of the Parity Error Response Bit in PCI Command Register 2Bh Bit 6.
	6	(R/W)	**SIGNALED SYSTEM ERROR:** This bit is set along with SERR# when the BA-81C15 detects a system error.
	5	(R/W)	**RECEIVED MASTER ABORT:** This bit is set by the firmware and cleared by the PCI host processor. When asserted this bit indicates that the last PCI transaction terminated with a master abort. The BA-81C15 generates a master abort only when the Target does not respond (assert DEVSEL) within sixteen local bus clock cycles of the address transaction. Register 36h contains the Device Timeout Bit.
	4	(R/W)	**RECEIVED TARGET ABORT:** This bit is set by the firmware and cleared by the PCI host processor. When asserted this bit indicates that the BA-81C15 received a target abort and terminated a bus master transfer early. Register 36h contains the Target Abort Bit.
	3:1	(R/W)	**RESERVED:** These bits are reserved and read zeros.
	0	(R/W)	**DATA PARITY DETECTED:** This bit is set in response to detecting PERR# asserted and the Parity Error Response Bit in PCI Command Register (Reg 2Bh Bit 6) is set.
2Eh–RESERVED	7:0	(R/W)	**RESERVED:**
2Fh–SYSTEM STATUS	7	(R)	**RESERVED:**
	6:4	(R)	**HOST OPERATION DONE, DMA OPERATION DONE, FIFO OPERATION DONE:** These bits indicate that the corresponding interface has completed its task. For example, when transferring data from the host to the FIFO and the transfer counter equals pseudo zero and the BA-81C15 chip has released the bus, then Bit 4 is asserted. These bits are valid only when the corresponding port is transferring data into the BA-81C15. **Note:** *"Pseudo" means that the FIFO look-ahead logic is setting the status until all of the writes and reads are reported.*
	3	(R)	**PCI FIFO FULL:** When asserted the PCI 128-byte FIFO is pseudo full.
	2	(R)	**PCI FIFO EMPTY:** When asserted thePCI 128-byte FIFO is pseudo empty.
	1	(R)	**PCI TRANSFER COUNTER = 0:** When this bit is asserted, the transfer counter is equal to pseudo zero. The transfer counter may in fact be non-zero but for the transfer size there are zero bytes left to transfer. For example, if the BA-81C15 is not in auto host sizing mode and is performing a straight 32-bit transfer (four bytes) from the host to the DMA interface and the transfer counter equals 3 (bytes), then this bit is set. The BA-81C15 cannot read any more data from the host (32 bits at a time) until the firmware changes the transfer size and re-issues the command.
	0	(R)	**PIO FIFO PORT DATA READY:** When the host is transferring data to/from the BA-81C15 using the FIFO port (Register 20h), this bit indicates that the chip is ready to accept more data.
30h–RESERVED	7:0	(R/W)	**RESERVED:**

Register	Bits	R/W	Function
31h–HOST STATUS 0			**Note:** *This status register provides information on the host interface when a transfer command is in progress.*
	7	(R)	**CONNECTED TO HOST:** When this bit is asserted the BA-81C15 is connected (BusMaster) to the host bus.
	6	(R)	**HOST THRESHOLD:** This bit indicates that the FIFO is ready for another block of data. This bit is for chip test purposes only.
	5	(R)	**HOST TERM COUNT:** When this bit is asserted the BA-81C15 chip must load the host transfer counter with the count in the FIFO (host write operations) or transfer counter (host read operations). This bit is asserted for the last host transfer before a command completes. This bit is for chip test purposes only.
	4:0	(R)	**RESERVED:**
32h–RESERVED	7:0	(R)	**RESERVED:**
33h–REVISION NUMBER	7:0	(R)	**REVISION NUMBER:** This number represents the current revision number of the BA-81C15.
34h–STACK DATA	7:0	(R/W)	**STACK DATA:** This register is for read/write access to a 16-byte deep stack with the address index programmed in Register 35h.
35h–STACK ADDRESS	7:4	(R/W)	**USER DEFINED:**
	3:0	(R/W)	**STACK ADDRESS:** This register is used to set the address index for data proper read/write access to stack through Register 34h.
36h–EXTENDED STATUS			**Note:** *This register provides extended status for the driver. When any error bit (Bits 6-0) in this register is asserted, extended status of the Interrupt Status Register 37h Bit1 is also asserted.*
	7	(R)	**COMMAND BUSY:** This bit is asserted while a BA-81C15 command is executing. The driver may poll this bit for a command complete condition.
	6	(R)	**HOST PIO FIFO PORT OVERRUN:** This bit indicates that an over/underrun condition occurred while transferring data between the BA-81C15 and the local Host PIO FIFO Port. The BA-81C15 needs twelve clocks from the trailing edge of an access to the Host PIO FIFO Data Buffer (Register 20h) to the leading edge of the next access. The overrun condition can be avoided by polling Register 2Fh Bit 0 before transferring data to/from Register 20h or by connecting the PIO FIFO RDY pin to a DMA controller on the PIO FIFO Port bus.
	5	(R)	**PARITY ERROR:** This bit is asserted when a parity error is detected on data received over the DMA interface or PCI parity error.
	4	(R)	**COMMAND ABORTED:** This bit is asserted when the driver performs a hard abort or halts command execution (Reg 0Fh [4:3]).
	3	(R)	**CHIP RESET OCCURRED:** This bit is asserted when a chip reset occurs.
	2	(R)	**FIFO OR TC CONTAINS DATA:** This bit sets if the FIFO contains data or the host transfer counter is not equal to pseudo zero when a command completes.
	1	(R)	**PCI TARGET TIMEOUT:** When performing a BusMaster cycle, the slave must respond with DEVSEL within sixteen local bus clocks or this bit is asserted and the transfer is terminated. When this bit is set the driver also should reset the PCI Status Configuration Register 2Dh Bit 5 before starting the next transfer command.
	0	(R)	**TARGET ABORT:** This bit is asserted when the BusMaster transaction is aborted by the Target. When this occurs the current command stops execution. The driver should reset the PCI Status Configuration Register 2Dh Bit 4 before starting the next transfer command.

Register	Bits	R/W	Function
37h–HOST INTERRUPT STATUS			**Note:** *When the Mask Bit in the Interrupt Enable Register 17h is asserted and the corresponding status bit in this register is a one, the BA-81C15 generates an interrupt to the host, using the configured interrupt line.*
	7	(R)	**COMMAND BUSY:** This bit indicates that the command loaded into the Command Register 1Bh is still operating and presumably still is transferring data.
	6	(R)	**SCATTER/GATHER RAM BUSY:** This bit indicates that the Scatter/Gather RAM has been enabled (Reg 29h Bit 0) and is still transferring data.
	5	(R)	**HOST INTERRUPT ASSERTED:** When this bit is asserted, the IRQA# host interrupt pin also is asserted. This pin is asserted by the BA-81C15.
	4	(R)	**FIFO READY:** This bit indicates the state of the MFIFO_RDY pin.
	3	(R)	**RESERVED:**
	2	(R)	**SCSI GLOBAL INTERRUPT:** This bit indicates that at least one of the enabled SCSI interrupts (Regs 40h–41h) has occurred.
	1	(R)	**EXTENDED STATUS:** This latched status bit is asserted when any of the extended status (Register 36h) bits is set to a one. The Latched Extended Status Bit is cleared when this register is read. The Extended Status Bit may be set before the transfer command completes; therefore this bit should not be used to indicate Command Done status.
	0	(R)	**CMD COMPLETE:** This latched status bit is asserted when the command specified in Transfer Command Register 1Bh finishes executing. The bit is cleared when this register is read. **Note:** *This status register is cleared by a firmware or hard reset.*
38H–HOST FIFO COUNTER	7:0	(R/W)	**HOST FIFO COUNT [7:0]:** This indicates the number of bytes currently in the FIFO. This register provides the driver with a method to directly read and write the FIFO counter. This is useful for error recovery. Since the FIFO counter is only seven bits wide, Bit 7 when asserted, forces a FIFO full condition.
39H–CURRENT HOST COUNTER	7:0	(R/W)	**CURRENT HOST COUNT [7:0]:** Indicates the number of transfers the BA-81C15 performed for the last host BusMaster access. This register is used primarily for chip testing.
3AH–RESERVED	7:0	(R/W)	**RESERVED:**
3BH–HOST FIFO IN ADDRESS	7:0	(R/W)	**HOST FIFO IN ADDRESS [7:0]:** This register provides the driver with a method to directly read and write the FIFO In Address. This is useful for error recovery.
3CH–HOST FIFO OUT ADDRESS	7:0	(R/W)	**HOST FIFO OUT ADDRESS [7:0]:** This register provides the driver with a method to directly read and write the FIFO Out Address. This is useful for error recovery.
3DH–RESERVED	7:0	(R/W)	**RESERVED:**
3Eh–RESERVED	7:0	(R/W)	**RESERVED:**
3Fh–RESERVED	7:0	(R/W)	**RESERVED:**

SCSI Register File

Register	Bits	R/W	Function
40h/41h SCSI INTERRUPT ENABLE 0/1	7:0		This bit, when set, causes Register 37h Bit 2 to be asserted when the corresponding readable bit is asserted in the Interrupt Status/Clear Registers (Regs 42h–43h, R/W). This bit, when cleared, prevents Register 37h Bit 2 from being asserted when the corresponding readable bit is asserted in the Interrupt Status/Clear Registers (Regs 42h–43h, R/W).
42h SCSI INTERRUPT STATUS/ CLEAR 0	7	(R)	**SCSI RESET OCCURRED:** This bit indicates that the SCSI Bus RST signal has been asserted. This will cause BA-81C15 to deassert all SCSI Bus signals it may have been driving. All BA-81C15 SCSI Controller Logic also will be reset to clear any active operations and to put the State Machines into a known state.
		(W)	**CLEAR SCSI RESET OCCURRED STATUS:** Setting this bit clears the SCSI Reset Occurred status (the readable value of this bit). This bit does not need to be explicitly reset.
	6	(R)	**AUTOMATION PHASE MISMATCH:** When set, this bit indicates that the SCSI Automation (also known as Initiator Automation Logic) has halted due to a phase mismatch.
		(W)	**CLEAR AUTOMATION PHASE MISMATCH STATUS:** Setting this bit clears Automation Phase Mismatch status (the readable value of this bit). This bit does not need to be explicitly reset.
	5	(R)	**PARITY ERROR:** This bit is set if a parity error is detected on the host or SCSI interfaces. The user must read Additional Status Register 4Eh Bit 0, R/W to determine the interface on which the parity error occurred.
		(W)	**CLEAR PARITY ERROR STATUS:** Setting this bit clears the Parity Error status (the readable value of this bit). This bit does not need to be explicitly reset.
	4	(R)	**SCSI FIFO ERROR:** This bit is set by an Overrun or Underrun Error on the FIFO. There may be a problem with the DMA or the Synchronous SCSI Transfer. The user must read the SCSI Signal Status Register to determine which port had the error.
		(W)	**CLEAR FIFO ERROR STATUS:** Setting this bit clears the FIFO Error Status (the readable value of this bit). Setting this bit also clears the FIFO, Current Offset, Read Address, Write Address, and Full/Empty Status Logic, *even if the FIFO Error Status Bit is not set.* This bit does not need to be explicitly reset.
	3	(R)	**SELECTION COMPLETE:** When set, this bit signals the successful completion of the command to "Arbitrate and Select a Target." It does not become set by being Re-selected. The Select Target Bit is loaded in Register 45h Bit 6.
		(W)	**CLEAR SELECTION COMPLETE:** Setting this bit clears the SCSI Selection Complete status (the readable value of this bit). This bit does not need to be explicitly reset.
	2	(R)	**SCAM SELECTION DETECTED:** Setting this bit signifies that a successful SCAM selection has been detected.
		(W)	**CLEAR SCAM SELECTION DETECTED:** Setting this bit clears the SCAM Selection Detected status. This bit does not need to be explicitly reset.
	1	(R)	**RESELECTED AS INITIATOR:** When set, this bit indicates that the BA-81C15 was Re-selected and now is an Initiator. This will only take place if the Re-Selection Enable Bit is set. This only is affected by being Re-Selected as an Initiator and does not reflect Selection. The Re-Selection Enable Bit is loaded in Register 45h Bit 2.
		(W)	**CLEAR RESELECTED AS INITIATOR:** Setting this bit clears the Re-Selected as an Initiator status (the readable value of this bit). This bit does not need to be explicitly reset.
	0	(R/W)	**TIMEOUT:** This bit becomes asserted when the General Purpose Timer (GPT) times out. The timer starts automatically when a Selection/Res-election is started in Register 45h [6:5]. **CLEAR TIME-OUT STATUS:** Setting this bit clears the Timeout status (the readable value of this bit). This bit does not need to be explicitly reset.

Register	Bits	R/W	Function
43h SCSI INTERRUPT STATUS/ CLEAR 1	7	(R)	**BUS FREE:** This bit indicates that the BA-81C15 has detected Bus Free and 800ns have elapsed and was the initiator. It is better to enable automatic selection and let a BA-81C15 state machine wait for Bus Free state, because the selection logic will automatically Arbitrate and Select the Target without host intervention.
		(W)	**CLEAR BUS FREE STATUS:** Setting this bit clears Bus Free status. This bit does not need to be explicitly reset.
	6	(R)	**SCSI TRANSFER COUNT ZERO:** This bit indicates that the multi-byte operation has completed the write and that Transfer Count has decremented to zero. It does not mean that the FIFO has been emptied.
		(W)	**CLEAR TRANSFER COUNT ZERO STATUS:** Setting this bit clears the Transfer Count Zero status. This bit does not need to be explicitly reset.
	5	(R)	**PHASE CHANGE:** This bit indicates that the SCSI Bus Phase (C/D, MSG, and I/O) does not match expectations (as written to SCSI Control) or has changed during the current command (i.e., Data Out Phase changed to Message In Phase so that the Target could send Save Data Pointers and Disconnect Messages). **Note:** *This status bit is held reset during automation, so that it will indicate a valid phase change after the automation logic has completed.*
		(W)	**CLEAR PHASE CHANGE STATUS:** Setting this bit clears the Phase Change status. This bit does not need to be explicitly reset.
	4:0	(R)	**AUTOMATION STATUS:** These bits are set by a Stop and Set Interrupt (SSI) command from the automation. The value corresponds to the value of the data field of the SSI command. There is no protection provided for these bits, therefore a value can be over-written by another SSI command before it is accessed and cleared.
		(W)	**CLEAR AUTOMATION STATUS:** Setting these bits clears the Automation status. These bits do not need to be explicitly reset.
44h SCSI SIGNAL			**Note:** *All of the SCSI signals are addressable (can be written) if the SCAM EN bit is set (47h Bit 5). The BA-81C15 can be in any mode with regard to the SCSI bus (Initiator, Disconnected).*
	7	(W)	**SCSI SEL SIGNAL:** In Initiator or Disconnect mode, setting this bit will make the SEL signal active, and resetting it will make the SEL signal inactive. This is the opposite polarity from the negative true signal on the SCSI bus.
		(R)	The unlatched (current) state of the same signal (from the SCSI bus itself): 0=deasserted; 1=asserted.
	6	(W)	**SCSI BSY SIGNAL:** In Initiator or Disconnect mode, setting this bit will make the BSY signal active; resetting this bit will make the BSY signal inactive. This is the opposite polarity from the negative true signal on the SCSI bus.
		(R)	The unlatched (current) state of the same signal (from the SCSI Bus itself): 0=deasserted; 1=asserted
	5	(W)	**SCSI REQ SIGNAL:** Writing this bit has no effect unless SCAM Enable is set.
		(R)	The unlatched (current) state of the same signal (from the SCSI bus itself): 0=deasserted; 1=asserted
	4	(W)	**SCSI ACK SIGNAL:** In Initiator mode, setting this bit will make the ACK signal active and resetting this bit will make ACK inactive (this is the opposite polarity from the negative true signal on the SCSI bus).
		(R)	The unlatched (current) state of the same signal (from the SCSI bus itself): 0=deasserted; 1=asserted
	3	(W)	**SCSI ATN SIGNAL:** In Initiator mode, setting this bit will make the ATN signal active and resetting this bit will make ATN inactive (this is the opposite polarity from the negative true signal on the SCSI bus).
		(R)	The unlatched (current) state of the same signal (from the SCSI bus itself): 0=deasserted; 1=asserted
	2	(W)	**SCSI C/D SIGNAL:** In Initiator mode, this bit forms part of the phase reference field used to determine phase mismatch status.
		(R)	The unlatched (current) state of the same signal (from the SCSI bus itself): 0=deasserted; 1=asserted

Register	Bits	R/W	Function
	1	(W)	**SCSI MSG SIGNAL:** In Initiator mode, this bit forms part of the phase reference field used to determine phase mismatch status.
		(R)	The unlatched (current) state of the same signal (from the SCSI bus itself): 0=deasserted; 1=asserted
	0	(W)	**SCSI I/O SIGNAL:** In Initiator mode, this bit forms part of the phase reference field used to determine phase mismatch status.
		(R)	The unlatched (current) state of the same signal (from the SCSI bus itself): 0=deasserted; 1=asserted

C/D	MSG	I/O	Bus Phase
0	0	0	DATA OUT
0	0	1	DATA IN
1	0	0	COMMAND
1	0	1	STATUS
1	1	0	MESSAGE OUT
1	1	1	MESSAGE IN
0	1	0	RESERVED OUT
0	1	1	RESERVED IN

45h SCSI CONTROL 0	7	(R/W)	**NO ARBITRATION:** This bit, when set, allows the BA-81C15 to skip the SCSI Arbitration phase and jump straight to SCSI selection. This is used when there is only one Initiator and all Targets do not support disconnect/reconnect.
	6	(R/W)	**SELECT TARGET:** If this bit is set, the BA-81C15 will wait for Bus Free and Arbitrate for the SCSI bus; if it wins, the BA-81C15 will then Select a Target with the Selection ID. At the end of the operation the Selection Complete status will be set (Reg 42h Bit 3). If the BA-81C15 does not win Arbitration, it will wait for Bus Free and try again. If the Target does not respond, the Command will abort with Selection Timeout (Reg 42h Bit 0).
	5	(R/W)	**RESERVED:** Must be set to zero.
	4	(R/W)	**ENABLE ATN ON SELECTION:** This bit determines if Attention will be set on the Selection phase. There is a separate bit for setting Attention during Errors or Setting Attention directly.
	3	(R/W)	**RESERVED:** Must be set to zero.
	2	(R/W)	**ENABLE BEING RESELECTED AS AN INITIATOR:** If this bit is set, BA-81C15 will respond to being re-selected when the Self ID matches the ID during Re-Selection phase and parity is valid. This will set the Re-Selected as Initiator Status Bit after the BA-81C15 has become the Initiator (Reg 42h Bit 1).
	1	(W)	**SCSI RST SIGNAL:** In Initiator or Disconnect mode, setting this bit will make the RST signal active, and resetting this bit will make RST inactive (there is no protection on this signal, because the SCSI bus may have to be reset at times when the BA-81C15 is an Initiator). This is the opposite polarity from the negative true signal on the SCSI bus.
		(R)	The unlatched (current) state of the same signal (from the SCSI bus itself): 0=deasserted; 1=asserted.
	0	(R/W)	**SCAM SELECTION ENABLE:** If this bit is set, the BA-81C15 will respond to SCAM selection. This will set the SCAM Selection Detected Status Bit after the BA-81C15 has responded.

Register	Bits	R/W	Function
46h SCSI PORT CONTROL 0	7	(R/W)	**ENABLE SCSI PORT:** When set, this bit enables the SCSI port and, along with SCSI Port Direction and SCSI Mode 8, controls the access of the SCSI bus to and from BA-81C15. The SCSI port has the highest FIFO access priority so it will *always* gain control of any FIFO channel (determined by SCSI Port Direction) it is attempting to control.
	6	(R/W)	**SCSI PORT DIRECTION:** This bit controls the direction of the SCSI transfer when the SCSI Port Enable Bit is set. It effectively selects the FIFO channel that the SCSI port controls ("owns"): If Enable SCSI Port and SCSI Port Direction, the BA-81C15 is receiving data from SCSI (i.e., the SCSI port controls FIFO Read Channel). If Enable SCSI Port and *not* SCSI Port Direction, the BA-81C15 is sending data to the SCSI bus (i.e., SCSI port controls FIFO Write Channel).
	5	(R/W)	**ENABLE DMA PORT:** When set this bit enables the DMA port and, along with DMA port direction and DMA Mode 8, controls the access of the DMA bus to and from BA-81C15. The DMA port has the second highest FIFO access priority, so it will gain control of the FIFO channel (determined by DMA Port Direction) it is attempting to control as long as the SCSI port is not requesting the same channel.
	4	(R/W)	**DMA PORT DIRECTION:** This bit controls the direction of the DMA transfer when the DMA Port Enable bit is set. It effectively selects the FIFO channel that the DMA Port controls ("owns"): If Enable DMA port and DMA Port Direction, the BA-81C15 is receiving data from DMA (i.e., DMA port controls FIFO Read Channel). If Enable DMA Port and DMA Port Direction, the BA-81C15 is sending data to the DMA bus (i.e., DMA port controls FIFO Write Channel).
	3	(R/W)	**ENABLE HOST PORT:** When set, this bit enables ExtHOST to access the FIFO via {FIFO Data}. Host port has lowest priority access to the FIFO channels; if either SCSI Port or DMA port controls the same FIFO Channel as the host port is trying to control, ExtCPU accesses {to FIFO Data} will not access the FIFO.
	2	(R/W)	**HOST PORT DIRECTION:** When the Enable Host Port bit is set, this bit selects the FIFO channel that the Slave port is attempting to use ("own"): If Enable Host Port and Host Port Direction, the Host may write {FIFO Data} to place data into the FIFO. If Enable Host Port and *not* Host Port Direction, the Host may read {FIFO Data} to fetch data from the FIFO. **Note:** *The Host port is subordinate to all other ports, which means that if any other port(s) are trying to control the same FIFO Channel, they will always "win" (and the Host port will be "shut out") so the above rules apply only if the SCSI and DMA ports are not attempting to control the same FIFO channel that the Host port is trying to use.*
	1	(R/W)	**MICRO-PROCESSOR SCSI BUS ACCESS ENABLE:** Setting this bit allows the Host to write data directly to the SCSI data bus, through SCSI DATA 0/1 (Regs 6Ch–6Dh). This is useful when writing a single message or status bytes to avoid having to move the data in through the FIFO. SCSI DATA 0/1 (Regs 6Ch–6Dh) can be read at any time.
	0	(R/W)	**START TIME-OUT COUNTER:** When this bit is set from a previously cleared state, the Timer Counter *begins* counting upward (incrementing). If this bit is written set and it was previously set, the Timer Counter values are unaffected (it was counting upward before, and will continue to count upward). When this bit is cleared, the Timeout Counter is halted and cleared.

Register	Bits	R/W	Function
47h SCSI RESET CONTROL 0	7	(W)	**INITIATOR MODE:** Writing this bit will set Initiator mode in the BA-81C15. This will only work if the Target has already connected to the SCSI bus and this bit was reset by Chip Reset or SCSI Block Reset.
		(R)	**INITIATOR MODE:** This bit is set by either the Selection Logic or the BA-81C15 being Re-Selected by a Target. The bit will stay active as long as the BA-81C15 remains in the Target mode. The BA-81C15 has to have the Target Disconnect from the SCSI bus before it is no longer an Initiator.
	6	(R/W)	**RESERVED:** Must be set to zero.
	5	(R/W)	**SCAM ENABLE:** If this bit is set, the BA-81C15 will allow the driver to write to any of the SCSI Bus Control signals which otherwise would be protected. This function is done to allow the driver to do SCAM Selection and to assign SCAM IDs.
	4	(R/W)	**ACK HOLD ENABLE:** In Initiator Mode, setting this will cause BA-81C15 to hold the ACK signal asserted on the last transfer so that the Initiator low-level driver can assert ATN (before deasserting ACK) if it wishes to signal the Target that it has a message for it. If this bit is not set, the handshake will complete normally and the Target is free to go to any SCSI Bus Phase it wants. On data from the SCSI bus, ACK is held on Transfer Counter = Zero. On transfers to the SCSI bus, ACK is held on the last byte out of the FIFO and Transfer Counter = Zero. Logic was added to allow the driver to single-step bytes into the BA-81C15. After the ACK Hold Logic has stopped the operation (i.e., Xfer CNT is zero and ACK is held), the driver writes a one to the already set ACK Hold Enable Bit. This causes the new logic to release the ACK, allowing the Target to transfer another byte. When the byte is transferred, the ACK Hold Logic will again hold the ACK.
	3	(W)	**DMA BLOCK RESET:** Setting this bit causes the DMA interface to reset. This bit is not self-clearing.
	2	(W)	**SCSI BLOCK RESET:** Setting this bit causes the SCSI interface to reset. This bit is not self-clearing.
	1	(W)	**PROGRAM BLOCK RESET:** Setting this bit causes the Program RAM State Machine, Related Address to the RAM, and Program Enable Bit to be reset. This bit is not self-clearing. This bit can be used to abort automation logic.
	0	(W)	**CLEAR FIFO:** Setting this bit causes the FIFO to reset independently of the interface logic. This bit resets the address counters (both in and out), the status counter, and the FIFO offset counter. This bit is self-clearing and will take four clocks to clear.
48h–4AH SCSI BYTE/ TRANSFER COUNT 0–2	23:0	(R/W)	**BYTE/TRANSFER COUNT:** This register holds the transfer count used during transfers between the DMA interface and the SCSI bus. This is a byte count and will decrement by two in word mode. Doing a byte write to Byte 0 will cause the upper two bytes to be cleared automatically. This forces the bytes to be written in lowest to highest order. This register can be loaded with a 32-bit write. This function was added because automation logic can only address the LSB. On DMA to SCSI, this counter is decremented when data is read out of the FIFO by the SCSI device. On SCSI to DMA, this counter will decrement when data is read by the DMA interface.
4Bh RESERVED	7:0	(R)	**RESERVED:**
4Ch/4Dh SCSI FIFO DATA 0/1	15:0	(R/W)	**FIFO DATA:** When Enable Host Port (Reg 46h Bit 3, R/W) is set, data can be written to or read from the FIFO through these registers. The SCSI Transfer Status and FIFO Address Registers are updated each time this register is read or written (by two when in Host Mode 16). When Enable Host Port is false, reads and writes to this register have no effect on the BA-81C15. **Note:** *In Host Mode 8, writing to Register 4Ch will load the adjacent bytes into the FIFO, and reading from Register 4Ch will unload the adjacent bytes from the FIFO. All data in 8-bit mode should be sent through this register.*

Register	Bits	R/W	Function
4Eh SCSI ADDITIONAL STATUS	7	(R/W)	**SCAM TIME OUT ENABLE:** Setting this bit reconfigures the TIMEOUT (Reg 64h) to compare bits [11:4] of the timer to determine timeout conditions. When this bit is cleared, then bits [19:12] are used to determine timeout conditions. This bit is used when checking for legacy devices during SCAM configuration, when a selection time-out of 1–4 milliseconds is needed.
	6	(R/W)	**AUTO EXEC:** This bit indicates the operation status of SCSI automation state machines. When set, it signifies that automation is executing.
	5	(R/W)	**FAST SYNC ENABLE:** Setting this bit adds a 1/2 clock to the Sync rate values (bits [7:5]) of the SCSI Sync Device Control Registers (Regs 54h–63h).
	4	(R)	**RESERVED:** Must be cleared to zero.
	3	(R)	**SCSI MODE 8 GLOBAL ENABLE:** Setting this bit overrides the SCSI 8-bit mode in the SCSI Sync Control Registers [3:0]. It is was added as a back-up to 8-bit SCSI support.
	2	(R)	**RESERVED:**
	1	(R)	**RESERVED:**
	0	(R)	**SCSI PARITY ERROR:** This bit sets when there is a parity error on the SCSI bus. The SCSI Signal Status Register also is cleared by writing so that an image does not need to be kept by the Slave.
4Fh SCSI PROGRAM COUNT 0	7	(R/W)	**RESERVED:**
	6	(R/W)	**RESERVED:**
	5:0	(R)	**AUTOMATION PROGRAM COUNTER [5:0]:** These bits show the word address of the instruction which is about to be executed in the automation RAM. This value is an offset from the beginning of the automation RAM (Reg 80h).
50h SCSI WAIT SELF ID 0	7:0	(R/W)	**WAIT SELF ID [7:0]:** (Low byte). These bits are used for Wait for Re-Selection IDs. Each bit set in this field represents a SCSI ID which the BA-81C15 will respond to when that SCSI ID is asserted during Re-Selected (if "Enable Re-Selection as Initiator" in {SCSI Interface Control} is set). This means that one BA-81C15 connected to a SCSI bus may take on the role of any number of Initiators (with the necessary low-level driver support). The low-level driver may determine which SCSI ID BA-81C15 was Re-Selected, as read by the (encoded) ID found in Current ID Bits in SCSI Self ID Register 52h [7:4], R.
51h SCSI WAIT SELF ID 1	7:0	(R/W)	**WAIT SELF ID [15:8]:** (High byte). See explanation above.
52h SCSI Current ID 0	7:4	(R)	**CURRENT ID [3:0]:** These bits signal the ID of the device the BA-81C15 is after being Re-selected. This is used when multiple bits are set in the Wait Self ID Register 50h–51h. Writing to these bits in this register will not affect any logic in BA-81C15.
	3:0	(R/W)	**SELF ARBITRATION ID [3:0]:** Contains the SCSI Device ID that the BA-81C15 will use during Arbitration. This is used because the BA-81C15 can operate with multiple bits set in the Wait Self ID Registers (Regs 50h–51h).
53h SCSI SELECT ID 1	7:4	(R/W)	**SELECTED/RE-SELECTED ID [3:0]:** These bits hold the ID of the SCSI device which was Selected by the BA-81C15 or which *most recently* Re-Selected the BA-81C15. These bits are default to Read Only. While Register 73h Bit 3 is set to one, these bits can be programmed as 0h–0fh to set the read pointer from 57h to 63h when doing read access to Register 60h. Information then can be obtained about the synchronous transfer rate for each corresponding target.
	3:0	(R/W)	**SCSI SELECTION ID [3:0]:** Contains the SCSI ID of the device that the BA-81C15 is going to Select (making it effectively an argument/parameter of the "Select Target" command in SCSI Control 1 {Reg 45h, R/W}). Bit 3 is the MSB and Bit 0 is the LSB. This addresses sixteen devices, and it should be noted that on an 8-bit SCSI bus only bits [2:0] are valid.

Register	Bits	R/W	Function
54h–63h SCSI SYNCHRO-NOUS DEVICE CONTROL 15–0	7:5	(R/W)	**SCSI RATE CONTROL [2:0]:** These bits control the time between pulse of REQ or ACK during the SCSI Synchronous Data Transfer. This is used with the SCSI speed to set the transfer rate. The pulse width will be exactly half of the value used. If the BA-81C15 is a Target, this sets the rate of REQ. If the BA-81C15 is an Initiator, this sets the rate of ACK, driving the SCSI bus interface. **Note:** *Only those values shown in the table are supported.*

SCSI RATE CONTROL 2:0	FAST SYNCI	PULSE WIDTH	PERIOD	TRANSFER
000	0	1.0 CLOCK	2.0 CLOCKS	20.0MB/S
000	1	1.5 CLOCKS	2.5 CLOCKS	20.0MB/S
001	0	2.0 CLOCKS	4.0 CLOCKS	10.0MB/S
001	1	2.5 CLOCKS	4.5 CLOCKS	10.0MB/S
010	0	3.0 CLOCKS	6.0 CLOCKS	6.6MB/S
010	1	3.5 CLOCKS	6.5 CLOCKS	6.6MB/S
011	0	4.0 CLOCKS	8.0 CLOCKS	5.0MB/S
011	1	4.5 CLOCKS	8.5 CLOCKS	5.0MB/S
100	0	5.0 CLOCK	10.0 CLOCKS	4.0MB/S
100	1	5.5 CLOCKS	10.5 CLOCKS	4.0MB/S
101	0	6.0 CLOCKS	12.0 CLOCKS	3.33MB/S
101	1	6.5 CLOCKS	12.5 CLOCKS	3.33MB/S
110	0	7.0 CLOCKS	14.0 CLOCKS	2.85MB/S
110	1	7.5 CLOCKS	14.5 CLOCKS	2.85MB/S
111	0	8.0 CLOCKS	16.0 CLOCKS	2.5MB/S
111	1	8.5 CLOCKS	16.5 CLOCKS	2.5MB/S

	4	(R/W)	**SCSI MODE 8:** When this bit is clear, any FIFO channel connected to the SCSI port (and the SCSI interface subsystem itself) transfers data in 16-bit parallel chunks during SCSI Bus *Data* phases (therefore the FIFO itself is said to be in a 16x16-bit configuration). During any other SCSI bus information transfer phases, regardless of the state of this bit, data is transferred in 8-bit parallel chunks (therefore the FIFO itself is said to be in a 32x8-bit configuration).
	3:0	(R/W)	**OFFSET COUNT [3:0]:** These bits control the offset, which is the number of unanswered REQs or ACKs on a SCSI Synchronous Data Transfer. This must not be set greater than 15 in word mode and 31 in byte mode, because the data will overrun the FIFO. If the offset count is set to zero then the SCSI Data Transfers are asynchronous. All non-data SCSI transfers are asynchronous. If the offset count is greater than zero, then the SCSI Data transfers are synchronous even if they are done by multi-byte PIO. Reading this register returns the value of the Offset Control Bits, not the Counter Bits. **Note:** *If in word (16-bit) SCSI mode, use even count (Mask Bit 0).*
64–67h START EXECUTION 0–3	7:5	(R/W)	**CONTROL OPTION [2:0]:** These bits select the condition used to start the automation logic. Only one start condition can start the automation at a time. Priority is assigned from Start Execution 3 to Start Execution 0, with Start Execution 3 having the highest priority. The execution is ordered and four programs can be set up to run under various conditions. If two starting registers have the same starting conditions, then the Automation Logic will start execution at the address in the register with the highest priority.

Condition	Comments
000	DISABLE
001	START IMMEDIATE
010	START ON SELECTION COMPLETE
011	START ON RESELECTION COMPLETE
100	START ON BUS FREE
101	START ON TRANSFER CNT = 0
110	START ON END OF DATA PHASE
111	START ON MSG IN OR MSG OUT PHASE

	4:0	(R/W)	**START ADDRESS [4:0]:** These are the upper five bits of the starting execution address of the automation. Since this field is only five bits wide, the automation must be started on an even word address.

Register	Bits	R/W	Function
68–6Bh GENERAL AUTO DATA	7:0	(R/W)	**DATA [7:0]:** These registers can be accessed by either the host or the automation. Automation instructions are designed to access these registers and can be used as a place to store such things as SCSI messages, error codes, and the like.
6Ch TIME-OUT	7:0	(R/W)	**TIMEOUT [7:0]:** The value written is compared against the Timeout counter (if running) to determine if Timeout (as defined by Interrupt Status) has occurred. If Test Mode is set then the Timeout runs off the DCLK signal, and if Test Mode is reset then the Timeout runs off of the SLOW SCSI CLK. Test Mode is Bit 0 of the SCSI Control 1 Register.
6Dh SCSI CLOCK CONTROL 0	7	(R/W)	**RESERVED:**
	6	(R/W)	**POWERDOWN:** Setting this bit turns off the internal clock.
	5	(R/W)	**RESERVED:** Writing or reading this bit has no effect on any logic in BA-81C15.
	4	(R/W)	**ENABLE ACTIVE DEASSERTION:** Setting this bit enables the active pull-ups on the SCSI bus (signals Data, Data Parity, REQ, ACK, I/O, C/D, MSG, and ATN), which will aid the termination in deasserting the SCSI bus signals by supplying current at three points on the bus. The active pull-up will supply between 7 and 14 mA of current until the driver senses about 3 volts.
	3	(R/W)	**SET ATN ON ERROR:** In Initiator Mode, setting this bit will cause BA-81C15 to assert ATN when there is a SCSI bus parity error during an information transfer phase. ATN is never set when the SCSI bus is in Bus Free mode, or after a SCSI reset.
	2:0	(R/W)	**SCSI SYSTEM CLOCK INTERFACE CONTROL [2:0]:** These bits control the relationship between the System Clock, the SCSI timers, and other time dependent logic in the SCSI interface of the BA-81C15 chip: **SCSI SYSTEM CLOCK INTERFACE CONTROL 2:0** — **FREQUENCY** 000 — DCLK ≤ 10MhZ 001 — 10MHz < DCLK ≤ 20MhZ 010 — 20MHz < DCLK ≤ 30MhZ 011 — 30MHz < DCLK ≤ 40MhZ 100 — 40MHz < DCLK ≤ 50MhZ **Note:** *Only those values shown in the table are supported.*
6Eh SCSI FIFO READ ADDRESS	7:5	(R/W)	**RESERVED:** Writing or reading this bit has no effect on any logic in the BA-81C15.
	4:0	(R/W)	**SCSI FIFO READ ADDRESS [4:0]:** These bits show the value of the Read Address Register, which is a mod 16 counter used to address the read side of the FIFO. This is only included for test purposes, and the user should not need to use these status bits. During an operation requiring the FIFO, this counter may have to be software debounced.
6Fh SCSI FIFO WRITE ADDRESS	7:5	(R/W)	**RESERVED:** Writing or reading this bit has no effect on any logic in the BA-81C15.
	4:0	(R/W)	**SCSI FIFO WRITE ADDRESS [4:0]:** These bits show the value of the Write Address Register, which is a mod 16 counter used to address the write side of the FIFO. This is only included for test purposes, and the user should not need to use these status bits. During an operation requiring the FIFO, this counter may have to be software debounced.

Register	Bits	R/W	Function
70h OFFSET COUNTER	7:5	(R/W)	**RESERVED:** Writing or reading these bits does not effect the BA-81C15.
	4:0	(R/W)	**REQ/ACK OFFSET COUNTER [4:0]:** Writing to this register is a asynchronous load of the REQ/ACK offset counter. Reading this register will return the value of the counter. The value of the counter is not affected by a read of this register. This counter is held at reset for all phases except data phase.
71h SCSI TRANSFER STATUS	7	(W)	Writing this bit does not affect the BA-81C15.
		(R)	**FIFO FULL:** This bit indicates the state of the FIFO. If it is set, the FIFO is full and cannot receive any more data. Since the Write operation is asynchronous to Changing the FIFO status, this signal has a time delay after the last write of as much as two clocks.
	6	(W)	Writing this bit does not affect the BA-81C15.
		(R)	**FIFO EMPTY:** This bit indicates the state of the FIFO. If it is set, the FIFO is empty and cannot be read. Since the Read operation is asynchronous to Changing the FIFO status, this signal has a time delay after the last read of as much as two clocks.
	5:0	(R/W)	**FIFO COUNT [5:0]:** These bits show the value of the counter which controls SCSI, and Slave access to the FIFO (reading this register does not affect the FIFO Counter). During an operation requiring the FIFO, this counter may have to be software debounced. Writing to this register is a synchronous load of the FIFO counter, therefore the driver should ensure that FIFO activity has ceased (by disabling *SCSI port* and the *processor port*) before writing. Further note that changing the value in this counter does not modify either FIFO address counter (i.e., the FIFO head or tail pointers): data read from the FIFO is still taken from *head, and data written is still written to *tail.
72h SCSI PORT CONTROL 1	7	(R/W)	**RESERVED:** Writing or reading this bit has no effect on any logic in BA-81C15.
	6	(R/W)	**TIMER TEST MODE:** Setting this bit causes the Timer to run off the fast clock. The fast clock comes from the OSCI input. It also changes the operation of the timer so that every eighth bit is driven from the fast clock.
	5	(R/W)	**HOST PARITY EVEN:** Setting this bit forces parity being generated for the SCSI FIFO on data coming from the *SLAVE Port* to be even. When this bit is reset, parity generated is odd.
	4	(R/W)	**INVERT SCSI PARITY:** Setting this bit forces parity being sent (generated or passed through parity) to the FIFO to be inverted for the SCSI interface data coming into the BA-81C15. This capability is available regardless of whether parity checking is enabled.
	3	(R/W)	**SCSI PARITY CHECKING:** Setting this bit enables parity checking on the SCSI data. In this mode parity is passed through to the FIFO. If this bit is reset, parity is generated on incoming data sent to the FIFO but not checked.
	2	(R/W)	**USER DEFINED:**
	1	(R)	**SCSI MODE:** Read Only Bit indicating the current bit width on SCSI interface. When this bit is a one, it means the 8-bit SCSI data path is being used.
	0	(R/W)	**HOST MODE 8:** This bit determines how a slave accesses the BA-81C15's register file. The CPU can change this mode at will. When Host Mode 8 = 0 ("Host Mode 16"), the LSB of the address is not used and all data accesses are 16 bits wide. E.g.,writing FIFO Data Register with Enable Host Port set inserts one word (two bytes) into the FIFO, incrementing the FIFO Counter and FIFO Tail pointer by two. When Host Mode 8 = 1, the LSB of the ExtCPU address is used to select a single byte in the register file that is to be accessed; only the low byte of the data bus is used. EX: writing FIFO Data Register with Enable Host Port set inserts one byte into the FIFO, incrementing the FIFO Counter and FIFO Tail pointer by one.

Register	Bits	R/W	Function
73h SPARE CONTROL	7:6	(R/W)	**RESERVED:** Writing or reading this bit has no effect on any logic in the BA-81C15.
	5	(R/W)	**USER DEFINED:**
	4	(R/W)	**LED*:** It is reset low by power on reset which means it is active. Writing a zero to this bit turns on the LED and writing a one turns off the LED.
	3	(R/W)	**ID_UNLOCK:** Setting this bit to one unlocks the host write access to high nibble of register 53h, which is read only (when this bit is zero) and indicates the Current Selected Device ID for normal application.
	2	(R/W)	**SCSI XFER PAD:** When this bit is set, transfer pad data on SCSI bus. A REQ*/ACK* handshake will be completed without altering or changing any FIFO data, counts, and status since there will be no real data transfer. This bit does not affect Syn Transfer; it only is used for Asyn Information phases.
	1	(R/W)	**USER DEFINED:**
	0	(R/W)	**USER DEFINED:**
74h/75h SCSI DATA BUS 0/1	15:0	(R/W)	**SCSI DATA [15:0]:** A *read* of this register returns the SCSI data held after it has been qualified. In the case of Commands, Messages, Status, and other 8-bit information, only Register 0Bh is valid. The SCSI data is qualified under the following conditions: a) The BA-81C15 is not in Initiator mode. The SCSI data is latched when the BA-81C15, having timed the Selection phase, has decided that the Selection is for itself and asserts BSY. b) The BA-81C15 is a Target and the Initiator has asserted ACK. c) The BA-81C15 is an Initiator and the Target has asserted REQ. Because this register works on the transfer signal from the sending device, it always stores the last data sent by the sending device. This register is not meant for use during any of the automatic transfers using multi-byte PIO or DMA. Writing to this register will not write to the FIFO and will not affect any registers in the BA-81C15.
76h–77h SCSI TIMER 0/1	15:0	(R)	**TIMER [15:0]:** These bits are to read the timer. Timer 1 accesses bits [19:12] of the selection timer, and Timer 0 accesses bits [11:4] of the timer. These bits are only included for test purposes, and the user should not need to use them. During an operation requiring the timer, this counter may have to be software debounced.
80h–FFh SCATTER/ GATHER INSTRUCTION RAM	31:24	(R/W)	**Note:** *If Register 29h Bit 1 is set, then Registers 80h–FFh become the Scatter/Gather Instruction RAM. This SGRAM is internally configured as 32-bits by 32-bytes, which forces all access to this RAM to be done using 32-bit double-word operations. If the bit is cleared, then Registers 80h–FFh become the Automation Program RAM. This RAM is internally configured as 16-bits by 64-bytes. The ARAM can be addressed as bytes or words only.* **BM COMMAND [7:0]:** These bits contain the command to be loaded into Command Register 1Bh when the Scatter/Gather processor executes this 8-byte command packet.
	23:0	(R/W)	**TRANSFER COUNT [23:0]:** These bits contain the Host Address count to be loaded into Xfer Count Registers 18h–1Ah when the Scatter/Gather processor executes this 8-byte command packet.

Register	Bits	R/W	Function
	31:0	(R/W)	**HOST ADDRESS [31:0]:** These bits contain the Data Transfer count to be loaded into Host Address Registers 1Ch–1Fh when the Scatter/Gather processor executes this 8-byte command packet.
			Command R/W | Transfer Count 2 R/W | Transfer Count 1 R/W | Transfer Count 0 R/W
			Host Address 3 R/W | Host Address 2 R/W | Host Address 1 R/W | Host Address 0 R/W
80h–FFh SCSI AUTOMATION RAM (Shadowed)	15:8	(R/W)	**PROGRAM OP CODE [15:8]:** These bits define the op code of the automation instruction to be executed. The instructions are defined in Chapter 7.
	7:0	(R/W)	**PROGRAM DATA [7:0]:** These bits define the data field associated with the Program Op Code. This field's definition varies depending upon the instruction selected in the Program Op Code Register.

7

Automation Instructions

About This Chapter

Read this chapter to find out

- A detailed definition of each automation instruction in the BA-81C15

7

Automation Instructions

No-Operation/Delay Instructions

No Operation/Delay Instructions

MNEMONIC = **NOP**

EXECUTION = 3 CLOCKS+(DELAY VALUE)_

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 0 0 0 0	0 0 0	X X DELAY VALUE

This instruction performs no operation and affects none of the internal registers. If the Delay Value is zero, this instruction executes in three clocks. For values greater than zero, this instruction will delay the specified number of clocks.

Compare Instructions

Compare Register with Instruction Data

MNEMONIC = **CRD**

EXECUTION = 3 CLOCKS+(SCSI **REQ/ACK** ASSERTION)

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 0 0 0 1	REG #	COMPARE DATA
08	0 0 0 - AR(0) 68h	
09	0 0 1 - AR(1) 69h	
0A	0 1 0 - AR(2) 6Ah	
0B	0 1 1 - AR(3) 6Bh	
0C	1 0 0 - SCSI DATA 74h	
	1 0 1 - AVAILABLE	
	1 1 0 - AVAILABLE	
	1 1 1 - RESERVED	

Note: *The term "available" denotes a space that is open for future use, but is undefined. "Reserved" means not usable.*

This instruction is used to compare the contents of the selected register with the data byte specified in the Instruction Data. The result of this operation is latched and remains valid until another COMPARE, OR, or AND instruction is executed.

The SCSI Data Register can be selected. If not in the Initiator mode, the instruction will wait for the Initiator mode before executing.

When in Initiator mode and the SCSI Data Register is specified, this instruction waits for the SCSI Request signal and compares the data present on the SCSI Data bus with the Instruction Data.

This instruction *does not* complete the SCSI Acknowledge handshake, and there is no Time Limit for the assertion of the SCSI Request signal.

Compare Register with Register

MNEMONIC = **CRR**

EXECUTION = 3 CLOCKS+(SCSI **REQ/ACK** ASSERTION)

OPCODE	***REGISTER***	***DATA***
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 0 0 1 0	REG #	X X X X X REG #
10	0 0 0 - AR(0)	X X X X X 0 0 0 - AR(0)
11	0 0 1 - AR(1)	X X X X X 0 0 1 - AR(1)
12	0 1 0 - AR(2)	X X X X X 0 1 0 - AR(2)
13	0 1 1 - AR(3)	X X X X X 0 1 1 - AR(3)
14	1 0 0 - SCSI DATA	X X X X X 1 0 0 - RESERVED
	1 0 1 - AVAILABLE	X X X X X 1 0 1 - AVAILABLE
	1 1 0 - AVAILABLE	X X X X X 1 1 0 - AVAILABLE
	1 1 1 - RESERVED	X X X X X 1 1 1 - LATCH_ID

This instruction is used to compare the contents of one register with the contents of another. The result of this operation is latched and remains valid until another COMPARE, OR, or AND instruction is executed.

The SCSI Data Register can be selected. If not in the Initiator mode, this instruction will wait for Initiator mode before executing.

When in Initiator mode and the SCSI Data Register is specified, this instruction waits for the SCSI Request signal and compares the data present on the SCSI Data bus with the Instruction Data.

This instruction *does not* complete the SCSI Acknowledge handshake, and there is no Time Limit for the assertion of the SCSI Request signal.

The LATCH_ID is the value of the Target Selected or the value of the Target which reselected the BA-81C15.

Branch Instructions

Compare SCSI Phase and Branch Equal

MNEMONIC = **CPE**

EXECUTION = 3 CLOCKS+(SCSI **REQ** ASSERTION)

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 1 0 0 1	PHASE	BRANCH ADDRESS
	C/D MSG I/O	ADDRESS

This instruction is used to compare the SCSI Bus Phase with the instruction Phase and branch to the specified address if the Phases match. It will only execute in the Initiator mode and will wait for that mode before executing. Once in Initiator mode, this instruction qualifies the SCSI Bus Phase with the SCSI Request signal and compares the Phase and Branches if Equal.

This instruction *does not* complete the SCSI Acknowledge handshake, and there is no Time Limit for the assertion of the SCSI Request signal.

Compare SCSI Phase and Branch Not Equal

MNEMONIC = **CPN**

EXECUTION = 3 CLOCKS+(SCSI **REQ** ASSERTION)

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 1 0 1 0	PHASE	BRANCH ADDRESS
	C/D MSG I/O	ADDRESS

This instruction is used to compare the SCSI Bus Phase with the instruction Phase and branch to the specified address if the Phase does not match. This instruction will only execute in the Initiator mode and will wait for that mode before executing. Once in Initiator mode, this instruction qualifies the SCSI Bus Phase with the SCSI Request signal and compares the Phase and Branches if Not Equal.

This instruction *does not* complete the SCSI Acknowledge handshake, and there is no Time Limit for the assertion of the SCSI Request signal.

Branch

MNEMONIC = **BRH**

EXECUTION = 3 CLOCKS

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 0 1 0 0	CONDITION	BRANCH ADDRESS
20	0 0 0 - ALWAYS	ADDRESS
21	0 0 1 - EQUAL	ADDRESS
22	0 1 0 - NOT EQUAL	ADDRESS
	0 1 1 - AVAILABLE	ADDRESS
	1 0 0 - AVAILABLE	ADDRESS
	1 0 1 - AVAILABLE	ADDRESS
	1 1 0 - AVAILABLE	ADDRESS
	1 1 1 - AVAILABLE	ADDRESS

This instruction is used to conditionally Branch to the specified address. The branch condition is set up by the previous COMPARE, OR, or AND instructions.

Test Condition and Branch

MNEMONIC = **TCB**

EXECUTION = 3 CLOCKS

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 0 1 0 1	CONDITION	BRANCH ADDRESS
	0 0 0 - RESERVED	ADDRESS
	0 0 1 - ATN SET	ADDRESS
	0 1 0 - ATN NOT SET	ADDRESS
	0 1 1 - XFER = 0	ADDRESS
	1 0 0 - FIFO = 0	ADDRESS
	1 0 1 - FIFO = 1	ADDRESS
	1 1 0 - Reserved	ADDRESS
	1 1 1 - AVAILABLE	ADDRESS

This instruction is used to conditionally Branch on the specified Conditions.

Move Instructions

Match SCSI Phase and Move Instruction Data

MNEMONIC = **MPM**

EXECUTION = 4 CLOCKS+(SCSI **REQ** ASSERTION)

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
1 0 0 0 0	PHASE	DATA
	C/D MSG I/O	

This instruction is used to match the SCSI Phase and move the Instruction Data field to the SCSI Data bus.

In Initiator mode, this instruction compares the SCSI Request qualified SCSI Bus phase with the Instruction Phase. If the Phases match, the Instruction Data is placed onto the SCSI Data bus, a 'Deskew+Cable Deskew' delay is generated, and the Acknowledge handshake is completed. If the Phases do not match, this instruction stops the current instruction sequence and generates an interrupt.

There is no Time Limit for the assertion of the SCSI Request signal.

Move Instruction Data to Register

MNEMONIC = **MDR**

EXECUTION = 3 CLOCKS or 4 CLOCKS+(SCSI **REQ** HANDSHAKE)

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 0 0 1 1	REG #	DATA
18	0 0 0 - AR(0)	
19	0 0 1 - AR(1)	
1A	0 1 0 - AR(2)	
1B	0 1 1 - AR(3)	
1C	1 0 0 - SCSI DATA	
	1 0 1 - AVAILABLE	
	1 1 0 - AVAILABLE	
	1 1 1 - AVAILABLE	

This instruction is used to move the Instruction Data field to the specified register. If not in Initiator mode, this instruction waits for Initiator mode before executing.

When in Initiator mode and the SCSI Data Register is specified, this instruction waits for the SCSI Request signal, places the Instruction Data onto the SCSI Data bus, waits one 'Deskew+Cable Deskew' delay, and completes the Acknowledge handshake.

There is no Time Limit for the assertion of the SCSI Acknowledge signal.

Move Register to Register

MNEMONIC = **MRR**

EXECUTION = 3 CLOCKS or 4 CLOCKS+(SCSI **REQ** HANDSHAKE)

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8 (SOURCE)**	**7 6 5 4 3 2 1 0 (DESTINATION)**
0 1 0 0 0	REG #	X X X X X REG #
40	0 0 0 - AR(0)	X X X X X 0 0 0 - AR(0)
41	0 0 1 - AR(1)	X X X X X 0 0 1 - AR(1)
42	0 1 0 - AR(2)	X X X X X 0 1 0 - AR(2)
43	0 1 1 - AR(3)	X X X X X 0 1 1 - AR(3)
44	1 0 0 - SCSI DATA	X X X X X 1 0 0 - SCSI DATA
45	1 0 1 - AVAILABLE	X X X X X 1 0 1 - AVAILABLE
	1 1 0 - AVAILABLE	X X X X X 1 1 0 - AVAILABLE
	1 1 1 - LATCH_ID	X X X X X 1 1 1 - BIT BUCKET

This instruction is used to move one specified register to another specified register. If not in the Initiator mode, this instruction will wait for the Initiator mode before executing.

When in Initiator mode and the SCSI Data is specified as the Source, this instruction waits for the SCSI Request signal, stores the data present on the SCSI Data bus in the specified Destination Register, and completes the Acknowledge handshake.

When in Initiator mode and the SCSI Data is specified as the Destination, this instruction waits for the SCSI Request signal, places the data specified by the Source Register onto the SCSI Data bus, a 'Deskew+Cable Deskew' delay is generated, and the Acknowledge handshake is completed.

There is no Time Limit for the assertion of the SCSI Request signal and the SCSI I/O signal is not qualified for Input or Output.

Do not specify the SCSI Data as both the Source and the Destination in either mode.

The LATCH_ID is the value of the Target Selected or the value of the Target which reselected the BA-81C15.

Logic Instructions

Logical AND Register with Instruction Data

MNEMONIC = **ADR**

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 0 1 1 0	REG #	DATA
	0 0 0 - AR(0)	
	0 0 1 - AR(1)	
	0 1 0 - AR(2)	
	0 1 1 - AR(3)	
	1 0 0 - SCSI DATA	
	1 0 1 - AVAILABLE	
	1 1 0 - AVAILABLE	
	1 1 1 - AVAILABLE	

This instruction is used to logically AND the specified register with the Instruction Data field. The result of this operation is latched and remains valid until another COMPARE, OR, or AND instruction is executed.

If the SCSI Data Register is selected in Initiator mode, this instruction waits for the SCSI Bus Request and logically ANDs the Instruction Data with the SCSI Data bus. If not in Initiator mode, this instruction waits for Initiator mode before executing.

The Acknowledge handshake is completed. There is no Time Limit for the assertion of the SCSI Bus Request signal.

Logical AND Register with Instruction Data and Store

MNEMONIC = **ADS**

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 1 1 1 0	REG #	DATA
	0 0 0 - AR(0)	
	0 0 1 - AR(1)	
	0 1 0 - AR(2)	
	0 1 1 - AR(3)	
	1 0 0 - RESERVED	
	1 0 1 - AVAILABLE	
	1 1 0 - AVAILABLE	
	1 1 1 - AVAILABLE	

This instruction is used to logically AND the specified register with the Instruction Data field and Store the results back into the specified register. The result of this operation is latched and remains valid until another COMPARE, OR, or AND instruction is executed.

Logical OR Register with Instruction Data

MNEMONIC = **ODR**

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 0 1 1 1	REG #	DATA
	0 0 0 - AR(0)	
	0 0 1 - AR(1)	
	0 1 0 - AR(2)	
	0 1 1 - AR(3)	
	1 0 0 - SCSI DATA	
	1 0 1 - AVAILABLE	
	1 1 0 - AVAILABLE	
	1 1 1 - AVAILABLE	

This instruction is used to logically OR the specified register with the Instruction Data field. The result of this operation is latched and will remain valid until another COMPARE, OR, or AND instruction is executed.

If the SCSI Data Register is selected in Initiator mode, this instruction waits for the SCSI Bus Request and logically ORs the Instruction Data with the SCSI Data bus.

The Acknowledge handshake is completed. There is no Time Limit for the assertion of the SCSI Bus Request signal.

Logical OR Register with Instruction Data and Store

MNEMONIC = **ODS**

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 1 1 1 1	REG #	DATA
	0 0 0 - AR(0)	
	0 0 1 - AR(1)	
	0 1 0 - AR(2)	
	0 1 1 - AR(3)	
	1 0 0 - RESERVED	
	1 0 1 - AVAILABLE	
	1 1 0 - AVAILABLE	
	1 1 1 - AVAILABLE	

This instruction is used to logically OR the specified register with the Instruction Data field and Store the results back into the specified register. The result of this operation is latched and remains valid until another COMPARE, OR, or AND instruction is executed.

Modify Instructions

Store to SCSI Register

MNEMONIC = **STR**

OPCODE	*REGISTER*	*DATA*
15 14 13 12	**11 10 9 8**	**7 6 5 4 3 2 1 0**
1 1 0 0	REG #	DATA/COMMENTS
	0 0 0 0 - INT ENABLE 1	ENABLE INTERRUPTS Reg 41h
	0 0 0 1 - INT STATUS 1	CLEAR INTERRUPT STATUS Reg 43h
	0 0 1 0 - SCSI SIGNAL	Reg 44h
	0 0 1 1 - SCSI CNTRL	Reg 45h
	0 1 0 0 - PORT CNTRL	Reg 46h
	0 1 0 1 - RESET SIGNAL	Reg 47h
	0 1 1 0 - XFER CNT 0	Reg 48h
	0 1 1 1 - XFER CNT 1	Reg 49h
	1 0 0 0 - XFER CNT 2	Reg 4Ah
	1 0 0 1 - RESERVED	
	1 0 1 0 - SCSI SEL ID	Reg 53h [0:3]
	1 0 1 1 - RESERVED	
	1 1 0 0 - AVAILABLE	
	1 1 0 1 - AVAILABLE	
	1 1 1 0 - AVAILABLE	
	1 1 1 1 - AVAILABLE	

This instruction is used to Store the Instruction Data into the specified register.

Reset ATN on REQ

MNEMONIC = **RAT**

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
0 1 1 0 1	RESERVED	RESERVED

This instruction is used to reset the Attention signal. Once this instruction is executed, the ATN signal will be deasserted before asserting ACK on the next handshake. Once ATN is deasserted, two "Deskew" delays are generated and the Acknowledge handshake is completed.

Stop and Set Interrupt

MNEMONIC = **SSI**

OPCODE	*REGISTER*	*DATA*
15 14 13 12 11	**10 9 8**	**7 6 5 4 3 2 1 0**
1 0 0 0 1	RESERVED	INTERRUPT VALUE

This instruction is used to set bits in the Interrupt Status 1, Register 43h. The Instruction Data is copied into the Interrupt Status 1 Register, and if the corresponding bit is set in the Interrupt Enable 1, Register 41h, an interrupt is generated.

8

Electrical Information

About This Chapter

Read this chapter to find out

- Electrical information about the BA-81C15
- Timing diagrams for the BA-81C15
- System cycles

8

Electrical Information

Absolute Maximum Ratings

Storage Temperature:	-55°C to 150°C
Power Supply Voltage:	0 to 7 V
Voltage on Any Pin:	VSS -.5 V to VDD + .5 V
Electrostatic Discharge:	5KV max.

Operating Test Conditions

Ambient Temperature:	0°C to 70°C
Supply Voltage:	4.75 to 5.25 V
Supply Current:	75mA typ.

DC Parameters

DC Specifications for PCI

Table 8-1 summarizes the DC specifications for 5 V signaling.

Table 8-1. DC Specifications for 5 V Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{cc}	Supply Voltage		4.75	5.25	V	
V_{ih}	Input High Voltage		2.0	V_{cc} + 0.5	V	
V_{il}	Input Low Voltage		-0.5	0.8	V	
I_{ih}	Input High Leakage Current	V_{in} = 2.7		70	µA	1
I_{il}	Input Low Leakage Current	V_{in} = 0.5		-70	µA	1
V_{oh}	Output High Voltage	I_{out} = -2mA	2.4		V	
V_{ol}	Output Low Voltage	I_{out} = 3mA, 6mA		0.55	V	2
C_{in}	Input Pin Capacitance			10	pF	3
C_{clk}	CLK Pin Capacitance		5	12	pF	
C_{IDSEL}	IDSEL Pin Capacitance			8	pF	4
L_{pin}	Pin Inductance			20	nH	5

[1] Input leakage currents include hi-Z output leakage for all bidirectional buffers with tri-state outputs.

[2] Signals without pull-up resistors must have 3mA low output current. Signals requiring pull-ups must have 6mA; the latter include FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used, AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.

[3] Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean, in general, that components for expansion boards would need to use alternatives to ceramic PGA packaging (i.e., PQFP, SGA, etc.)

[4] Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

[5] This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

SCSI

Table 8-2. SCSI Signals—SD(15-0)/, SDPO/, REQ/, MSG/, I/O, C/D, ATN/ ACK/, BSY/, SEL/, RST/, SDP1/

Parameter	Symbol	Min	Max	Unit	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Output low voltage	V_{OL}	V_{SS}	0.5	V	I_{OL} = 48mA
Hysteresis	V_{HYS}	200	-	mV	-
Input leakage current	I_{IN}	-10	10	µA	-
Input leakage—SCSI RST		-200	50	µA	-
Tri-state leakage current	I_{OZ}	-10	10	µA	-

Memory Port

Ta = 0° C to 70° C
VCC = 5 V ± 5%
GND = 0 V

Symbol	Definition	Min	Max	Units	Test Condition	Notes
V_{CC}	Supply Voltage	4.75	5.25	V		
I_{il1}	Input Current Leakage		+/-10	µA	V_{in} - .4 to V_{CC}	1
I_{il2}	Input Current Leakage		-50	µA	V_{in} - .4	2
I_{ol}	Output Current Leakage		+/-10	µA	V_{out} = .5 to V_{CC}	
V_{ih}	Input High Voltage	2.0		V		
V_{il}	Input Low Voltage		.8	V		
V_{oh1}	Ouput High Voltage	2.4			I_o = -4mA	3
V_{oh2}	Output High Voltage	2.4			I_o = -8mA	4
V_{oh3}	Output High Voltage	2.4			I_o = -24mA	5
V_{ol1}	Output Low Voltage		.5	V	I_o = 4mA	3
V_{ol2}	Output Low Voltage		.5	V	I_o = 8mA	4
V_{ol3}	Output Low Voltage		.5	V	I_o = 24mA	5

[1] Input leakage includes hi-Z output leakage for bidirectional buffers with tri-state outputs (MD[7:0]).

[2] Input leakage includes internal pull-up resistor (EXTARBACK#).

[3] Pouts (SEECS, ROMCS#)

[4] Outputs (MD[7:0], MA[14:0], EXTARBREQ#).

[5] Outputs (MRW).

Clock Timing

The clock waveform must be delivered to each 66 MHz PCI component in the system. In the case of add-in boards, compliance with the clock specification is measured at the add-in board component, not at the connector slot. Figure 8-1 shows the clock waveform and required measurement points for 3.3 V signaling environments. Table 8-3 summarizes the clock specifications.

3.3 Volt Clock

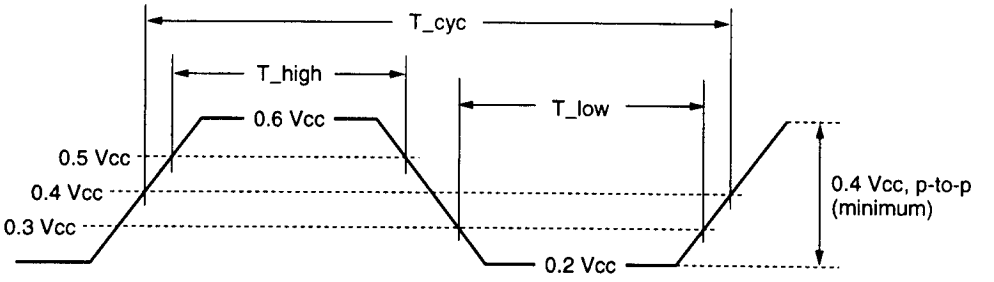


Figure 8-1. 3.3 V Clock Waveform

Table 8-3. Clock Specifications

		66 MHz		33 MHz			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
t_{cyc}	CLK Cycle Time	15	30	30	∞	ns	1, 2
t_{high}	CLK High Time	6		11		ns	
t_{low}	CLK Low Time	6		11		ns	
-	CLK Slew Rate	1.5	4	1	4	V/ns	3

[1] In general, all 66 MHz PCI components must work with any clock frequency up to 66 MHz. The clock frequency may be changed at any time during the operation of the system so long as the clock edges remain "clean", or monotonic, and the minimum cycle and high and low times are not violated. The clock may only be stopped in a low state. A variance on this specification is allowed for components designed for use on the system planar only. For clock frequencies between 33 MHz and 66 MHz, the clock frequency may not change except in conjunction with a PCI reset.

[2] The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

[3] Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 8-1.

OSCI Table

Table 8-4. PCI Clock Specification

Symbol	Parameter	Min	Max	Units	Notes
tpcyc	PCLK Cycle Time	30		ns	1
tphigh	PCLK High Time	11		ns	
tplow	PCLK Low Time	11		ns	
	PCLK Slew Rate	1	4	V/ns	2
tscyc	SCLK Cycle Time	25		ns	1
tshigh	SCLK High Time	7		ns	
tslow	SCLK Low Time	8		ns	
	SCLK Slew Rate		3	V/ns	

PCI Timing

Timing Parameters

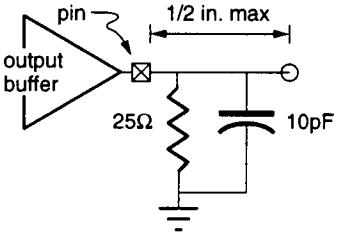
The following table provides the timing parameters for 5 V and 3.3 V signaling environments.

Table 8-5. 5 V and 3.3 V Timing Parameters

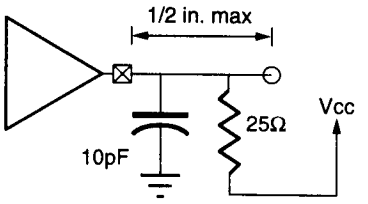
Symbol	Parameter	Min	Max	Units	Notes
^{t}val	CLK to Signal Valid Delay—bused signals	2	11	ns	1, 2
$t_{val(ptp)}$	CLK to Signal Valid Delay—point to point	2	12	ns	1, 2
t_{on}	Float to Active Delay	2		ns	5
t_{off}	Active to Float Delay		28	ns	5
t_{su}	Input Set up Time to CLK—bused signals	7		ns	2
$t_{su(ptp)}$	Input Set up Time to CLK—point to point	10, 12		ns	2
t_{h}	Input Hold Time from CLK	0		ns	
t_{rst}	Reset Active Time After Power Stable	1		ms	3
$t_{rst-clk}$	Reset Active Time After CLK Stable	100		µs	3
$t_{rst-off}$	Reset Active to Output Float Delay		40	ns	3, 4, 5
t_{rrsu}	REQ64# to RST# Setup Time	$10*T_{cyc}$		ns	
T_{rrh}	RST# to REQ63# Hold Time	0	50	ns	

[1] For parts compliant to the 5 V signaling environment:
Minimum times are evaluated with 0 pF equivalent load; maximum times are evaluated with 50 pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications. Note that faster buffers may exhibit some ring back when attached to a 50 pF lump load, which should be of no consequence as long as the output buffers are in full compliance with slew rate and V/I curve specifications.
For parts compliant to the 3.3 V signaling environment:
Minimum times are evaluated with same load used for slew rate measurement; maximum times are evaluated with the following load circuits, for high-going and low-going edges respectively.

Tval(max) Rising Edge



Tval(max) Falling Edge



[2] REQ# and GNT# are point-to-point signals, and have different output valid delay and input set-up times than do bused signals. GNT# has a setup of 10; REQ# has a setup of 12. All other signals are bused.

[3] RST# is asserted and deasserted asynchronously with respect to CLK.

[4] All output drivers must be asynchronously floated when RST# is active.

[5] For purposes of Active/Float timing measurements, the hi-Z or *off* state occurs when the total current delivered through the component pin is less than or equal to the leakage current specification.

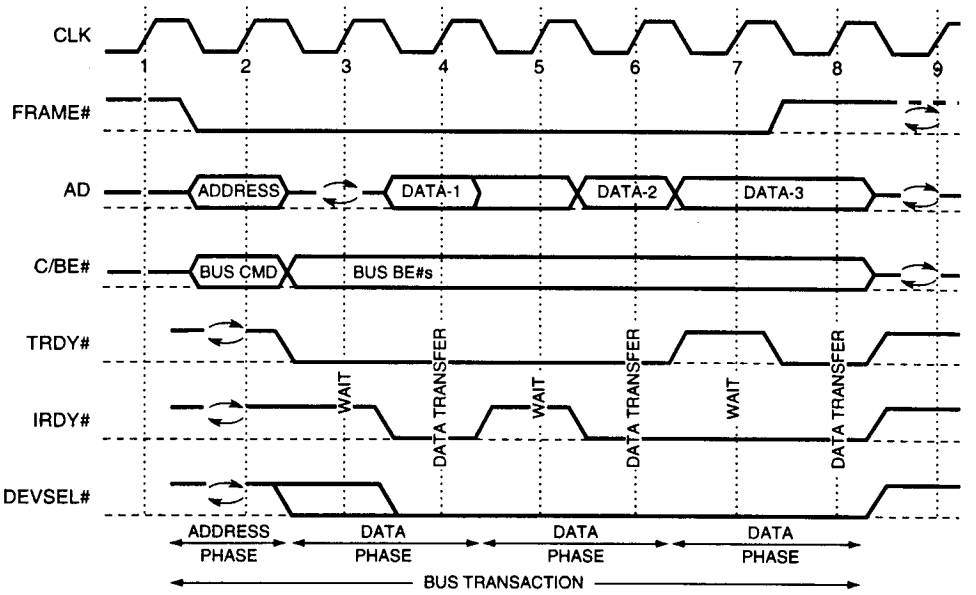


Figure 8-2. Basic Read Operation

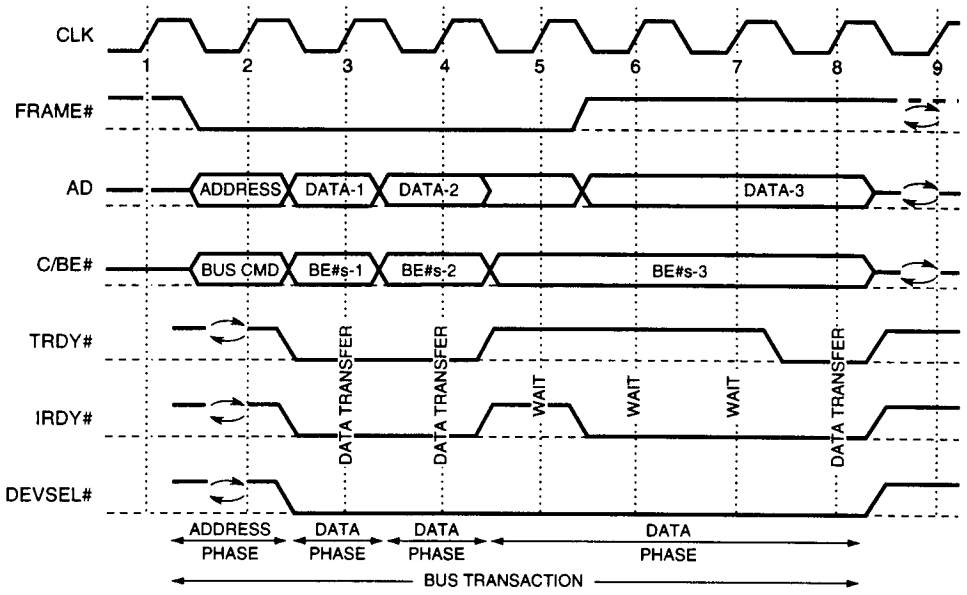


Figure 8-3. Basic Write Operation

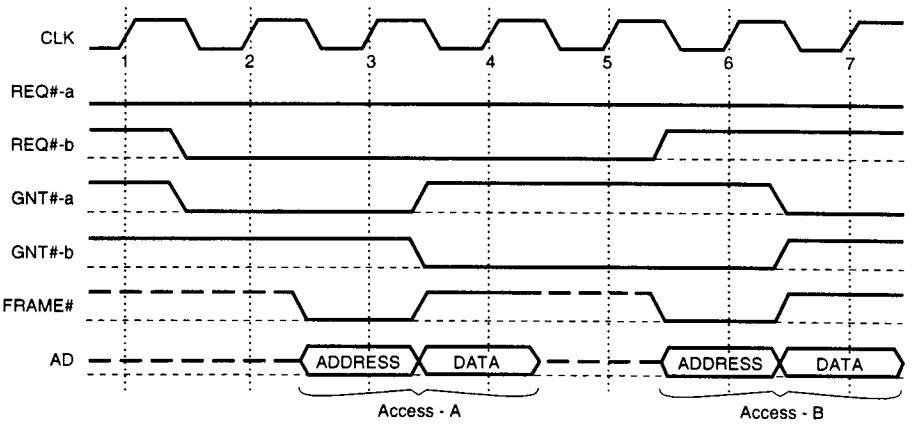


Figure 8-4. Basic Arbitration

Wave Forms

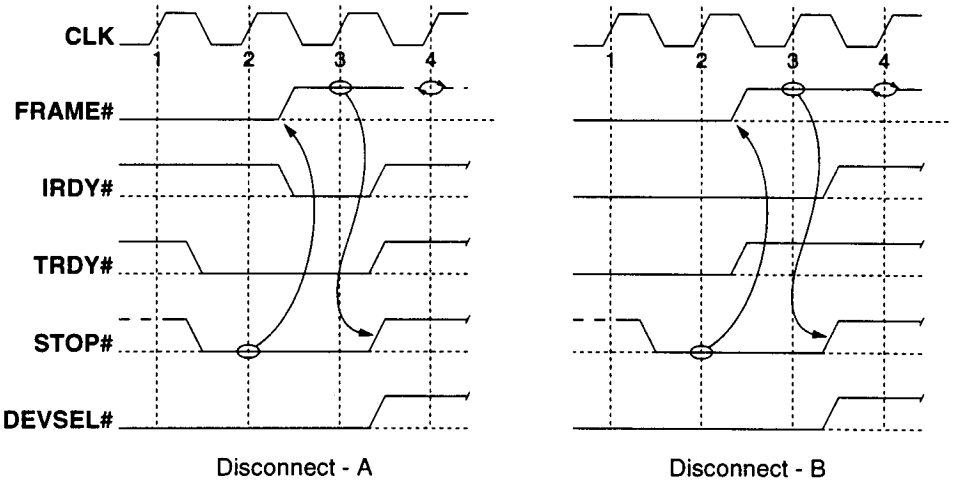


Figure 8-5. Disconnect with Data

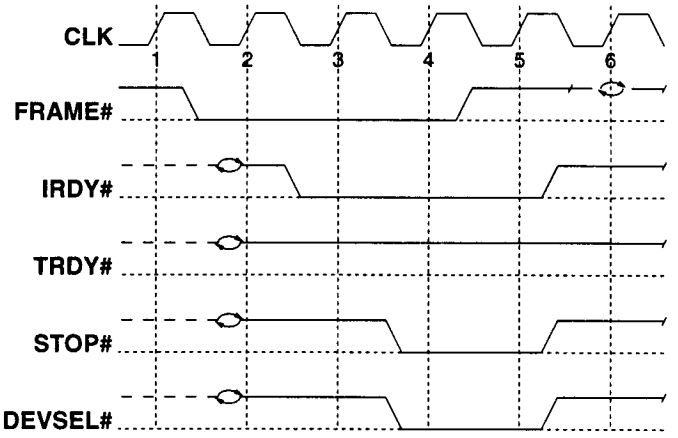


Figure 8-6. Retry

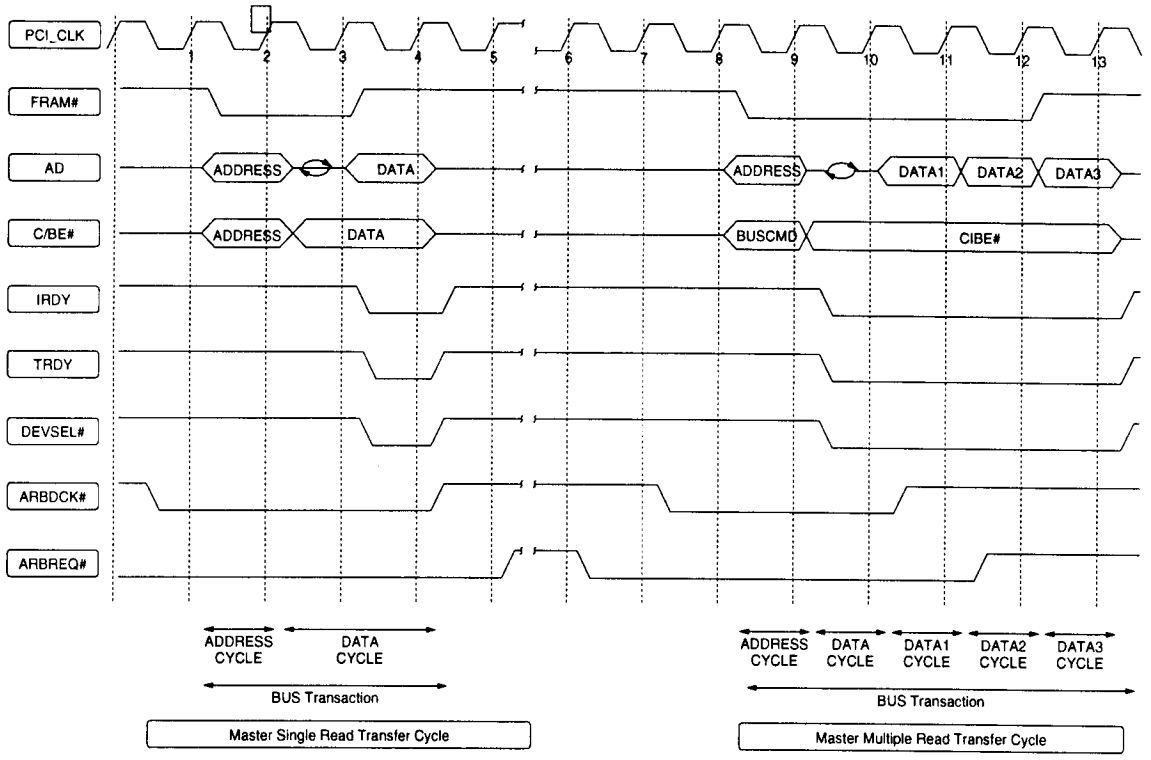


Figure 8-7. Master Read Transfer Cycle

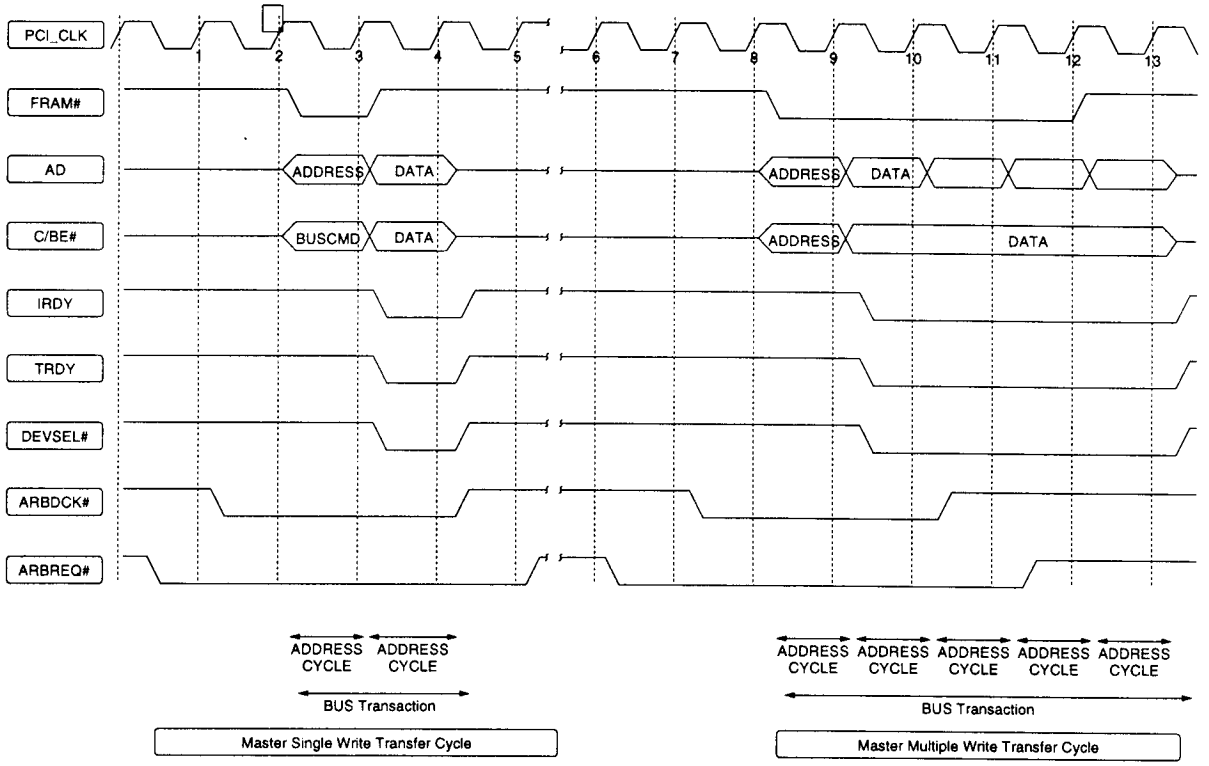


Figure 8-8. Master Write Transfer Cycle

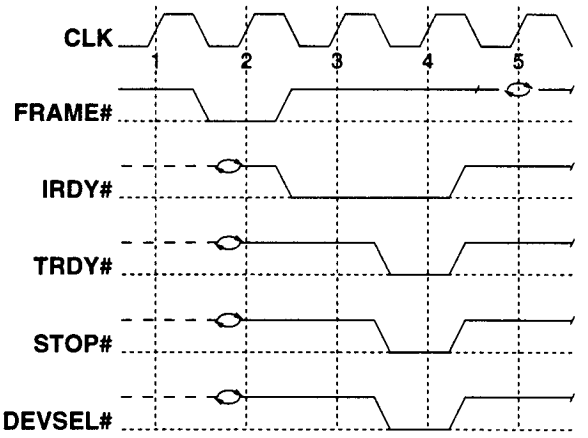


Figure 8-9. Master Completion Termination

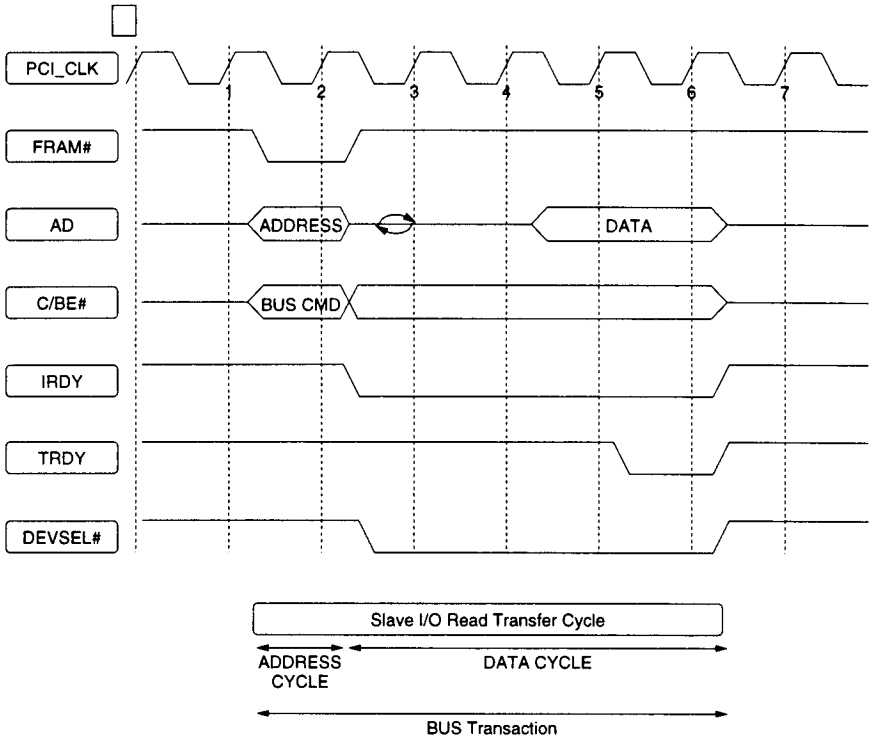


Figure 8-10. Slave I/O Read Transfer Cycle

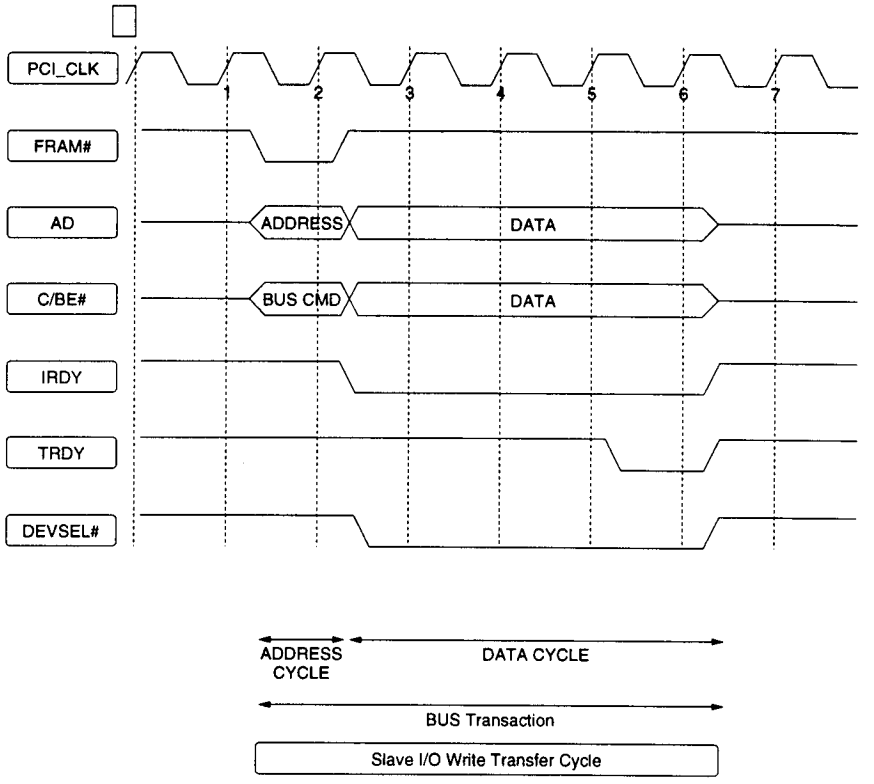


Figure 8-11. Slave I/O Write Transfer Cycle

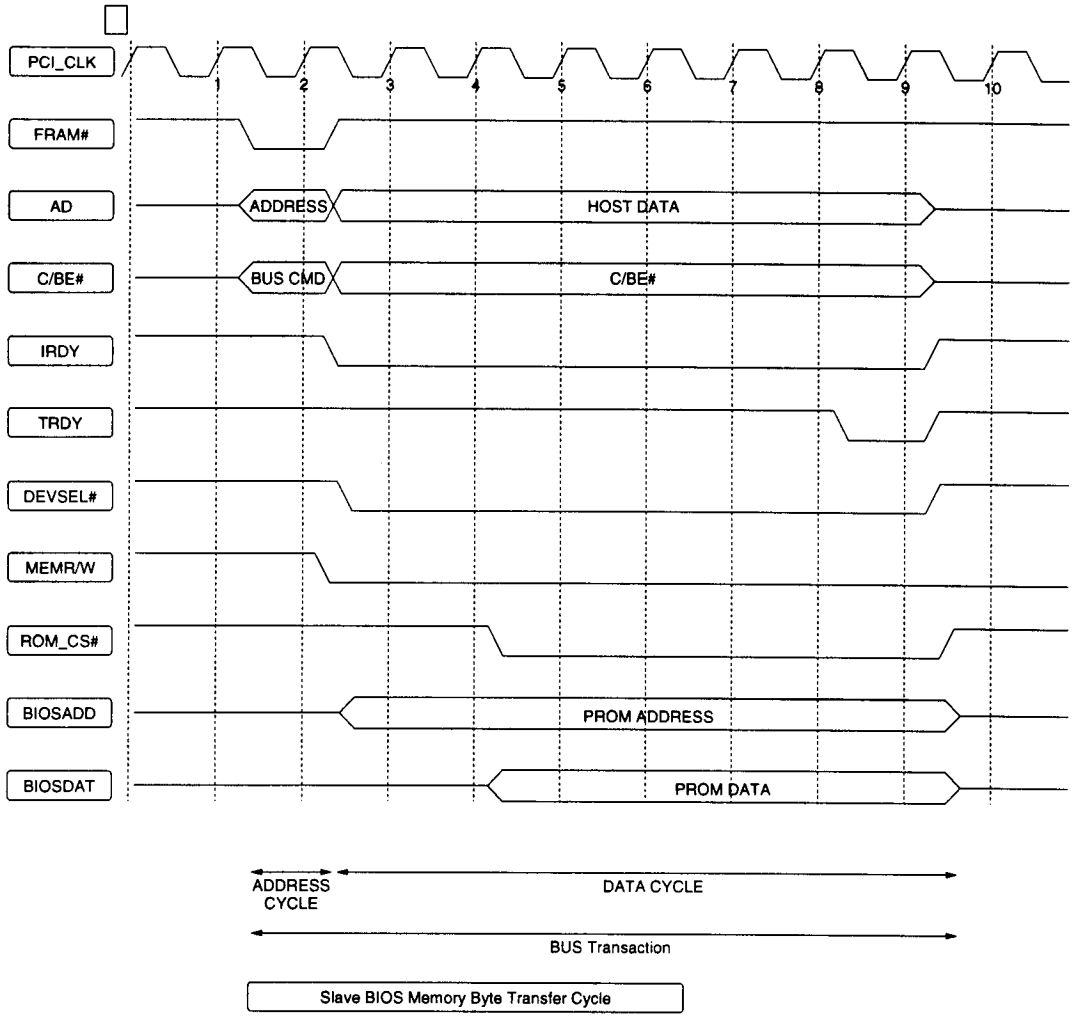


Figure 8-12. Slave BIOS Memory Byte Transfer Cycle

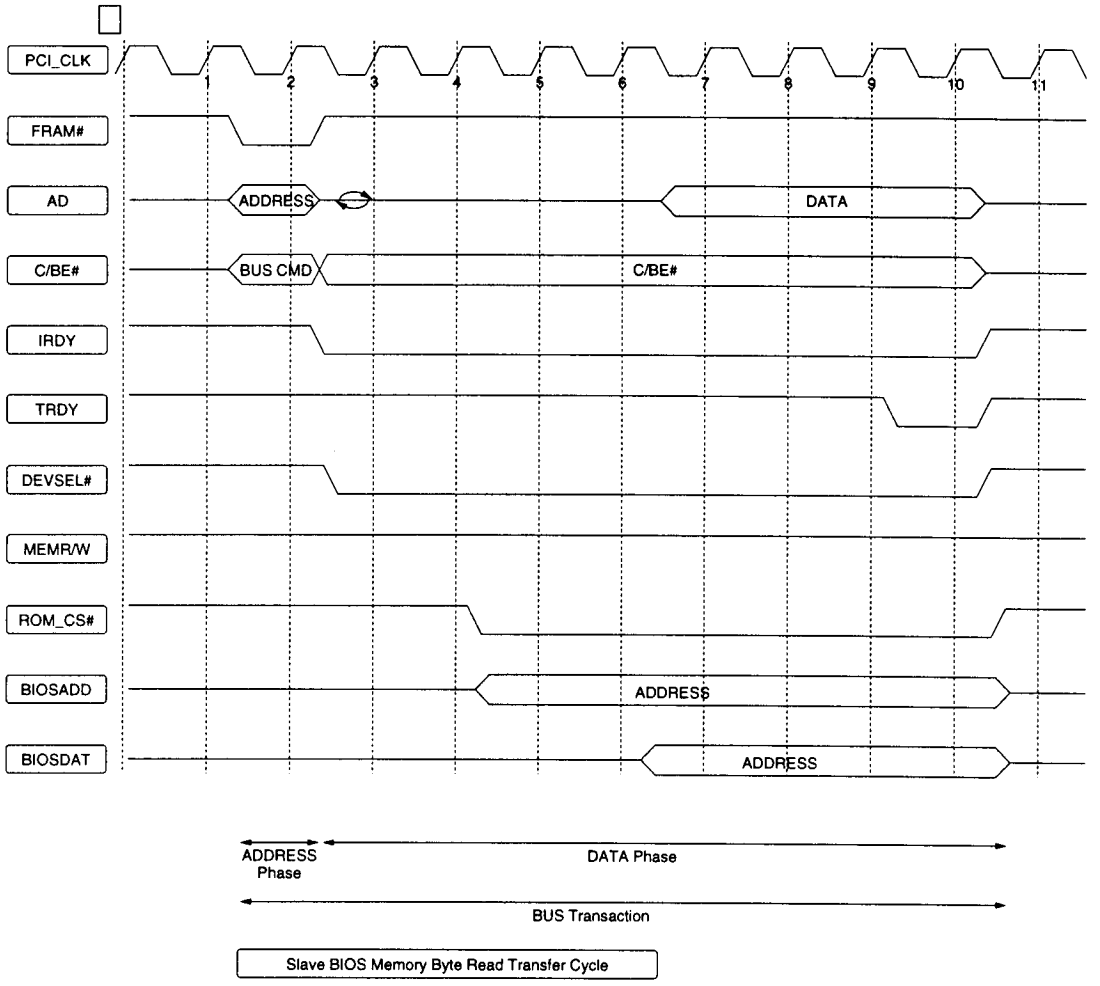


Figure 8-13. Slave BIOS Memory Byte Read Transfer Cycle

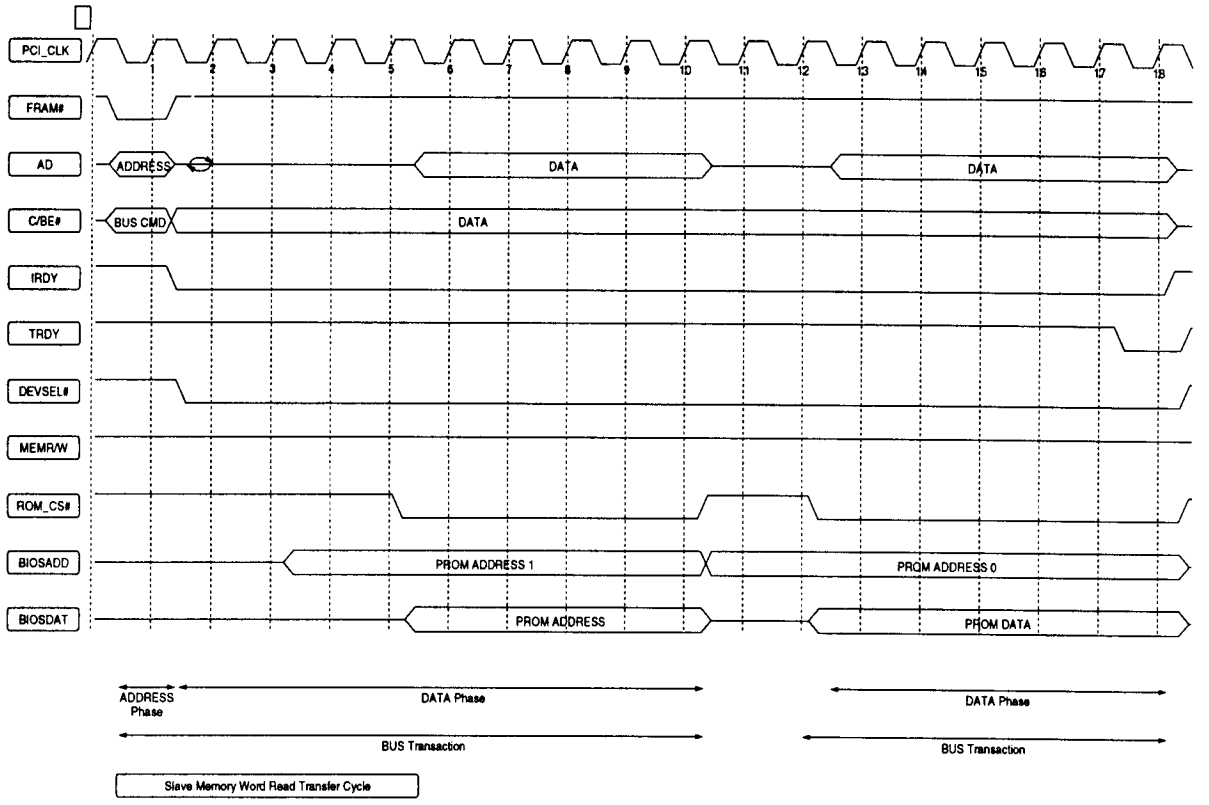


Figure 8-14. Slave Memory Word Read Transfer Cycle

A

Package Description

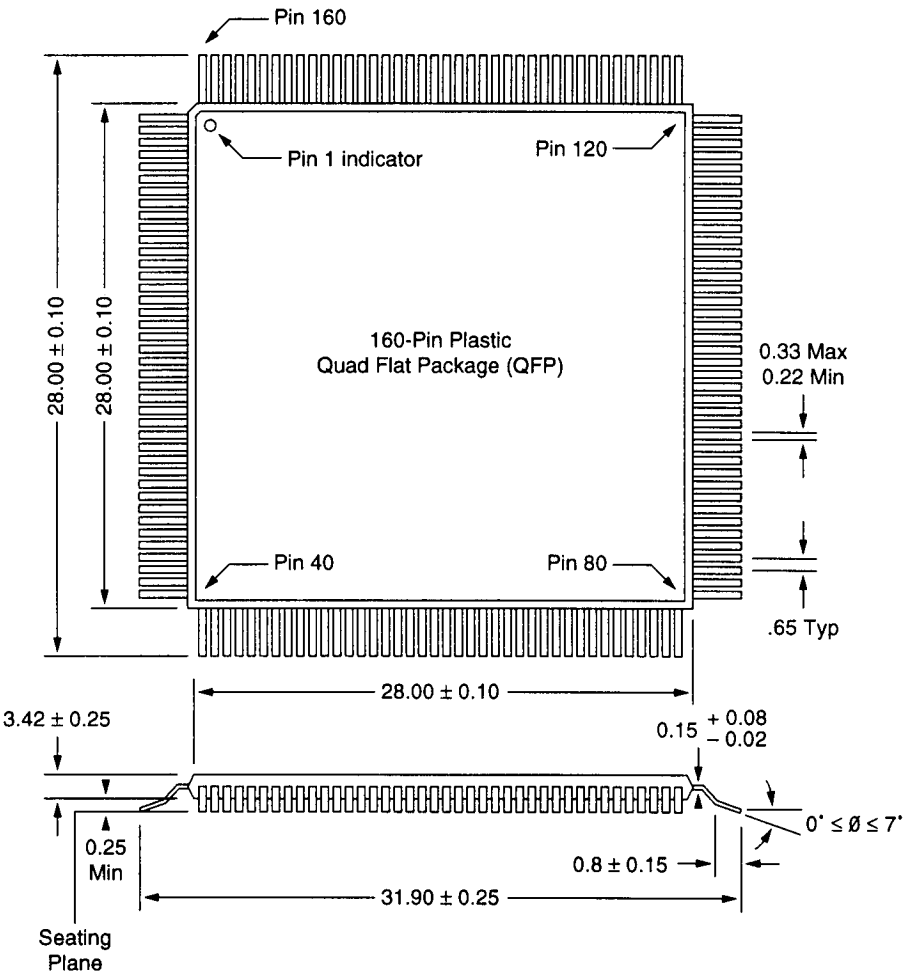


Figure A-1. BA-81C15 Package Description

Glossary

ExtCPU: External CPU or system host.

PCI: Peripheral Component Interconnect

SCSI: Small Computer System Interface. An industry standard for connecting peripheral devices and their controllers to a microprocessor.

HOST FIFO: A set of four 32x8 bit FIFOs used to buffer data transfers to or from the PCI bus and the SCSI block.

SCSI FIFO: A set of two 16x9 bits FIFOs used to buffer data transfers to or from the SCSI bus and the PCI controller. There are read and write channels to the SCSI FIFO. The write channel is the only path for data to flow into the FIFO, while the read channel is the only path for data to flow out of the FIFO. The three FIFO ports feed either the read or the write channel control of the two channels, but each FIFO port can only control *one* of the two channels at a time.

SCSI Port: Highest priority FIFO port, connected to SCSI bus interface. The SCSI bus can also be read and written to from the register file.

DMA Port: Second priority FIFO port, connected to DMA PCI Interface.

Host Port: Lowest priority FIFO port, connected to FIFO Data Register.

DMA Channel: An 8-bit I/O path between the PCI block and the SCSI block. The DMA has only one supported mode, high-speed 40 MB operation. DMA REQ is asserted by the SCSI block and held as long as the SCSI block is ready. The PCI block asserts DMA ACK and holds it as long as it is ready. One byte is transferred on every OSCI clock as long as both the DMA REQ and DMA ACK are asserted.

LastByte: The last byte is being transferred so that BA-81C15 will not assert ACK in response to assertion of REQ.

Arbitration ID: The SCSI ID of the BA-81C15 used as the Self ID during arbitration and selection.

Wait for Self ID: The SCSI ID of the BA-81C15 used to match the SCSI bus while waiting for re-selection. When multiple bits are set, the BA-81C15 will respond to being re-selected if the SCSI bus ID matches any of the bits—as long as the chip is enabled to respond. This part can respond to more than one SCSI ID.

Selected ID: Stores the encoded Device ID of the other device which was selected or device which re-selected the BA-81C15.

Select ID: The encoded SCSI Device ID which the BA-81C15 is trying to select.

Current ID: The encoded ID which is stored when connecting to the SCSI bus when being re-selected by another device. This is very useful when using the Multiple Self ID. This determines which ID the BA-81C15 is now.

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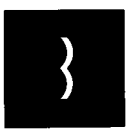

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