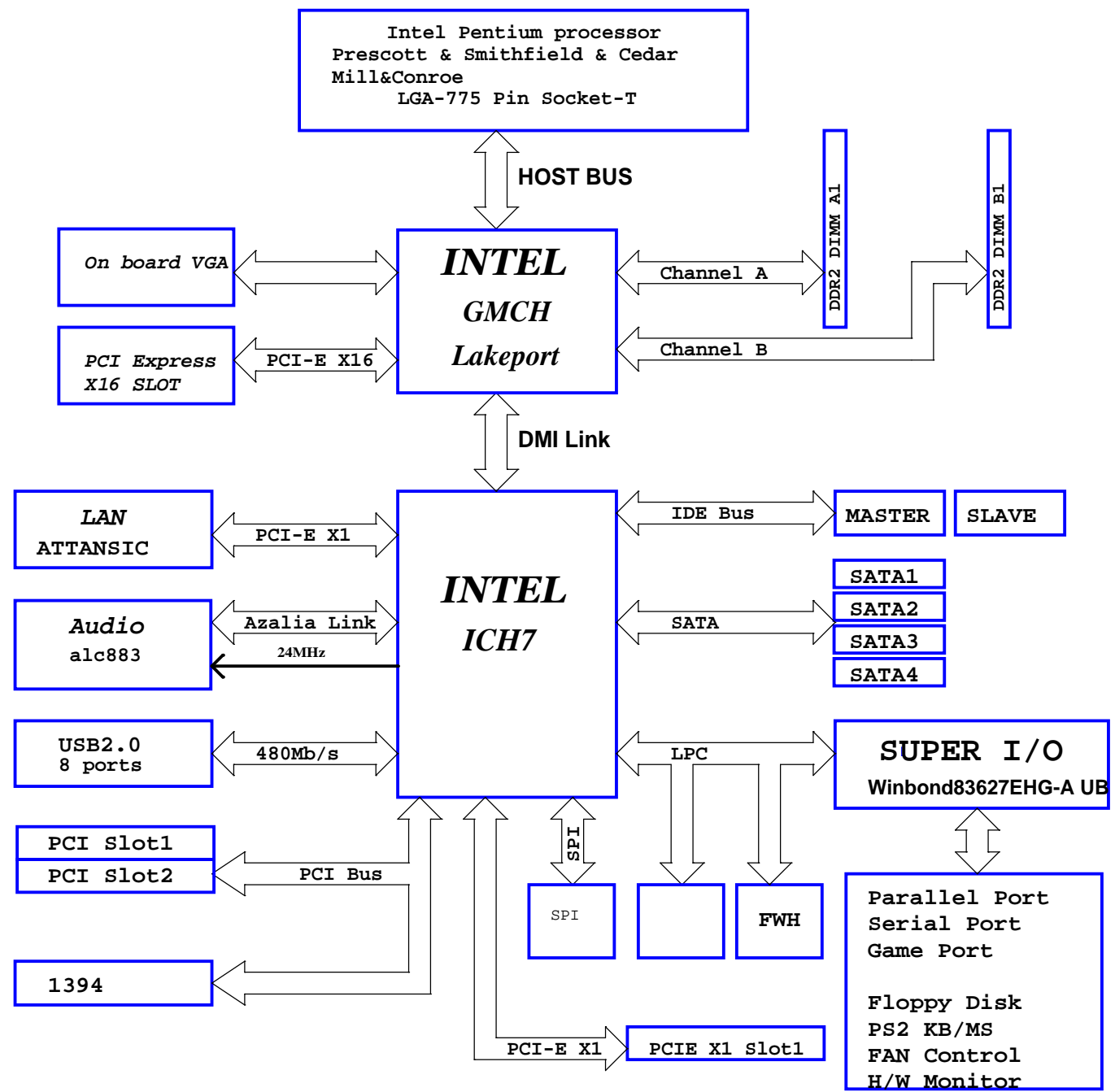
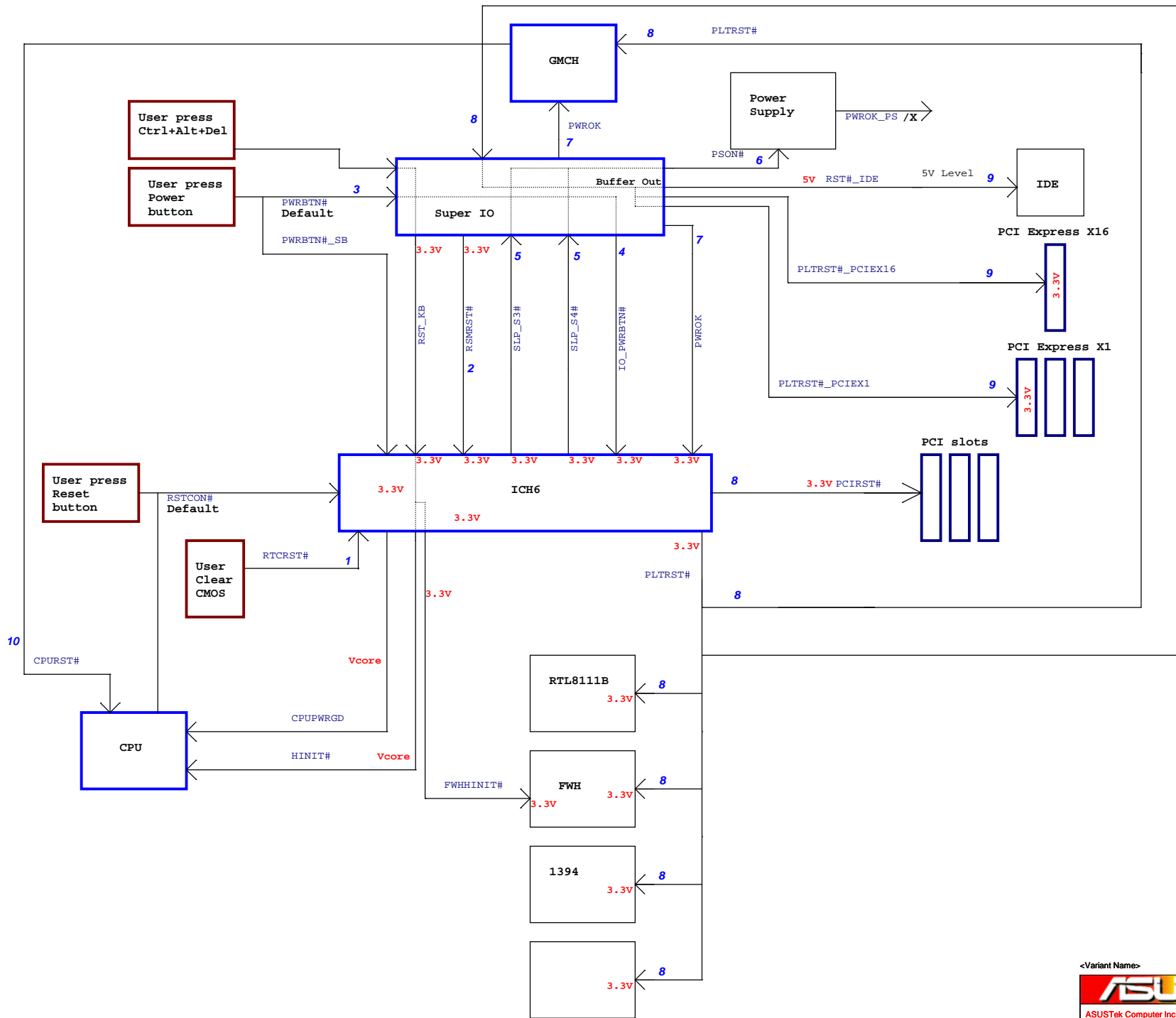



P5GC-MX

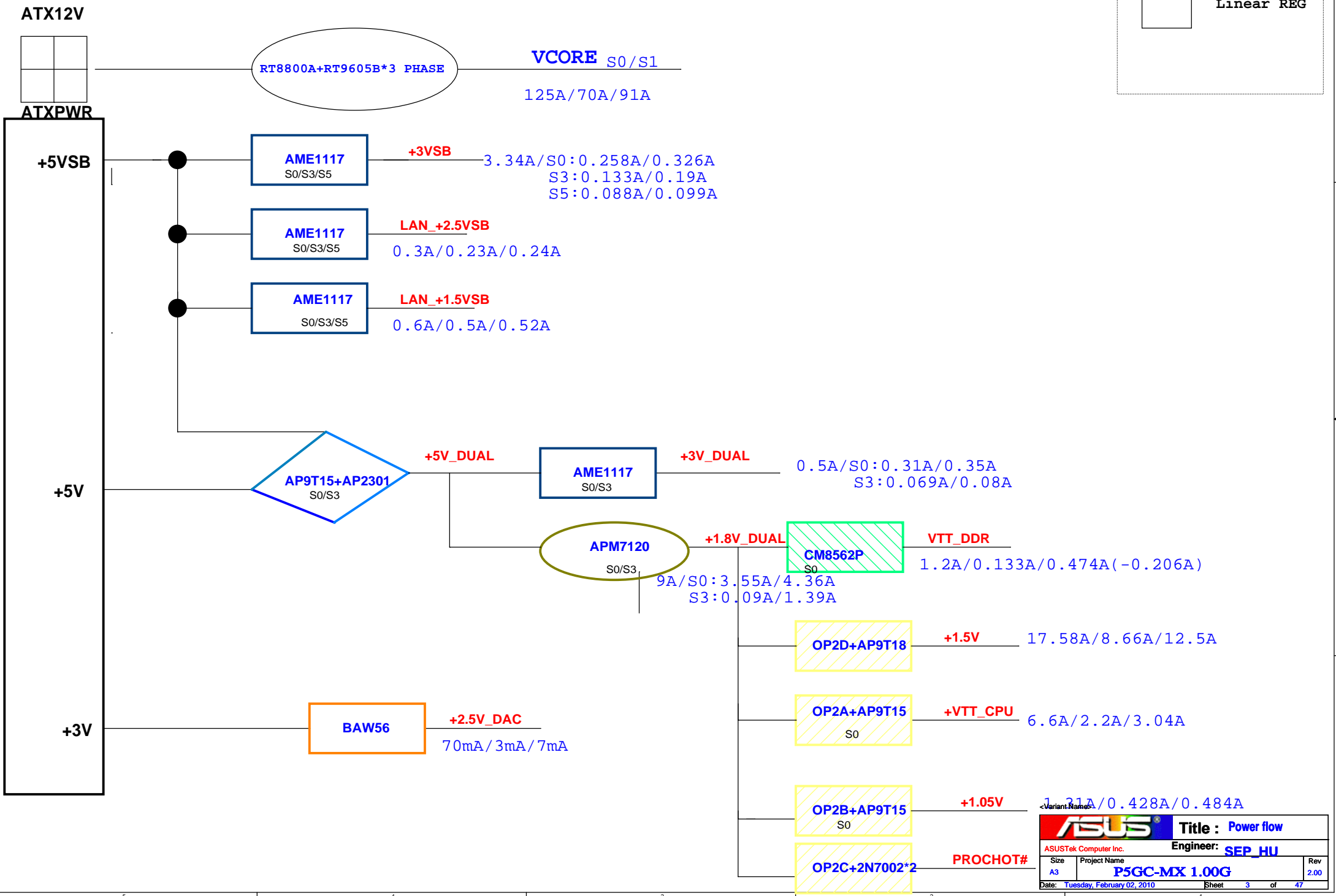
Revision:1.00G




01	Block Diagram
02	Power Sequence
03	Power Flow
04	Clock Distribution
05	Clock
06	Clock Trap
07	LGA775-1
08	LGA775-2
09	LGA775-3
10	LGA775-4
11	LGA775-5
12	Lakeport-1
13	Lakeport-2
14	Lakeport-3
15	Lakeport-4
16	Lakeport-5
17	DDR2-CHA Control
18	DDR2-CHA Power
19	DDR2-CHB Control
20	DDR2-CHB Power
21	PCI Express X16
22	Onboard VGA
23	ICH7-1
24	ICH7-2
25	ICH7-3
26	ICH7-4
27	PCI Express X1
28	PCI
29	IDE and SATA
30	SPI
31	KB/MS/GAME
32	LPT & COM & FDD
33	USB
34	FAN Control & H/W Mointor
35	Super IO
36	AUDIO 1986A
37	AUDIO-1
38	Front Panel
39	FWH
40	1394
41	LAN(ATTANSIC)
42	1.8v_dual&vtt_ddr&5v_dual&lan
43	+3v_dual&+3vsb&
44	Vcore Controller
45	Vcore Driver
46	VTT_CPU
47	+1.5v



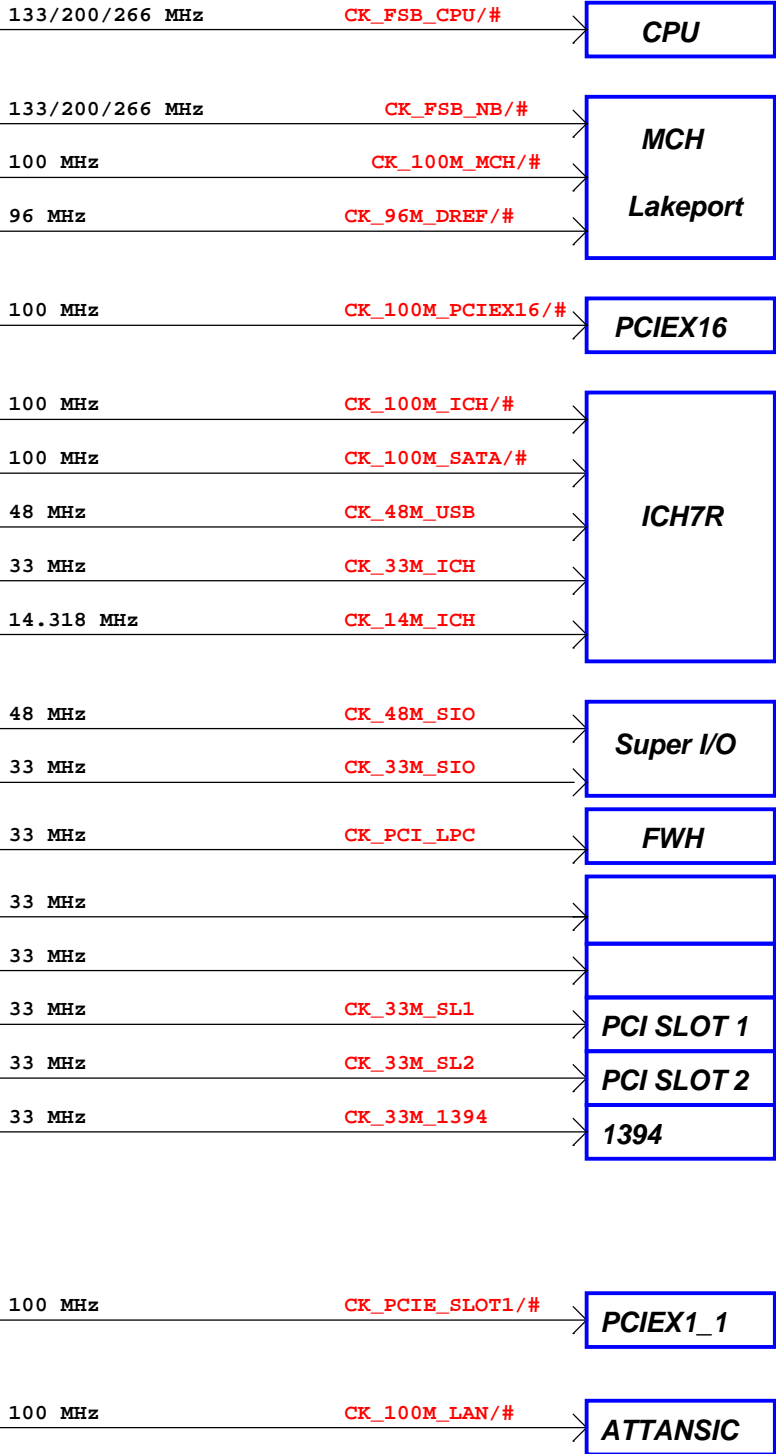
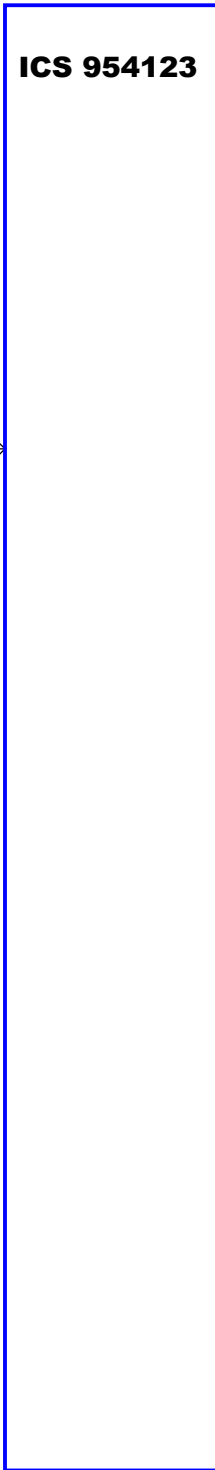
NOTE:
 Linear REG

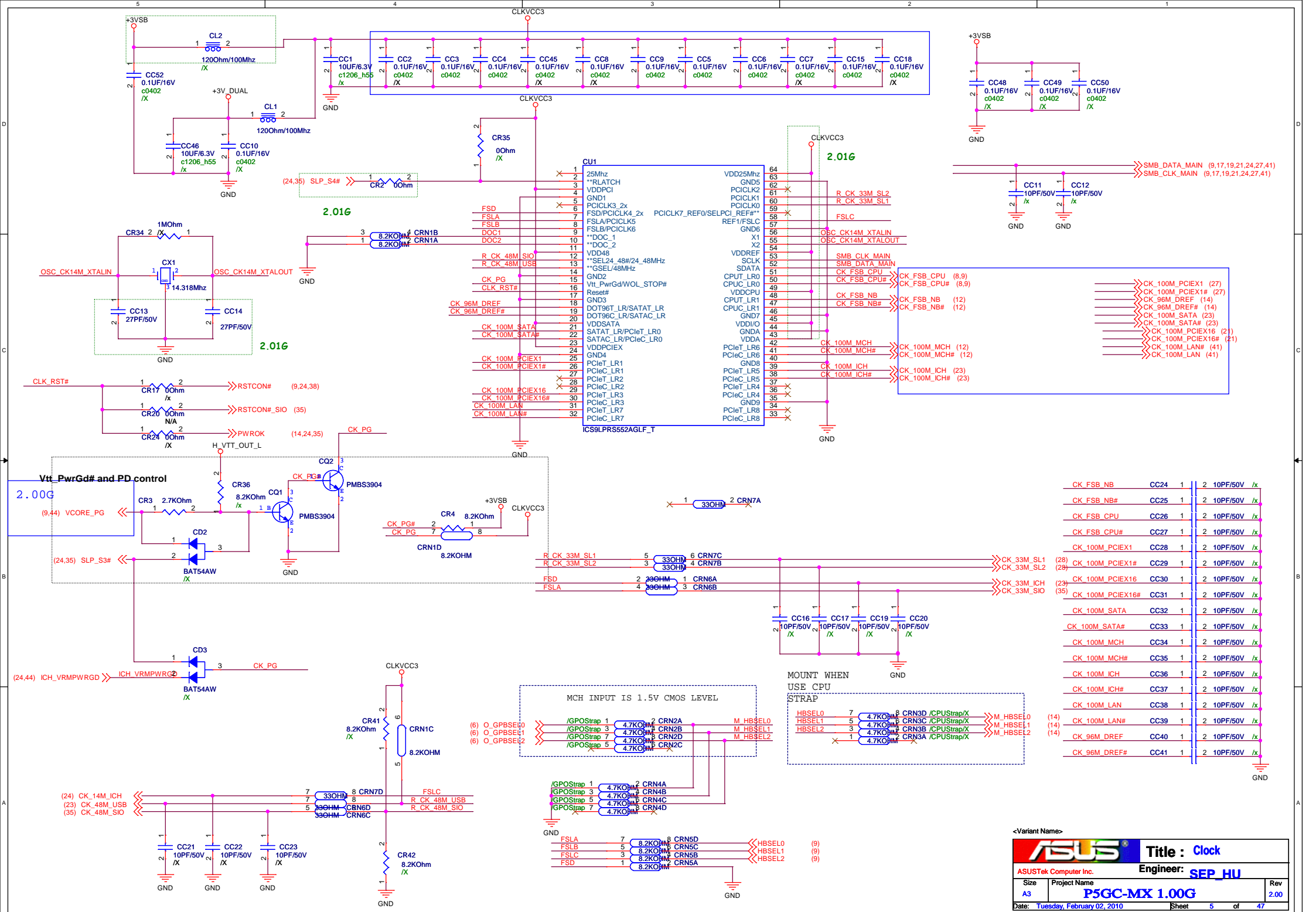


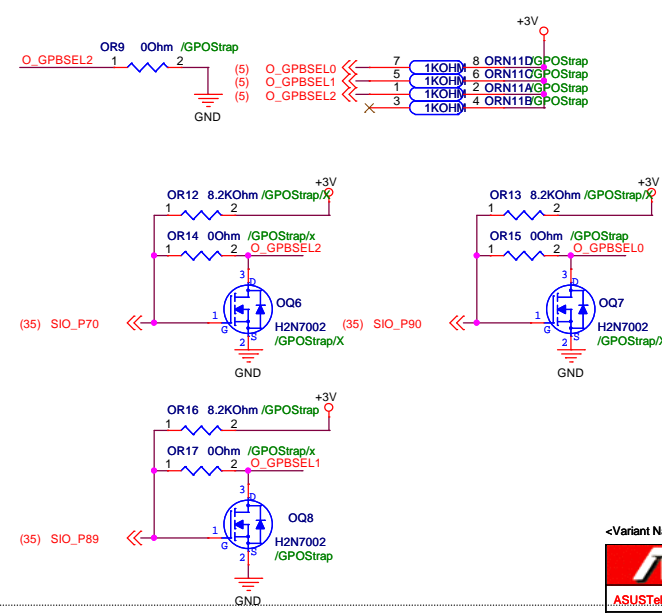
		Title : Power flow	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010		Sheet	3 of 47

XTAL

14.318 MHz

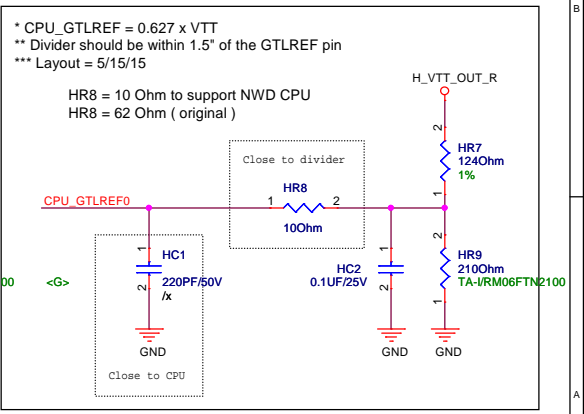
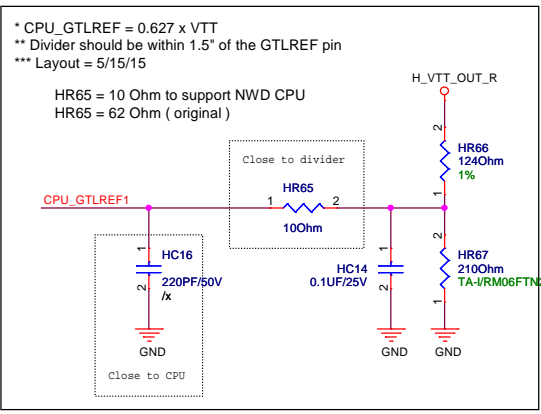
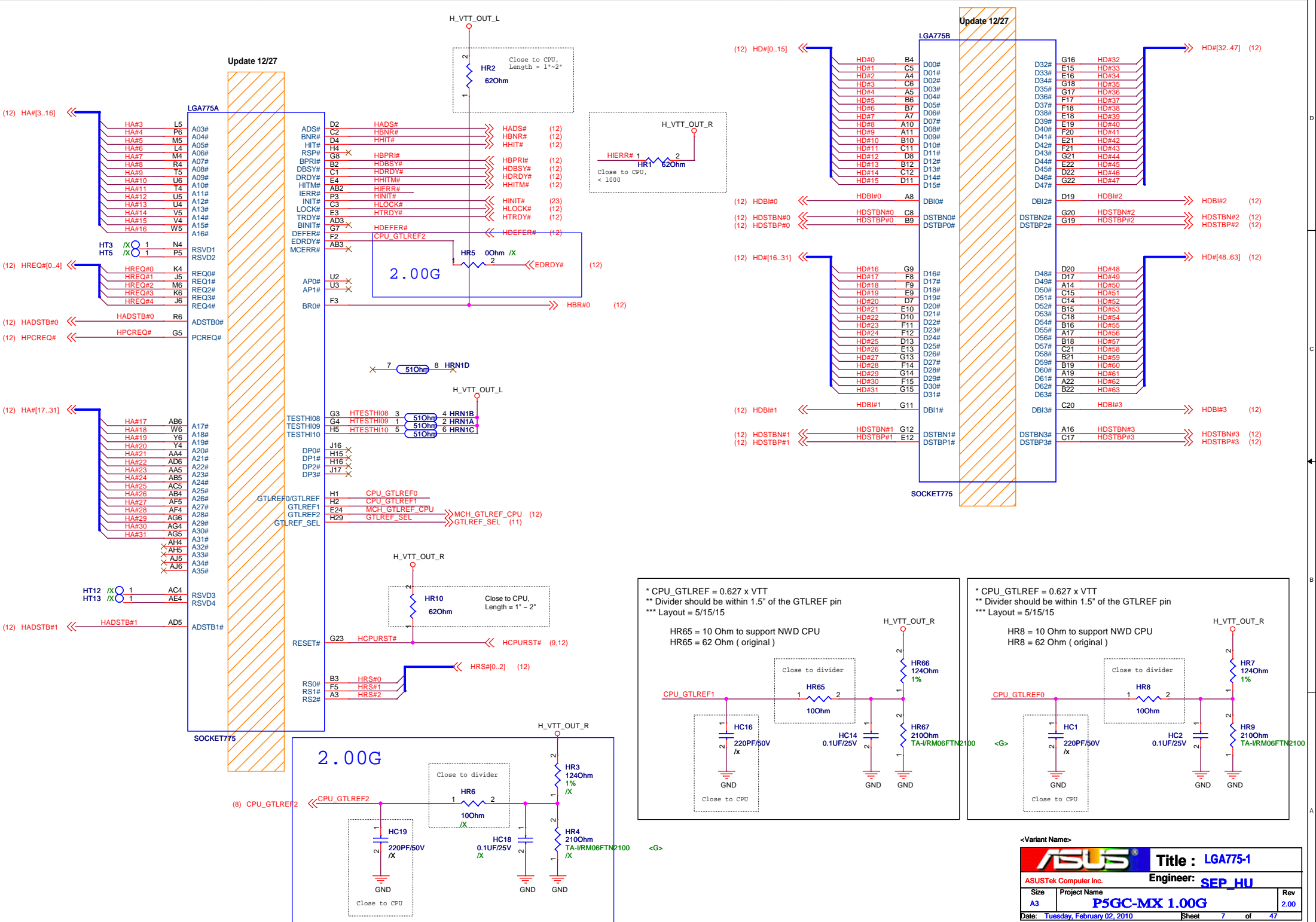






<Variant Name>

ASUS		Title : Clock	
ASUSTek Computer, Inc.		Engineer: SEP_HU	
Size	Project Name		Rev
A3	P5GC-MX 1.00G		2.00
Date: Tuesday, February 02, 2010		Sheet	6 of 47



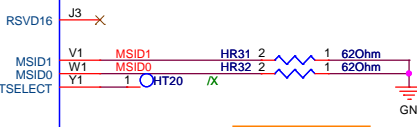
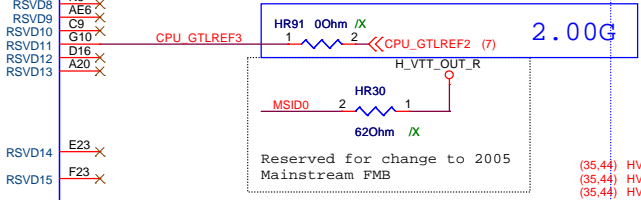
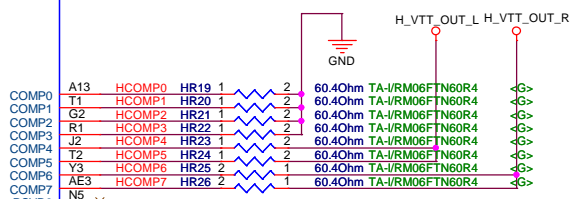
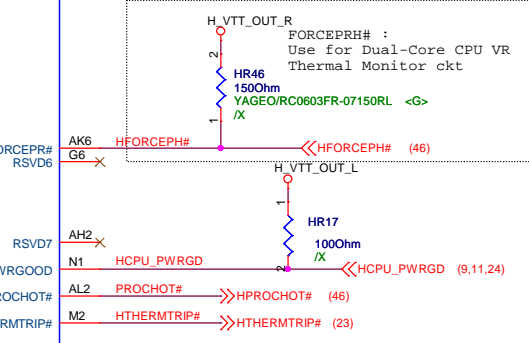
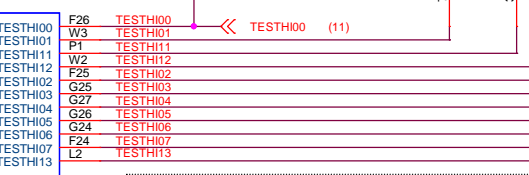
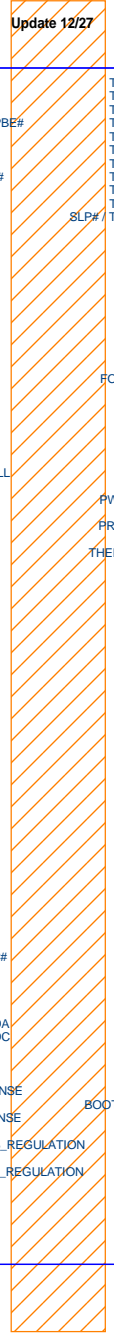
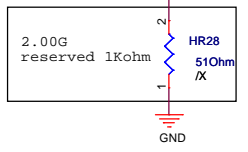
In 915/925 series use:
09-022104300
INDUCTOR 10UH/100mA
(0805)

- (23) HSMI#
- (23) HA20M#
- (23) HFERR#
- (23) HINTR
- (23) HNMI
- (23) HIGNNE#
- (23) HSTPCLK#

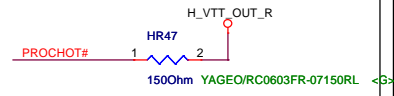
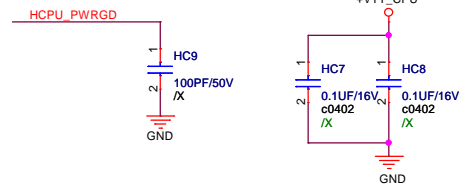
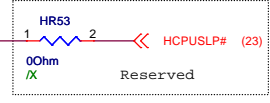
Inductor 10UH (0805) EL CAP 33UF/25V
TOL: +/-20% 6.3x7
SRF: >30 MHz TOL: +/-20%
I rated: > 120 mA ESL: < 9nH
DCR: < 0.36 Ohm ESR: < 0.3 Ohm

2.00G
CHVID0 AM2 VID0
CHVID1 AL5 VID1
CHVID2 AM3 VID2
CHVID3 AL6 VID3
CHVID4 AK4 VID4
CHVID5 AL4 VID5
CHVID6 AM5 VID6

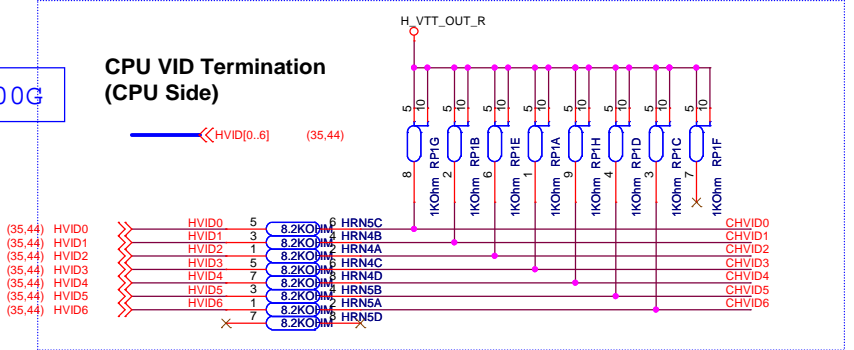
Reserved !!
Intel CRB is NC
and add TP only



Reserved !!
Intel CRB
is NC and
add TP
only



CPU VID Termination (CPU Side)



	2005 Performance FMB	2005 Mainstream FMB
MSID1	62 ohm PD	62 ohm PD
MSID0	62 ohm PD	62 ohm PU to VTT

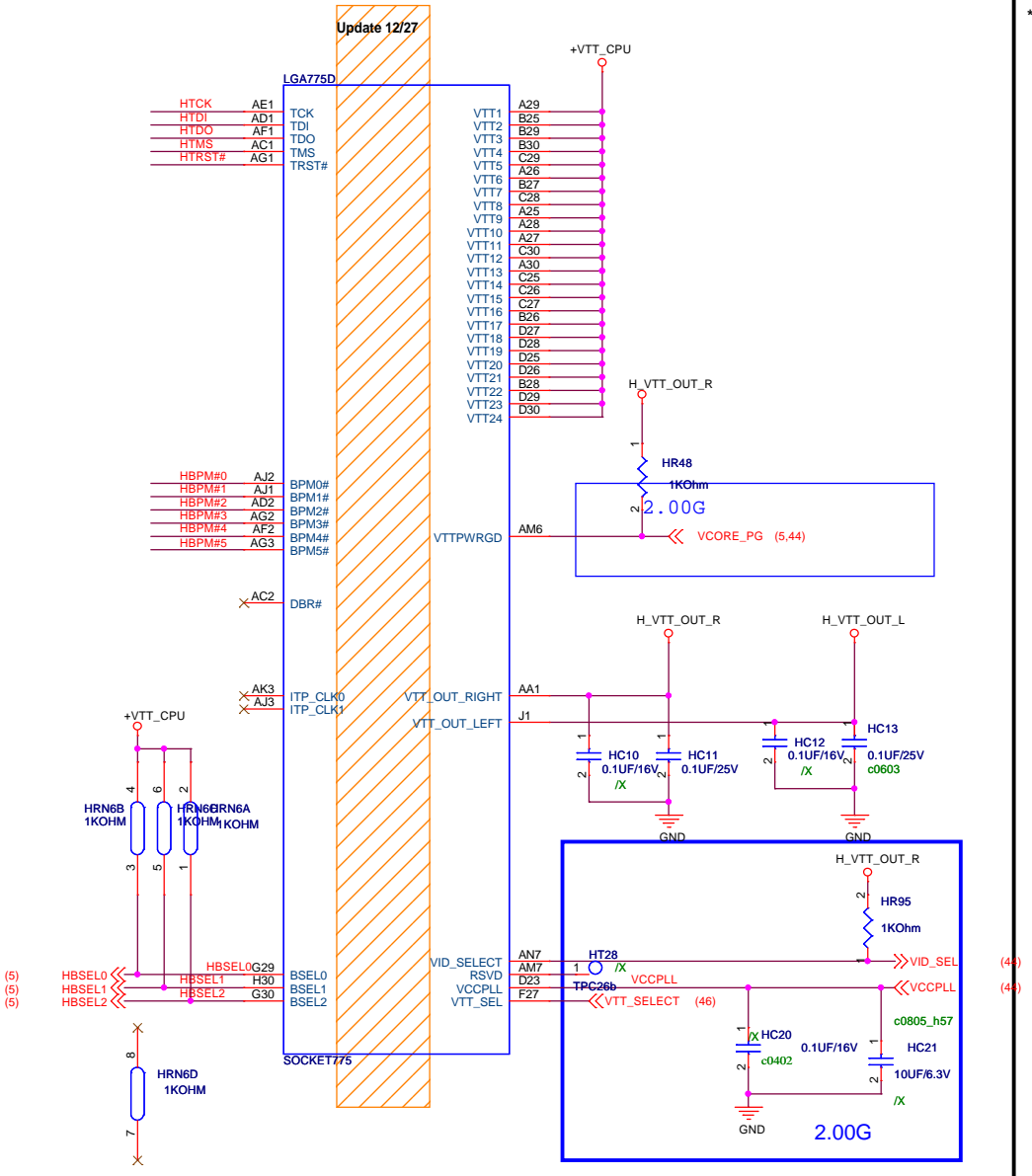
<Variant Name>

ASUS Title : LGA775-2
ASUSTek Computer Inc. Engineer: SEP_HU

Size	Project Name	Rev
A3	P5GC-MX 1.00G	2.00

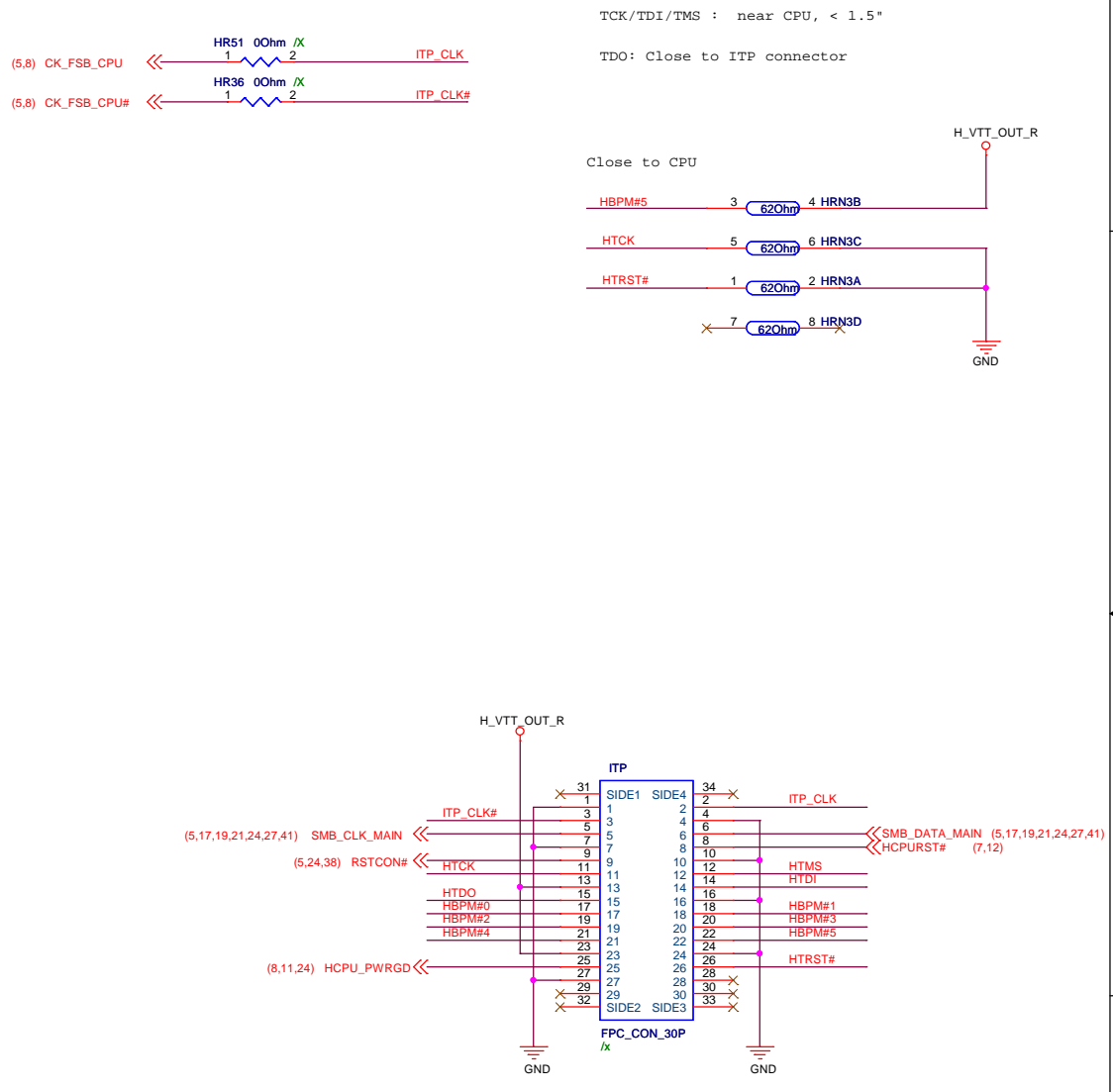
Date: Tuesday, February 02, 2010 Sheet 8 of 47

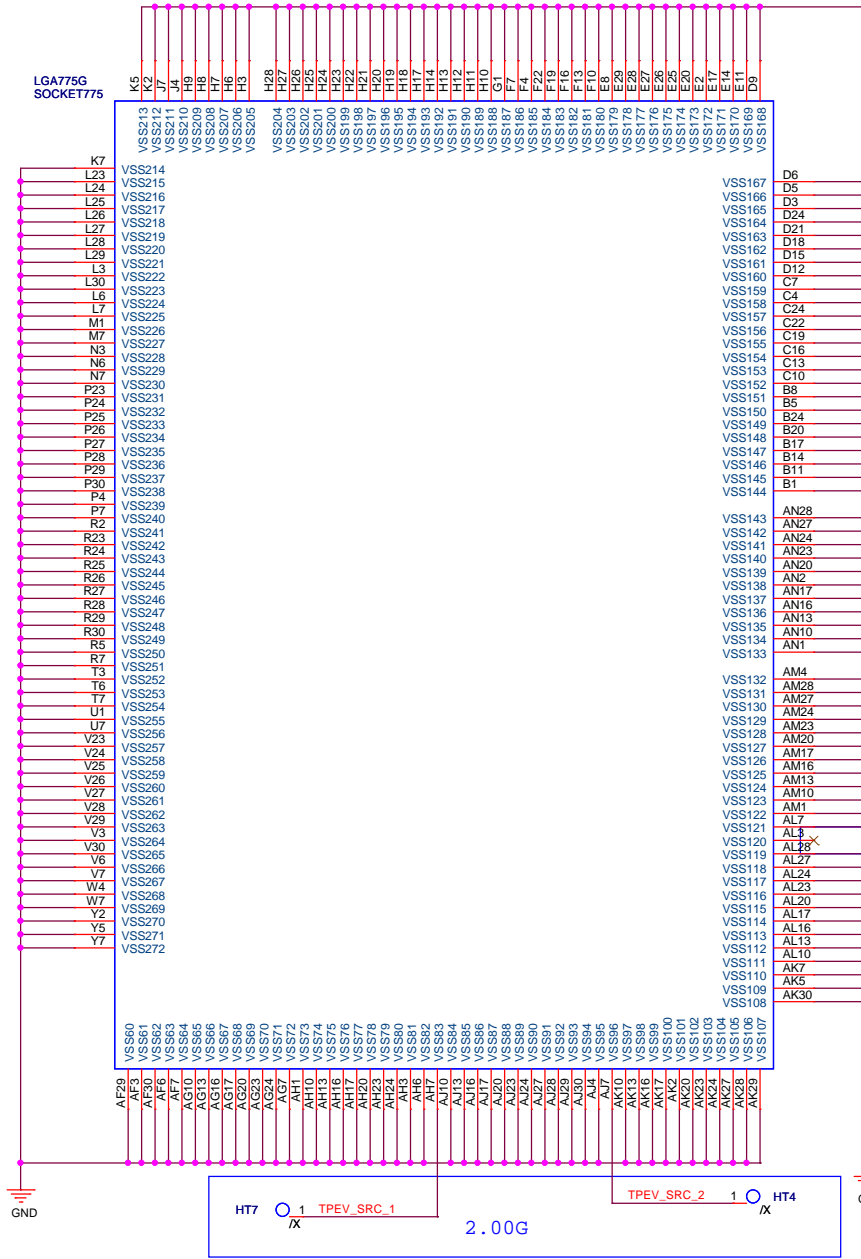
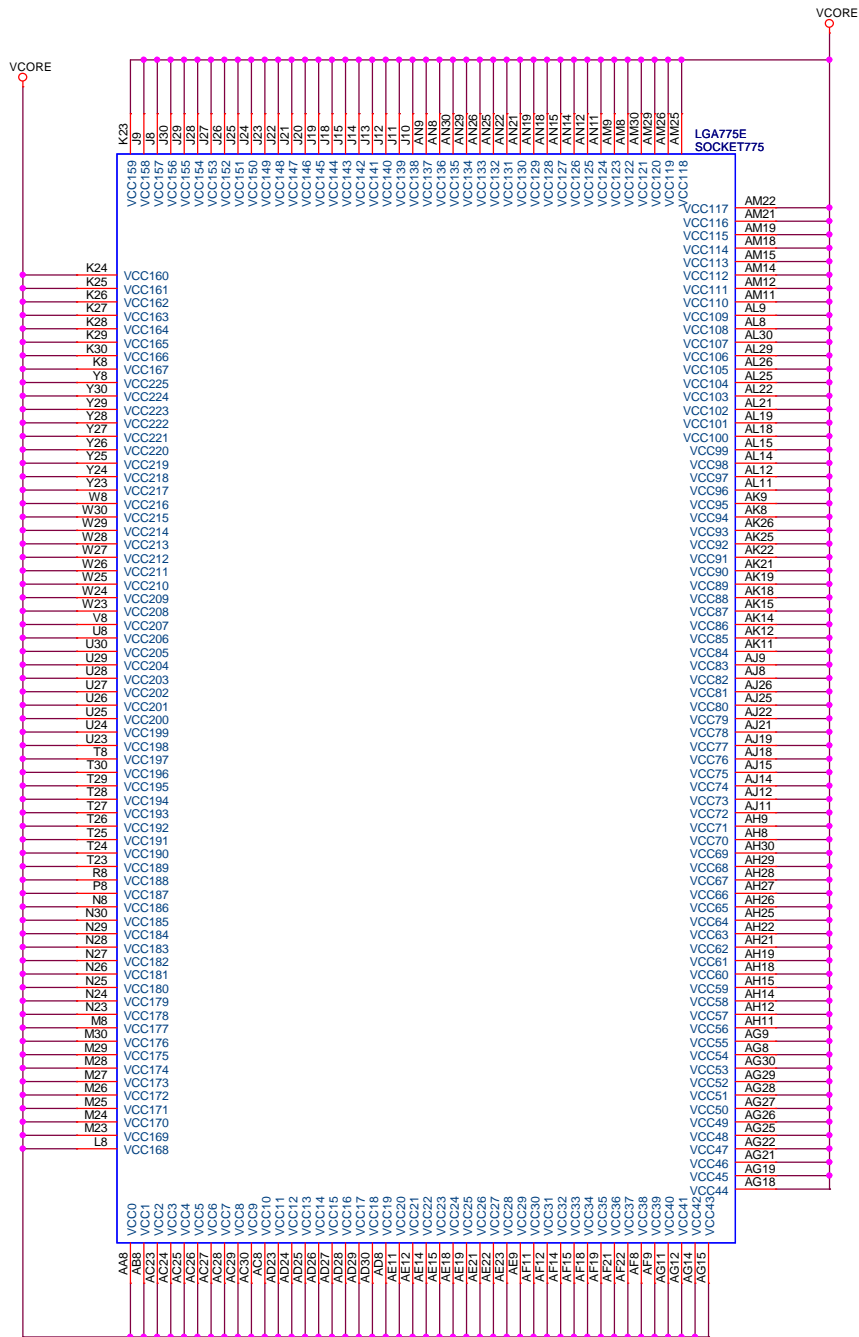
Update 12/27



ITP

* All ITP related resistor can be placed in back side except RN16(TCK and TRST) and BPM5#
 ** The resistors of HTCK(HR48), HTRST#(HR47), and HBPM5#(HR71) must be mounted.





2.00G

<Variant Names>

ASUS		Title : LGA775-4
ASUSTek Computer Inc.		Engineer: SEP_HU
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00
Date: Tuesday, February 02, 2010		Sheet 10 of 47

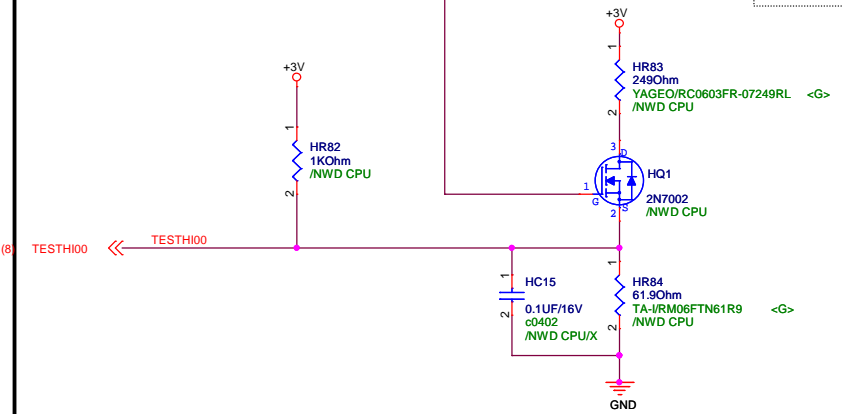
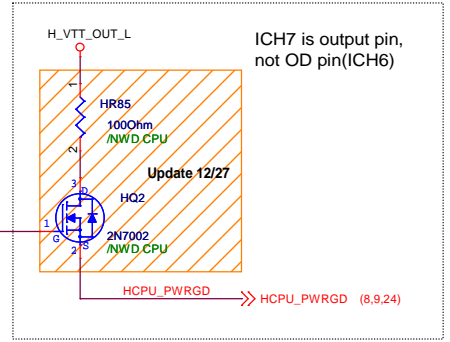
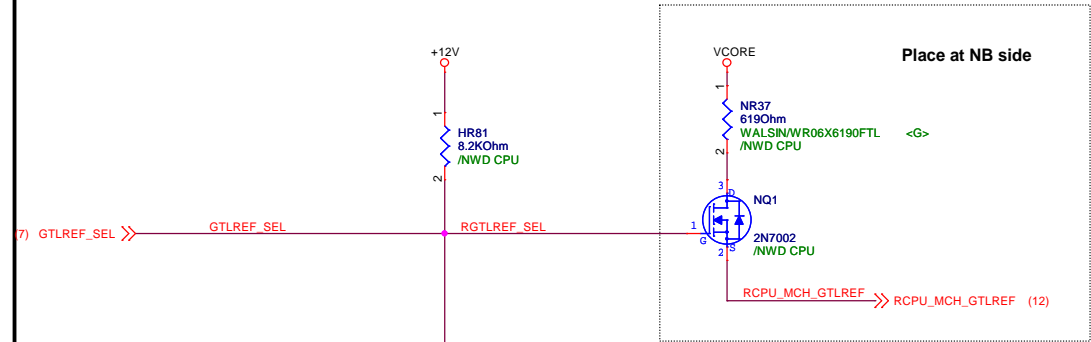
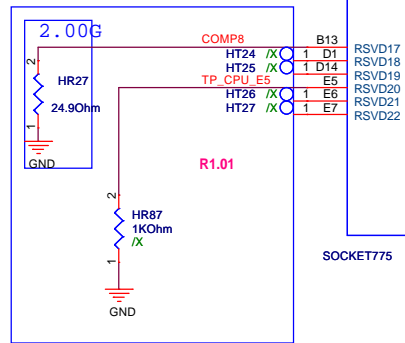
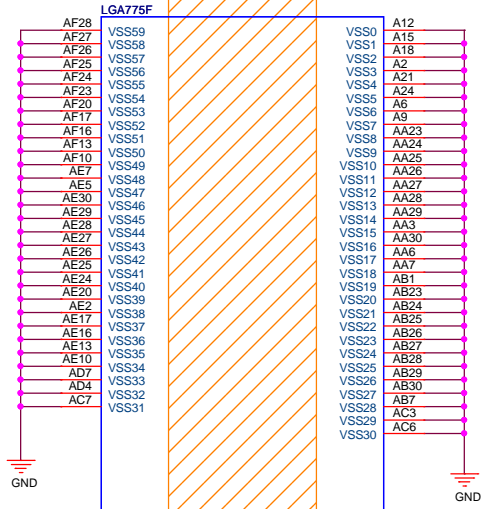
For Support NWD-T CPU

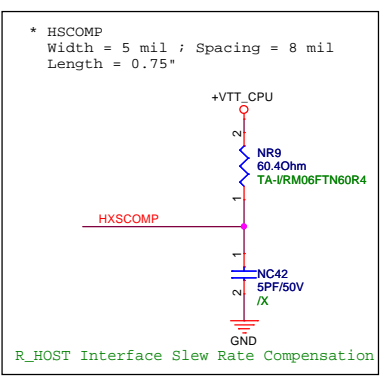
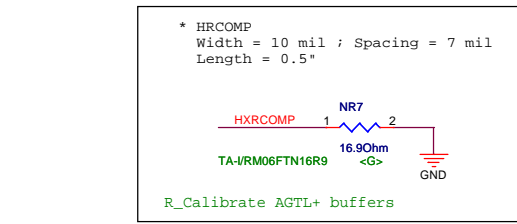
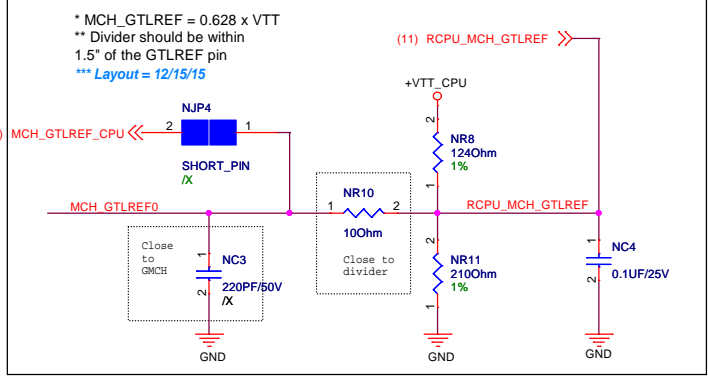
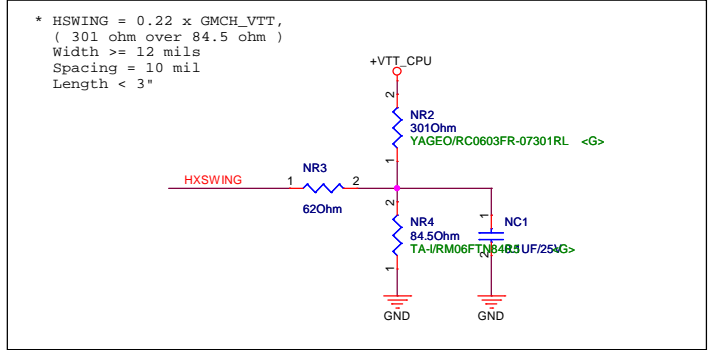
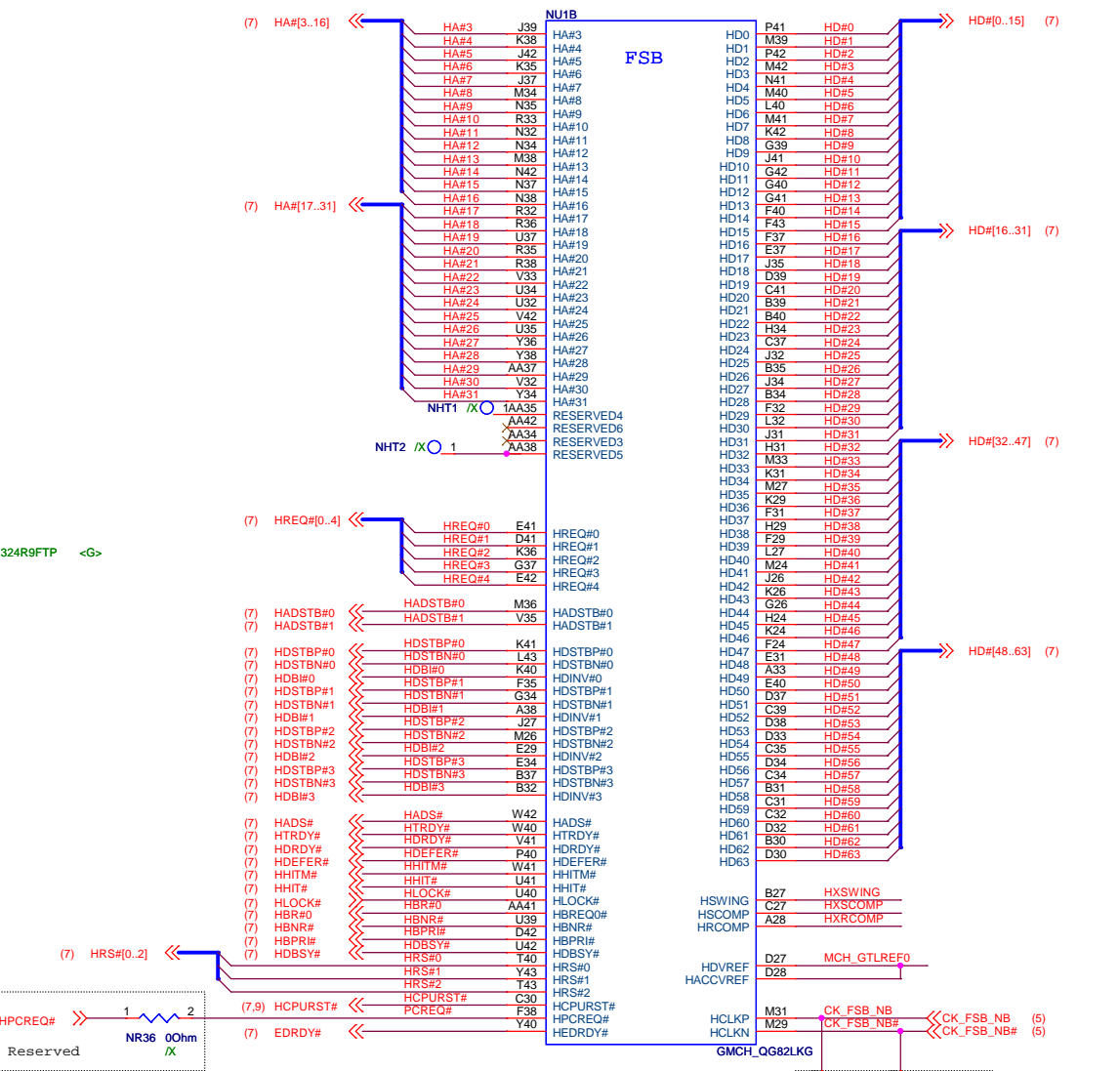
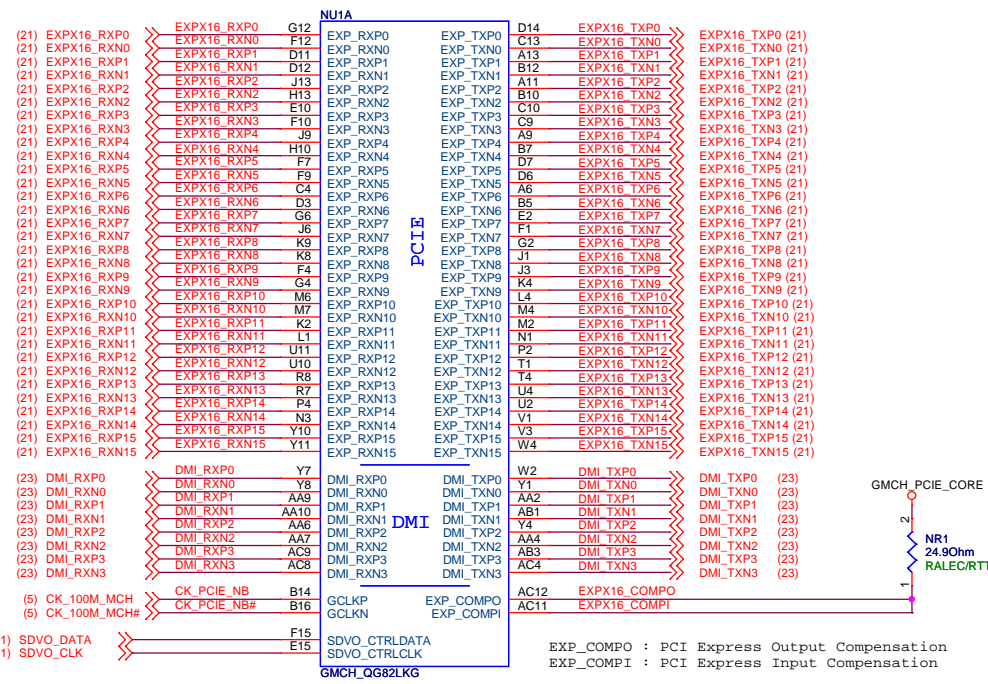
VTT_OUT_L
 RESET#
 BR0#
 PWRGOOD
 TESTH1
 TESTH1[8:12]

VTT_OUT_R
 VTTTPWRGD
 VID[5:0] /w 680 ohm
 (x) GTLREF0 /w divider 49.9/100 ohm
 TD1 /w 49.9 ohm
 TDO /w 49.9 ohm
 BPM[5:0] /w 49.9 ohm

ANY
 (x) COMP[2:3] /w 100 ohm

Update 12/27





<Variant Name>

ASUS Title : Lakeport-1

ASUSTek Computer Inc. Engineer: SEP_HU

Size	Project Name	Rev
A3	P5GC-MX 1.00G	2.00

Date: Tuesday, February 02, 2010 Sheet 12 of 47

NU1C

Table of pin connections for NU1C, including SMA, SDQS, SCLK, SCLK_A#, SCLK_A#0, SCLK_A#1, SCLK_A#2, SCLK_A#3, SCLK_A#4, SCLK_A#5, SCLK_A#0, SCLK_A#0#, SCLK_A#1, SCLK_A#1#, SCLK_A#2, SCLK_A#2#, SCLK_A#3, SCLK_A#3#, SCLK_A#4, SCLK_A#4#, SCLK_A#5, SCLK_A#5#, SCLK_A#0, SCLK_A#0#, SCLK_A#1, SCLK_A#1#, SCLK_A#2, SCLK_A#2#, SCLK_A#3, SCLK_A#3#, SCLK_A#4, SCLK_A#4#, SCLK_A#5, SCLK_A#5#, SCLK_A#0, SCLK_A#0#, SCLK_A#1, SCLK_A#1#, SCLK_A#2, SCLK_A#2#, SCLK_A#3, SCLK_A#3#, SCLK_A#4, SCLK_A#4#, SCLK_A#5, SCLK_A#5#.

NU1D

Table of pin connections for NU1D, including SMA, SDQS, SCLK, SCLK_A#, SCLK_A#0, SCLK_A#1, SCLK_A#2, SCLK_A#3, SCLK_A#4, SCLK_A#5, SCLK_A#0, SCLK_A#0#, SCLK_A#1, SCLK_A#1#, SCLK_A#2, SCLK_A#2#, SCLK_A#3, SCLK_A#3#, SCLK_A#4, SCLK_A#4#, SCLK_A#5, SCLK_A#5#, SCLK_A#0, SCLK_A#0#, SCLK_A#1, SCLK_A#1#, SCLK_A#2, SCLK_A#2#, SCLK_A#3, SCLK_A#3#, SCLK_A#4, SCLK_A#4#, SCLK_A#5, SCLK_A#5#.

DDR_A

Table of pin connections for DDR_A, including SDQS, SCLK, SCLK_A#, SCLK_A#0, SCLK_A#1, SCLK_A#2, SCLK_A#3, SCLK_A#4, SCLK_A#5, SCLK_A#0, SCLK_A#0#, SCLK_A#1, SCLK_A#1#, SCLK_A#2, SCLK_A#2#, SCLK_A#3, SCLK_A#3#, SCLK_A#4, SCLK_A#4#, SCLK_A#5, SCLK_A#5#.

DDR_B

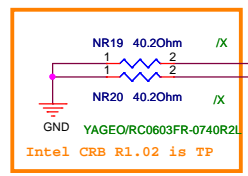
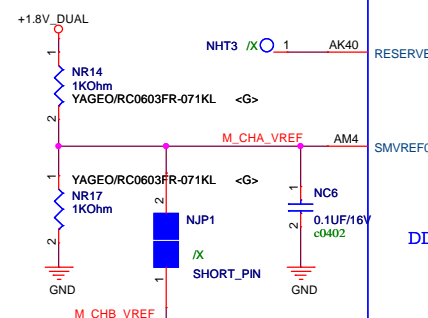
Table of pin connections for DDR_B, including SDQS, SCLK, SCLK_A#, SCLK_A#0, SCLK_A#1, SCLK_A#2, SCLK_A#3, SCLK_A#4, SCLK_A#5, SCLK_A#0, SCLK_A#0#, SCLK_A#1, SCLK_A#1#, SCLK_A#2, SCLK_A#2#, SCLK_A#3, SCLK_A#3#, SCLK_A#4, SCLK_A#4#, SCLK_A#5, SCLK_A#5#.

GMCH_OG82LKG

Table of pin connections for GMCH_OG82LKG, including SDQS, SCLK, SCLK_A#, SCLK_A#0, SCLK_A#1, SCLK_A#2, SCLK_A#3, SCLK_A#4, SCLK_A#5, SCLK_A#0, SCLK_A#0#, SCLK_A#1, SCLK_A#1#, SCLK_A#2, SCLK_A#2#, SCLK_A#3, SCLK_A#3#, SCLK_A#4, SCLK_A#4#, SCLK_A#5, SCLK_A#5#.

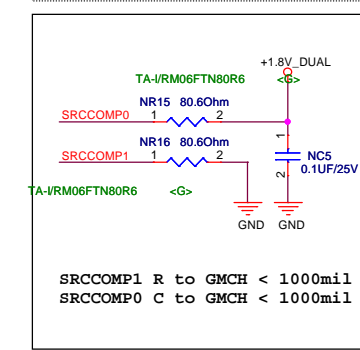
GMCH_OG82LKG

Table of pin connections for GMCH_OG82LKG, including SDQS, SCLK, SCLK_A#, SCLK_A#0, SCLK_A#1, SCLK_A#2, SCLK_A#3, SCLK_A#4, SCLK_A#5, SCLK_A#0, SCLK_A#0#, SCLK_A#1, SCLK_A#1#, SCLK_A#2, SCLK_A#2#, SCLK_A#3, SCLK_A#3#, SCLK_A#4, SCLK_A#4#, SCLK_A#5, SCLK_A#5#.



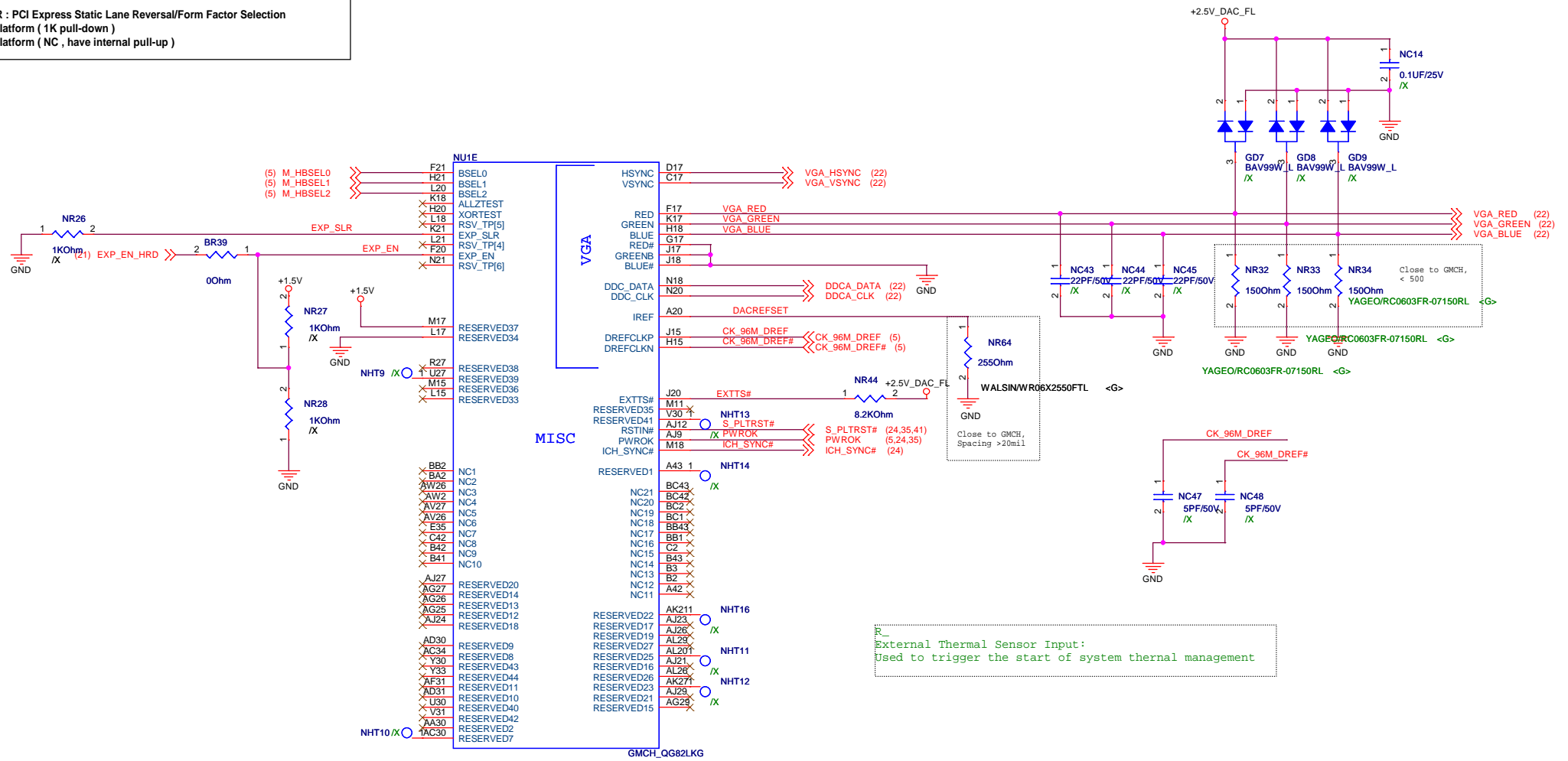
R_OCD Calibration during DRAM Device buffer impedance adjustment mode

GMCH adjust internal DDR2 IO buffers' driving impedance, RCOMP[1]:pull high impedance, RCOMP[0]:pulldown impedance.

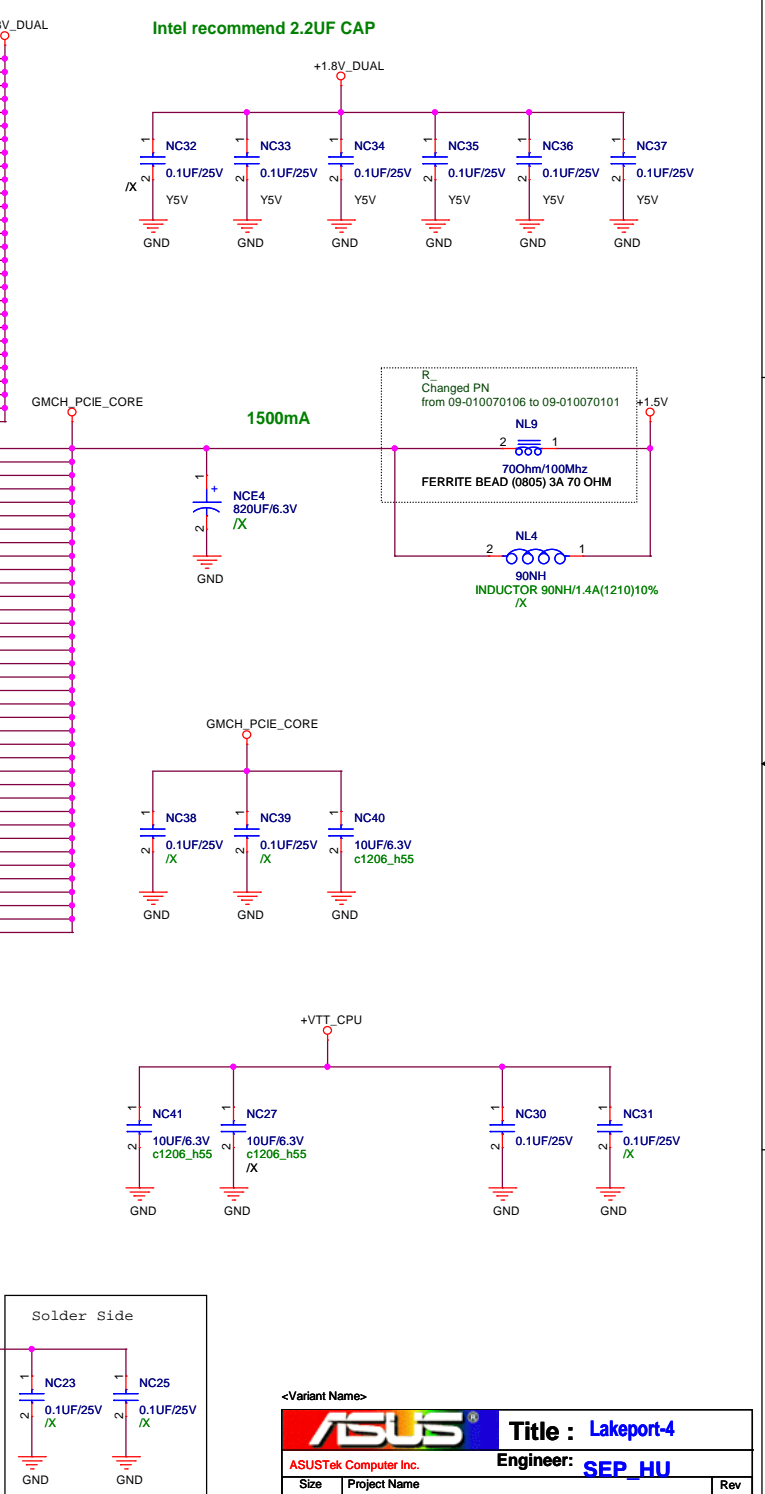
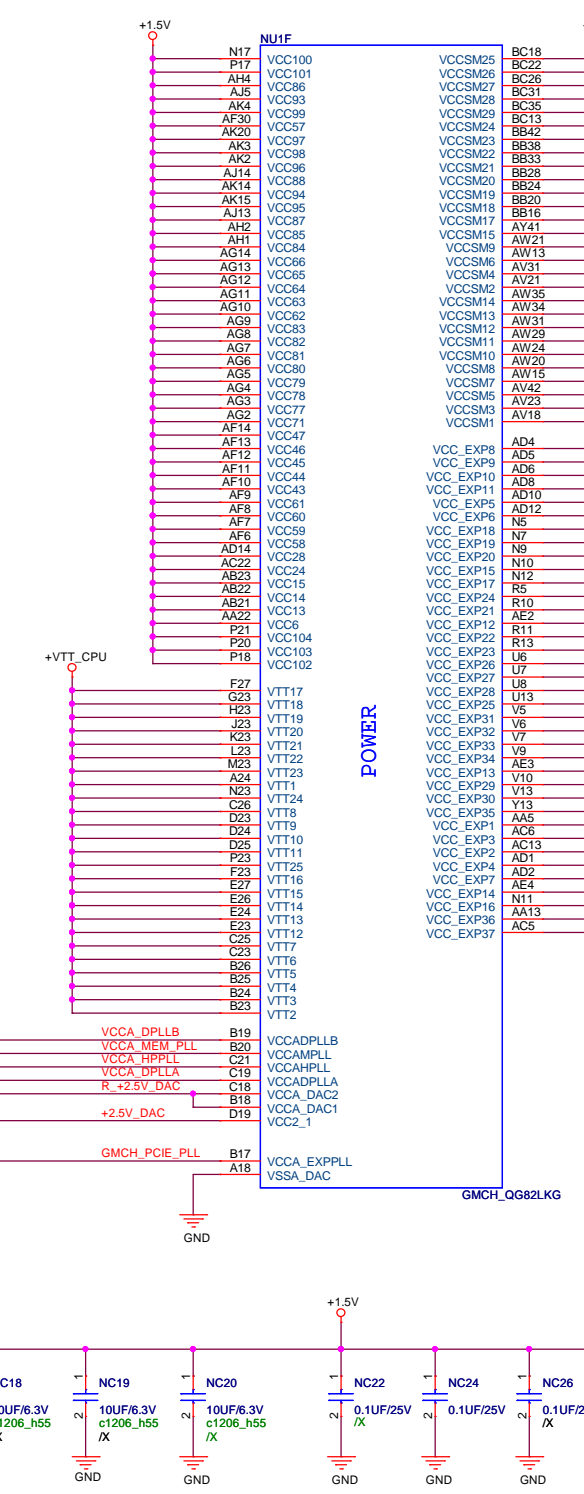
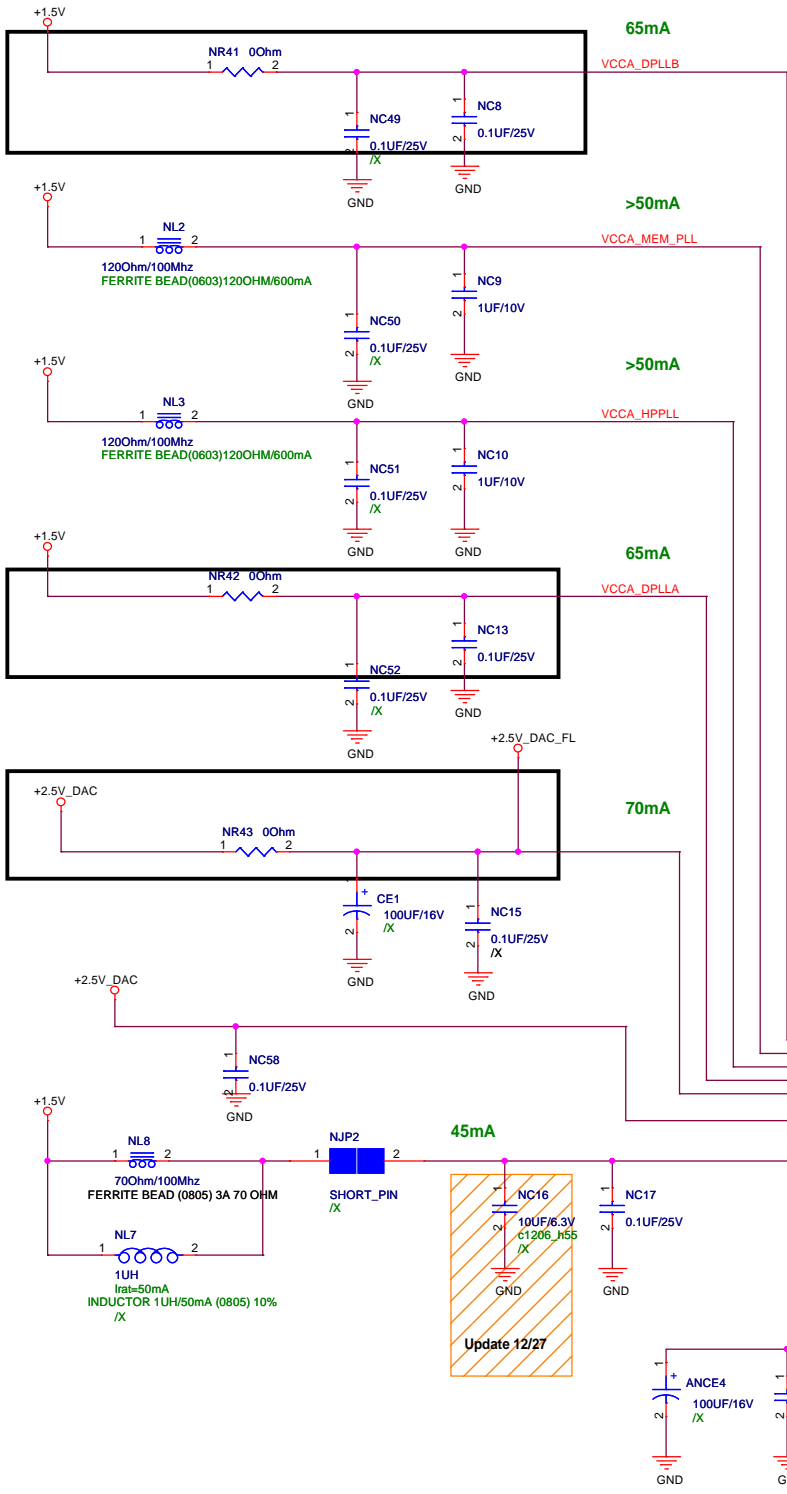


ASUS logo and product information: Title: Lakeport-2, ASUSTek Computer Inc., Engineer: SEP_HU, Size A3, Project Name: P5GC-MX 1.00G, Date: Tuesday, February 02, 2010, Sheet 13 of 47, Rev 2.00

* EXP_SLR : PCI Express Static Lane Reversal/Form Factor Selection
 0 : BTX platform (1K pull-down)
 1 : ATX platform (NC , have internal pull-up)



External Thermal Sensor Input:
 Used to trigger the start of system thermal management



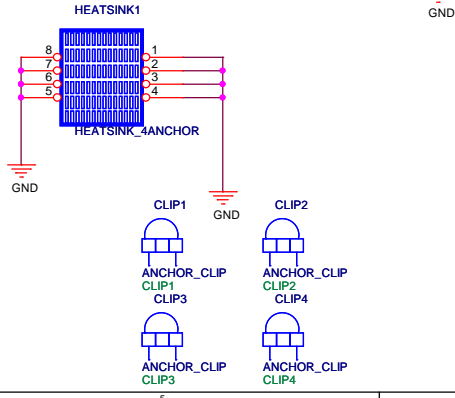
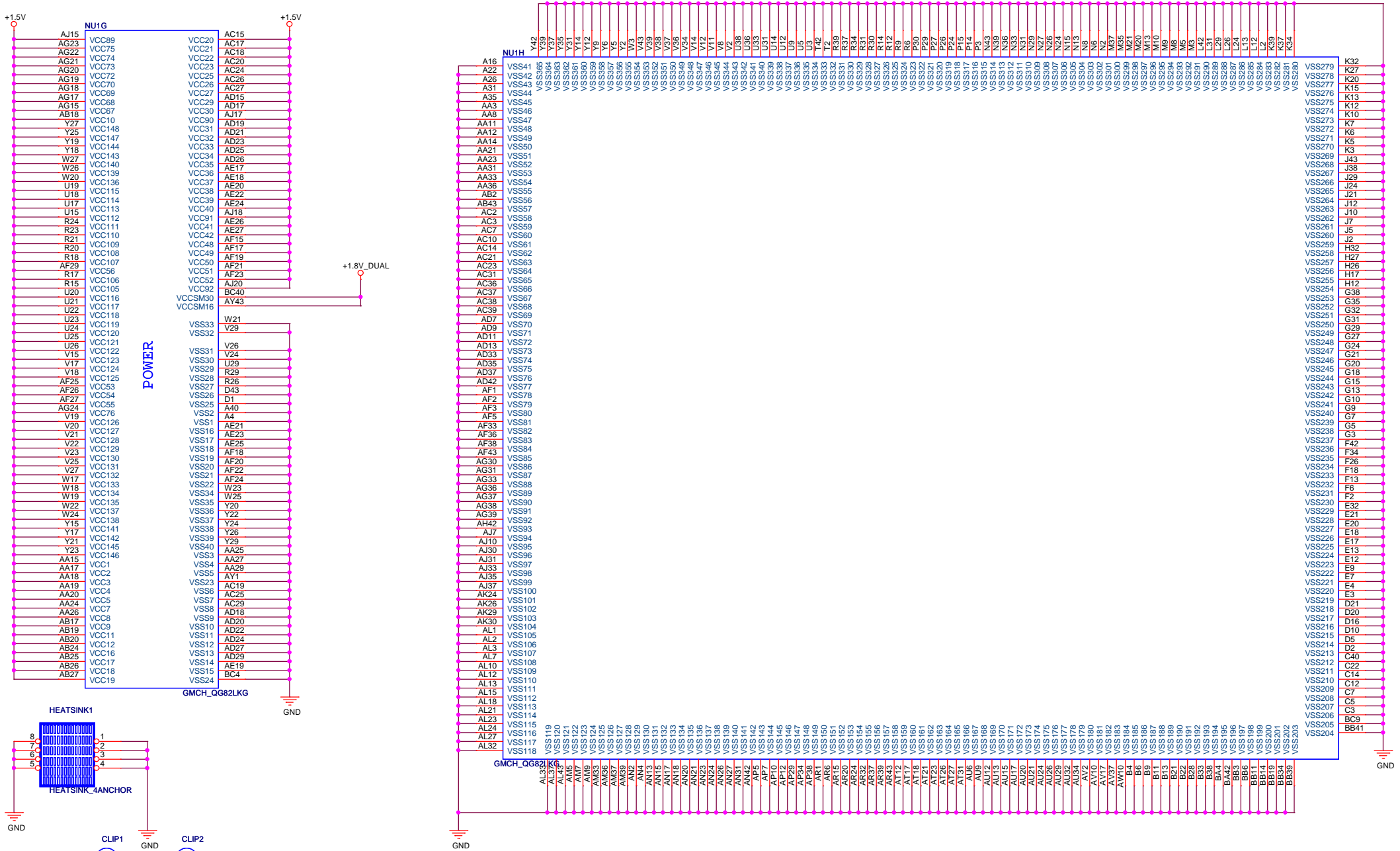
<Variant Name>

ASUS Title : **Lakeport-4**

ASUSTek Computer Inc. Engineer: **SEP_HU**

Size	Project Name	Rev
A3	P5GC-MX 1.00G	2.00

Date: Tuesday, February 02, 2010 Sheet 15 of 47



<-Variant Name>

ASUS		Title : Lakeport-5	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010	Sheet 16	of 47	

LP FootPrint

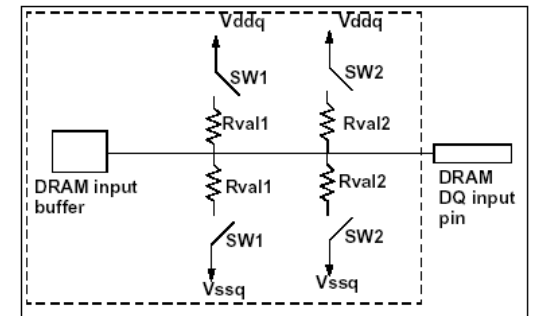
DIMM_A1A

MAA_A0	188	A0	DQ63	236 MD A63
MAA_A1	183	A1	DQ62	235 MD A62
MAA_A2	62	A2	DQ61	230 MD A61
MAA_A3	182	A3	DQ60	229 MD A60
MAA_A4	61	A4	DQ59	117 MD A59
MAA_A5	60	A5	DQ58	116 MD A58
MAA_A6	180	A6	DQ57	111 MD A57
MAA_A7	58	A7	DQ56	110 MD A56
MAA_A8	179	A8	DQ55	227 MD A55
MAA_A9	177	A9	DQ54	226 MD A54
MAA_A10	70	A10/AP	DQ53	218 MD A53
MAA_A11	57	A11	DQ52	217 MD A52
MAA_A12	176	A12	DQ51	108 MD A51
MAA_A13	196	A13	DQ50	107 MD A50
174	X	A14	DQ49	99 MD A49
173	X	A15	DQ48	98 MD A48
CK_DIMM_A2	220	CK2P	DQ47	215 MD A47
CK_DIMM_A2#	221	CK2N	DQ46	214 MD A46
CK_DIMM_A1	137	CK1P	DQ45	209 MD A45
CK_DIMM_A1#	138	CK1N	DQ44	208 MD A44
CK_DIMM_A0#	185	CK0P	DQ43	96 MD A43
CK_DIMM_A0#	186	CK0N	DQ42	95 MD A42
MCS_A1#	76	CS1#	DQ41	89 MD A40
MCS_A0#	193	CS0#	DQ40	206 MD A39
MCKE_A1	171	CKE1	DQ39	205 MD A38
MCKE_A0	52	CKE0	DQ38	200 MD A37
MBS_A2	54	A16/BA2	DQ37	199 MD A36
MBS_A1	190	BA1	DQ36	87 MD A35
MBS_A0	71	BA0	DQ35	86 MD A34
SMB_DATA_MAIN	119	SDA	DQ34	81 MD A33
SMB_CLK_MAIN	120	SCL	DQ33	80 MD A32
168	X	NC/CB7	DQ32	159 MD A31
167	X	NC/CB6	DQ31	158 MD A30
162	X	NC/CB5	DQ30	153 MD A29
161	X	NC/CB4	DQ29	152 MD A28
49	X	NC/CB3	DQ28	40 MD A27
48	X	NC/CB3	DQ27	39 MD A26
43	X	NC/CB2	DQ26	34 MD A25
42	X	NC/CB1	DQ25	33 MD A24
42	X	NC/CB0	DQ24	150 MD A23
101	X	SA2	DQ23	149 MD A22
240	X	SA1	DQ22	144 MD A21
239	X	SA0	DQ21	143 MD A20
73	X	WE#	DQ20	31 MD A19
192	X	RAS#	DQ19	30 MD A18
74	X	CAS#	DQ18	25 MD A17
77	X	ODT1	DQ17	24 MD A16
195	X	ODT0	DQ16	24 MD A16
55	X	RC02	DQ15	140 MD A14
18	X	RESET#	DQ14	132 MD A13
164	X	DM8/DQS17P	DQ13	131 MD A12
165	X	NC/DQS17N	DQ12	22 MD A11
232	X	DM7/DQS16P	DQ11	21 MD A10
233	X	NC/DQS16N	DQ10	13 MD A9
223	X	DM6/DQS15P	DQ9	12 MD A8
224	X	NC/DQS15N	DQ8	129 MD A7
211	X	DM5/DQS14P	DQ7	128 MD A6
212	X	NC/DQS14N	DQ6	123 MD A5
202	X	DM4/DQS13P	DQ5	122 MD A4
155	X	NC/DQS13N	DQ4	10 MD A3
156	X	DM3/DQS12P	DQ3	9 MD A2
146	X	NC/DQS12N	DQ2	4 MD A1
147	X	DM2/DQS11P	DQ1	3 MD A0
134	X	NC/DQS11N	DQ0	
135	X	DM1/DQS10P		
125	X	NC/DQS10N		
126	X	DM0/DQS9P		
46	X	NC/DQS9N		
45	X	NC/DQS8P		
45	X	NC/DQS8N		
102	X	NC2	241	MDQS_A7
68	X	NC1	242	MDQS_A7#
19	X	NC0	243	MDQS_A6

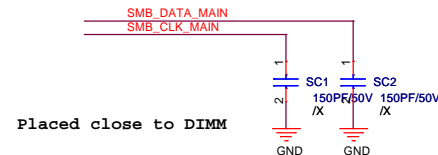
- >> MD_A[63..0] (13)
- >> MAA_A[13..0] (13,18)
- >> MBS_A[2..0] (13,18)
- >> MODT_A[1..0] (13,18)
- >> MDQM_A[7..0] (13)
- >> MCKE_A[1..0] (13,18)
- >> MCS_A0# (13,18)
- >> MCS_A1# (13,18)
- >> MWE_A# (13,18)
- >> MCAS_A# (13,18)
- >> MRAS_A# (13,18)
- >> CK_DIMM_A0 (13)
- >> CK_DIMM_A0# (13)
- >> CK_DIMM_A1 (13)
- >> CK_DIMM_A1# (13)
- >> CK_DIMM_A2 (13)
- >> CK_DIMM_A2# (13)
- >> MDQS_A7# (13)
- >> MDQS_A7 (13)
- >> MDQS_A6# (13)
- >> MDQS_A6 (13)
- >> MDQS_A5# (13)
- >> MDQS_A5 (13)
- >> MDQS_A4# (13)
- >> MDQS_A4 (13)
- >> MDQS_A3# (13)
- >> MDQS_A3 (13)
- >> MDQS_A2# (13)
- >> MDQS_A2 (13)
- >> MDQS_A1# (13)
- >> MDQS_A1 (13)
- >> MDQS_A0# (13)
- >> MDQS_A0 (13)
- >> SMB_CLK_MAIN (5,9,19,21,24,27,41)
- >> SMB_DATA_MAIN (5,9,19,21,24,27,41)

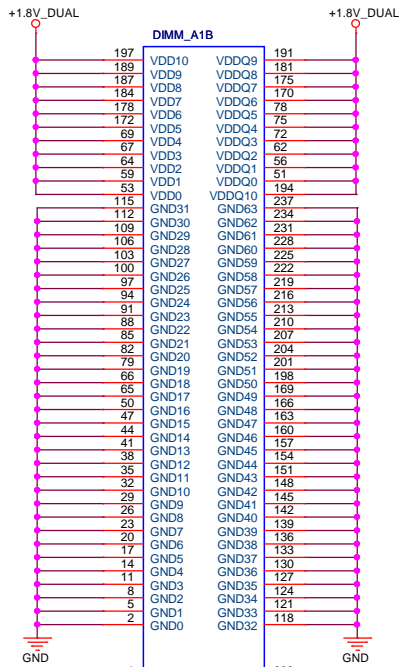
1.00 ODT On die Termination
 1.Reduced DQ and DQS skew
 2.Increased voltage margin
 3.Reduced board area and BOM cost
 There status Off,75,150 Ohm

ODT: On Die Termination



- Controlled by memory controller via ODT pin.
- Can be turned on/off in 2 cycles
- Provides active termination at the receiver interface.

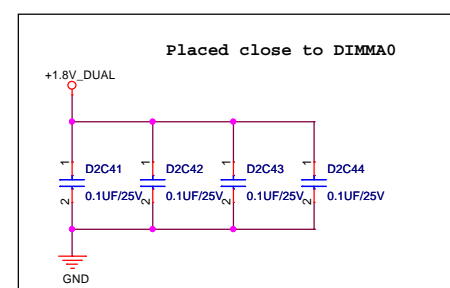
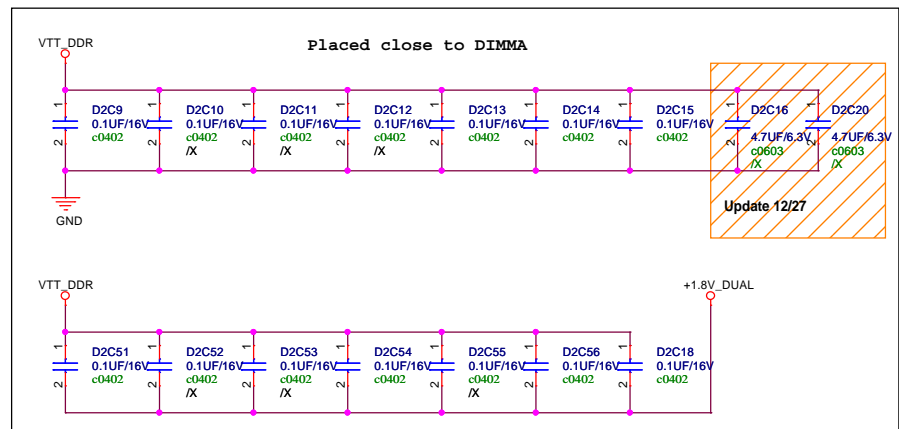
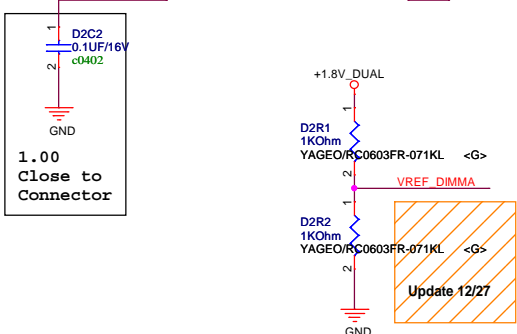
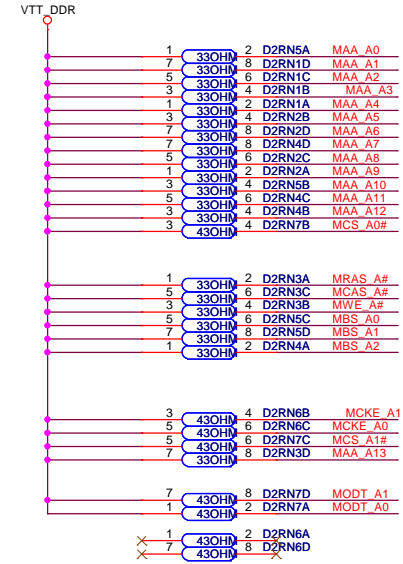
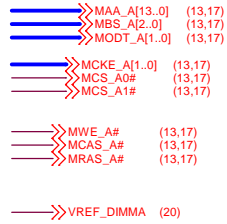




1.00 DDR2 need termination signals :

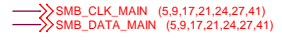
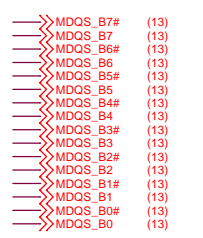
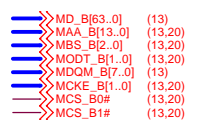
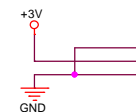
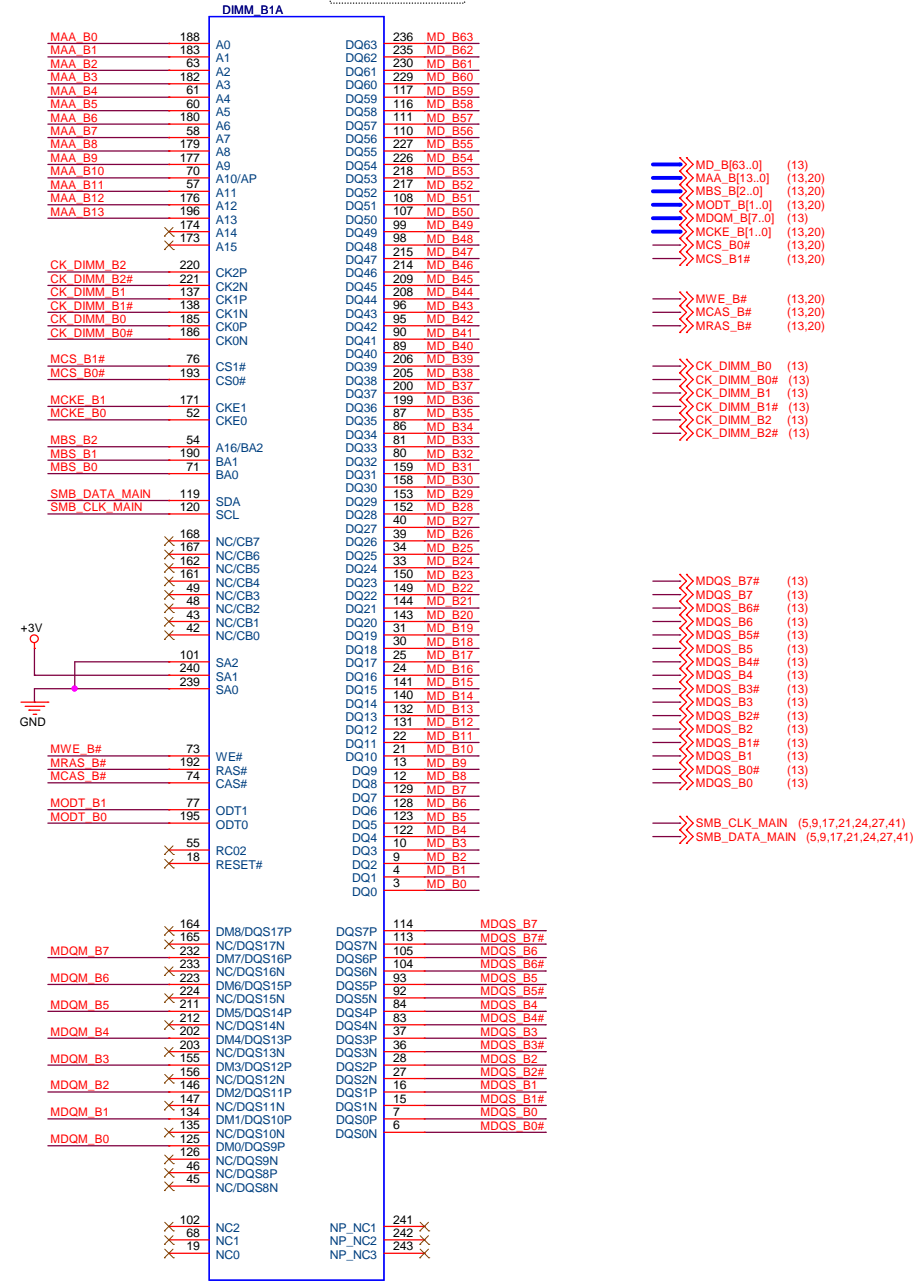
```

CS#[3:0]
CKE[3:0]
ODT[3:0]
MA[13:0]
BS[2:0]
CAS#
CAS#
WE#
  
```



1.00 DDR2 Spec.
VDDQ 1.8V for DQ power
VDD 1.8V for power
VDDL 1.8V for DLL power

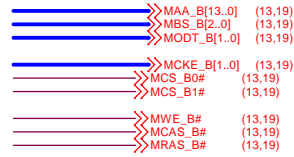
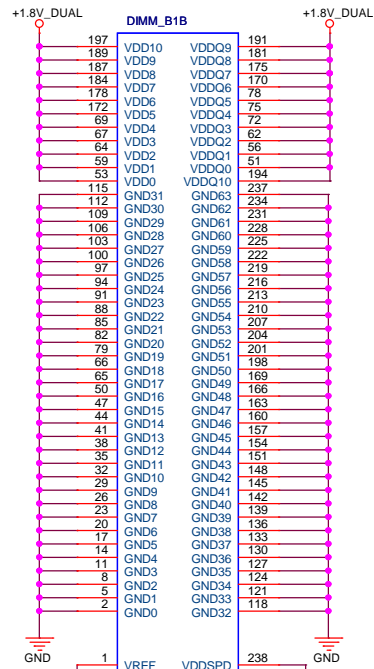
LF FootPrint



DDR_DIMM_240P

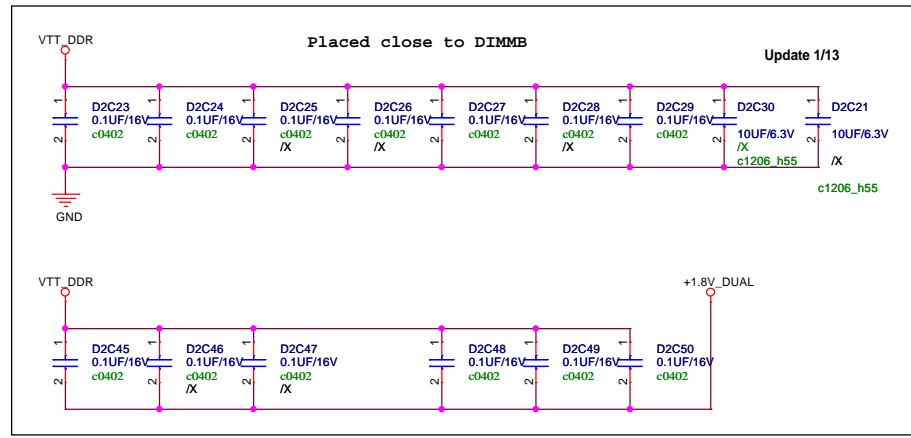
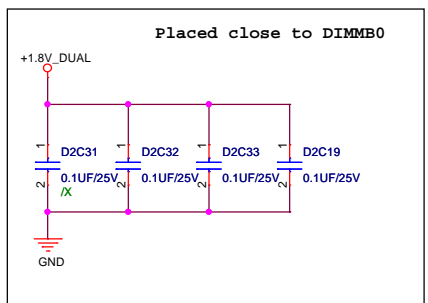
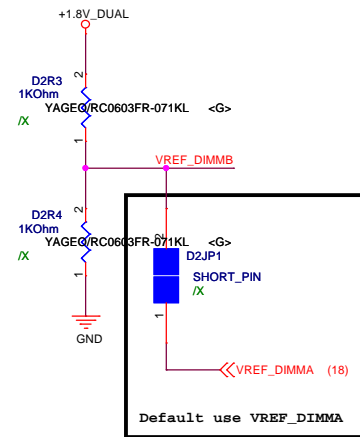
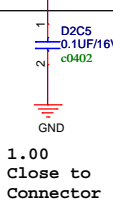
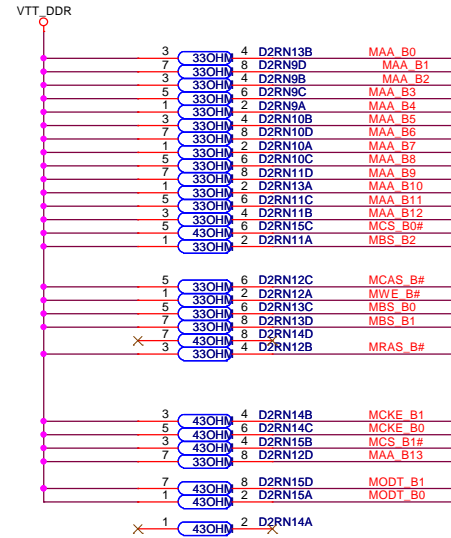
<Variant Name>

ASUS		Title : DDR2-CHB Control	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010		Sheet	19 of 47

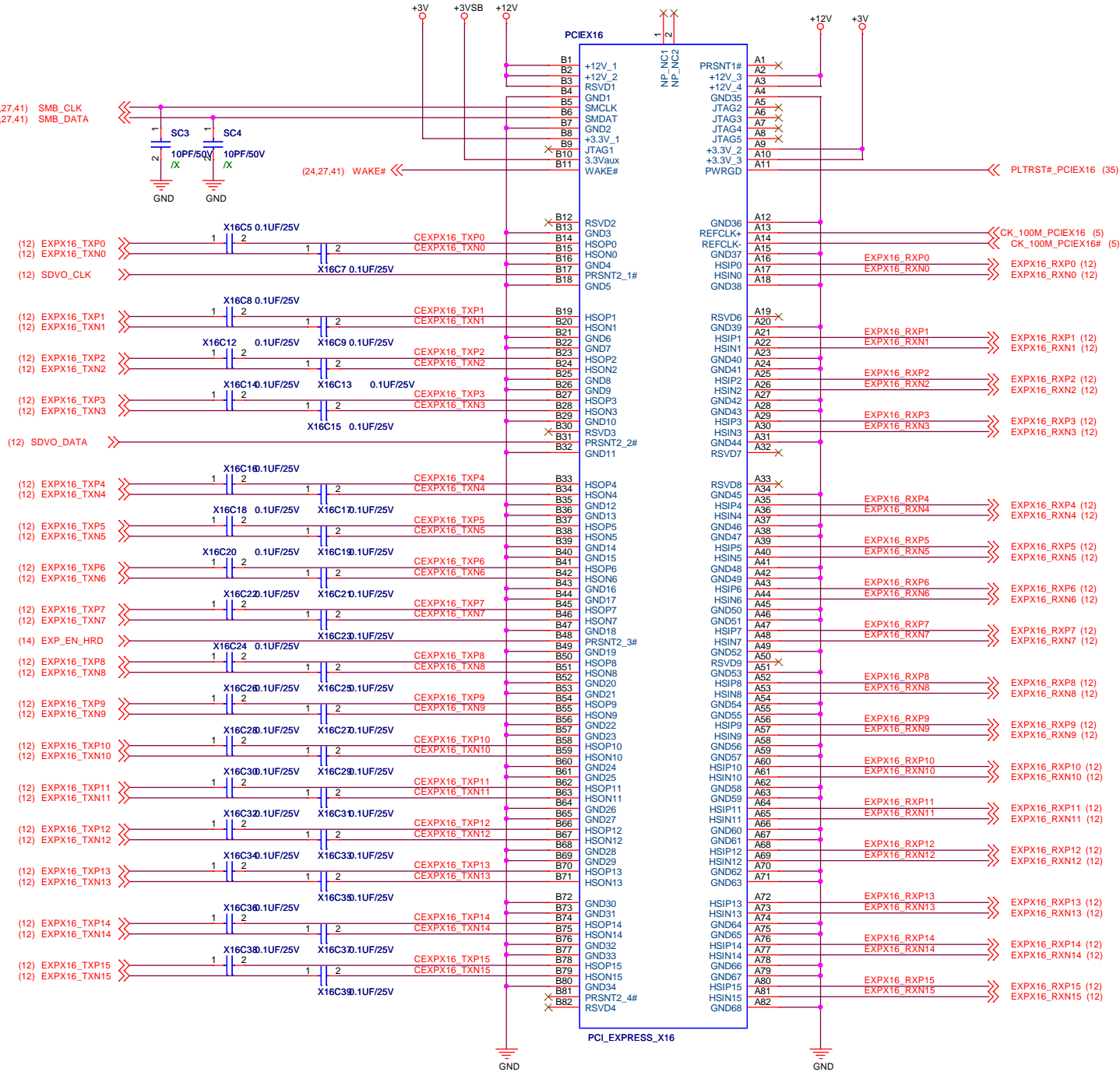


1.00 DDR2 need termination signals :

CS#[3:0]
 CKE[3:0]
 ODT[3:0]
 MA[13:0]
 BS[2:0]
 RAS#
 CAS#
 WE#

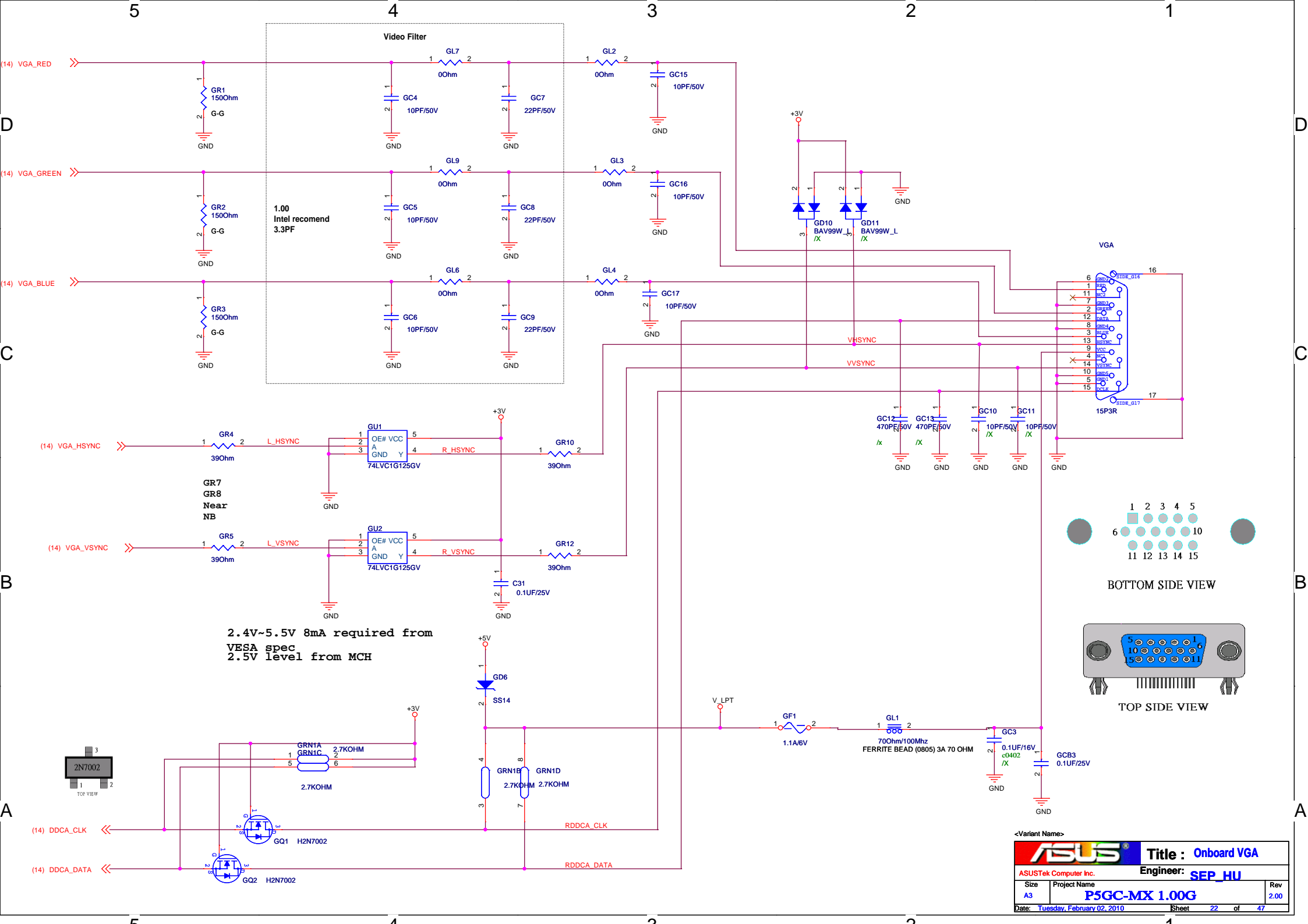


(5,9,17,19,24,27,41) SMB_CLK
(5,9,17,19,24,27,41) SMB_DATA



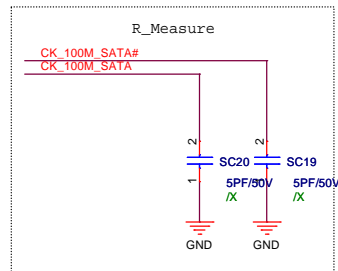
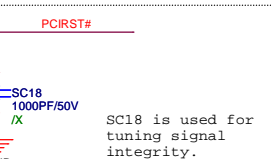
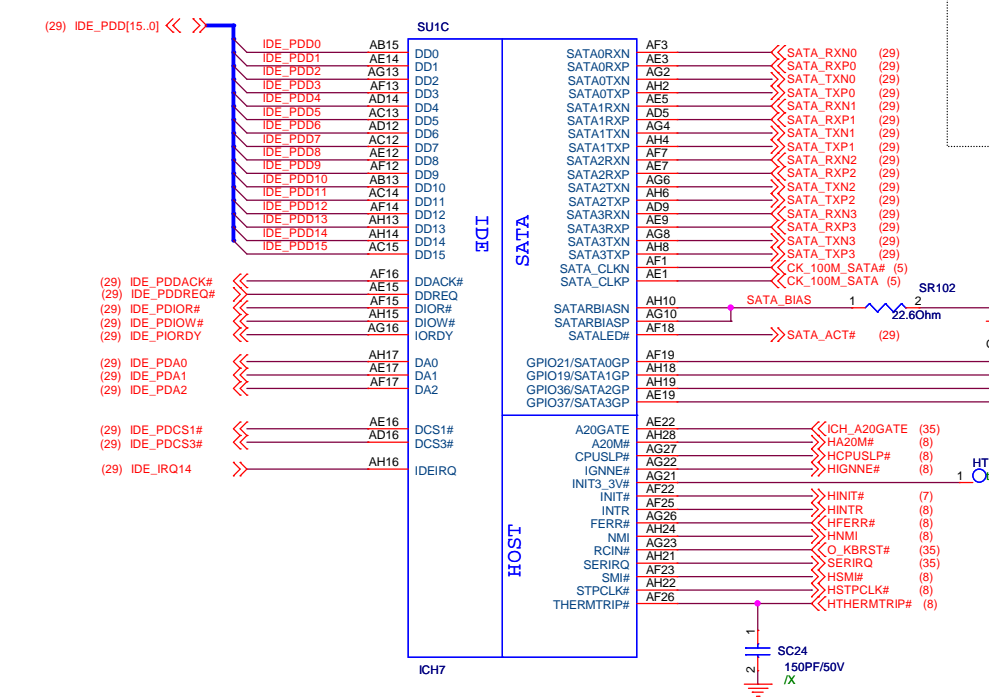
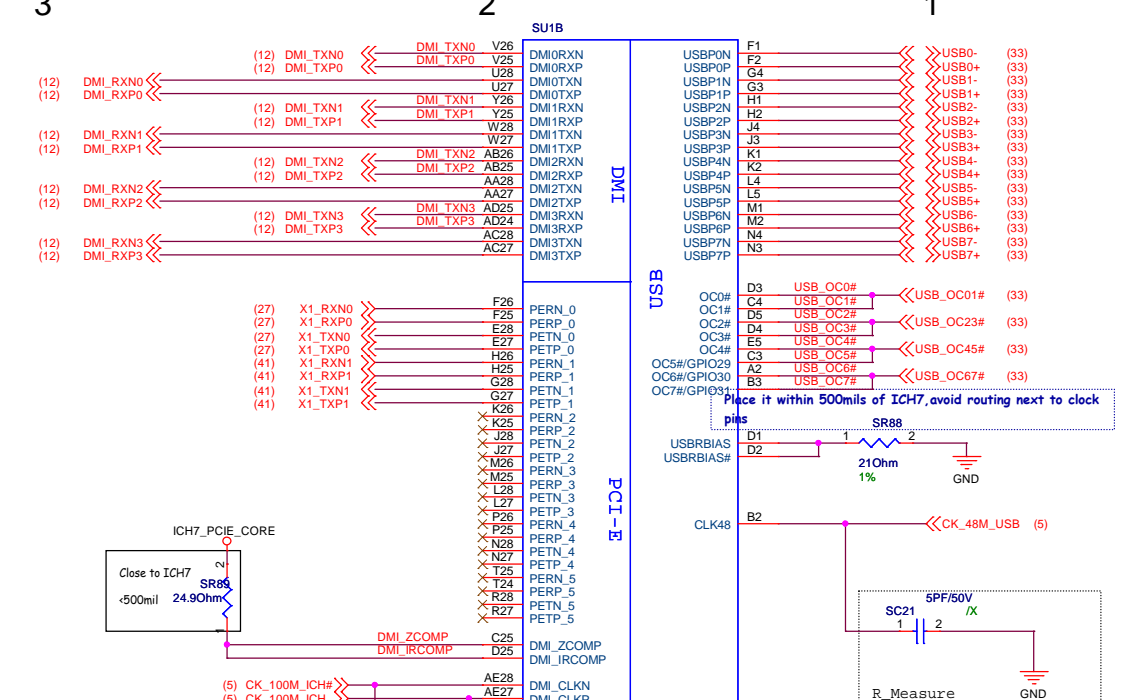
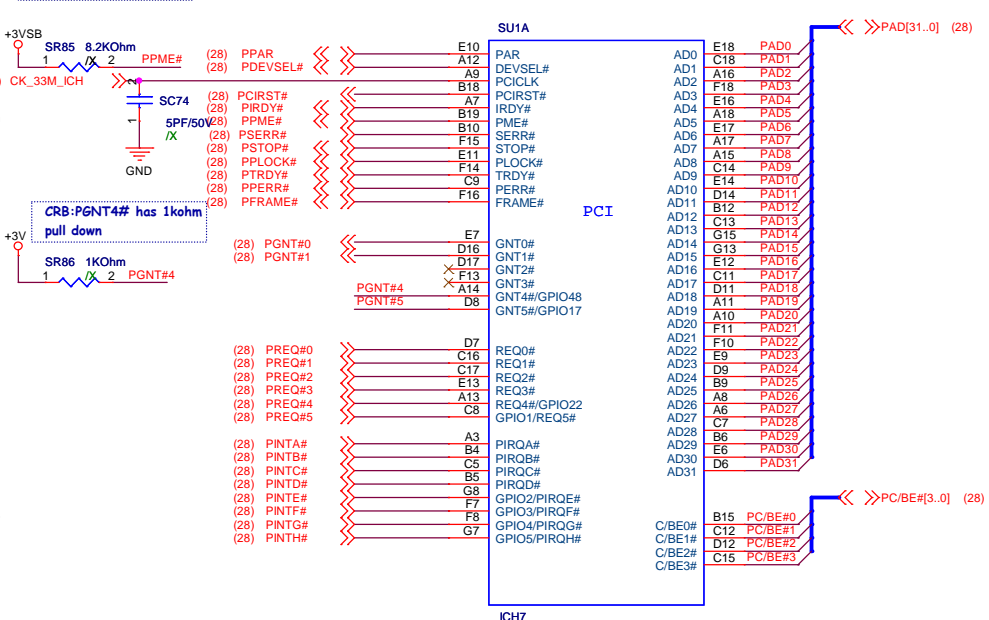
<Variant Name>

ASUS		Title : PCI Express X16	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size	Project Name	Rev	
A3	P5GC-MX 1.00G	2.00	
Date: Tuesday, February 02, 2010	Sheet 21	of 47	



Note: check naming rule CK_33M_? PCIRST#

ICH7 will not driver PME# high, but it will be pull up to +3VSB by an internal pull-up resistor

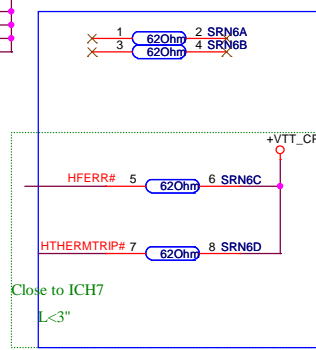


Boot BIOS Destination Selection

Sampled at Rising edge of PWROK (GNT5# is MSB)

0 : SPI

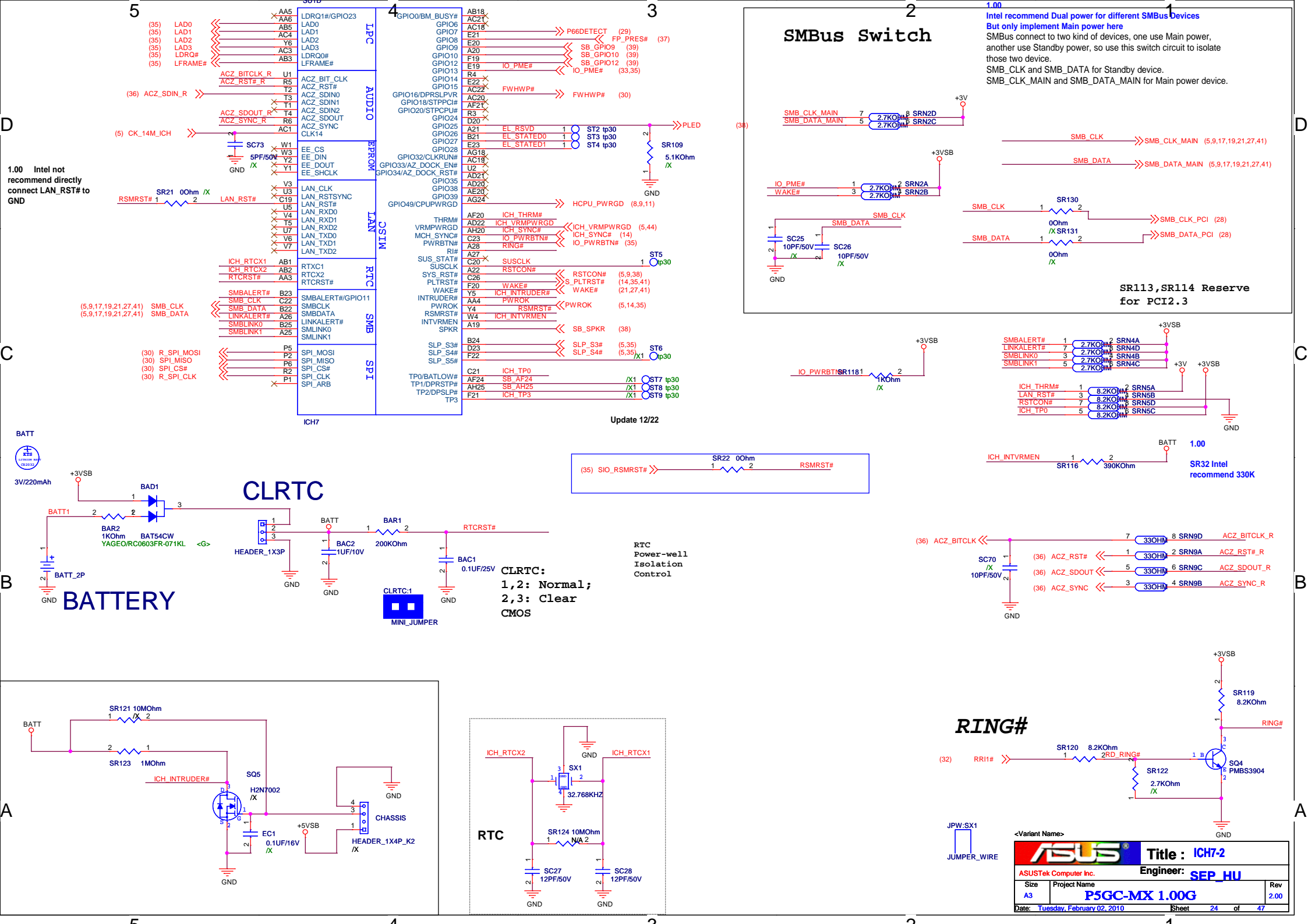
1 : LPC (Weak internal pull-up)

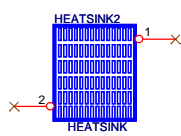
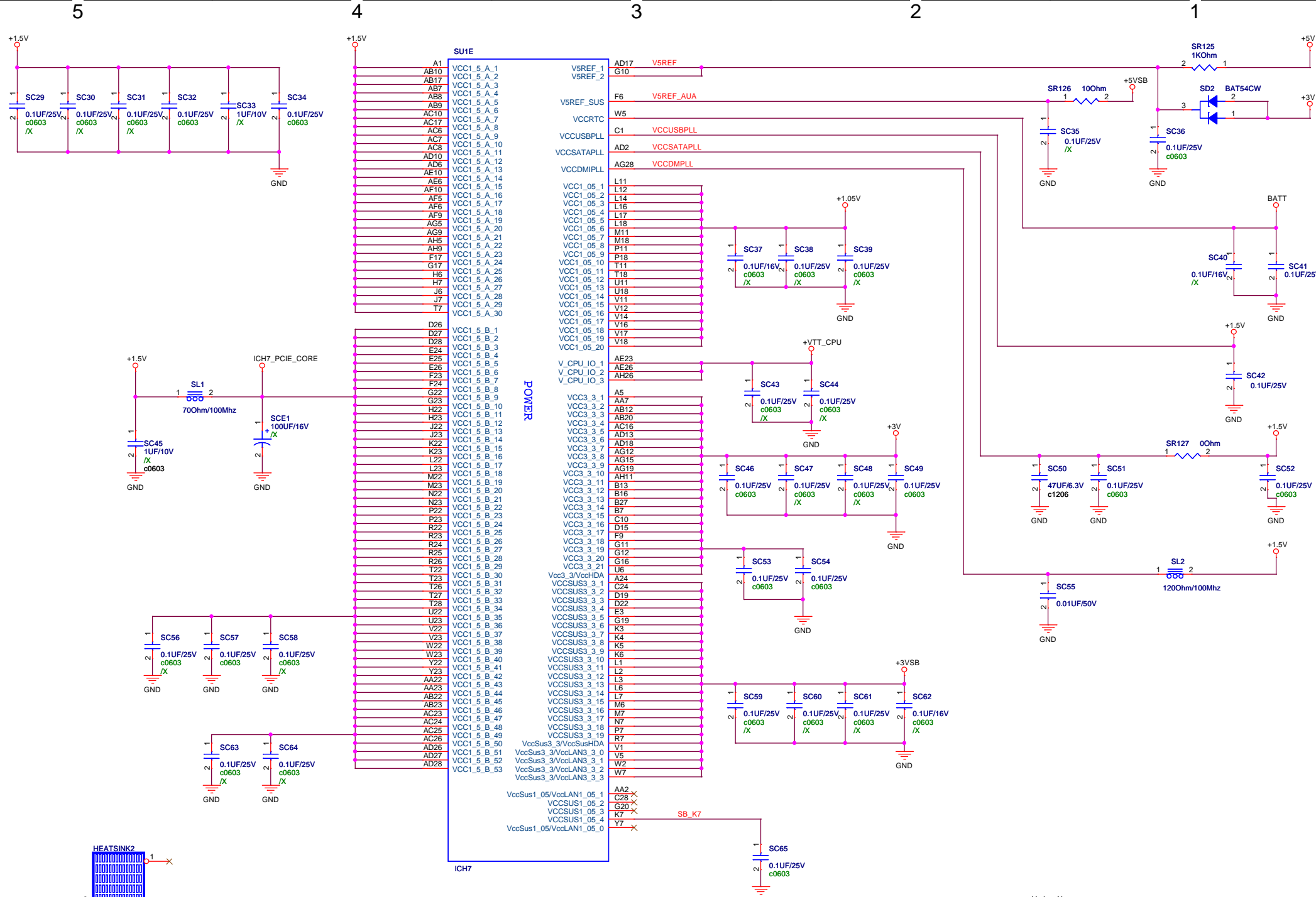


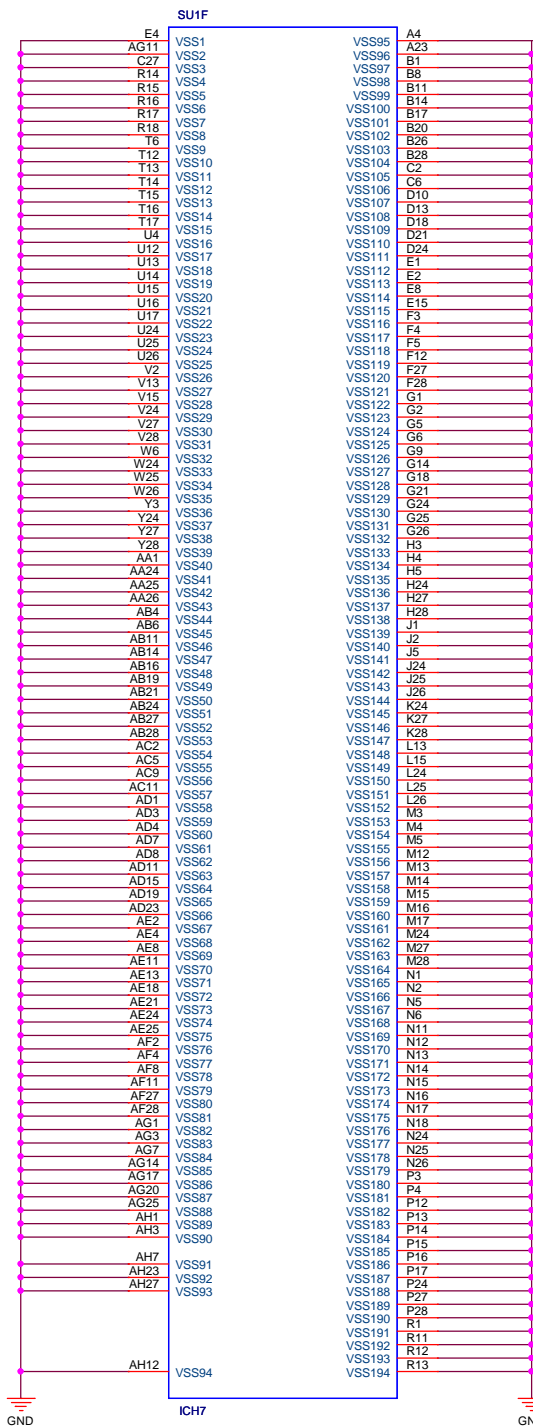
ASUS Title : ICH7-1

ASUSTek Computer Inc. Engineer: SEP_HU

Size	Project Name	Rev
A3	P5GC-MX 1.00G	2.00
Date: Tuesday, February 02, 2010	Sheet 23 of 47	



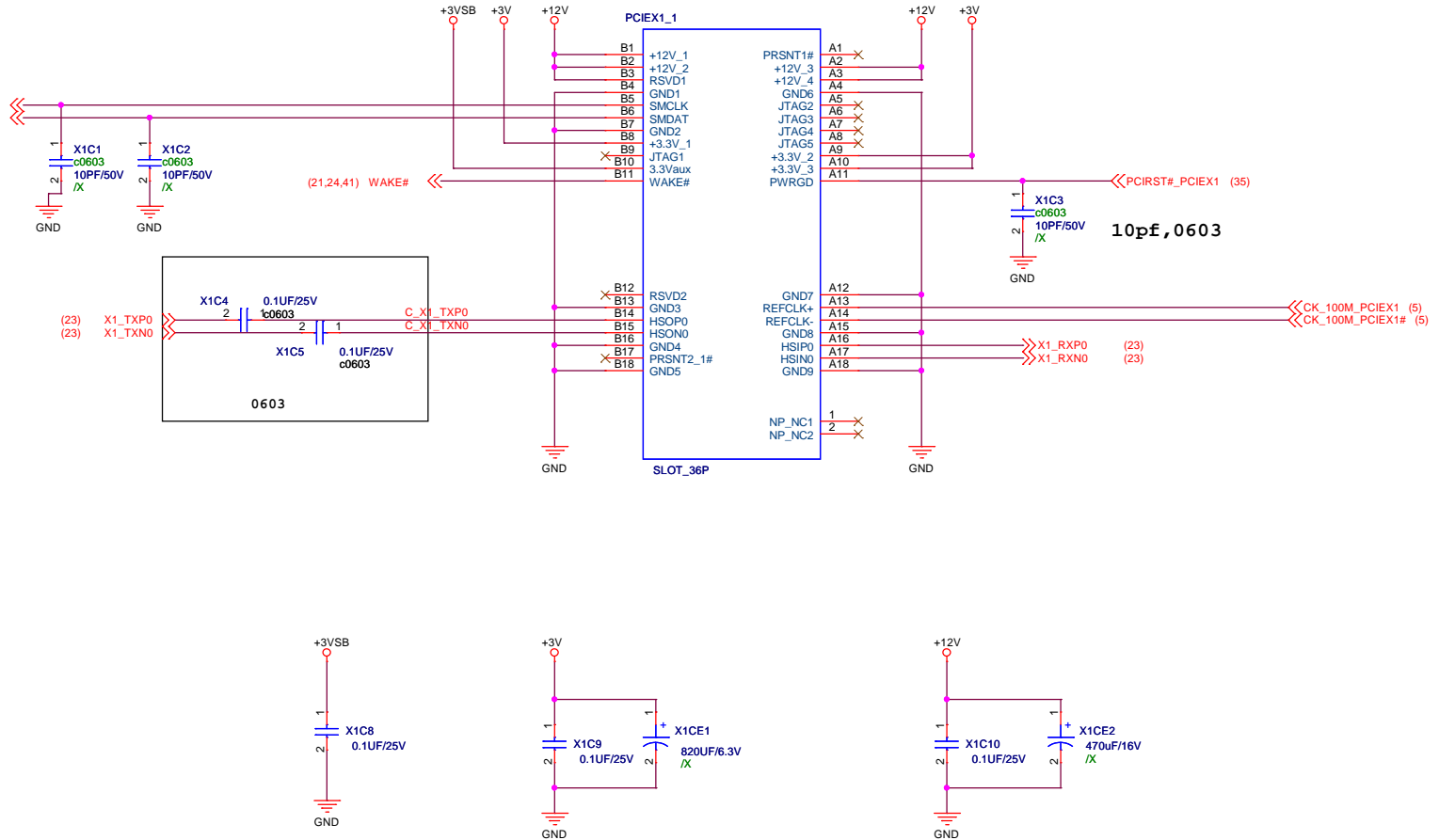




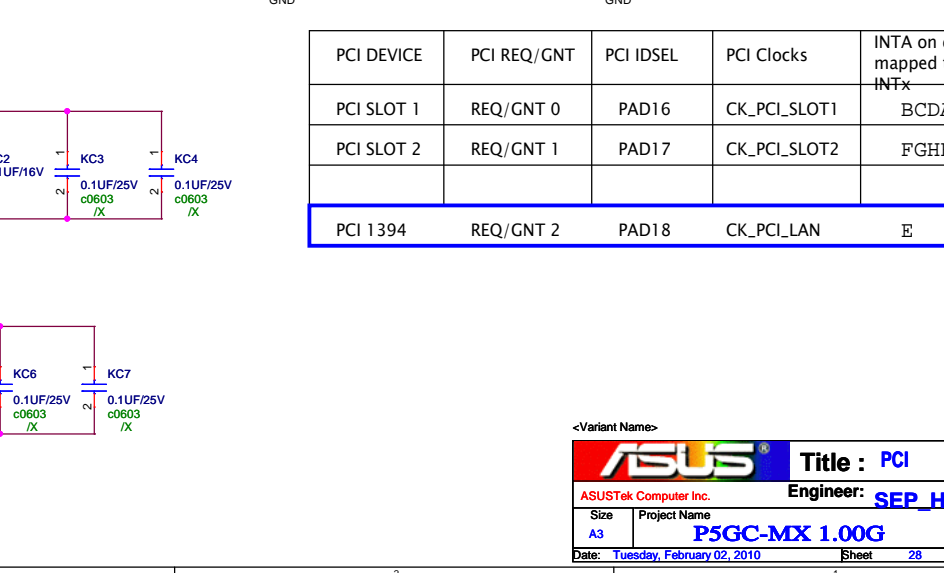
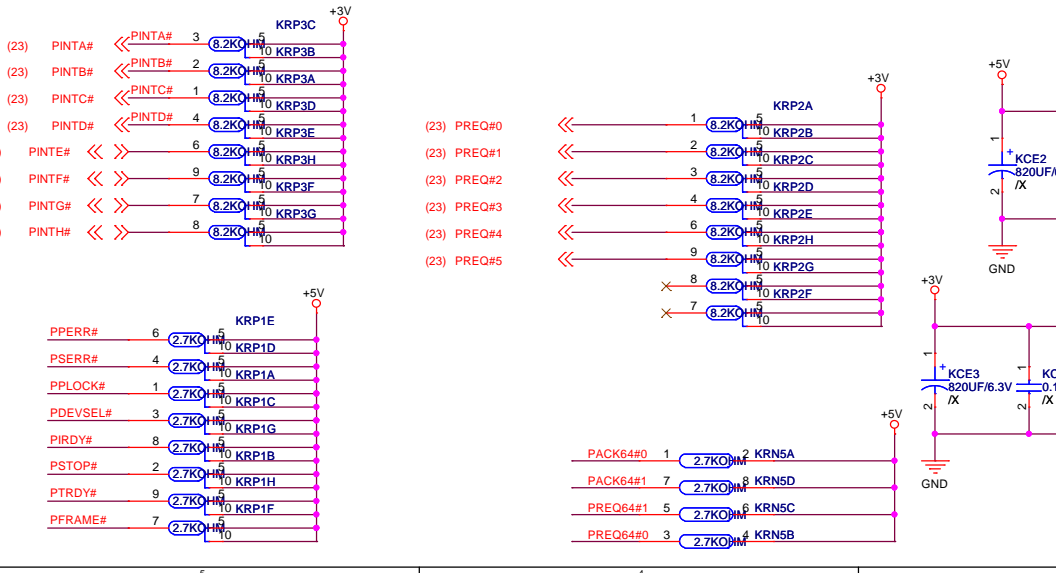
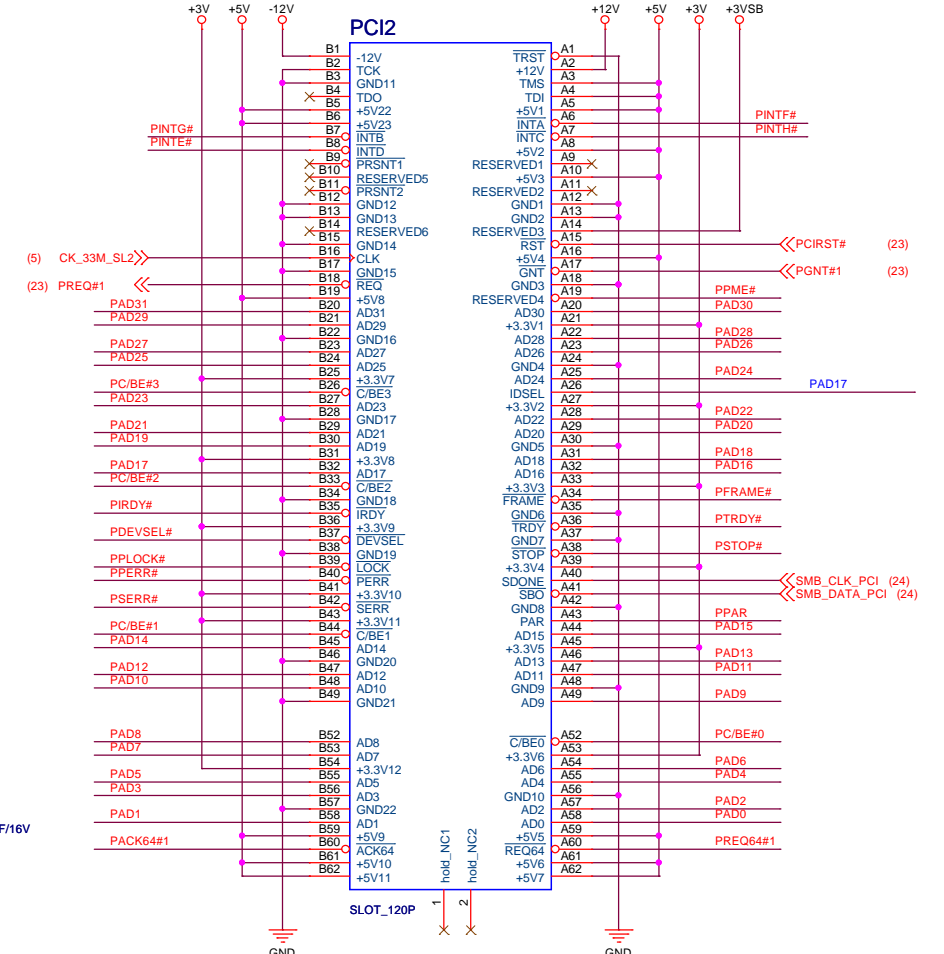
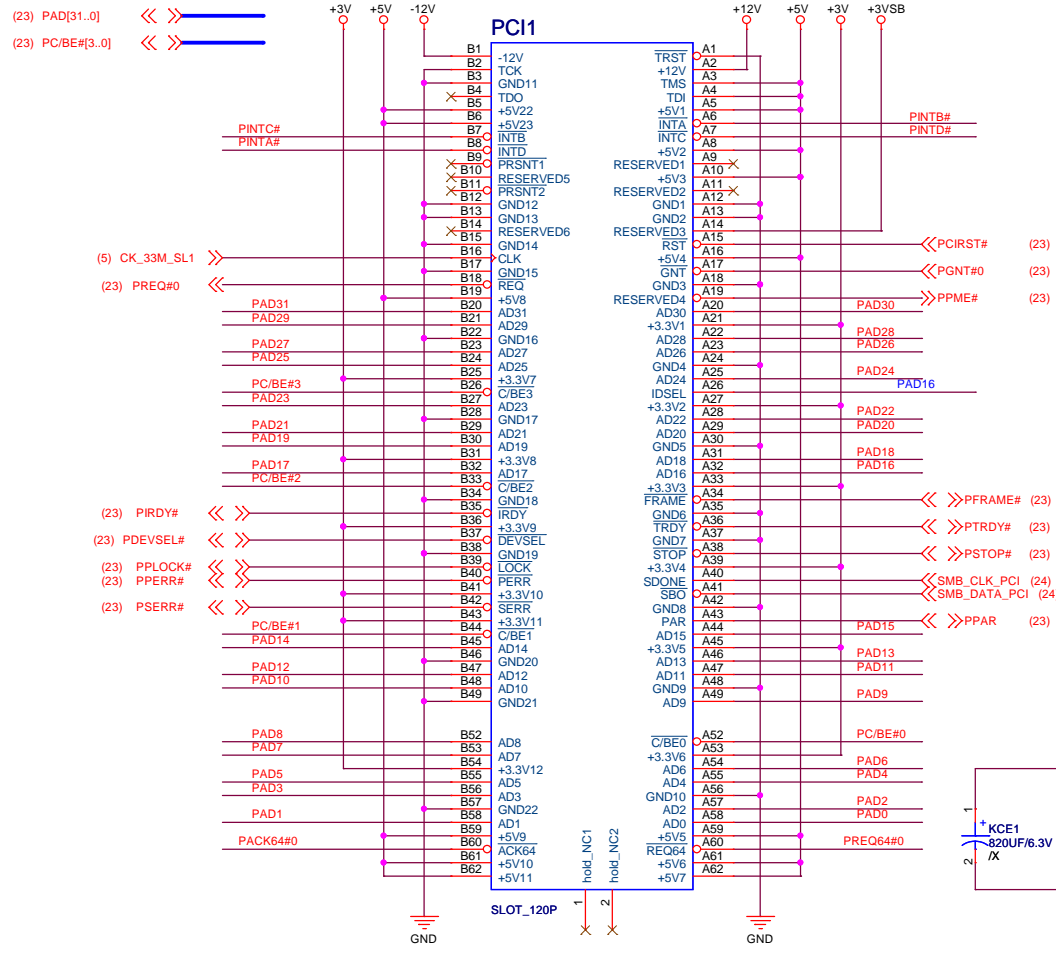
<Variant Name>

Title : ICH7-4	
ASUSTek Computer Inc. Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G
Date: Tuesday, February 02, 2010	Rev 2.00
Sheet 26 of 47	

(5,9,17,19,21,24,41) SMB_CLK
 (5,9,17,19,21,24,41) SMB_DATA



<Variant Name>



PCI DEVICE	PCI REQ/GNT	PCI IDSEL	PCI Clocks	INTA on device mapped to
PCI SLOT 1	REQ/GNT 0	PAD16	CK_PCI_SLOT1	BCDA
PCI SLOT 2	REQ/GNT 1	PAD17	CK_PCI_SLOT2	FGHE
PCI 1394	REQ/GNT 2	PAD18	CK_PCI_LAN	E

<-Variant Name-

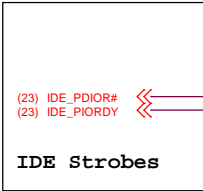
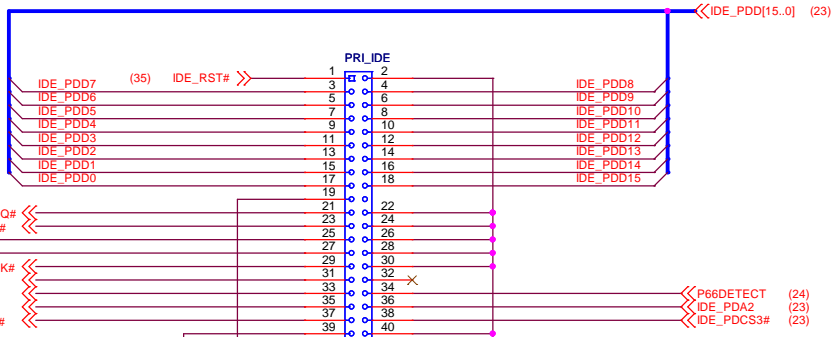
Title : PCI

ASUSTek Computer Inc. **Engineer: SEP_HU**

Size A3	Project Name P5GC-MX 1.00G	Rev 2.00
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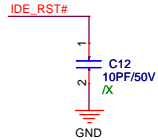
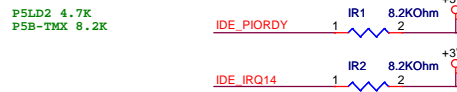
Date: Tuesday, February 02, 2010 Sheet 28 of 47

IDE

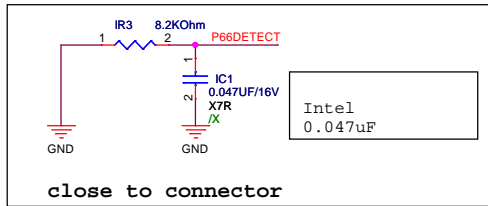


IDE ACTP#
 This pin is open collector output driven by the device. Device has pulled up to +5V. MB need no pull up.

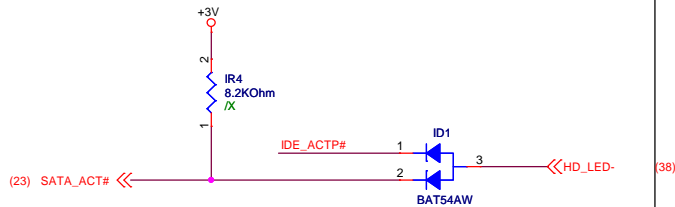
[IR1] Demo Circuit use 4.7k



IR2 P5B-TMX 8.2K
 CRB 10K
 P5PL2 15K

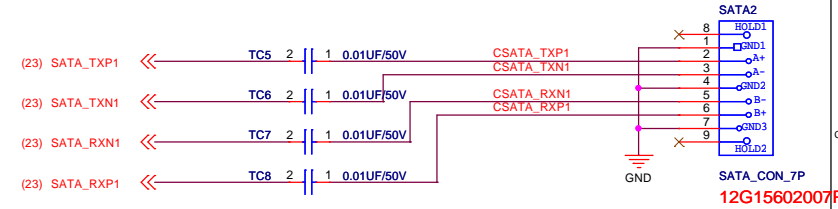
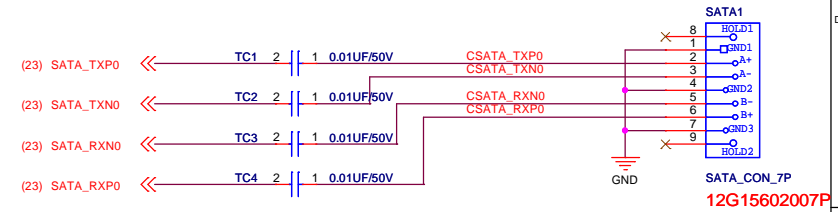


IDE & SATA LED

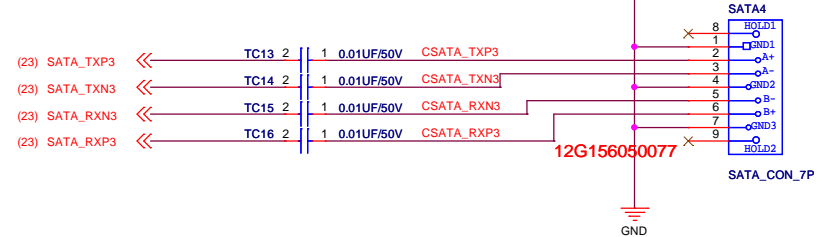
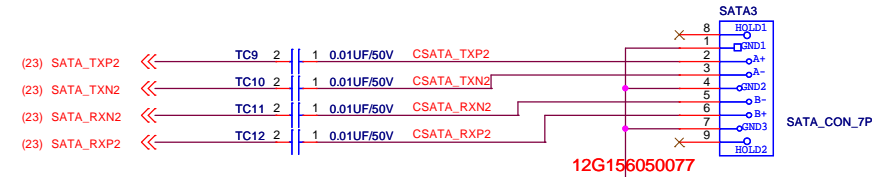


Serial ATA

Color: RED



Color: BLACK



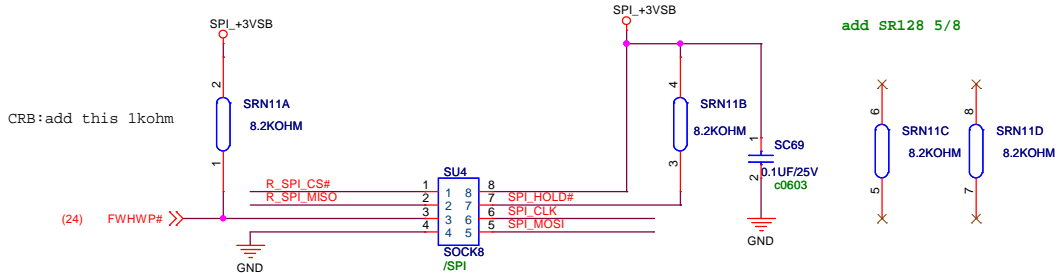
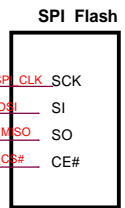
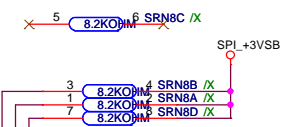
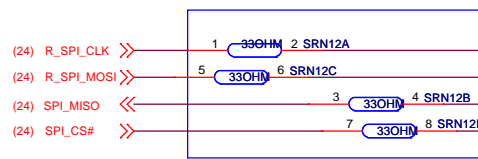
<Variant Name>

ASUS		Title : IDE & SATA	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010	Sheet 29	of 47	



SPI Flash

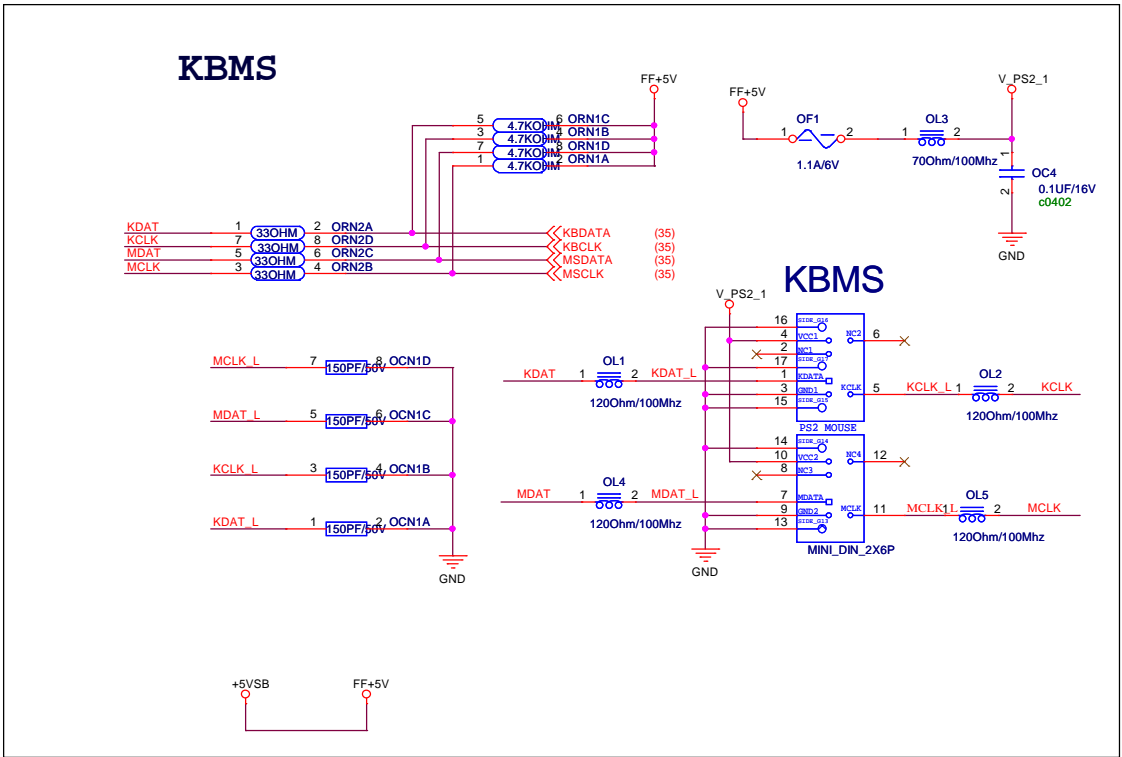
Place near ICH
for Termination use



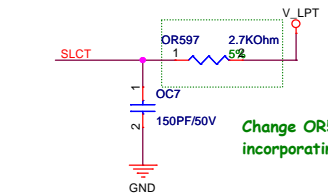
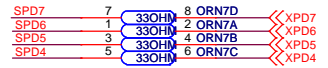
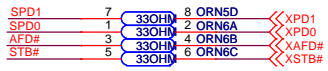
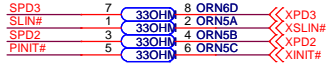
CRB:SR82,SR83,SR84 470HM

CRB:add this 1kohm

add SR128 5/8

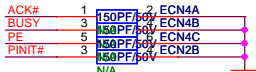
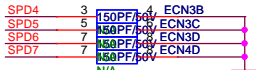
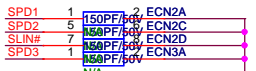
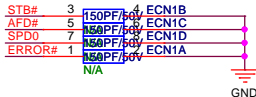
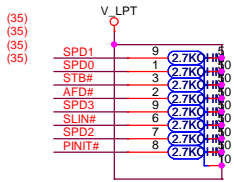
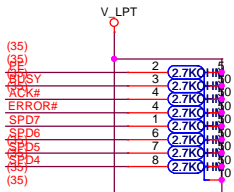


LPT PORT

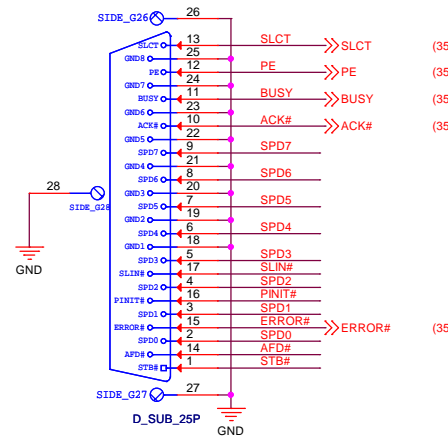


Change OR597 from 5% to 1% for incorporating components

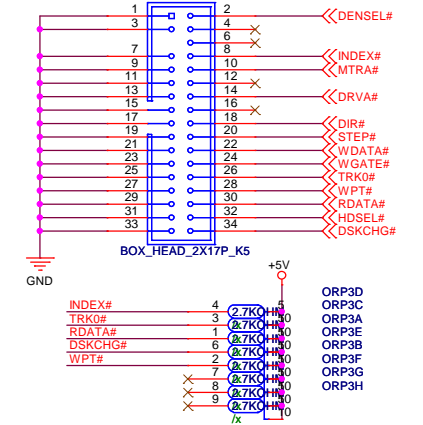
For EMI 150P --> 330P



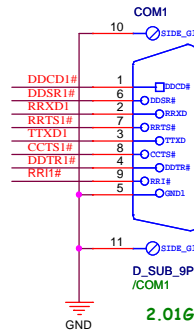
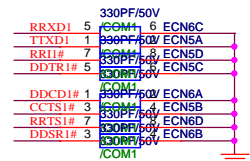
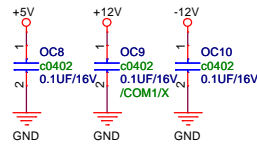
LPT



FLOPPY

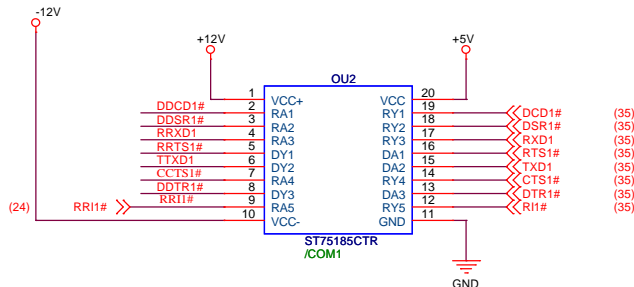


COM1



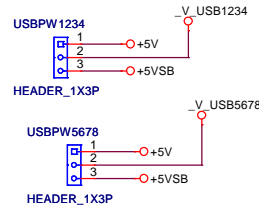
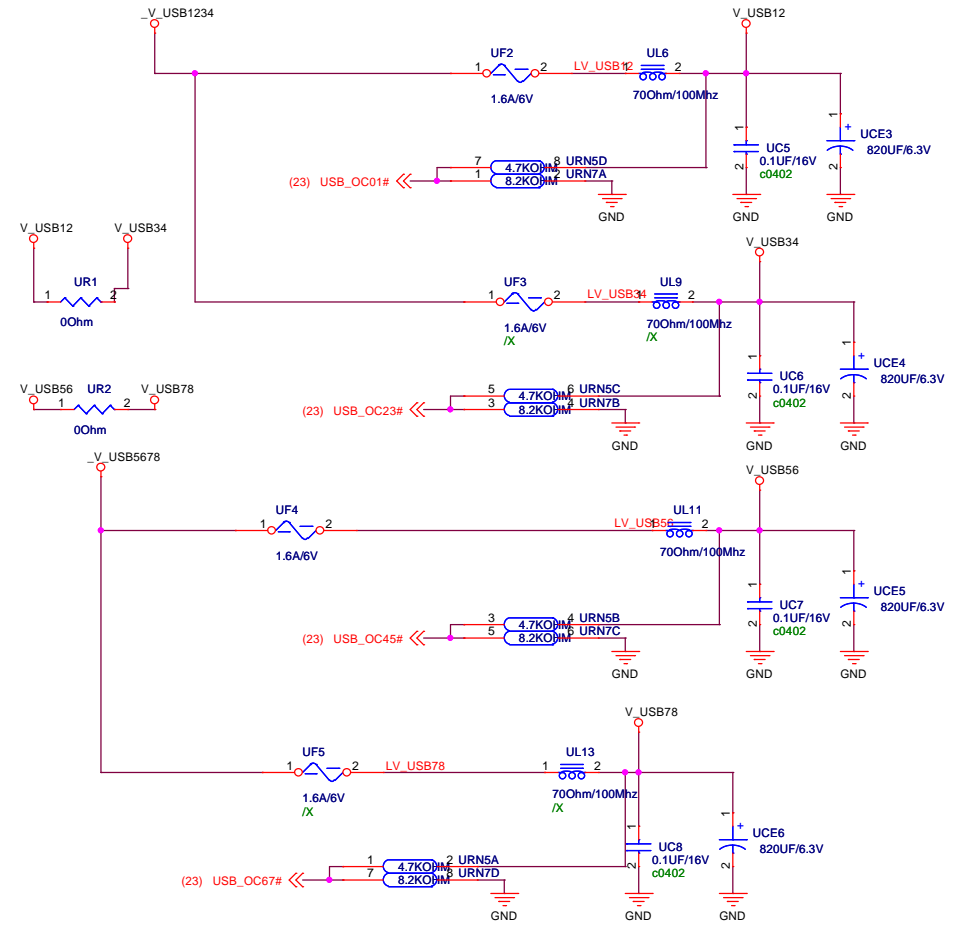
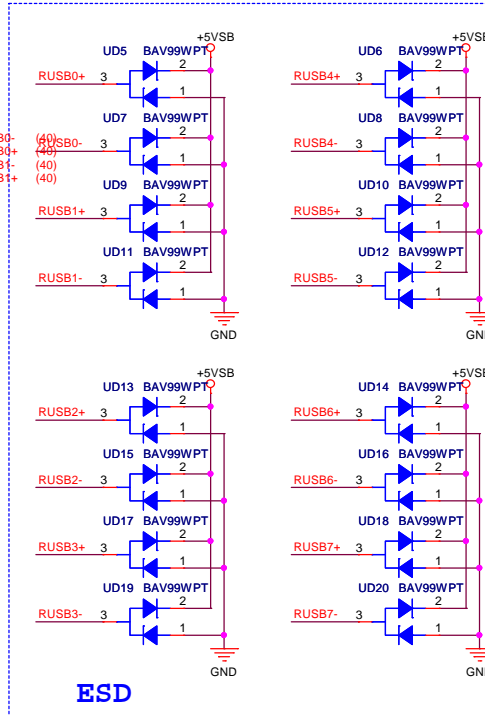
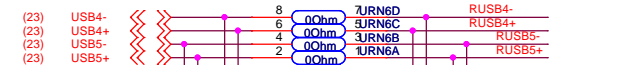
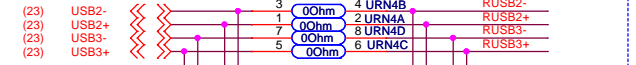
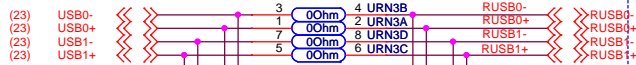
2.01G:change COM1 P/N

1.00 For EMI

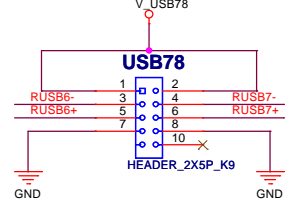
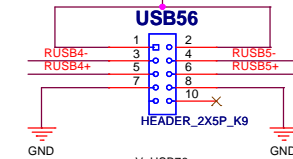
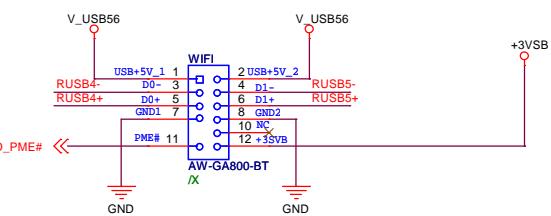


Part number: 04G521011011

Need 3.9ohm resistors?



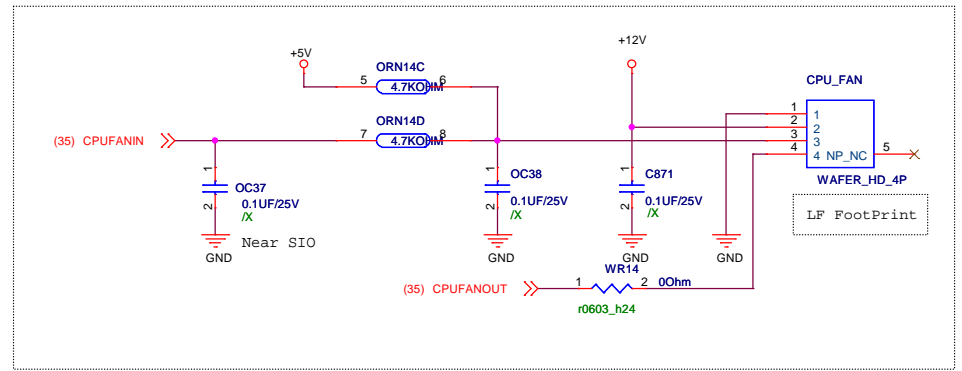
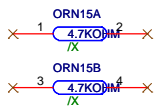
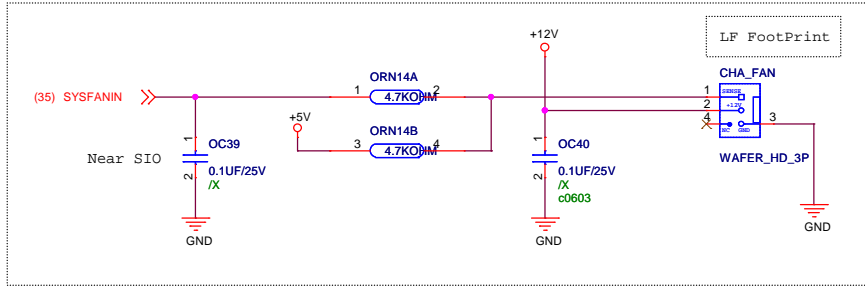
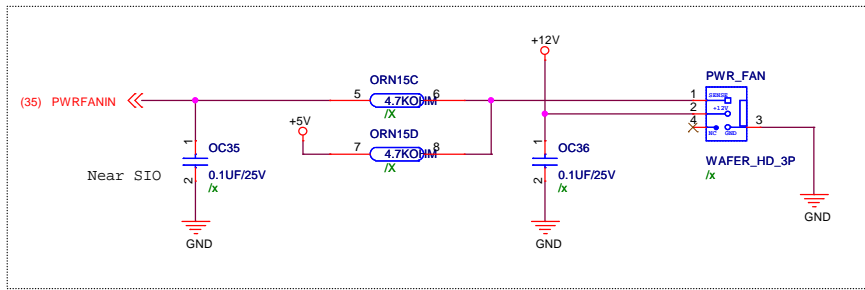
WIFI-G



<Variant Name>

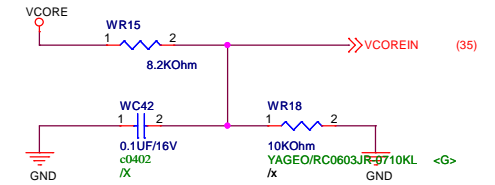
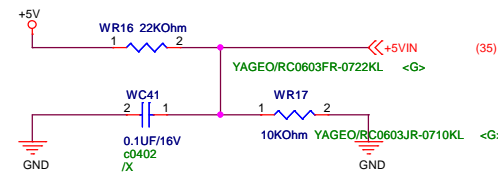
ASUS		Title : USB	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010	Sheet 33	of 47	

04G521011011

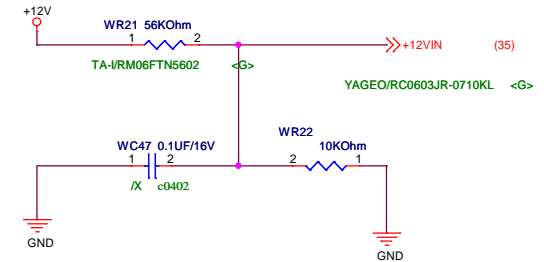
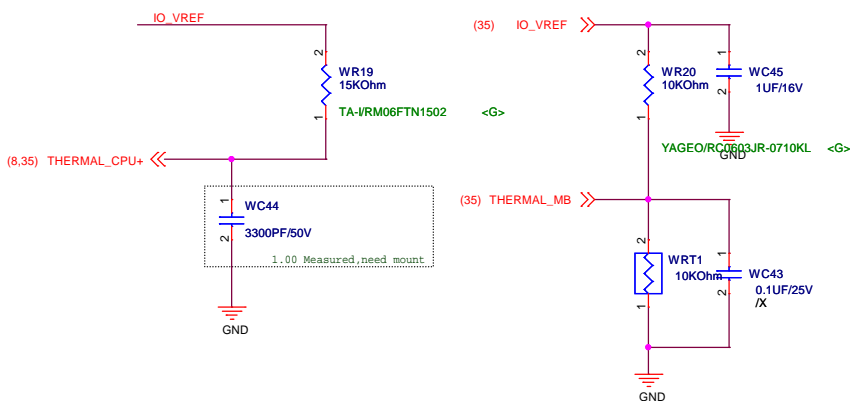


Pin Number	Signal
1	Ground
2	+12V
3	Sense
4	Control

Requirement	Value
Peak fan current draw	1.5A
Average fan current draw	1.1A
Fan start-up current draw	2.2A
Fan start-up current draw maximum duration	1.0 second
Fan header voltage	12V ± 10%

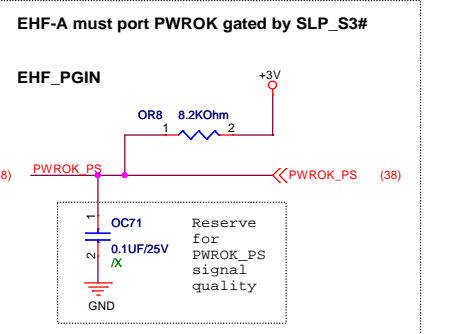
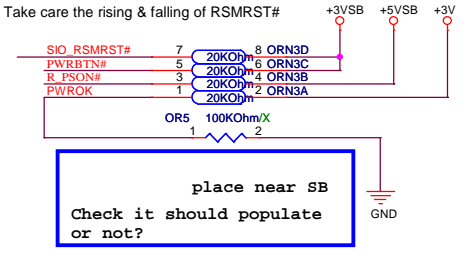
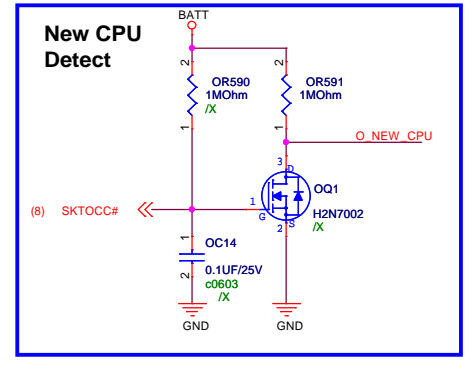
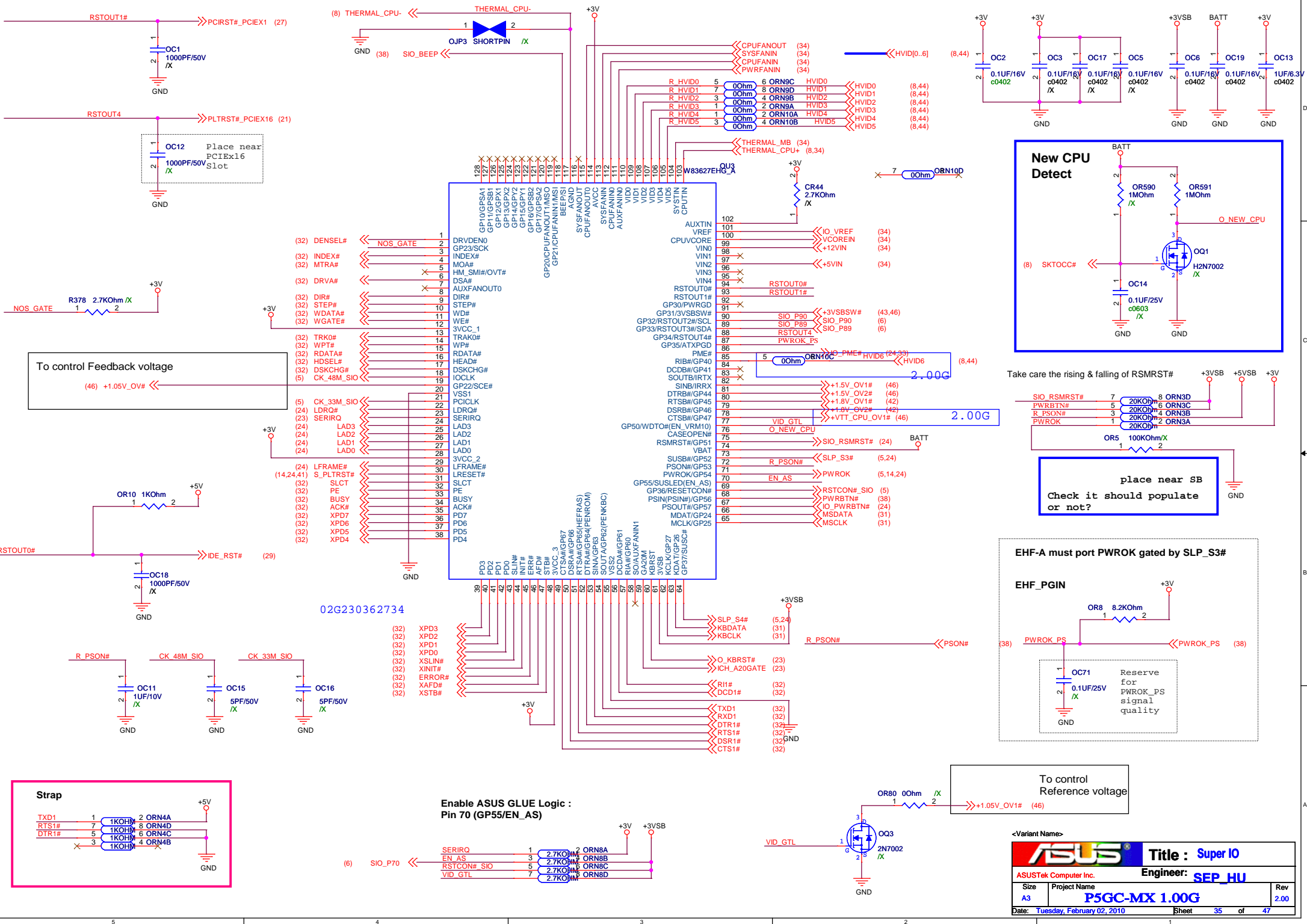


Hardward Mointor



<Variant Name>

ASUS		Title : FAN Control&HW mointor	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010	Sheet 34	of 47	



To control Reference voltage

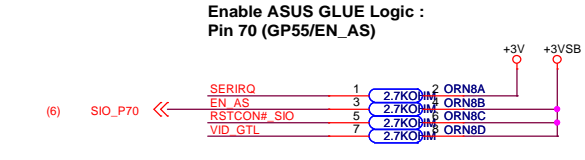
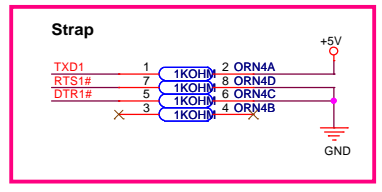
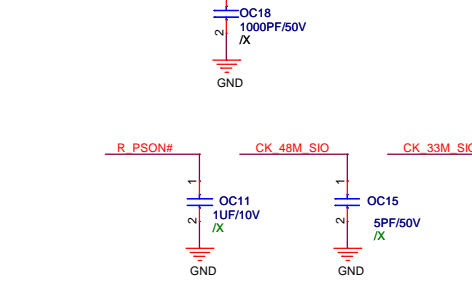
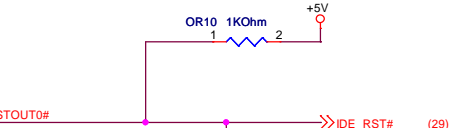
Circuit diagram for reference voltage control. It shows a resistor (OR80, 0Ω) connected to the +3V supply and the +1.05V_OV1# pin (pin 46). A diode (OQ3, 2N7002) is connected between the +1.05V_OV1# pin and ground.

<-Variant Name->

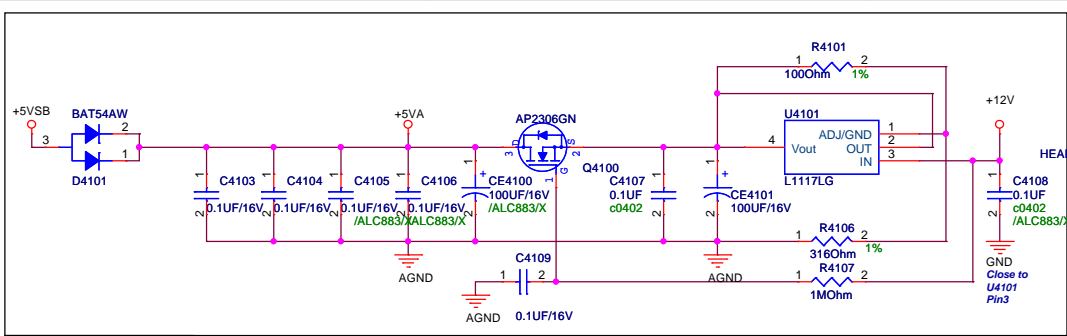
ASUS		Title : Super IO
ASUSTek Computer Inc.		Engineer: SEP_HU
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00
Date: Tuesday, February 02, 2010	Sheet 35	of 47

To control Feedback voltage

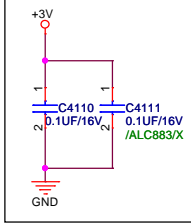
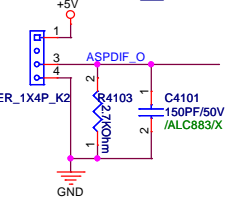
(46) +1.05V_OV#



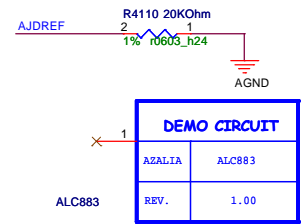
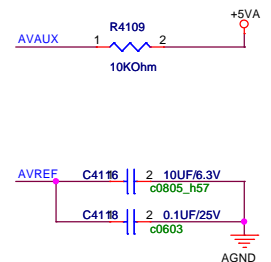
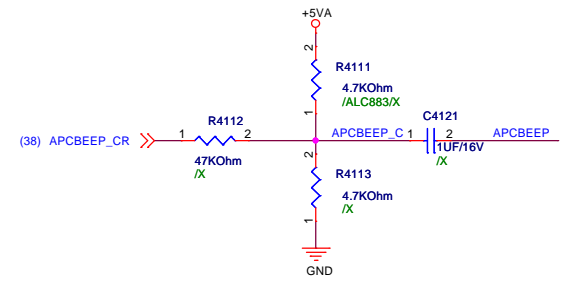
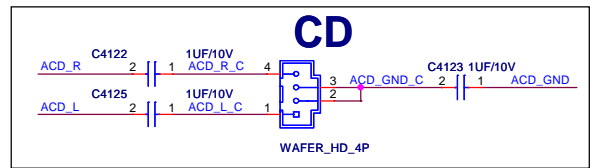
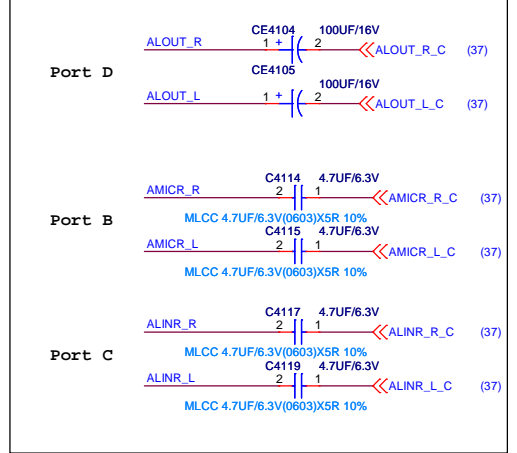
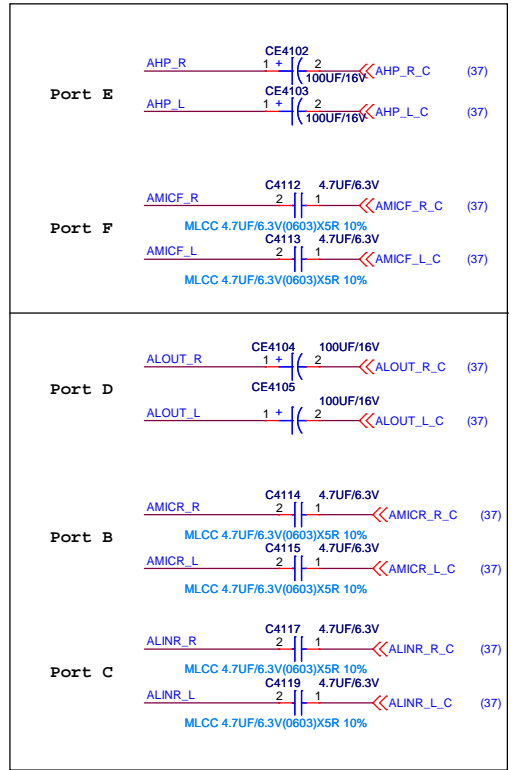
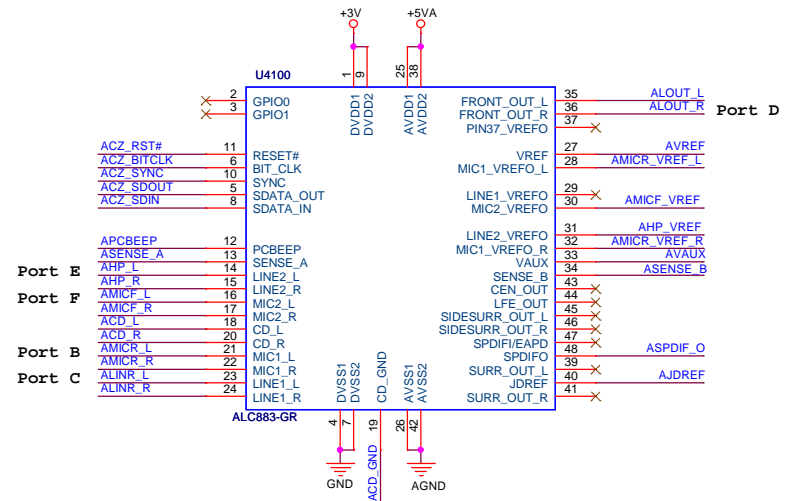
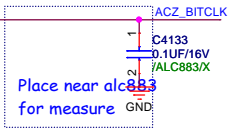
02G230362734



SPDIF_OUT



- (37) AMICR_VREF_L >>> AMICR_VREF_L
- (37) AMICF_VREF >>> AMICF_VREF
- (37) AMICR_VREF_R <<< AMICR_VREF_R
- (37) ASENSE_A <<< ASENSE_A
- (37) ASENSE_B <<< ASENSE_B
- (24) ACZ_RST# >>> ACZ_RST#
- (24) ACZ_SYNC >>> ACZ_SYNC
- (24) ACZ_SDOUT >>> ACZ_SDOUT
- (24) ACZ_SDIN_R >>> ACZ_SDIN
- (24) ACZ_BITCLK >>> ACZ_BITCLK



DEMO CIRCUIT	
AZALIA	ALC883
REV.	1.00

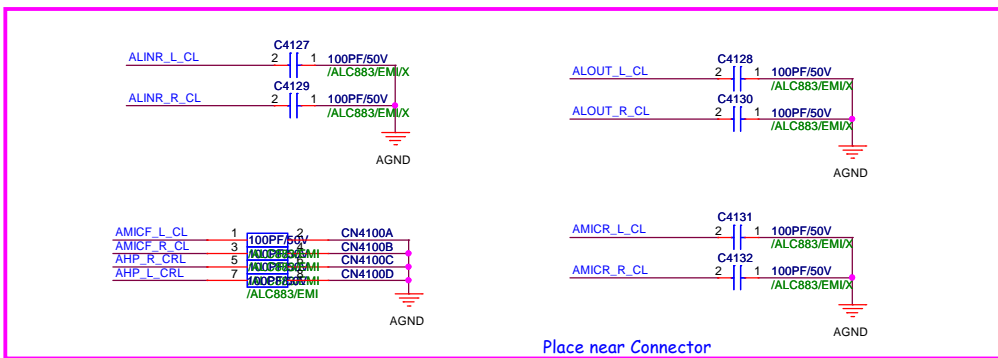
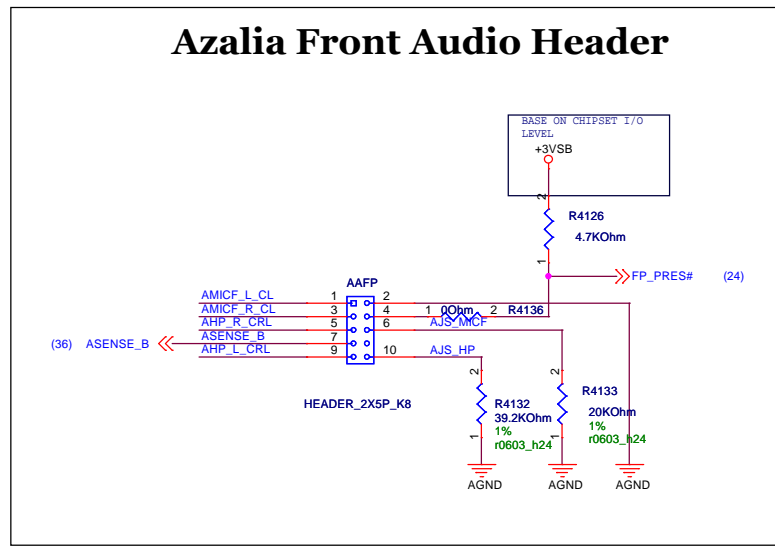
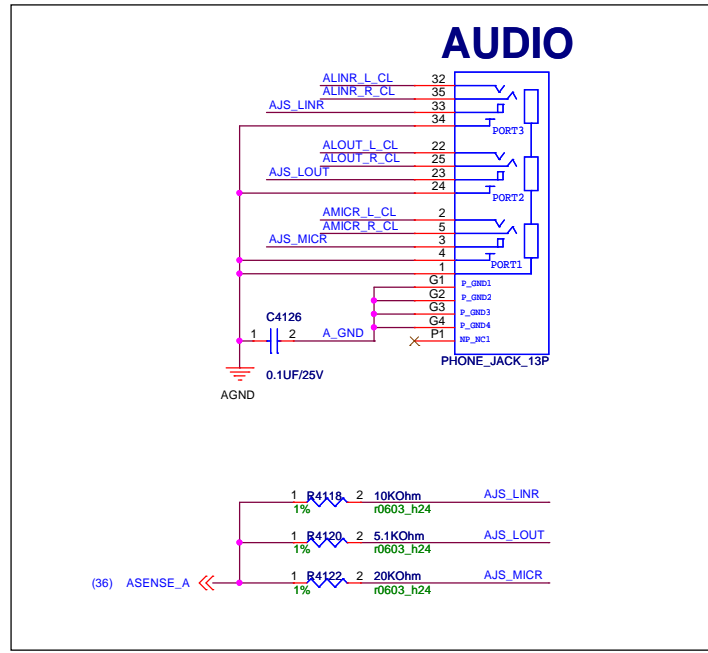
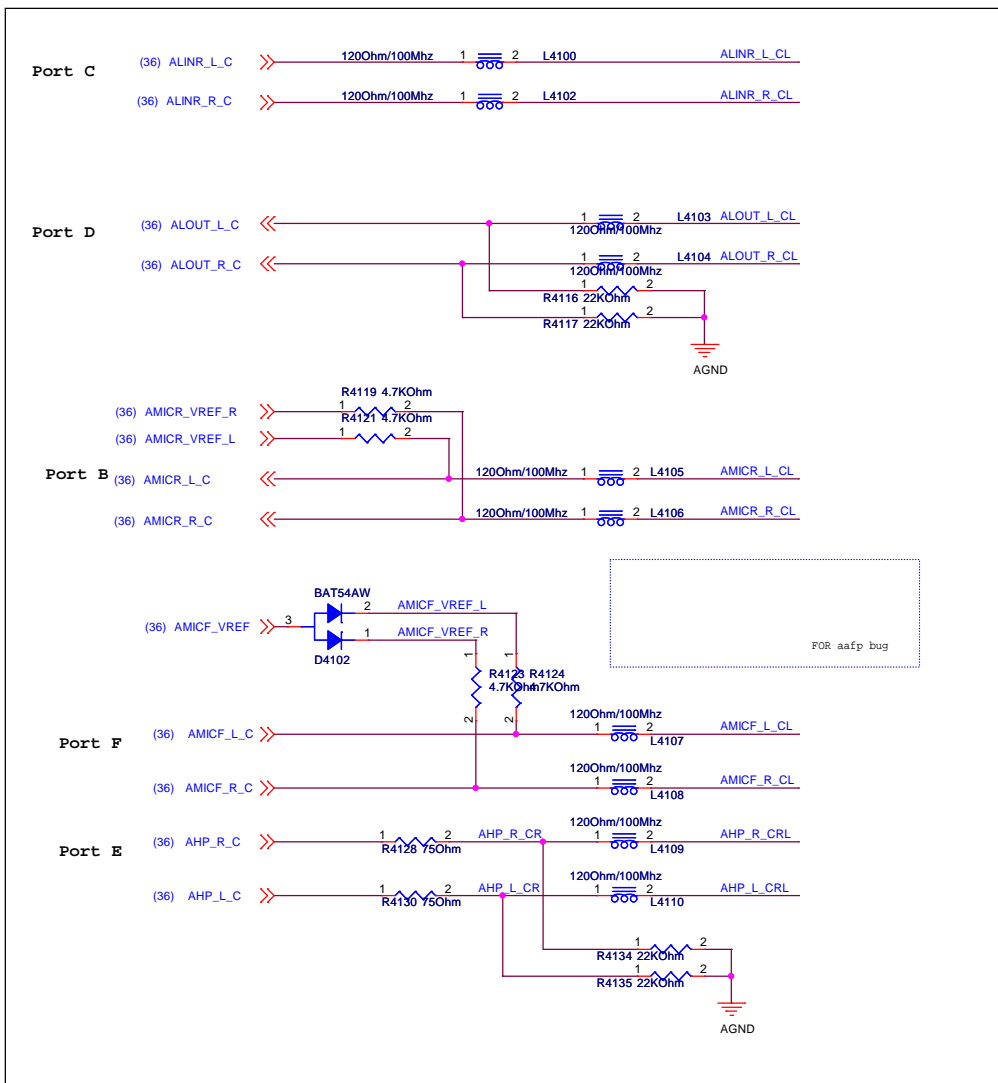
<Variant Name>

Title : AUDIO

ASUSTek Computer Inc. **Engineer: SEP_HU**

Size	Project Name	Rev
A3	P5GC-MX 1.00G	2.00

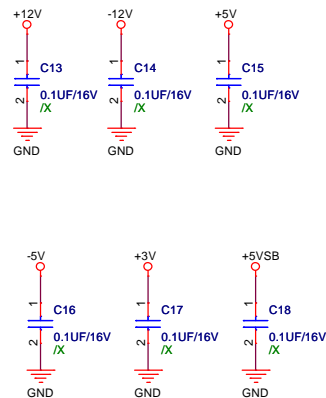
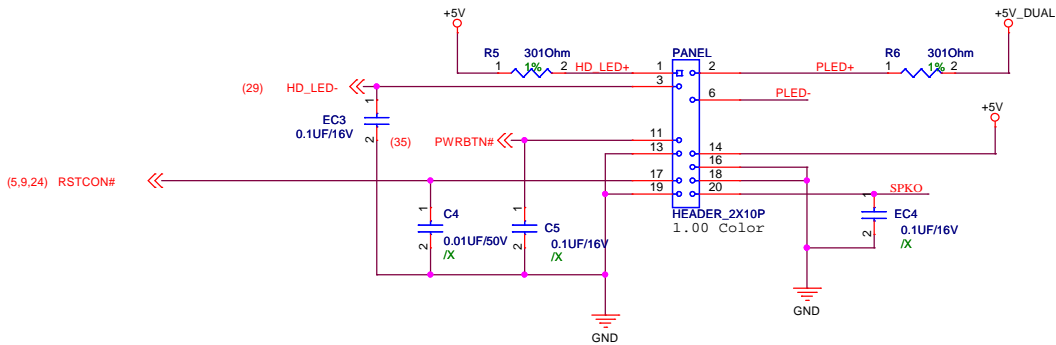
Date: Tuesday, February 02, 2010 Sheet 36 of 47



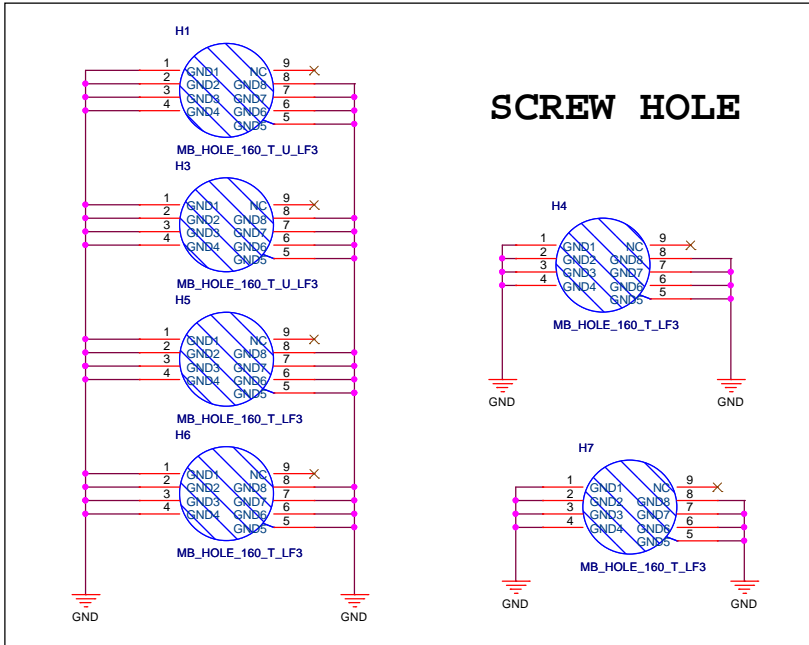
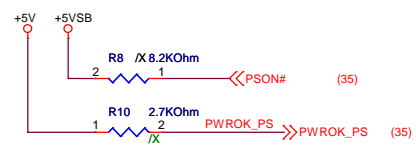
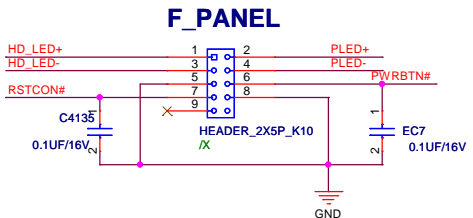
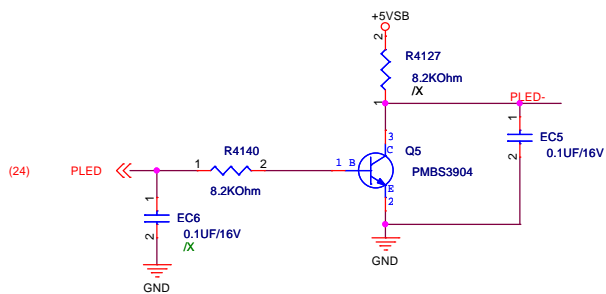
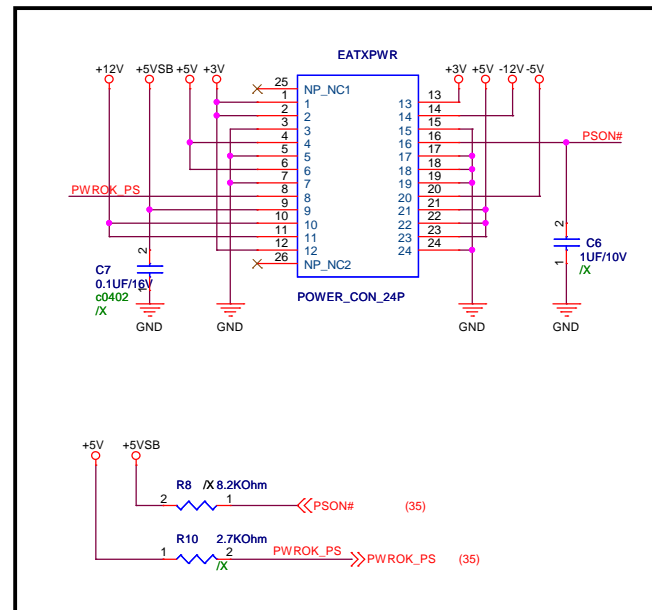
<Variant Name>

ASUS		Title : AUDIO-1*	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name PSGC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010	Sheet	37	of 47

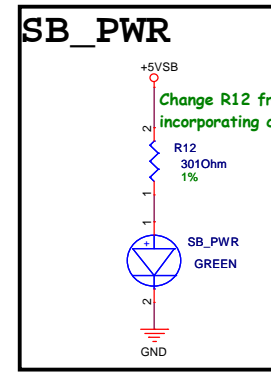
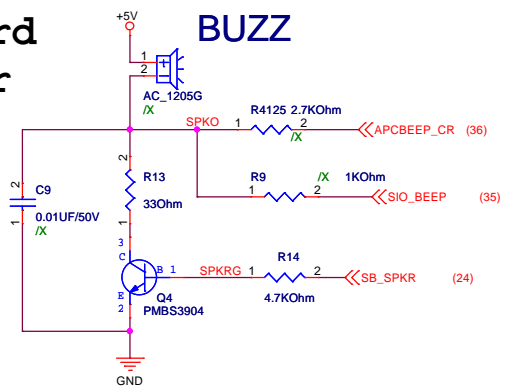
Change R5,R6 from 300ohm to 301ohm for incorporating components



ATX Connector (24 pin)



OnBoard Buzzer

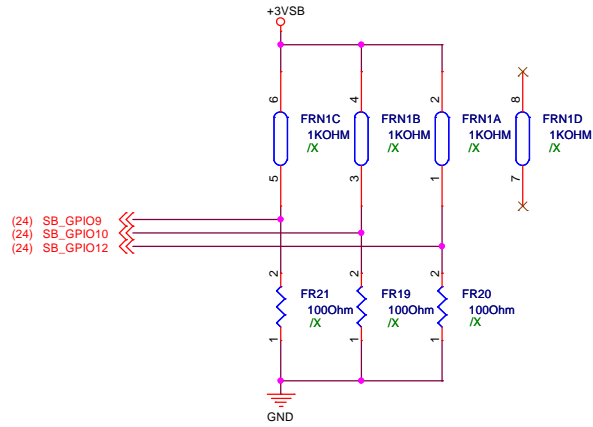


Change R12 from 300ohm to 301ohm for incorporating components

<Variant Name>

ASUS		Title : Front Panel	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010	Sheet 38	of 47	

1.00 WE# Write Enable



<Variant Name>

ASUS		Title : FWH	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010		Sheet 39	of 47

5

4

3

2

1

D

D

C

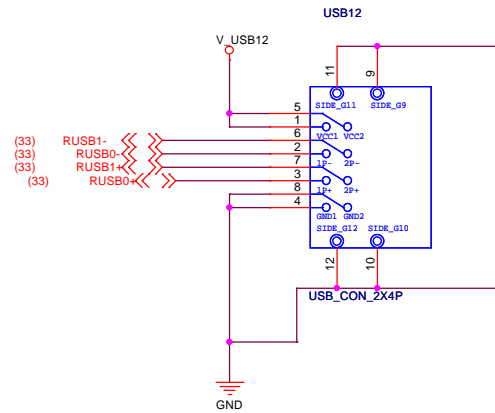
C

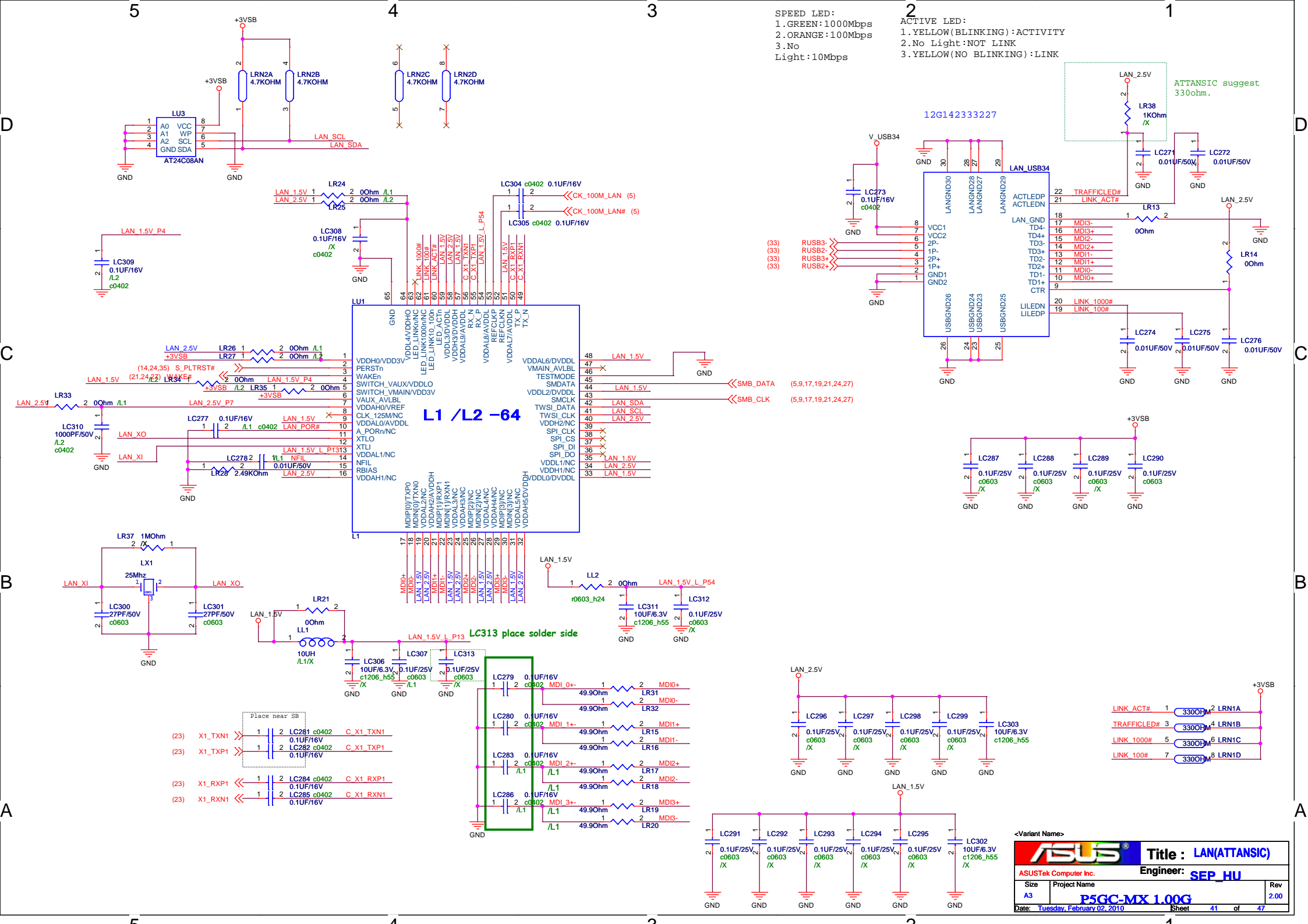
B

B

A

A





SPEED LED:
 1. GREEN:100Mbps
 2. ORANGE:100Mbps
 3.No Light:10Mbps

ACTIVE LED:
 1. YELLOW (BLINKING):ACTIVITY
 2.No Light:NOT LINK
 3. YELLOW(NO BLINKING):LINK

ATTANSIC suggest
 330ohm.

L1 /L2 -64

LC313 place solder side

Place near SB

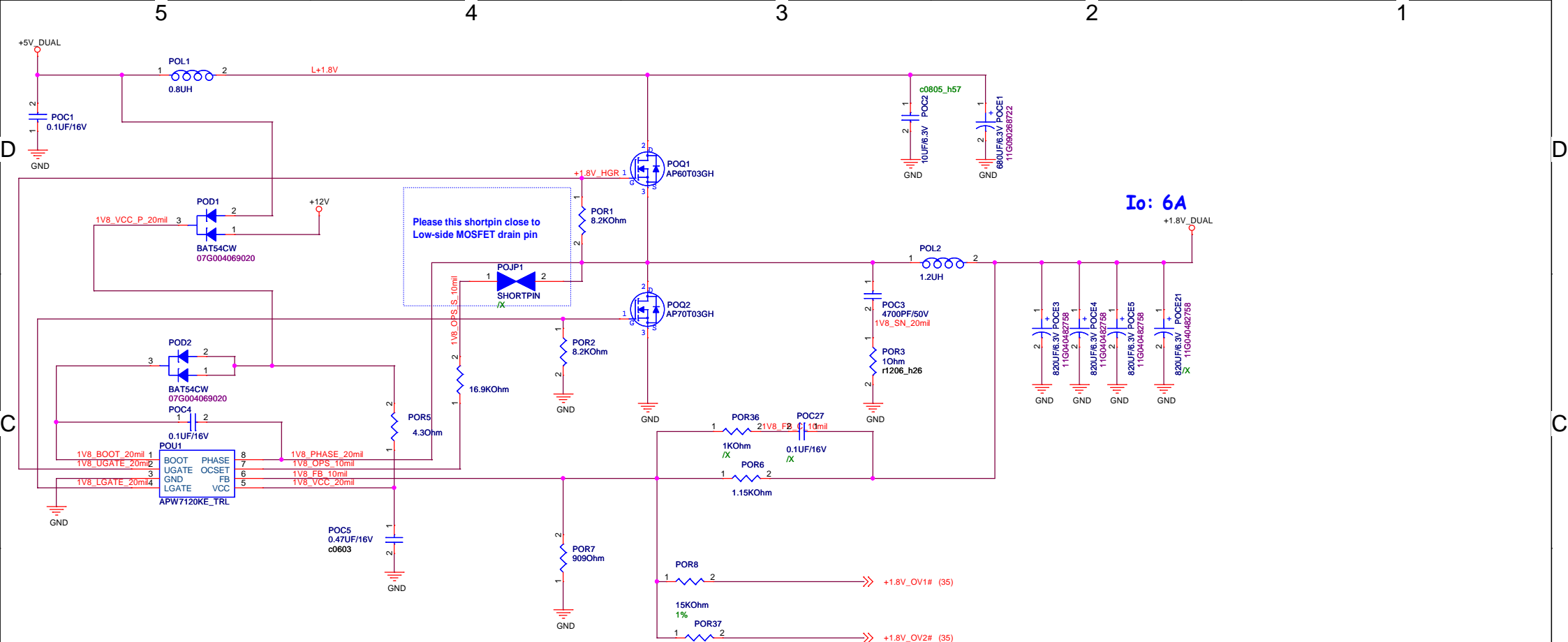
- (23) X1_TXN1 <--> 1 2 LC281 c0402 C X1_TXN1
- (23) X1_TXP1 <--> 1 2 LC282 c0402 C X1_TXP1
- (23) X1_RXN1 <--> 1 2 LC284 c0402 C X1_RXN1
- (23) X1_RXP1 <--> 1 2 LC285 c0402 C X1_RXP1

<Variant Name>

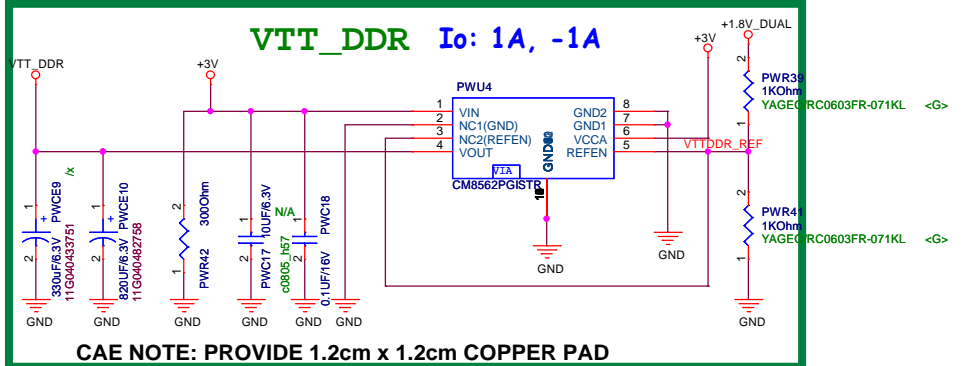
ASUS Title: LAN(ATTANSIC)
 ASUSTek Computer Inc. Engineer: SEP_HU

Size	Project Name	Rev
A3	P5GC-MX 1.00G	2.00

Date: Tuesday, February 02, 2010 Sheet 41 of 47

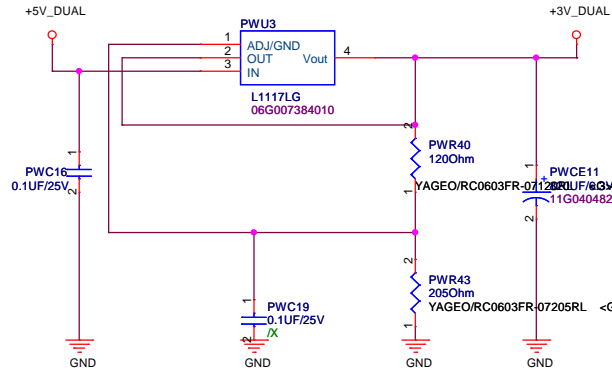


+1.8V_OV3#	+1.8V_OV2#	+1.8V_OV1#	+1.8V_DUAL
1	1	1	+1.812V
1	1	0	+1.85V
1	0	1	+1.904V
1	0	0	+1.942V
0	1	1	+1.992V
0	1	0	+2.030V
0	0	1	+2.084V
0	0	0	+2.122V

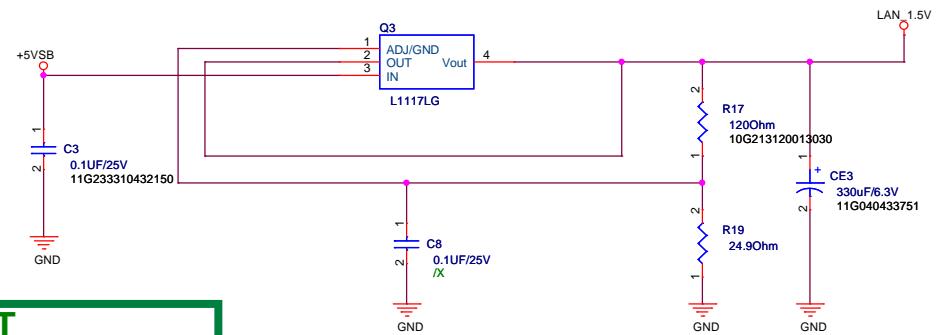
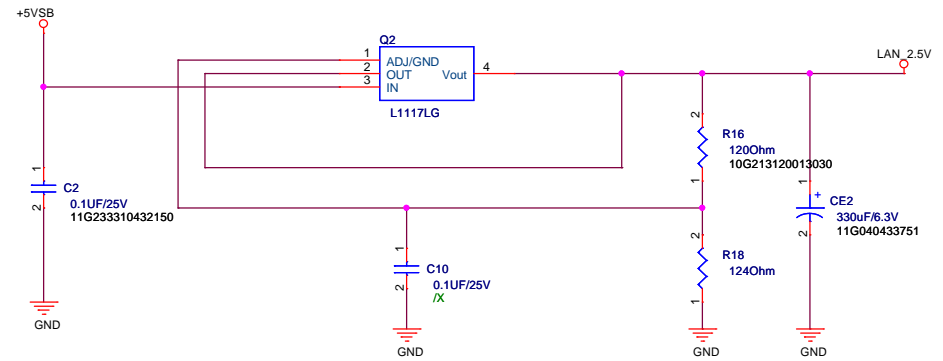


CAE NOTE: PROVIDE 1.2cm x 1.2cm COPPER PAD FOR DPAK(TO252) LET TjA OF 20C/W FOR 1.2A ON DDR VTT

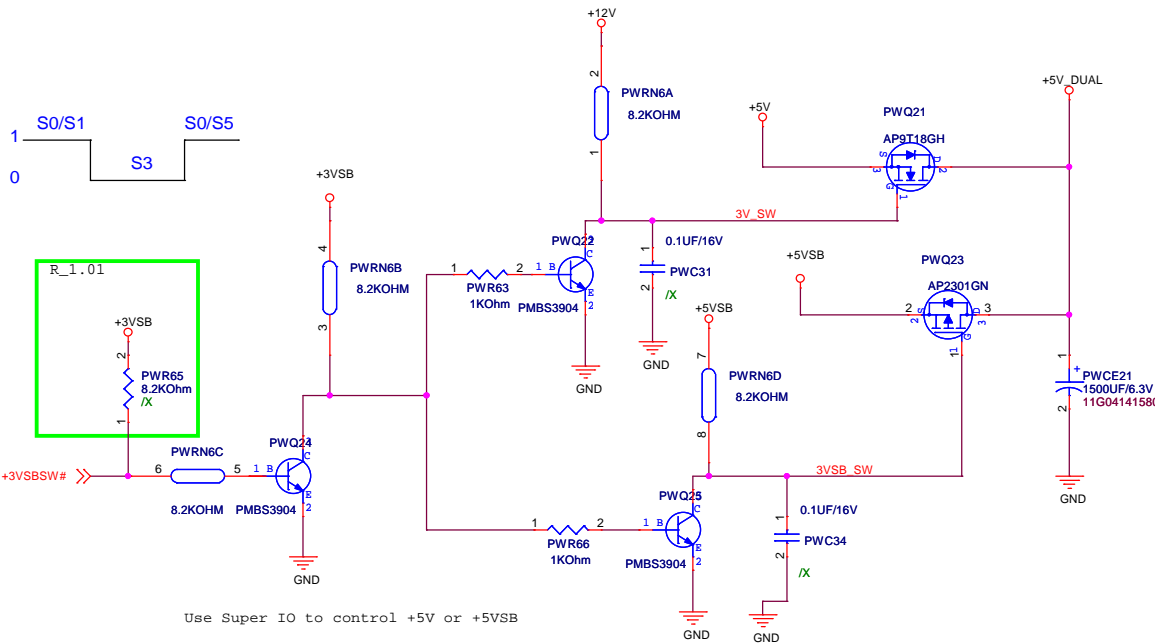
+5V_Dual ==>+3V_Dual for Clock gen



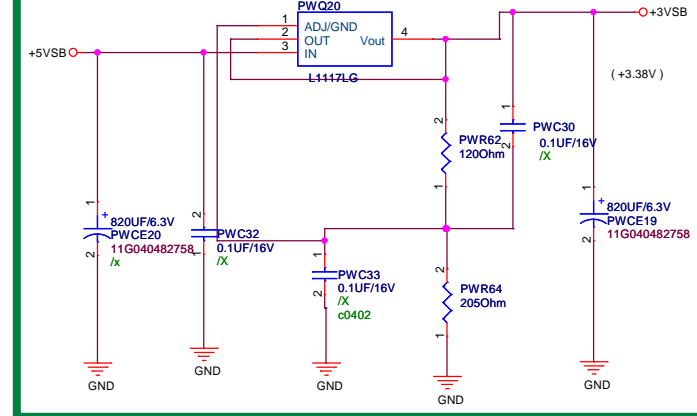
+5VSB ==>LAN_2.5V /0.3A



+5V_DUAL VOLTAGE SWITCH & POWER CIRCUIT

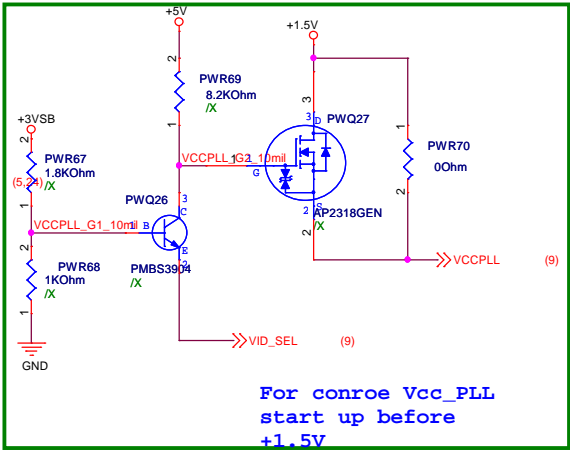
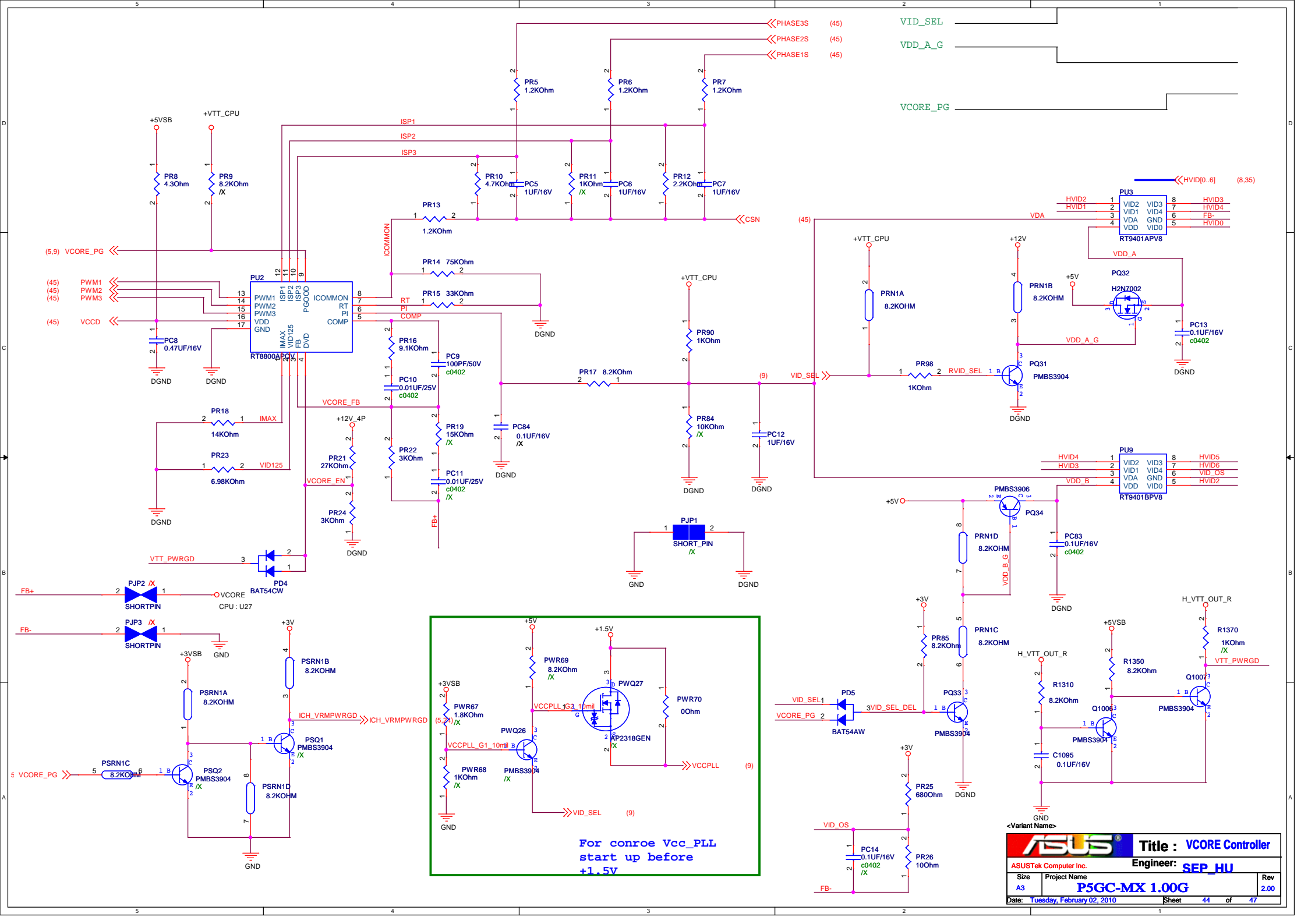


+5VSB ==>+3VSB Io: 2A



<Variant Name>

ASUS		Title : 3V_DYAL&+3VSB&+5VDUAL&LAN	
ASUSTek Computer Inc.		Engineer: SEP_HU	
Size A3	Project Name P5GC-MX 1.00G	Rev 2.00	
Date: Tuesday, February 02, 2010		Sheet 43 of 47	



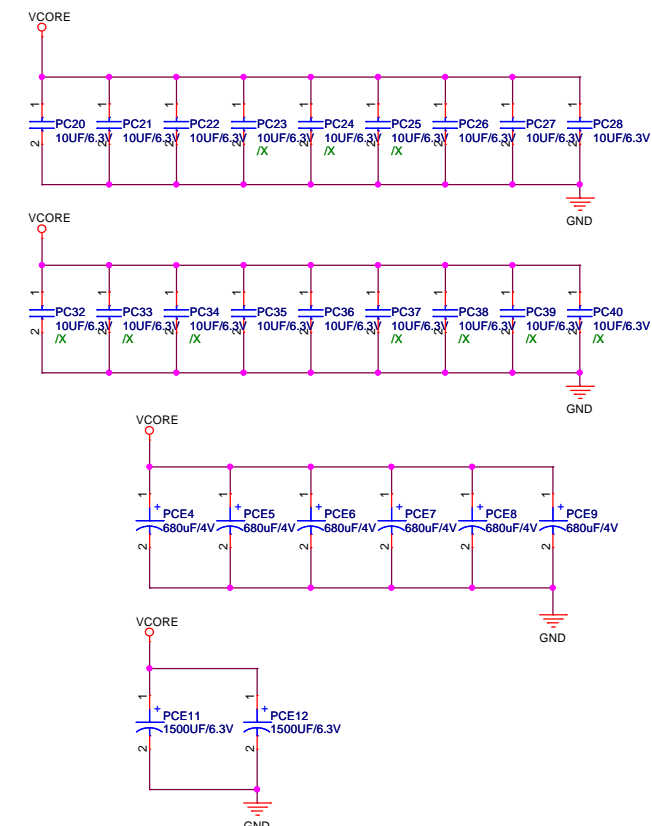
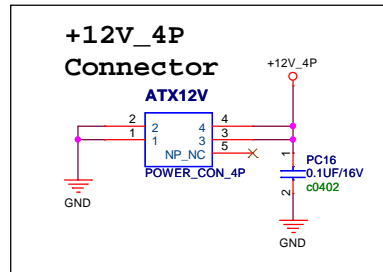
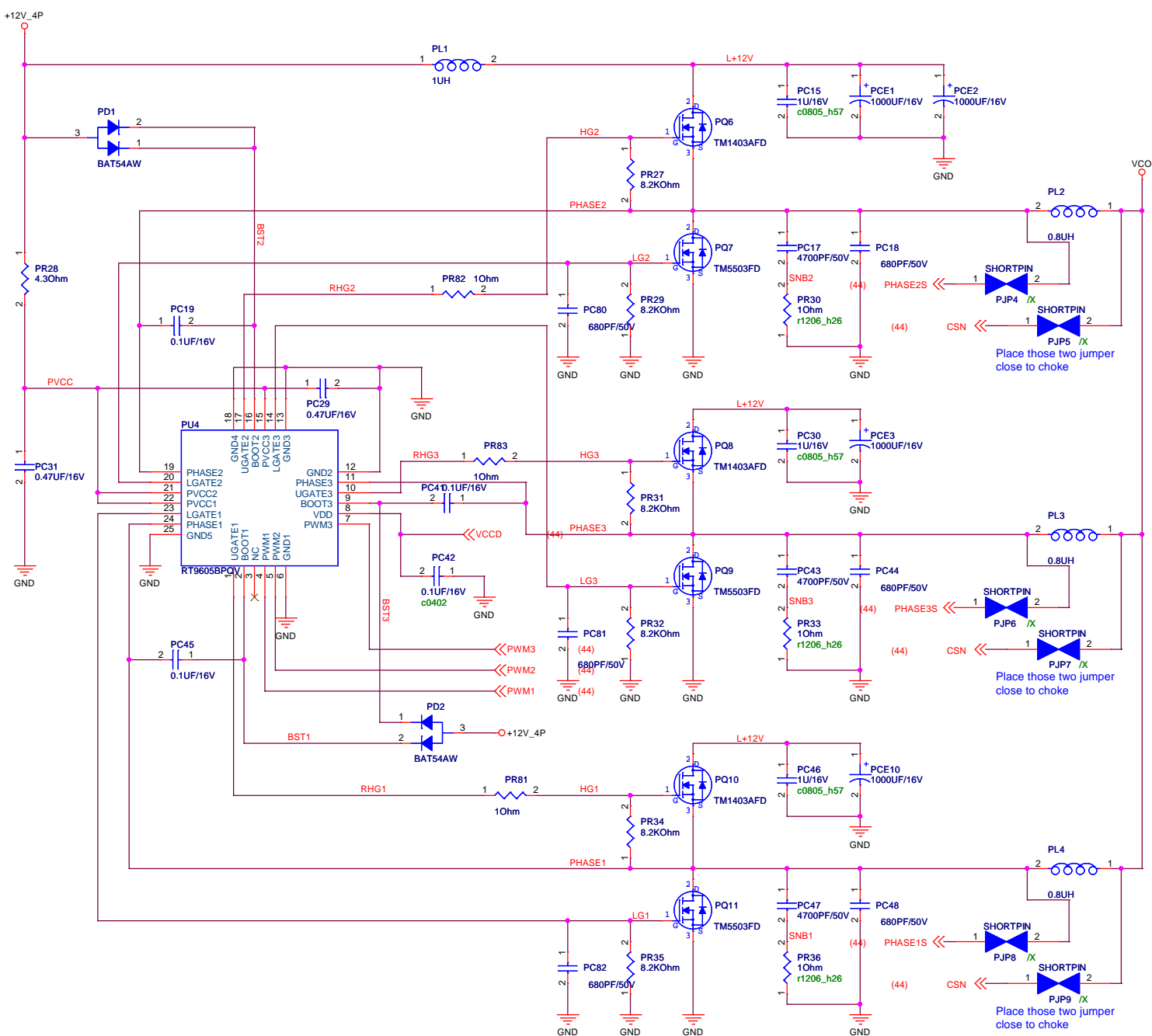
<Variant Name>

Title : VCORE Controller

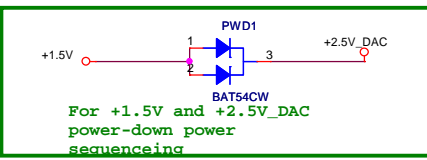
ASUSTek Computer Inc. Engineer: **SEP_HU**

Size	Project Name	Rev
A3	P5GC-MX 1.00G	2.00

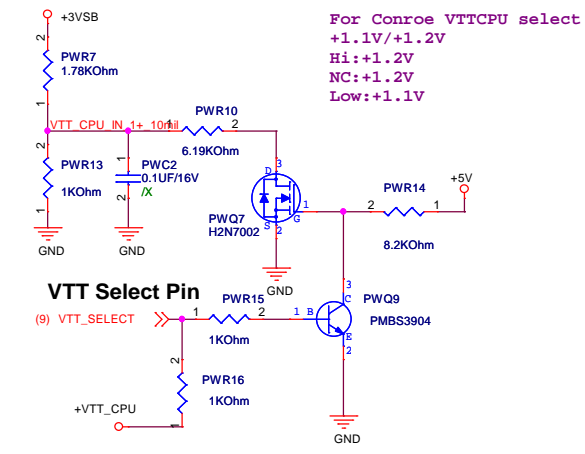
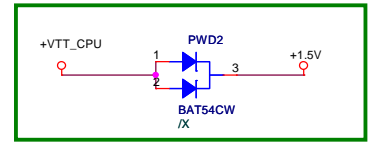
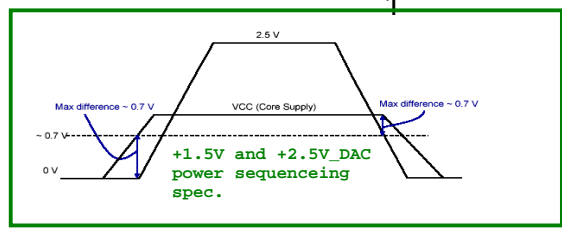
Date: Tuesday, February 02, 2010 Sheet 44 of 47



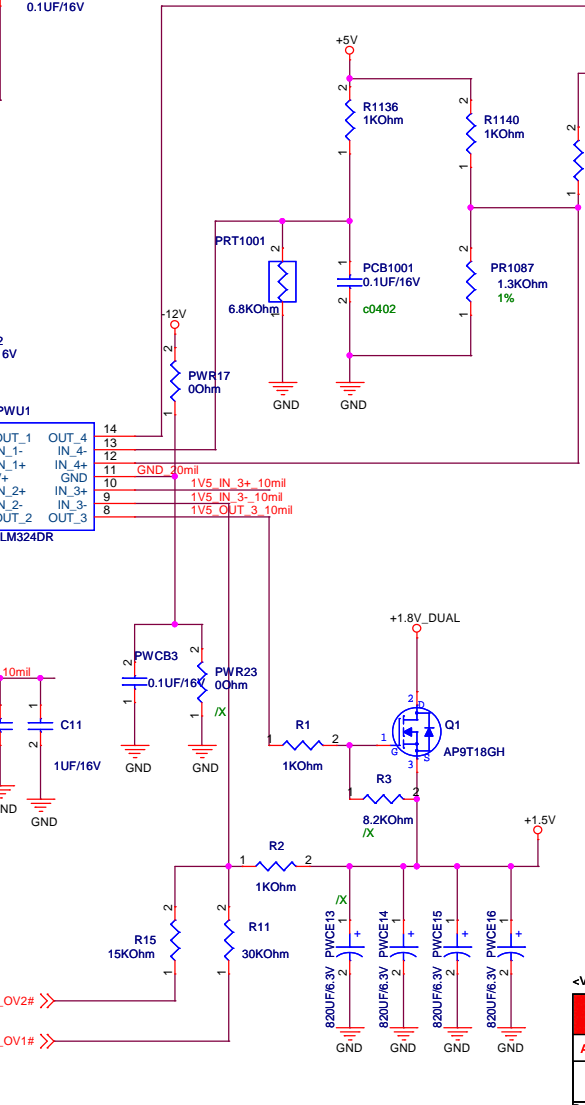
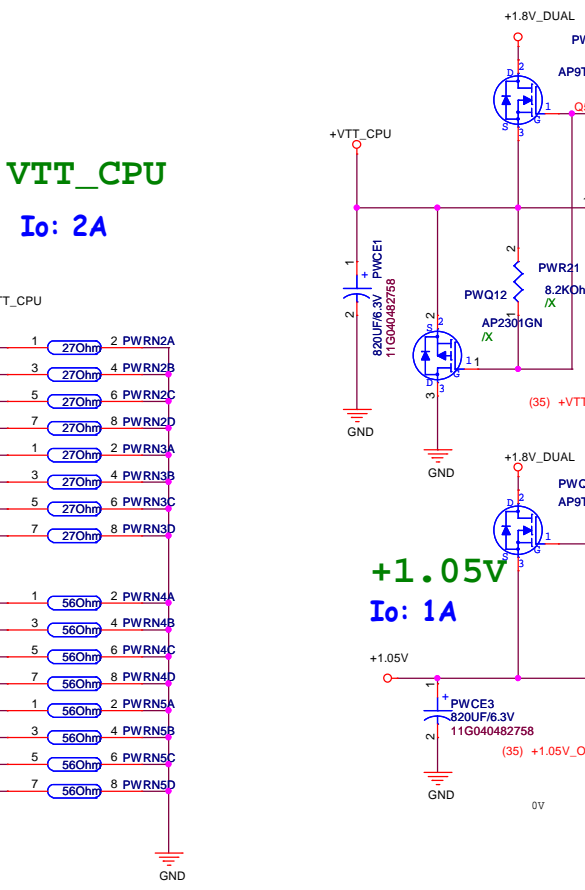
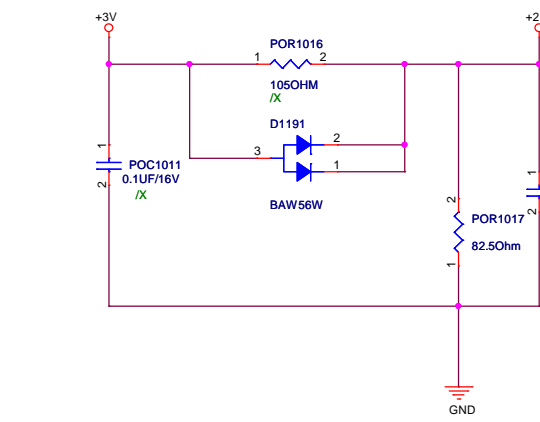
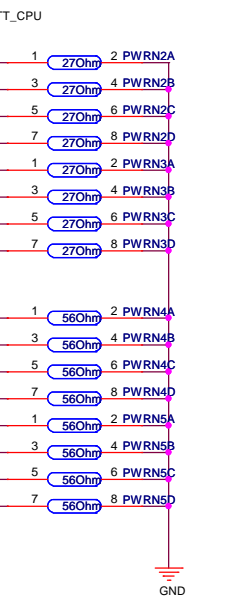
+VTT_CPU_OV1#	+VTT_CPU
1	+1.217V
0	+1.299V



+2.5V_DAC
Io: 70mA



VTT_CPU
Io: 2A



+1.5V_OV2#	+1.5V_OV1#	+1.5V
1	1	+1.5V
1	0	+1.55V
0	1	+1.6V
0	0	+1.65V

+1.05V_OV#	+1.05V	+1.05V_OV1#	+1.05V
1	+1.057V	0	+1.052V
0	+1.215V	1	+1.194V

