

Features

- 16-pin SOP package

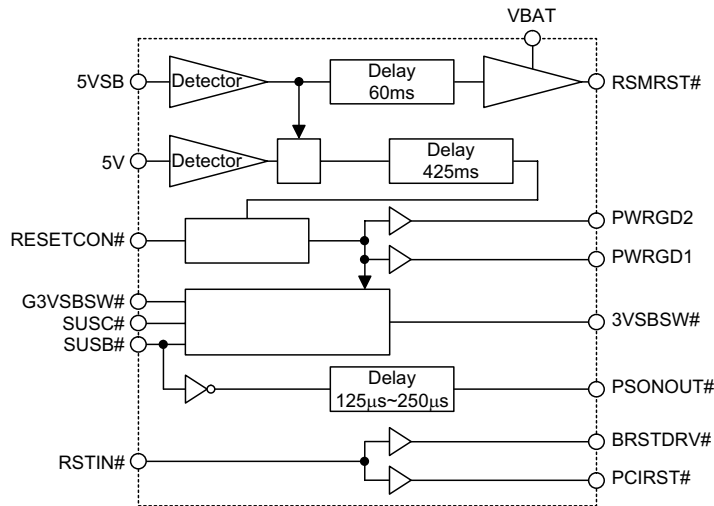
General Description

This ASIC is designed to reduce the discrete logics used in the mother board. With this device, the mother board's reliability is increased, while its size and cost are reduced.

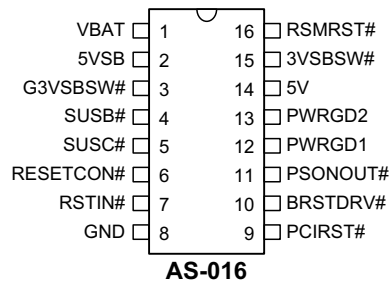
The function of this device is to regulate the power control of the mother board. The RSMRST# signal is used to identify the status of the 5VSB. The 3VSBSW# signal

is used to select the 3.3V power source. The PWRGD1 and PWRGD2 signals are used to indicate whether the power is OK or not. The PSONOUT# signal is used to control the On and Off of the power supply. The BRSTDRV# and PCIRST# signals are used to reset the devices.

Block Diagram



Pin Assignment



Pin Description

Pin No.	Pin Name	I/O Spec.	Description
Power & reset control: 8 pins			
16	RSMRST#	@VDD=VBAT (3.3V) O/P spec: NMOS OD I _{OL} =4mA/0.4V Pull-high 5V tolerance	This is the +5VSB power good signal, with Schmitt trigger input, the high threshold is 4V±0.2V, and the low threshold is 3.5V±0.2V
6	RESETCON#	@VDD=5VSB I/P spec: TTL input Internal pull-high 100kΩ to 5VSB	This pin connects to the reset button, and also to the other reset source on the motherboard. Low reset chip (5V logic) PWRGD follows with RESETCON
12	PWRGD1	@VDD=5VSB O/P spec: NMOS OD I _{OL} =10mA/0.4V	5V>4volt, wait for 425ms then rising PWRGD to high 5V<3.5volt, then falling PWRGD to low This pin also follows with RESETCON
13	PWRGD2	@VDD=5VSB O/P spec: NMOS OD I _{OL} =10mA/0.4V	5V>4volt, wait for 425ms then rising PWRGD to high 5V<3.5volt, then falling PWRGD to low This pin also follows with RESETCON
7	RSTIN#	@VDD=VDD5VSB I/P spec: TTL input Internal pull-high 100kΩ to 5VSB	Original Reset signal from chipset
9	PCIRST#	@VDD=VDD5VSB O/P spec: CMOS O/P I _{OL} =16mA/0.4V I _{OH} =16mA/4.5V	Reset for add-on PCI card
10	BRSTDRV#	@VDD=VDD5VSB O/P spec: CMOS O/P I _{OL} =16mA/0.4V I _{OH} =16mA/4.5V	Reset for IDE
11	PSONOUT#	@VDD=5VSB O/P spec: NMOS OD I _{OL} =10mA/0.4V	PSON# signal to power supply PSONOUT#= NOT (SUSB#) Propagation delay=125μs~250μs
Suspend control: 4 pin			
4	SUSB#	@VDD=5VSB I/P spec: TTL input Internal pull-high 100kΩ to 5VSB	SUSB# signal from Intel/VIA South Bridge. High at S0~S2 and turn low when S3/S4/S5
5	SUSC#	@VDD=5VSB I/P spec: TTL input Internal pull-high 100kΩ to 5VSB	SUSC# signal from Intel/VIA South Bridge. High at S0~S3 and turn low when S4/S5
15	3VSBSW#	@VDD=5VSB O/P spec: CMOS O/P I _{OL} =4mA/0.4V I _{OH} =4mA/4.5V	Active low when system enters the S3 state until system enters the S0 state and PWRGD is active high
3	G3VSBSW#	@VDD=5VSB I/P spec: TTL input Internal pull-low 100kΩ to GND	Signal used for gating off 3VSBSW# Low: Gating off 3VSBSW# (default, BIOS will program low when power on) High: not gating off 3VSBSW# (BIOS will program high before entering S3 state) This signal will be transparent while PWRGD is high internally and latched with the falling edge of SUSB#.

Pin No.	Pin Name	I/O Spec.	Description
Power/GND: 4 pin			
14	5V	Power	
2	5VSB	Power	
1	VBAT	Power	
3	GND	GND	

Absolute Maximum Ratings

Supply Voltage-0.3V to 5.5V Storage Temperature-50°C to 125°C
 Input Voltage $V_{SS}-0.3V$ to $V_{DD}+0.3V$ Operating Temperature-25°C to 70°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

$T_a=25^\circ\text{C}$, $V_{DD5V}=5V$, $V_{DD5VSB}=5V$, $V_{BAT}=3.3V$

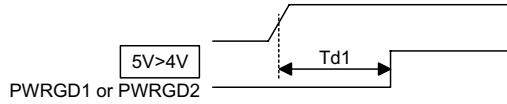
Pin Name	Symbol	I/O Spec. & Test Condition	Min.	Typ.	Max.	Unit
VBAT	I_{OP}	$V_{DD5VSB}=5V$, $V_{DD5V}=5V$	—	—	5	μA
	I_{SB}	$V_{DD5VSB}=0V$, $V_{DD5V}=0V$	—	—	1	μA
VDD5VSB	I_{OP}	$V_{BAT}=3.3V$, $V_{DD5V}=5V$	—	—	5	mA
	I_{SB}	$V_{BAT}=3.3V$, $V_{DD5V}=0V$	—	—	1	mA
VDD5V	I_{OP}	$V_{BAT}=3.3V$, $V_{DD5V}=5V$	—	—	5	mA
RSMRST#	I_{OL}	$V_{BAT}=3.3V$, $V_{OL}=0.4V$	4	6	—	mA
RESETCON#	V_{IL}	$V_{DD5VSB}=5V$	0	—	0.8	V
RSTIN#	V_{IH}	$V_{DD5VSB}=5V$	2	—	5	V
SUSB#	R_H	$V_{DD5VSB}=5V$, $V_{IL}=0V$	60	100	150	$\text{K}\Omega$
G3VSBSW#	V_{IL}	$V_{DD5VSB}=5V$	0	—	0.8	V
	V_{IH}	$V_{DD5VSB}=5V$	2	—	5	V
	R_L	$V_{DD5VSB}=5V$, $V_{IH}=5V$	85	125	165	$\text{K}\Omega$
3VSBSW#	I_{OL}	$V_{DD5VSB}=5V$, $V_{OL}=0.4V$	4	—	—	mA
	I_{OH}	$V_{DD5VSB}=5V$, $V_{OH}=4.5V$	4	—	—	mA
PWRGD1 PWRGD2 PSONOUT#	I_{OL}	$V_{DD5VSB}=5V$, $V_{OL}=0.4V$	10	—	—	mA
PCIRST# BRSTDRV#	I_{OL}	$V_{DD5VSB}=5V$, $V_{OL}=0.4V$	16	—	—	mA
	I_{OH}	$V_{DD5VSB}=5V$, $V_{OH}=4.5V$	16	—	—	mA

A.C. Characteristics

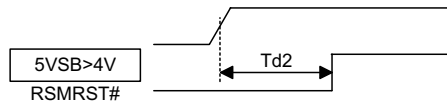
Ta=25°C, VDD5V=5V, VDD5VSB=5V, VBAT=3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
Td1	Power Good Delay	300	425	600	ms
Td2	RSMRST# Delay	40	60	90	ms

- Power good delay

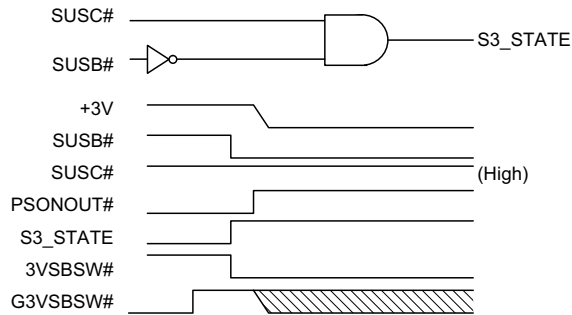


- RSMRST# delay

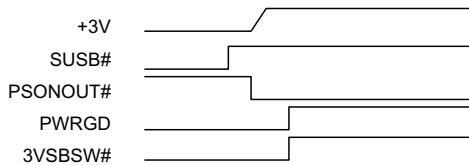


Timing Diagrams

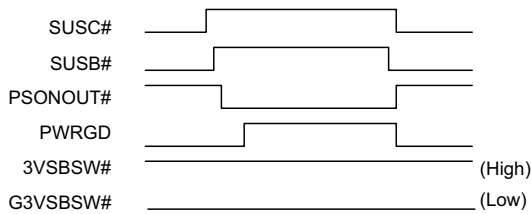
From S0 to S3 (SW off to on)



From S3 to S0 (SW on to off)

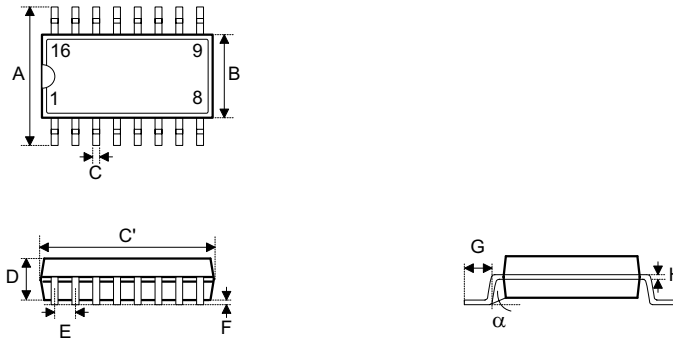


From S5 to S0 and from S0 to S5 (not SW on)



Package Information

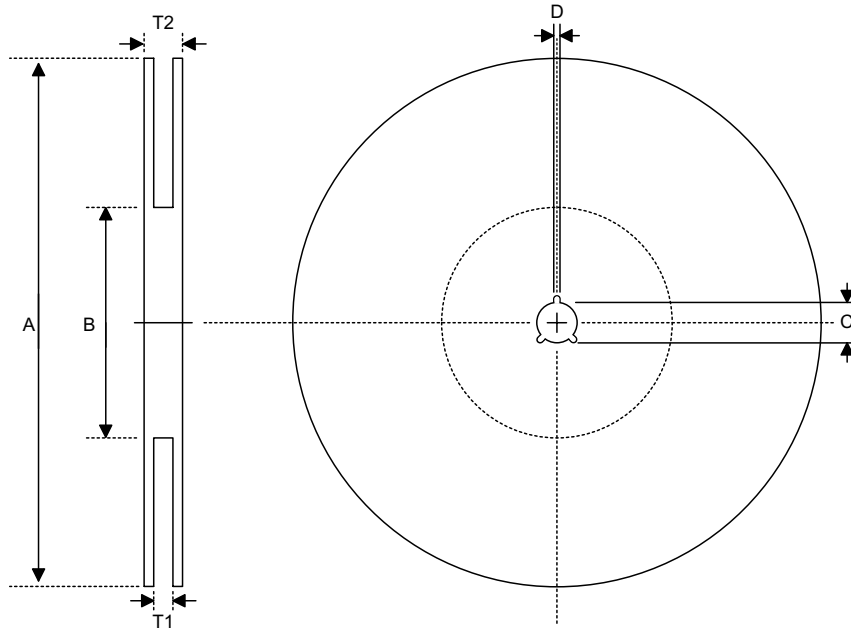
16-pin NSOP (150mil) outline dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	149	—	157
C	14	—	20
C'	386	—	394
D	53	—	69
E	—	50	—
F	4	—	10
G	22	—	28
H	4	—	12
α	0°	—	10°

Product Tape and Reel Specifications

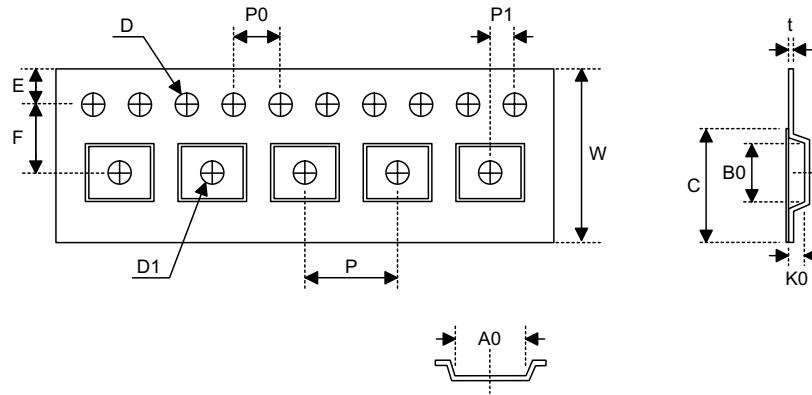
Reel dimensions



SOP 16N

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	12.75+0.5
D	Key Slit Width	1.5+0.15
T1	Space Between Flange	16.4+0.2
T2	Reel Thickness	22.4+0.4

Carrier tape dimensions



SOP 16N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0±0.3
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.5±0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.5±0.1
B0	Cavity Width	10.3±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	13.3

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