

REVISIONS			
REV	ECO	DESCRIPTION	BY

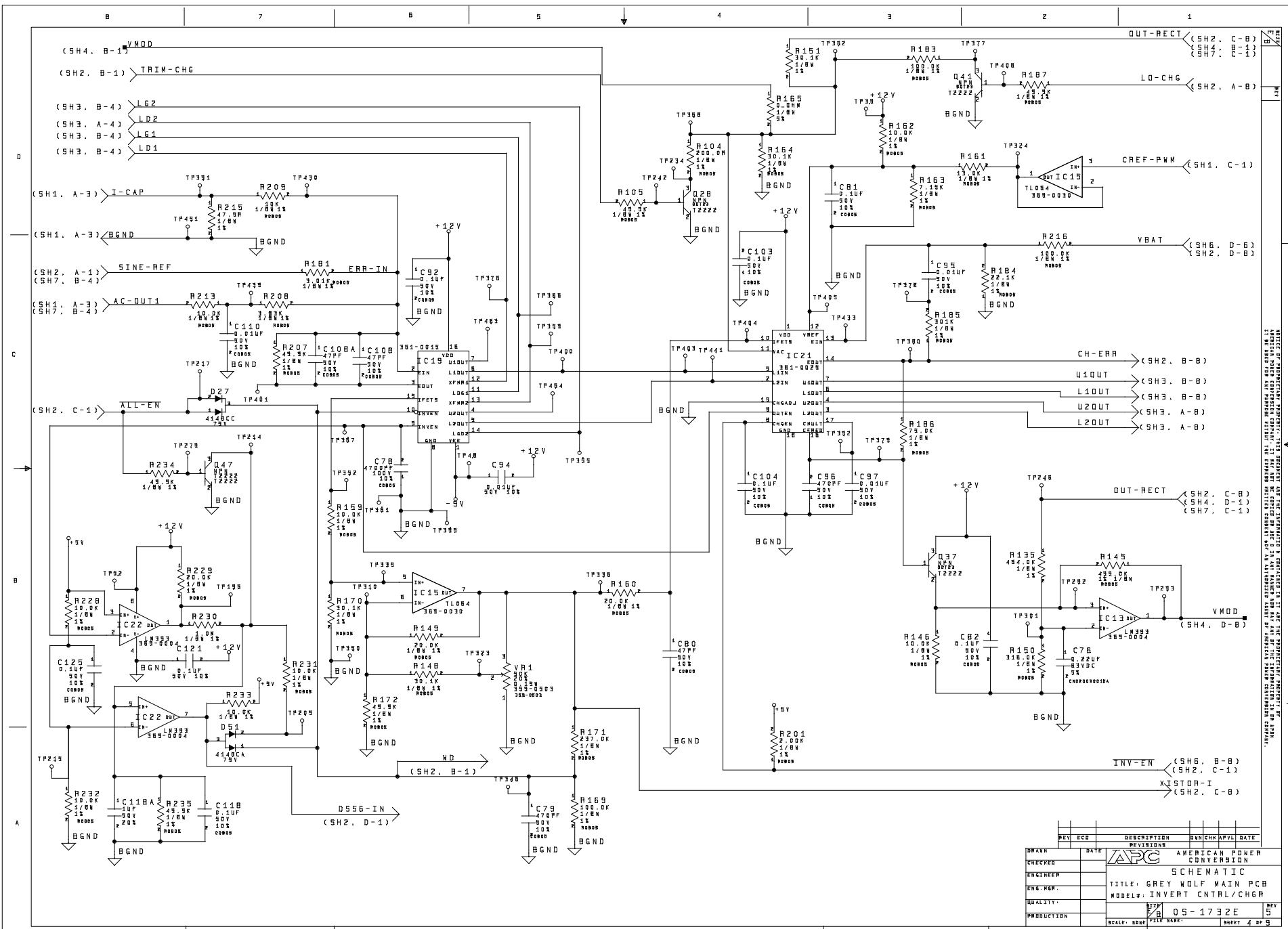
  

DRAWN		DATE		DESCRIPTION		APP'D		DATE	

APC		AMERICAN POWER CONVERSION	
CHECKED		SCHEMATIC	
ENGINEER		TITLE: GREY WOLF MAIN PCB	
DESIGN		MODEL: MICROPROCESSOR	
QUALITY			
PRODUCTION		05-1732E	REV D





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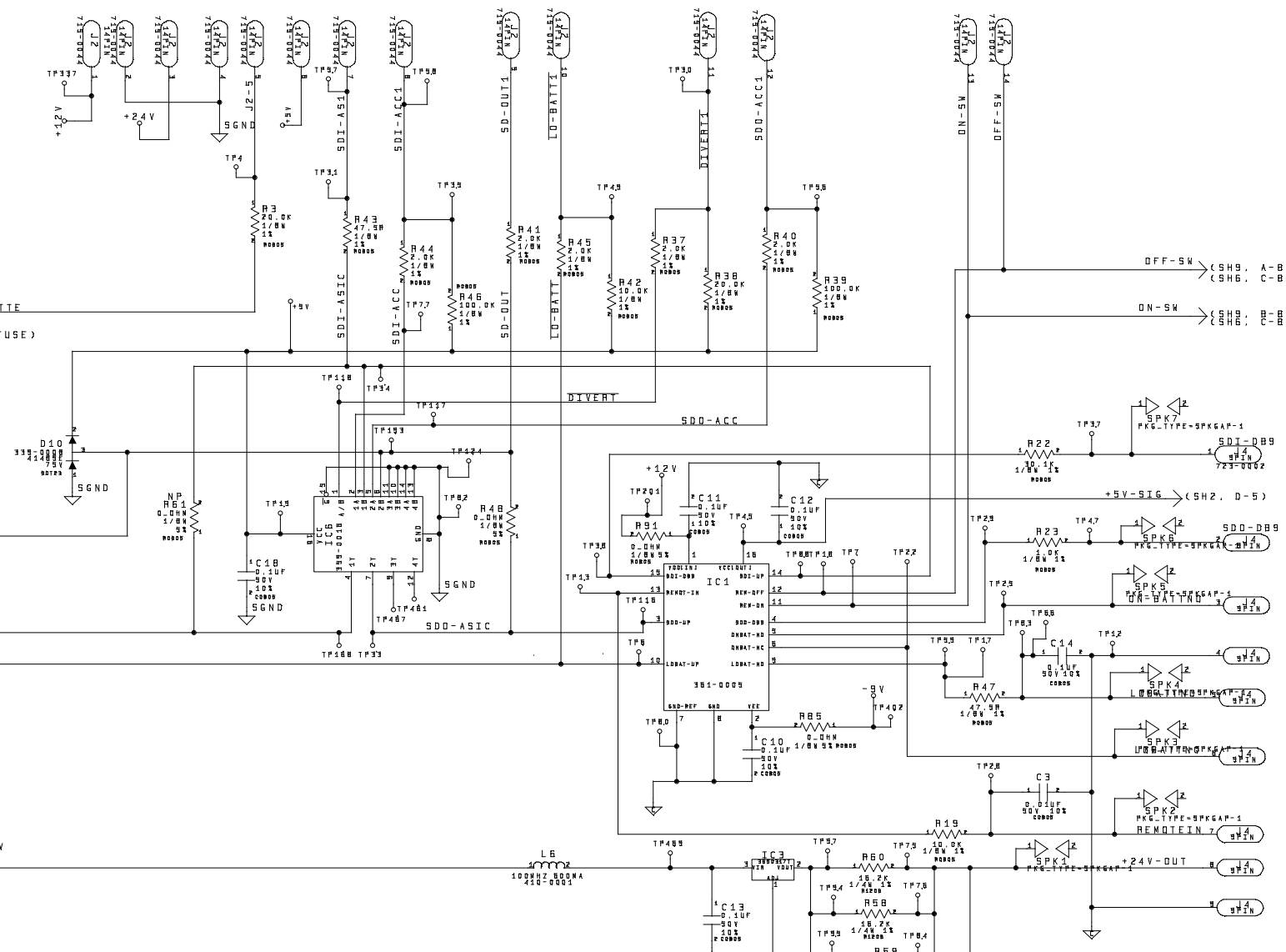
REV	ECO	DESCRIPTION	BY	CHK	APVL	DATE
		REVISIONS				
		AMERICAN POWER CONVERSION				
SCHEMATIC TITLE: GREY WOLF MAIN PCB MODEL: INVERT CNTRL/CHGR						
QUALITY		05-1732E				REV
PRODUCTION		SCALE: NONE	FILE NAME:			SHEET 4 OF 9

Pin	Signal Name
1	SGND
2	+2.4V
3	+2.4V
4	+2.4V
5	+2.4V
6	+2.4V
7	+2.4V
8	+2.4V
9	+2.4V
10	+2.4V
11	+2.4V
12	+2.4V
13	+2.4V
14	+2.4V
15	+2.4V
16	+2.4V
17	+2.4V
18	+2.4V
19	+2.4V
20	+2.4V
21	+2.4V
22	+2.4V
23	+2.4V
24	+2.4V
25	+2.4V
26	+2.4V
27	+2.4V
28	+2.4V
29	+2.4V
30	+2.4V
31	+2.4V
32	+2.4V
33	+2.4V
34	+2.4V
35	+2.4V
36	+2.4V
37	+2.4V
38	+2.4V
39	+2.4V
40	+2.4V
41	+2.4V
42	+2.4V
43	+2.4V
44	+2.4V
45	+2.4V
46	+2.4V
47	+2.4V
48	+2.4V
49	+2.4V
50	+2.4V
51	+2.4V
52	+2.4V
53	+2.4V
54	+2.4V
55	+2.4V
56	+2.4V
57	+2.4V
58	+2.4V
59	+2.4V
60	+2.4V
61	+2.4V
62	+2.4V
63	+2.4V
64	+2.4V
65	+2.4V
66	+2.4V
67	+2.4V
68	+2.4V
69	+2.4V
70	+2.4V
71	+2.4V
72	+2.4V
73	+2.4V
74	+2.4V
75	+2.4V
76	+2.4V
77	+2.4V
78	+2.4V
79	+2.4V
80	+2.4V
81	+2.4V
82	+2.4V
83	+2.4V
84	+2.4V
85	+2.4V
86	+2.4V
87	+2.4V
88	+2.4V
89	+2.4V
90	+2.4V
91	+2.4V
92	+2.4V
93	+2.4V
94	+2.4V
95	+2.4V
96	+2.4V
97	+2.4V
98	+2.4V
99	+2.4V
100	+2.4V

+BATT F  
 {SH6: D-1}  
 (SHORT to +BATT thru FUSE)

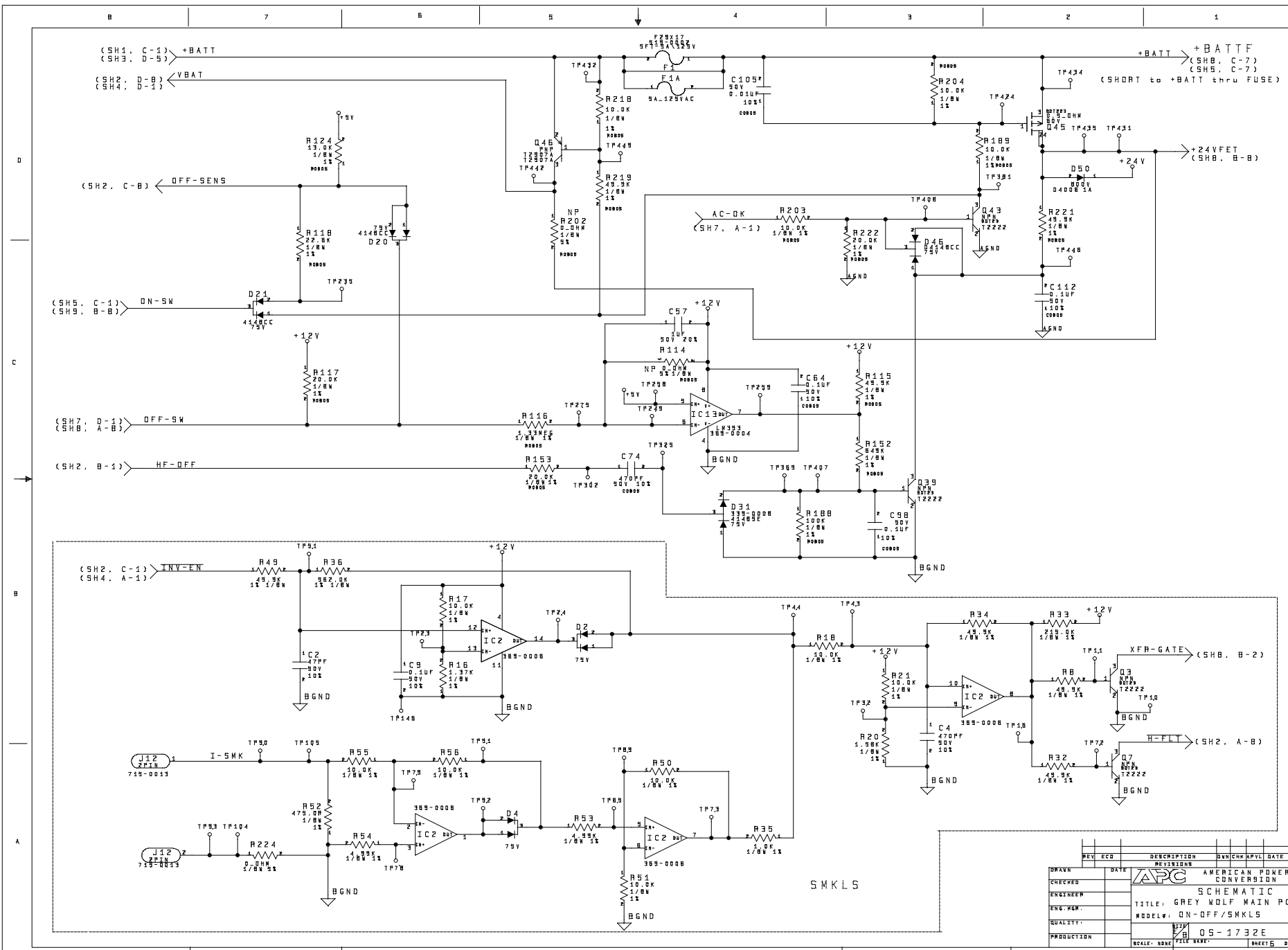
(SH2: B-B) SD-DUT  
 (SH2: B-B) RXD  
 (SH2: C-1) LU-BATT

(SH6: D-2) +2.4V



REV	ECO	DESCRIPTION	DATE	APV	DATE
		REVISIONS <td></td> <td></td> <td></td>			
		AMERICAN POWER <td></td> <td></td> <td></td>			
		CONVERSION <td></td> <td></td> <td></td>			
		SCHEMATIC <td></td> <td></td> <td></td>			
		TITLE: GREY WOLF MAIN PCB <td></td> <td></td> <td></td>			
		MODEL#: SMARTSLOT/DB9 <td></td> <td></td> <td></td>			
		QUALITY:			
		PRODUCTION			
		SCALE: NONE			
		FILE NAME:			
		05-1732E			
		SHEET 9			
		OF 9			

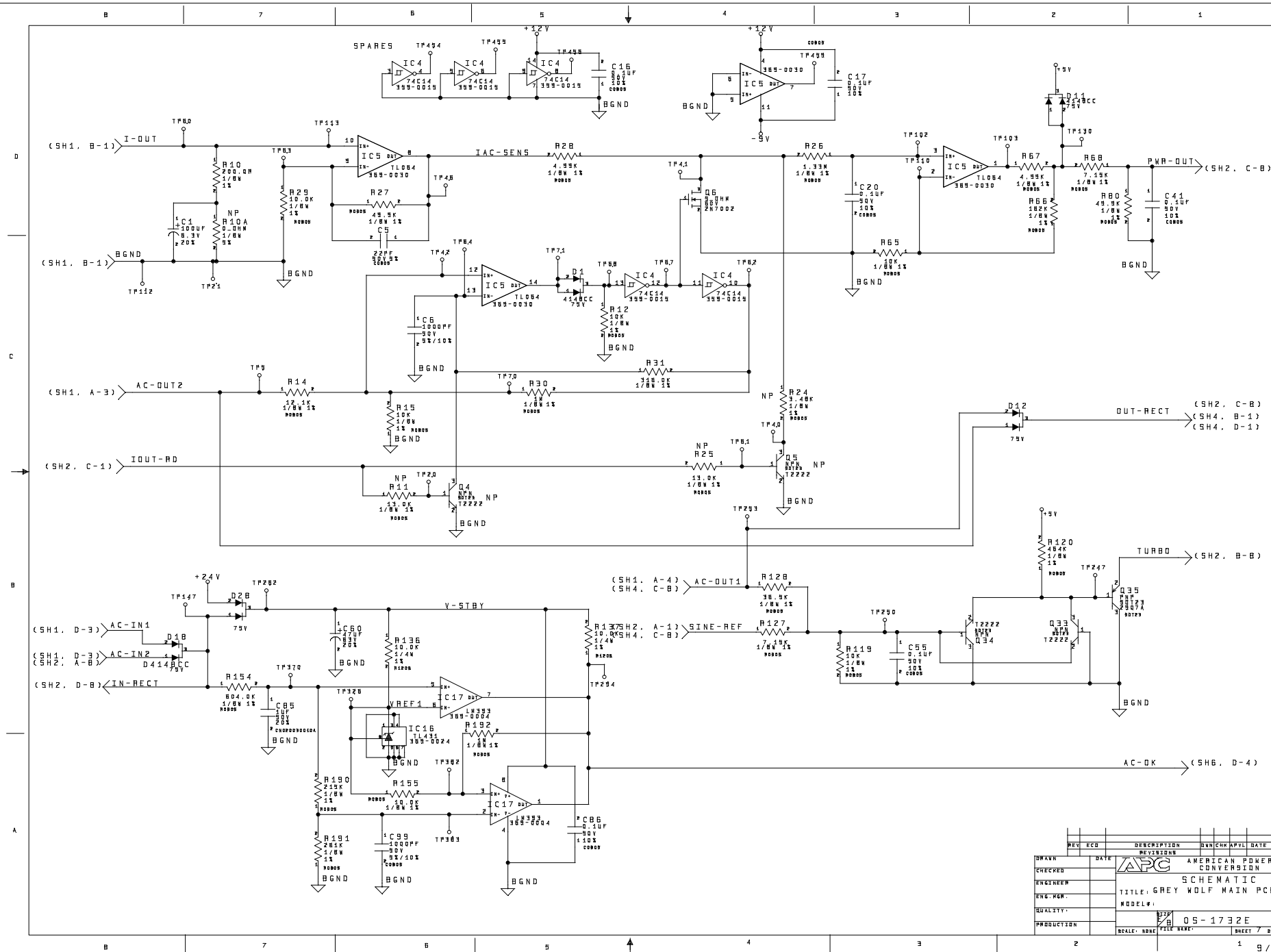
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SMKLS

REV	ECO	DESCRIPTION	DRN	CHK	APVL	DATE
REVISIONS DATE: _____ AMERICAN POWER CONVERSION						
ENGINEER: _____ TITLE: GREY WOLF MAIN PCB						
MODEL#: QN-OFF/SMKLS						
QUALITY: _____ FILE NAME: 05-1732E						
PRODUCTION: _____ SCALE: NONE SHEET 5 OF 5						



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REV	ECO	DESCRIPTION	DATE	APPV	DATE

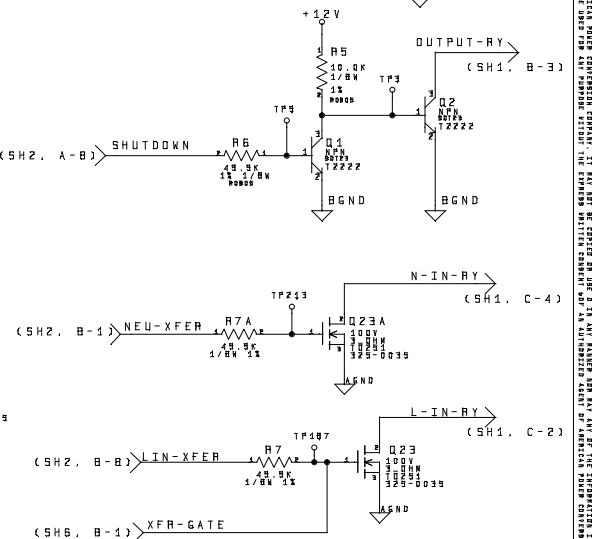
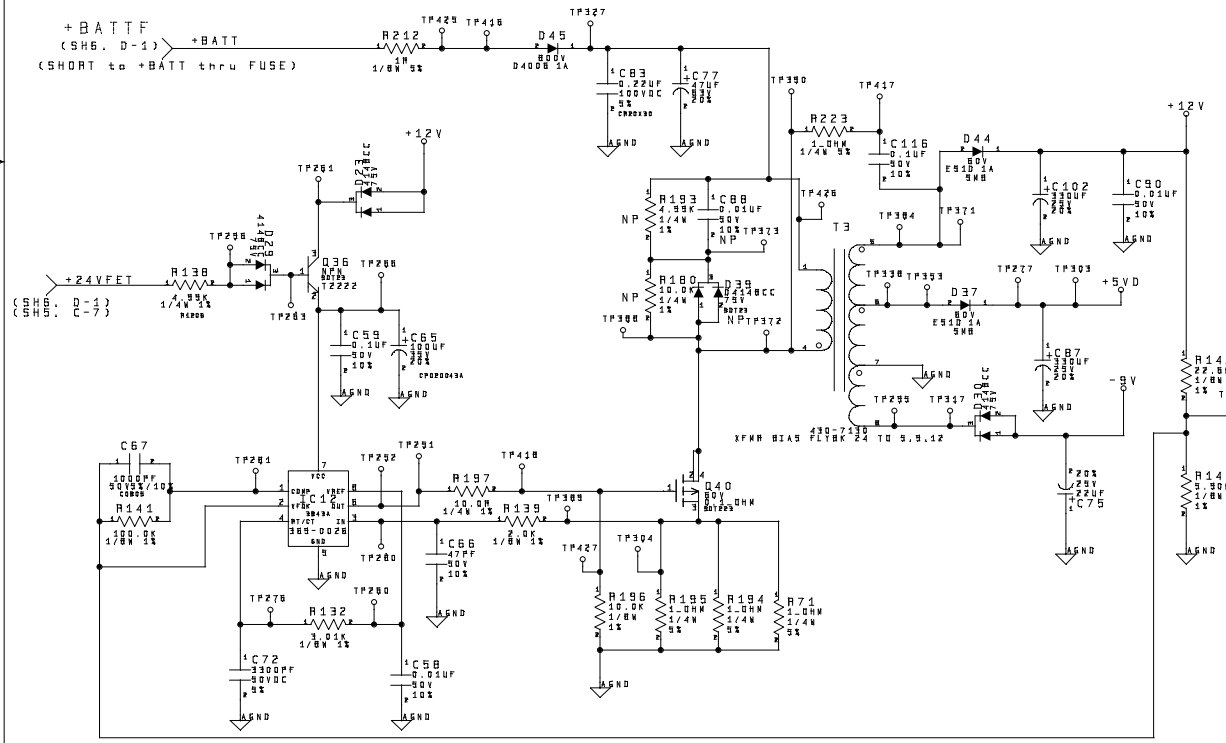
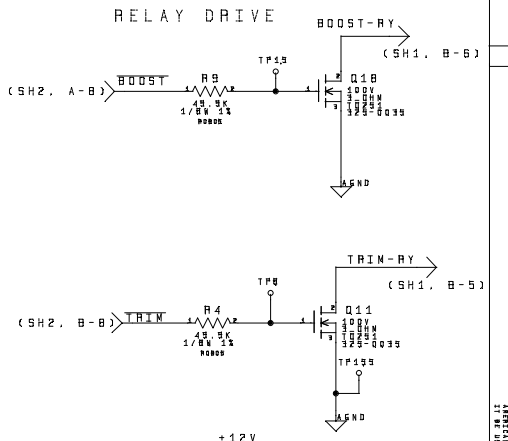
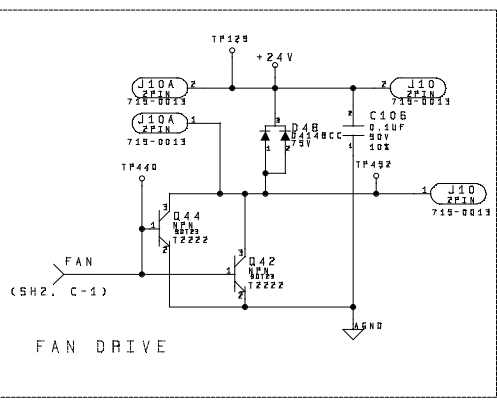
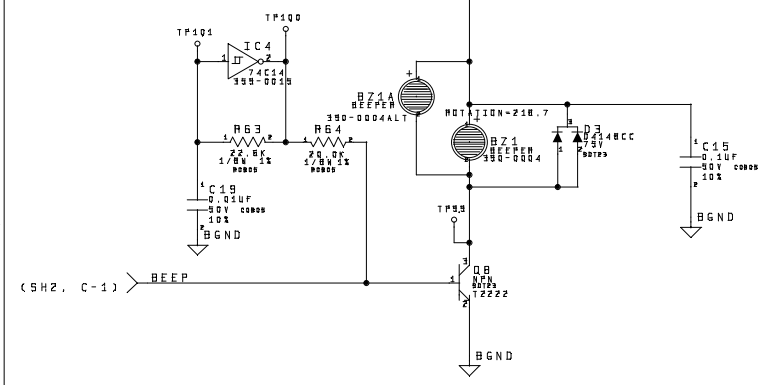
  

DRAWN	DATE	REVISIONS	AMERICAN POWER CONVERSION
CHECKED			
ENGINEER			
ENG-PGM			
QUALITY			
PRODUCTION			

**SCHEMATIC**  
 TITLE: GREY WOLF MAIN PCB  
 MODEL#: 05-1732E  
 SCALE: NONE FILE NAME: SHEET 7 OF 9

B 7 6 5 4 3 2 1

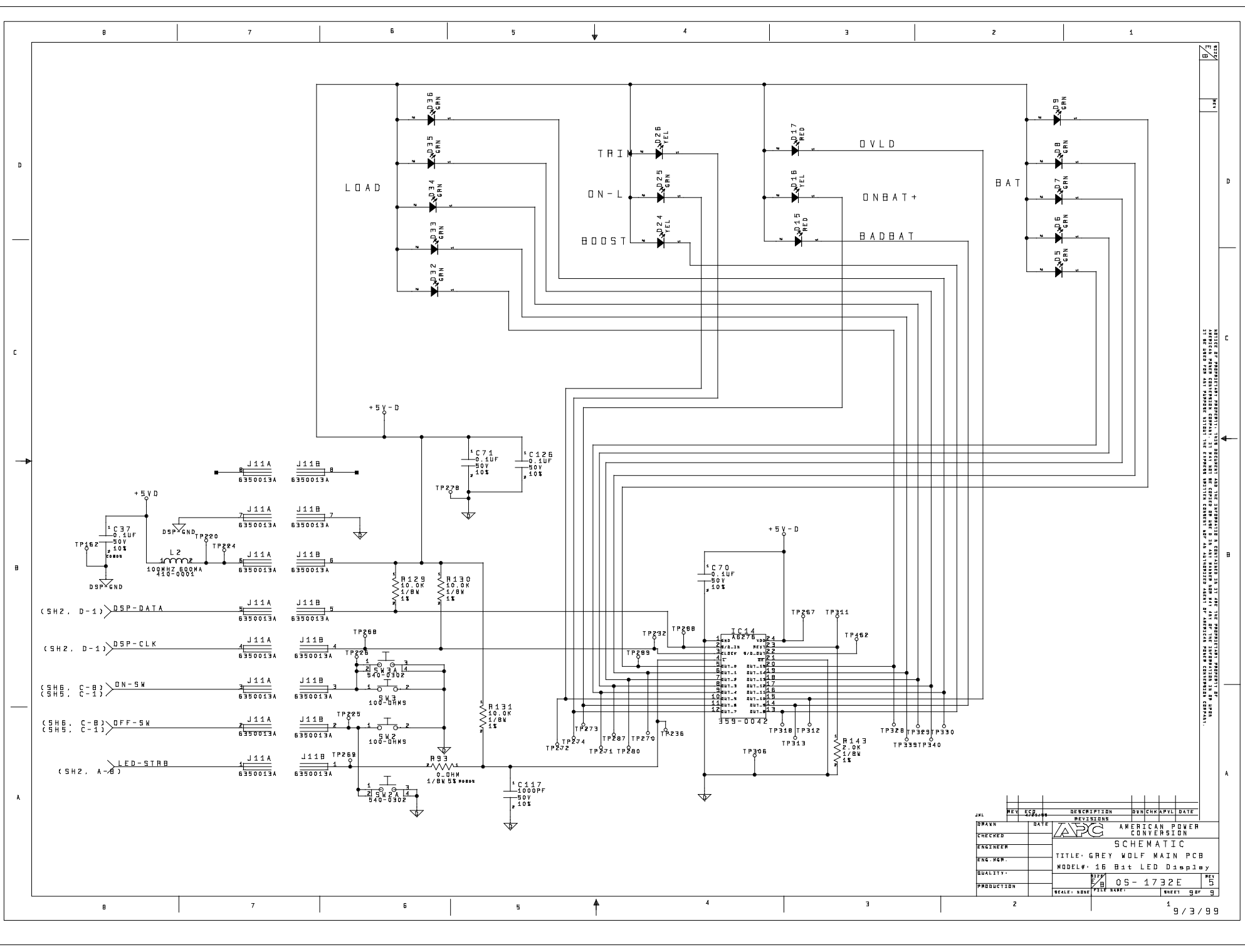
BEEPER



REV	ECO	DESCRIPTION	BY	CHKD	APVL	DATE																								
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QUALITY																														
PRODUCTION																														
TITLE: GREY WOLF MAIN PCB MODEL#:			SHEET 8 OF 9																											
SCALE: NONE			FILE NAME: 05-1732E																											

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REV	DATE	DESCRIPTION	BY	CHK	APVL	DATE
1						

DRAWN		AMERICAN POWER CONVERSION
CHECKED		SCHEMATIC
ENG. NO.		MODEL# 16 Bat LED Display
QUALITY		
PRODUCTION		

SCALE	DATE	FILE NAME	SHEET	OF	TOTAL
			5		9

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