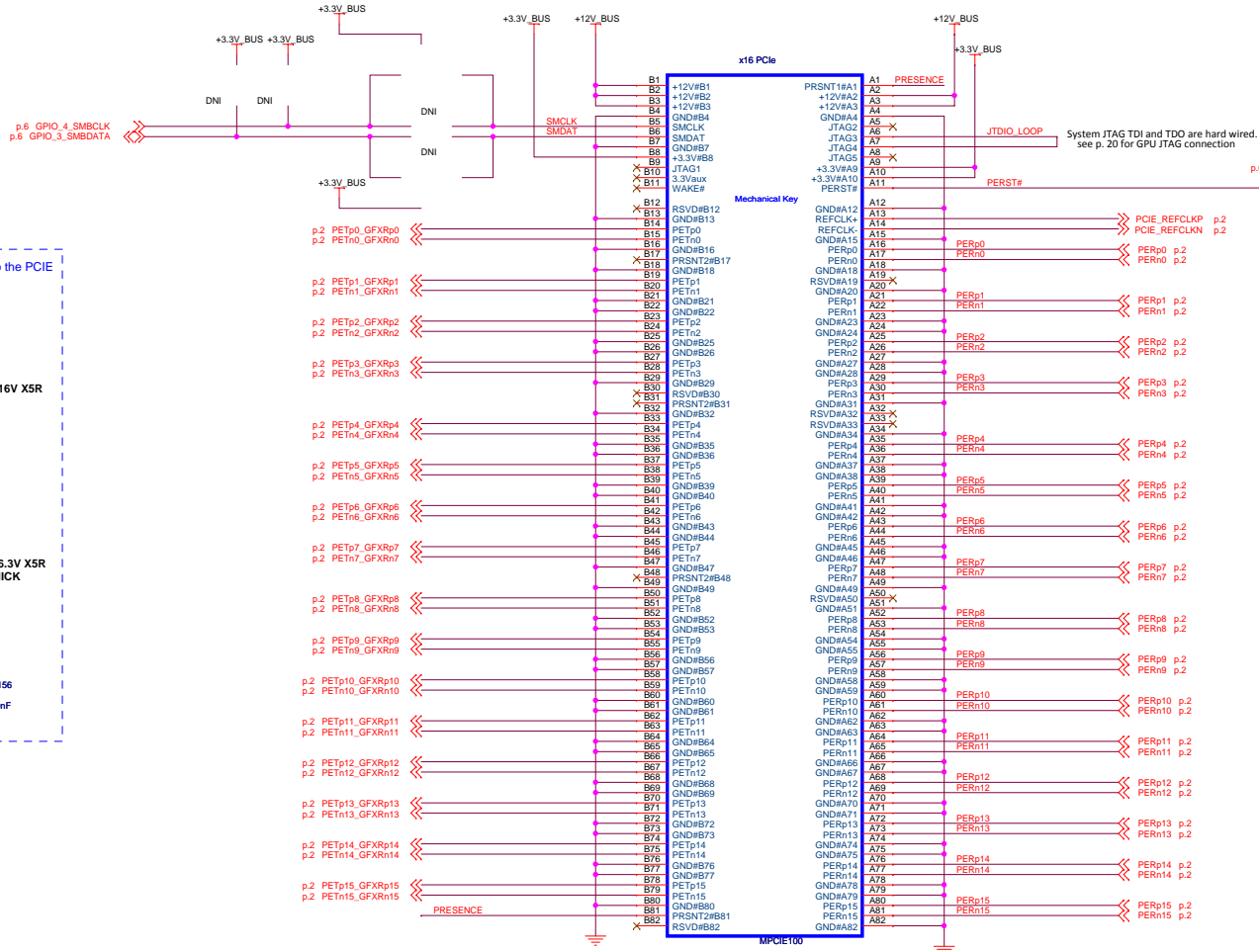
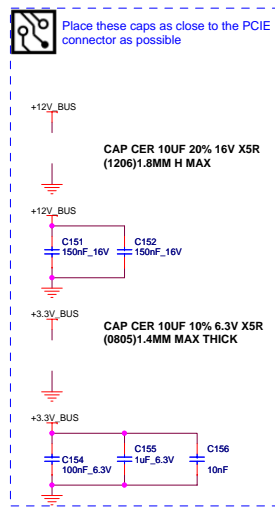
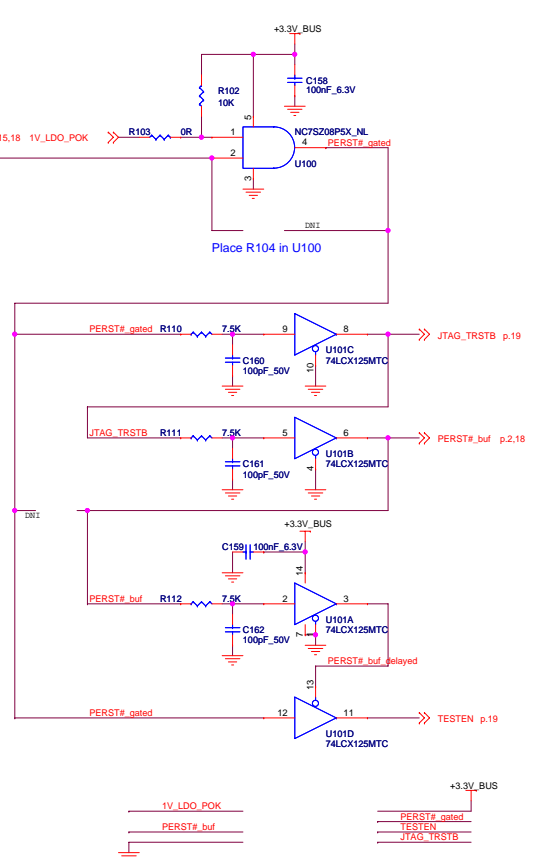


# PCI-EXPRESS EDGE CONNECTOR

C013



## PCIe RESET Buffered



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
⏏	DIGITAL GROUND
⏏	ANALOG GROUND
BUO	BRING UP ONLY

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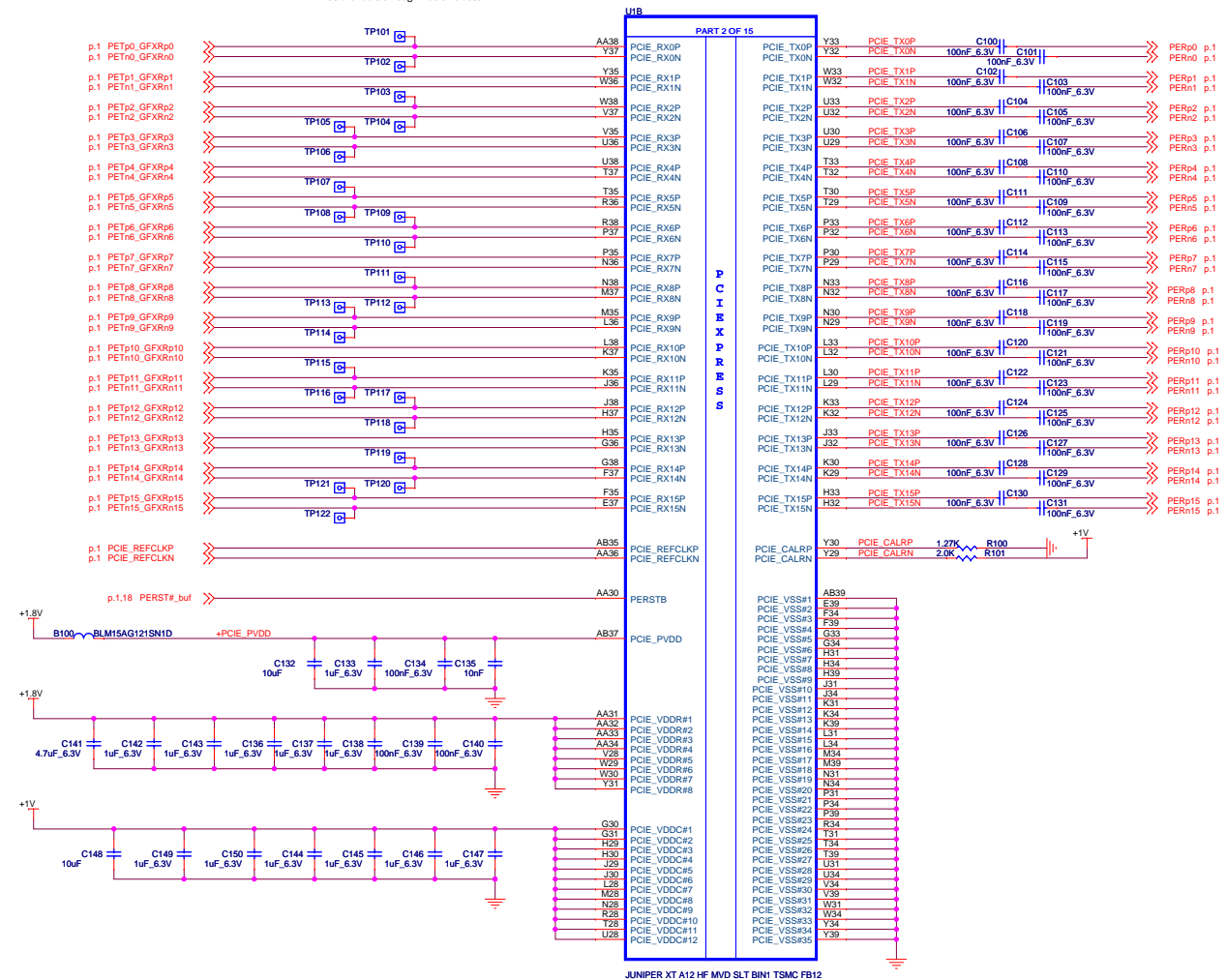
DATE: Tuesday, November 10, 2009 Rev 50

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File: RH JUNIPER GDDR5 1GB DP+DP/HDMI+DVI /S/VA Doc No: 102-C01301-00

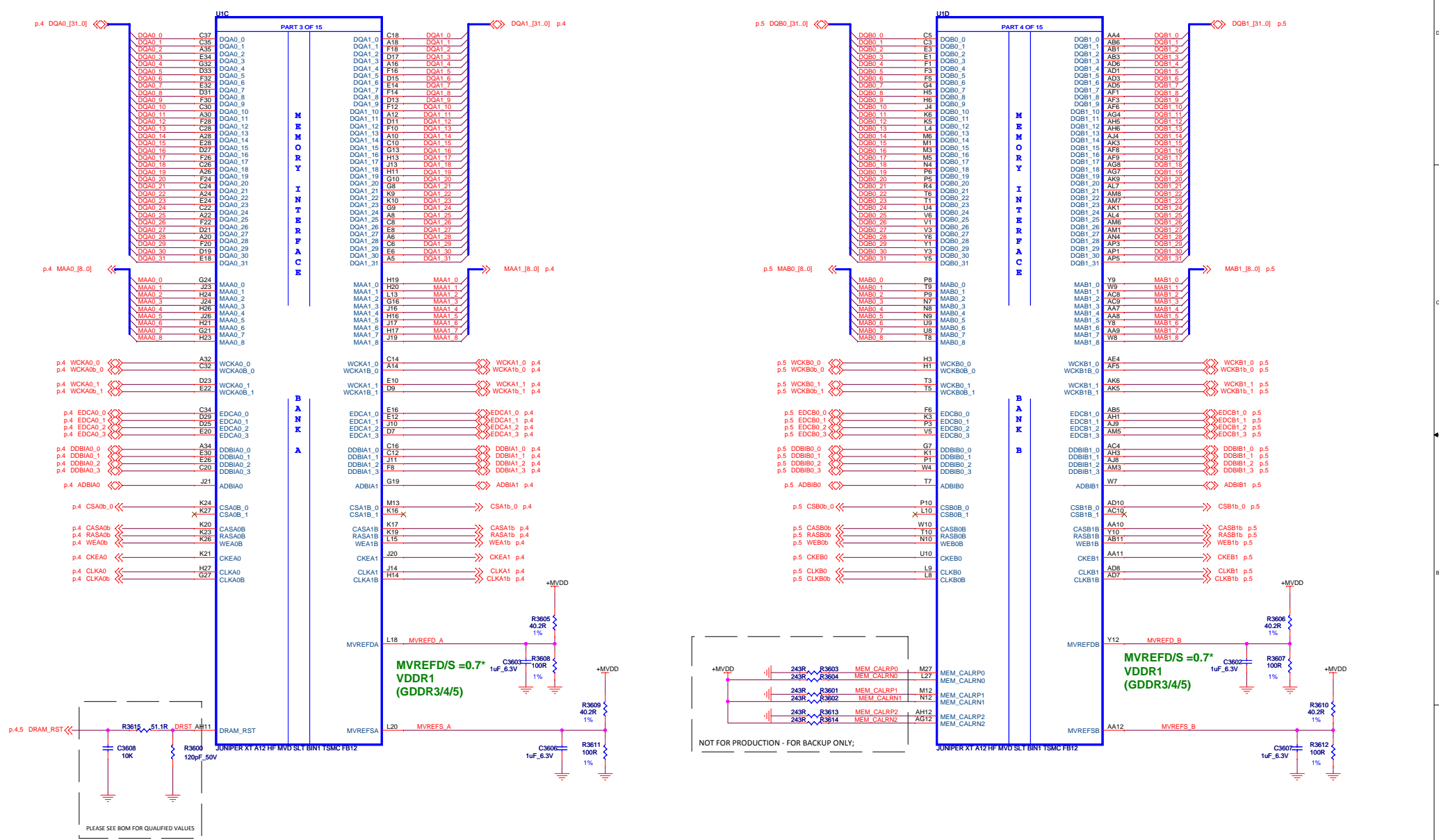
# (2) JUNIPER PCIe Interface

NOTE: Some of the PCIe testpoints will be available through vias on traces.

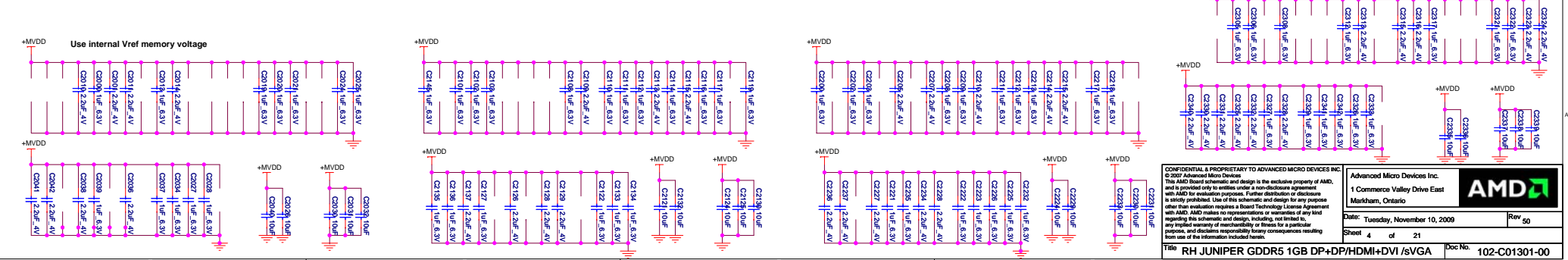
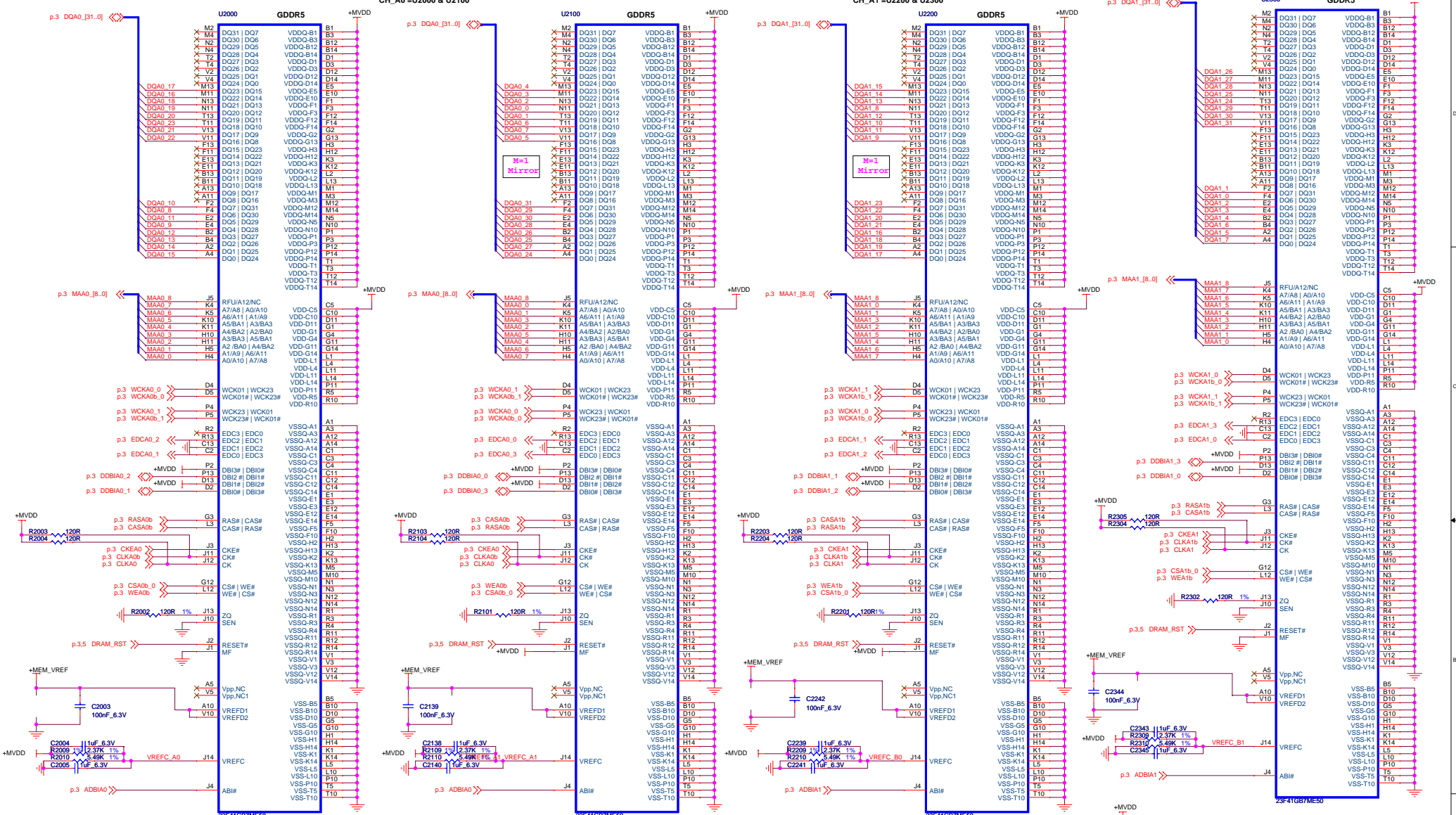


JUNIPER AT A12 HF MVD SLT BIN1 TSMC FB12

# (3) JUNIPER MEM Interface Ch A&B



# (4) GDDR5 x16 MEM Channel A



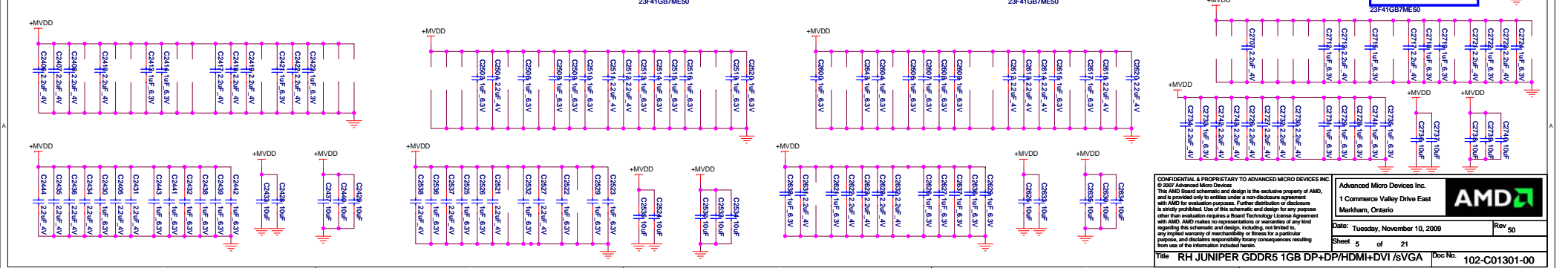
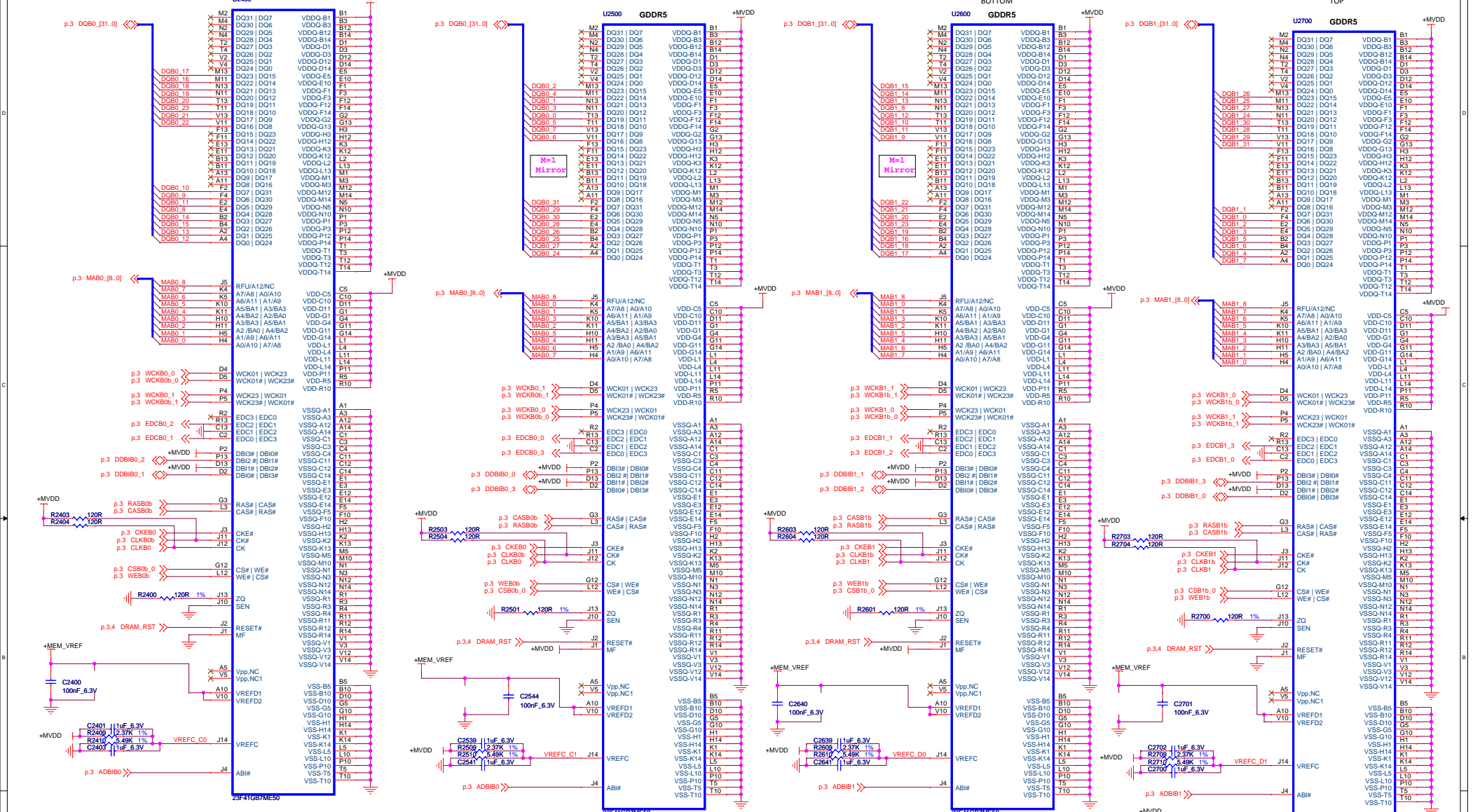
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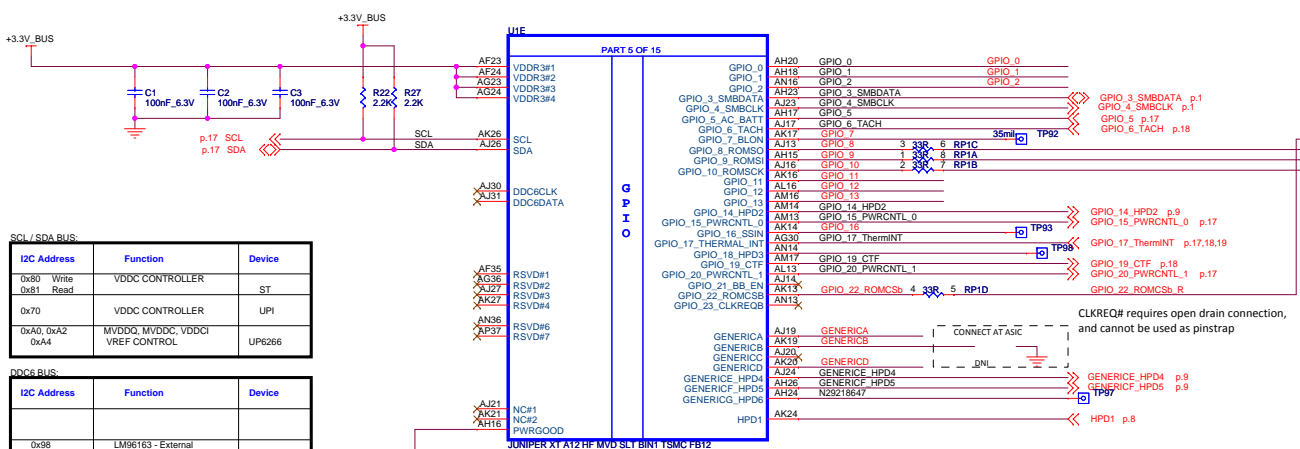
File: RH JUNIPER GDDR5 1GB DP+DP/HDMI+DVI/SVGA Doc No: 102-C01301-00

(5) GDDR5 x16 MEM Channel B





# (06) JUNIPER GPIOs Strap CF XTAL OSC



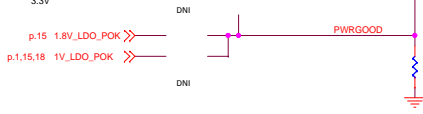
**I2C (SDA BUS)**

I2C Address	Function	Device
0x80 Write	VDDC CONTROLLER	ST
0x81 Read	VDDC CONTROLLER	ST
0x70	VDDC CONTROLLER	LPI1
0xA0, 0xA2	MVDDQ, MVDDC, VDDCI VREF CONTROL	UP266

**DDC6 BUS:**

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

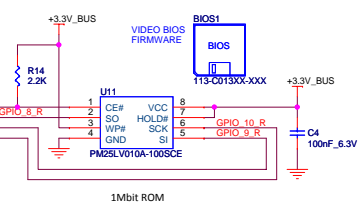
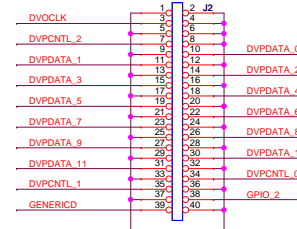
NOTE: If connecting 1V LDO\_POK, only one pull up either to 1.8V or 3.3V



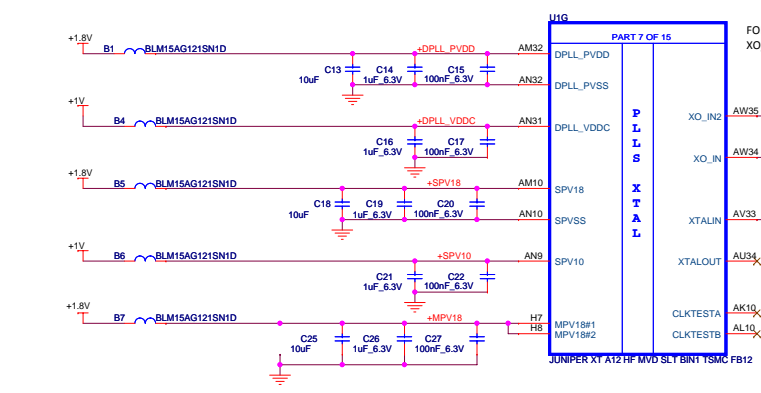
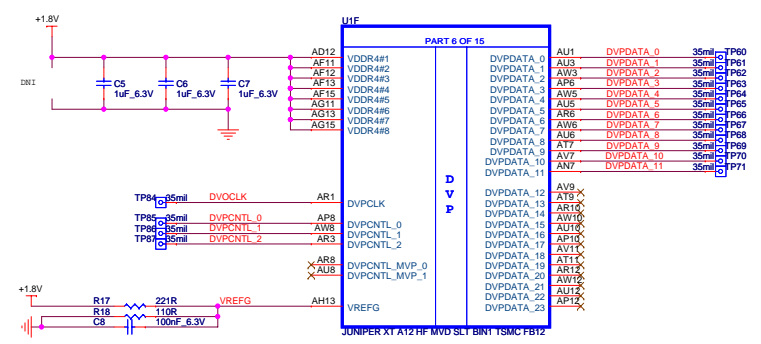
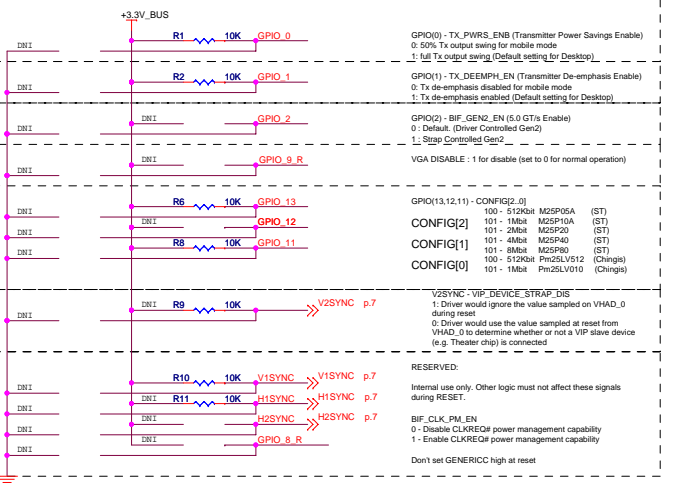
## CrossFire Card-Edge

## Upper Cable Card Edge or Bundle B

## Lower Cable Card Edge or Bundle A (closer to the bracket)

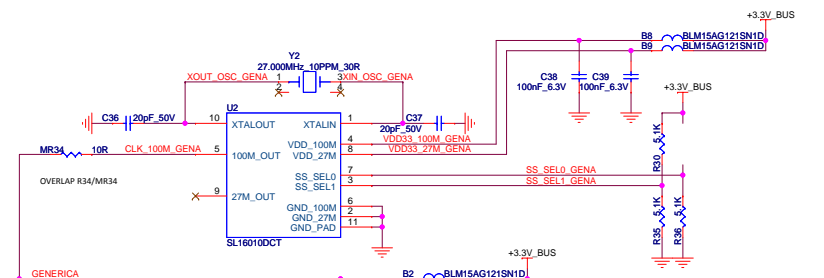


## PIN BASED STRAPS



FOR 740: DNI R28/TR19 - XO\_IN/2 ARE GND on 740/730

route 50ohms single-ended/100ohms diff and keep short



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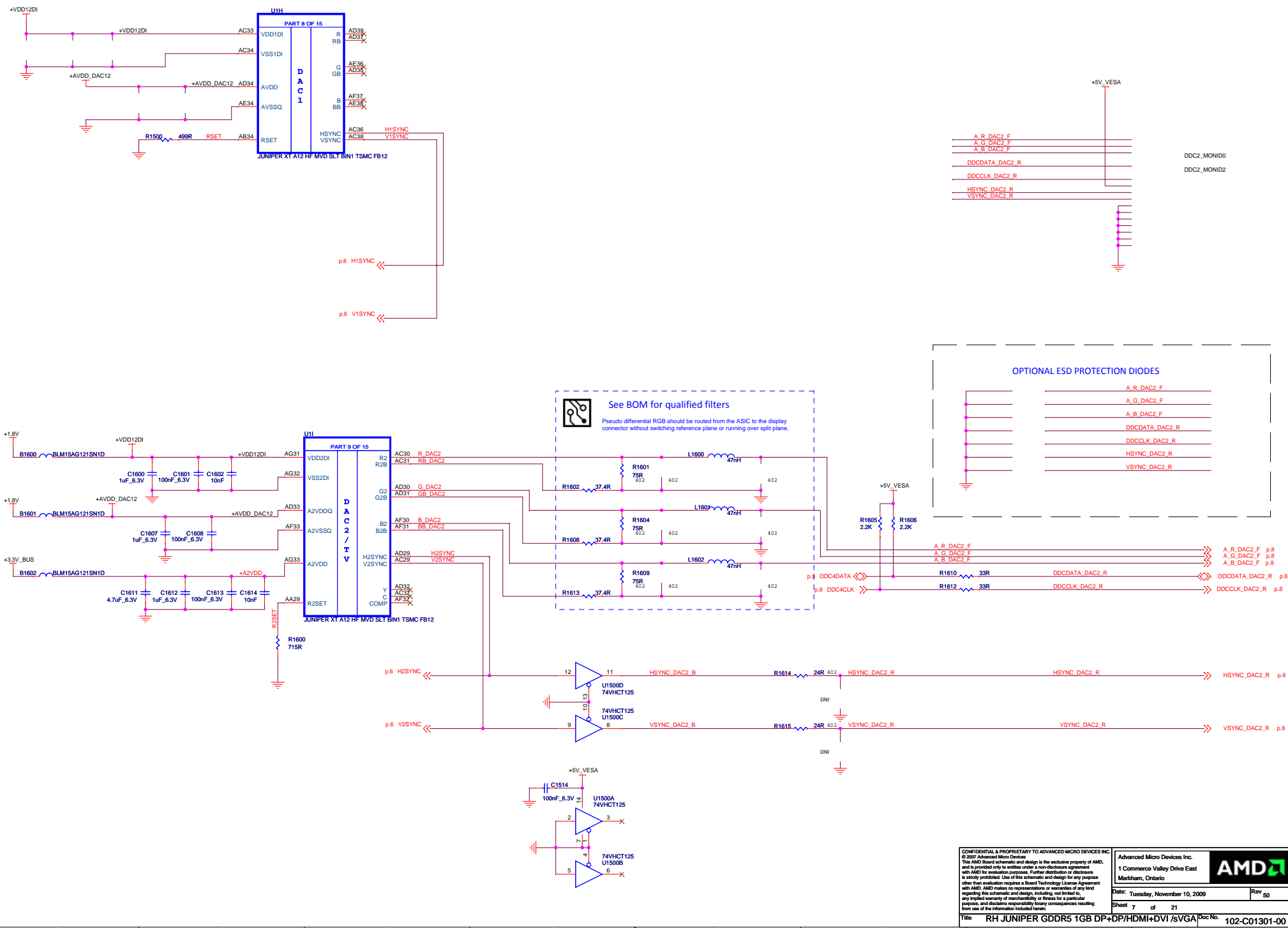
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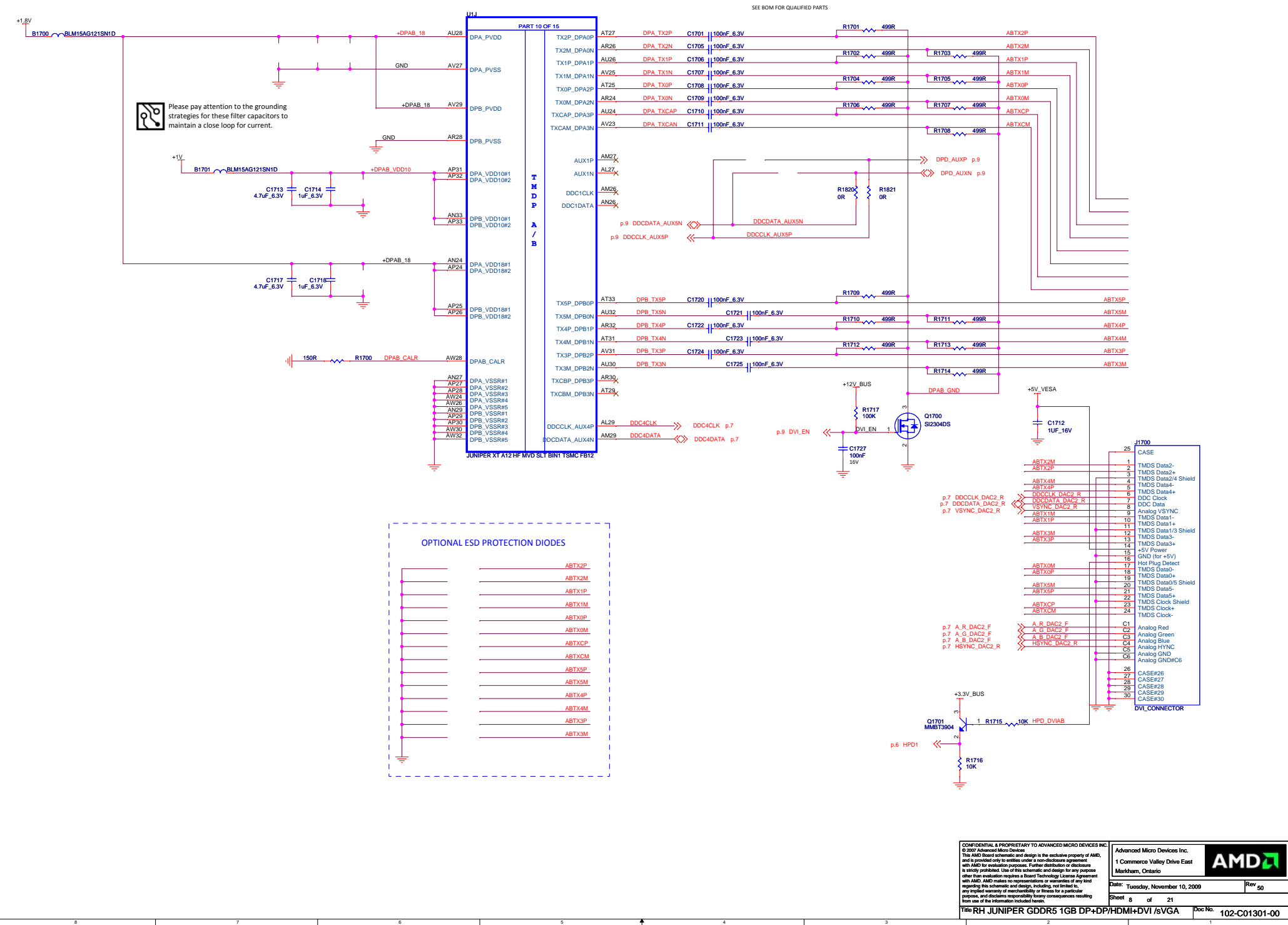
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File: RH JUNIPER GDDR5 1GB DP+DP/HDMI+DVI/sVGA Doc No: 102-C01301-00

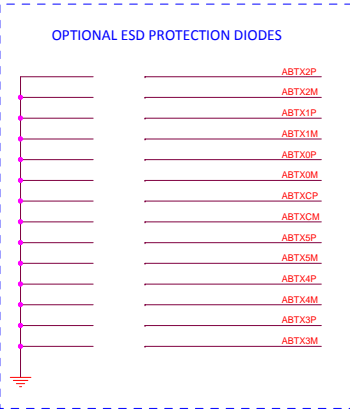
# (07) JUNIPER DAC1 and DAC2



# (08) JUNIPER TMDP A&B dDVI-I TOP



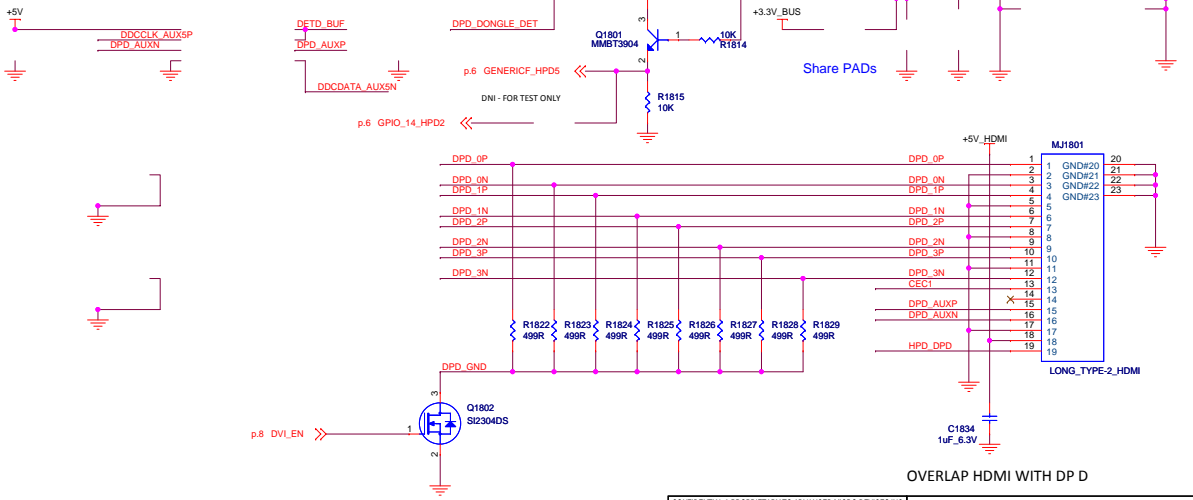
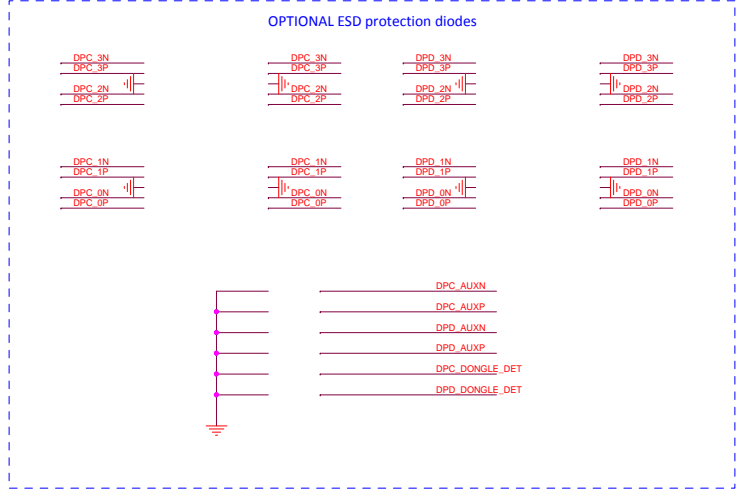
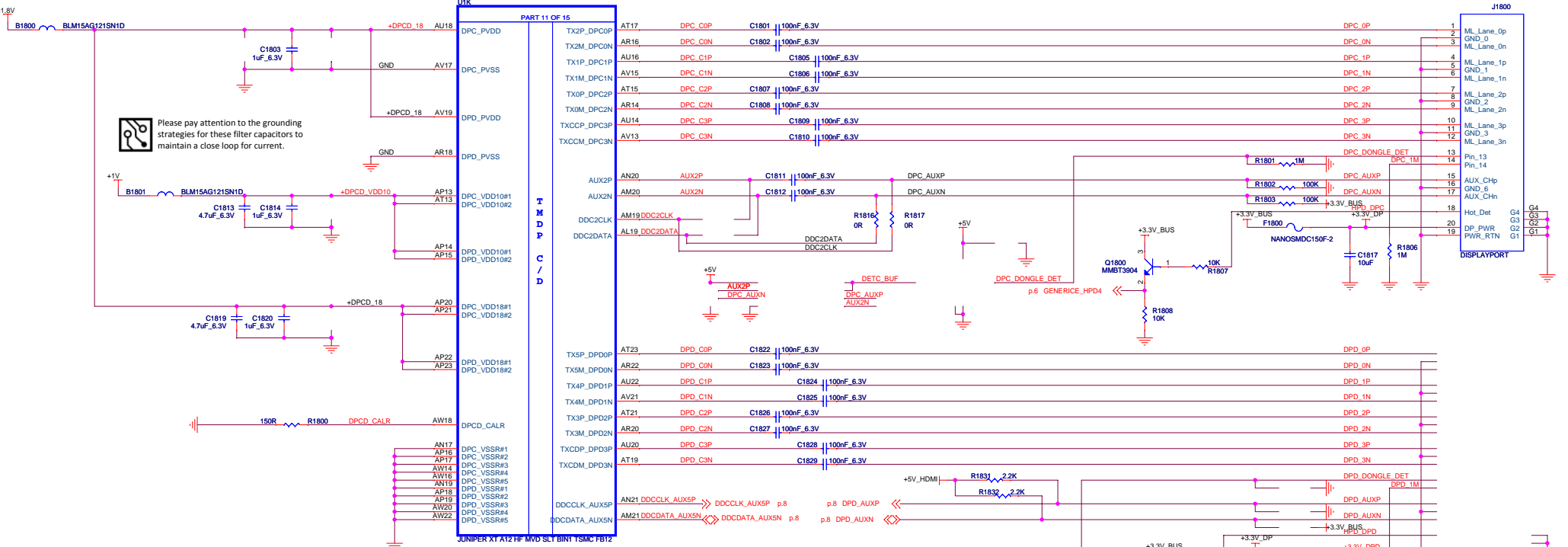
Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.





# (09) JUNIPER Display Port C & Display Port/HDMI D

AUX/DDC:  
 FOR 740/730, INSTALL OR ON ASIC-SIDE OF AC COUPLING CAPS ONLY;  
 FOR JUNIPER, INSTALL OR ON CONNECTOR SIDE OF AC COUPLING CAPS ONLY;



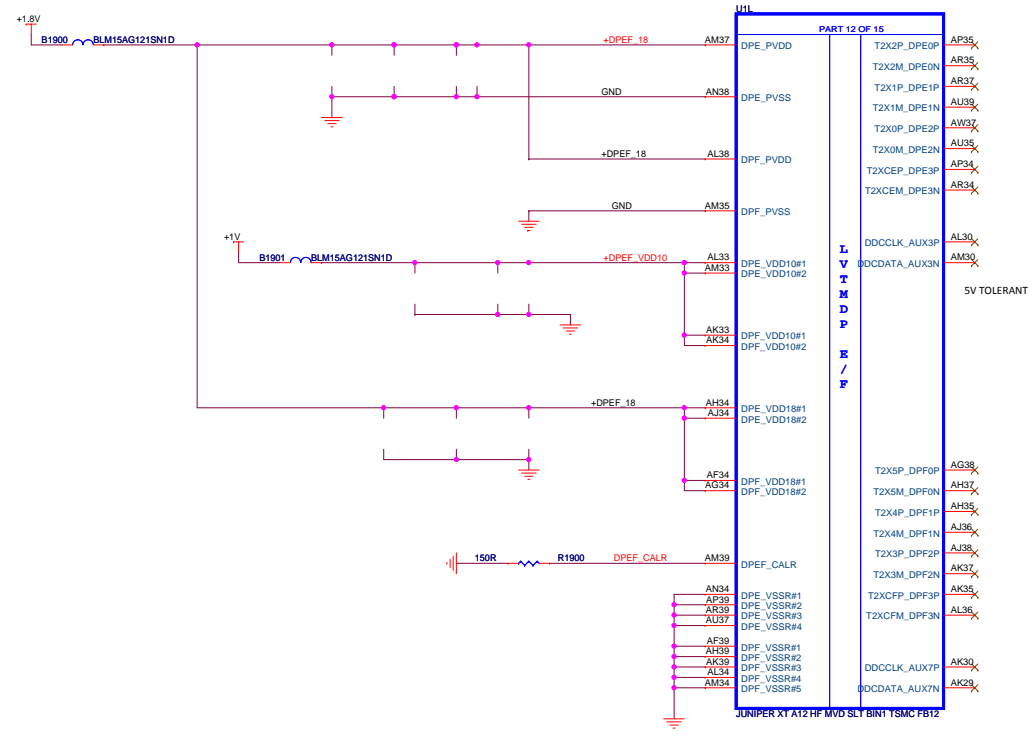
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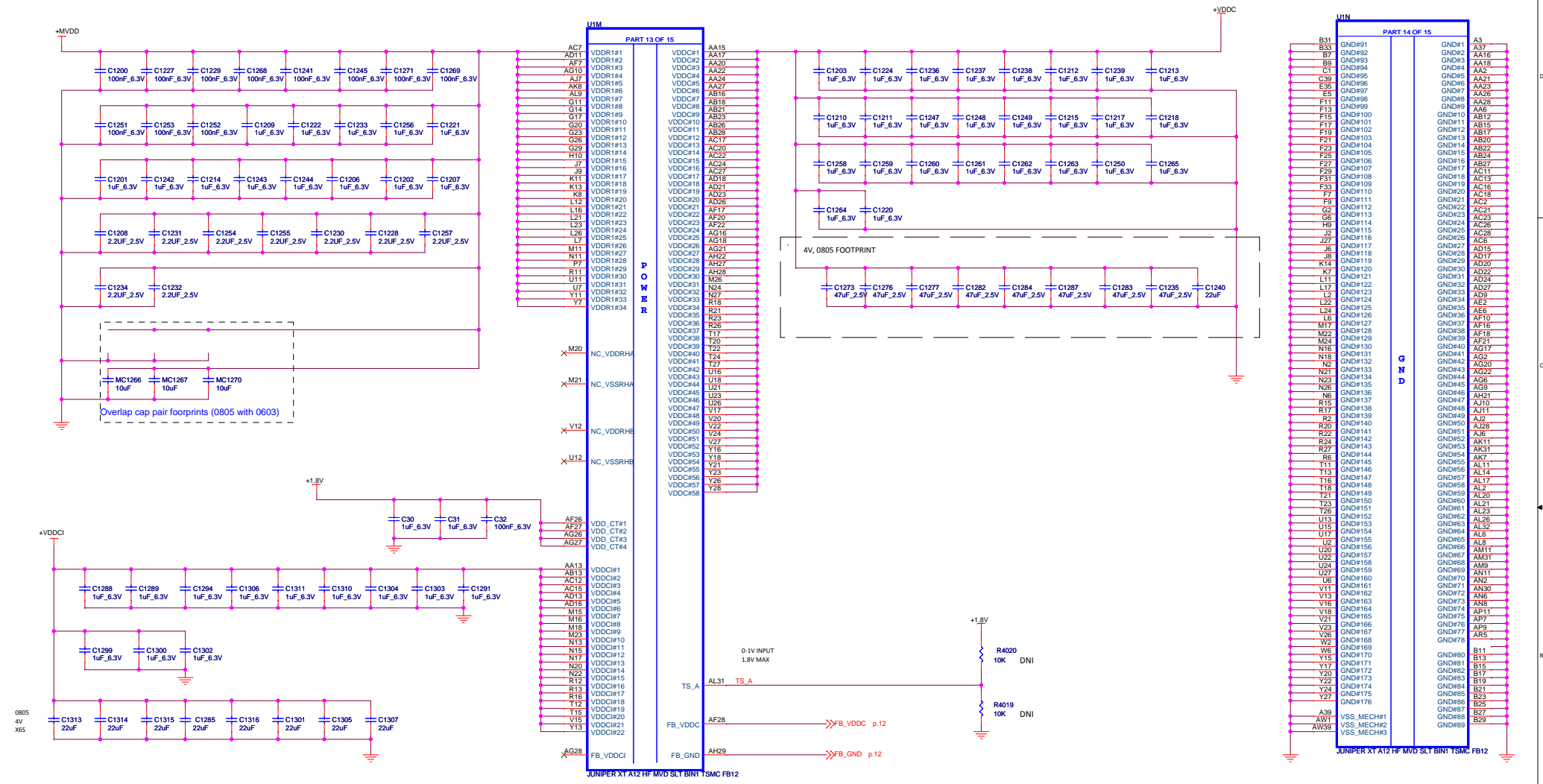
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# (10) JUNIPER LVTMDP E&F



# (11) JUNIPER Power & GND

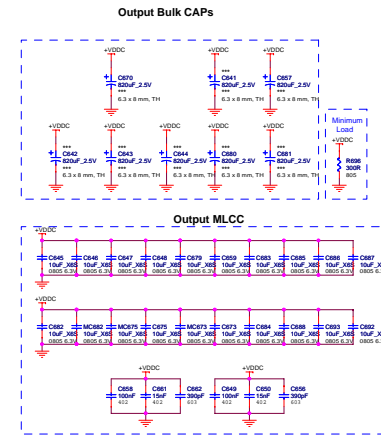
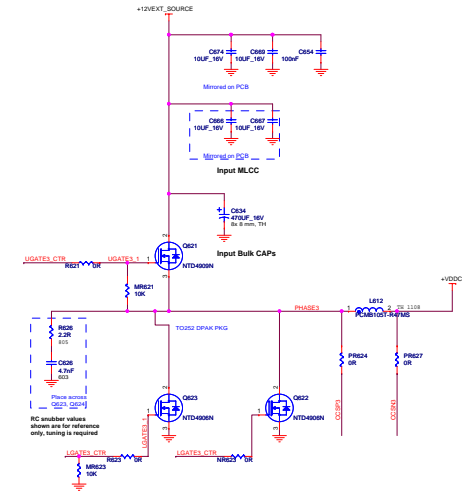
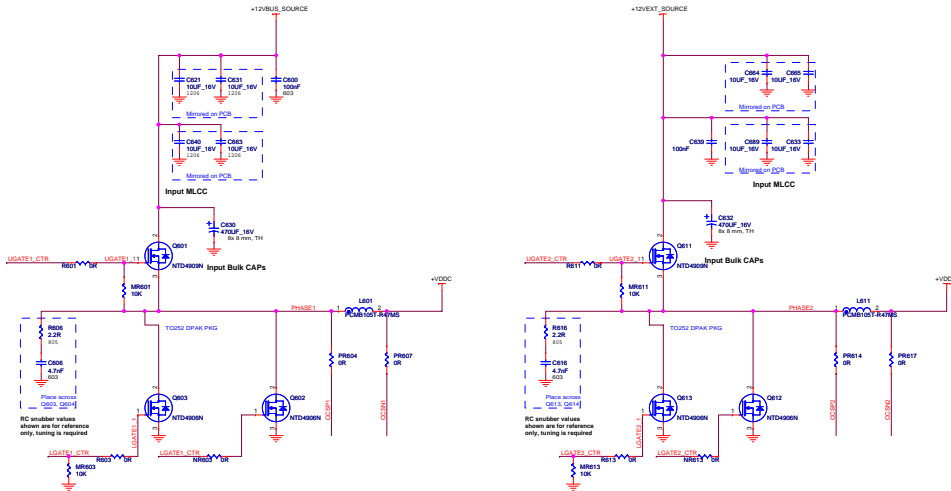


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Circuitry that have to be placed close to the device:  
 - current sense,  
 - compensation network,  
 - thermal compensation network (Droop, OCP, etc)

Table 1 MODE Pin Definition Table

VPM Mode	Mode Pin Status	Mode Pin Voltage (V)	Phase 1	Phase 2	Phase 3
3-Phase Mode	0	0	Enabled	Enabled	Enabled
2-Phase Mode	1	3.3	Enabled	Enabled	Disabled
1-Phase Mode	Floating	-1.7	Enabled	Disabled	Disabled

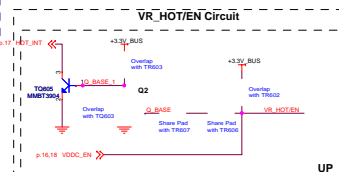
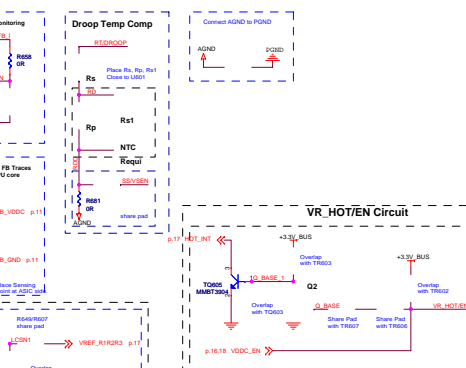
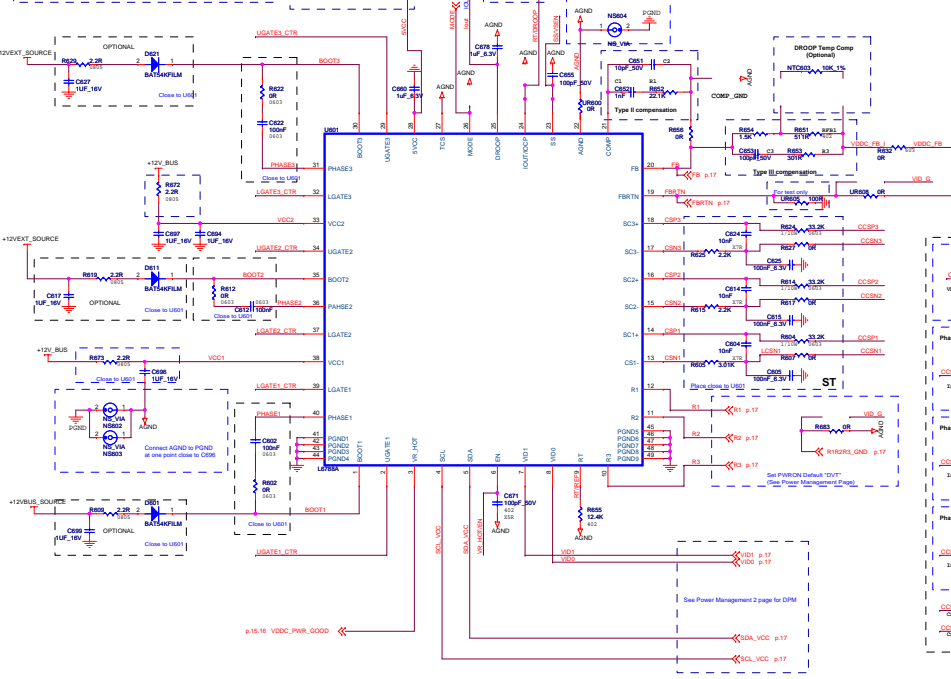


Table 1 VRHOT/EN Table

EN	Q1	Q2	VR_HOT/EN	IC	VR_HOT	GPIO
1	on	off	0	Disabled	/	1
0	off	on	5V	Enabled	No Warning	0
0	off	off	0.5V	Enabled	Warning	1

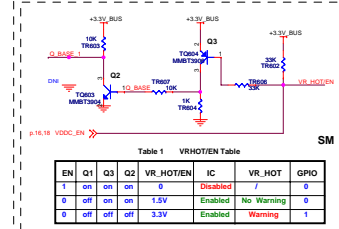


Table 1 VRHOT/EN Table

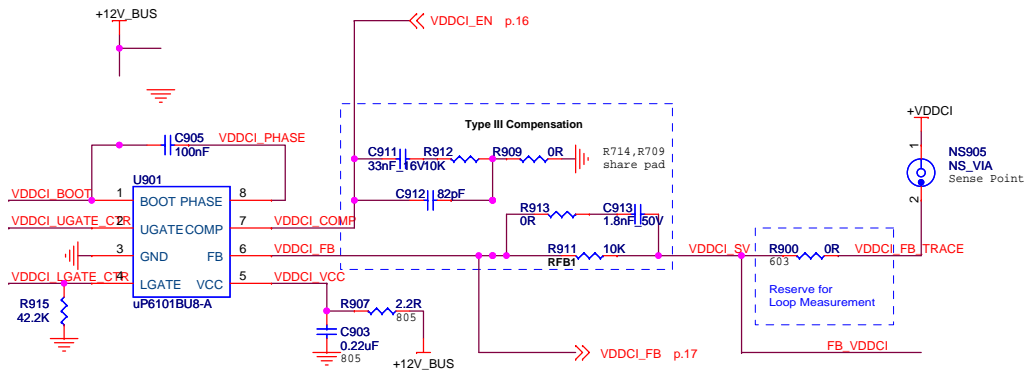
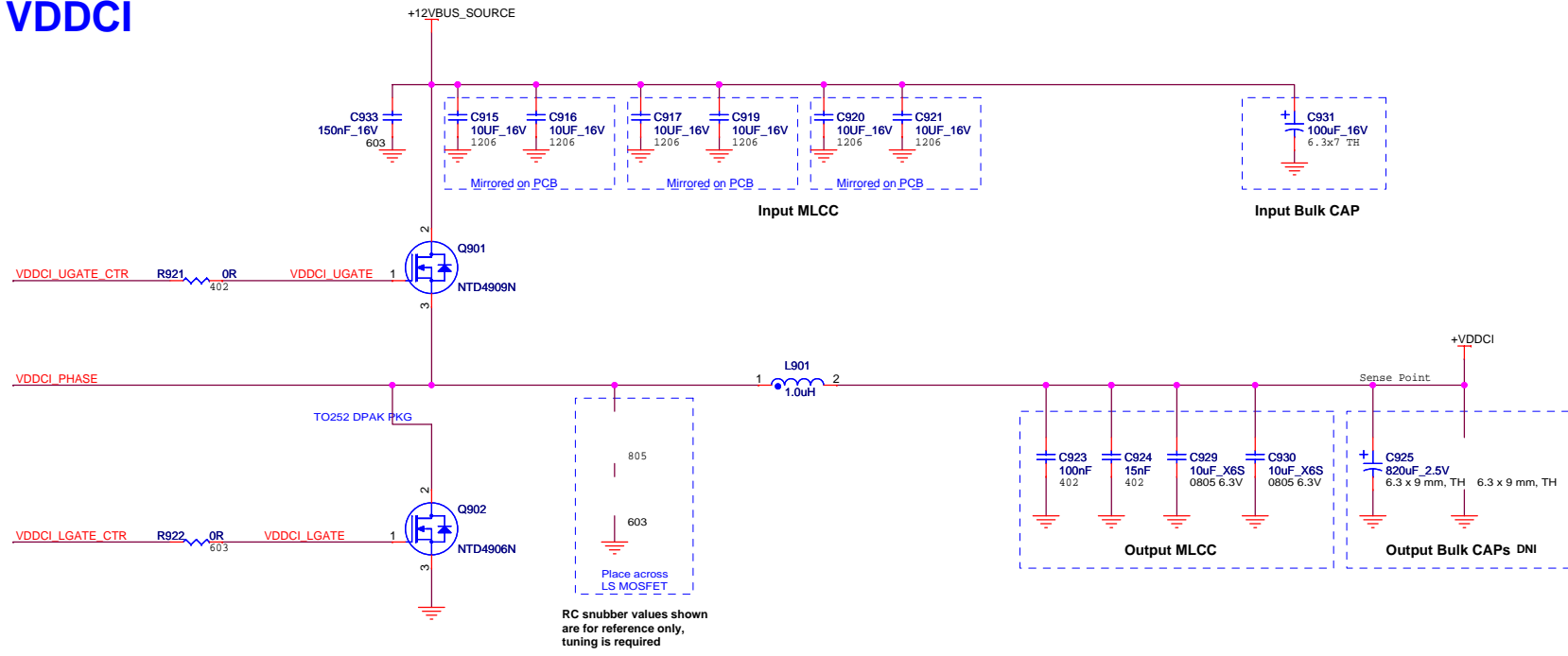
EN	Q1	Q2	Q3	VR_HOT/EN	IC	VR_HOT	GPIO
1	on	on	on	0	Disabled	/	0
0	off	on	on	1.5V	Enabled	No Warning	0
0	off	off	off	3.3V	Enabled	Warning	1

CASE1, CASE3 Special Case Power Up Detection  
 NOTE: This is for the IC that uses VDDC2 for EXT\_12V Detection.

Table 5 MODE Pin & Phase3 Strip Detection Table

App	Condition	MODE Pin	VPM Mode	Phase 3	IC Behavior
CASE 1	PowerUp without EXT_12V Cable	1	2-Ph Mode	Open	IC enabled without detecting EXT_12V (VDDC2) voltage.
CASE 2	PowerUp with EXT_12V Cable	1	2-Ph Mode	Pull Down	Detect EXT_12V (VDDC2) voltage before IC enable.

# (13) VDDCI



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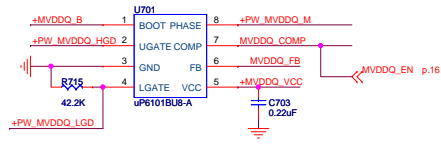


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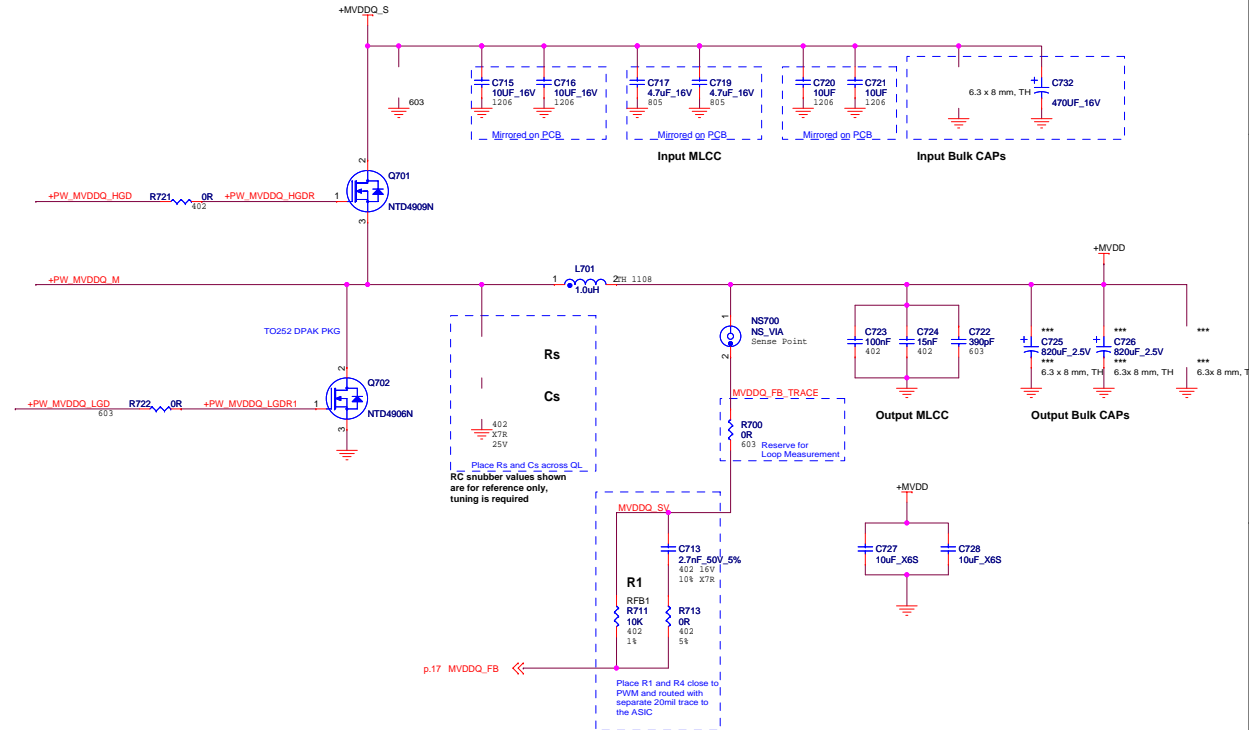


# (14) MVDDQ

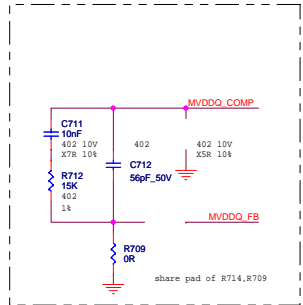


### Layout guideline

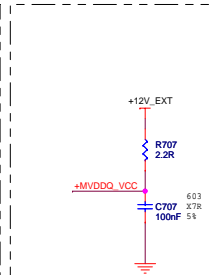
- 1-Position the controller (U703) such that LGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW\_MVDDQ\_LGD and PW\_MVDDQ\_HGD) as short and as wide as possible to reduce the trace inductance.
- 2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows:  
Vcc bypass cap is C703, and Boost cap is C705.
- 3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



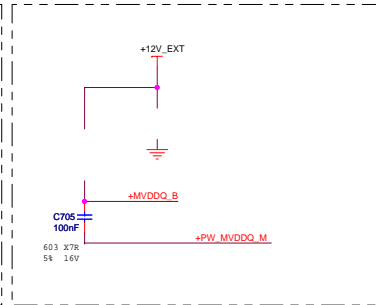
### COMPENSATION CIRCUIT



### FILTERED SMPS VCC



### BOOT CIRCUIT



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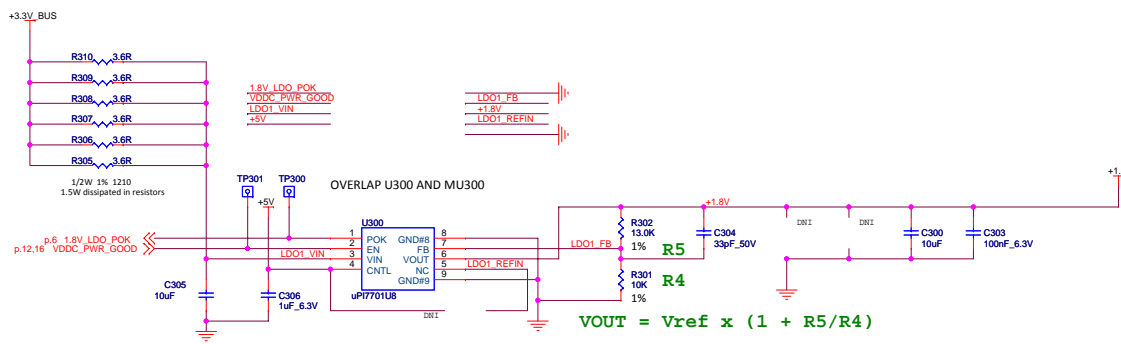


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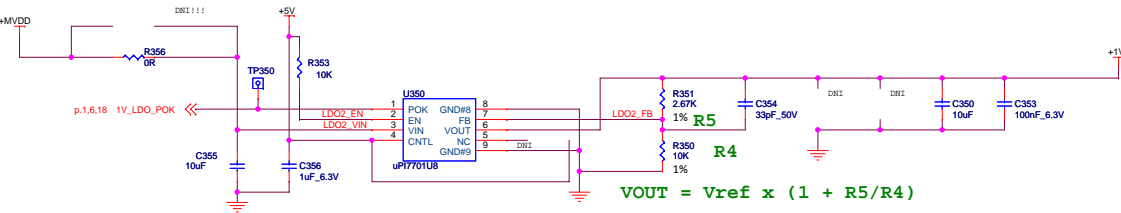


# (15) Linear Regulators

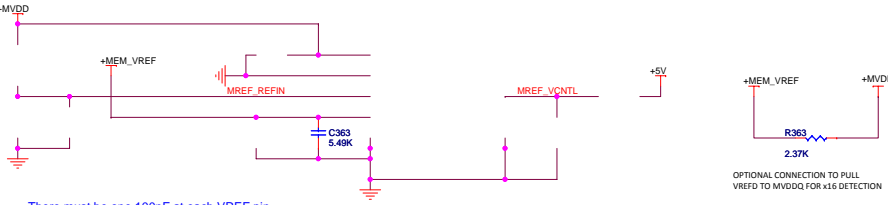
**LDO #1:** Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX  
 PCB: 50 to 70mm sq. copper area for cooling



**LDO #2:** Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX  
 PCB: 50 to 70mm sq. copper area for cooling

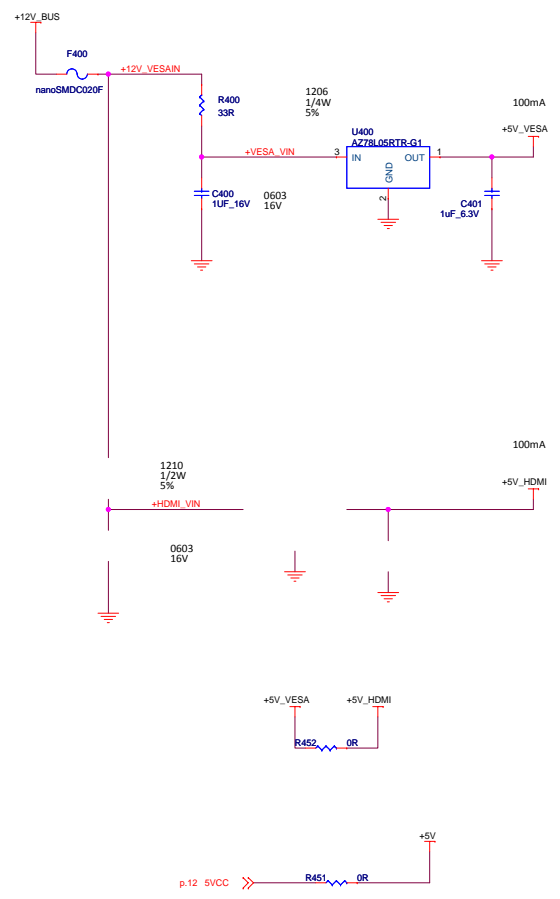


**Memory VREF:** Vin = MVDDQ Vout = 0.7xMVDDQ

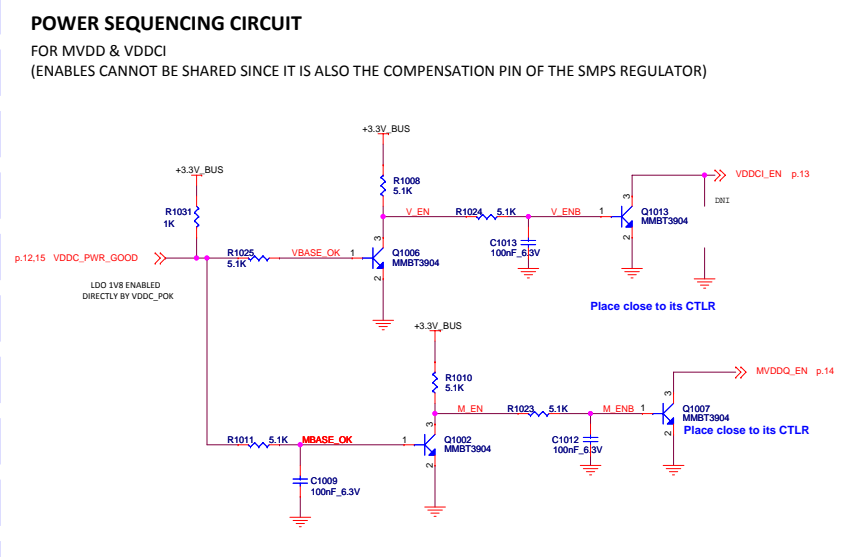
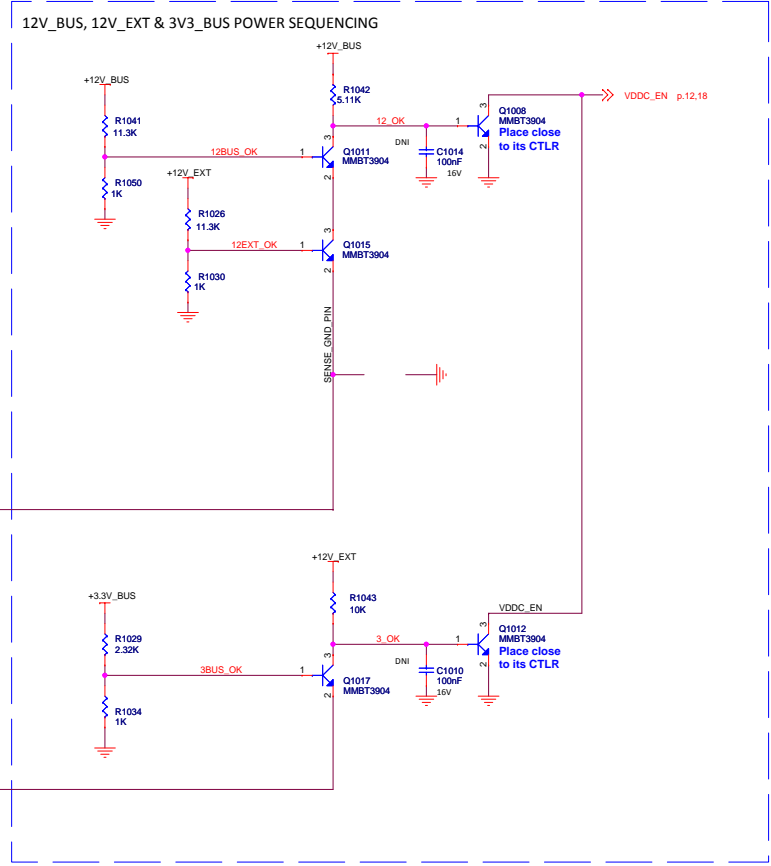
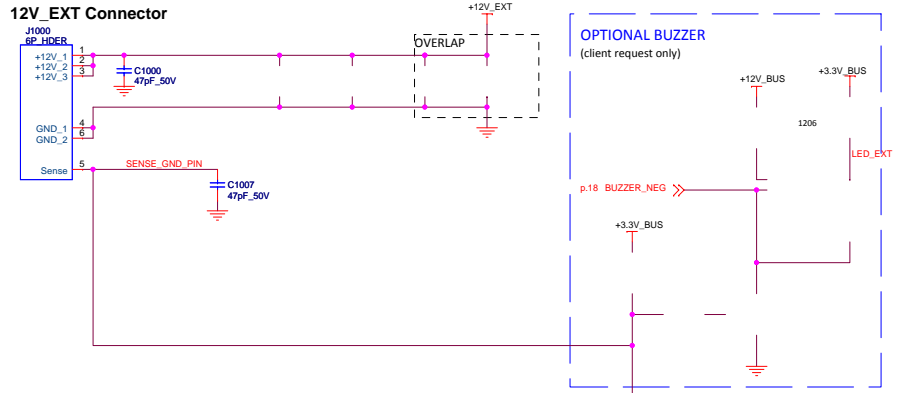


There must be one 100nF at each VREF pin  
 Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices

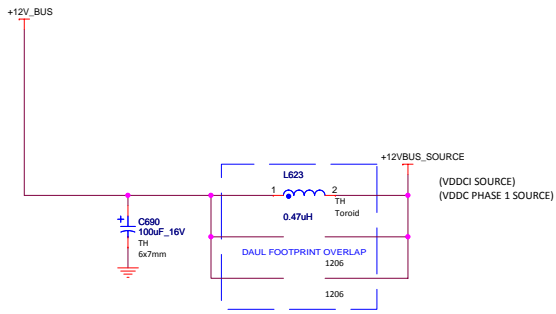
## Regulators for +5V, +5V\_VESA and +5V\_HDMI



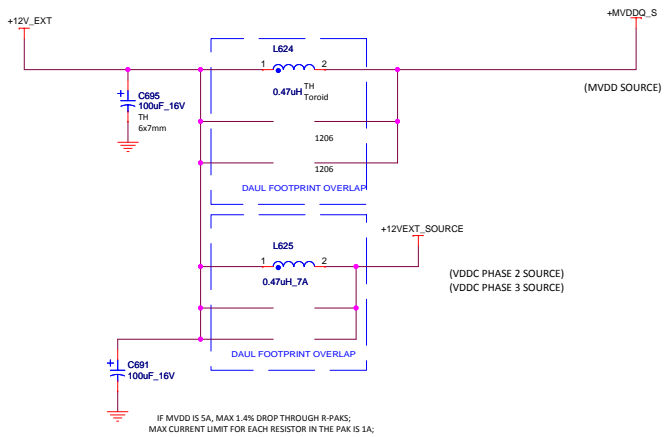
# (16) Power Management - Power Gating



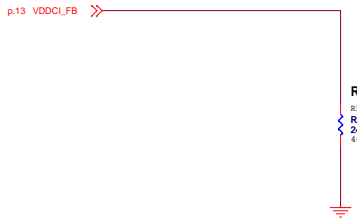
# (17) Power Management 2



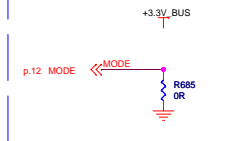
NOTE: Use ML623 with Fansik P/N 7120084000G



## VDDCI Low Side Divider



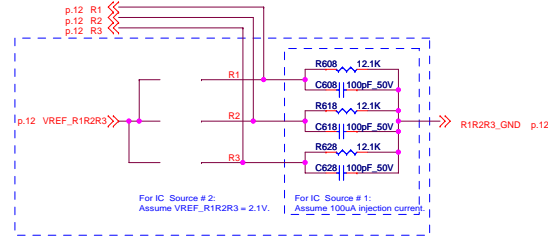
## MODE Pin Detection Circuit



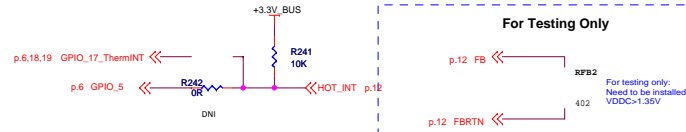
## VDDC Setting

Analog Reference (Refer R to AGND)  
Close to U601  
Be careful when changing R655 value (VDDC IREF)

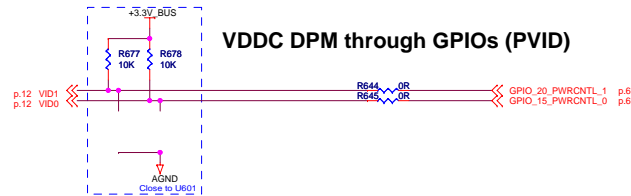
### SET DEFAULT VOLTAGE POWER-ON TABLE



### For Testing Only



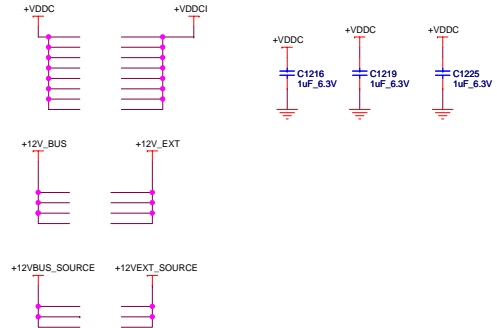
## VDDC DPM through GPIOs (PVID)



## VDDC I2C INTERFACE



ALL OR RESISTORS TO BE REMOVED FOR PRODUCTION;



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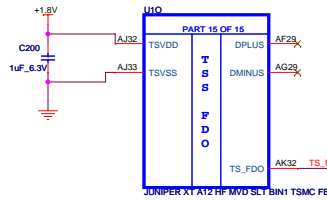
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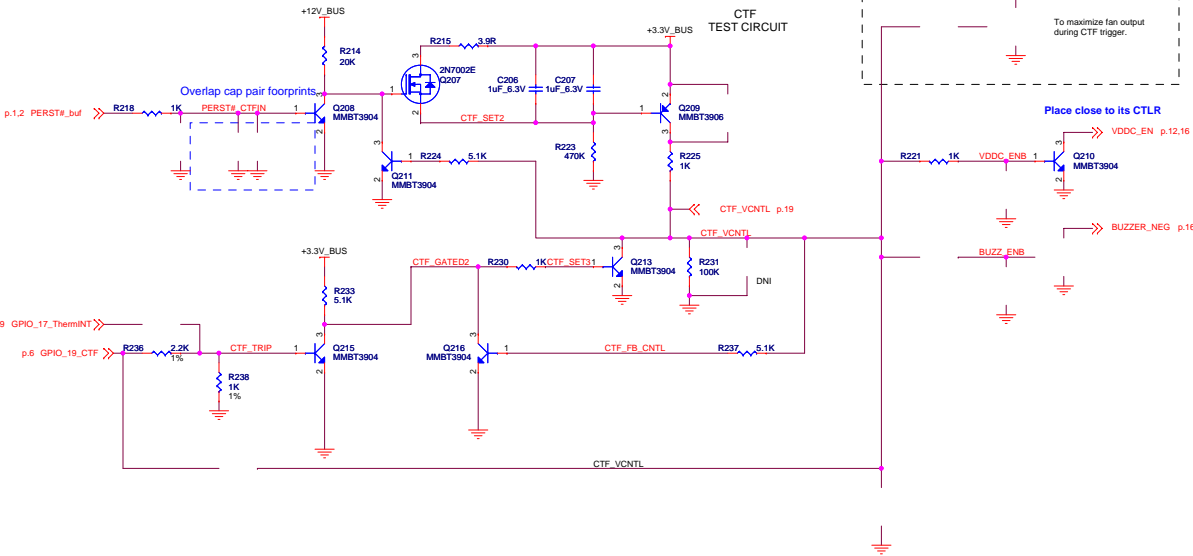
# (18) Mechanical and Thermal Management



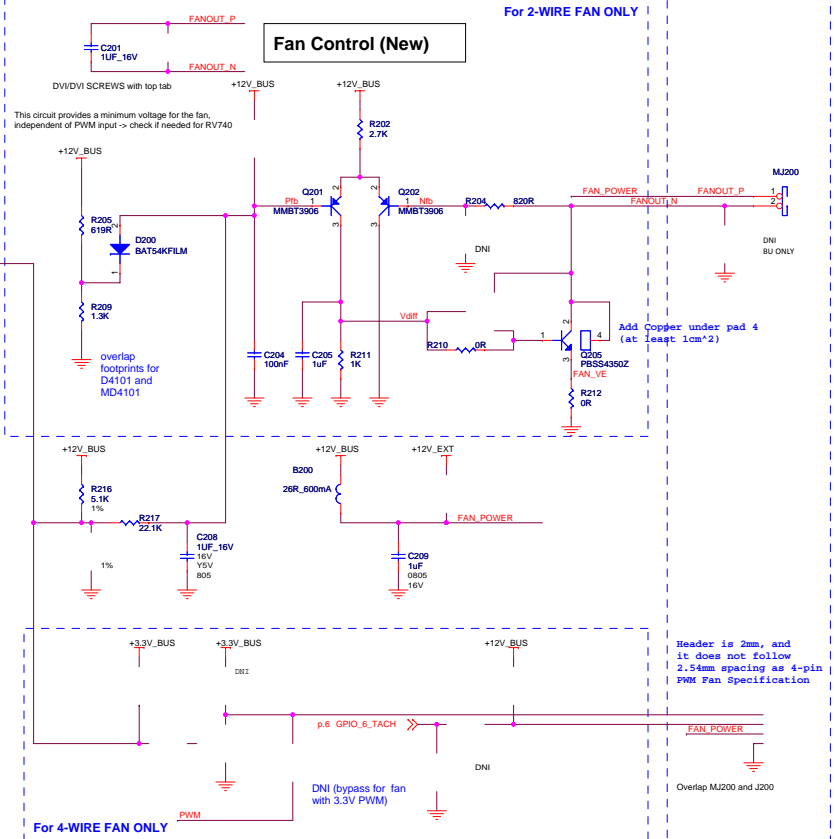
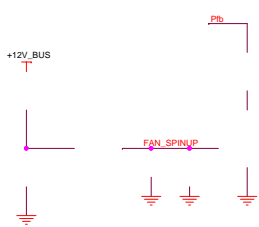
Warning: TS\_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.

## Critical Temperature Fault

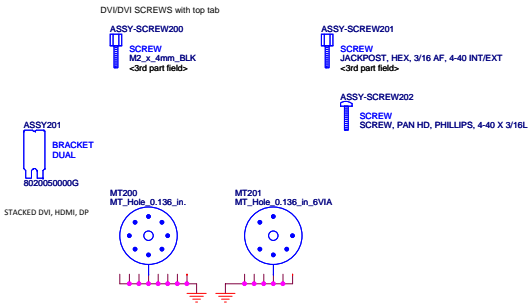
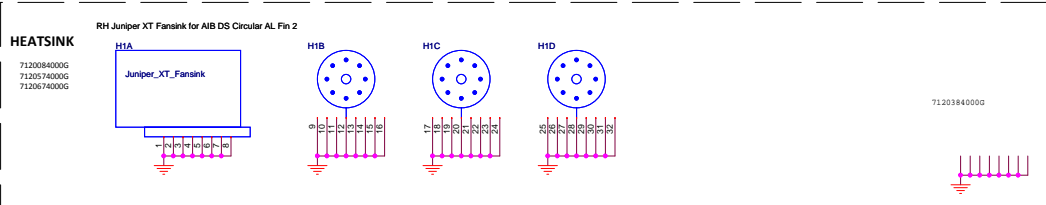


2-WIRE FAN SPINUP CIRCUIT  
PLEASE CHECK BOM FOR VALUES

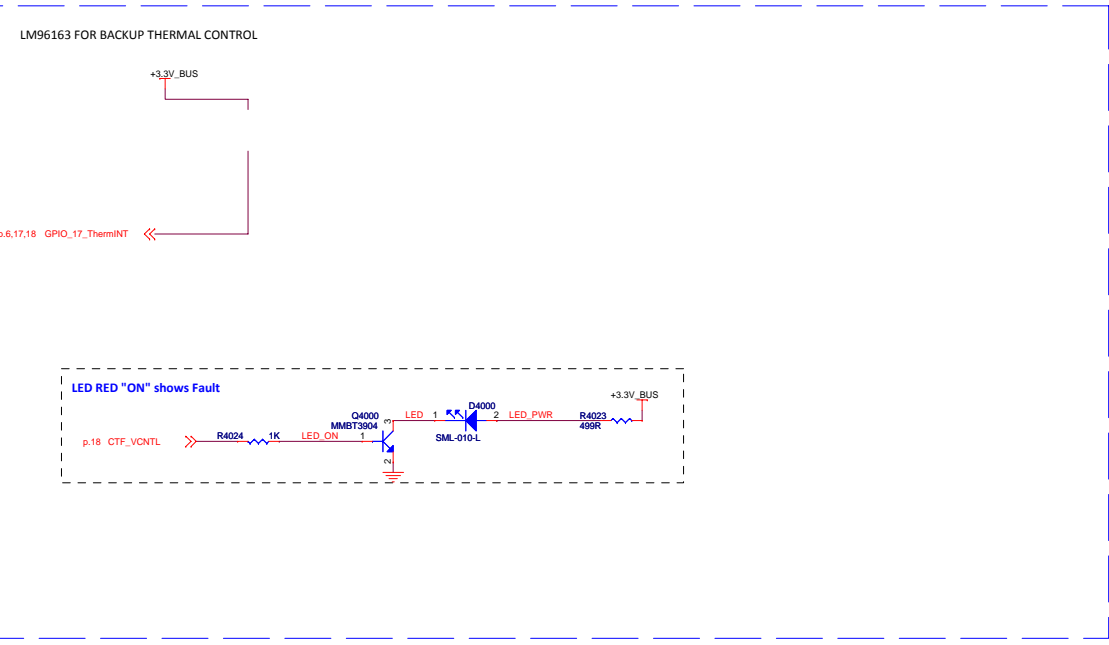
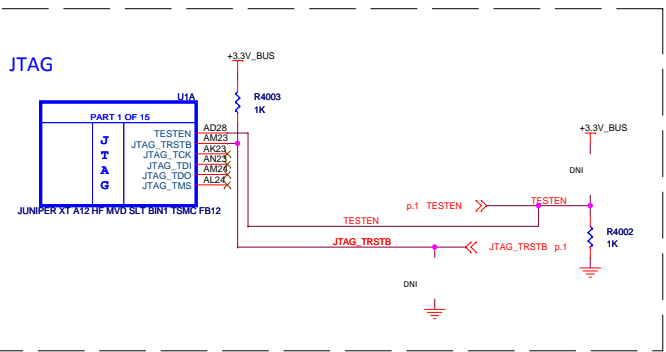


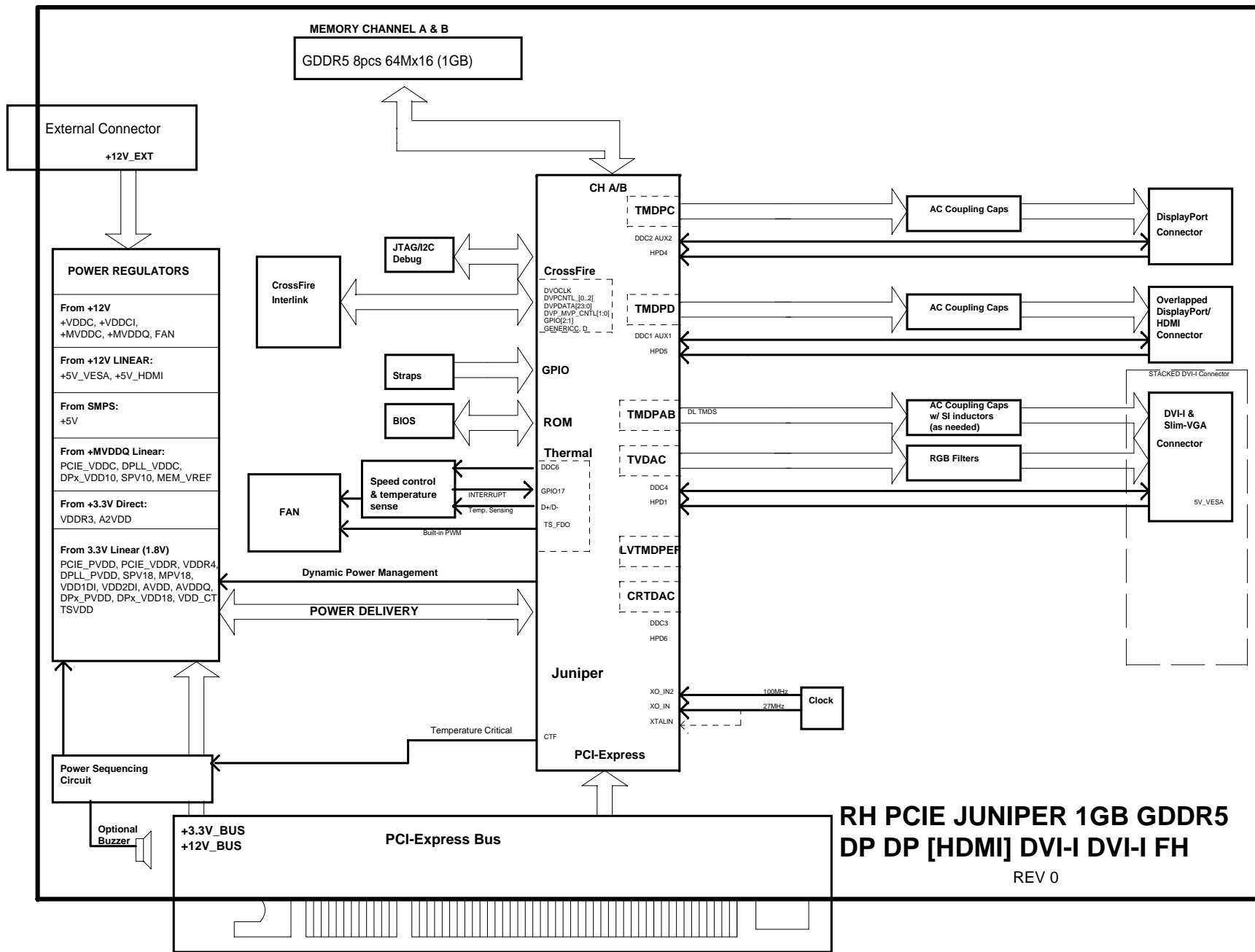
For 4-WIRE FAN ONLY

Header is 2mm, and it does not follow 2.54mm spacing as 4-pin PWM Fan Specification



# (19) Debug Circuits





**RH PCIe JUNIPER 1GB GDDR5  
DP DP [HDMI] DVI-I DVI-I FH**  
REV 0





Title

RH JUNIPER GDDR5 1GB DP+DP/HDMI+DVI /sVGA

Schematic No.

102-C01301-00

Date:

Tuesday, November 10, 2009

### REVISION HISTORY

**NOTE:** This schematic represents the PCB, it does not represent any specific SKU.  
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.  
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 50

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/07/14	JUNIPER GDDR5 1GB - BASED ON C010; VDDC/VDDCI/MVDD SMPS CHANGES; OTHER CIRCUITS UPDATED;
01	00B	2009/09/10	p. 1 - add reset gate circuit (C159,C160,C161,C162,MU101,R109,R110,R111,R112,U101); p. 2 - remove FB_VDDCI (NC U1.AG28); P. 11- add C670, C657,C673,C675,C682,C684,C688,C692,C693,MC673,MC675,MC682; p. 13- remove FB_VDDCI off-page; p. 19- remove J4004, add TESTEN/JTAG_TRSTB off-page;
02	00C	2009/09/25	p. 8- connect AUX1P/AUX1N DDC1CLK/DDC2DATA to DDCCLK_AUX5P/DDCDATA_AUX5N