Columbia/Tangiz Block Diagram

Project code: 91.4T301.001
PCB P/N : 48.4T301.0SA
REVISION : 06236-SA

CLK GEN.
ICS 9LPRS502
(RTM875T-605) 3
71.09502.00W

Mobile CPU
Merom 479
2G/2.33G
2.0G : 71.MEROM.A0U
2.33G : 71.MEROM.B0U
4, 5

G792
20

HOST BUS 667/800MHz@1.05V

DDR2
533/667 MHz
12,13

DDR2
533/667 MHz
12,13

533/667MHz

533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CREST.00U
6,7,8,9,10,11

X4 DMI
400MHz

C-Link0

TV Out 14
CRT 15
LCD 14
DVI 44
VGA Borad 28

PCB STACKUP
TOP
VCC
S
S
GND
BOTTOM

Line In
MIC In
14
31
INT.SPKR
Line Out
(No-SPDIF)

Codec
ALC268
30

AZALIA

OP AMP
G1431Q 31

OP AMP
G1412 31

MODEM
MDC Card
22

RJ11

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U
16,17,18,19

PCI BUS

TI
PCI7412
Cardbus
Cardreader
25/26

PCMCIA I/F

PWR SW
CP2211F 26

PCMCIA
SLOT
Support
TypeII 27

1394
CONN 27

MS/MS Pro/xD/
MMC/SD
5 in 1 27

LAN
GIGA
BCM5787M 23

TXFM 24

RJ45 24

PCIex1

Mini Card
Kedron a/b/g/n 29

LPC BUS

New card 29

PCI Express

SATA

PATA

USB

P2231NFC1 29

HDD 21

CDROM 21

MINI USB
BlueTooth 22

Finger print 34

USB
4 Port 22

CAMERA 13

KBC
Winbond
WPC8768L 32

SPI I/F

BIOS
W25X80-VSS 34

LPC
DEBUG
CONN. 35

Touch
Pad 33

INT.
KB 33

FIR 32

SYSTEM DC/DC
MAX8744 38

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)

SYSTEM DC/DC
Max8717 39

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)

TPS51100 41

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5915 41

1D8V_S3	1D25V_S0 (2A)

APL531230

3D3V_S0	2D5V_S0 (300mA)

APW5912 40

3D3V_S5	1D5V_S3 (7.5A)

ISL CHARGER
ISL6255 41

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
MAX8770 35,36

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

<Core Design>

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Title: BLOCK DIAGRAM
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ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

UMA

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Title: Reference

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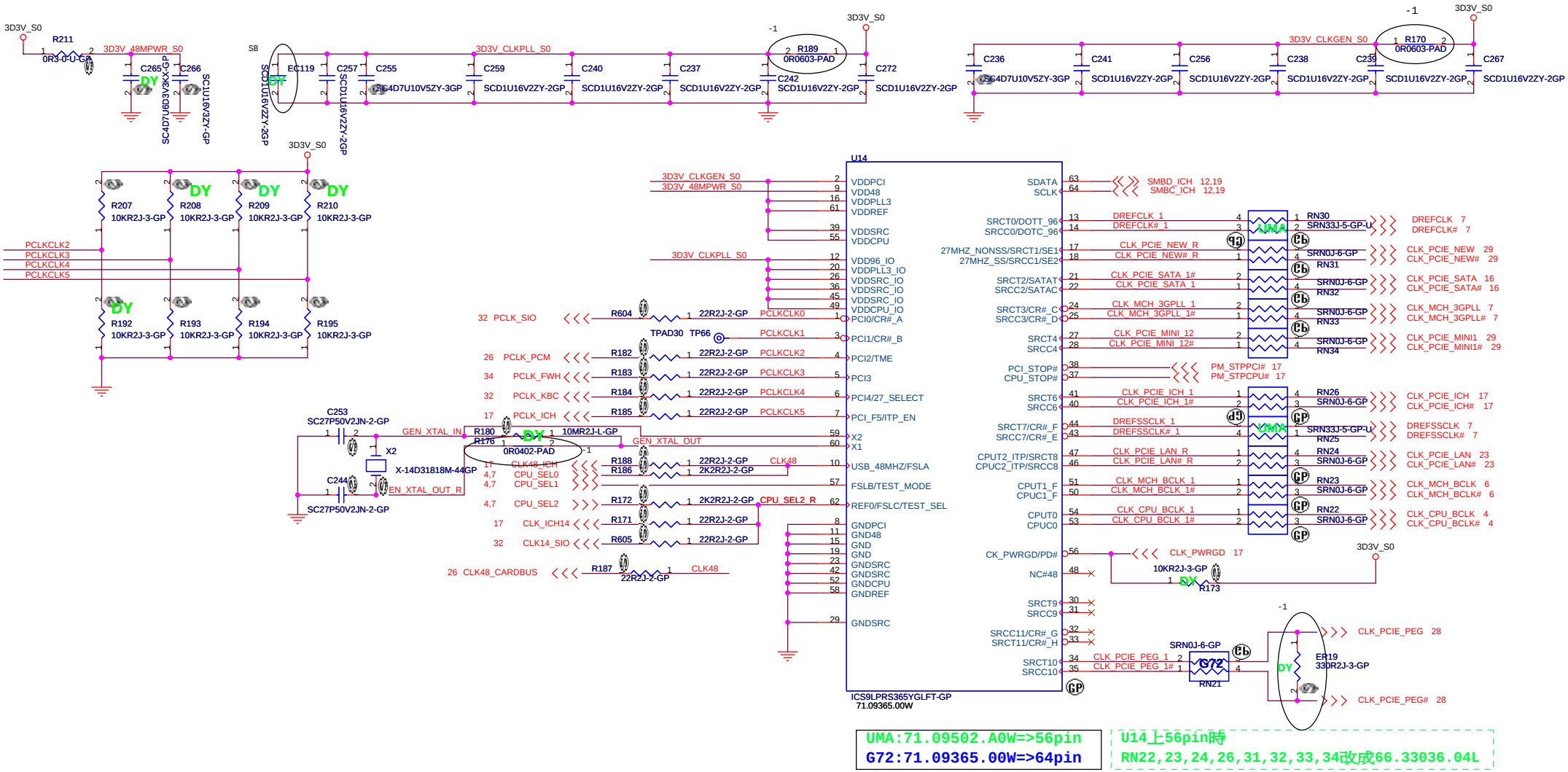

ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

UMA

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Title: Clock Generator

Size | Document Number: Columbia/Tangiz | Rev: SA

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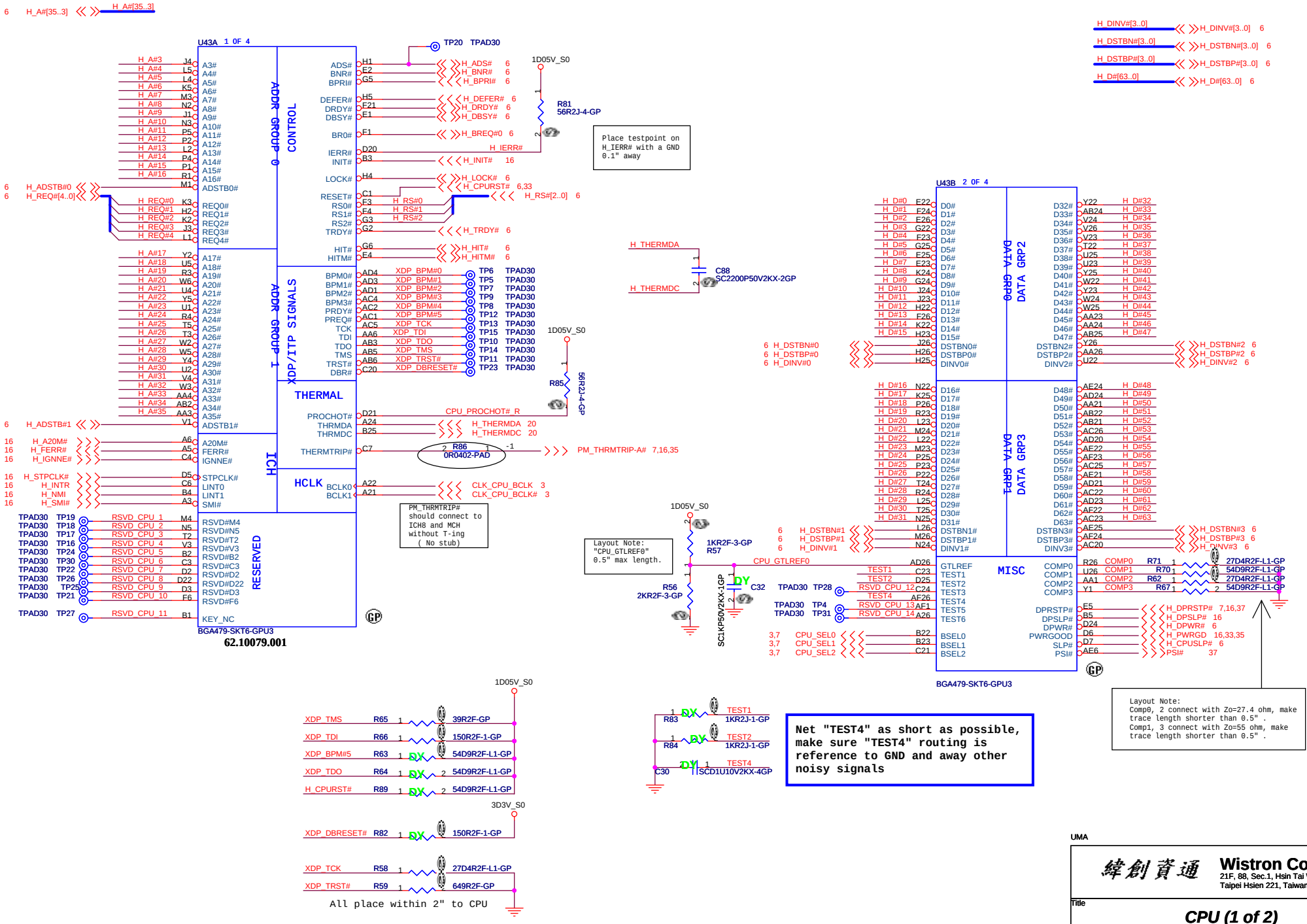
U43A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU3
62.10079.001
U43B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP1
DATA GRP3
MISC
BGA479-SKT6-GPU3
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH8 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
UMA
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CPU (1 of 2)
Columbia/Tangiz
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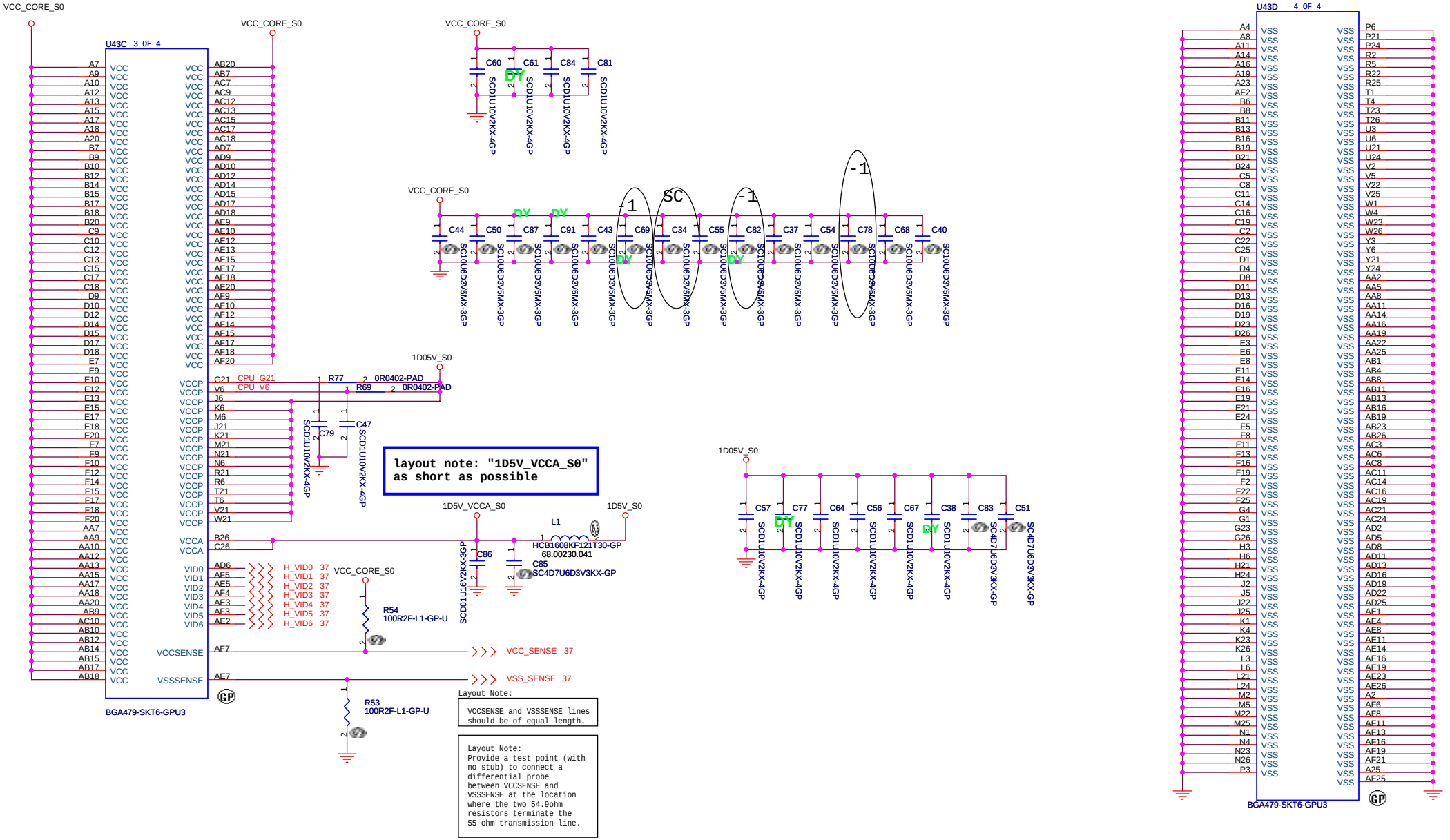

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Title	***CPU (2 of 2)***	
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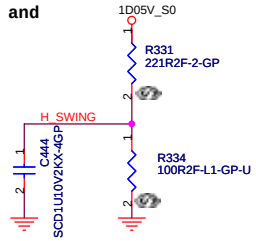
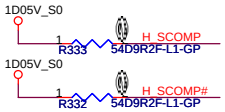
H_SWING routing Trace width and Spacing use 10 / 20 mil

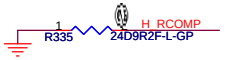
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

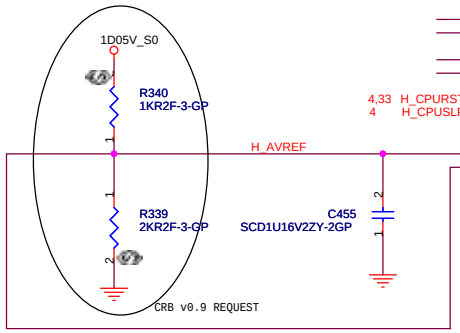


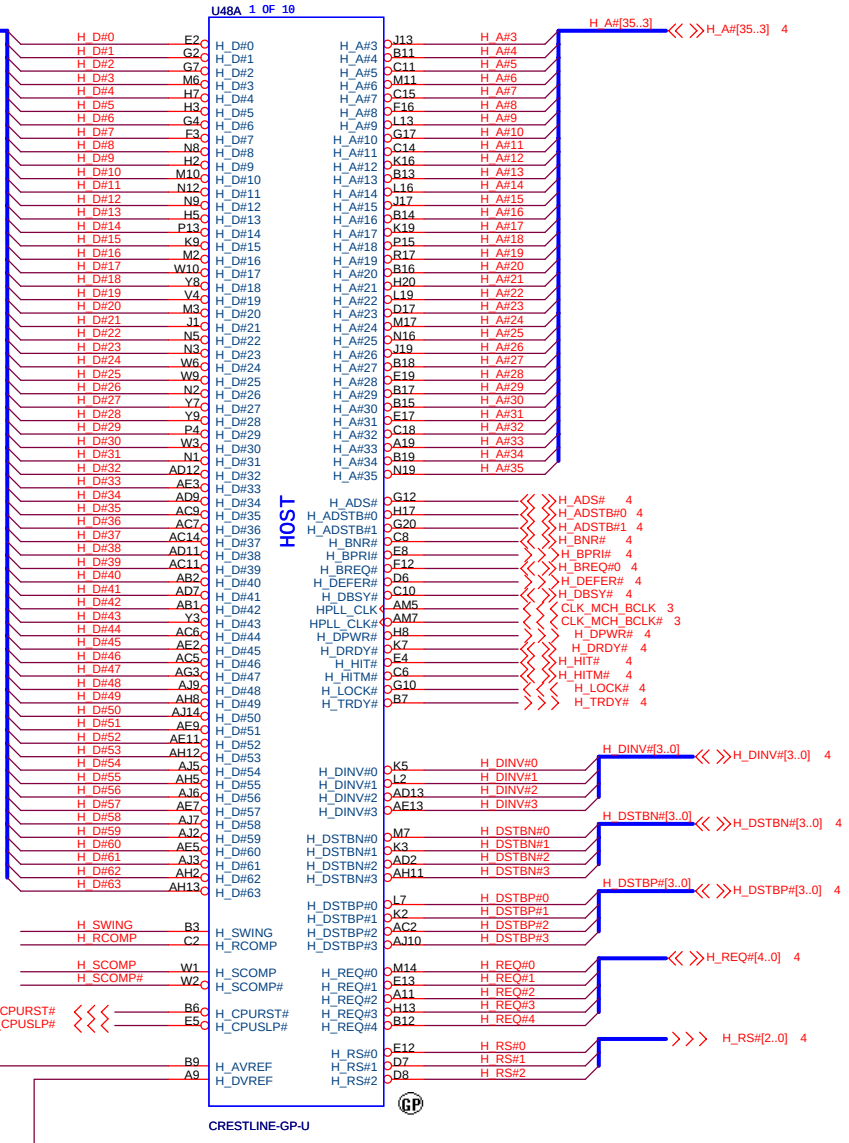
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





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Title	***GMCH (1 of 6)***	
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RSVD
RSVD#P36
RSVD#P37
RSVD#R35
RSVD#N35
RSVD#AR12
RSVD#AR13
RSVD#AM12
RSVD#AN13
RSVD#J12
RSVD#AR37
RSVD#AM36
RSVD#AL36
RSVD#AM37
RSVD#D20
RSVD#H10
RSVD#B51
RSVD#BJ20
RSVD#BK22
RSVD#BF19
RSVD#BH20
RSVD#BK18
RSVD#BJ18
RSVD#BF23
RSVD#BG23
RSVD#BC23
RSVD#BD24
RSVD#BH39
RSVD#AW20
RSVD#BK20
RSVD#B44
RSVD#C44
RSVD#A35
RSVD#B37
RSVD#B36
RSVD#B34
RSVD#C34

DDR MUXING
SM_CK0 SM_CK1 SM_CK2 SM_CK3
SM_CK#0 SM_CK#1 SM_CK#2 SM_CK#3
SM_CKE0 SM_CKE1 SM_CKE2 SM_CKE3
SM_CS#0 SM_CS#1 SM_CS#2 SM_CS#3
SM_ODT0 SM_ODT1 SM_ODT2 SM_ODT3
SM_RCOMP_VOH SM_RCOMP_VOL SM_RCOMP SM_RCOMP#
SM_VREF#AR49 SM_VREF#AW4
M_CLK_DDR0 M_CLK_DDR1 M_CLK_DDR2 M_CLK_DDR3
M_CLK_DDR#0 M_CLK_DDR#1 M_CLK_DDR#2 M_CLK_DDR#3
M_CKE0 M_CKE1 M_CKE2 M_CKE3
M_CS0# M_CS1# M_CS2# M_CS3#
M_ODT0 M_ODT1 M_ODT2 M_ODT3
SM_RCOMP_VOH SM_RCOMP_VOL
M_RCOMPP M_RCOMPN
DDR_VREF_S3

CLK
DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#
DREFCLK DREFCLK# DREFSSCLK DREFSSCLK#
PEG_CLK PEG_CLK#
CLK_MCH_3GPLL CLK_MCH_3GPLL#

DMI
DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3

CFG
CPU_SEL0 CPU_SEL1 CPU_SEL2
CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19 CFG20
DUMMY-R2 CFG18 CFG19 CFG20 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17

GRAPHICS VID
GFX_VID0 GFX_VID1 GFX_VID2 GFX_VID3 GFX_VR_EN
TP48 TP51 TP116 TP49 TP50 TPAD28

PM
PM_BM_BUSY# PM_DPRSTP# PM_EXT_TS#0 PM_EXT_TS#1 PWROK RSTIN# THERMTRIP# DPRSLPVR
H_DPRSTP# PM_EXTTS#0 PM_EXTTS#1 NB_THERMTRIP# PM_DPRSLPVR

ME
CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF
CL_CLK0 CL_DATA0 PWROK RSTIN#
CLPWROK_MCH MCH_CLVREF

NC
NC#BJ51 NC#BK51 NC#BK50 NC#BL50 NC#BL49 NC#BL3 NC#BL2 NC#BK1 NC#BJ1 NC#E1 NC#A5 NC#C51 NC#B50 NC#A50 NC#A49 NC#BK2

MISC
SDVO_CTRL_CLK SDVO_CTRL_DATA CLKREQ# ICH_SYNC#
CLK_3GPLLREQ# MCH_ICH_SYNC#
TEST1 TEST2 TEST2_GMCH

CRESTLINE-GP-U

UMA
U48C 3 OF 10

LVDS
L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK L_CTRL_DATA L_DDC_CLK L_DDC_DATA L_VDD_EN
LVDS_IBG LVDS_VBG LVDS_VREFH LVDS_VREFL
LVDSA_CLK# LVDSA_CLK LVDSB_CLK# LVDSB_CLK
LVDSA_DATA#0 LVDSA_DATA#1 LVDSA_DATA#2 LVDSA_DATA#3
LVDSA_DATA0 LVDSA_DATA1 LVDSA_DATA2 LVDSA_DATA3
LVDSB_DATA#0 LVDSB_DATA#1 LVDSB_DATA#2
LVDSB_DATA0 LVDSB_DATA1 LVDSB_DATA2
L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK L_CTRL_DATA L_DDC_CLK L_DDC_DATA L_VDD_EN
LIBG L_LVBG
TPAD30 TP52 TPAD30 TP53 TPAD30 TP54

TV
TVA_DAC TVB_DAC TVC_DAC
TVA_RTN TVB_RTN TVC_RTN
TV_DCONSEL0 TV_DCONSEL1

VGA
CRT_BLUE CRT_BLUE# CRT_GREEN CRT_GREEN# CRT_RED CRT_RED#
CRT_DDC_CLK CRT_DDC_DATA CRT_VSYNC CRT_TVO_IREF CRT_HSYNC
GMCH_BLUE GMCH_GREEN GMCH_RED GMCH_DDCCLK GMCH_DDCDATA GMCH_VSYNC GMCH_VS GMCH_HS GMCH_HSYNC CRT_IREF

PCI_EXPRESS GRAPHICS
PEG_COMPI PEG_COMPO
PEG_RX#0 PEG_RX#1 PEG_RX#2 PEG_RX#3 PEG_RX#4 PEG_RX#5 PEG_RX#6 PEG_RX#7 PEG_RX#8 PEG_RX#9 PEG_RX#10 PEG_RX#11 PEG_RX#12 PEG_RX#13 PEG_RX#14 PEG_RX#15
PEG_RXN0 PEG_RXN1 PEG_RXN2 PEG_RXN3 PEG_RXN4 PEG_RXN5 PEG_RXN6 PEG_RXN7 PEG_RXN8 PEG_RXN9 PEG_RXN10 PEG_RXN11 PEG_RXN12 PEG_RXN13 PEG_RXN14 PEG_RXN15
PEG_RXP0 PEG_RXP1 PEG_RXP2 PEG_RXP3 PEG_RXP4 PEG_RXP5 PEG_RXP6 PEG_RXP7 PEG_RXP8 PEG_RXP9 PEG_RXP10 PEG_RXP11 PEG_RXP12 PEG_RXP13 PEG_RXP14 PEG_RXP15
PEG_TX#0 PEG_TX#1 PEG_TX#2 PEG_TX#3 PEG_TX#4 PEG_TX#5 PEG_TX#6 PEG_TX#7 PEG_TX#8 PEG_TX#9 PEG_TX#10 PEG_TX#11 PEG_TX#12 PEG_TX#13 PEG_TX#14 PEG_TX#15
PEG_TXN0 PEG_TXN1 PEG_TXN2 PEG_TXN3 PEG_TXN4 PEG_TXN5 PEG_TXN6 PEG_TXN7 PEG_TXN8 PEG_TXN9 PEG_TXN10 PEG_TXN11 PEG_TXN12 PEG_TXN13 PEG_TXN14 PEG_TXN15
PEG_TXP0 PEG_TXP1 PEG_TXP2 PEG_TXP3 PEG_TXP4 PEG_TXP5 PEG_TXP6 PEG_TXP7 PEG_TXP8 PEG_TXP9 PEG_TXP10 PEG_TXP11 PEG_TXP12 PEG_TXP13 PEG_TXP14 PEG_TXP15
GTXN0 GTXN1 GTXN2 GTXN3 GTXN4 GTXN5 GTXN6 GTXN7 GTXN8 GTXN9 GTXN10 GTXN11 GTXN12 GTXN13 GTXN14 GTXN15
GTXP0 GTXP1 GTXP2 GTXP3 GTXP4 GTXP5 GTXP6 GTXP7 GTXP8 GTXP9 GTXP10 GTXP11 GTXP12 GTXP13 GTXP14 GTXP15
G72

1D05V_S0 R155 24D9R2F-L-GP PEG_CMP
PEG_RXN[15..0] 28
PEG_RXP[15..0] 28
PEG_TXN[15..0] 28
PEG_TXP[15..0] 28
C203 C189 C205 C211 C213 C200 C192 C207 C229 C221 C217 C517 C228 C226 C514 C219 SCD1U10V2KX-5GP
C201 C187 C204 C208 C215 C193 C190 C206 C224 C220 C216 C518 C227 C225 C515 C218 SCD1U10V2KX-5GP

3D3V_S0 RN15 SRN2K2J-8-GP
TV_DCONSEL0 TV_DCONSEL1

1D8V_S3 R350 20R2J-GP M_RCOMPP R348 20R2J-GP M_RCOMPN

3D3V_S0 R110 R104 R133 R106 R126 R117 R101 R121 R108 R107 R125 R122 R131 R124 R102 R120 R109 R127 DUMMY-R2 CFG18 CFG19 CFG20 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17

4,16,37 H_DPRSTP# R152 0R0402-PAD H_DPRSTP# PM_BMBUSY# R159 0R0402-PAD PM_EXTTS#0 PM_EXTTS#1
17,37 VGATE_PWRGD
17,20 PWROK 7,21,23,28,29,32,34 PLT_RST1# R158 0R0402-PAD R105 100R2J-2-GP
PWROK_GD RSTIN# PM_DPRSLPVR
C153 SC100P50V2JN-3GP
4,16,35 PM_THRMTRIP-A# R103 0R0402-PAD
17,37 PM_DPRSLPVR R134 0R0402-PAD

3D3V_S0 R141 10KR2J-3-GP CLK_3GPLLREQ#

1D25V_S0 R161 1KR2F-3-GP R157 392R2F-GP C209 SCD1U10V2KX-4GP

1D8V_S3 R353 1KR2F-3-GP
R356 3K01R2F-3-GP C468 SCD01U16V2KX-3GP C465 SC2D2U6D3V3MX-1-GP SM_RCOMP_VOH
R358 1KR2F-3-GP C473 SCD01U16V2KX-3GP C474 SC2D2U6D3V3MX-1-GP SM_RCOMP_VOL

UMA R360 1K3R2F-1-GP
UMA R369 33R2F-3-GP
UMA R368 33R2F-3-GP

FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil

UMA R142 150R2F-1-GP GMCH_BLUE
UMA R139 150R2F-1-GP GMCH_GREEN
UMA R137 150R2F-1-GP GMCH_RED
FOR Discrete change R137, R139 & R142 to 0 ohm

SB R128 150R2F-1-GP TV_DACA R129 150R2F-1-GP TV_DACB R130 150R2F-1-GP TV_DACC UMA

UMA GMCH_BL_ON R149 100KR2J-1-GP GMCH_LCDVDD_ON R138 100KR2J-1-GP LIBG R154 2K4R2F-GP
G72 GMCH_VS R153 0R2J-2-GP GMCH_HS R148 0R2J-2-GP

3D3V_S0 RN20 LCTLB_DATA LCTLA_CLK PM_EXTTS#0 PM_EXTTS#1 SRN10KJ-6-GP

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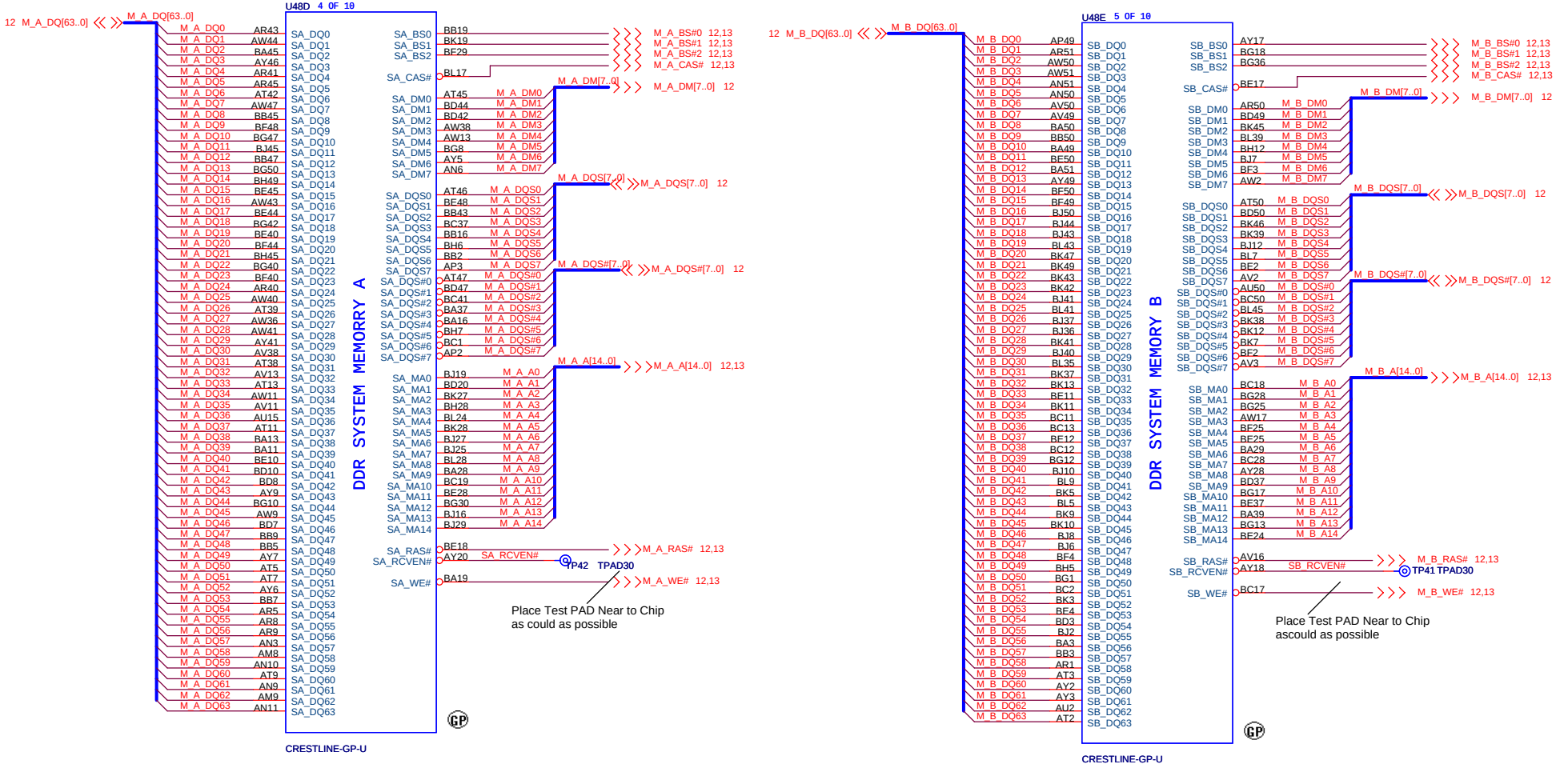
Title: GMCH (2 of 6)
Size: Document Number: Columbia/Tangiz Rev: -1
Date: Monday, February 26, 2007 Sheet 7 of 45



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Title: ***GMCH (3 of 6)***

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VCC_NCTF + VCC=1573mA

1573mA

U48F 6 OF 10

VCC CORE

R143 0R0402-PAD

POWER

3138mA

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

CRESTLINE-GP-U

SB:Remove R123,R132,R136,R144

VCC_AXG_NCTF + VCC_AXG=7700mA

UMA

SB:DIS remove 0 ohm on C129,C210,C158,C161

FOR VCC CORE AND VCC NCTF

308 mils from the Edge

Coupling CAP

FOR VCC CORE

Coupling CAP 370 mils from the Edge

U48G 7 OF 10

VCC NCTF

VSS NCTF

VSS SCB

VSS AXM

VSS AXM NCTF

FOR VCC AXM NCTF AND VCC AXM

Place on the Edge

VCC_AXM_NCTF + VCC_AXM=540mA

Place CAP where LVDS and DDR2 taps

FOR VCC SM

Place on the Edge

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Title: GMCH (4 of 6)

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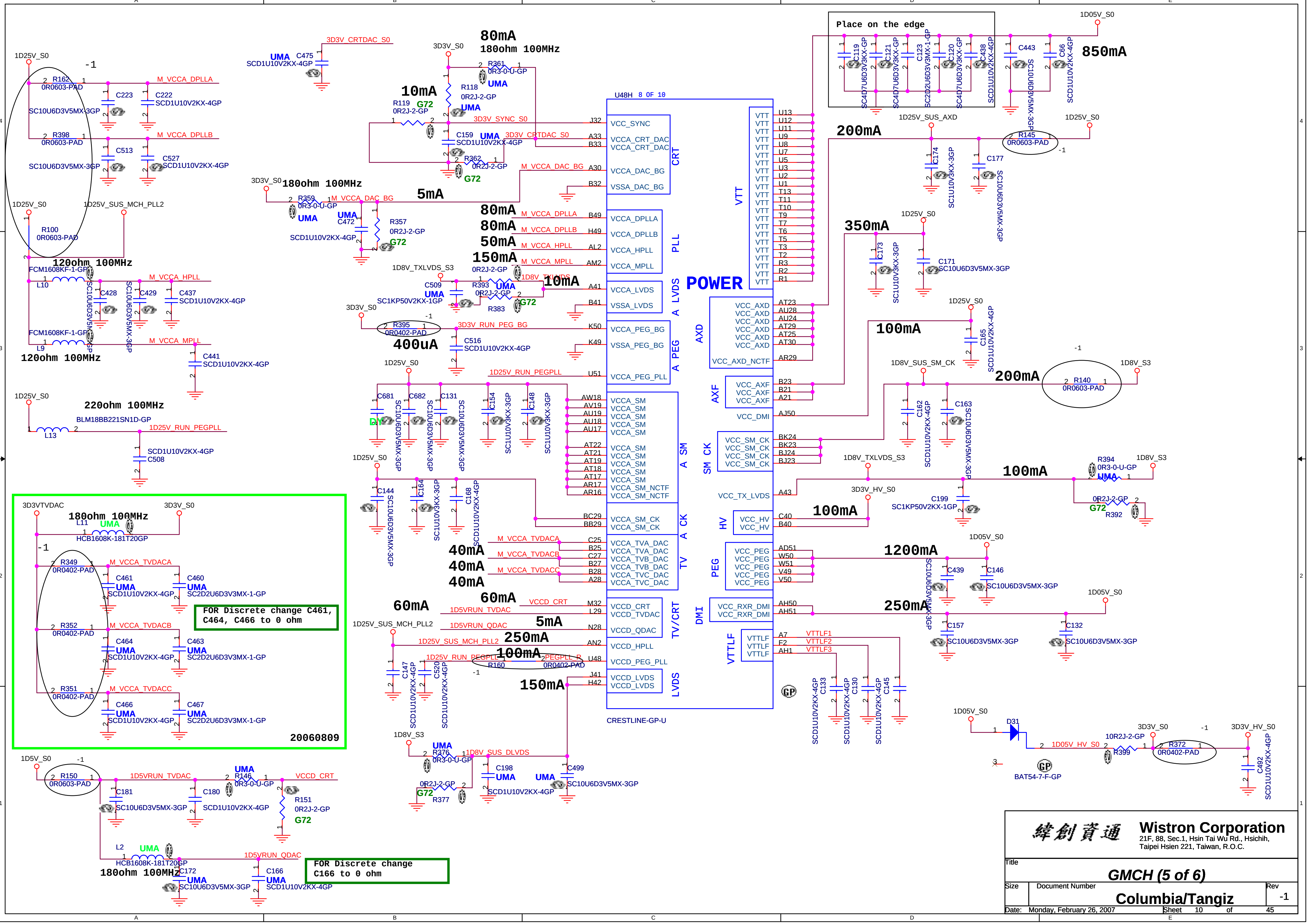

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Title	GMCH (5 of 6)
Size / Document Number	Columbia/Tangiz
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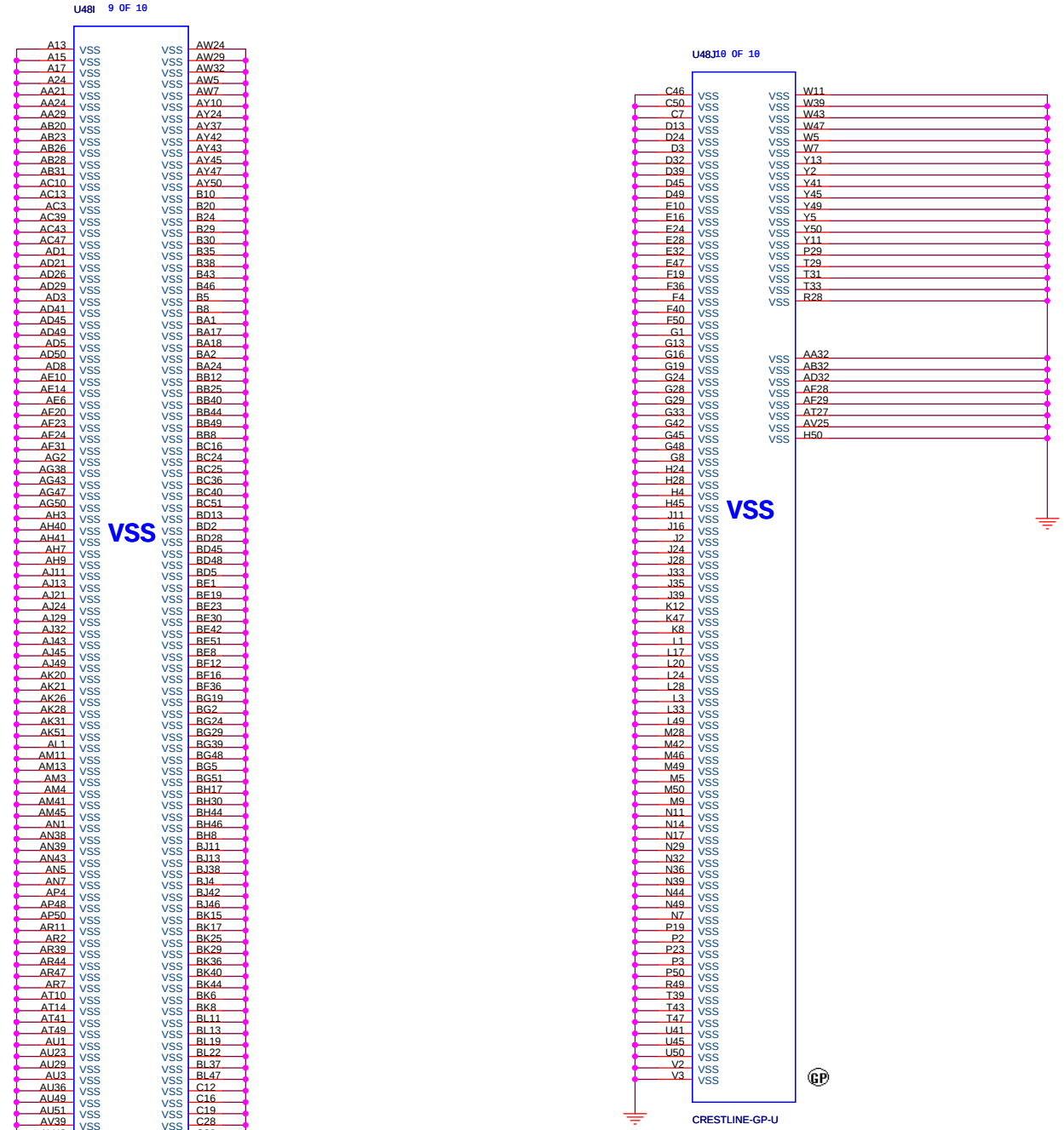

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Title: ***GMCH (6 of 6)***

Size	Document Number	Rev
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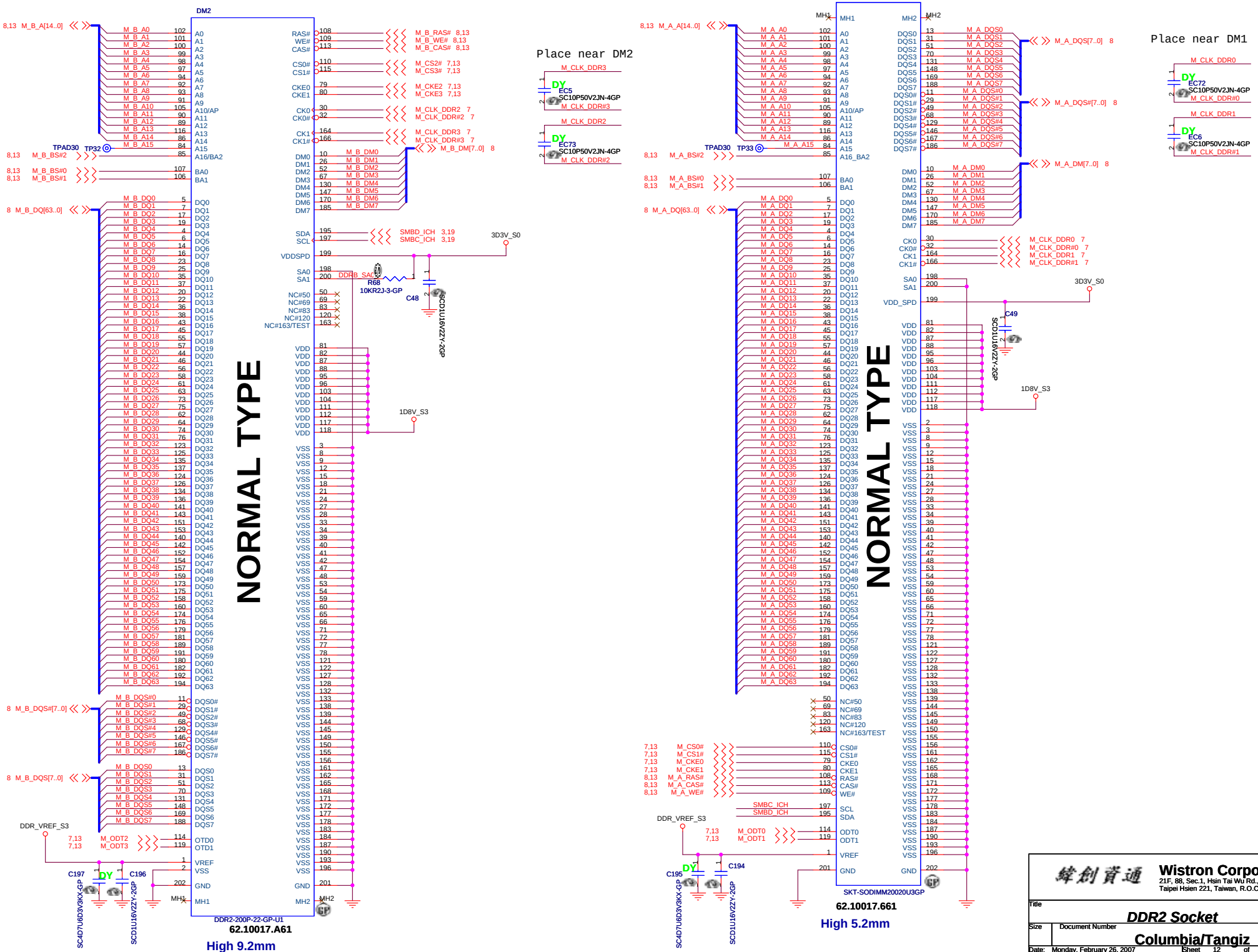
DM2
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
DM1
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
Place near DM2
Place near DM1
M_CLK_DDR3
M_CLK_DDR2
EC5
EC73
EC72
EC6
SC10P50V2JN-4GP
M_CLK_DDR#3
M_CLK_DDR#2
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR#0
M_CLK_DDR#1
DY
R68
10KR2J-3-GP
C48
C49
C194
C195
C196
C197
SCD1U16V2ZY-2GP
SC4D7U6D3V3KX-GP
DDR_VREF_S3
3D3V_S0
1D8V_S3
SMBC_ICH
SMBD_ICH
TPAD30
TP32
TP33
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Title
DDR2 Socket
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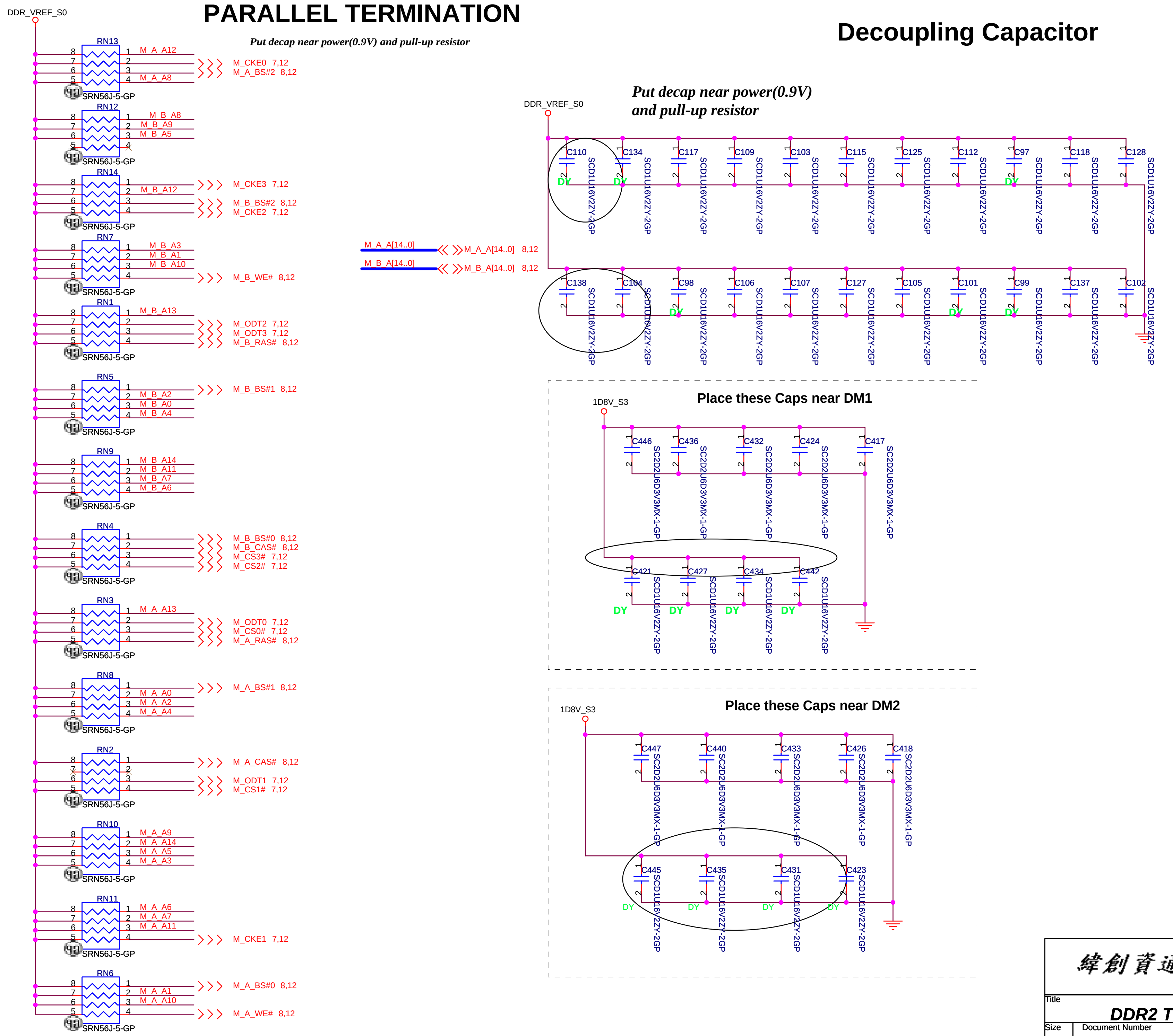
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor



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Title		
DDR2 Termination Resistor		
Size	Document Number: **Columbia/Tangiz**	Rev: -1
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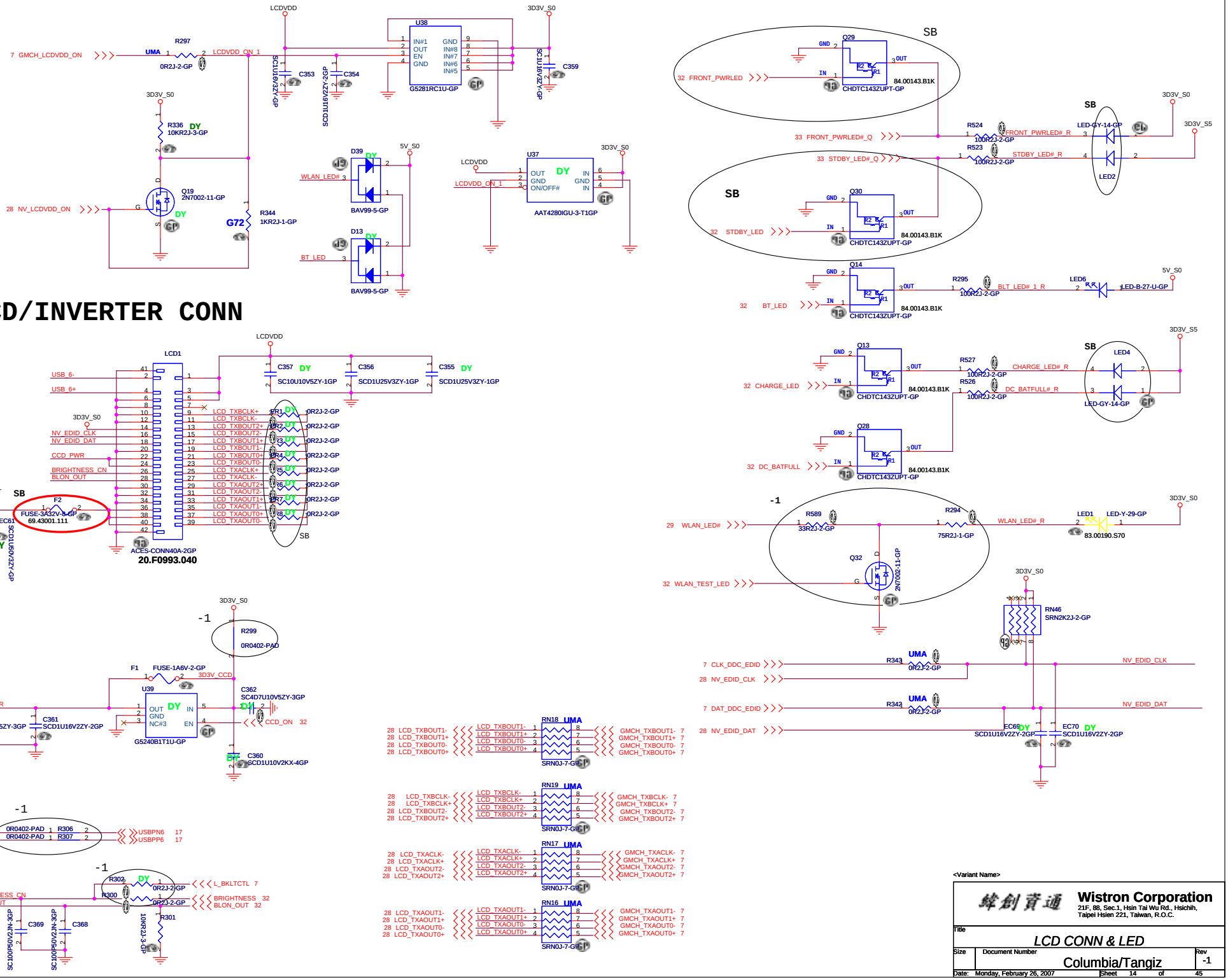
LCD/INVERTER CONN



<Variant Name>

華創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD CONN & LED	
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CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

28 NV_RED
7 GMCH_RED
28 NV_GREEN
7 GMCH_GREEN
28 NV_BLUE
7 GMCH_BLUE
R113 R112 R111 UMA 0R2J-2-GP
L8 L7 L6 FCB1608CF-GP
CRT_R CRT_G CRT_B
R328 R325 R323 150R2F-1-GP
C416 C411 C407 SC22P50V2JN-4GP DY
C420 C413 C409 SC6D8P50V2DN-GP UMA
SC
-1

For DIS
C420--->78.15034.1FL
C413,C409--->78.18034.1FL

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT1
CRT_R CRT_G CRT_B
DAT_DDC1_5
CRT_VSYNC1
C415 SC100P50V2JN-3GP
C405 SC18P50V2JN-1-GP
CRT_HSYNC1
5V_CRT_S0
CLK_DDC1_5
C419 SCD01U16V2KX-3GP
C414 SC100P50V2JN-3GP
C406 SC18P50V2JN-1-GP
MH1 MH2
VIDEO-15-21-U4-GP
20.20334.015

32 CRT_DEC#
R321 470R2J-2-GP
CRT_DEC_R
C404 SC100P50V2JN-3GP
D1 BAV99-5-GP
5V_S0

Hsync & Vsync level shift

7 GMCH_HSYNC
28 NV_HSYNC
7 GMCH_VSYNC
28 NV_VSYNC
R363 R364 UMA 0R2J-2-GP
5V_S0
C108 SCD1U16V2ZY-2GP
U44A U44B TSAHCT125PW-GP
CRT_HSYNC1_R CRT_VSYNC1_R
R324 R322 0R0402-PAD
CRT_HSYNC1 CRT_VSYNC1
C412 C408 SC18P50V2JN-1-GP DY
-1

28 NV_DDCDAT
7 GMCH_DDCDATA
28 NV_DDCCLK
7 GMCH_DDCCLK
R366 R365 0R2J-2-GP UMA
NV_DDCDAT NV_DDCCLK
3D3V_S0
RN44 SRN2K2J-2-GP
Q16 2N7002DW-1-GP
5V_CRT_S0
CH751H-40PT D23
SRN10KJ-6-GP RN43
CRT_DEC#
DAT_DDC1_5
CLK_DDC1_5

DDC_CLK & DATA level shift

TV CONN

28 NV_TV_LUMA
7 TV_DACB
28 NV_TV_CRMA
7 TV_DACC
28 NV_TV_COMP
7 TV_DACA
R115 R116 R114 UMA 0R2J-2-GP
R430 R413 R423 150R2F-1-GP
C565 C545 C554 SC33P50V2JN-3GP
L17 L15 L16 IND-1D2UH-5-GP
C570 C544 C558 SC150P50V2JN-3GP
C566 C546 C555 SC270P50V2JN-2GP
LUMA_1 CRMA_1 COMP_1
MINDIN7-22-GP TVOUT1
22.10021.I81

D11 D8 D9 BAV99-5-GP
D5 D3 D2 BAV99-5-GP
5V_S0
LUMA_1 CRMA_1 COMP_1
CRT_R CRT_G CRT_B

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Title: *CRT/TV Connector*
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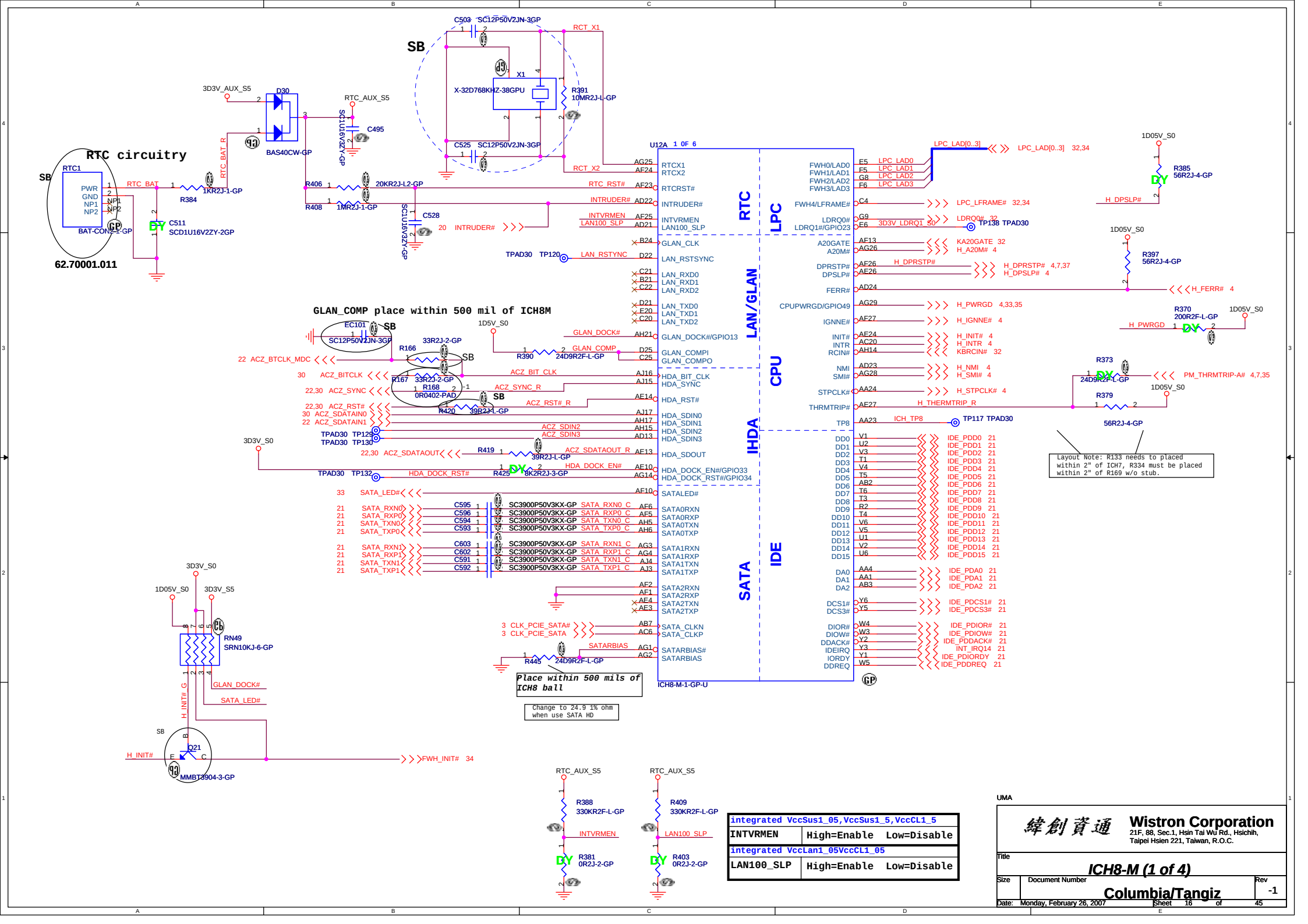
RTC circuitry
62.70001.011
GLAN_COMP place within 500 mil of ICH8M
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
ICH8-M-1-GP-U
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
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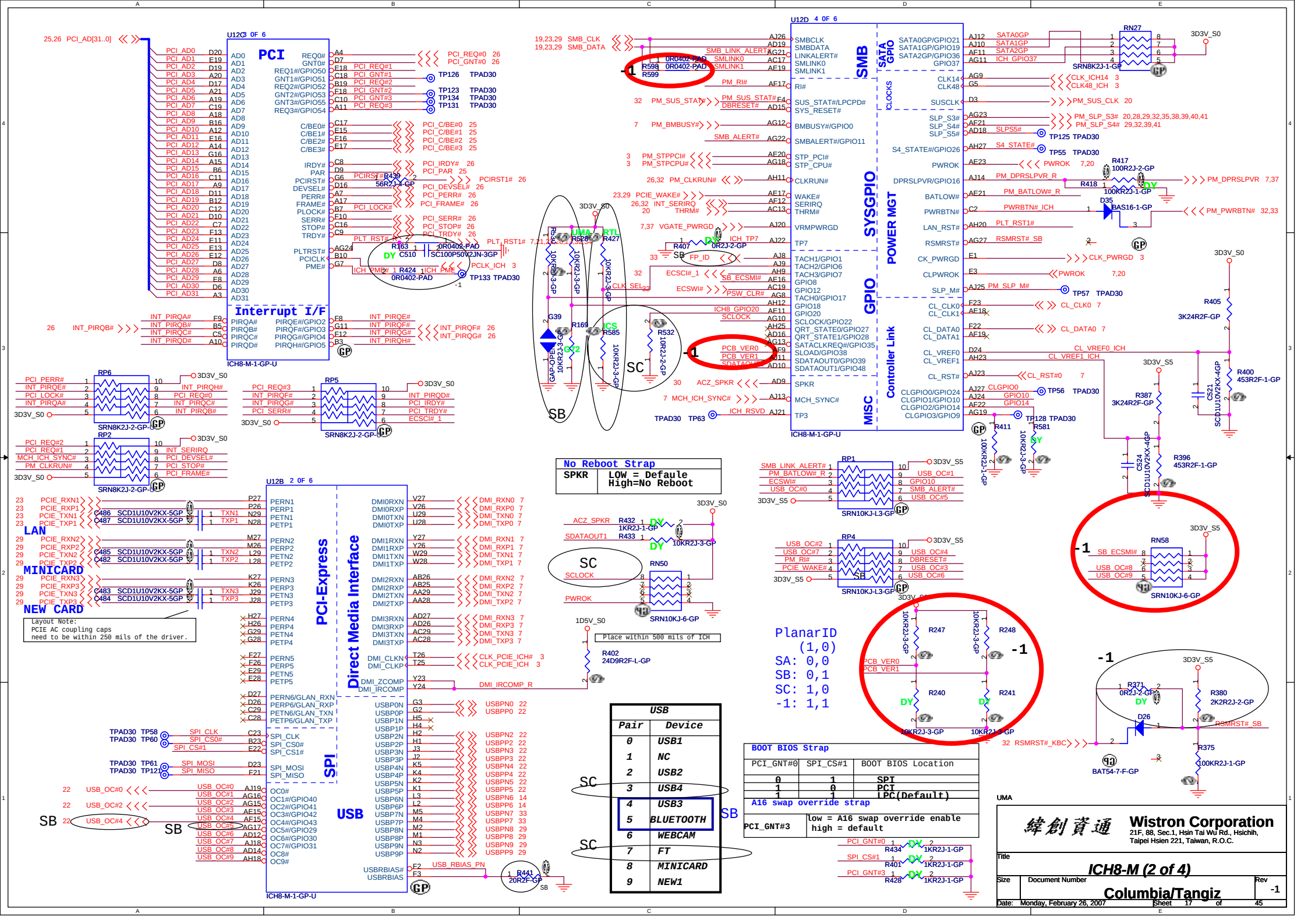
ICH8-M (1 of 4)
Columbia/Tangiz
Monday, February 26, 2007


PCI
Interrupt I/F
ICH8-M-1-GP-U
SMB
GPIO
SYSGPIO
POWER MGT
Controller Link
MISC
ICH8-M-1-GP-U
No Reboot Strap
SPKR LOW = Defaule High=No Reboot
LAN
MINICARD
NEW CARD
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M-1-GP-U
Place within 500 mils of ICH
USB
Pair Device
0 USB1
1 NC
2 USB2
3 USB4
4 USB3
5 BLUETOOTH
6 WEBCAM
7 FT
8 MINICARD
9 NEW1
PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable
high = default
UMA
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Title
ICH8-M (2 of 4)
Size
Document Number
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-1
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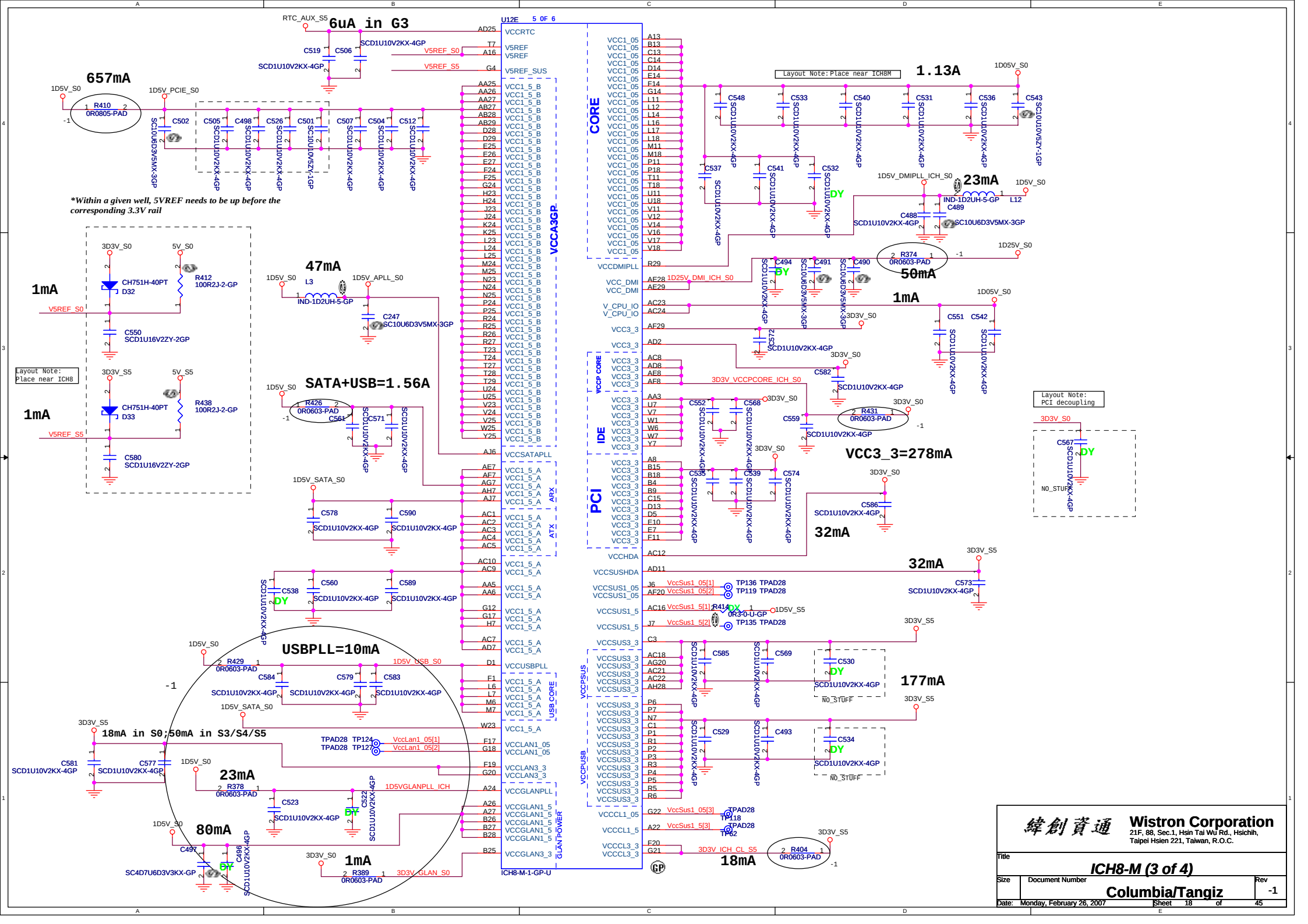
6uA in G3
657mA
1.13A
23mA
50mA
1mA
47mA
SATA+USB=1.56A
VCC3_3=278mA
32mA
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
80mA
177mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH8M
Layout Note: Place near ICH8
Layout Note: PCI decoupling
U12E 5 OF 6
ICH8-M-1-GP-U
CORE
VCCA3GP
IDE
PCI
ARX
ATX
USB CORE
GLAN POWER
VCCP CORE
VCCPSUS
VCCPUSB
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ICH8-M (3 of 4)
Columbia/Tangiz
Monday, February 26, 2007
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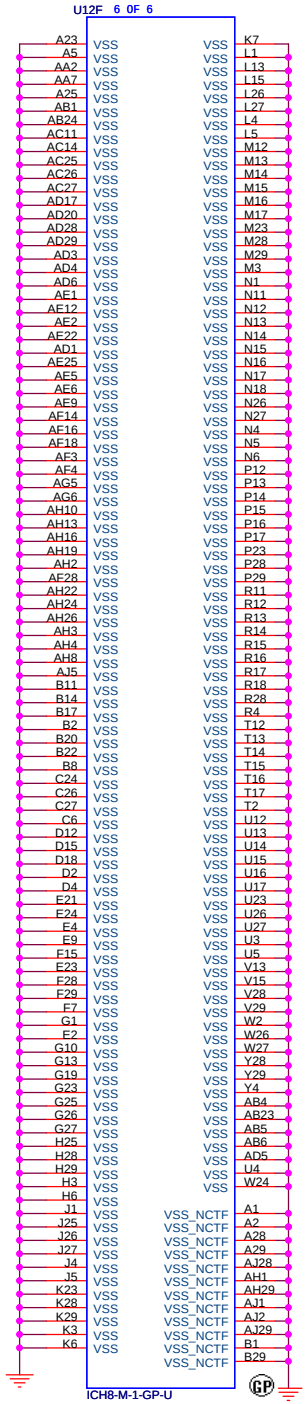

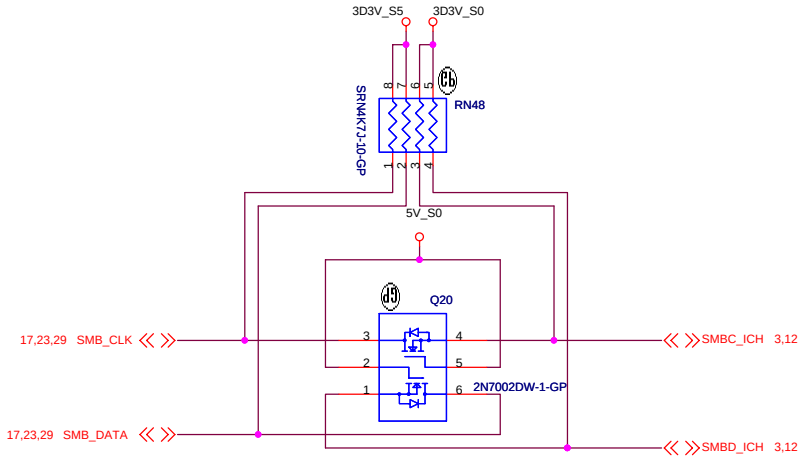

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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Title	*ICH8-M (4 of 4)*	
Size	Document Number: **Columbia/Tangiz**	Rev: -1
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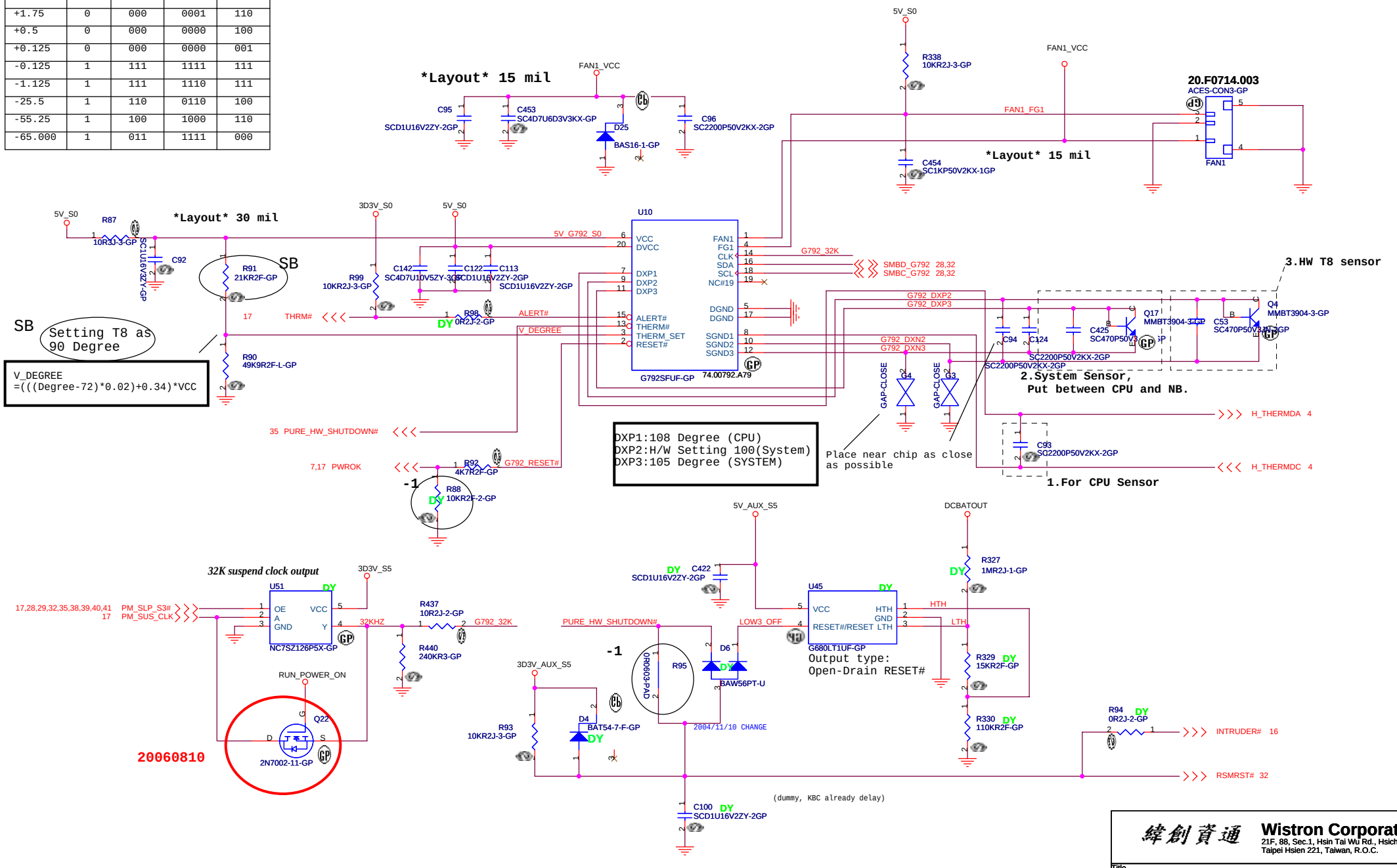
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



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Title: Thermal/Fan Controllor

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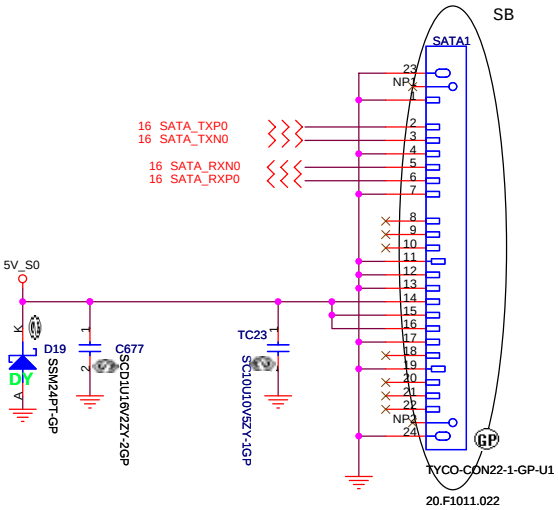
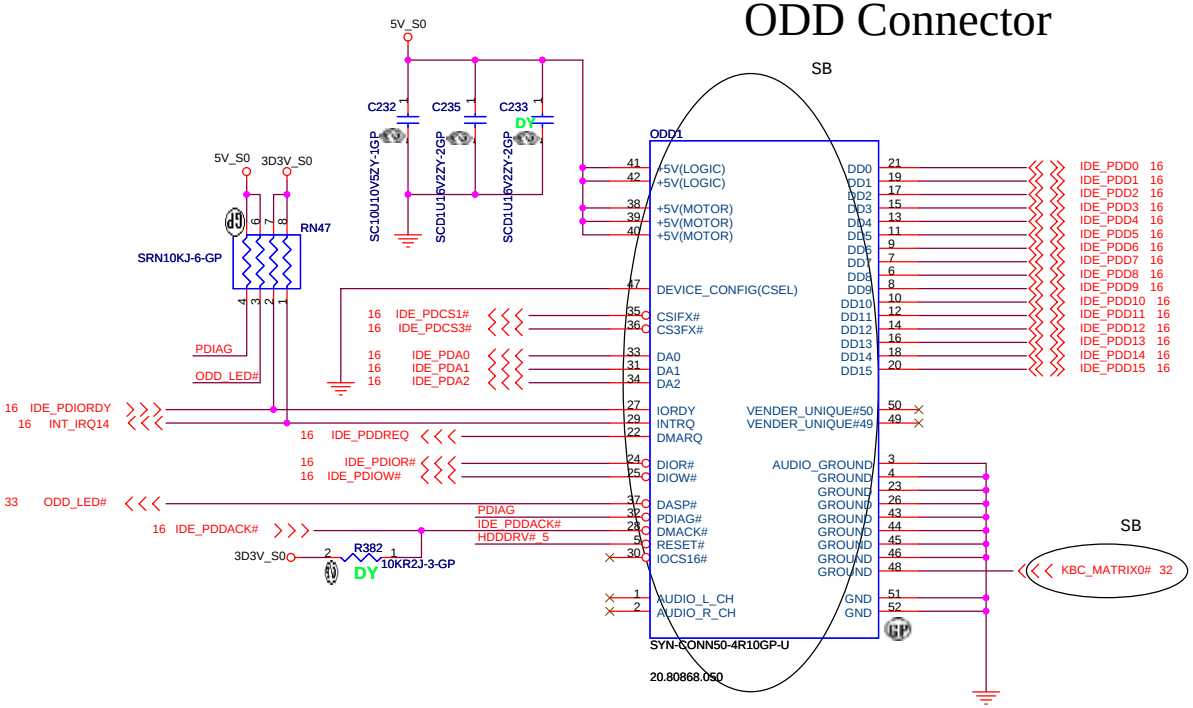
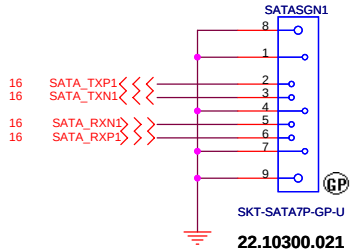
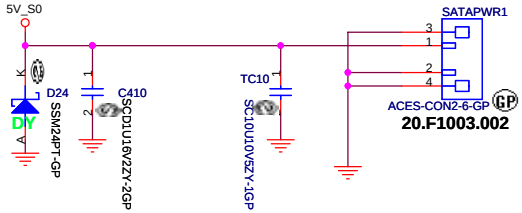
SATA HD Connector

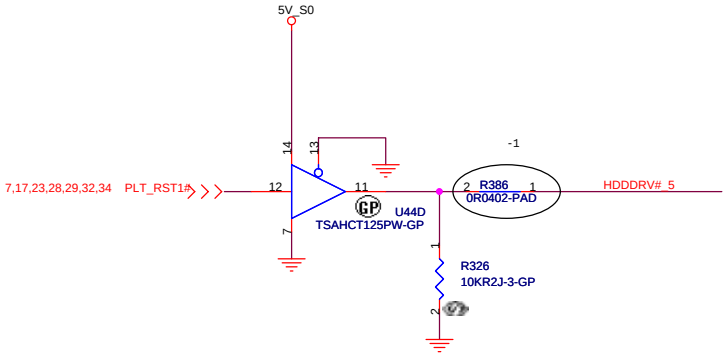


ODD Connector









bom1

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Title: HDD and CDROM

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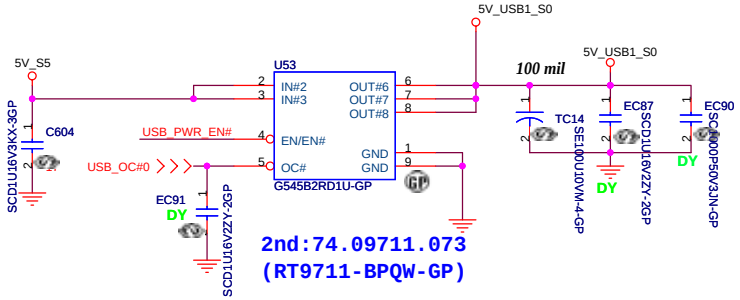
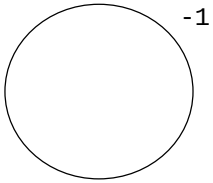
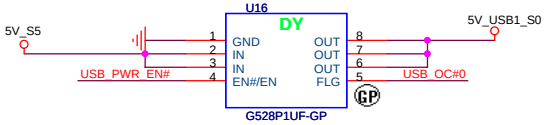
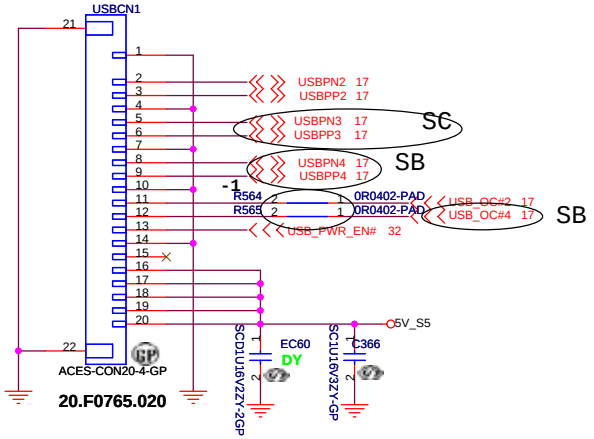
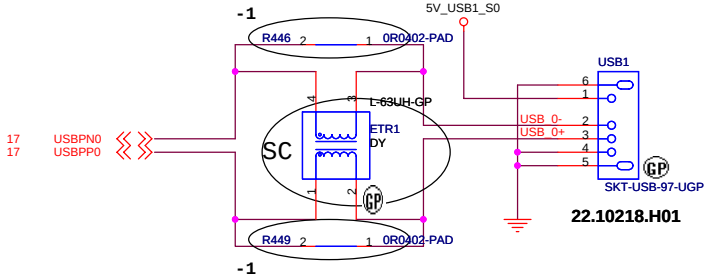




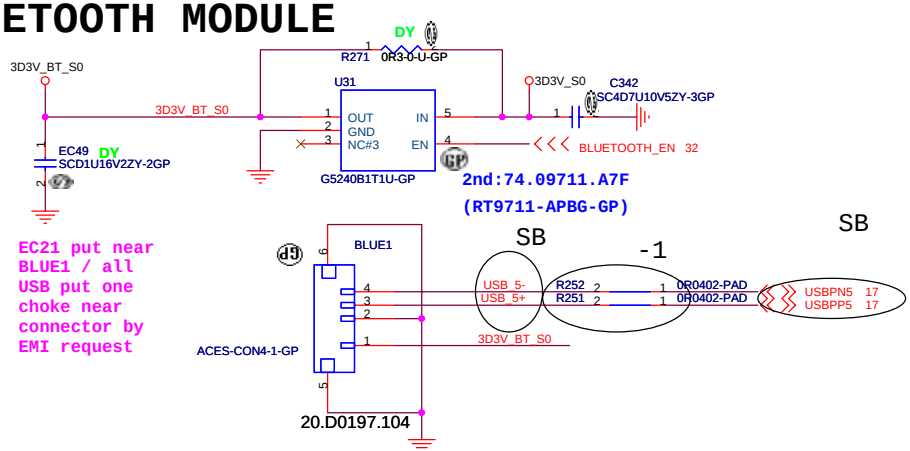


2nd:74.09711.07D
(RT9711-BPS-GP)

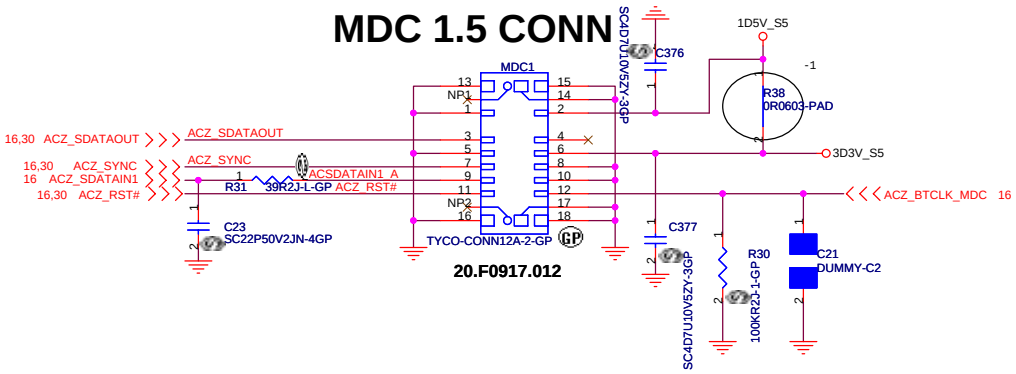


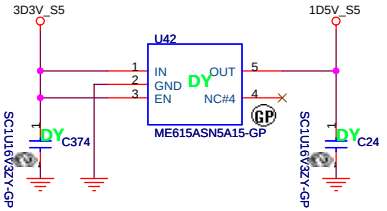


BLUETOOTH MODULE



MDC 1.5 CONN





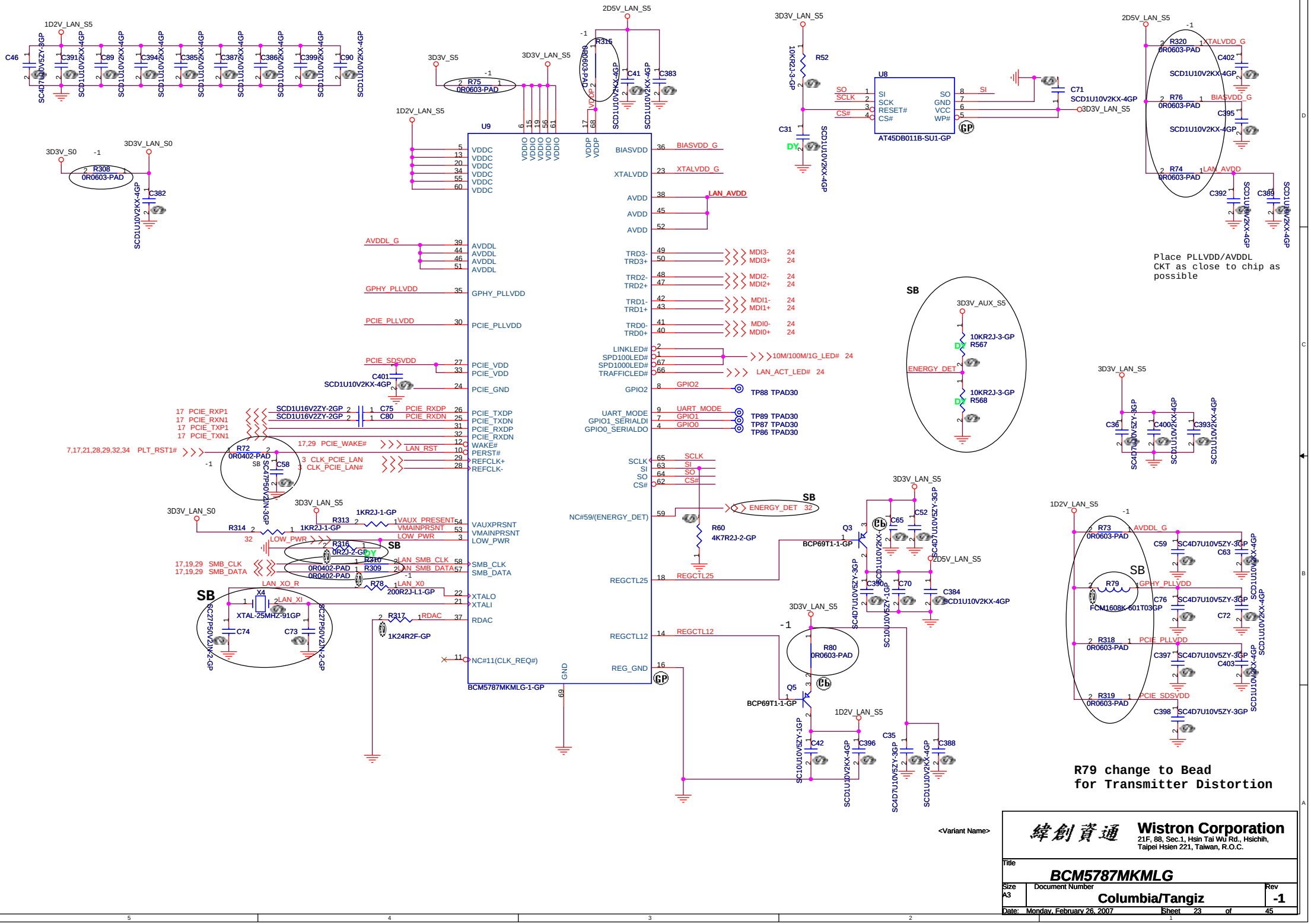
bom1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / MDC / BLUETOOTH

Size	Document Number	Rev
	Columbia/Tangiz	-1

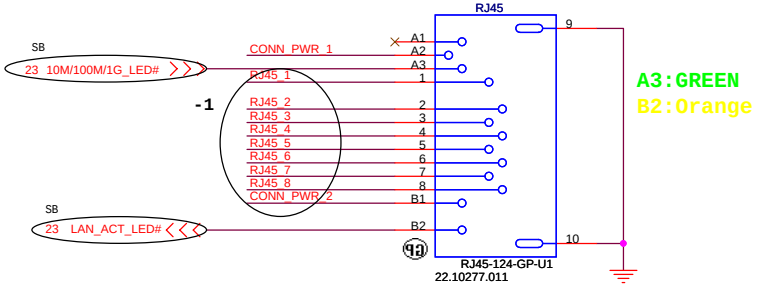
Date: Monday, February 26, 2007 Sheet 22 of 45


U9
BCM5787MKMLG-1-GP
U8
AT45DB011B-SU1-GP
Q3
BCP69T1-1-GP
Q5
BCP69T1-1-GP
X4
XTAL-25MHZ-91GP
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R79 change to Bead
for Transmitter Distortion
SB
GP
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size A3
Document Number
Columbia/Tangiz
Rev -1
Date: Monday, February 26, 2007
Sheet 23 of 45

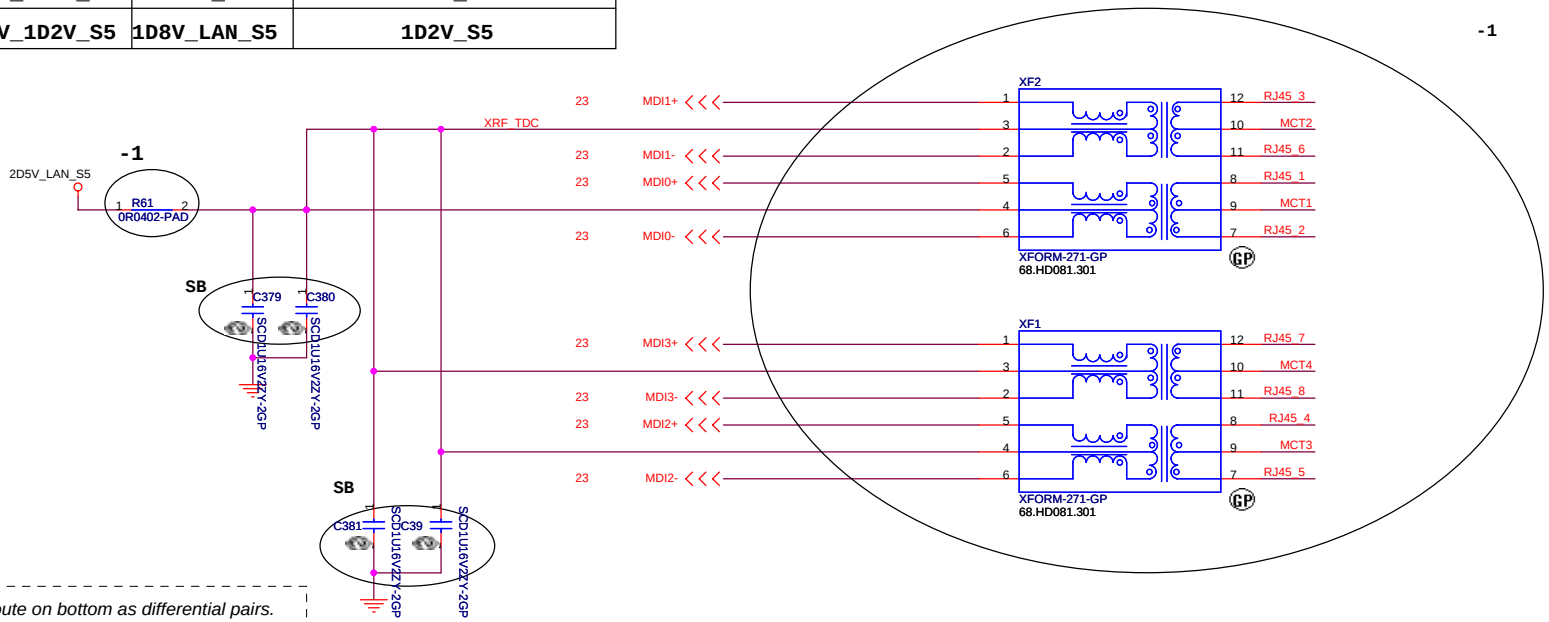
LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

GIGA Lan Transformer



-1



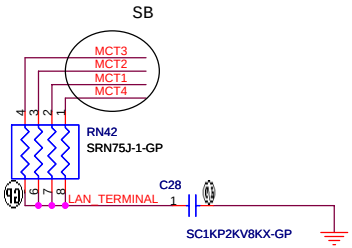
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

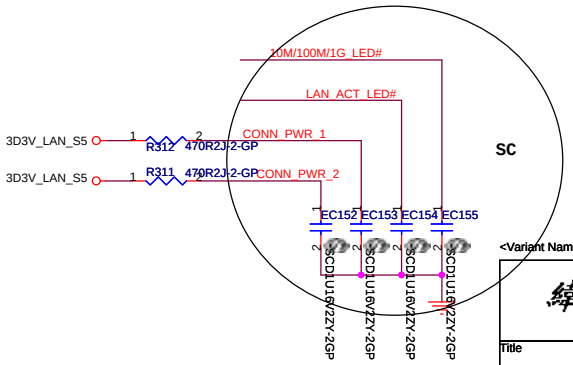
LAN Data: Yellow(B2), when LAN is transfering data.

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers





10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: Columbia/Tangiz | Rev: -1
Date: Monday, February 26, 2007 | Sheet 24 of 45

C782 should close Pin-P15
and Pin-R17.

TI PCI7412

U54A

71.07412.B0U

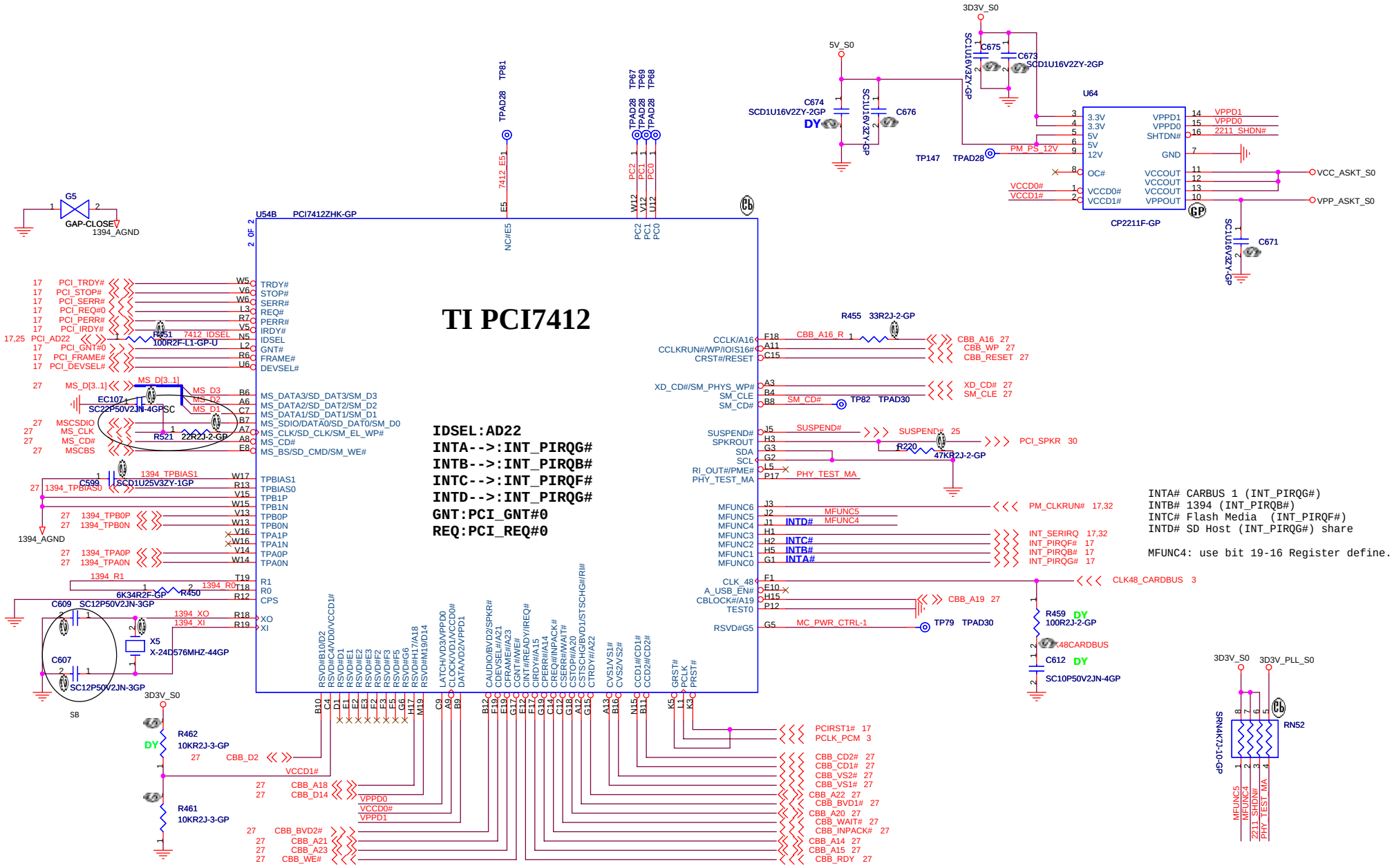
PCI7412ZHK-GP

* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible

Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible

<Variant Name>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TI PCI7412 (1 of 2)		
Size	Document Number: Columbia/Tangiz	Rev: -1
Date: Monday, February 26, 2007	Sheet 25 of 45	



<variant_name>

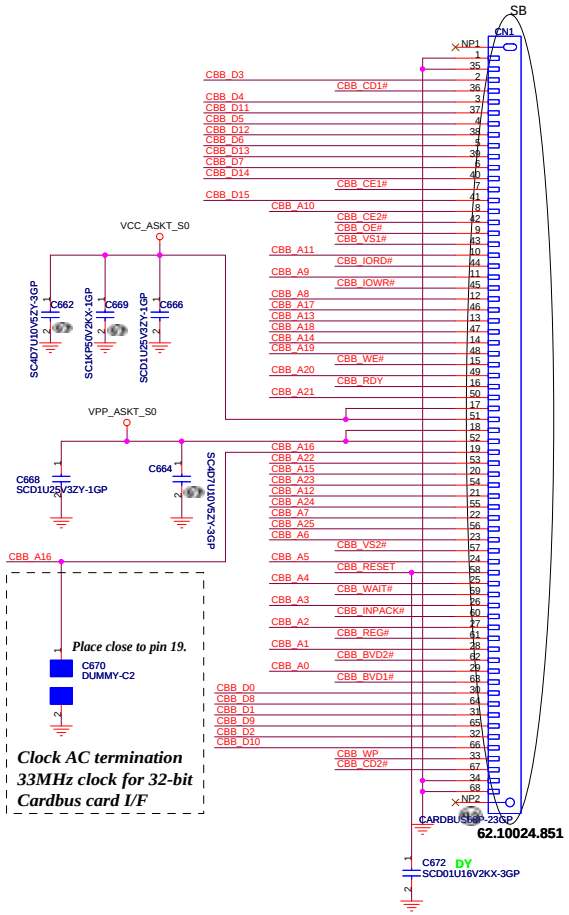
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI PCI7412 (2 of 2)

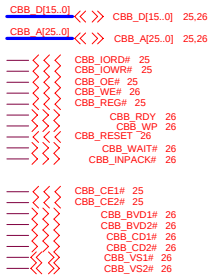
Size	Document Number	Rev
	Columbia/Tangiz	-1

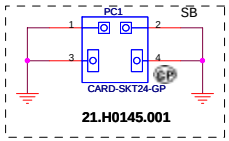
Date: Monday, February 26, 2007 Sheet 26 of 45

PCMCIA Socket

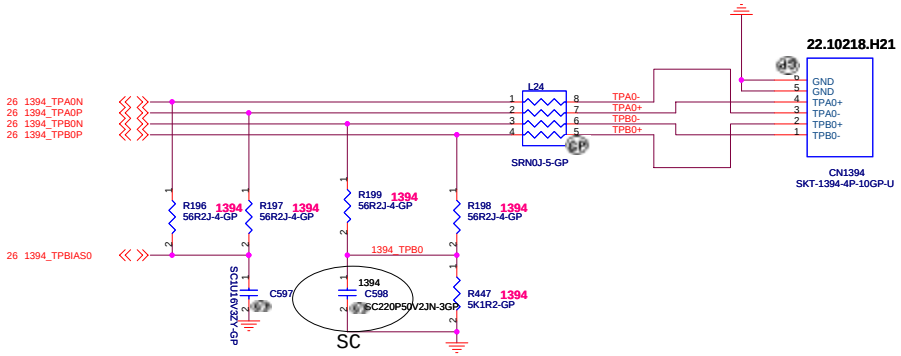


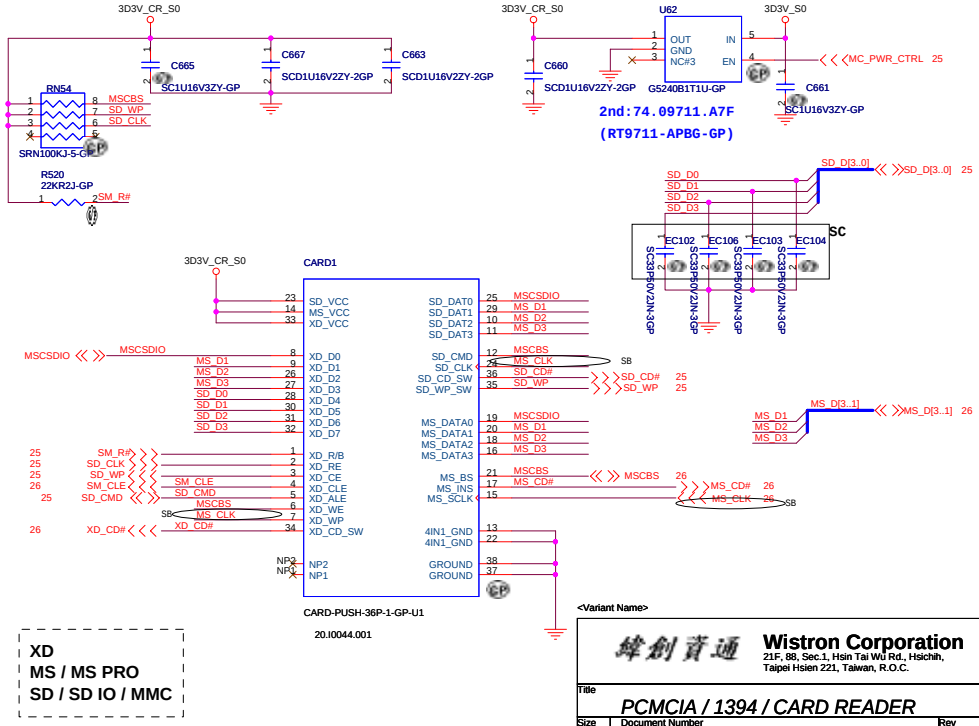
Cardbus I/F





1394 Connector





<variant_name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / 1394 / CARD READER

Size | Document Number: Columbia/Tangiz | Rev: -1

Date: Monday, February 26, 2007 | Sheet 27 of 45

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]

5V_S0
37,38,39,40,41 CPUCORE_ON
17,20,29,32,35,38,39,40,41 PM_SLP_S3#
G72
R347 0R2J-2-GP
R337 0R2J-2-GP
C457 SCD1U25V3KX-GP
TPAD30TP95
DY
-1
1D8V_S0
SC
C691 SCD1U25V3KX-GP
C692 SCD1U25V3KX-GP
CN1 20.F0871.230

14 LCD_TXBOUT0+
14 LCD_TXBOUT0-
14 LCD_TXBOUT1+
14 LCD_TXBOUT1-
14 LCD_TXBOUT2+
14 LCD_TXBOUT2-
14 LCD_TXBCLK+
14 LCD_TXBCLK-
15 NV_BLUE
15 NV_GREEN
15 NV_RED
15 NV_TV_COMP
15 NV_TV_LUMA
15 NV_TV_CRMA

LCD_TXACLK- 14
LCD_TXACLK+ 14
LCD_TXAOUT2- 14
LCD_TXAOUT2+ 14
LCD_TXAOUT1- 14
LCD_TXAOUT1+ 14
LCD_TXAOUT0- 14
LCD_TXAOUT0+ 14
NV_EDID_DAT 14
NV_EDID_CLK 14
NV_LCDVDD_ON 14
NV_BLON 32
NV_DVI_DAT 44
NV_DVI_CLK 44

2D5V_S0
3D3V_S0
R579 0R3-0-U-GP
NV
C456 SC10U10V5ZY-1GP
C458 SCD1U25V3KX-GP
MXM1
TYCO-CONN230A-GP-U3

PEG_TXN15 PEG_TXP15 PEG_TXN14 PEG_TXP14 PEG_TXN13 PEG_TXP13 PEG_TXN12 PEG_TXP12 PEG_TXN11 PEG_TXP11 PEG_TXN10 PEG_TXP10 PEG_TXN9 PEG_TXP9 PEG_TXN8 PEG_TXP8 PEG_TXN7 PEG_TXP7 PEG_TXN6 PEG_TXP6 PEG_TXN5 PEG_TXP5 PEG_TXN4 PEG_TXP4 PEG_TXN3 PEG_TXP3 PEG_TXN2 PEG_TXP2 PEG_TXN1 PEG_TXP1 PEG_TXN0 PEG_TXP0
TP92 TP91 TP96 TP93 TP94 TP97 TPAD30

DCBATOUT
C476 SCD1U25V3KX-GP
C477 SCD1U25V3KX-GP
C480 SC4D7U25V6KX-1GP
C479 SC4D7U25V6KX-1GP
C481 SC4D7U25V6KX-1GP

PEG_RXN15 PEG_RXP15 PEG_RXN14 PEG_RXP14 PEG_RXN13 PEG_RXP13 PEG_RXN12 PEG_RXP12 PEG_RXN11 PEG_RXP11 PEG_RXN10 PEG_RXP10 PEG_RXN9 PEG_RXP9 PEG_RXN8 PEG_RXP8 PEG_RXN7 PEG_RXP7 PEG_RXN6 PEG_RXP6 PEG_RXN5 PEG_RXP5 PEG_RXN4 PEG_RXP4 PEG_RXN3 PEG_RXP3 PEG_RXN2 PEG_RXP2 PEG_RXN1 PEG_RXP1 PEG_RXN0 PEG_RXP0
TP43 TP106 TPAD30

3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG

7,17,21,23,29,32,34 PLT_RST1#
R367 0R0402-PAD
C478
SC100P50V2JN-3GP
PLT_RST1#_MXM

20,32 SMBD_G792
20,32 SMBC_G792
R586 0R0402-PAD
R587 0R0402-PAD
SMBD_MXM
SMBC_MXM

35 MXM_THER

15 NV_HSYNC
15 NV_VSYNC
15 NV_DDCCLK
15 NV_DDCDAT

TPAD30 TP44 SPDIF_HDMI
TPAD30 TP112 GPU_BUFRST#
TPAD30 TP107 MP_INT
TPAD30 TP99 GPU_PRGM#
TPAD30 TP98 IGP_UTX2#
TPAD30 TP103 IGP_UTX2
TPAD30 TP108 TMDS_GPIO6_SW
TPAD30 TP148

EMI REQUEST

TMDS_A_TX0+ 1 → SRN33J-5-GP-U ERN4 → TMDS_A_TX0+ 44
TMDS_A_TX0- 1 → SRN33J-5-GP-U ERN3 → TMDS_A_TX0- 44
TMDS_A_TX1+ 1 → SRN33J-5-GP-U ERN2 → TMDS_A_TX1+ 44
TMDS_A_TX1- 1 → SRN33J-5-GP-U ERN2 → TMDS_A_TX1- 44
TMDS_A_TX2+ 1 → SRN33J-5-GP-U ERN1 → TMDS_A_TX2+ 44
TMDS_A_TX2- 1 → SRN33J-5-GP-U ERN1 → TMDS_A_TX2- 44
TMDS_A_TXC+ 1 → SRN33J-5-GP-U → TMDS_A_TXC+ 44
TMDS_A_TXC- 1 → SRN33J-5-GP-U → TMDS_A_TXC- 44

ERN77~ERN80要靠近MXM1

DVI_A_HPD 44

TMDS_B_TX0+ TP115 TPAD30
TMDS_B_TX0- TP114 TPAD30
TMDS_B_TX1+ TP105 TPAD30
TMDS_B_TX1- TP104 TPAD30
TMDS_B_TX2+ TP111 TPAD30
TMDS_B_TX2- TP110 TPAD30
G72_27MHZ TP102 TPAD30
G72_27MHZSS TP113 TPAD30
DVI_B_HPD TP109 TPAD30
TMDS_B_TXC+ TP101 TPAD30
TMDS_B_TXC- TP100 TPAD30

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Graphic MXM CONN
Size: A3
Document Number: Columbia/Tangiz
Rev: -1
Date: Monday, February 26, 2007
Sheet 28 of 45

Mini Card Connector

NEWCARD Connector

SB

SK1
CARDBUS-SKT91-GP

Reserve the symbol for bottom side connector

CARDBUS26P-8GP
NEW1
62.10024.881

17 PCIE_TXP3
17 PCIE_TXN3
17 PCIE_RXP3
17 PCIE_RXN3
3 CLK_PCIE_NEW
3 CLK_PCIE_NEW#
CPPE#
TP146 NEWCARD_TEST
3D3V_NEW_S0
EC97 SCD1U10V2KX-4GP
3D3V_NEW_LAN_S5
EC96 SCD1U10V2KX-4GP
17,23 PCIE_WAKE#
1D5V_NEW_S0
R497 0R2J-2-GP
PCIE_WAKE# R
SRN33J-5-GP-U
TPS2231_PERST#
17,19,23 SMB_DATA
17,19,23 SMB_CLK
SMB_DATA_NEW
SMB_CLK_NEW
CONN_TP1
CONN_TP2
TP144 TP145 RN53
CPUTSB#
17 USBPP9
17 USBPN9

W83L351YG-GP U61
1D5V_NEW_S0
1D5V_S0
3D3V_NEW_LAN_S5
3D3V_S5
R518 100KR2J-1-GP
R477 100KR2J-1-GP
CPPE#
CPUSB#
TPS2231_PERST#
NEW_PLT_RST1#
PM_SLP_S4# 17,32,39,41
SB
7,17,21,23,28,32,34 PLT_RST1#
R516 0R0402-PAD
C658 SC100P50V2JN-3GP
2nd:74.00577.073
(G577R9U-GP)
PM_SLP_S3# 17,20,28,32,35,38,39,40,41
3D3V_S0
3D3V_NEW_S0

Place them Near to Chip
Place them Near to Connector

C656 SCD1U16V2ZY-2GP
C657 C655 C647 C646 C654 SCD1U16V2ZY-2GP
SC1U16V3ZY-4GP

Mini Card Connector

SB

MINIC1
SKT-MINI52P-13-GP
62.10043.461

3D3V_S0
3D3V_S5
SC
DY R582 0R3-0-U-GP
R583 0R3-0-U-GP
3D3V_S0_MINI
MINI_WAKE#
TP3 TPAD30
1D5V_S0
R39 10KR2J-3-GP
32 WIRELESS_EN
7,17,21,23,28,32,34 PLT_RST1#
CLK_PCIE_MINI1# 3
CLK_PCIE_MINI1 3
E51_RxD 32
E51_TxD 32
PCIE_RXN2 17
PCIE_RXP2 17
PCIE_TXN2 17
PCIE_TXP2 17
17,19,23 SMB_CLK
17,19,23 SMB_DATA
0R2J-2-GP
R13
R12
SMB_CLK_MINI
SMB_DATA_MINI
17 USBPN8
17 USBPP8
TP1
LED_WPAN#
TPAD28
WLAN_LED#
14 WLAN_LED#
TP2 TPAD28
5V_AUX_S5_MINI
R563 0R0603-PAD
5V_S5
-1

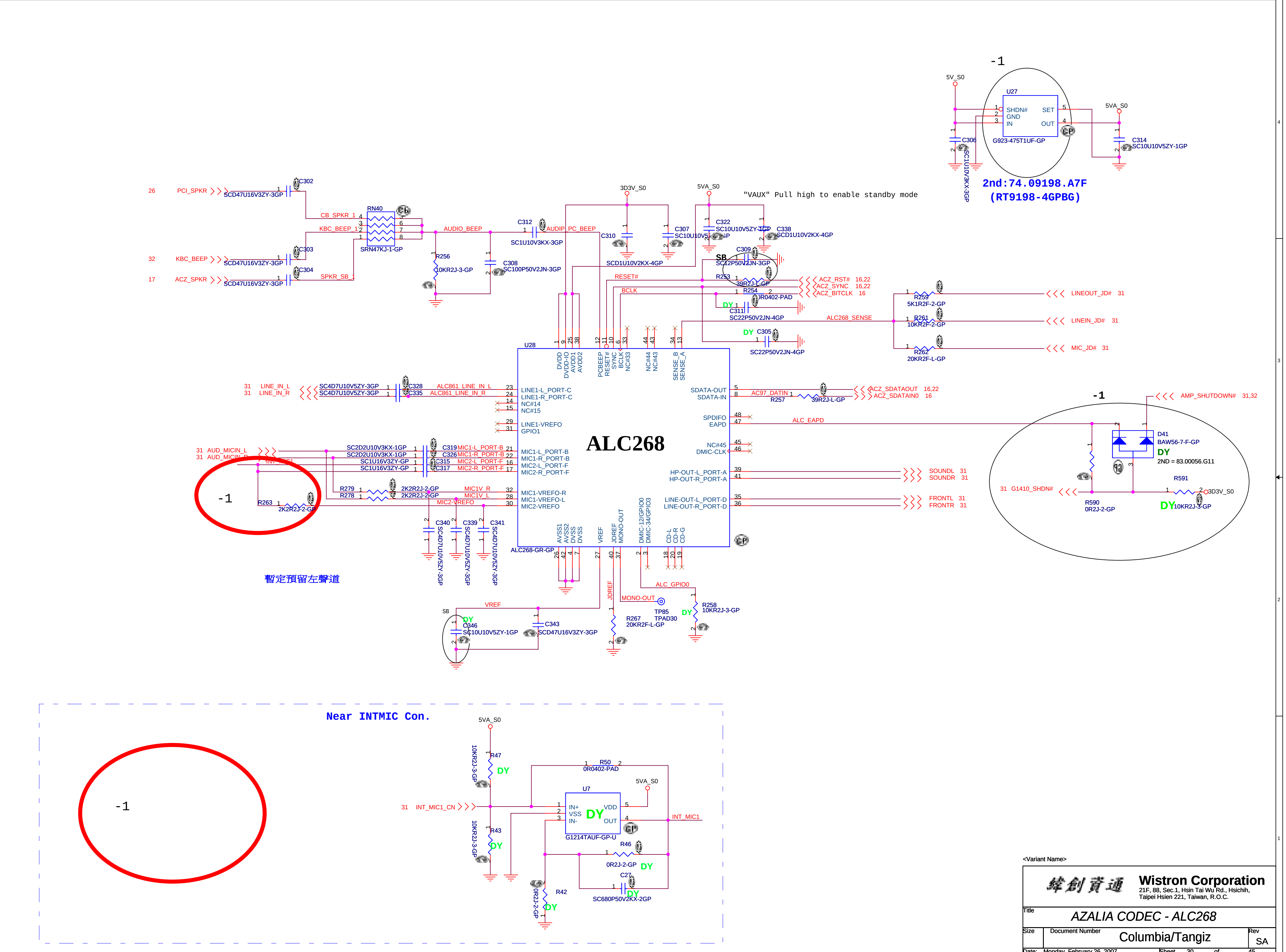
Place near MINIC1

ST220U6D3VDM-13GP
0R5J-5-GP R55
0R5J-5-GP R584
TC9 C33 C351 C378
C375 C20 C358
C22 C373
SC1U6D3V5MX-3GP
SC1U16V3ZY-4GP
SCD1U16V2ZY-2GP

bom1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / NEW CARD
Size
Document Number: Columbia/Tangiz
Rev: -1
Date: Monday, February 26, 2007
Sheet 29 of 45



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AZALIA CODEC - ALC268	
Size	Document Number: Columbia/Tangiz	Rev: SA
Date: Monday, February 26, 2007	Sheet 30 of 45	

AUDIO OP AMPLIFIER

R,L 1.5W Speaker
mount R274,R281
R269->63.36334.1DL
R268->63.33334.1DL

R,L 1W Speaker
mount R280,R281
R269->63.15334.1DL
R268->63.12334.1DL

R,L 1.2W Speaker
mount R280,R281
R269->63.10334.1DL
R268->63.68234.1DL

KBC_MUTE_GPIO8

SB:U30 trace modify

LINE IN

Internal Microphone

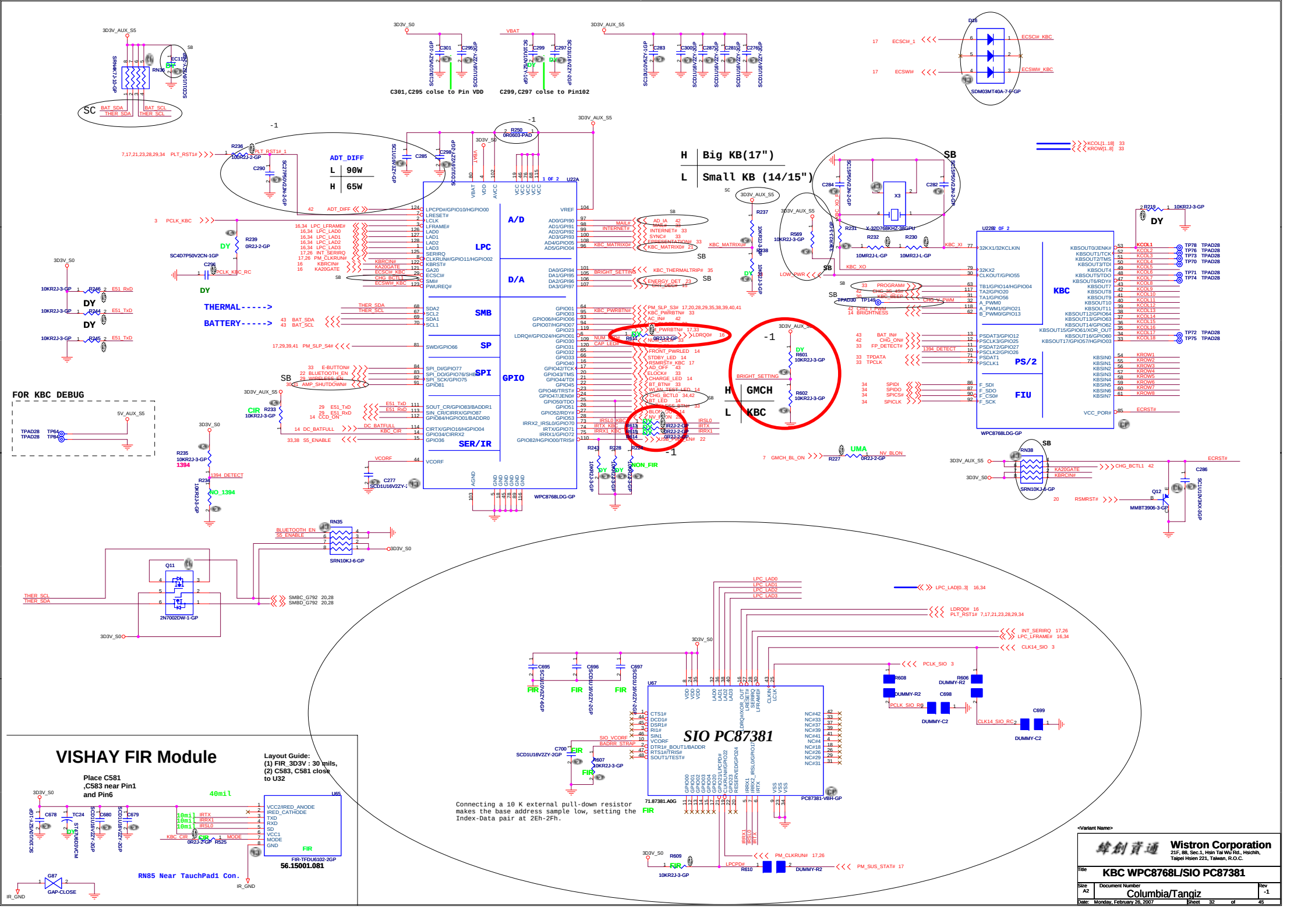
Internal Speaker

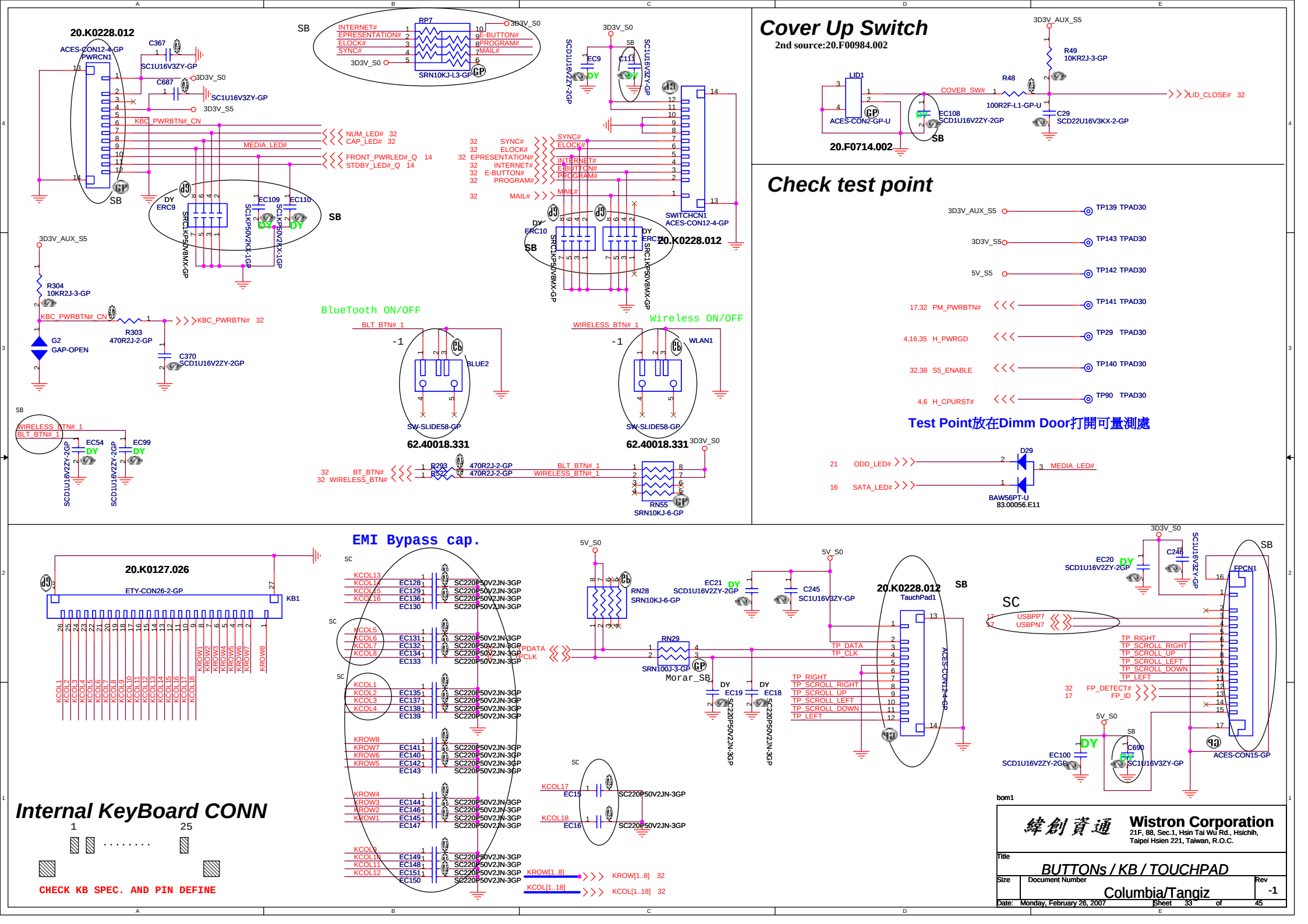
MIC IN

LINE OUT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP AND JACK
Size: Document Number: Columbia/Tangiz Rev: -1
Date: Monday, February 26, 2007 Sheet 31 of 45


C301,C295 colse to Pin VDD
C299,C297 colse to Pin102
ADT_DIFF
L 90W
H 65W
H Big KB(17")
L Small KB (14/15")
H GMCH
L KBC
THERMAL----->
BATTERY----->
FOR KBC DEBUG
SIO PC87381
VISHAY FIR Module
Place C581 ,C583 near Pin1 and Pin6
Layout Guide: (1) FIR_3D3V : 30 mils, (2) C583, C581 close to U32
RN85 Near TauchPad1 Con.
Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L/SIO PC87381
Columbia/Tangiz
Monday, February 26, 2007



Cover Up Switch

2nd source:20.F00984.002

Check test point

Test Point放在Dimm Door打開可量測處

Internal KeyBoard CONN

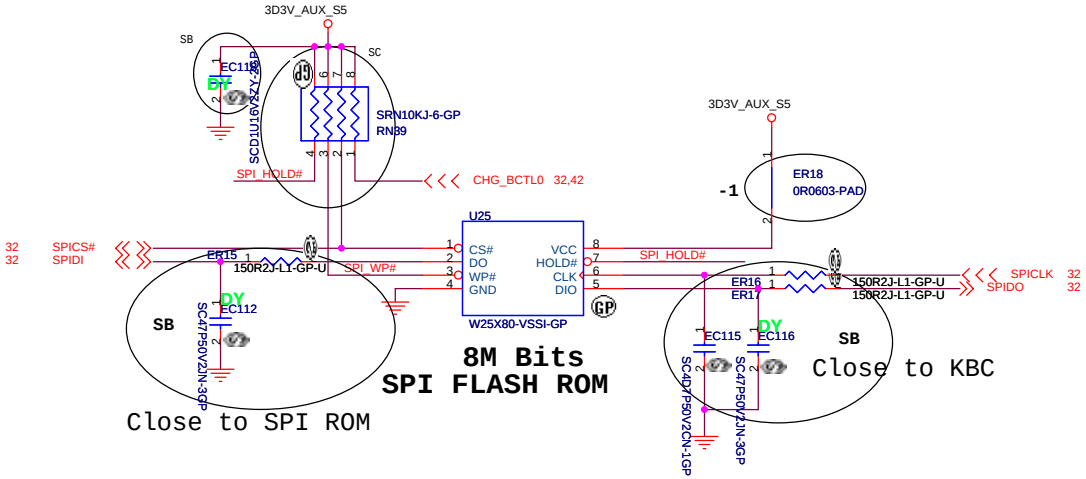
1 25

CHECK KB SPEC. AND PIN DEFINE

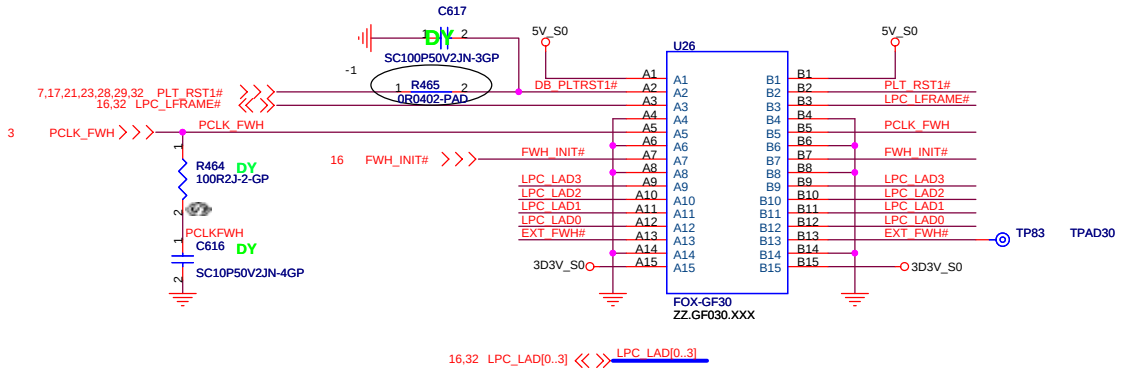
EMI Bypass cap.

bom1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*BUTTONs / KB / TOUCHPAD*
Size / Document Number	Columbia/Tangiz
Rev	-1
Date: Monday, February 26, 2007	Sheet 33 of 45



GOLDEN FINGER FOR DEBUG BOARD

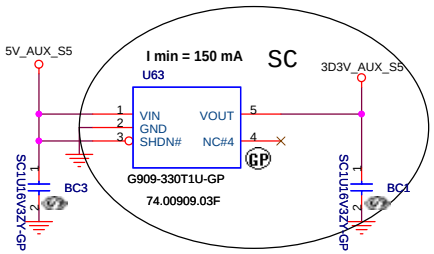


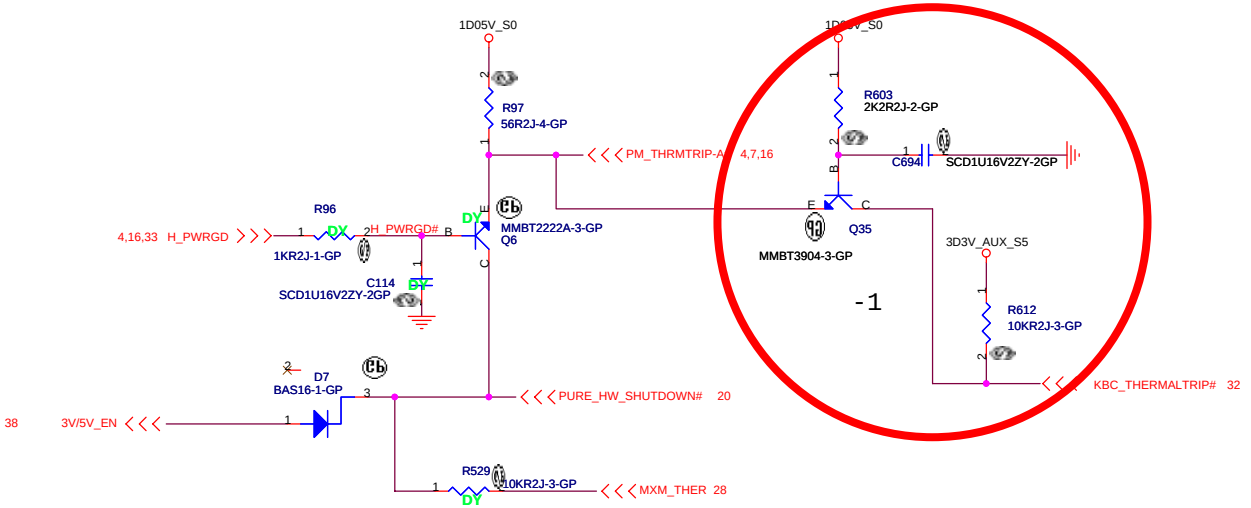
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

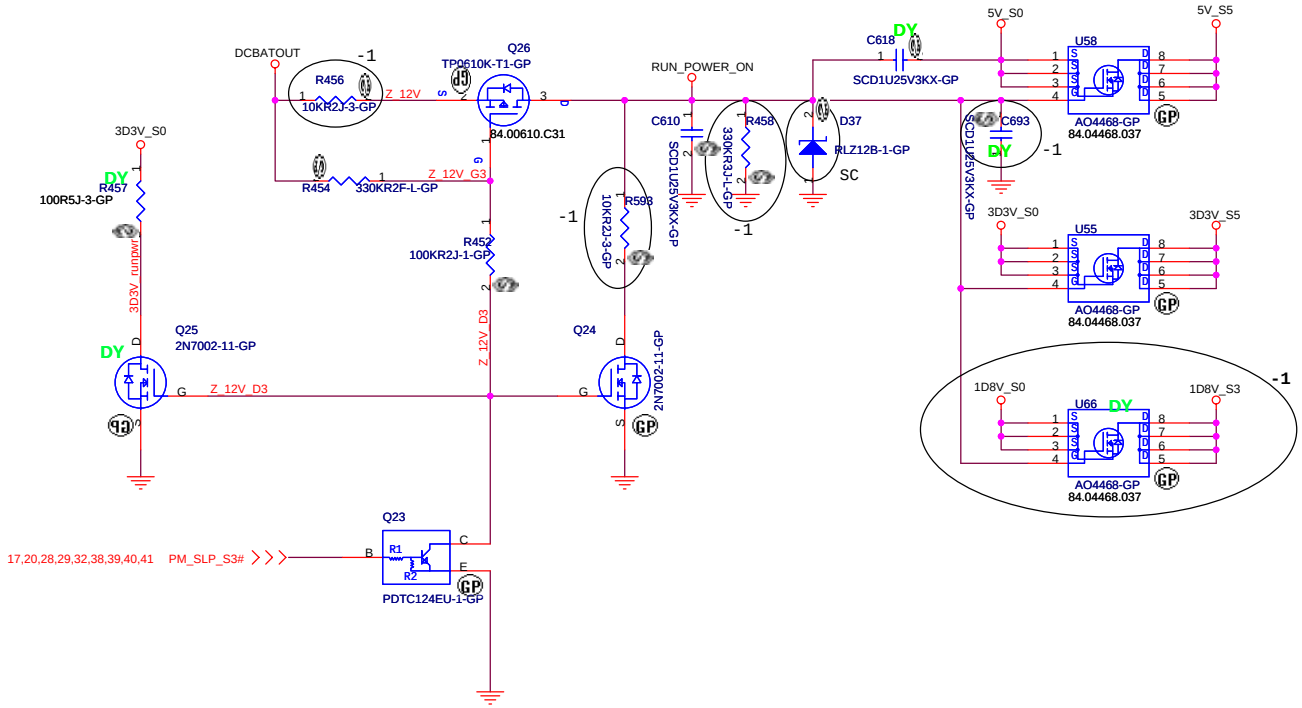
Title: BIOS		
Size: A3	Document Number: Columbia/Tangiz	Rev: -1
Date: Monday, February 26, 2007	Sheet 34 of 45	

Aux Power 3D3V_AUX_S5





Run Power



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RUN POWER and 3D3V_AUX_S5***	
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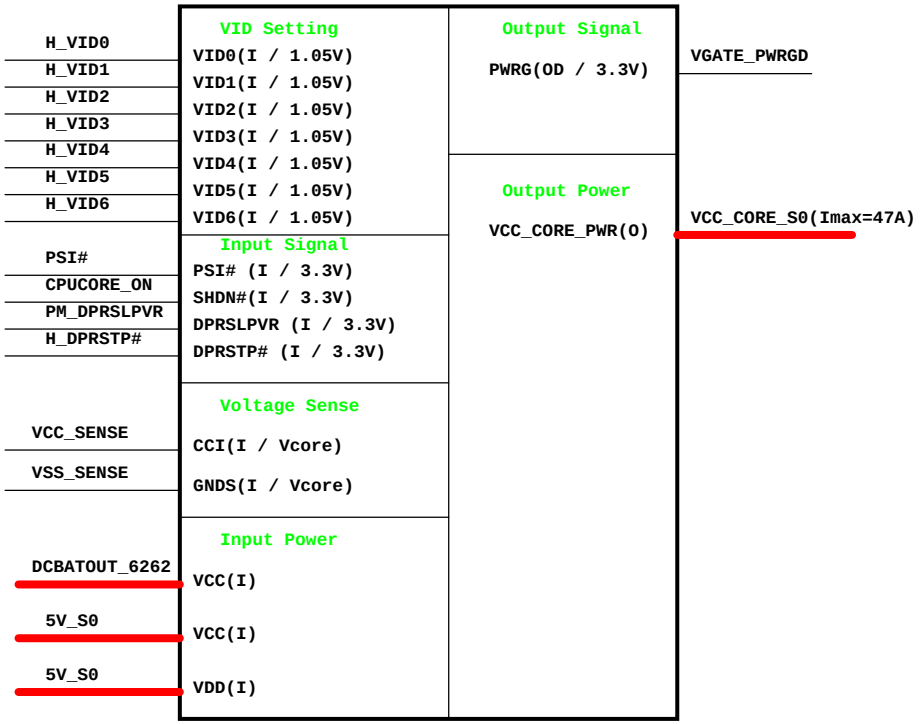
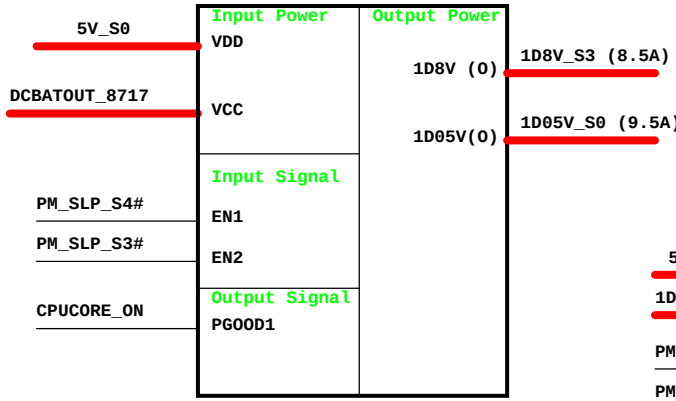
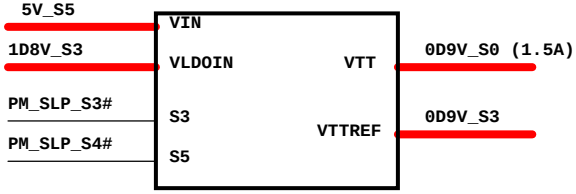
CPU_CORE
MAX8770



MAX8717
1D8V/1D05V

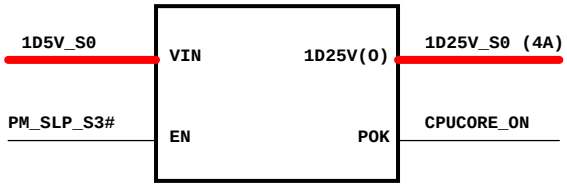


0D9V_S0



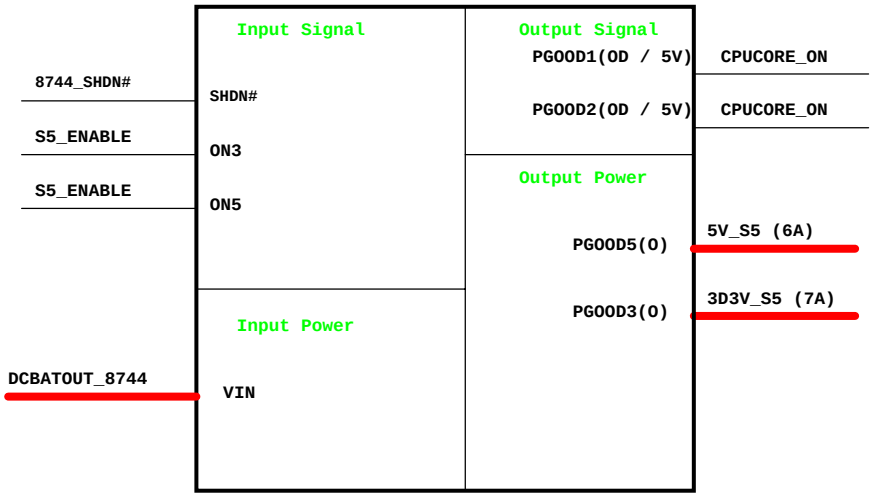
TPS51100

1D25V_S0

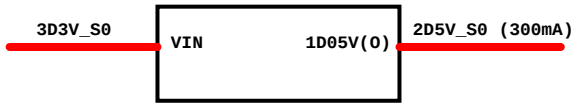


APL5915

MAX8744
5V/3D3V

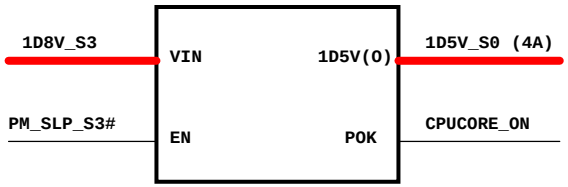


2D5V_S0



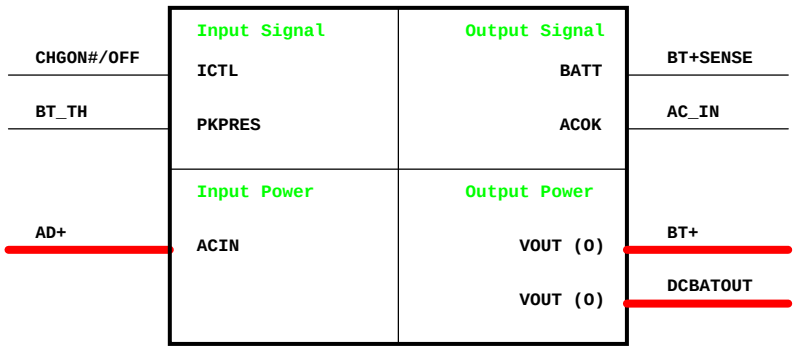
APL5308

1D5V_S0



APL5912

Charger ISL6255



<Variant Name>

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Title: Power Block Diagram

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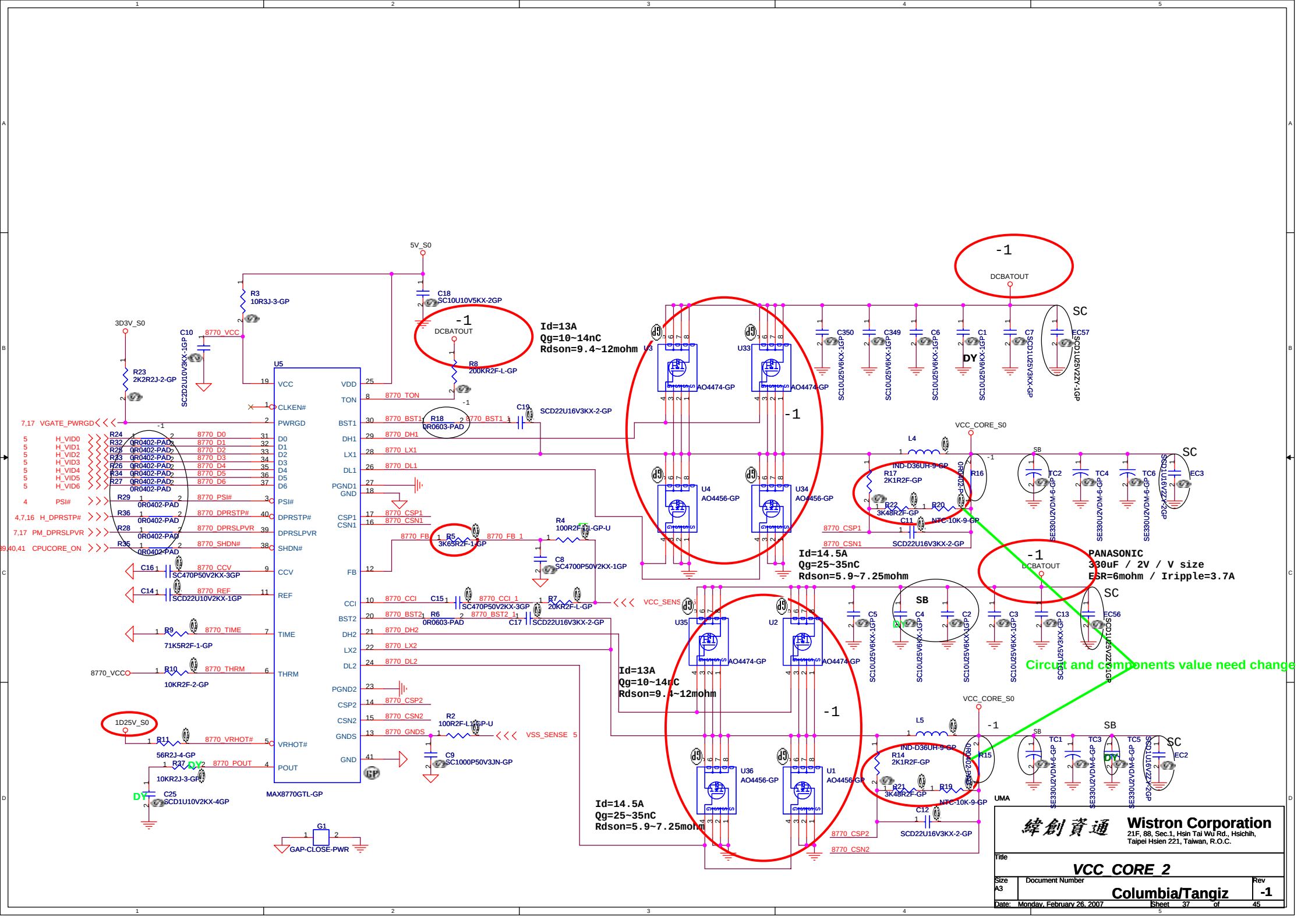
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
MAX8770GTL-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VCC_CORE_2
Columbia/Tangiz
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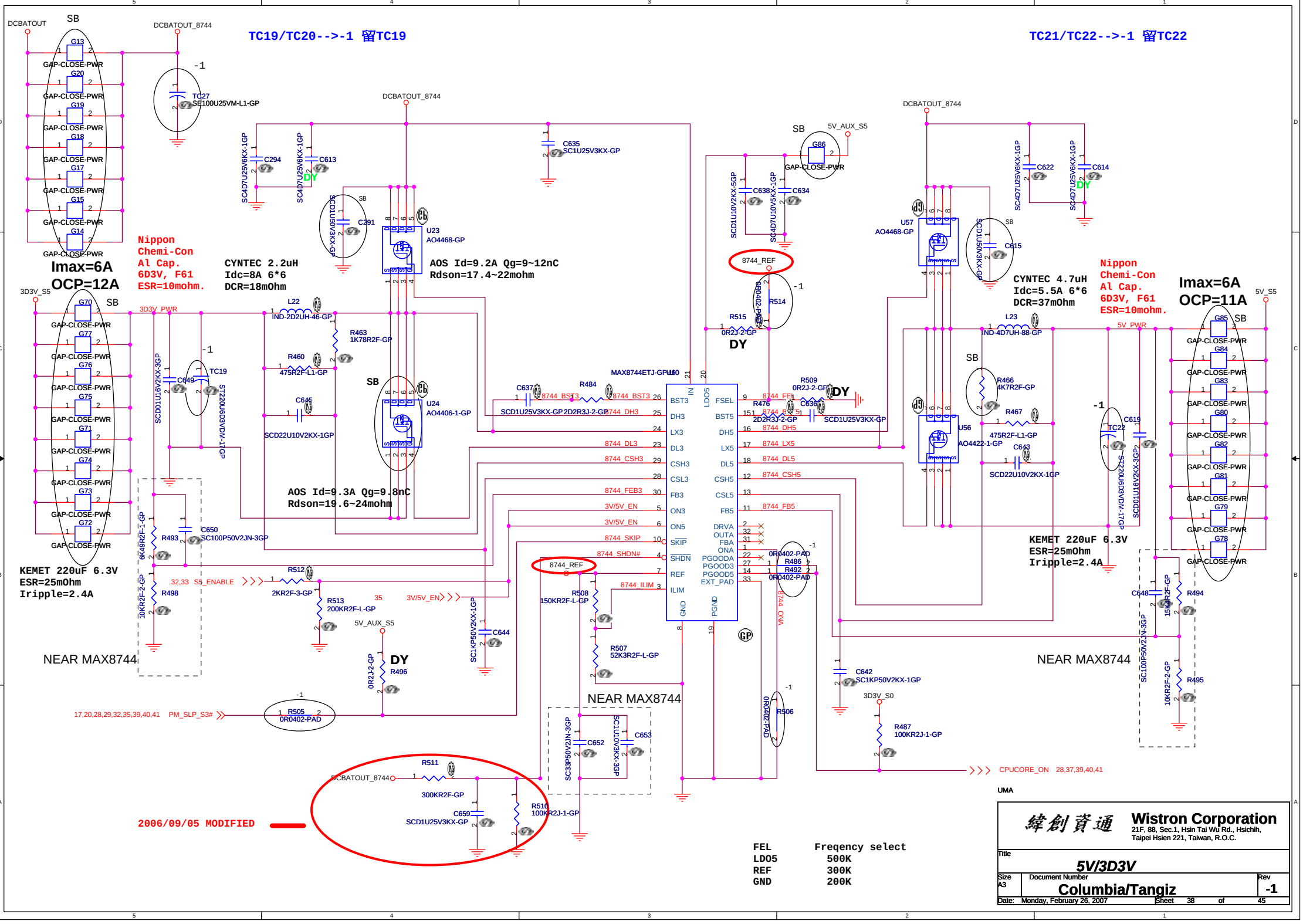
TC19/TC20-->-1 留TC19
TC21/TC22-->-1 留TC22
Imax=6A
OCP=12A
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
CYNTEC 2.2uH Idc=8A 6*6 DCR=18mOhm
AOS Id=9.2A Qg=9~12nC Rdson=17.4~22mohm
AOS Id=9.3A Qg=9.8nC Rdson=19.6~24mohm
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
NEAR MAX8744
CYNTEC 4.7uH Idc=5.5A 6*6 DCR=37mOhm
Imax=6A
OCP=11A
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
2006/09/05 MODIFIED
FEL Freqency select
LDO5 500K
REF 300K
GND 200K
UMA
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
5V/3D3V
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TC15/TC16-->-1 留TC15

TC17/TC18-->-1 留TC17

-1
SB
DCBATOUT
TC25
SE100U25VM-L1-GP

1D05V Iomax=12A
OCP>19A

Vcal.=1.0511V

CYNTEC 1uH
Idc=11A,Isat=22A
DCR=9mOhm

Rs2 = L / DCR / Cs2

Id=13A
Qg=10~14nC,
Rdson=9.4~12mohm

Id=14.5A
Qg=25~35nC,
Rdson=13.5~16.5mohm

Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm

Id=9.6A
Qg=18nC,
Rdson=13.5~16.5mohm

1D8V Iomax=9.5A
OCP>17A

Vcal.=1.8V

CYNTEC 2.2uH
Irms=14A Isat=16A
DCR=5.8~7mOhm

Rs1 = L / DCR / Cs1

Vout=(1+Ra/Rb)*1

Vout=[1+(Rc/Rd)]*1

Panasonic 330uF
2.5V ESR=15mOhm
Iripple=3.1A

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm

Panasonic 220uF
2.5V ESR=25mOhm
Iripple=1.8A

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm

2006.0928 add

SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping

FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz

Adjust the current limit threshold from R14, R15

VILIM = 0.5V~2.0V

Output Current =
ILIM / 10 / LDCR - dI/2

MAX8717ETI-T-GP

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Title: MAX8717 1D8V 1D05V

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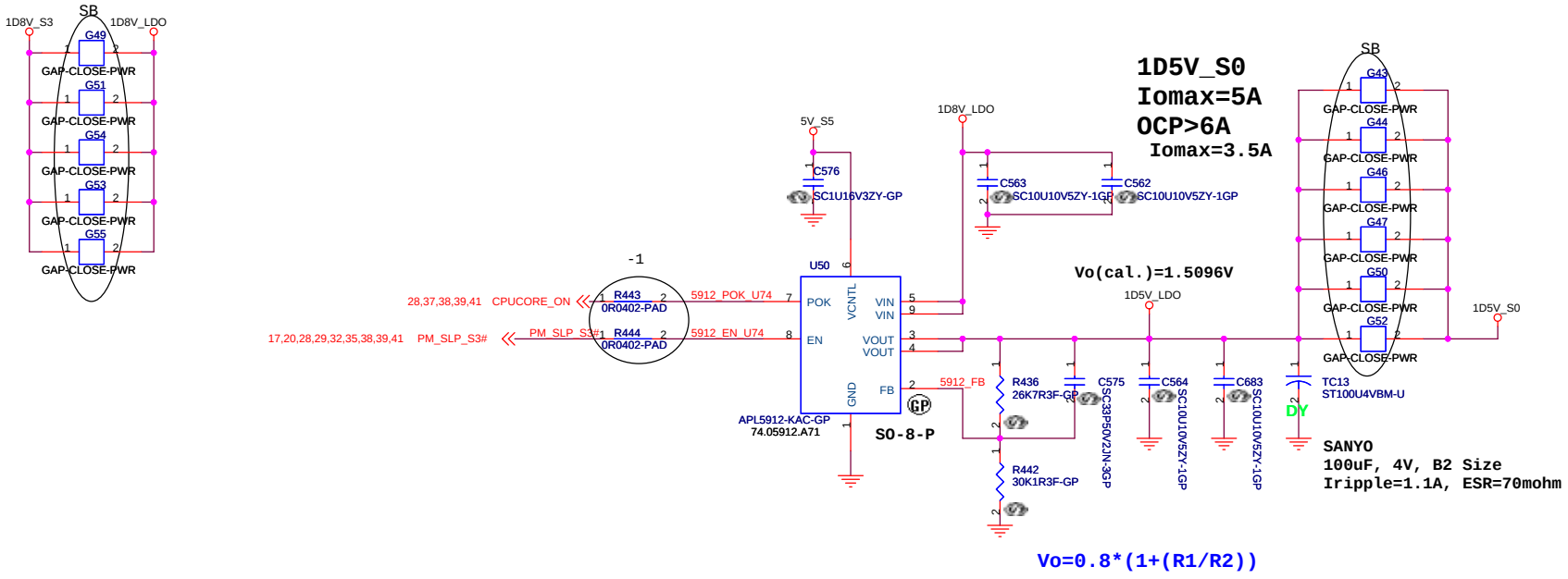

UMA

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Title	APW5912_1D5V	
Size	Document Number: Columbia/Tangiz	Rev: -1
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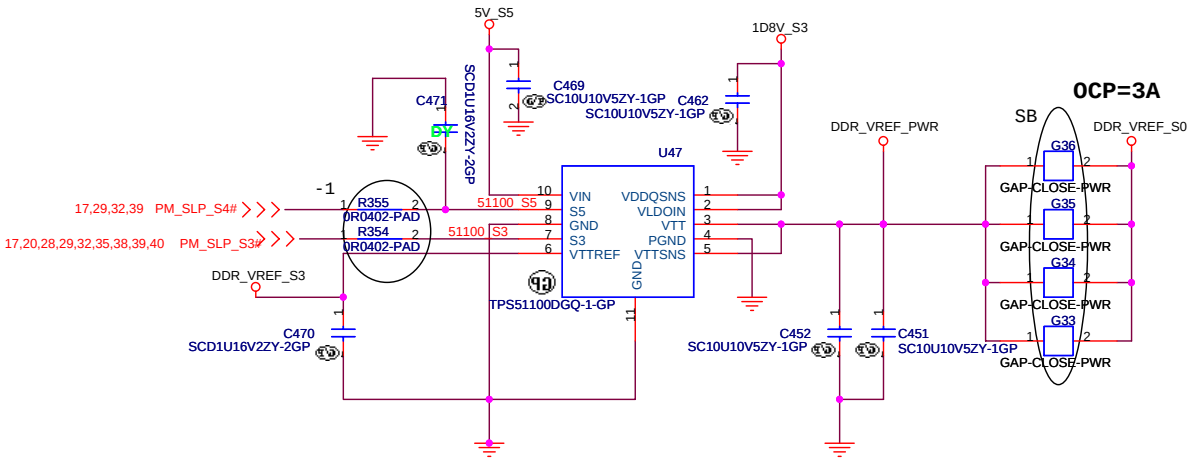
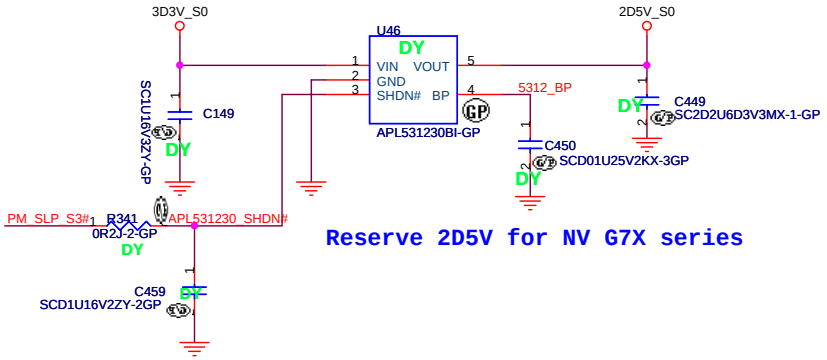
0D9V_S3
Iomax=1.2A

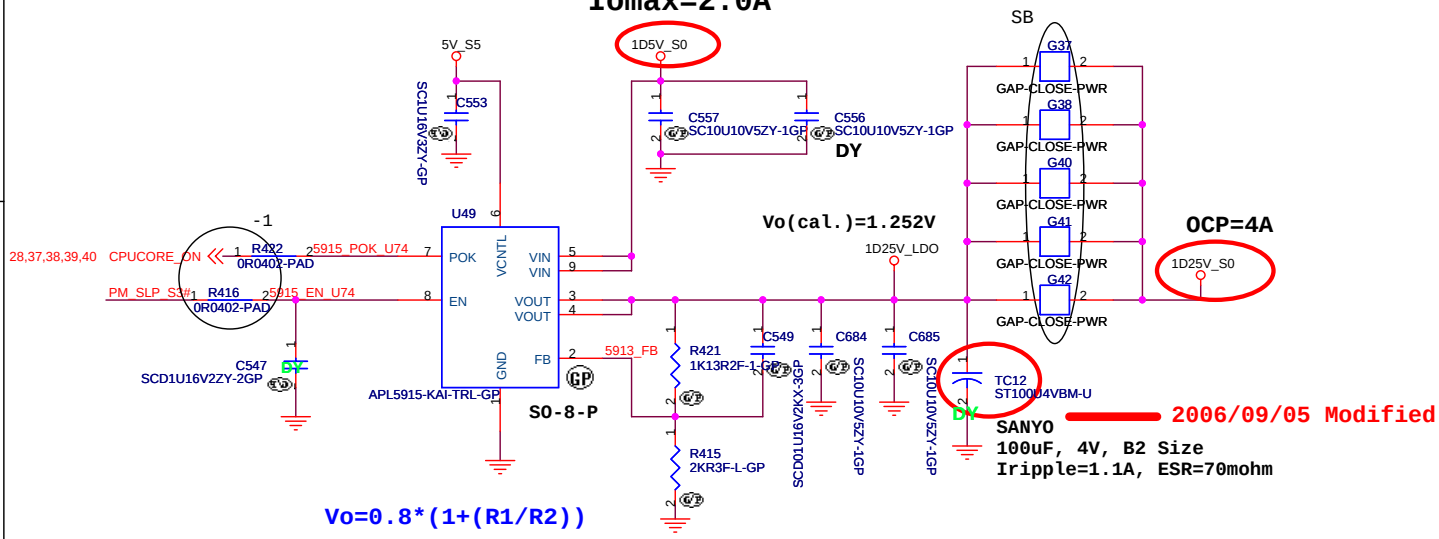


2D5V
Iomax=130mA



Reserve 2D5V for NV G7X series

1D25V_S0
Iomax=2.0A



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*1D25V/2D5V//1D05V/0D9V*	
Size B	Document Number **Columbia/Tangiz**	Rev -1
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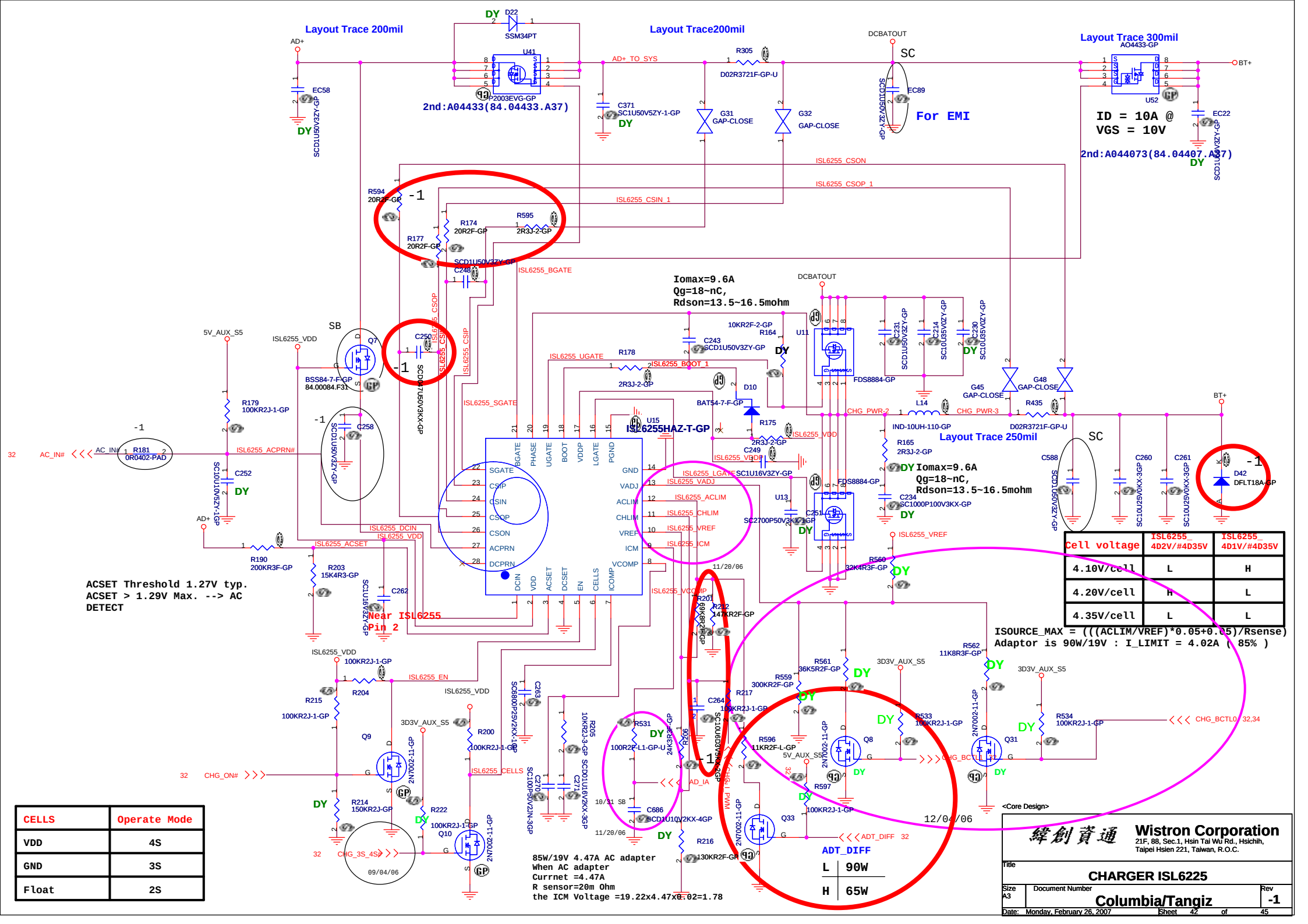
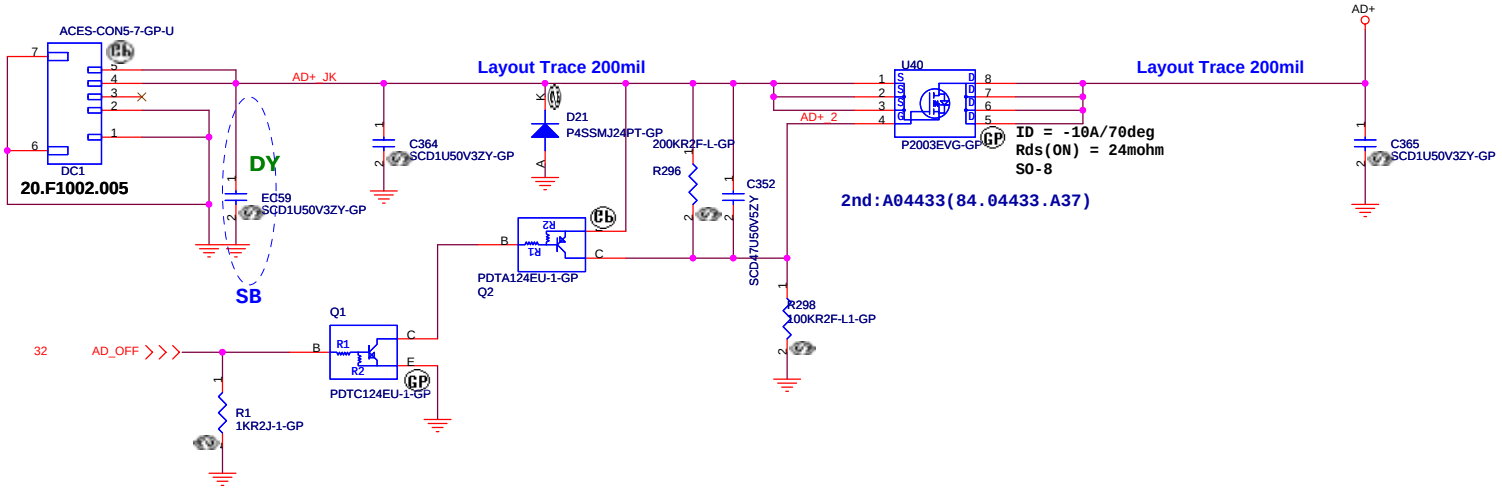


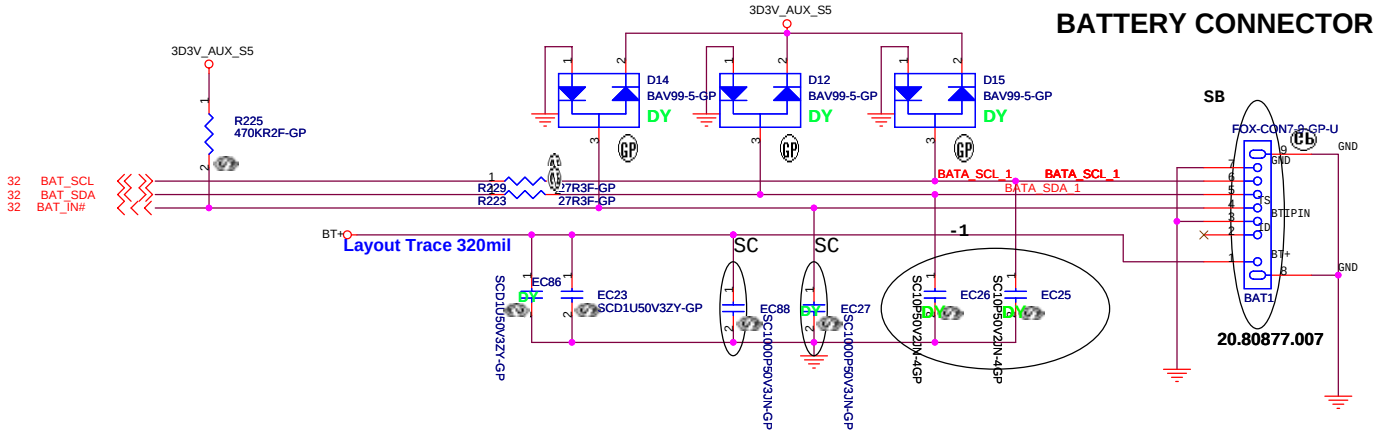
Cell voltage	ISL6255_4D2V/#4D35V	ISL6255_4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Variant Name>

緯創資通 **Wistron Corporation**
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Title	AD/BATT CONN	
Size A3	Document Number Columbia/Tangiz	Rev -1
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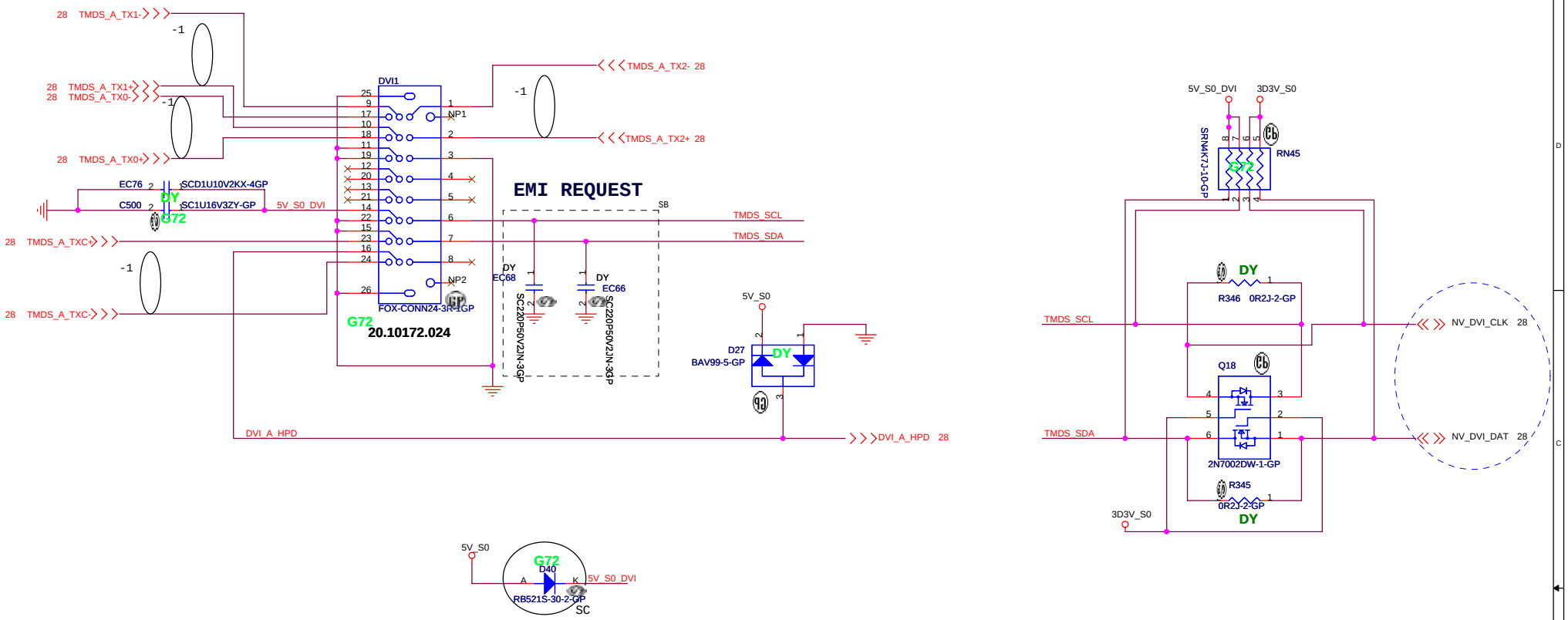

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: **DVI CONNECTOR**

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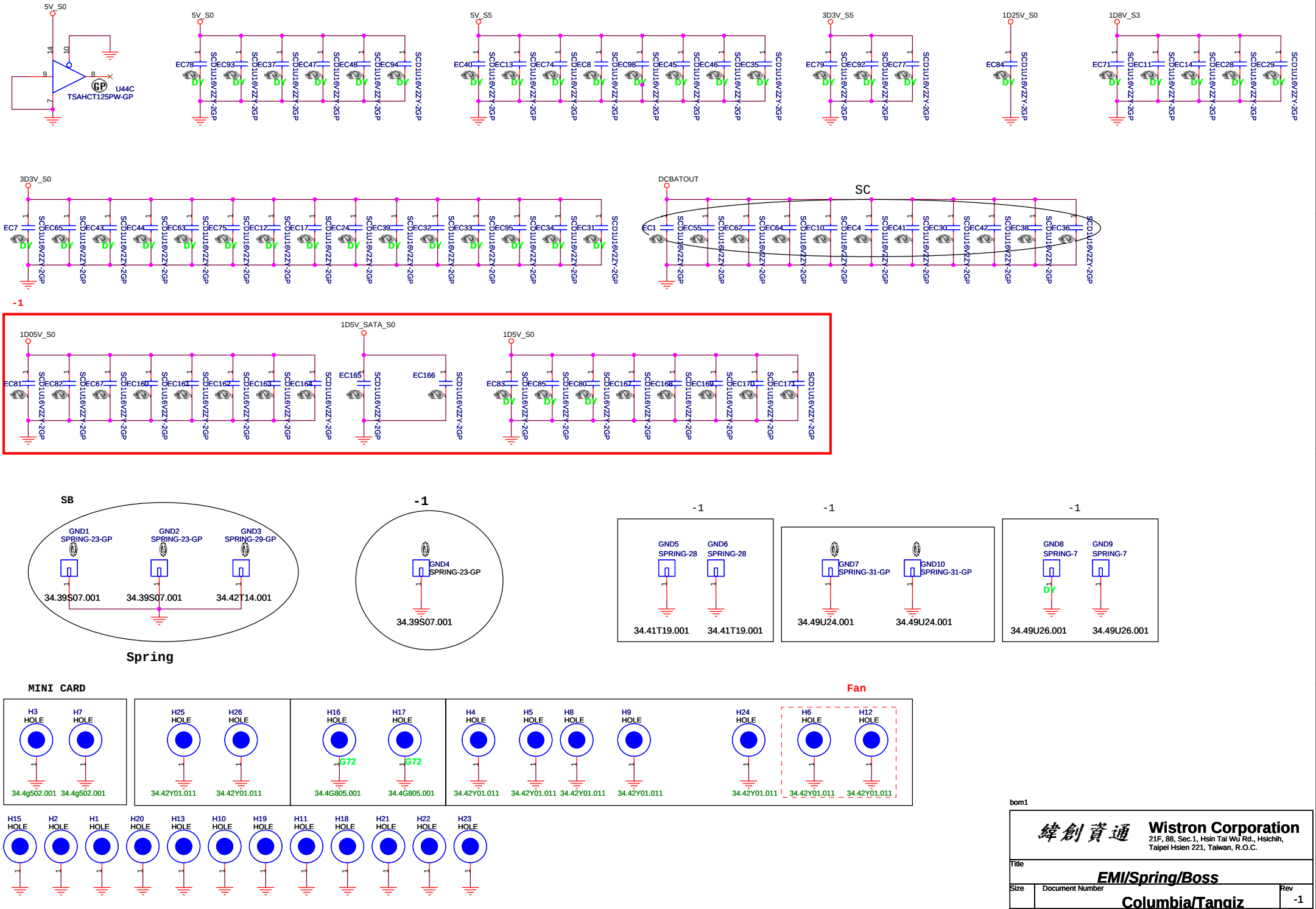

bom1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size | Document Number: **Columbia/Tangiz** | Rev: -1

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