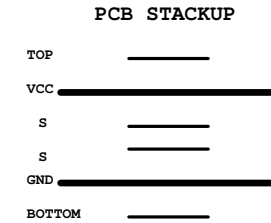
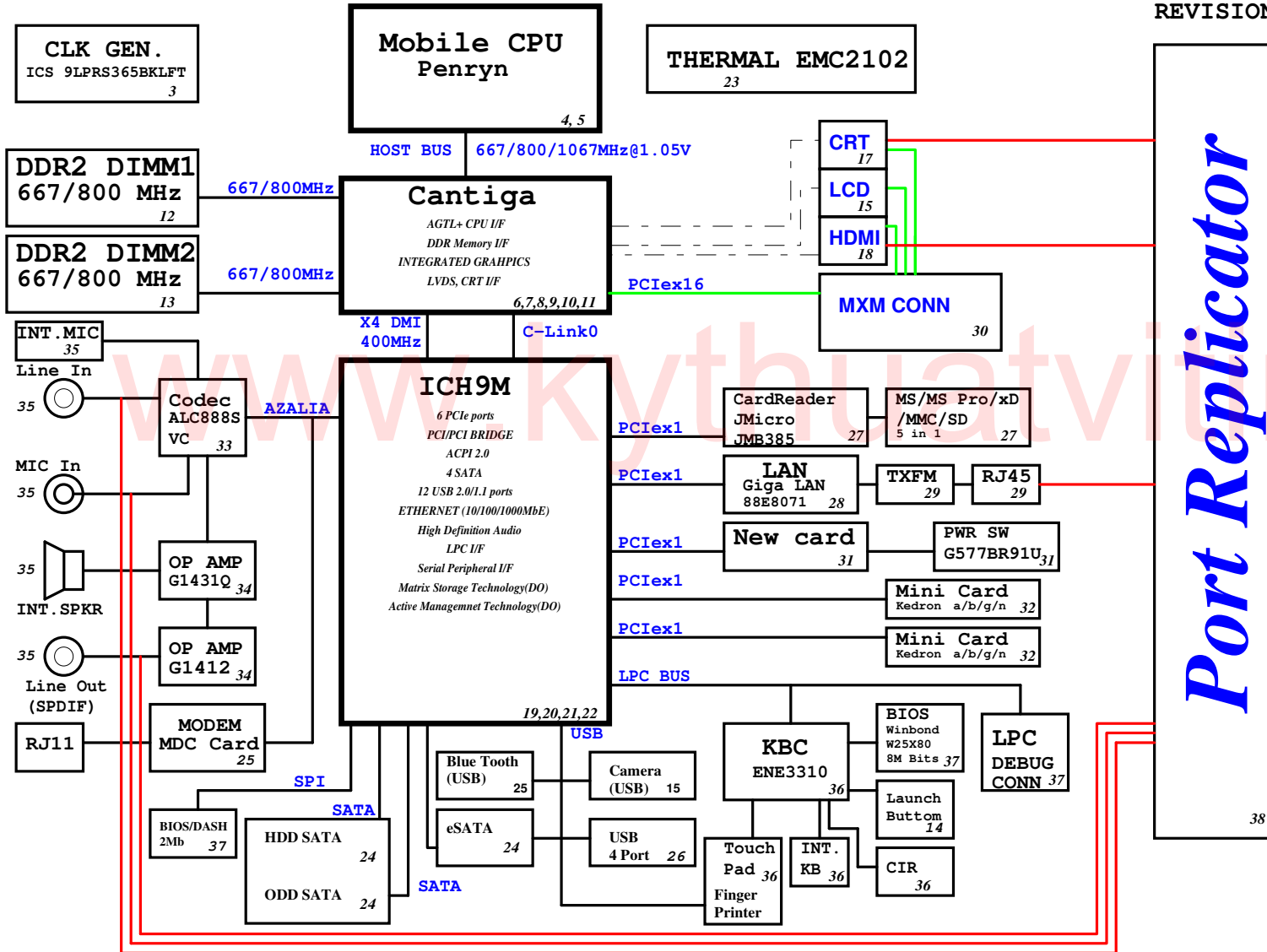


Eiger Block Diagram

Project code: 91.4Z501.001
 PCB P/N : 48.4Z501.001
 REVISION : 07246- -1



Port Replicator

SYSTEM DC/DC TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3
RT9018A 44	
1D8V_S3	1D5V_S0
G9131 44	
3D3V_S0	2D5V_S0
GFXCORE DC/DC ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V
CPU DC/DC ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V
CHARGER BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high, the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS1PVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled(Note2) 1 = The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALL2 mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIe disabled

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

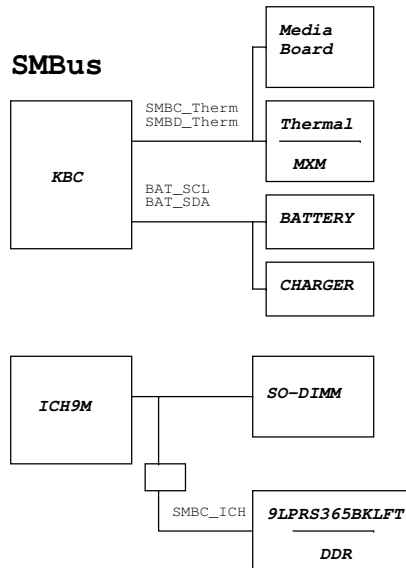
PCIe Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	NC

USB Table

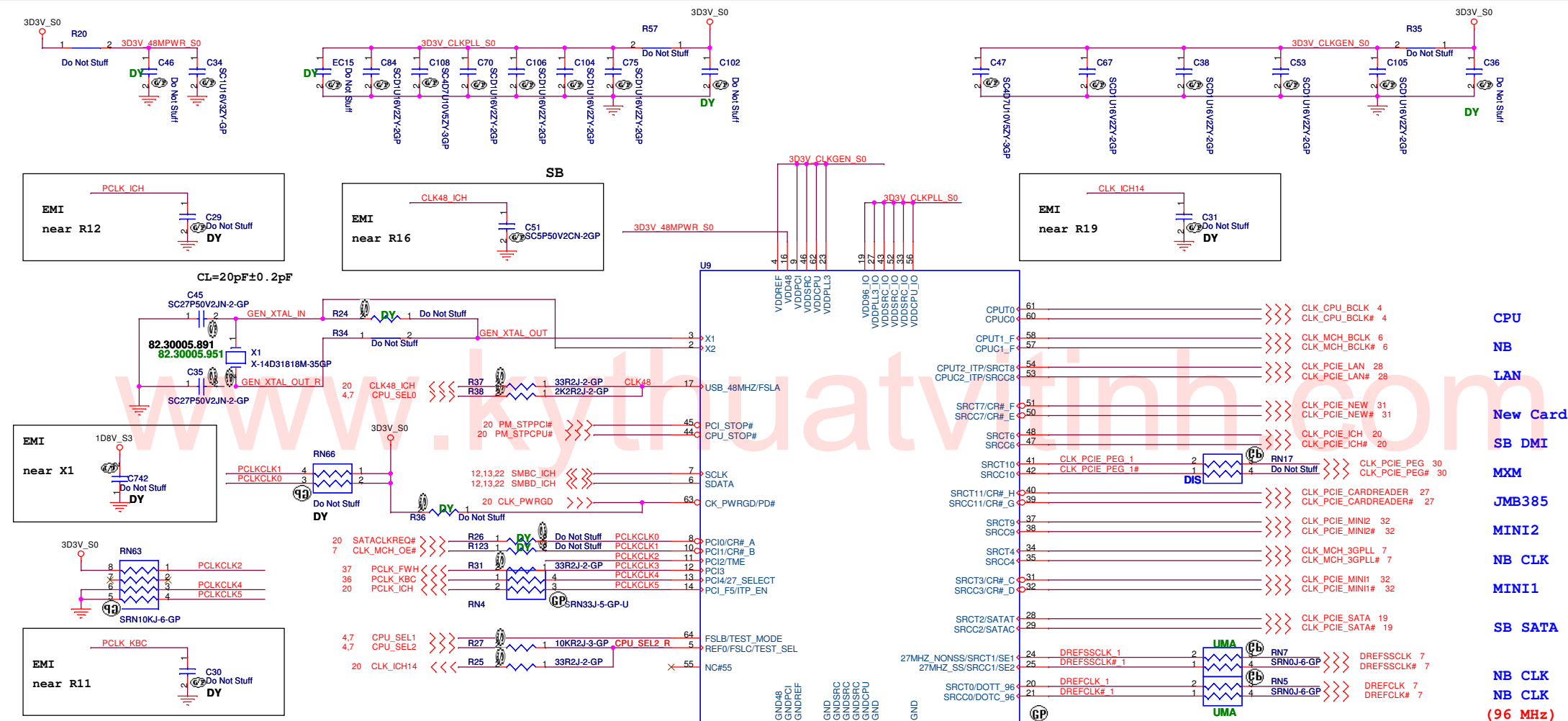
USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	USB5 (DOCK)
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

SMBus



UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Reference			
File	Document Number		Rev
Size A3	Eiger		-1
Date: Tuesday, April 01, 2008	Sheet 2	of	50



ICS9LPRS365BKLF1T setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1 = CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7 enabled (default) 1 = CR#_E controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1 = CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11 enabled (default) 1 = CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10

SEL2	SEL1	SEL0	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator**

Size: Document Number: **Eiger** Rev: -1

Date: Tuesday, April 01, 2008 Sheet 3 of 50

6 H_A#(35..3) <<<>> H_A#(35..3)

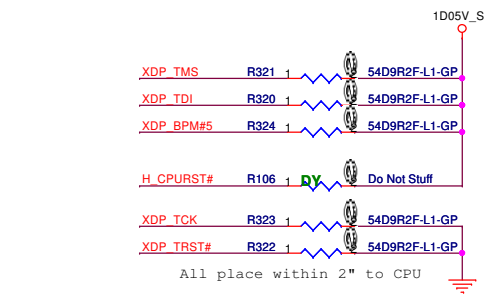
H_DINV#(3..0) <<<>> H_DINV#(3..0) 6
H_DSTBN#(3..0) <<<>> H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<<>> H_DSTBP#(3..0) 6
H_D#(63..0) <<<>> H_D#(63..0) 6

Side Band
Non GTL

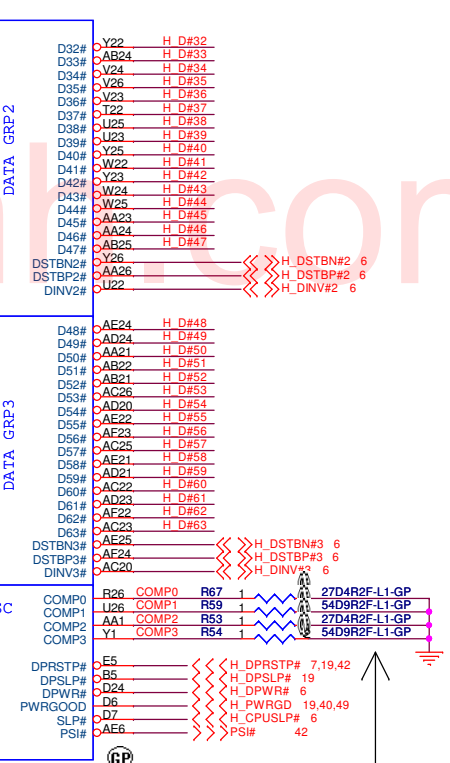
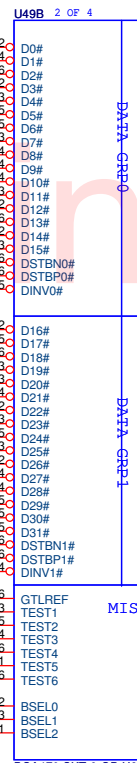
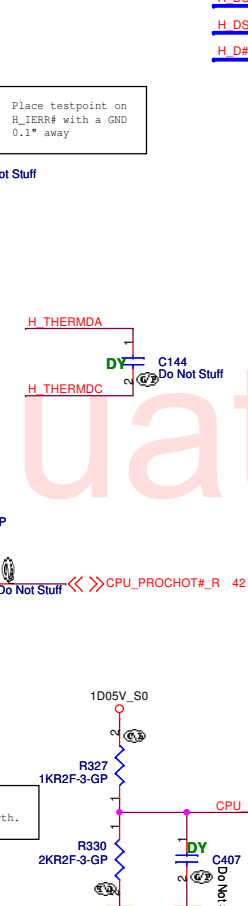
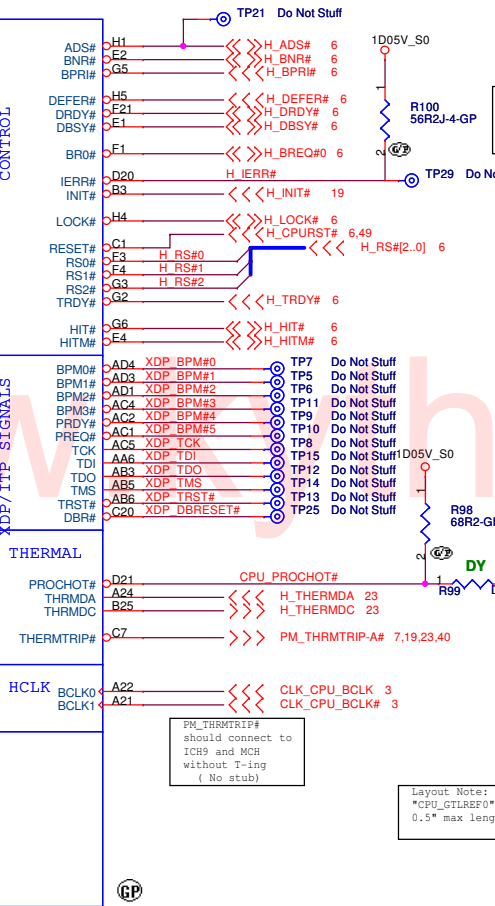
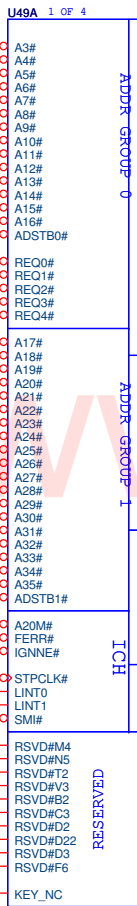
6 H_ADSTB#0 <<<>> H_ADSTB#0
6 H_REQ#(4..0) <<<>> H_REQ#(4..0)
19 H_A20M# <<<>> H_A20M#
19 H_FERR# <<<>> H_FERR#
19 H_IGNNE# <<<>> H_IGNNE#
19 H_STPCLK# <<<>> H_STPCLK#
19 H_INTR <<<>> H_INTR
19 H_NMI <<<>> H_NMI
19 H_SMI# <<<>> H_SMI#

Do Not Stuff#19 RSVD CPU 1 M4
Do Not Stuff#18 RSVD CPU 2 N5
Do Not Stuff#17 RSVD CPU 3 T2
Do Not Stuff#16 RSVD CPU 4 V3
Do Not Stuff#27 RSVD CPU 5 V3
Do Not Stuff#21 RSVD CPU 6 C3
Do Not Stuff#24 RSVD CPU 7 D2
Do Not Stuff#28 RSVD CPU 8 D22
Do Not Stuff#26 RSVD CPU 9 D3
Do Not Stuff#22 RSVD CPU 10 F6
Do Not Stuff#32 RSVD CPU 11 B1

BGA479-SKT-8-GP-U2
62.10053.401
62.10079.001

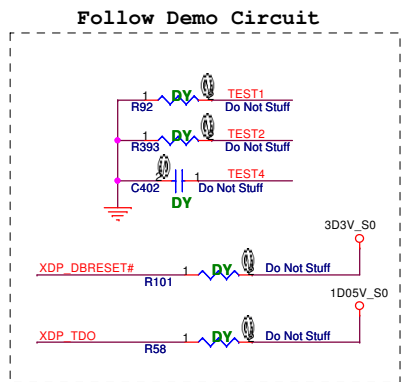


All place within 2" to CPU



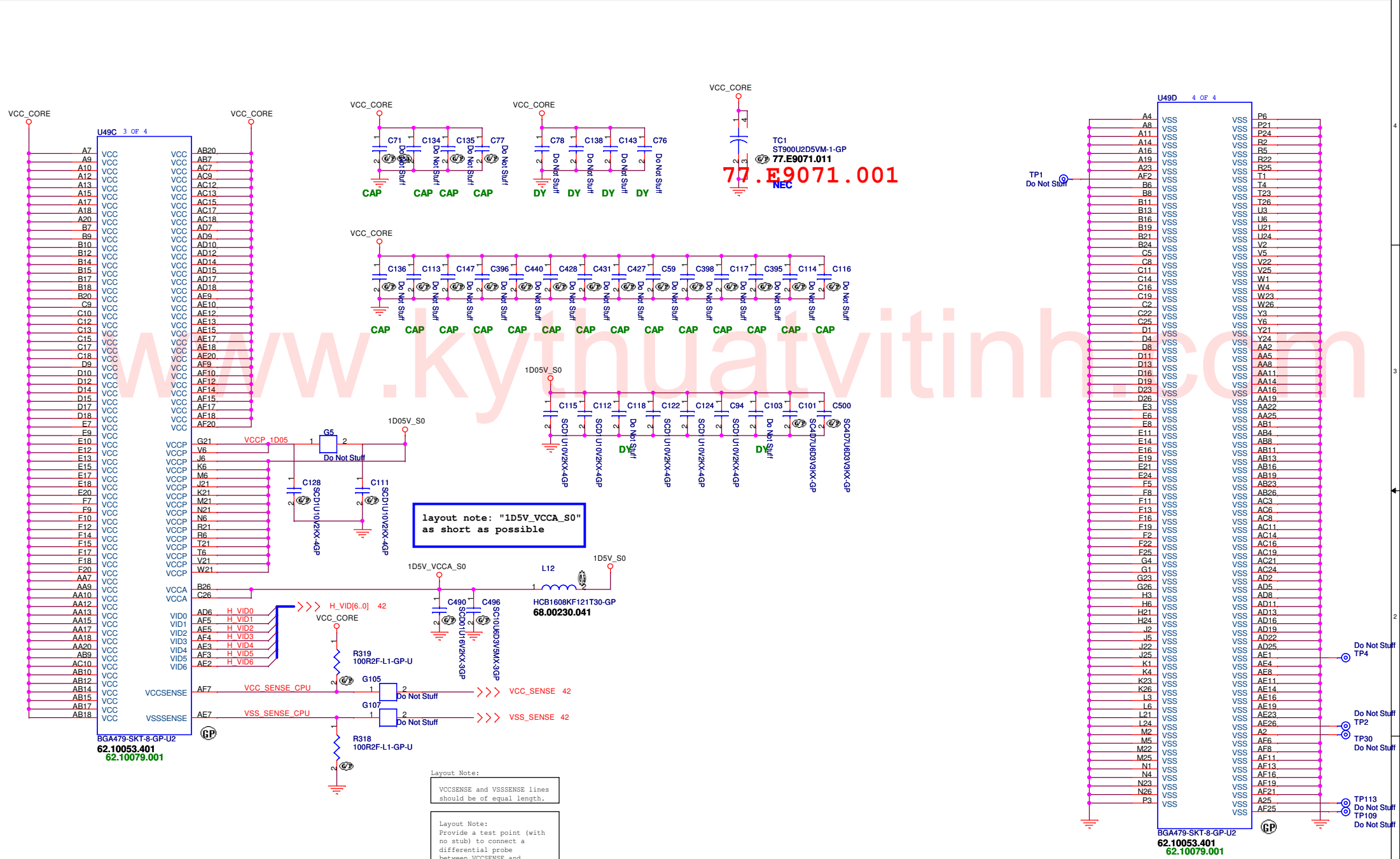
Layout Note:
CPU_GTLREF0
0.5" max length.

Layout Note:
Comp0, 2 connect with 20-27.4 ohm, make trace length shorter than 0.5"
Comp1, 3 connect with 20-55 ohm, make trace length shorter than 0.5"



Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

UMA
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title CPU (1 of 2)
Size Document Number Rev -1
Date: Tuesday, April 01, 2008 Sheet 4 of 50



TC1
ST900U2D5VM-1-GP
77.E9071.011
NEC
77.E9071.001

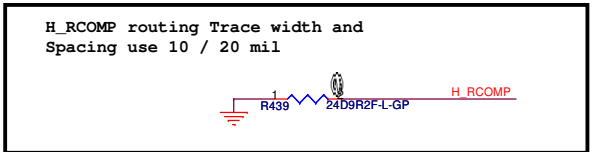
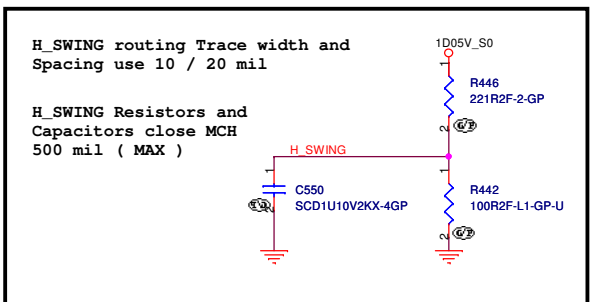
layout note: "1D5V_VCCA_S0"
as short as possible

Layout Note:
VCCSENSE and VSSSENSE lines
should be of equal length.

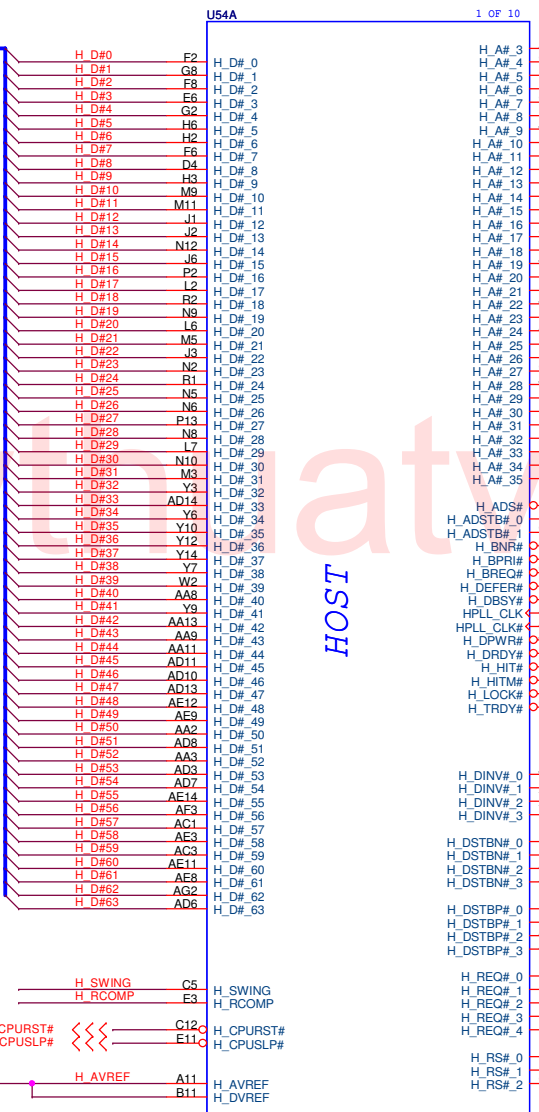
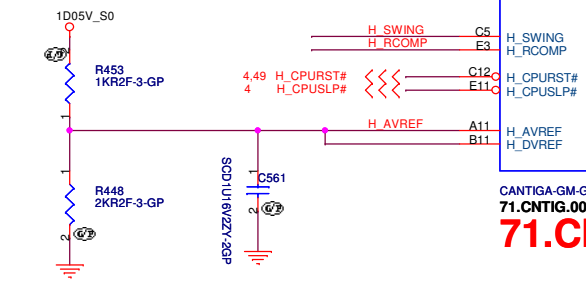
Layout Note:
Provide a test point (with
no stub) to connect a
differential probe
between VCCSENSE and
VSSSENSE at the location
where the two 54.9ohm
resistors terminate the
55 ohm transmission line.

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

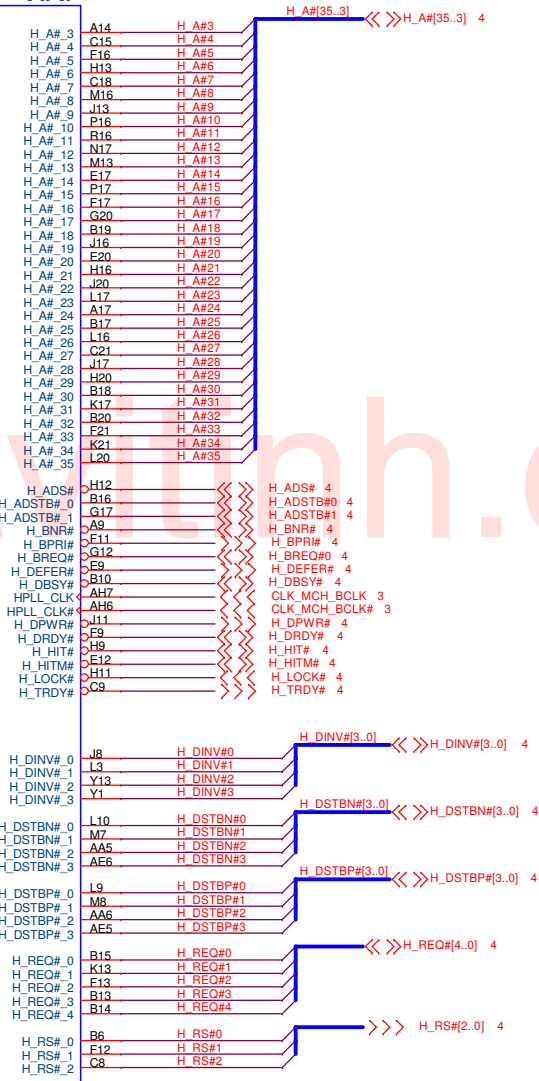
Title		
CPU (2 of 2)		
Size	Document Number	Rev
		-1
Eiger		
Date: Tuesday, April 01, 2008	Sheet 5	of 50



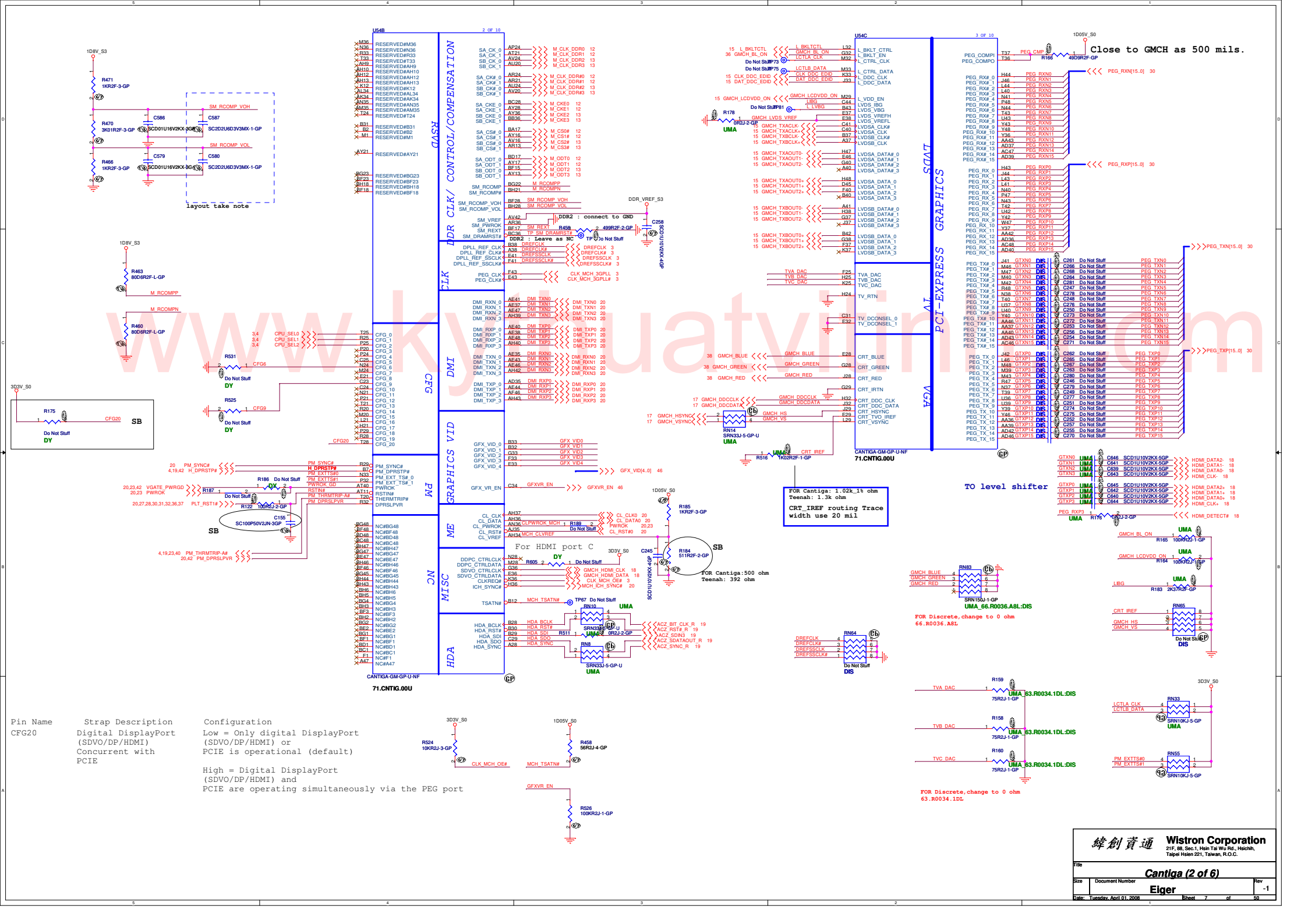
Place them near to the chip (< 0.5")



HOST



CANTIGA-GM-GP-U-NF
71.CNTIG.00U
71.CNTIG.D1U



Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI)	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default)
	Concurrent with PCIE	High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG strap

12 M_A_DQ[63.0] <<< M_A_DQ[63.0]

M A DQ0 AJ38 SA_DQ_0
 M A DQ1 AJ41 SA_DQ_1
 M A DQ2 AN38 SA_DQ_2
 M A DQ3 AM36 SA_DQ_3
 M A DQ4 AJ36 SA_DQ_4
 M A DQ5 AJ40 SA_DQ_5
 M A DQ6 AM44 SA_DQ_6
 M A DQ7 AM42 SA_DQ_7
 M A DQ8 AN43 SA_DQ_8
 M A DQ9 AN44 SA_DQ_9
 M A DQ10 AJ40 SA_DQ_10
 M A DQ11 AT38 SA_DQ_11
 M A DQ12 AN41 SA_DQ_12
 M A DQ13 AN39 SA_DQ_13
 M A DQ14 AU44 SA_DQ_14
 M A DQ15 AU42 SA_DQ_15
 M A DQ16 AV39 SA_DQ_16
 M A DQ17 AY44 SA_DQ_17
 M A DQ18 BA40 SA_DQ_18
 M A DQ19 BD43 SA_DQ_19
 M A DQ20 AV41 SA_DQ_20
 M A DQ21 AY43 SA_DQ_21
 M A DQ22 BA41 SA_DQ_22
 M A DQ23 BC40 SA_DQ_23
 M A DQ24 AY37 SA_DQ_24
 M A DQ25 BD38 SA_DQ_25
 M A DQ26 AV37 SA_DQ_26
 M A DQ27 AT36 SA_DQ_27
 M A DQ28 AY38 SA_DQ_28
 M A DQ29 BA39 SA_DQ_29
 M A DQ30 AV36 SA_DQ_30
 M A DQ31 AW36 SA_DQ_31
 M A DQ32 BD13 SA_DQ_32
 M A DQ33 AU11 SA_DQ_33
 M A DQ34 BC11 SA_DQ_34
 M A DQ35 BA12 SA_DQ_35
 M A DQ36 AU13 SA_DQ_36
 M A DQ37 AV13 SA_DQ_37
 M A DQ38 BD12 SA_DQ_38
 M A DQ39 BC12 SA_DQ_39
 M A DQ40 BA9 SA_DQ_40
 M A DQ41 BA9 SA_DQ_41
 M A DQ42 AU10 SA_DQ_42
 M A DQ43 AV9 SA_DQ_43
 M A DQ44 BA11 SA_DQ_44
 M A DQ45 BD9 SA_DQ_45
 M A DQ46 AY8 SA_DQ_46
 M A DQ47 BA6 SA_DQ_47
 M A DQ48 AV5 SA_DQ_48
 M A DQ49 AV7 SA_DQ_49
 M A DQ50 AT9 SA_DQ_50
 M A DQ51 AN8 SA_DQ_51
 M A DQ52 AU5 SA_DQ_52
 M A DQ53 AU6 SA_DQ_53
 M A DQ54 AT5 SA_DQ_54
 M A DQ55 AN10 SA_DQ_55
 M A DQ56 AM11 SA_DQ_56
 M A DQ57 AM5 SA_DQ_57
 M A DQ58 AJ9 SA_DQ_58
 M A DQ59 AJ8 SA_DQ_59
 M A DQ60 AN12 SA_DQ_60
 M A DQ61 AM13 SA_DQ_61
 M A DQ62 AJ11 SA_DQ_62
 M A DQ63 AJ12 SA_DQ_63

U54D 4 OF 10

DDR SYSTEM MEMORY A

SA_BS_0 BD21 >>> M_A_BS#0 12
 SA_BS_1 BG18 >>> M_A_BS#1 12
 SA_BS_2 AT25 >>> M_A_BS#2 12

SA_RAS# BB20 >>> M_A_RAS# 12
 SA_CAS# BD20 >>> M_A_CAS# 12
 SA_WE# AY20 >>> M_A_WE# 12

SA_DM_0 AM37 M A DM0 >>> M_A_DM[7..0] 12
 SA_DM_1 AT41 M A DM1 >>> M_A_DM[7..0] 12
 SA_DM_2 AY41 M A DM2 >>> M_A_DM[7..0] 12
 SA_DM_3 AU39 M A DM3 >>> M_A_DM[7..0] 12
 SA_DM_4 BB12 M A DM4 >>> M_A_DM[7..0] 12
 SA_DM_5 AT9 M A DM5 >>> M_A_DM[7..0] 12
 SA_DM_6 AJ5 M A DM6 >>> M_A_DM[7..0] 12
 SA_DM_7 AJ5 M A DM7 >>> M_A_DM[7..0] 12

SA_DQS_0 AJ44 M A DQS0 >>> M_A_DQS[7..0] 12
 SA_DQS_1 AT44 M A DQS1 >>> M_A_DQS[7..0] 12
 SA_DQS_2 BA43 M A DQS2 >>> M_A_DQS[7..0] 12
 SA_DQS_3 BC37 M A DQS3 >>> M_A_DQS[7..0] 12
 SA_DQS_4 AW12 M A DQS4 >>> M_A_DQS[7..0] 12
 SA_DQS_5 BC8 M A DQS5 >>> M_A_DQS[7..0] 12
 SA_DQS_6 AU8 M A DQS6 >>> M_A_DQS[7..0] 12
 SA_DQS_7 AM7 M A DQS7 >>> M_A_DQS[7..0] 12

SA_DQS#_0 AJ43 M A DQS#0 >>> M_A_DQS#[7..0] 12
 SA_DQS#_1 BA44 M A DQS#1 >>> M_A_DQS#[7..0] 12
 SA_DQS#_2 BD37 M A DQS#2 >>> M_A_DQS#[7..0] 12
 SA_DQS#_3 AY12 M A DQS#3 >>> M_A_DQS#[7..0] 12
 SA_DQS#_4 BD8 M A DQS#4 >>> M_A_DQS#[7..0] 12
 SA_DQS#_5 AU9 M A DQS#5 >>> M_A_DQS#[7..0] 12
 SA_DQS#_6 AM8 M A DQS#6 >>> M_A_DQS#[7..0] 12
 SA_DQS#_7 AM8 M A DQS#7 >>> M_A_DQS#[7..0] 12

SA_MA_0 BA21 M A A0 >>> M_A_A[14..0] 12
 SA_MA_1 BC24 M A A1 >>> M_A_A[14..0] 12
 SA_MA_2 BG24 M A A2 >>> M_A_A[14..0] 12
 SA_MA_3 BH24 M A A3 >>> M_A_A[14..0] 12
 SA_MA_4 BG25 M A A4 >>> M_A_A[14..0] 12
 SA_MA_5 BA24 M A A5 >>> M_A_A[14..0] 12
 SA_MA_6 BD24 M A A6 >>> M_A_A[14..0] 12
 SA_MA_7 BG27 M A A7 >>> M_A_A[14..0] 12
 SA_MA_8 BF25 M A A8 >>> M_A_A[14..0] 12
 SA_MA_9 AW24 M A A9 >>> M_A_A[14..0] 12
 SA_MA_10 BC21 M A A10 >>> M_A_A[14..0] 12
 SA_MA_11 BG26 M A A11 >>> M_A_A[14..0] 12
 SA_MA_12 BH17 M A A12 >>> M_A_A[14..0] 12
 SA_MA_13 BH17 M A A13 >>> M_A_A[14..0] 12
 SA_MA_14 AY25 M A A14 >>> M_A_A[14..0] 12

CANTIGA-GM-GP-U-NF
71.CNTIG.00U

13 M_B_DQ[63.0] <<< M_B_DQ[63.0]

M B DQ0 AK47 SB_DQ_0
 M B DQ1 AH46 SB_DQ_1
 M B DQ2 AP47 SB_DQ_2
 M B DQ3 AP46 SB_DQ_3
 M B DQ4 AJ46 SB_DQ_4
 M B DQ5 AJ48 SB_DQ_5
 M B DQ6 AM48 SB_DQ_6
 M B DQ7 AP48 SB_DQ_7
 M B DQ8 AU47 SB_DQ_8
 M B DQ9 AJ46 SB_DQ_9
 M B DQ10 BA48 SB_DQ_10
 M B DQ11 AY48 SB_DQ_11
 M B DQ12 AT47 SB_DQ_12
 M B DQ13 AR47 SB_DQ_13
 M B DQ14 BA47 SB_DQ_14
 M B DQ15 BC47 SB_DQ_15
 M B DQ16 BC46 SB_DQ_16
 M B DQ17 BC44 SB_DQ_17
 M B DQ18 BG43 SB_DQ_18
 M B DQ19 BF43 SB_DQ_19
 M B DQ20 BE45 SB_DQ_20
 M B DQ21 BC41 SB_DQ_21
 M B DQ22 BF40 SB_DQ_22
 M B DQ23 BF41 SB_DQ_23
 M B DQ24 RG38 SB_DQ_24
 M B DQ25 BF38 SB_DQ_25
 M B DQ26 BH35 SB_DQ_26
 M B DQ27 BG35 SB_DQ_27
 M B DQ28 BH40 SB_DQ_28
 M B DQ29 RG39 SB_DQ_29
 M B DQ30 RG34 SB_DQ_30
 M B DQ31 BH34 SB_DQ_31
 M B DQ32 BH14 SB_DQ_32
 M B DQ33 BG12 SB_DQ_33
 M B DQ34 BH11 SB_DQ_34
 M B DQ35 BG8 SB_DQ_35
 M B DQ36 BH12 SB_DQ_36
 M B DQ37 BE11 SB_DQ_37
 M B DQ38 BF8 SB_DQ_38
 M B DQ39 BG7 SB_DQ_39
 M B DQ40 BC5 SB_DQ_40
 M B DQ41 BC6 SB_DQ_41
 M B DQ42 AY3 SB_DQ_42
 M B DQ43 AY2 SB_DQ_43
 M B DQ44 BF6 SB_DQ_44
 M B DQ45 BF5 SB_DQ_45
 M B DQ46 BA1 SB_DQ_46
 M B DQ47 BD3 SB_DQ_47
 M B DQ48 AV2 SB_DQ_48
 M B DQ49 AU3 SB_DQ_49
 M B DQ50 AR3 SB_DQ_50
 M B DQ51 AN2 SB_DQ_51
 M B DQ52 AY2 SB_DQ_52
 M B DQ53 AV1 SB_DQ_53
 M B DQ54 AP3 SB_DQ_54
 M B DQ55 AR1 SB_DQ_55
 M B DQ56 AL1 SB_DQ_56
 M B DQ57 AL2 SB_DQ_57
 M B DQ58 AJ1 SB_DQ_58
 M B DQ59 AH1 SB_DQ_59
 M B DQ60 AM2 SB_DQ_60
 M B DQ61 AM3 SB_DQ_61
 M B DQ62 A33 SB_DQ_62
 M B DQ63 A35 SB_DQ_63

U54E 5 OF 10

DDR SYSTEM MEMORY B

SB_BS_0 BC16 >>> M_B_BS#0 13
 SB_BS_1 BB17 >>> M_B_BS#1 13
 SB_BS_2 BB33 >>> M_B_BS#2 13

SB_RAS# AU17 >>> M_B_RAS# 13
 SB_CAS# BG16 >>> M_B_CAS# 13
 SB_WE# BF14 >>> M_B_WE# 13

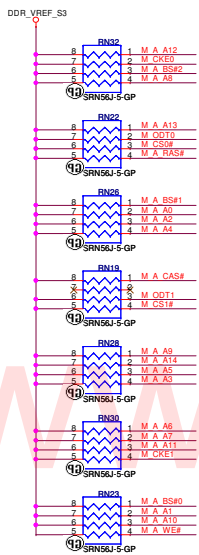
SB_DM_0 AM47 M B DM0 >>> M_B_DM[7..0] 13
 SB_DM_1 AY47 M B DM1 >>> M_B_DM[7..0] 13
 SB_DM_2 BD40 M B DM2 >>> M_B_DM[7..0] 13
 SB_DM_3 BF35 M B DM3 >>> M_B_DM[7..0] 13
 SB_DM_4 BG11 M B DM4 >>> M_B_DM[7..0] 13
 SB_DM_5 BA3 M B DM5 >>> M_B_DM[7..0] 13
 SB_DM_6 AP1 M B DM6 >>> M_B_DM[7..0] 13
 SB_DM_7 AK2 M B DM7 >>> M_B_DM[7..0] 13

SB_DQS_0 AL47 M B DQS0 >>> M_B_DQS[7..0] 13
 SB_DQS_1 AV48 M B DQS1 >>> M_B_DQS[7..0] 13
 SB_DQS_2 BC41 M B DQS2 >>> M_B_DQS[7..0] 13
 SB_DQS_3 RG37 M B DQS3 >>> M_B_DQS[7..0] 13
 SB_DQS_4 BH9 M B DQS4 >>> M_B_DQS[7..0] 13
 SB_DQS_5 BB2 M B DQS5 >>> M_B_DQS[7..0] 13
 SB_DQS_6 AU1 M B DQS6 >>> M_B_DQS[7..0] 13
 SB_DQS_7 AN6 M B DQS7 >>> M_B_DQS[7..0] 13

SB_DQS#_0 AL49 M B DQS#0 >>> M_B_DQS#[7..0] 13
 SB_DQS#_1 AV49 M B DQS#1 >>> M_B_DQS#[7..0] 13
 SB_DQS#_2 BH41 M B DQS#2 >>> M_B_DQS#[7..0] 13
 SB_DQS#_3 BH37 M B DQS#3 >>> M_B_DQS#[7..0] 13
 SB_DQS#_4 BG9 M B DQS#4 >>> M_B_DQS#[7..0] 13
 SB_DQS#_5 BC2 M B DQS#5 >>> M_B_DQS#[7..0] 13
 SB_DQS#_6 AT2 M B DQS#6 >>> M_B_DQS#[7..0] 13
 SB_DQS#_7 AN5 M B DQS#7 >>> M_B_DQS#[7..0] 13

SB_MA_0 AV17 M B A0 >>> M_B_A[14..0] 13
 SB_MA_1 BA25 M B A1 >>> M_B_A[14..0] 13
 SB_MA_2 BC25 M B A2 >>> M_B_A[14..0] 13
 SB_MA_3 AU25 M B A3 >>> M_B_A[14..0] 13
 SB_MA_4 AW25 M B A4 >>> M_B_A[14..0] 13
 SB_MA_5 BB28 M B A5 >>> M_B_A[14..0] 13
 SB_MA_6 AU28 M B A6 >>> M_B_A[14..0] 13
 SB_MA_7 AW28 M B A7 >>> M_B_A[14..0] 13
 SB_MA_8 AT33 M B A8 >>> M_B_A[14..0] 13
 SB_MA_9 BD33 M B A9 >>> M_B_A[14..0] 13
 SB_MA_10 BB16 M B A10 >>> M_B_A[14..0] 13
 SB_MA_11 AW33 M B A11 >>> M_B_A[14..0] 13
 SB_MA_12 BH15 M B A12 >>> M_B_A[14..0] 13
 SB_MA_13 AU33 M B A13 >>> M_B_A[14..0] 13
 SB_MA_14 AU33 M B A14 >>> M_B_A[14..0] 13

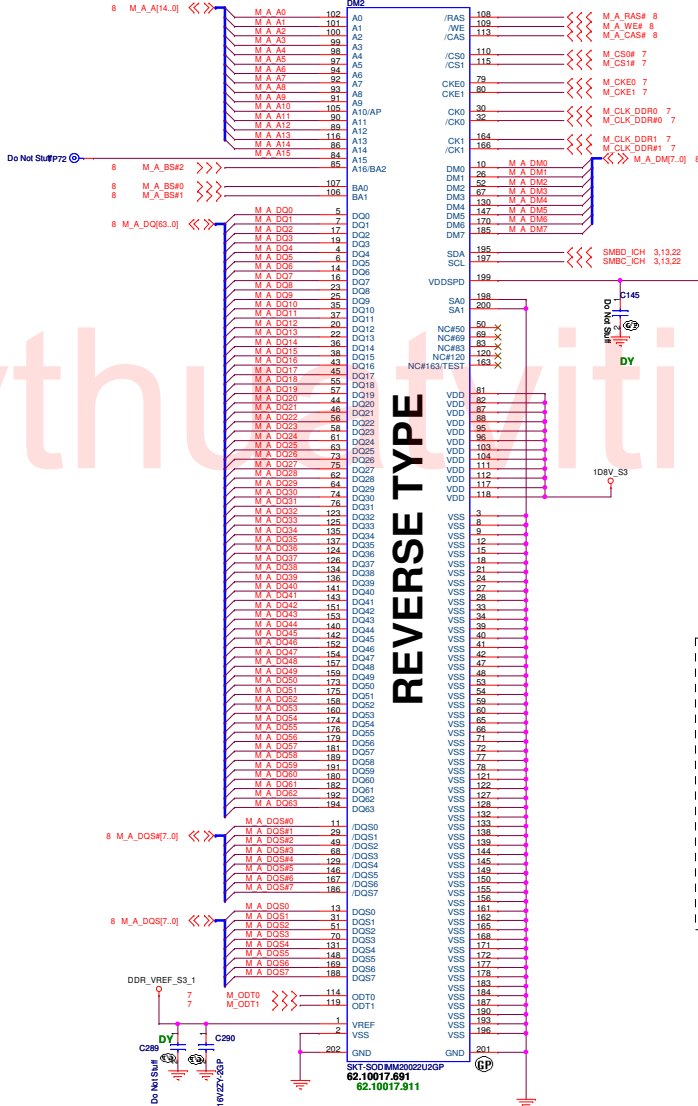
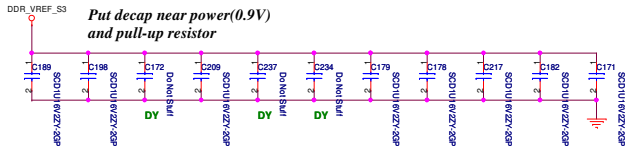
CANTIGA-GM-GP-U-NF
71.CNTIG.00U



PARALLEL TERMINATION

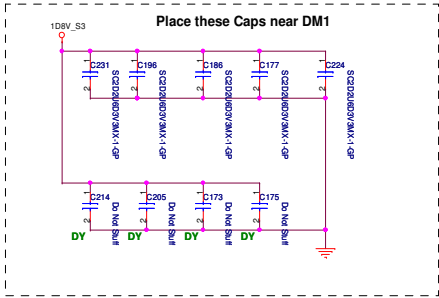
Put decap near power(0.9V) and pull-up resistor

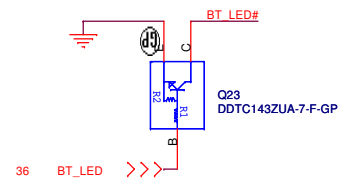
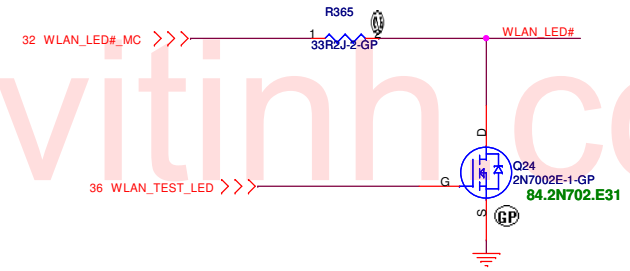
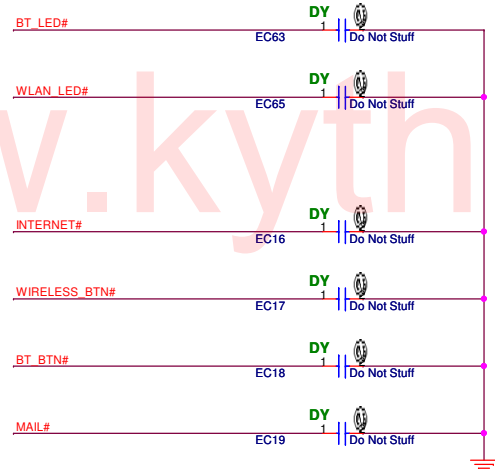
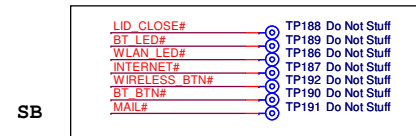
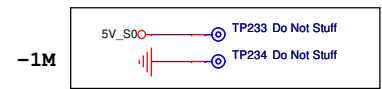
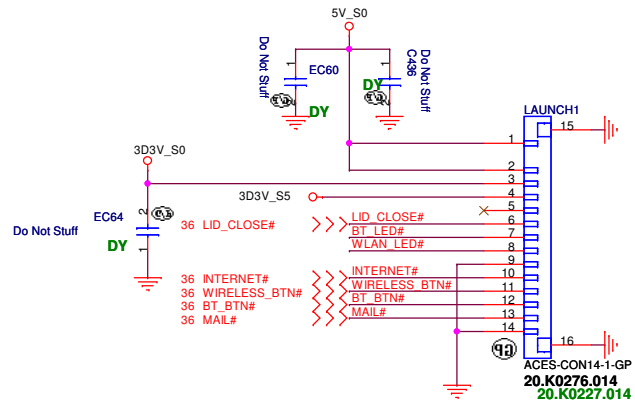
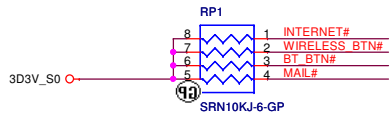
Decoupling Capacitor



REVERSE TYPE

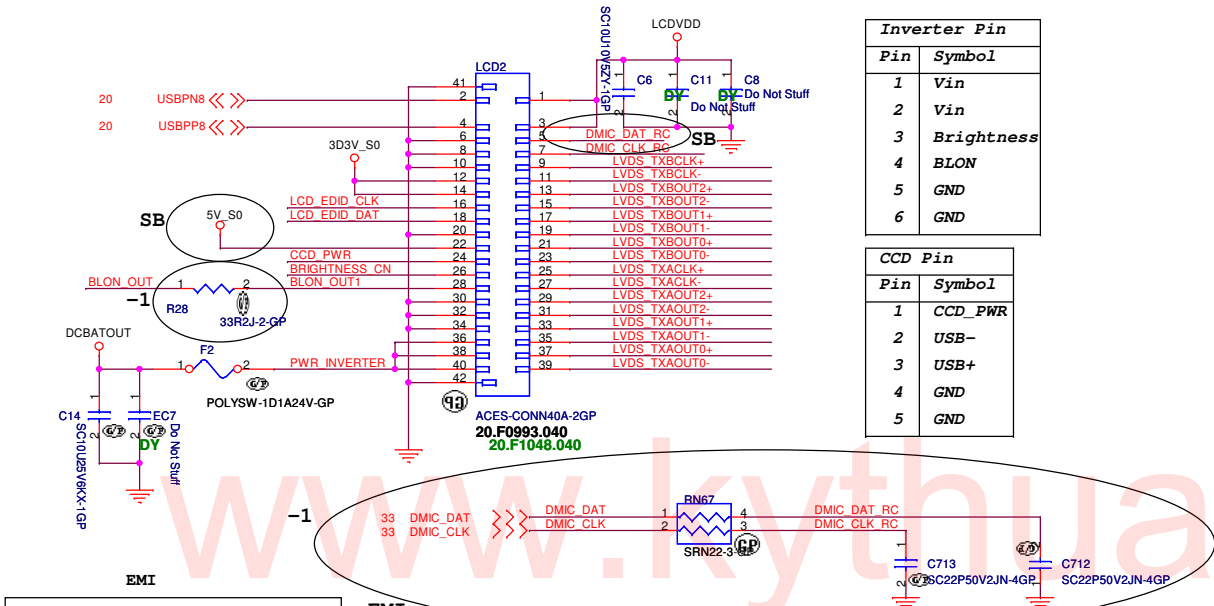
High 5.2mm





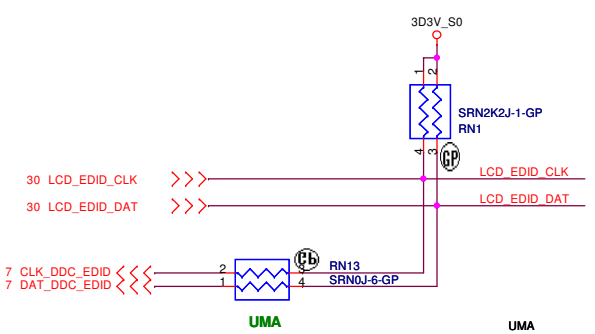
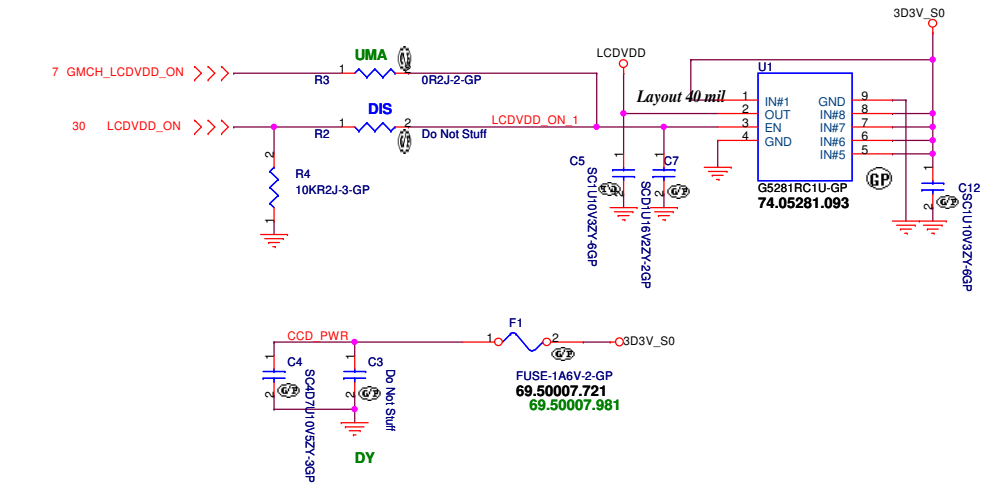
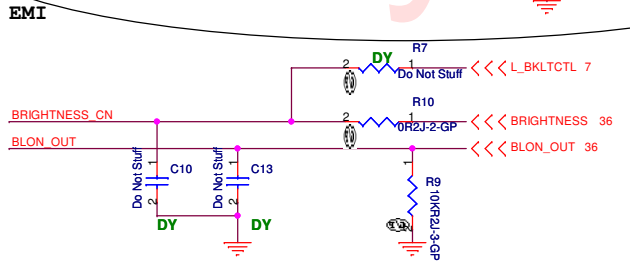
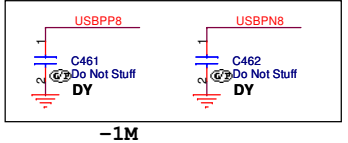
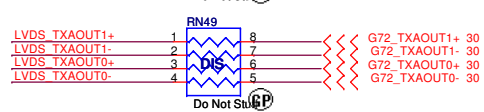
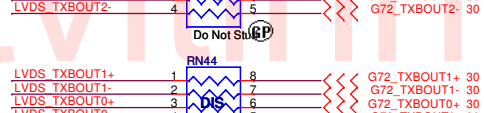
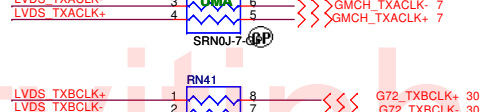
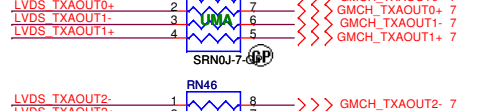
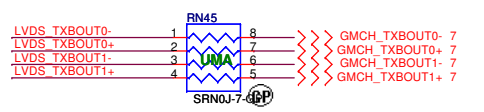
www.kythuatchitinh.com

LCD/INVERTER/CCD CONN



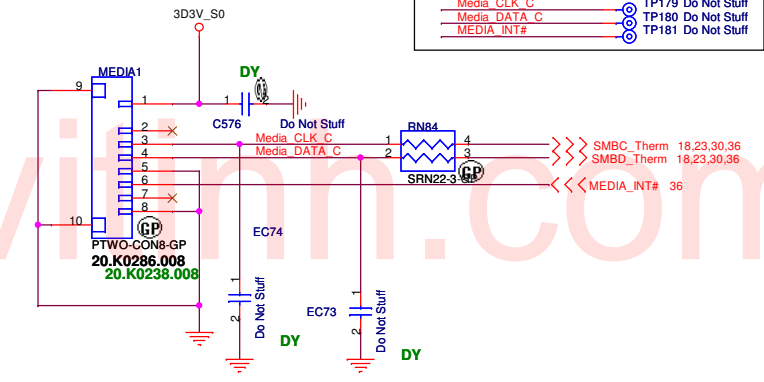
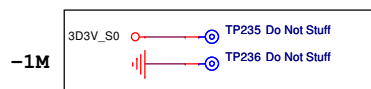
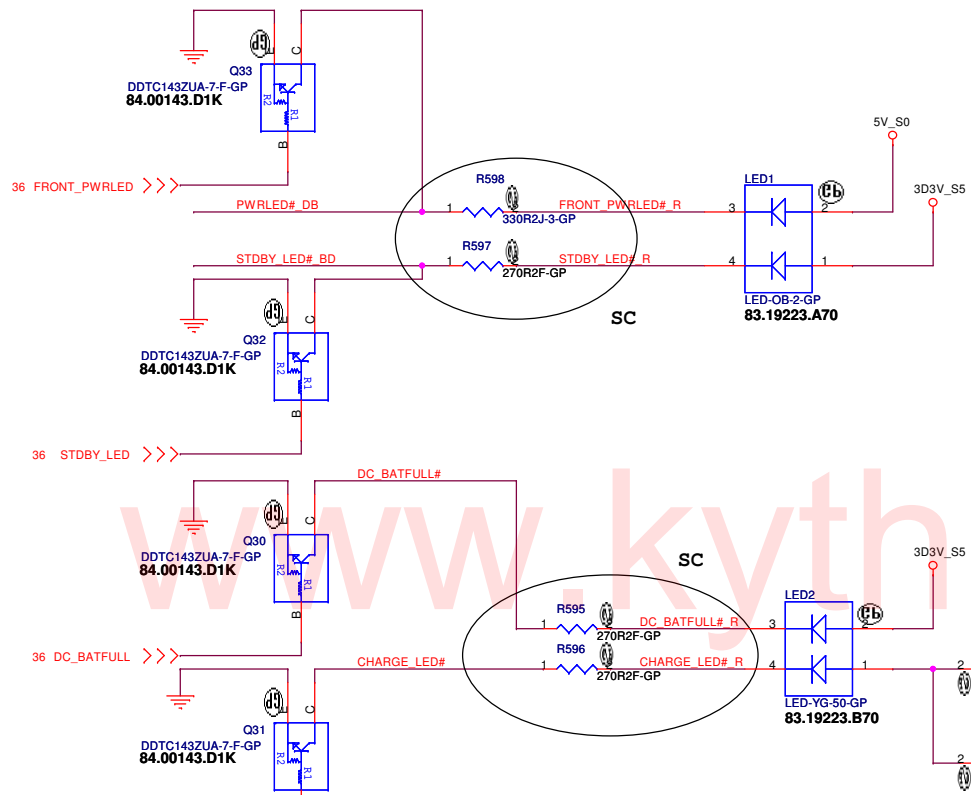
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

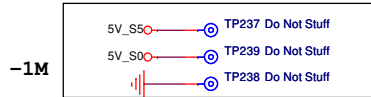
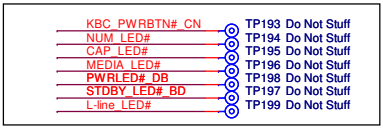
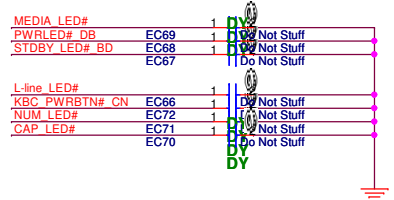
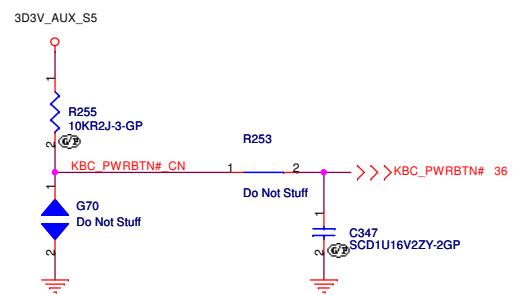
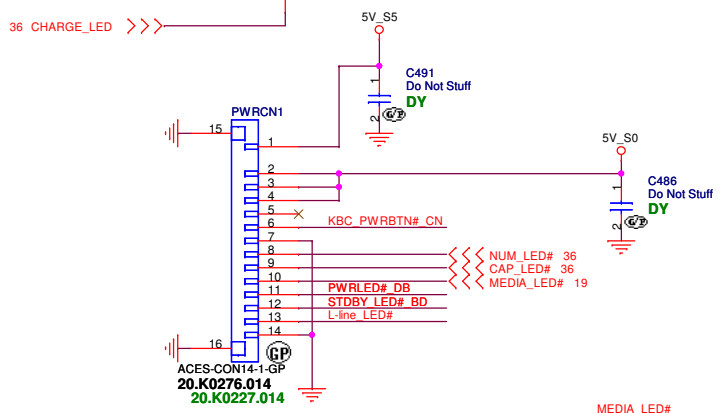


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LCD CONN			
File			
Size	Document Number	Eiger	Rev -1
Date: Tuesday, April 01, 2008	Sheet	15	of 50



MEDIA BOARD



UMA

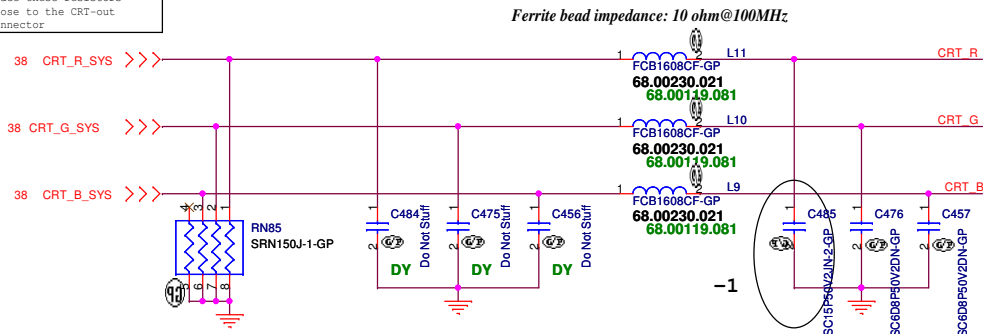
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Title: **Power & Media Board**

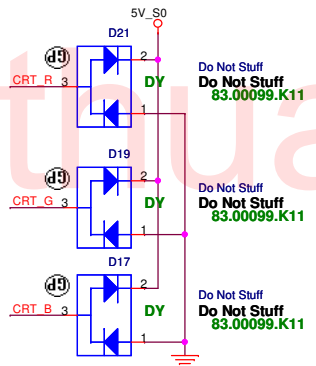
Size: Document Number: Rev: -1

Date: Tuesday, April 01, 2008 Sheet 16 of 50

Layout Note:
Place these resistors
close to the CRT-out
connector

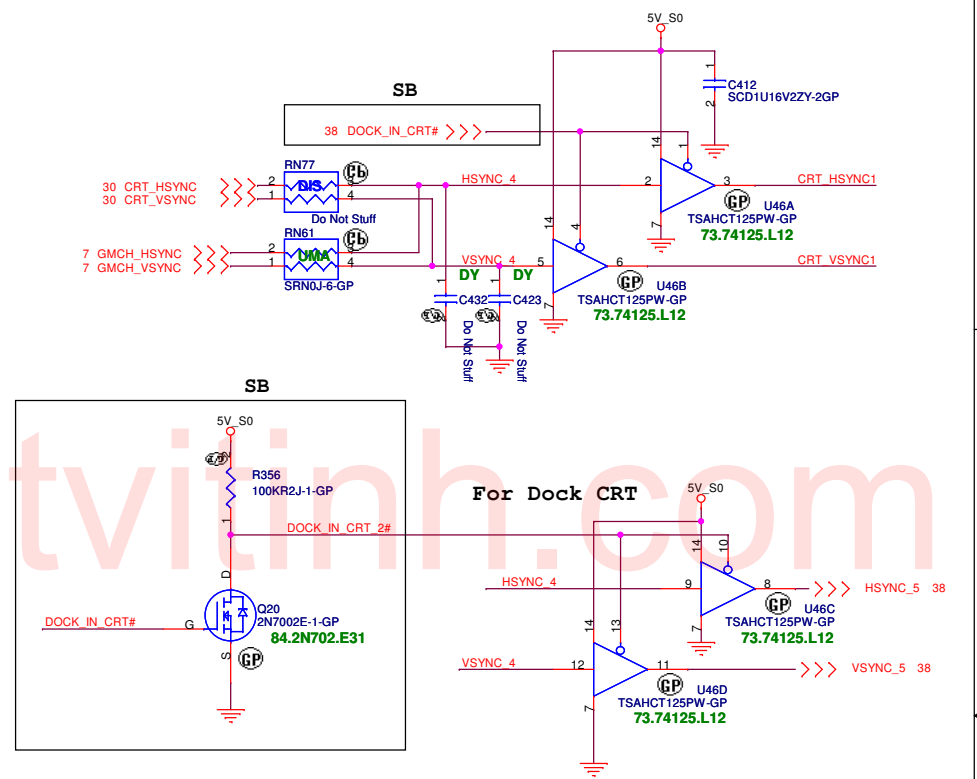


Ferrite bead impedance: 10 ohm@100MHz:

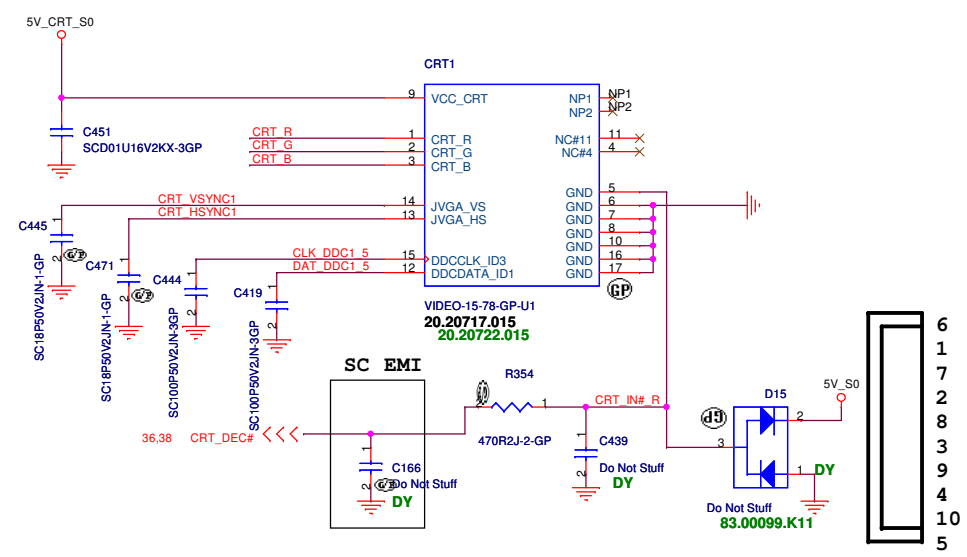


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

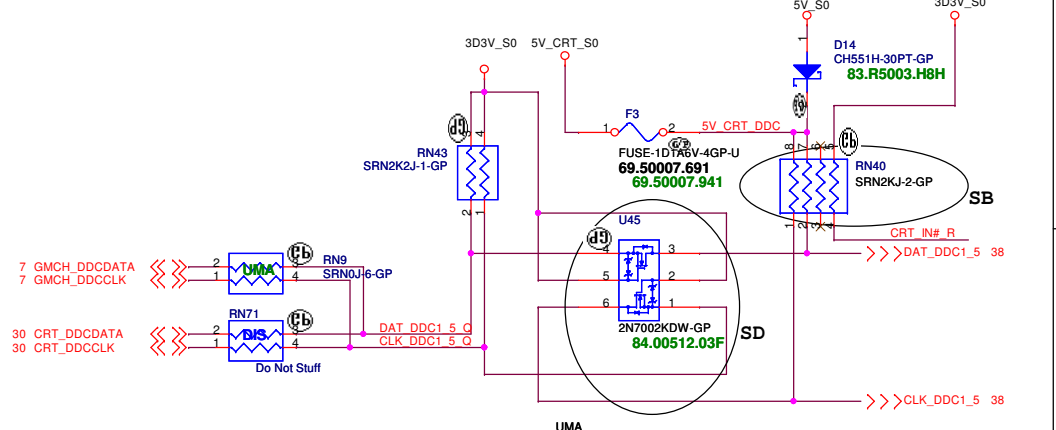
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



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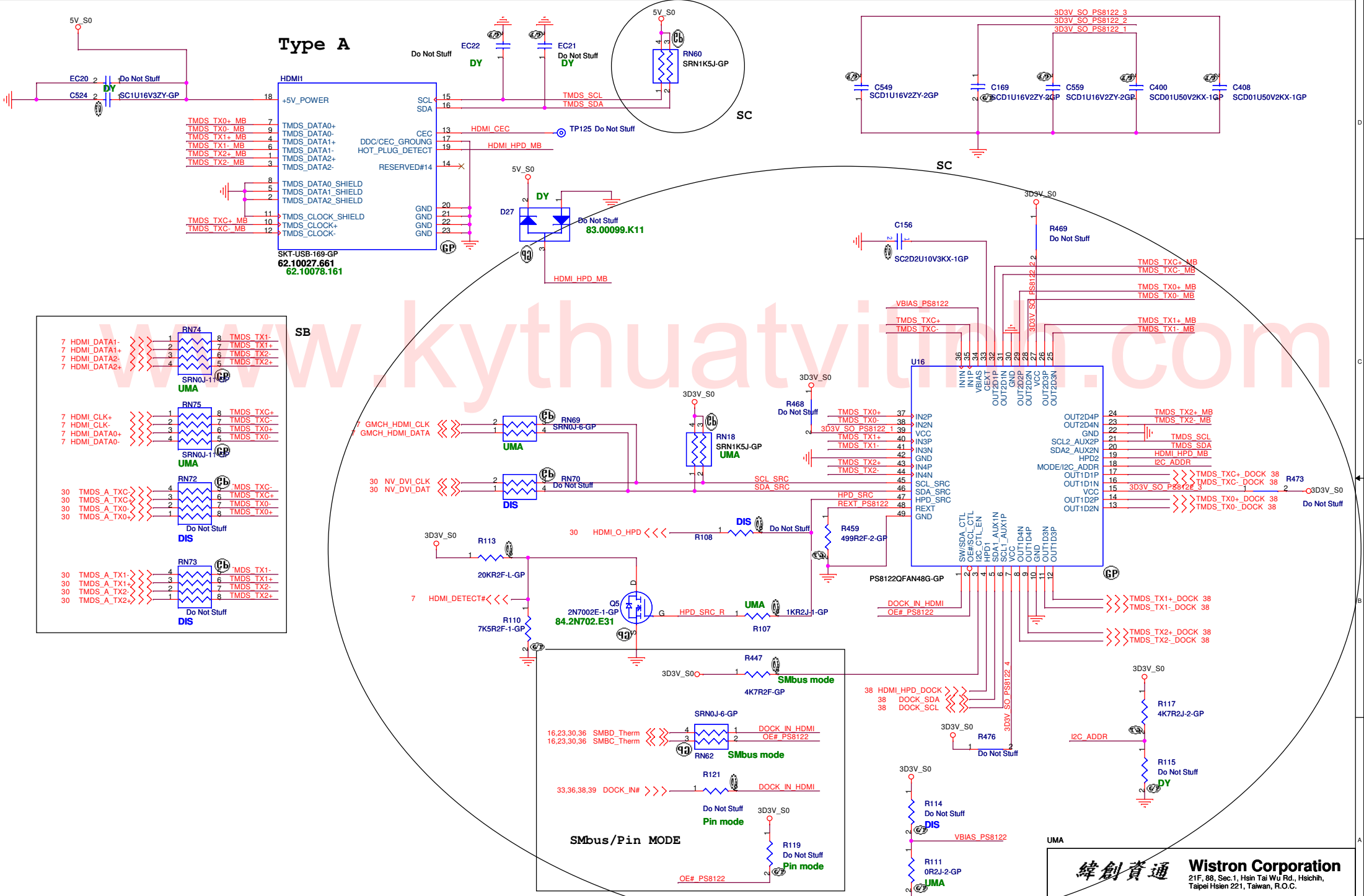
Title: **CRT Connector**

Size: Document Number

Date: Tuesday, April 01, 2008

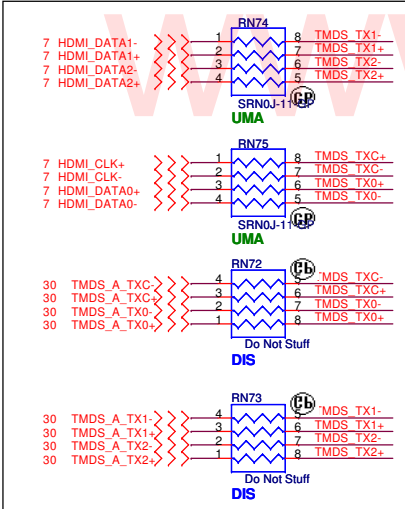
Sheet 17 of 50

Rev -1



Type A

SB



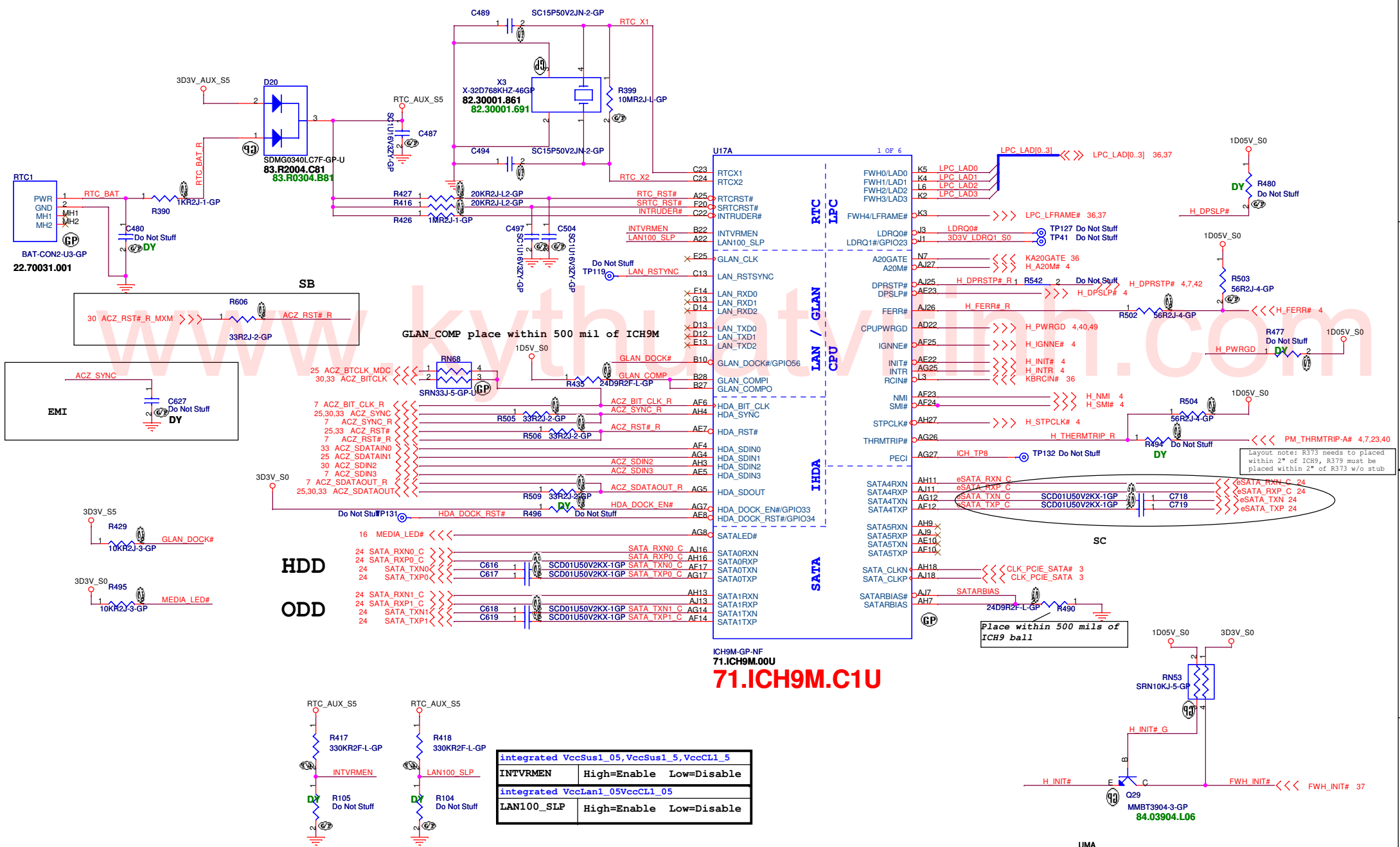
緯創資通 Wistron Corporation
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DVI CONNECTOR

File: **Eiger**

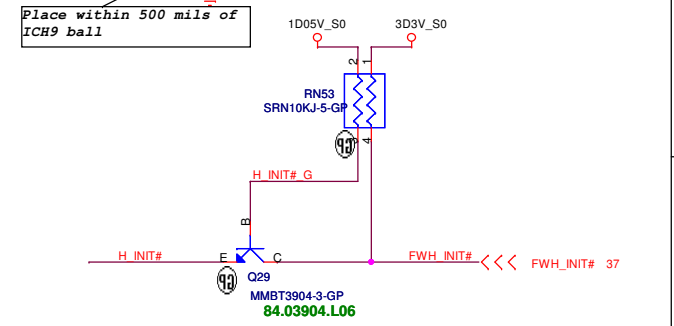
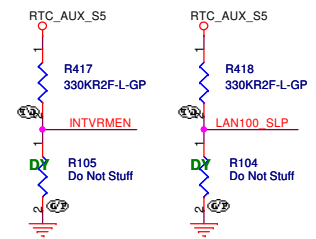
Size: A3 Document Number: **Eiger** Rev: **-1**

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**ICH9M-GP-NF
71.ICH9M.00U
71.ICH9M.C1U**

integrated VccSus1_05, VccSus1_5, VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



Layout note: R373 needs to be placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub

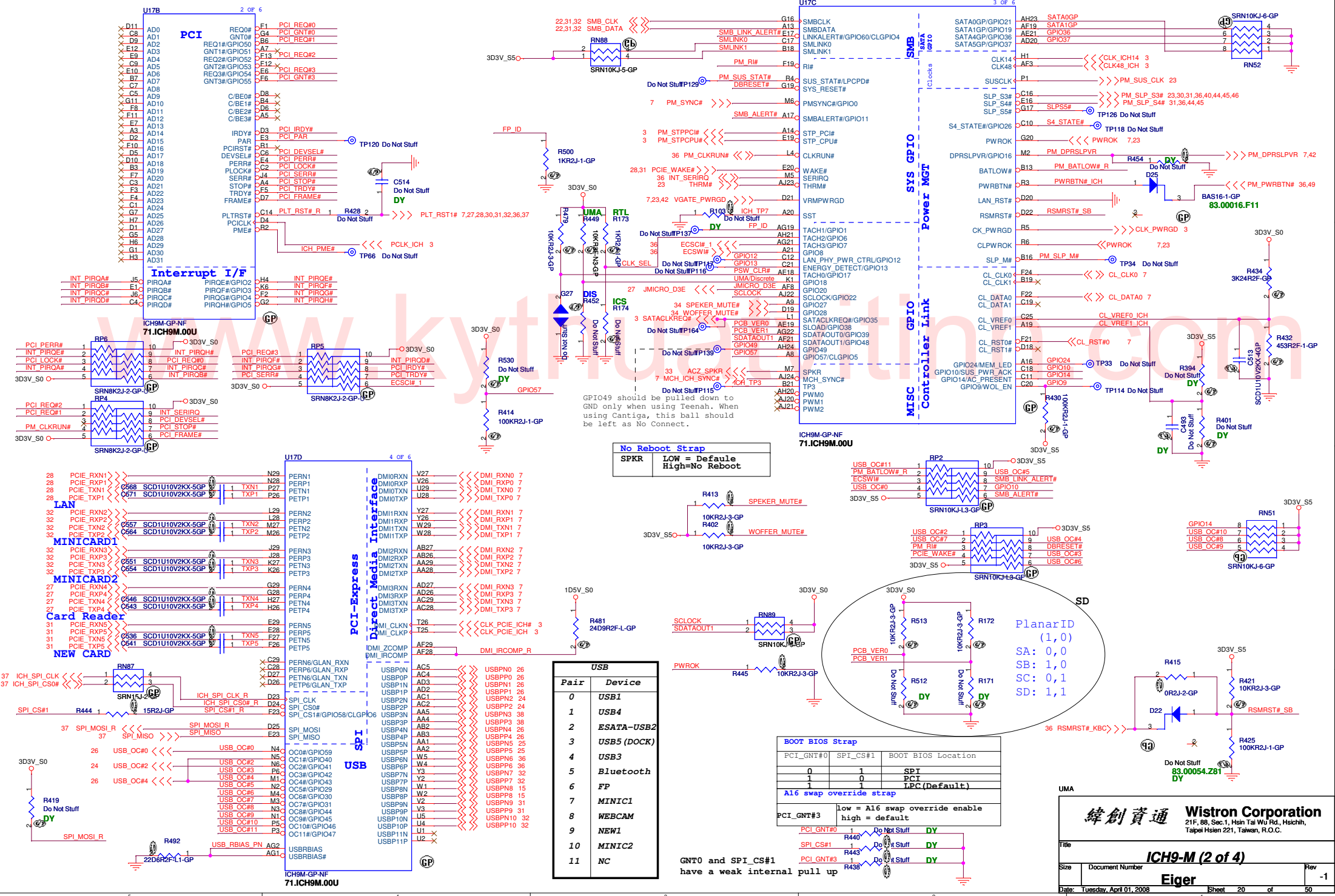
UMA

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Title: **ICH9-M (1 of 4)**

Size: Document Number: _____ Rev: **-1**

Date: Tuesday, April 01, 2008 Sheet 19 of 50



No Reboot Strap
 SPKR LOW = Default
 High = No Reboot

Pair	Device
0	USB1
1	USB4
2	ESATA-(DOCK)
3	USB3
4	Bluetooth
5	MINIC1
6	FP
7	MINIC2
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC (Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable	high = default
0	R440	Do Not Stuff
1	R443	Do Not Stuff
3	R438	Do Not Stuff

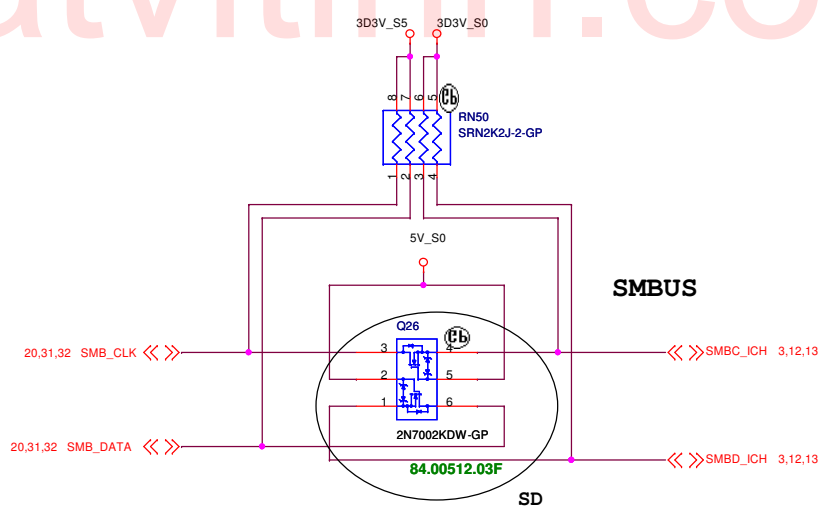
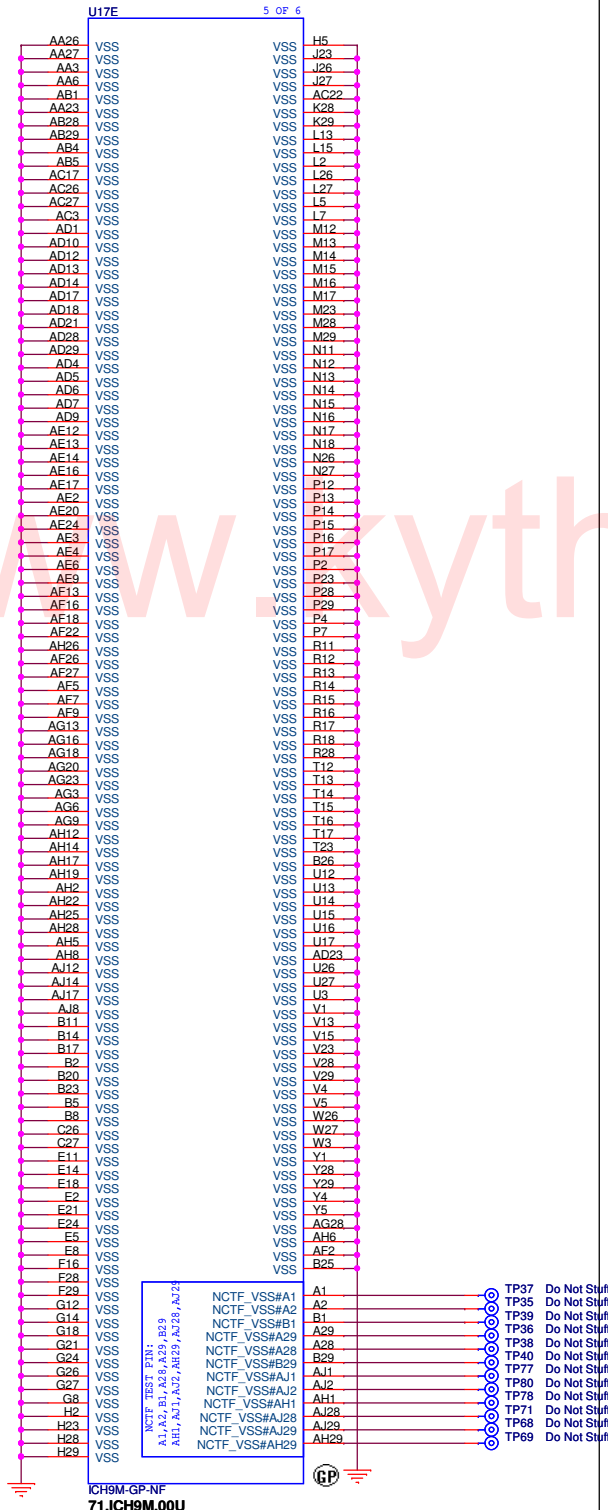
GNT0 and SPI_CS#1 have a weak internal pull up

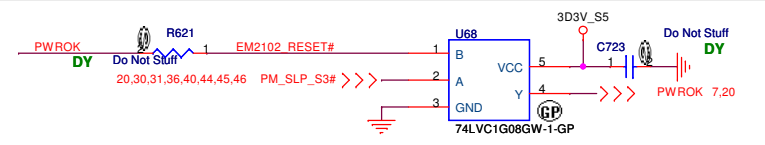
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (2 of 4)**
Eiger

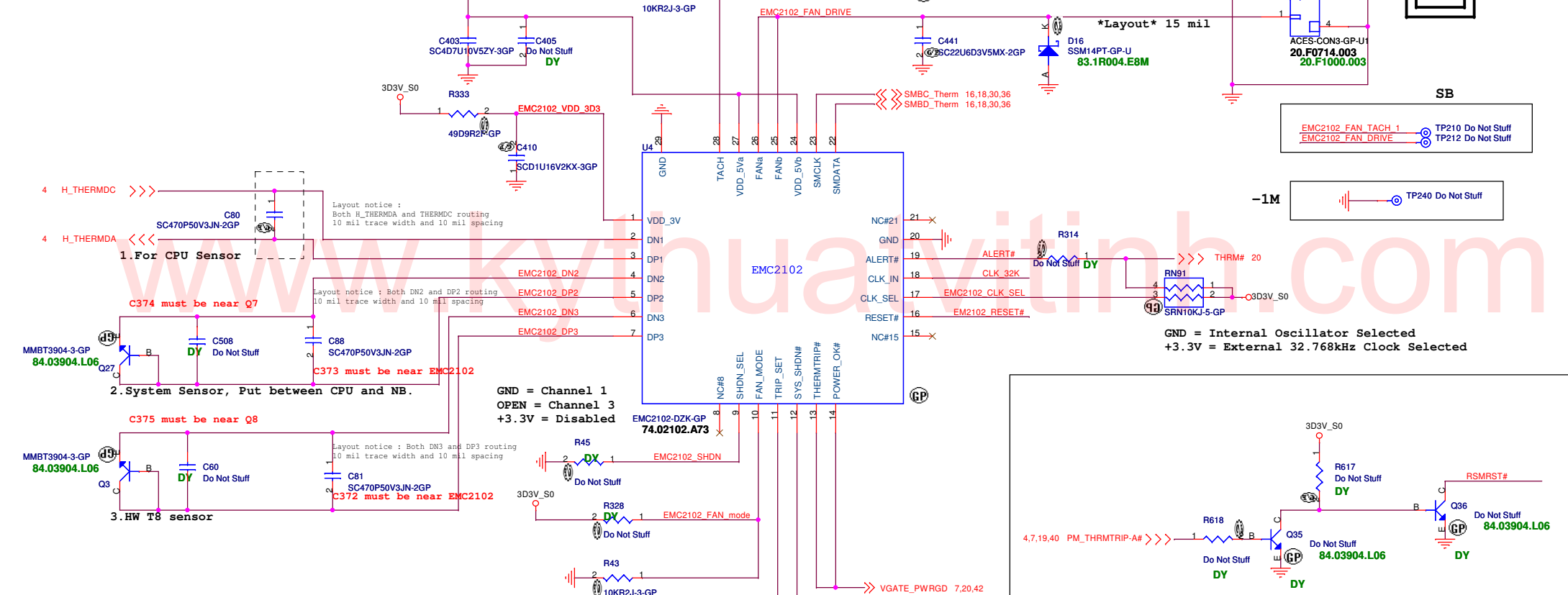
Size	Document Number	Rev
		-1

Date: Tuesday, April 01, 2008 Sheet 20 of 50





SC



SB

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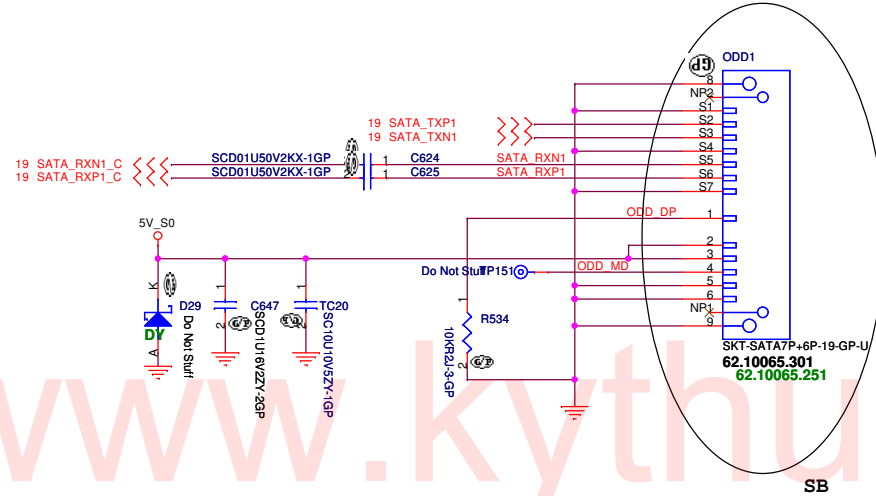
UMA

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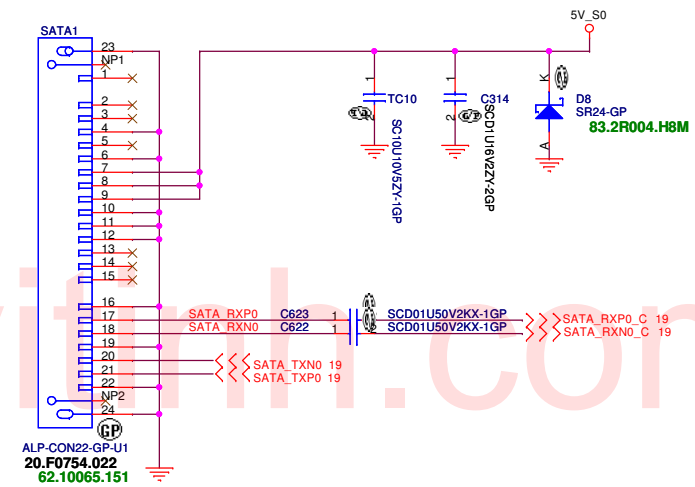
UMA

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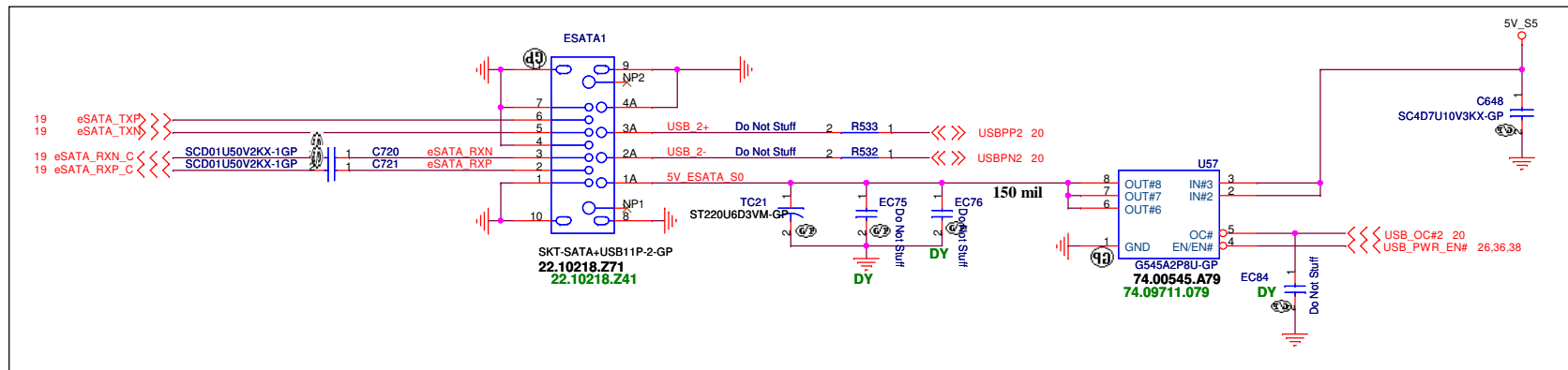
SATA ODD Connector



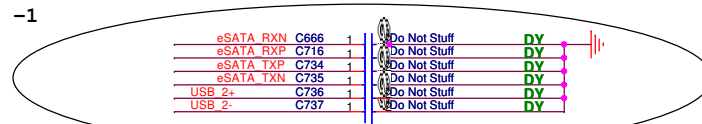
SATA Connector



SC



-1



EMI

UMA

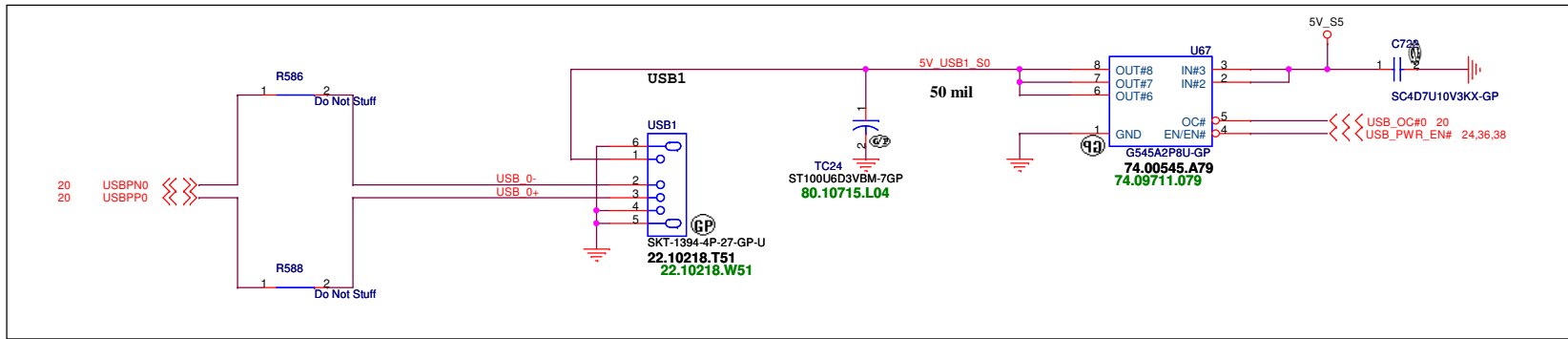
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD & CDROM & ESATA**

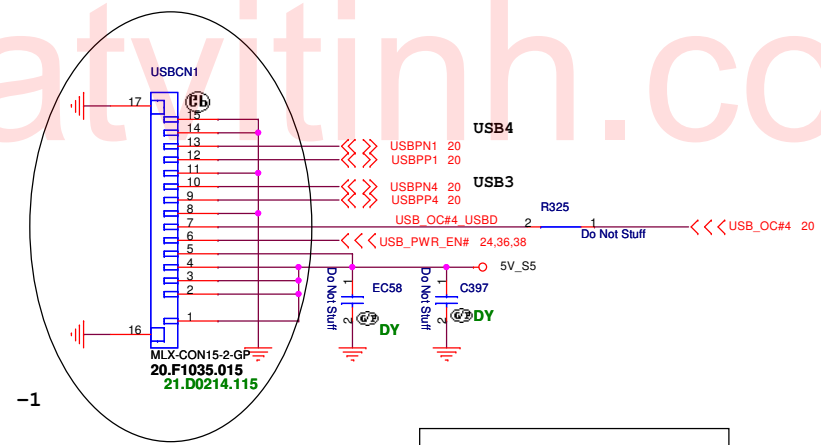
Size: Document Number: **Eiger** Rev: **-1**

Date: Tuesday, April 01, 2008 Sheet 24 of 50

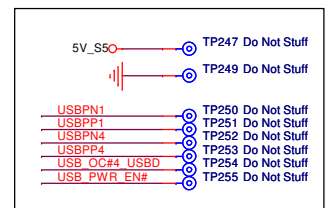
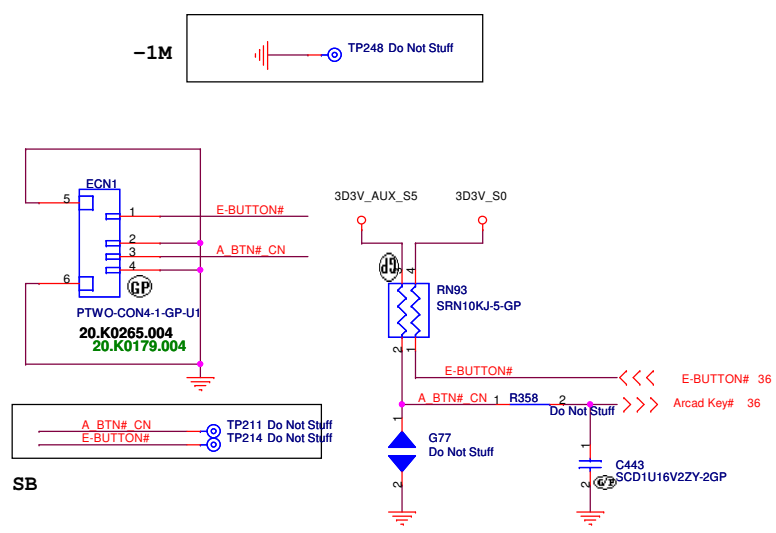
SC



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ECN BOARD



UMA

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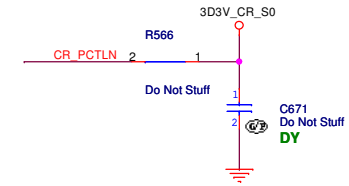
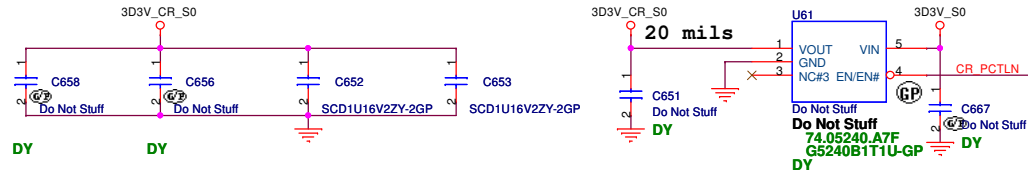
Title: **USB & ECN**

Size: Document Number: **Eiger** Rev: **-1**

Date: Tuesday, April 01, 2008 Sheet: 26 of 50

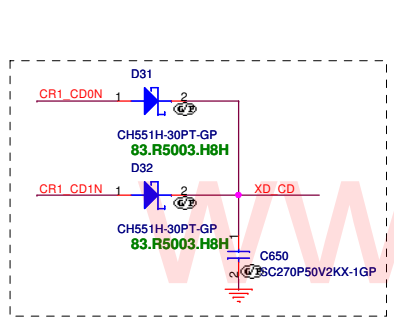
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

1.5A / High Active Voltage 2V

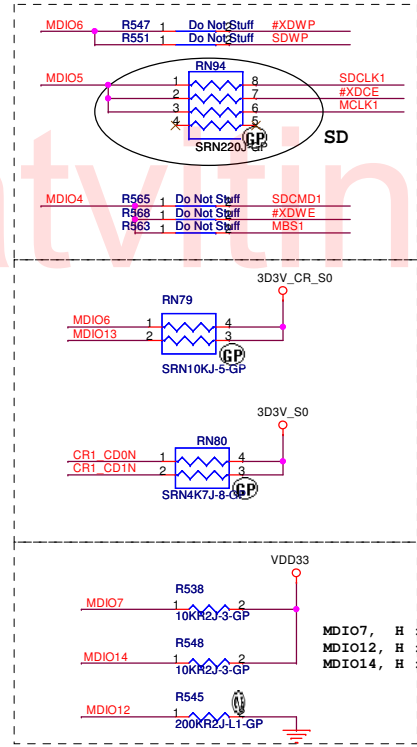
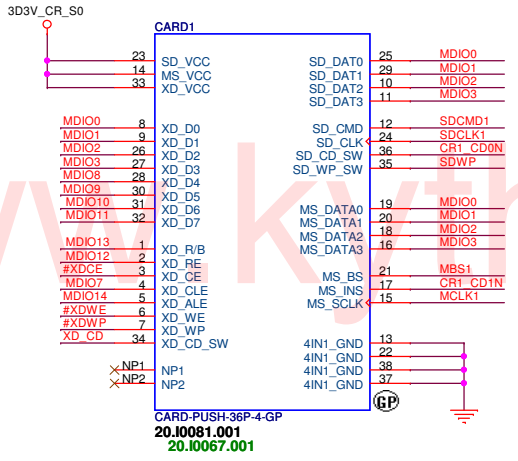


SC
EMI

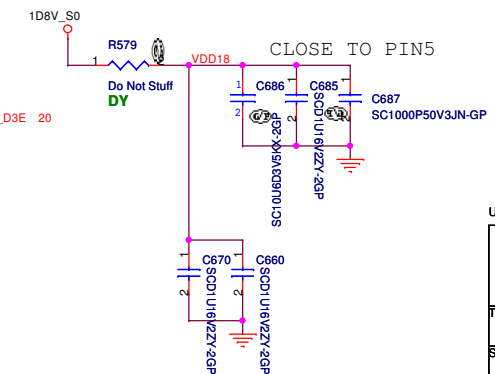
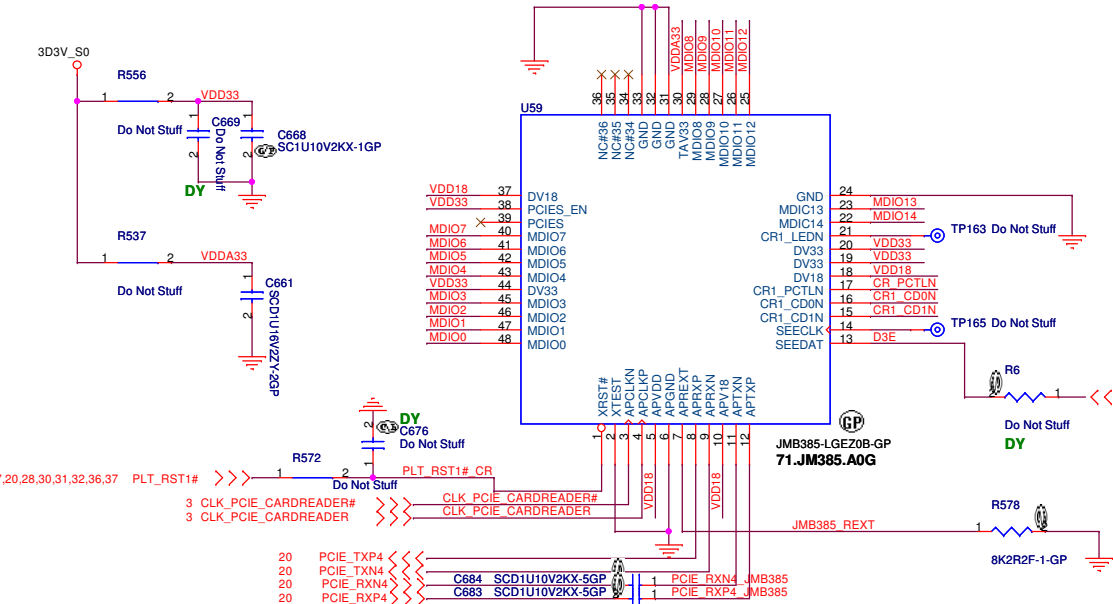
MDIO0	C555	1	2	Do Not Stuff	DY
MDIO1	C556	1	2	Do Not Stuff	DY
MDIO2	C597	1	2	Do Not Stuff	DY
MDIO3	C598	1	2	Do Not Stuff	DY
SDCMD1	C602	1	2	Do Not Stuff	DY
SDCLK1	C603	1	2	Do Not Stuff	DY
CR1_CD0N	C714	1	2	Do Not Stuff	DY
SDWP	C715	1	2	Do Not Stuff	DY



SD/XD/MS/MS PRO/MMC



MDIO7, H on-board, L : on Add-in card or Express card
MDIO12, H CR1_LEDN high active, L : CR1_LEDN low active
MDIO14, H CR1_PCTLN high active, L : CR1_PCTLN low active



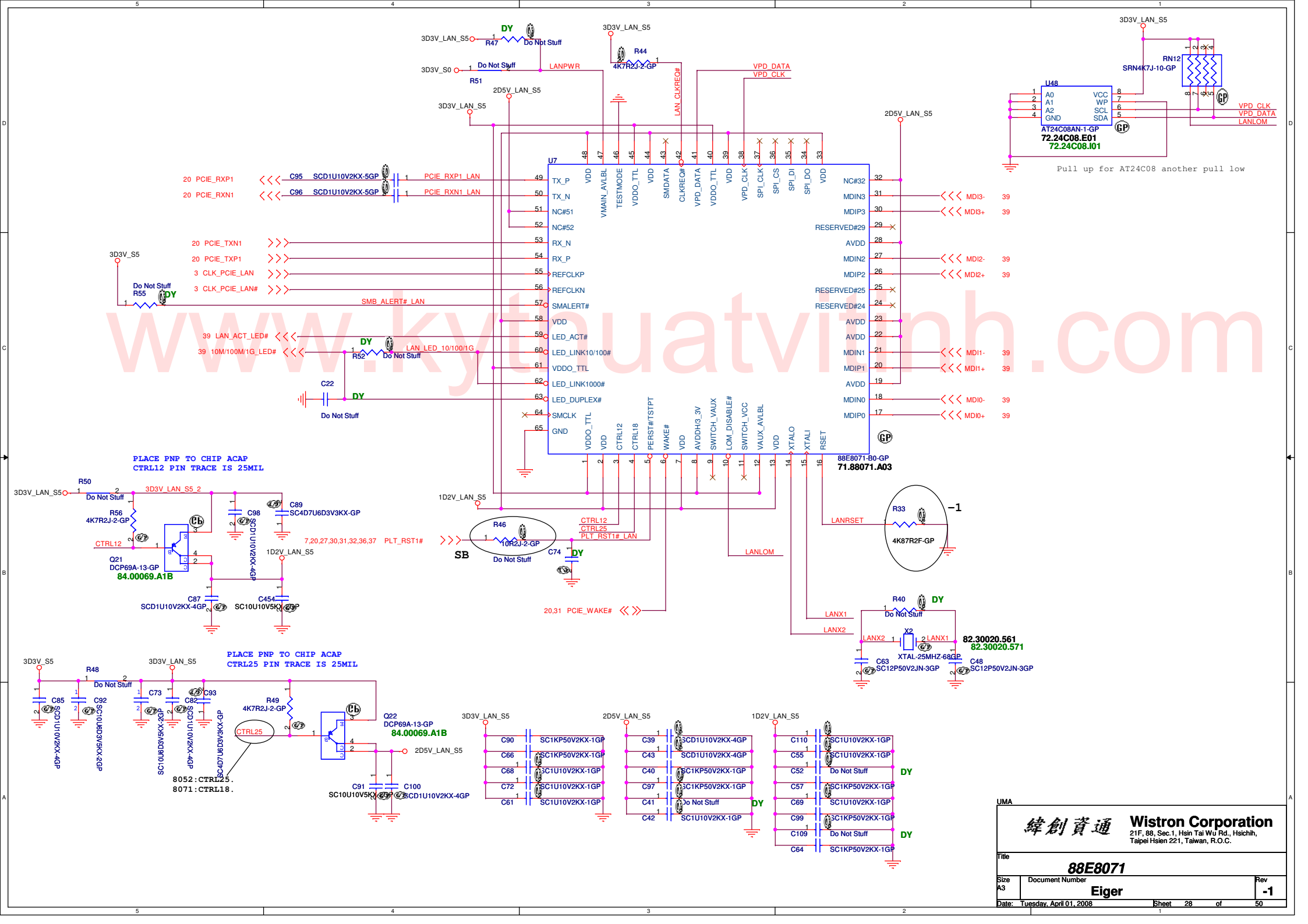
UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **JMB385 Card Reader**

Size: Document Number Rev: -1

Date: Tuesday, April 01, 2008 Sheet 27 of 50



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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

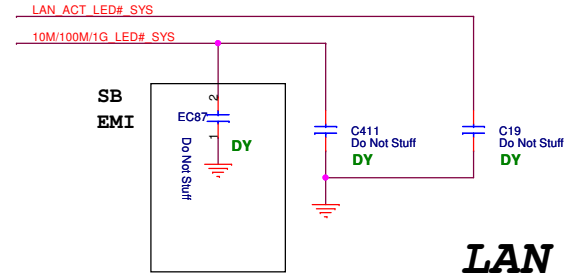
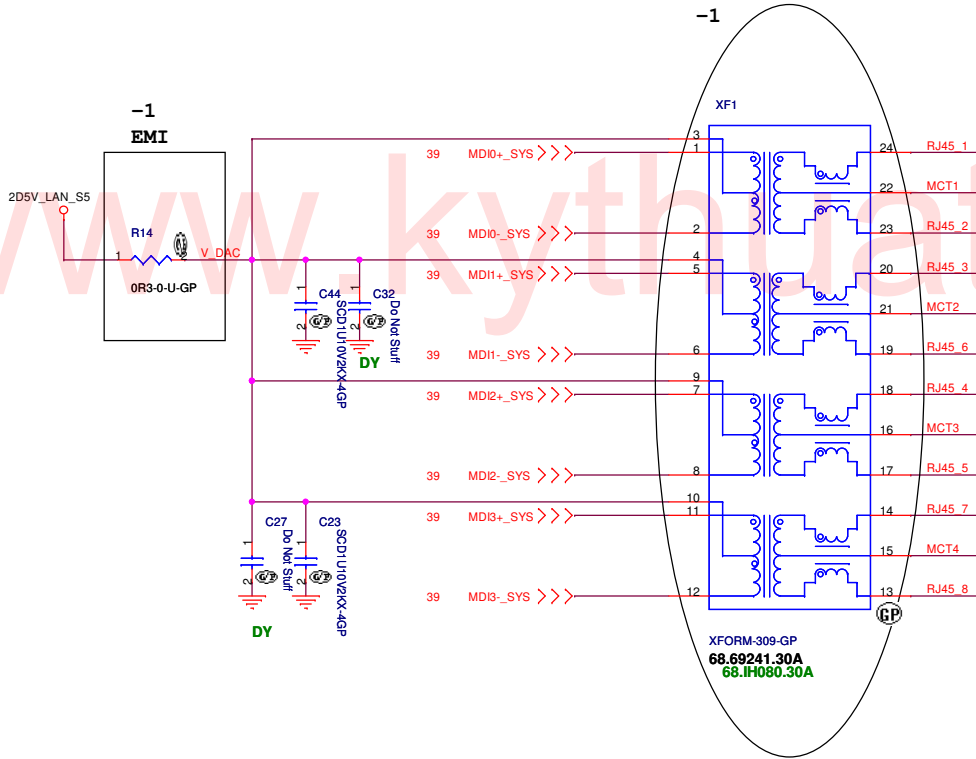
Title: **88E8071**

Size: A3 Document Number: **Eiger** Rev: **-1**

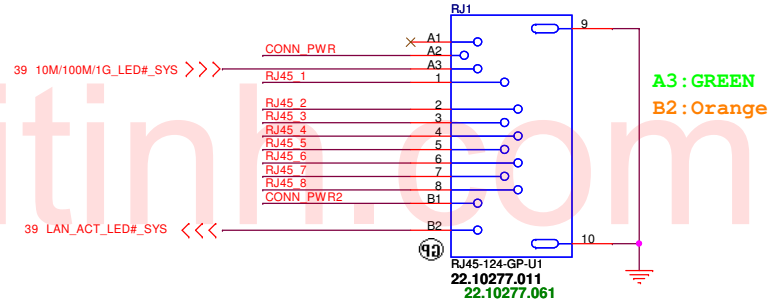
Date: Tuesday, April 01, 2008 Sheet 28 of 50

LAN Connector

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



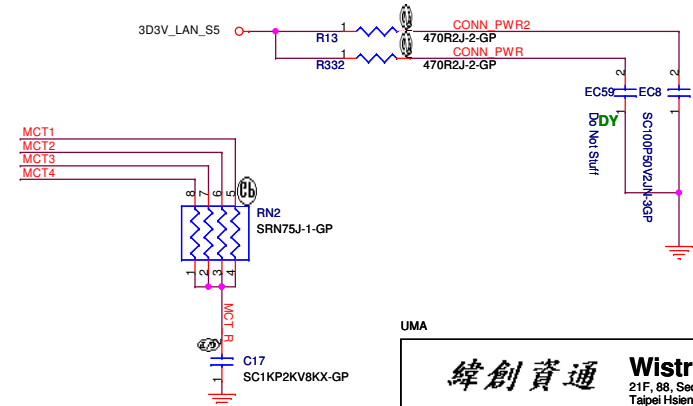
LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

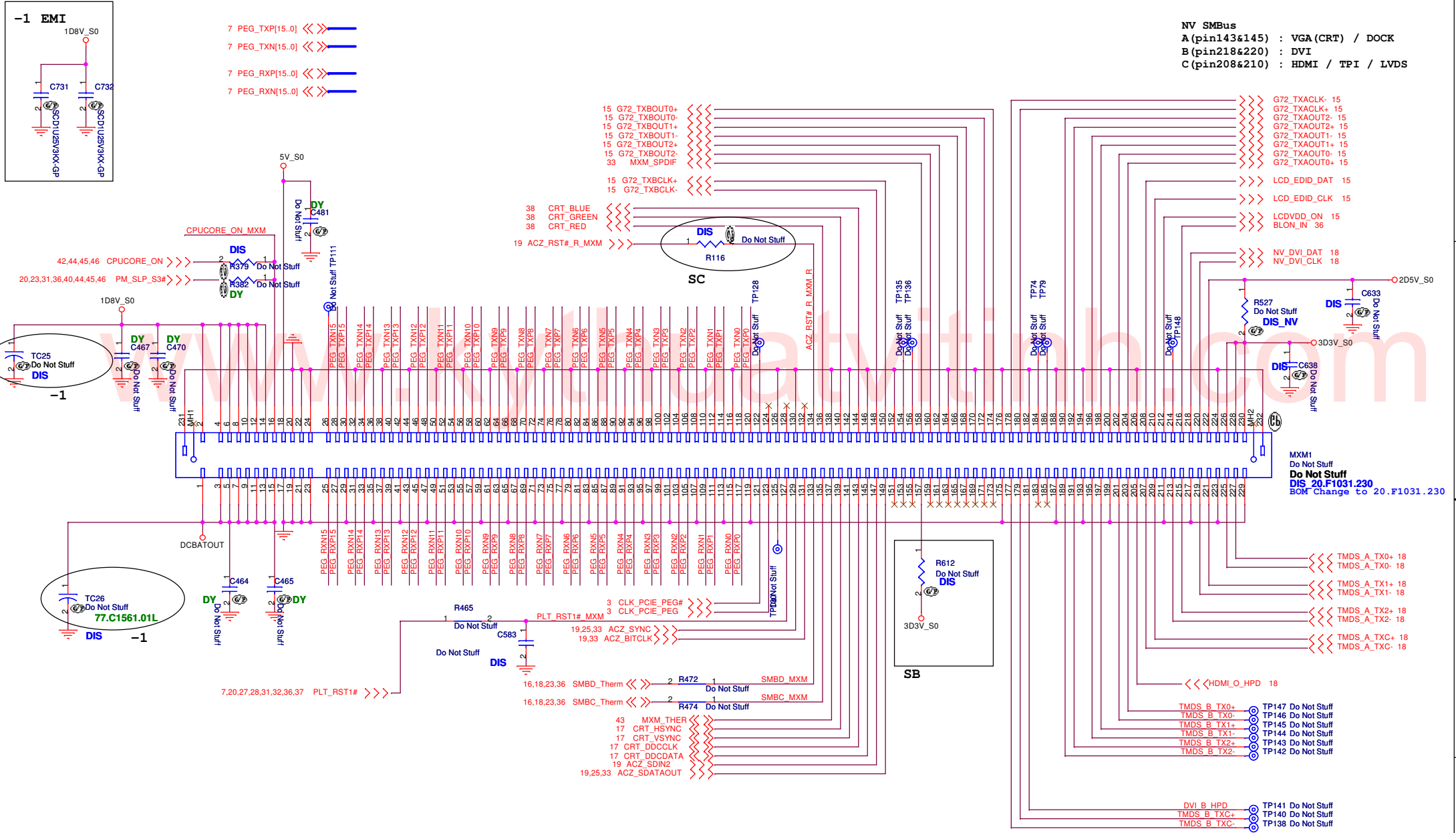
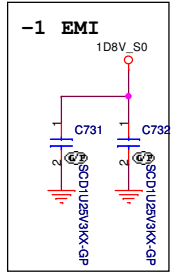


UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

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NV SMBus
 A(pin143&145) : VGA(CRT) / DOCK
 B(pin218&220) : DVI
 C(pin208&210) : HDMI / TPI / LVDS

G72_TXACLK- 15
 G72_TXACLK+ 15
 G72_TXAOUT2- 15
 G72_TXAOUT2+ 15
 G72_TXAOUT1- 15
 G72_TXAOUT1+ 15
 G72_TXAOUT0- 15
 G72_TXAOUT0+ 15
 LCD_EDID_DAT 15
 LCD_EDID_CLK 15
 LCDVDD_ON 15
 BLON_IN_36

NV_DVI_DAT 18
 NV_DVI_CLK 18
 2D5V_S0
 3D3V_S0

MXM1
 Do Not Stuff
DIS 20.F1031.230
 BOM Change to 20.F1031.230

TMDS_A_TX0+ 18
 TMDS_A_TX0- 18
 TMDS_A_TX1+ 18
 TMDS_A_TX1- 18
 TMDS_A_TX2+ 18
 TMDS_A_TX2- 18
 TMDS_A_TXC+ 18
 TMDS_A_TXC- 18

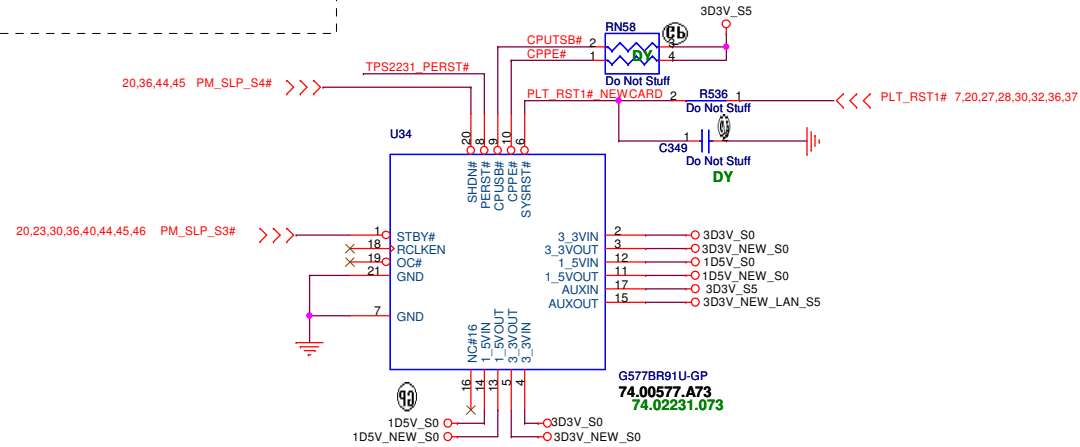
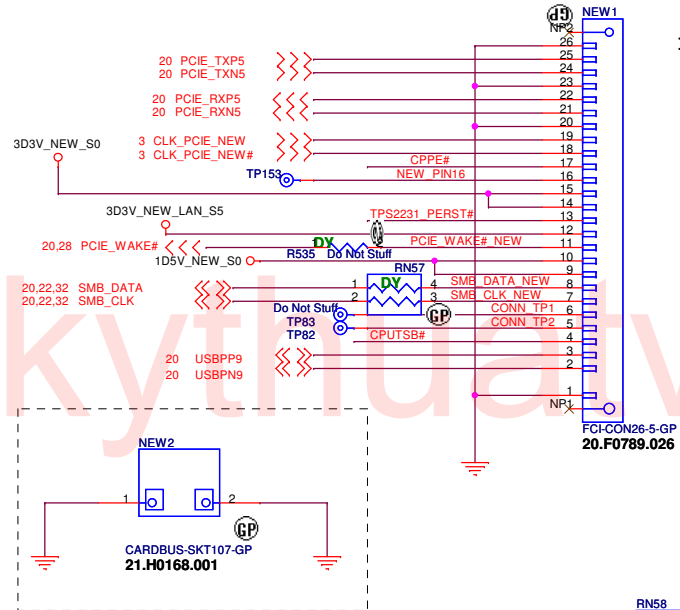
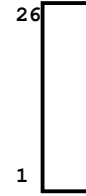
TP147 Do Not Stuff
 TP146 Do Not Stuff
 TP145 Do Not Stuff
 TP144 Do Not Stuff
 TMDS_B_TX1+
 TMDS_B_TX1-
 TP143 Do Not Stuff
 TMDS_B_TX2+
 TMDS_B_TX2-
 TP142 Do Not Stuff

DVI B HPD
 TP141 Do Not Stuff
 TMDS_B_TXC+
 TP140 Do Not Stuff
 TMDS_B_TXC-
 TP138 Do Not Stuff

NEWCARD Connector

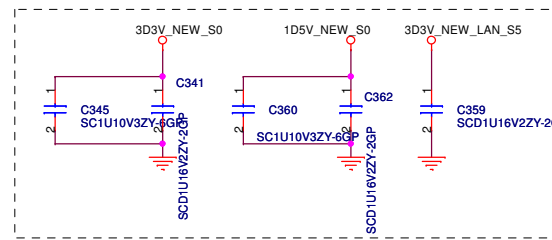
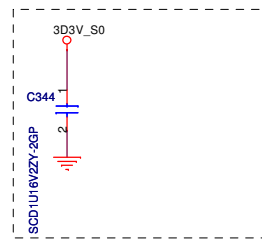
Reserve the symbol for bottom side connector

TOP VIEW



Place them Near to Chip

Place them Near to Connector



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Title: **NEW CARD**

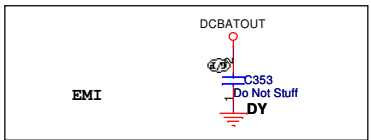
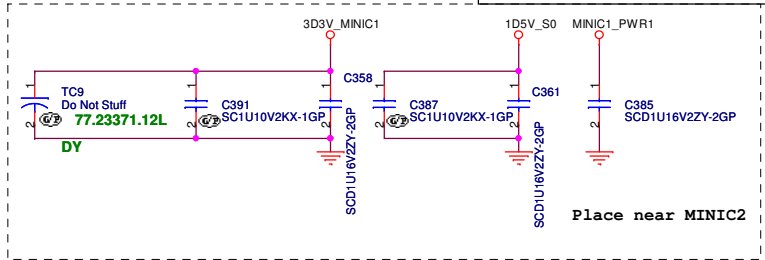
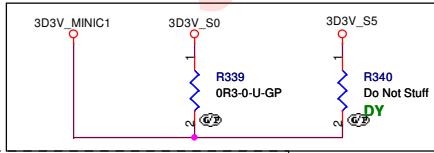
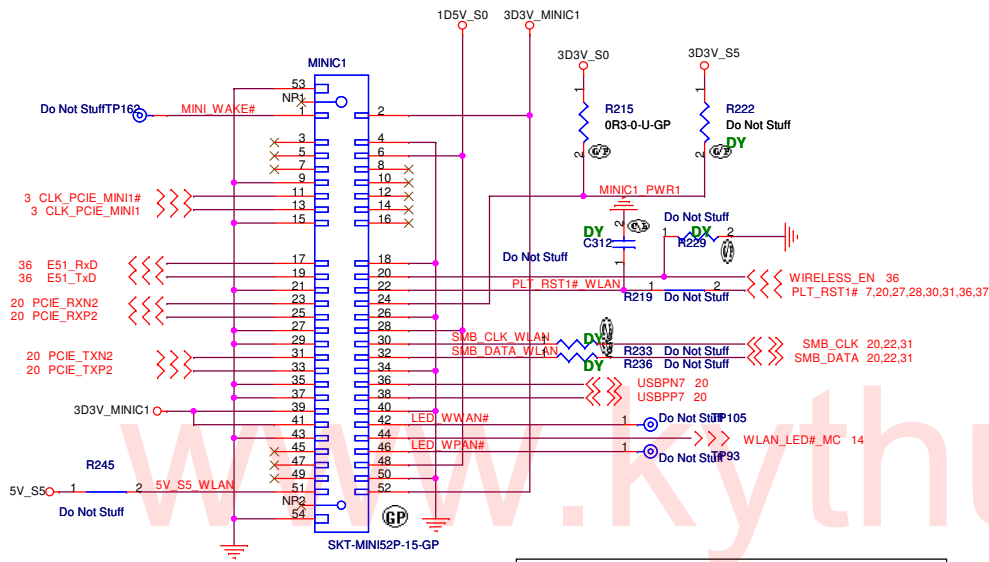
Size: Document Number

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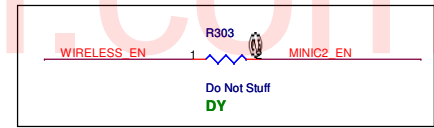
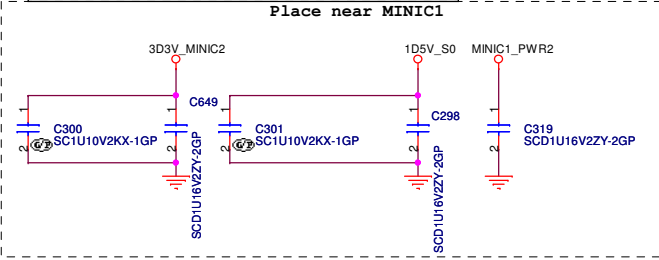
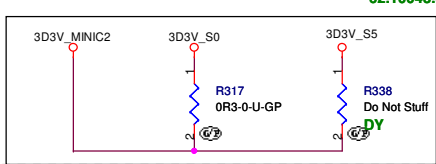
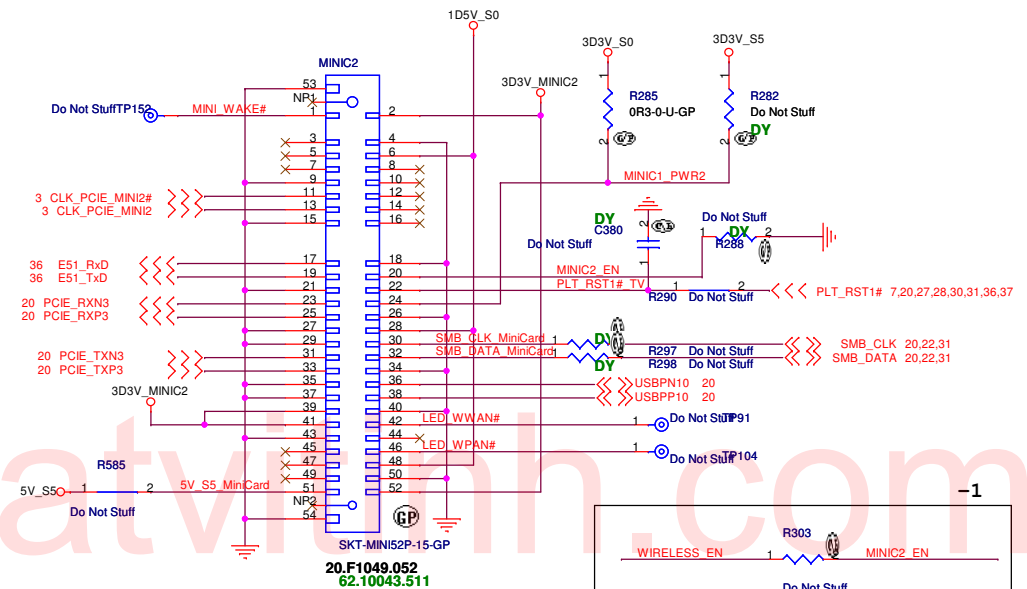
Eiger

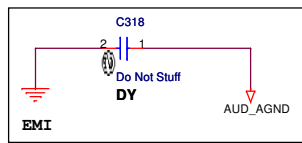
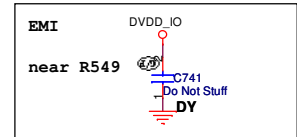
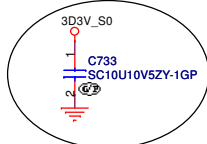
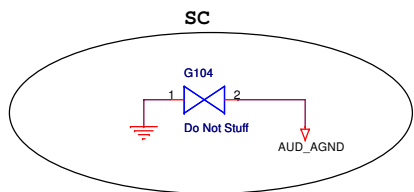
Rev -1

Mini Card Connector(WLAN)



Mini Card Connector(TV)

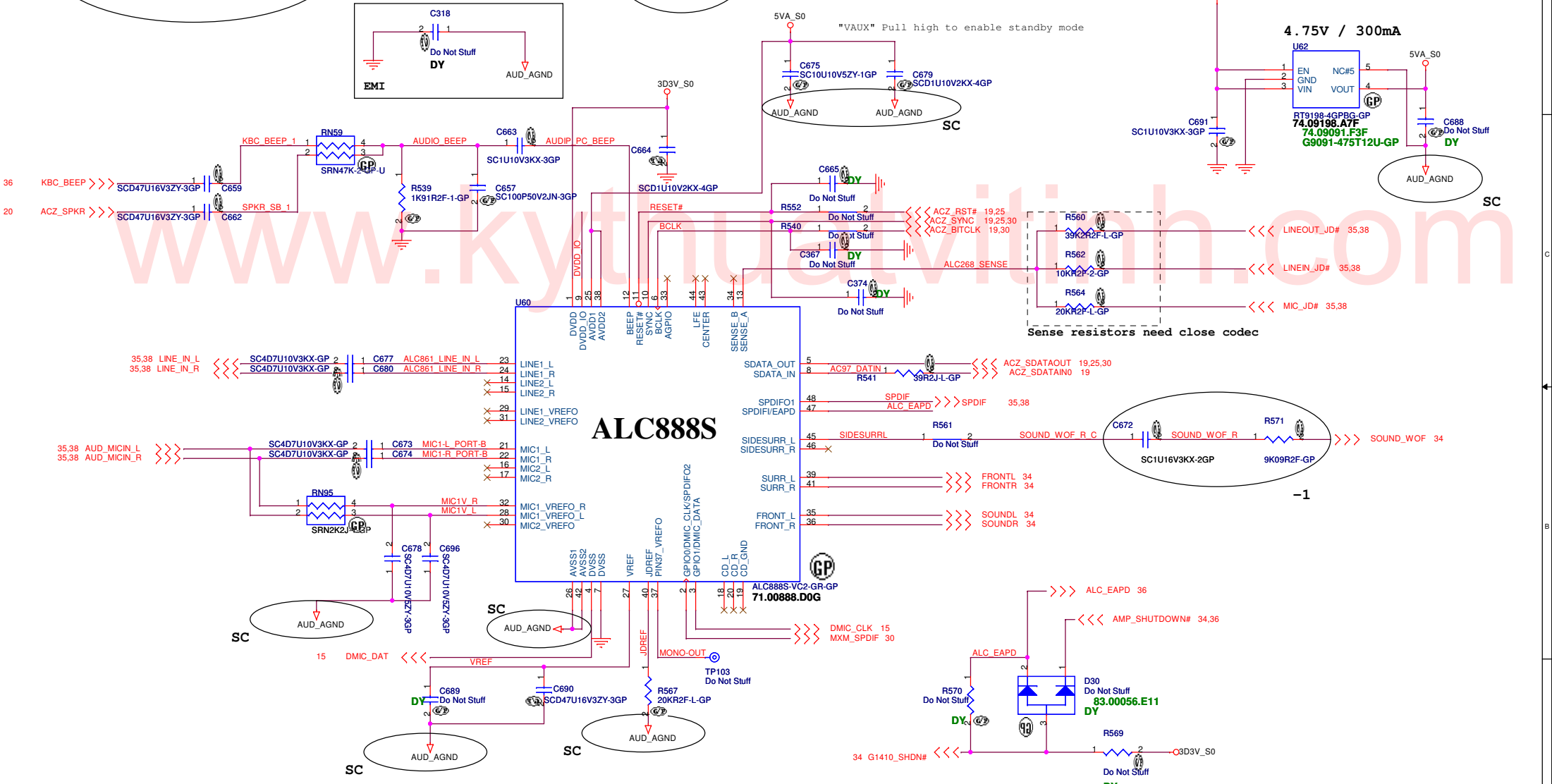
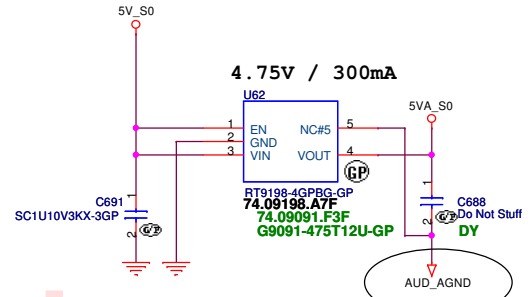




-1

"VAUX" Pull high to enable standby mode

4.75V / 300mA



ALC888S

ALC888S-VC2-GR-GP
71.00888.D0G

Sense resistors need close codec

-1



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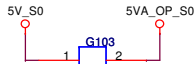
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC268**

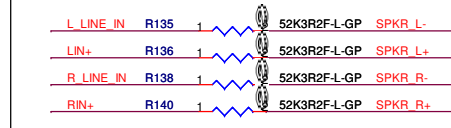
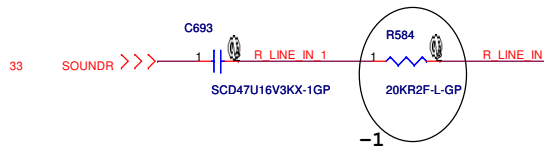
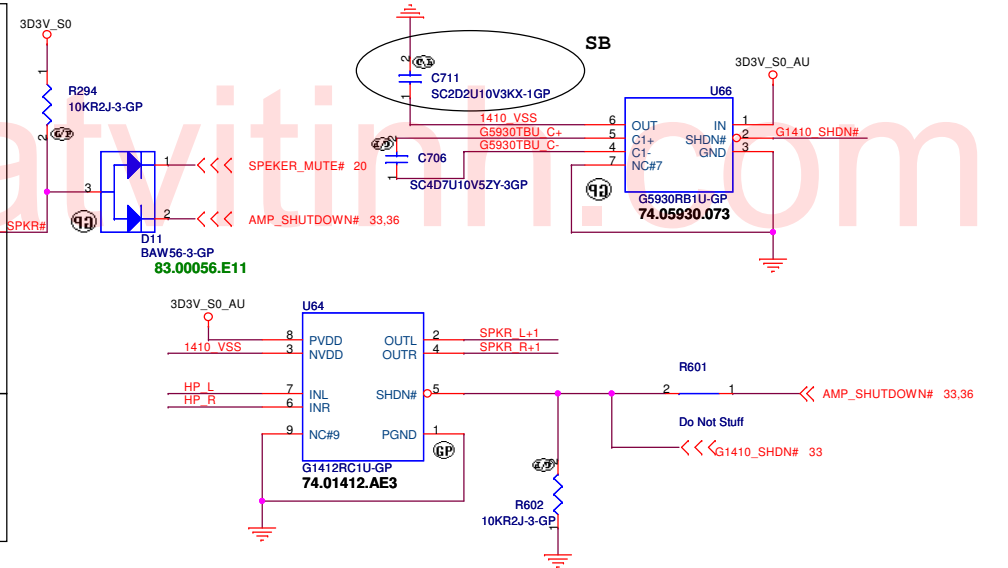
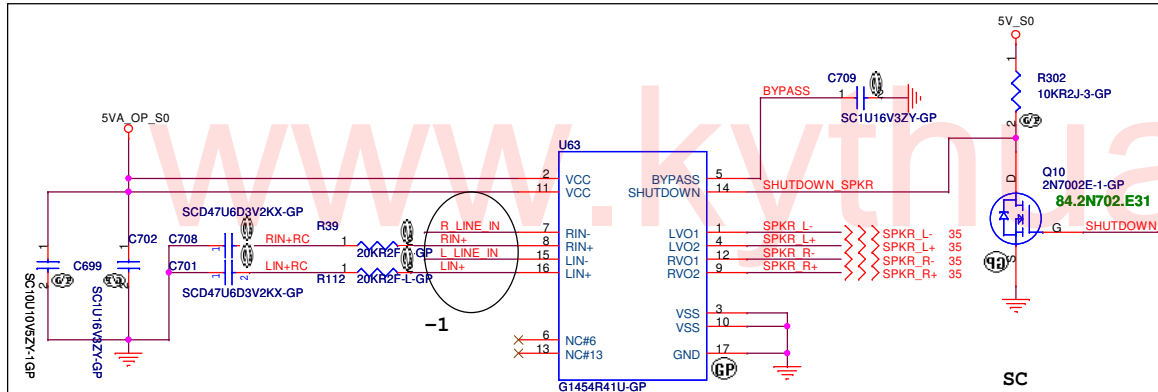
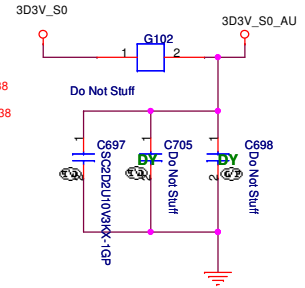
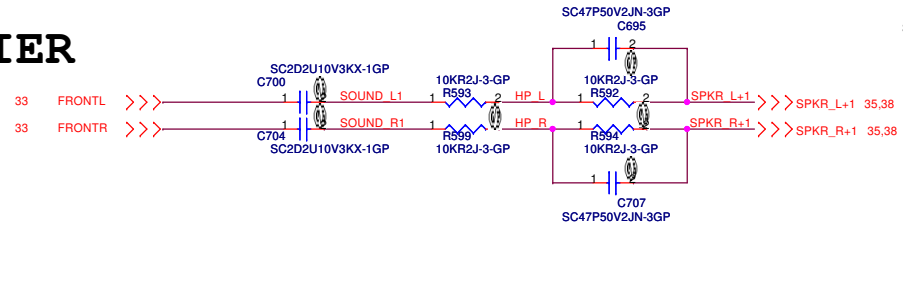
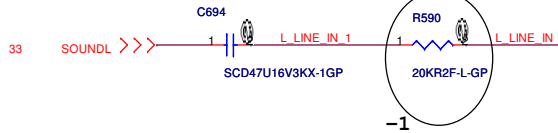
Size A3	Document Number	Rev -1
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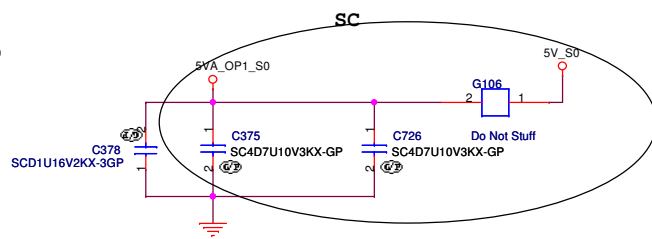
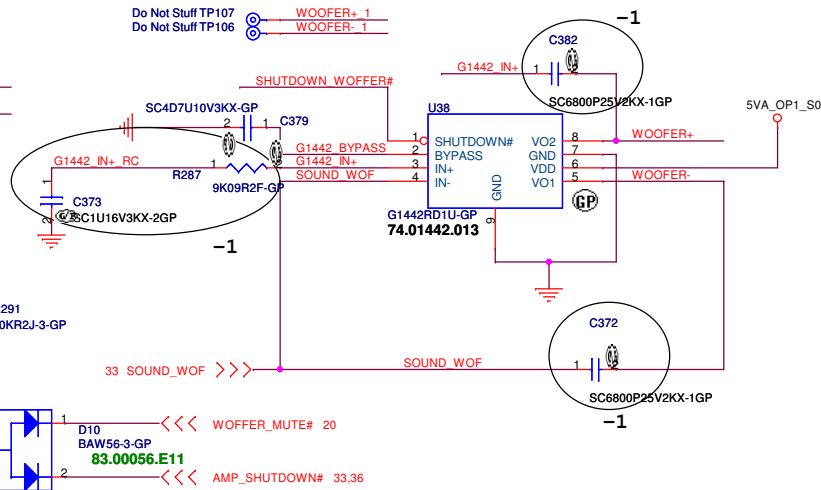
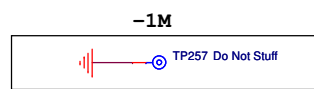
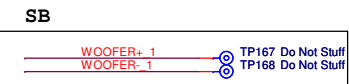
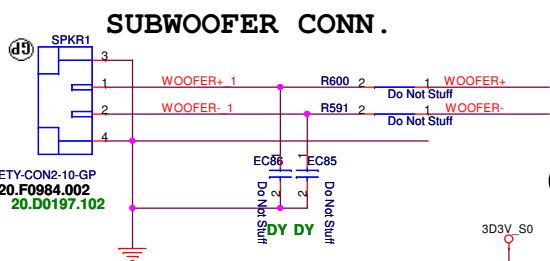
AUDIO OP AMPLIFIER



Do Not Stuff



SUBWOOFER CONN.



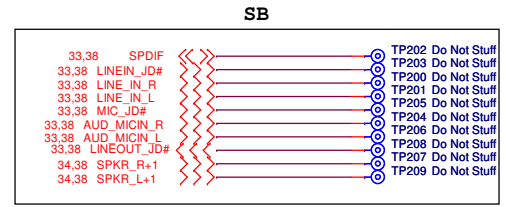
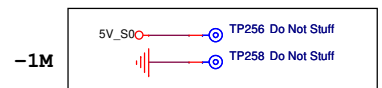
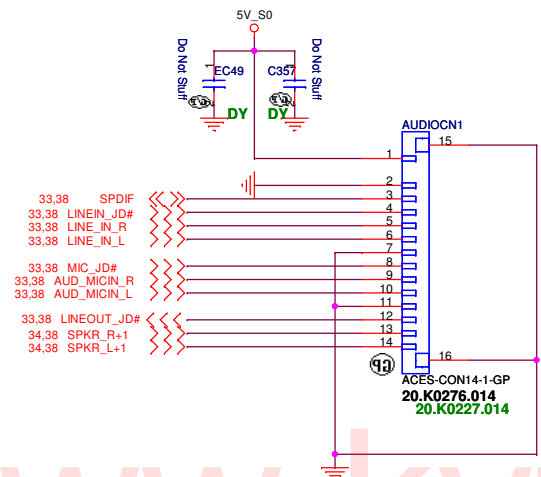
UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP AND JACK**

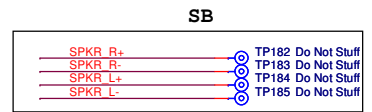
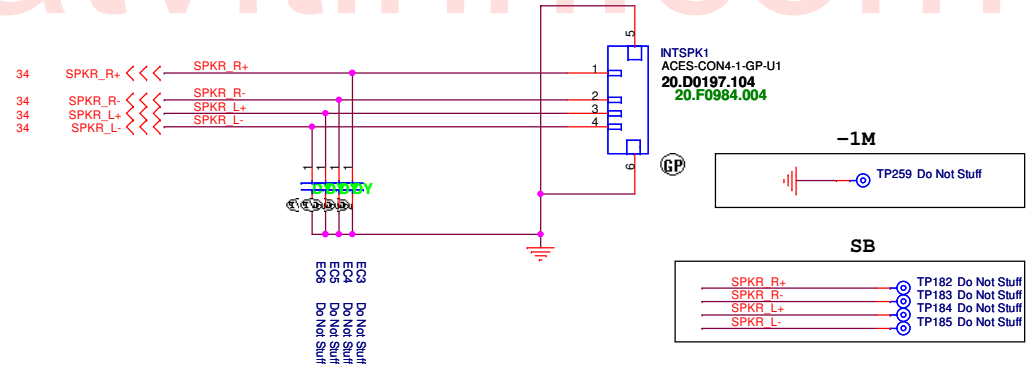
Size: Document Number: **Eiger** Rev: **-1**

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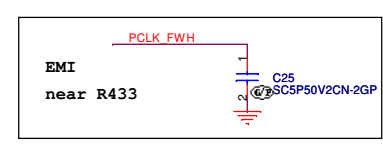
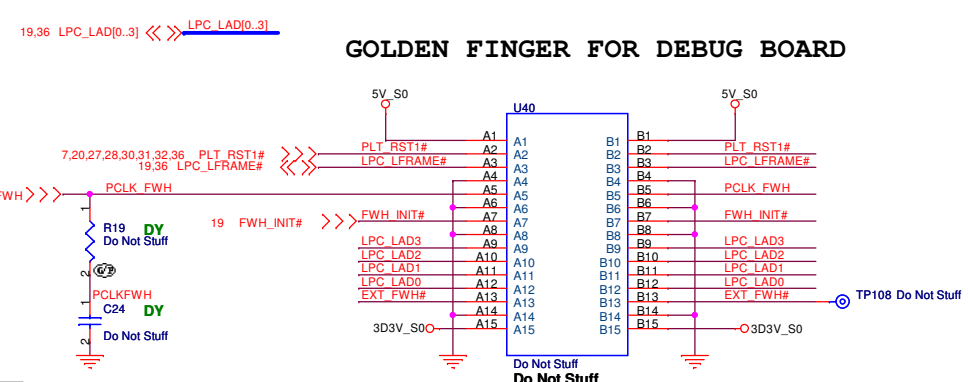
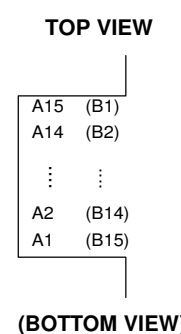
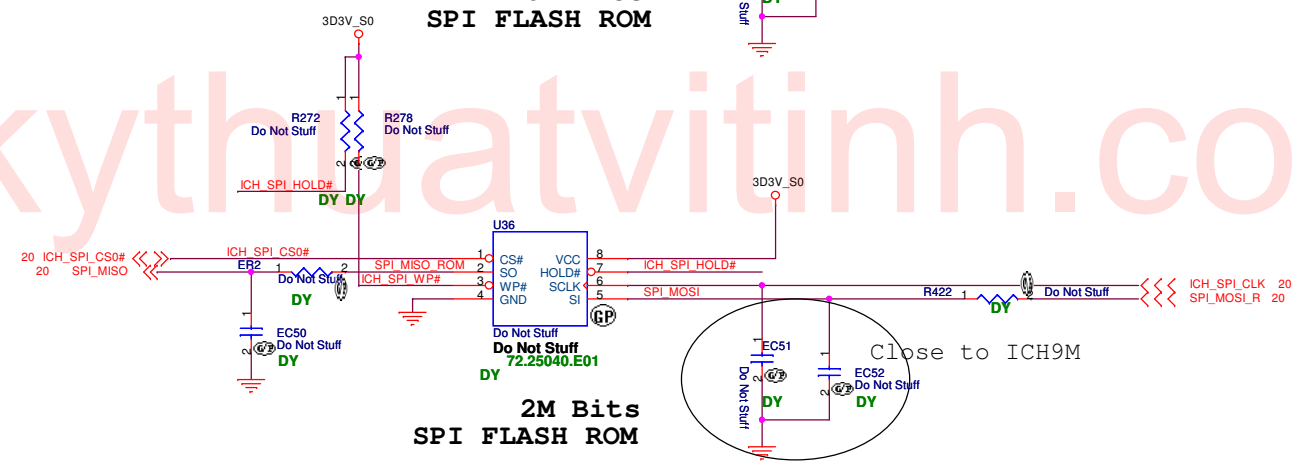
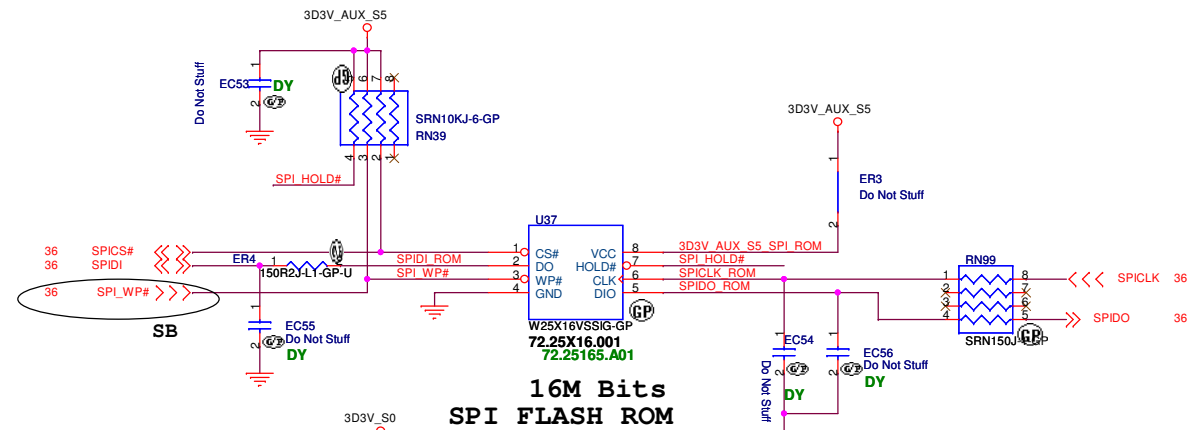


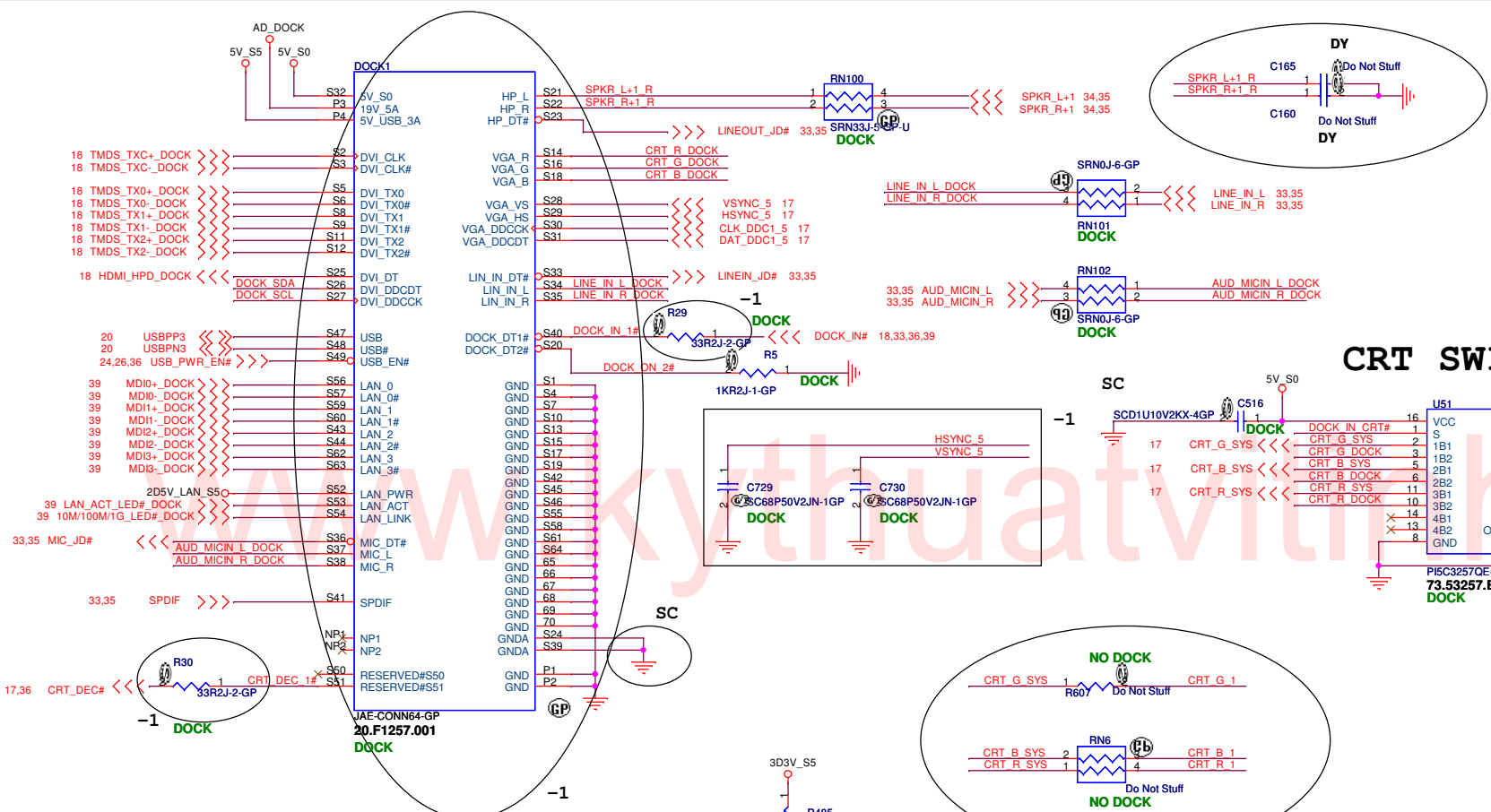
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Internal Speaker



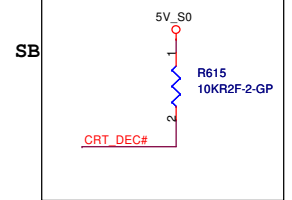
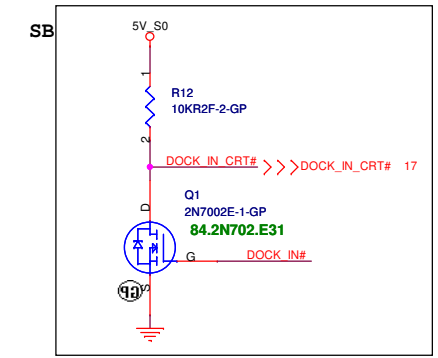
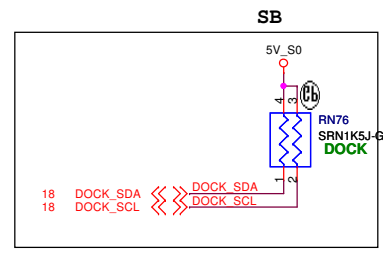
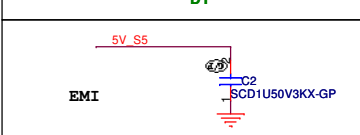
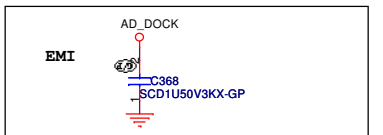
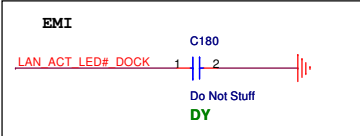
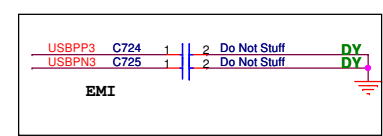
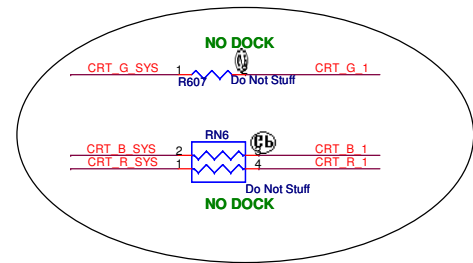
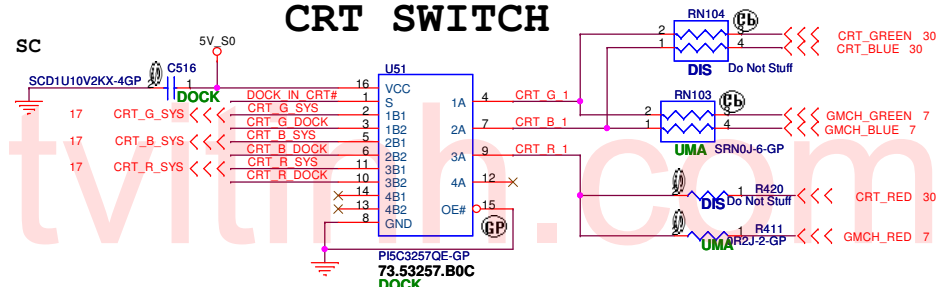
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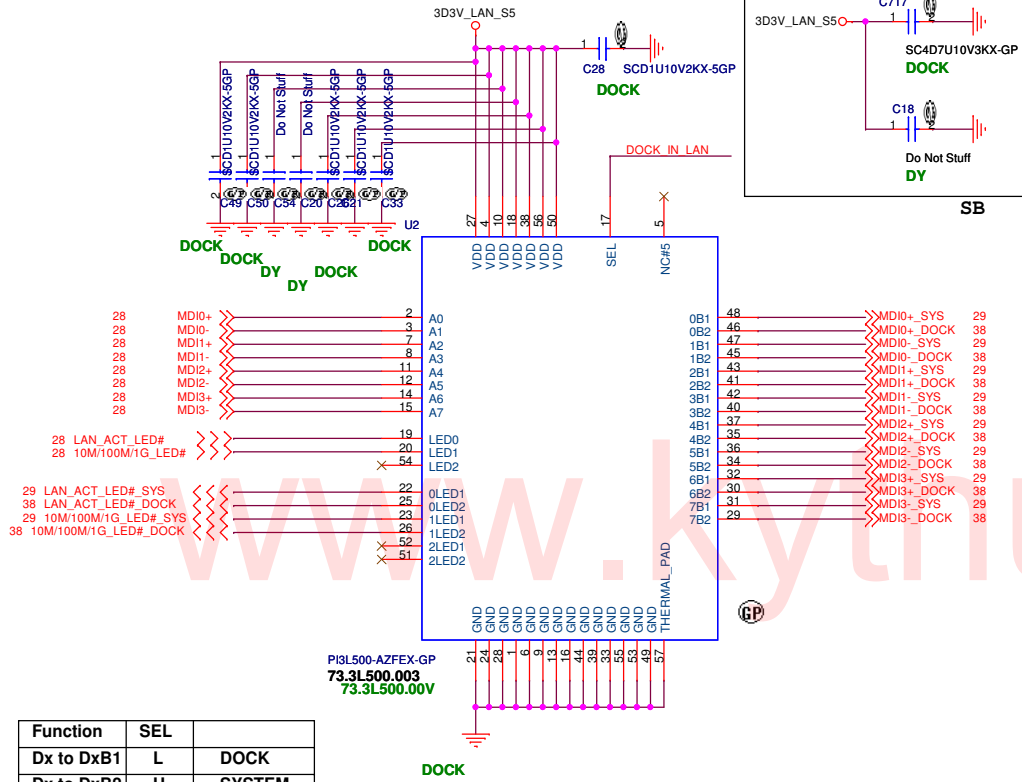


Function	SEL	SYSTEM
A to 1	L	SYSTEM
A to 2	H	DOCK

CRT SWITCH



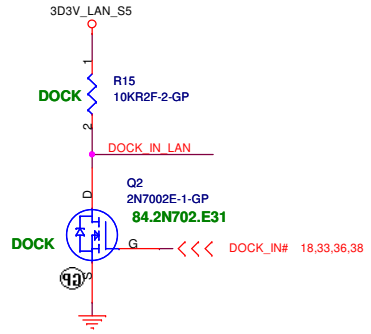
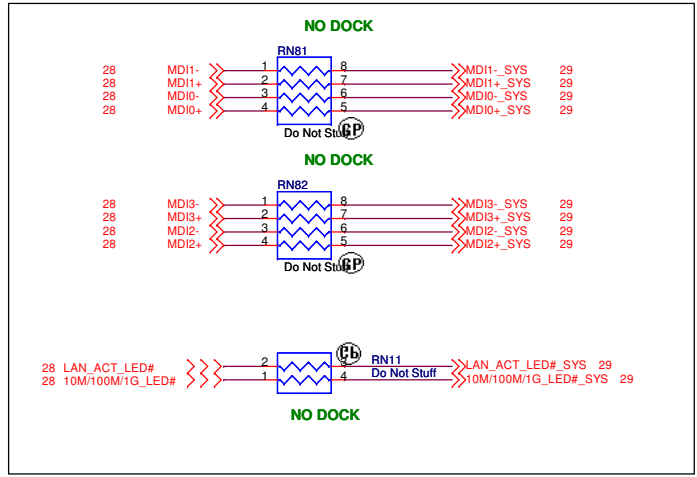
LAN switch

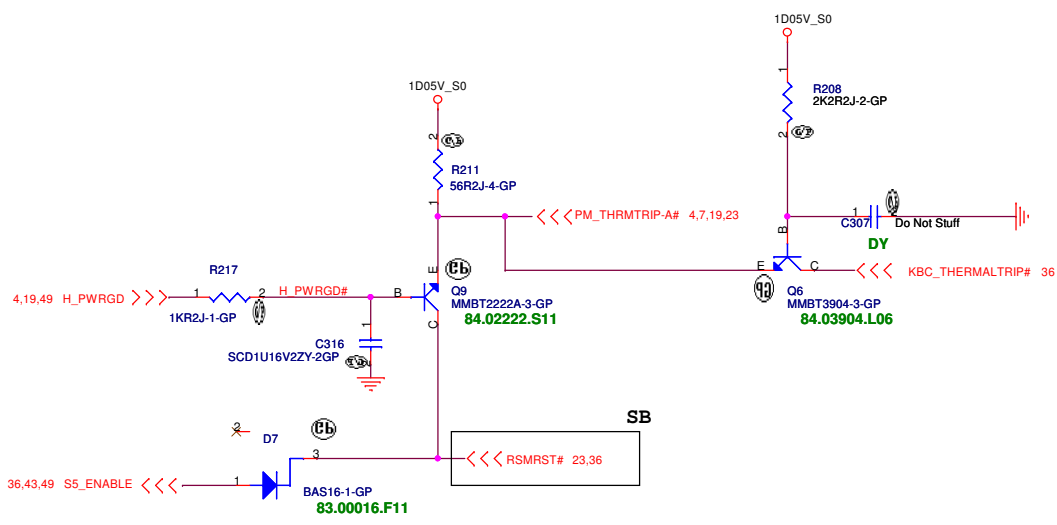
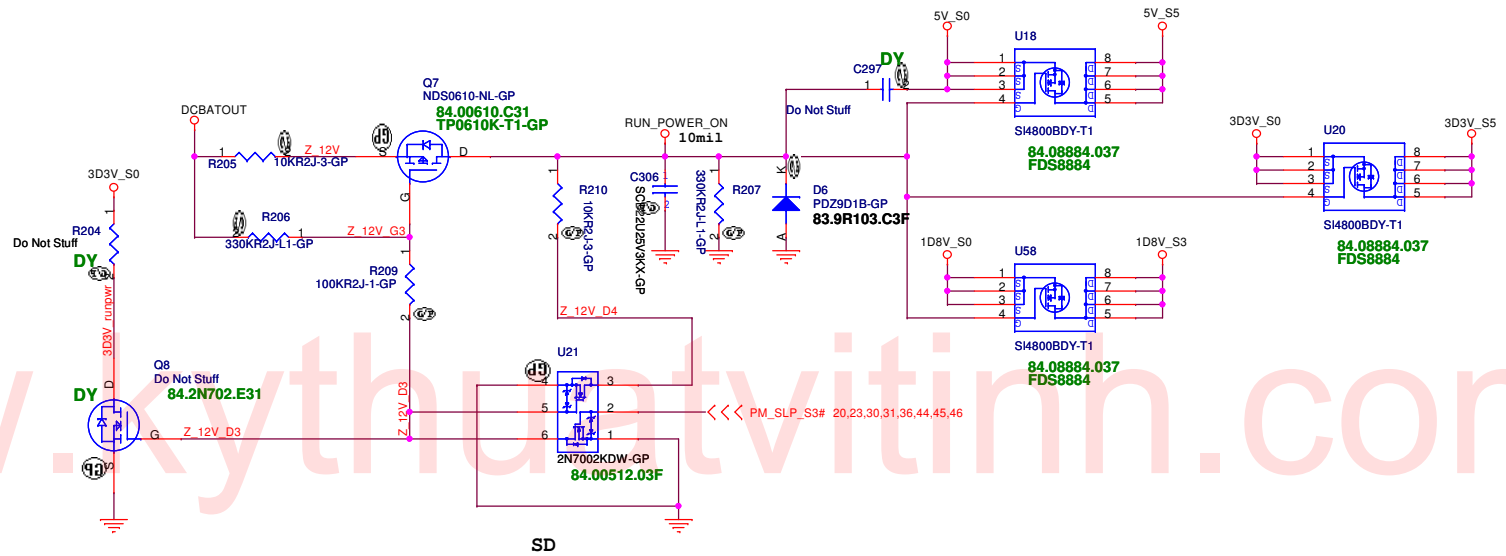
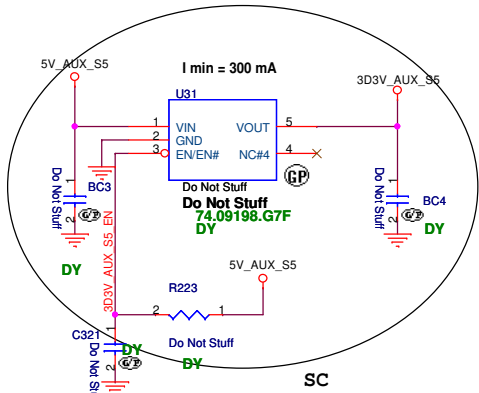


- 28 MDIO+
- 28 MDIO-
- 28 MDI+
- 28 MDI-
- 28 MDI2+
- 28 MDI2-
- 28 MDI3+
- 28 MDI3-
- 28 LAN_ACT_LED#
- 28 10M/100M/1G_LED#
- 29 LAN_ACT_LED#_SYS
- 38 LAN_ACT_LED#_DOCK
- 29 10M/100M/1G_LED#_SYS
- 38 10M/100M/1G_LED#_DOCK

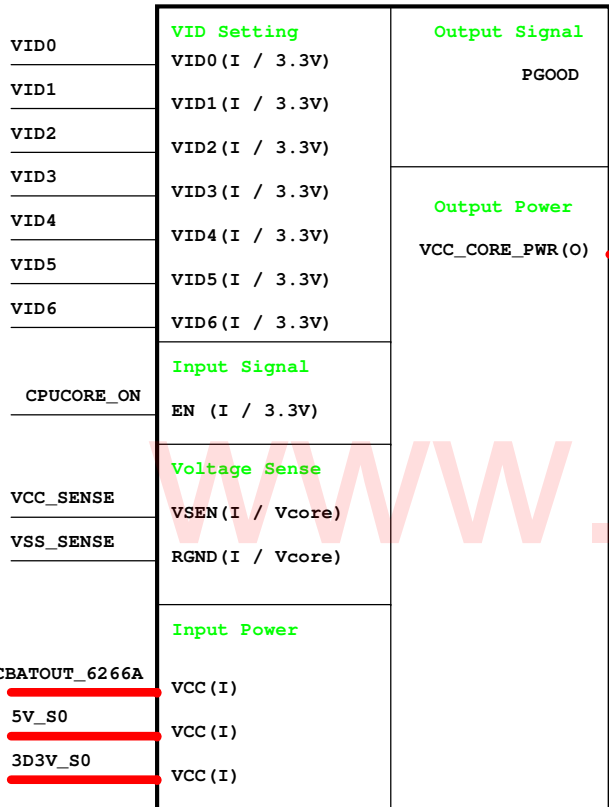
Function	SEL	
Dx to DxB1	L	DOCK
Dx to DxB2	H	SYSTEM

SB

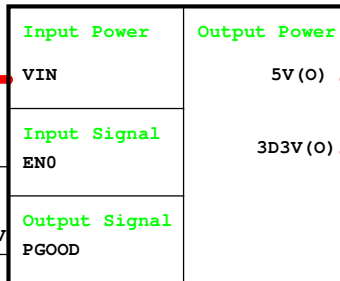




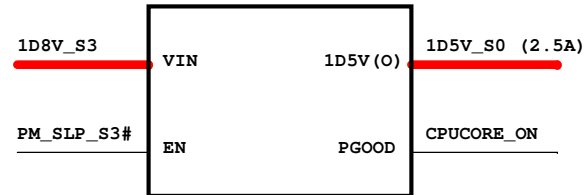
CPU_CORE
ISL6266A



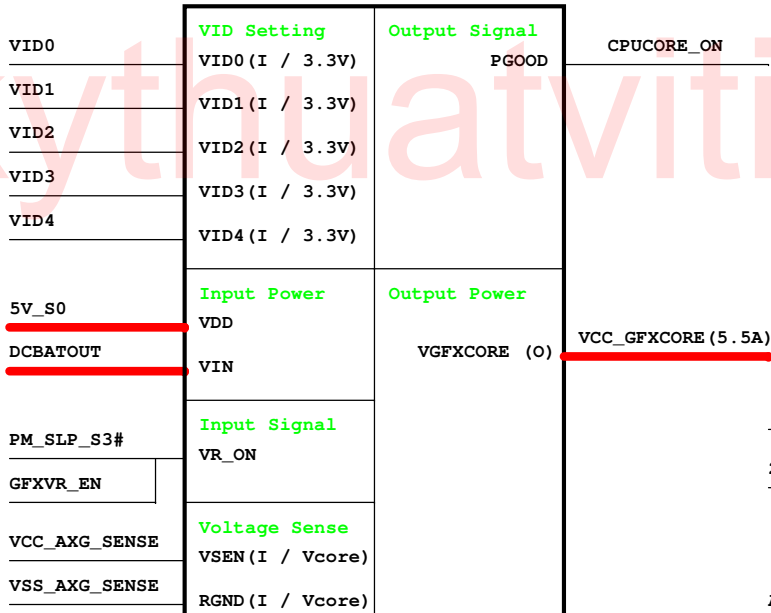
TPS51125
5V/3D3V



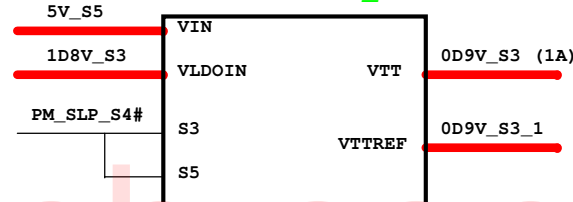
RT9018A
1D5V_S0



GFX_CORE
ISL6263A



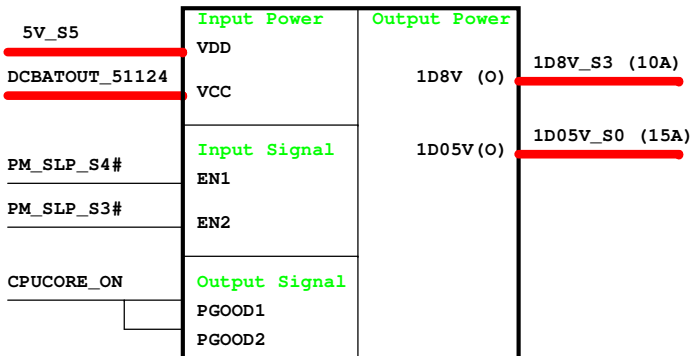
RT9026 0D9V_S0



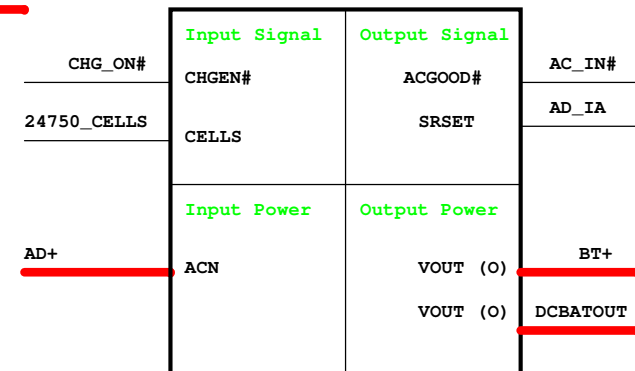
G9131 2D5V_S0



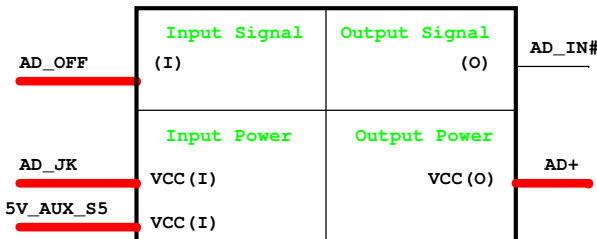
TPS51124
1D8V/1D05V



Charger BQ24750



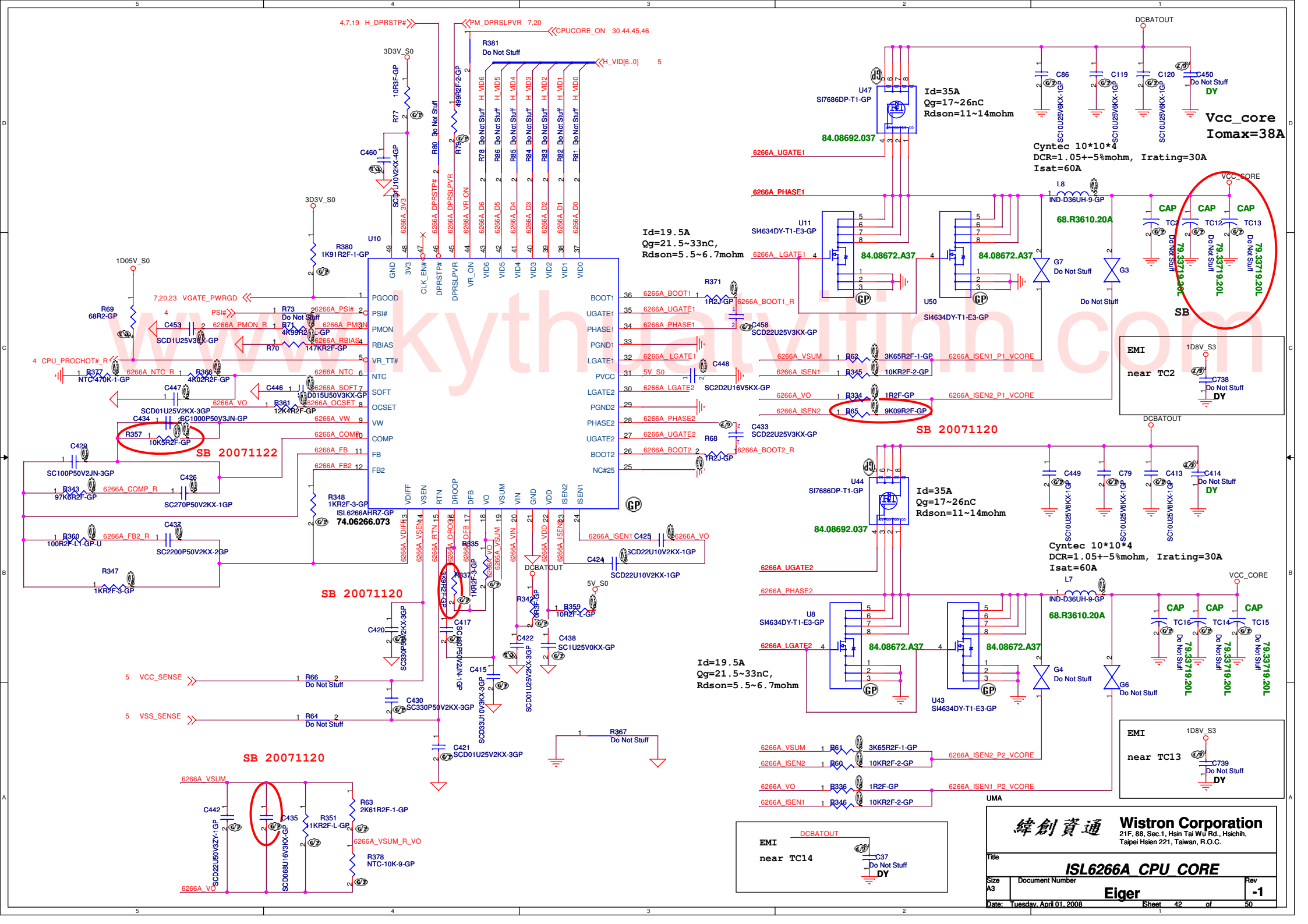
Adapter



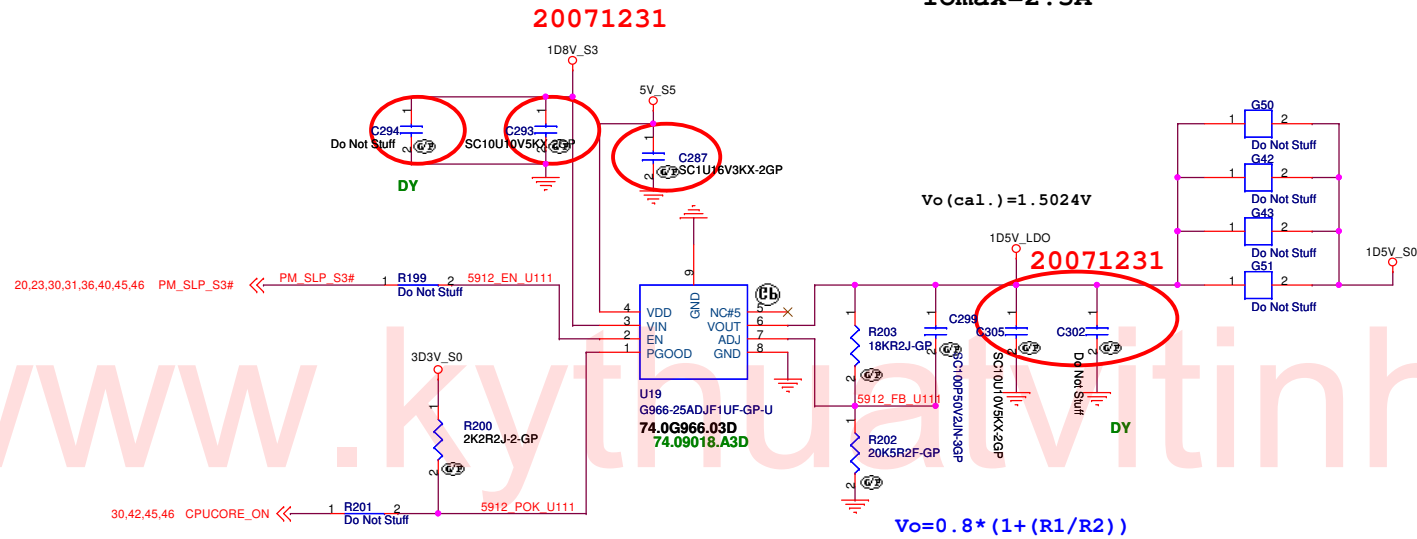
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Power Sequence Logic**

Size B Document Number **Eiger** Rev -1
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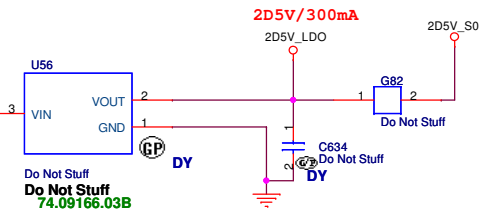
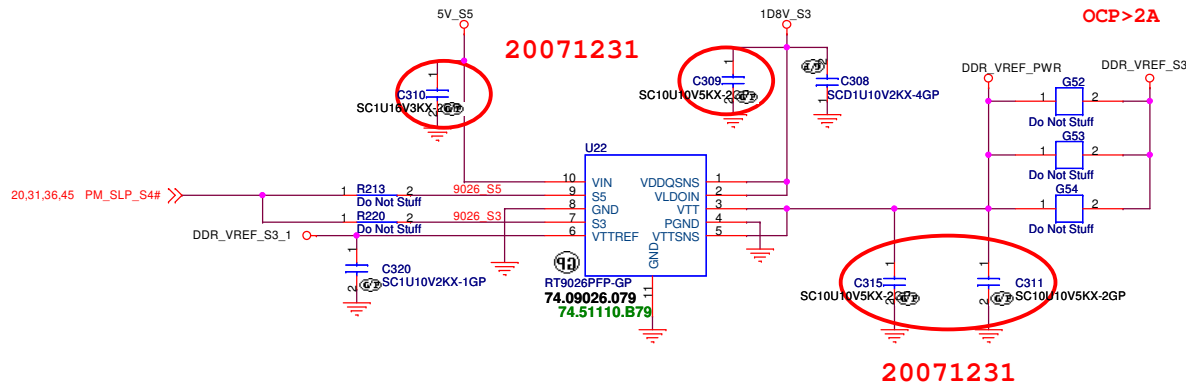


1D5V_S0
I_{omax}=2.5A

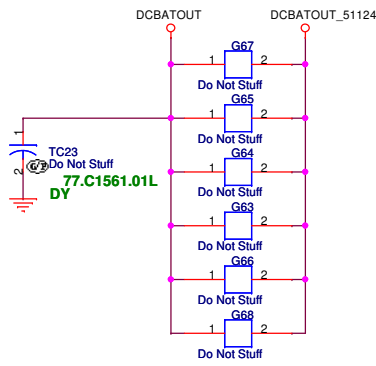


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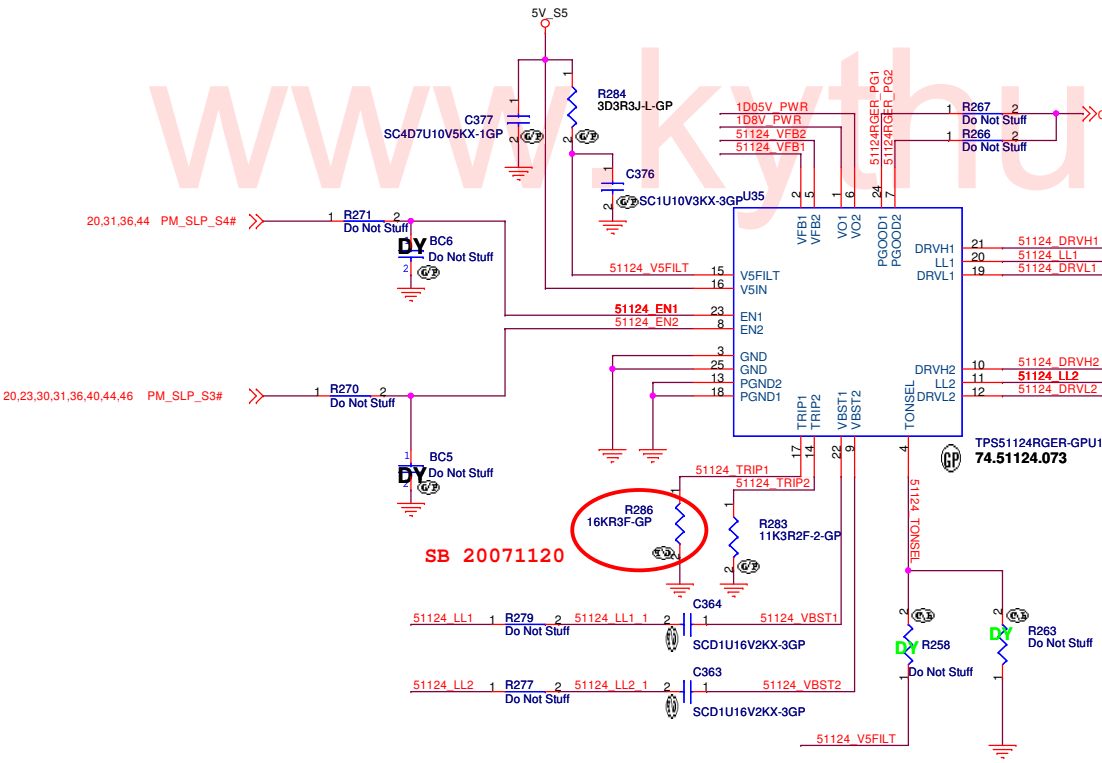
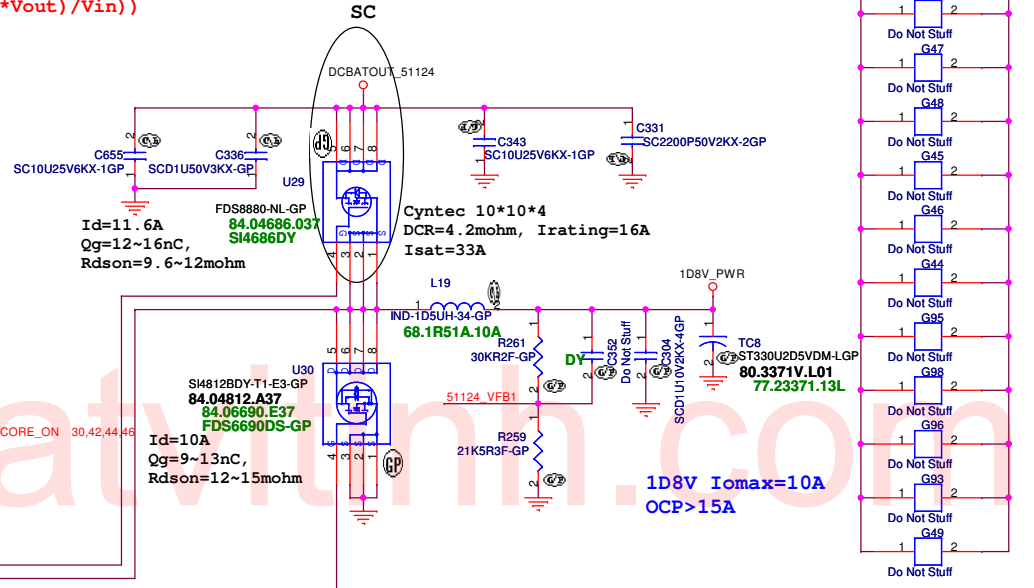
2D5V_S0
I_{omax}=1A
OCP>2A



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1D5V & 0D9V & 2D5V		
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$V_{trip} (mV) = R_{trip} (Kohm) * 10 (uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out})/V_{in})$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

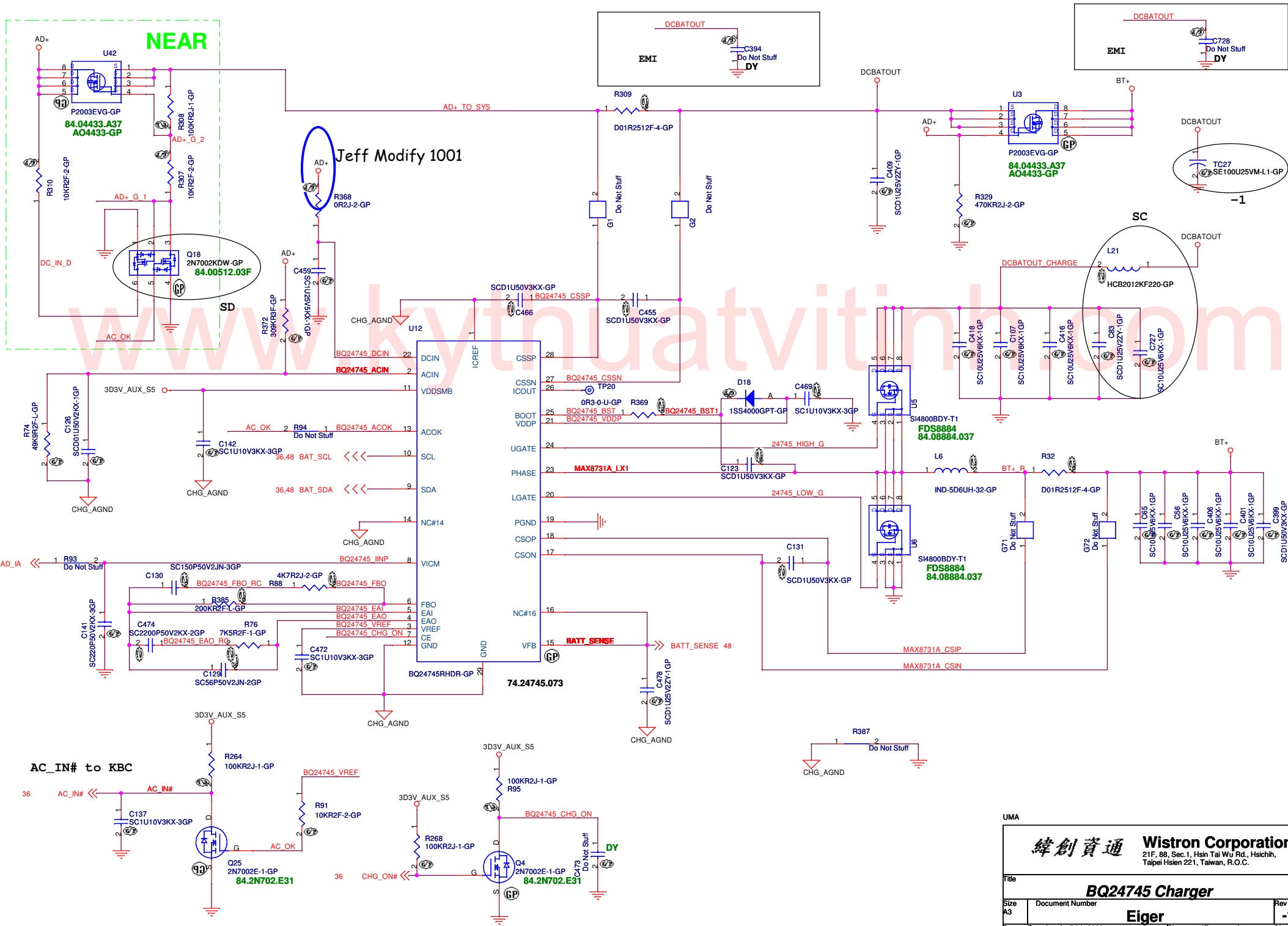


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

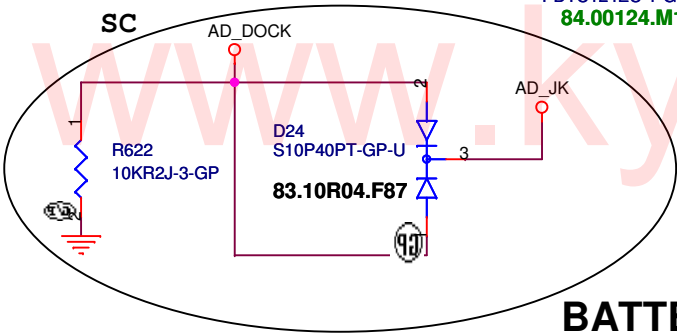
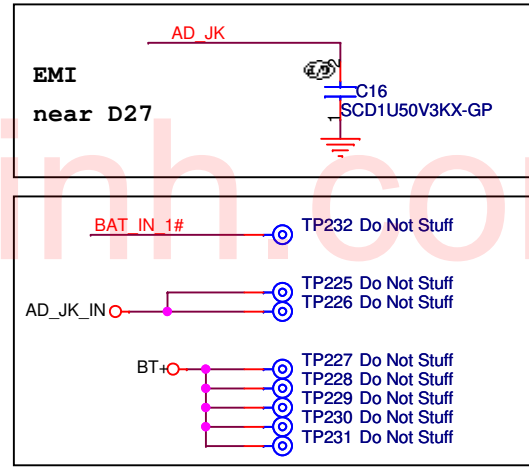
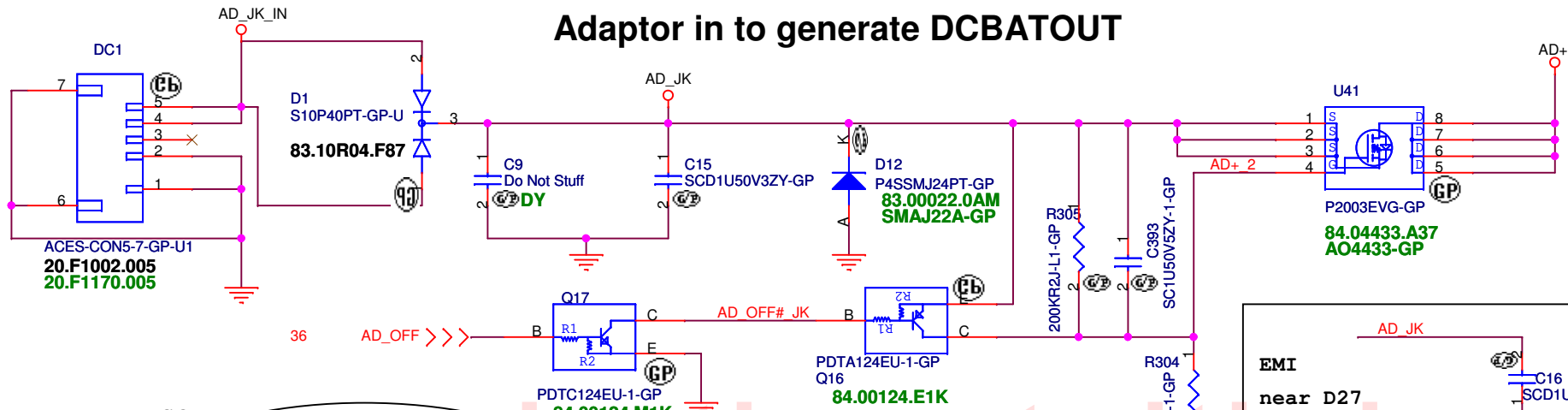
$V_{out} = 0.758V * (R1+R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2) / R2$ --> Skip Mode

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

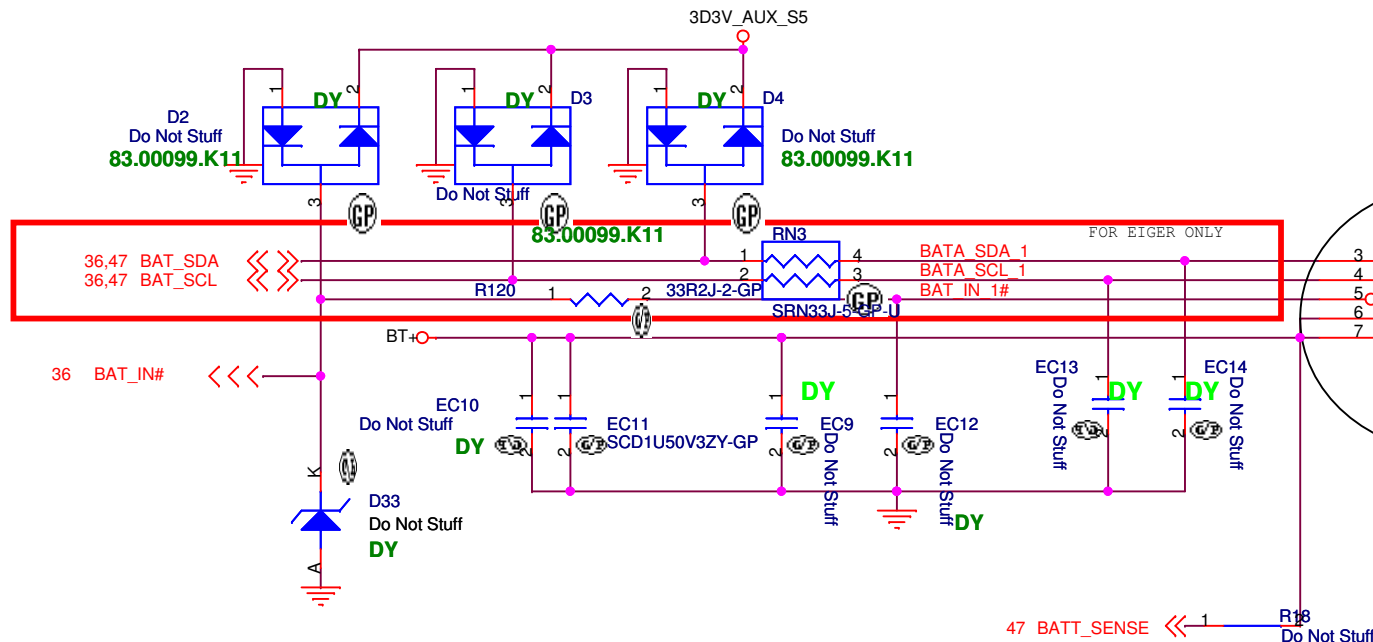
TPS51124 1D8V 1D05V
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



-1M

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Eiger

- EC SB01/07/ DY R175 (fix can not boot)
- EC SB02/07/ change R184 (intel spec change)
- EC SB03/10/ mount L2,C221 (intel spec change)
- EC SB04/15/ modify LCD2 pin define(add dig-MIC,backlight)
- EC SB05/17/ DOCK_IN_CRT# logic change
- EC SB06/18/ change HDMI level shift IC setting
- EC SB07/19/ change R606(meet HDA SPEC)
- EC SB08/23/ change PURE_HW_SHUTDOWN# ,PM_THRMTRIP-A# schematic
- EC SB09/26/ change C648 ,deltree poly switch
- EC SB10/27/ change R555,R557,R559 (vendor request)
- EC SB11/30/ change R612 (vendor request)
- EC SB12/34/ add C711 (fix audio noise)
- EC SB13/36/ add SPL_WP# (BIOS write protect)
- EC SB14/38/ add CRT_DEC# (Acer change spec)
- EC SB15/38/ add dock/no dock option schematic
- EC SB16/40/ D7(power sequencing)
- EC SC01/16/ R595,R596,R597,R598(LED)
- EC SC02/18/ HEMI level shift & switch solution change
- EC SC03/19/ ESATA function
- EC SC04/23/ H/W Thermal shut down,power off Sequence
- EC SC05/24/ Add ESATA circuit
- EC SC06/30/ Add R116(MXM acrst# Acer request)
- EC SC07/33/ Add audio ground
- EC SC08/34/ Change audio AMP circuit
- EC SC09/38/ Add RC circuit to reduce audio noise
- EC SC10/40/ 3D3V_AUX_S5 from U32 internal LDO
- EC SC11/43/ Change 5V to 5.1V
- EC SC12/47/ Isolate Change IC switching high side MOS input power
- EC SC13/48/ Isolate AD19V in and Dock19V in

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UMA

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Title EC Tracking Record			
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