

Compal Confidential

PEW71_81_91 UMA <LA-6582P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2010-06-18

REV: 0.2

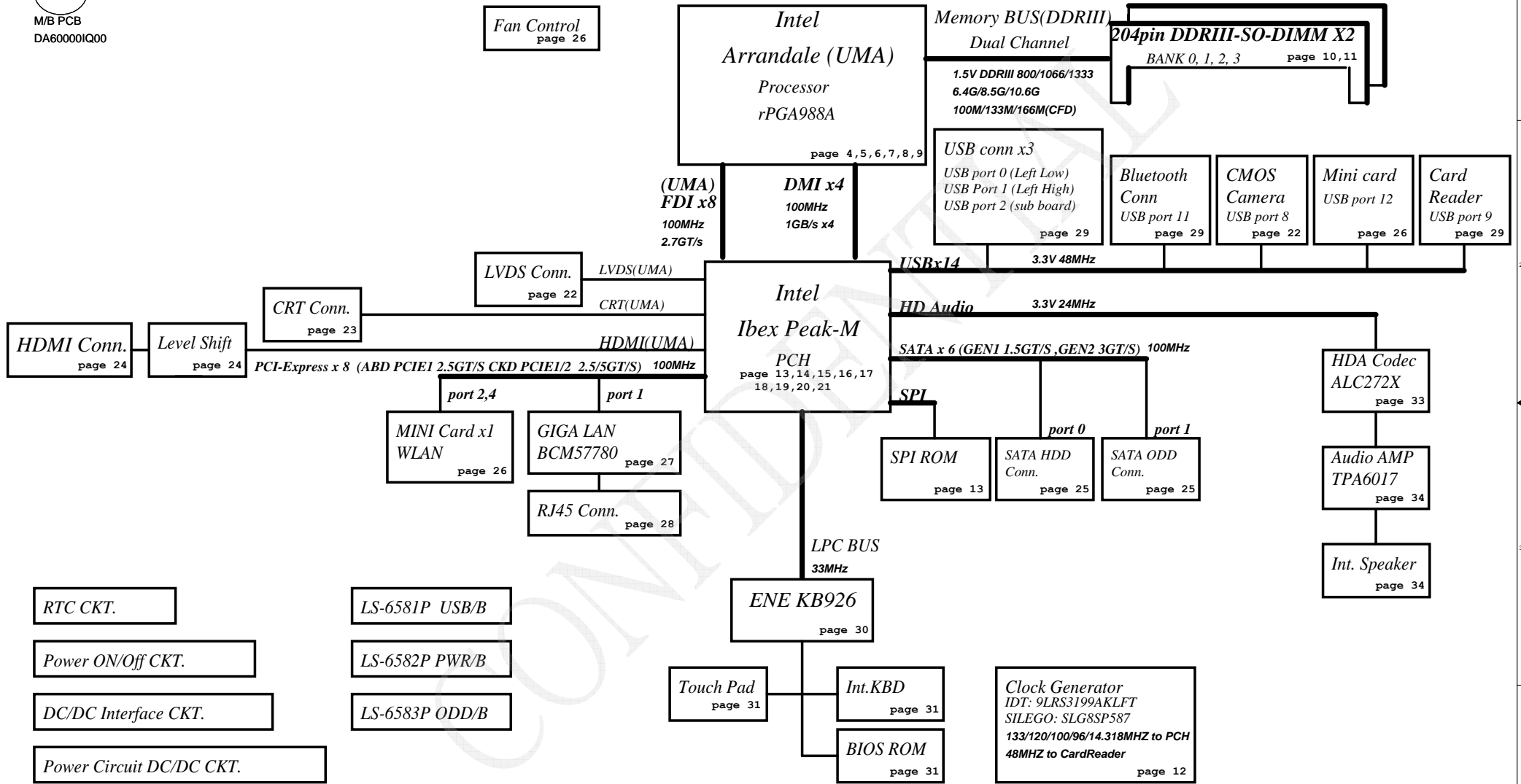
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				Date:	Friday, July 02, 2010	Sheet 1 of 48

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Model Name PEW71_81 UMA

File Name : LA-6582P

ZZZ1
M/B PCB
DA60000IQ00



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Date:	Friday, July 02, 2010	Sheet	2	of	48

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Project ID / Board ID Table for EC-AD channel

Vcc	3.3V +/- 5%					
Ra/Rc	100K +/- 5%					
	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max	Board ID	Project ID
0	0	0 V	0 V	0 V	0.1	Original NEW70/80/90/50/71/91
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2	PEW71/81/91 Audio Mono/Crystal
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	0.3	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	1.0	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V		
5	100K +/- 5%	1.453 V	1.650 V	1.759 V		
6	200K +/- 5%	1.935 V	2.200 V	2.341 V		PEW71/81/91 Audio Mono/SUSCLK
7	NC	2.500 V	3.300 V	3.300 V		NEW71/91 Optimis

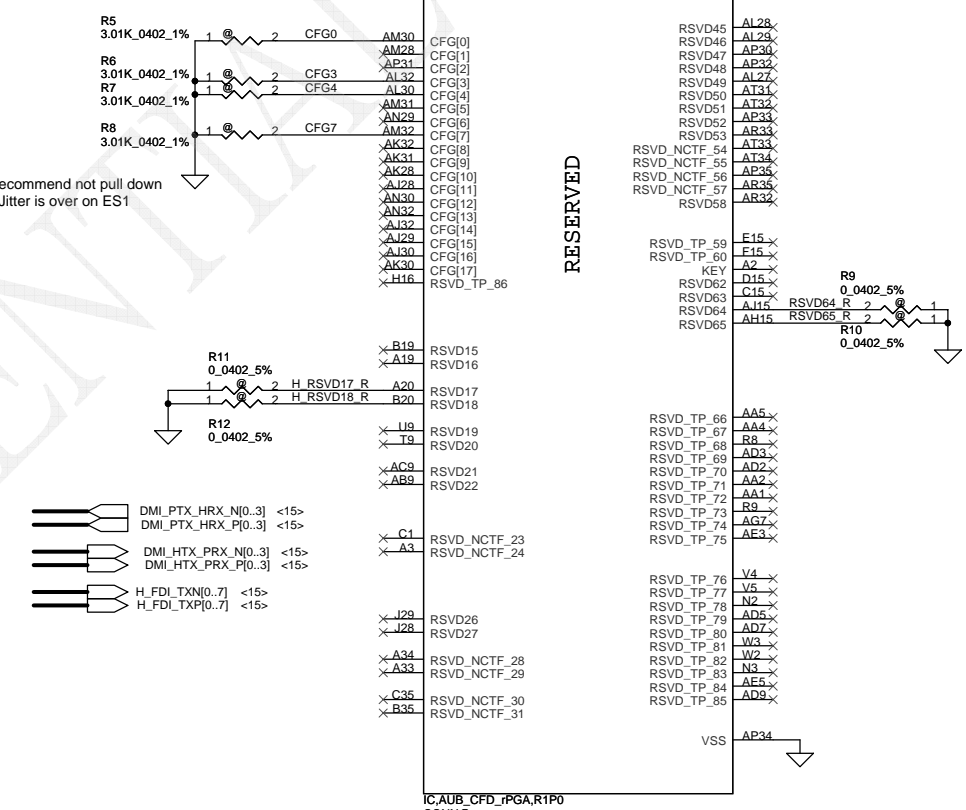
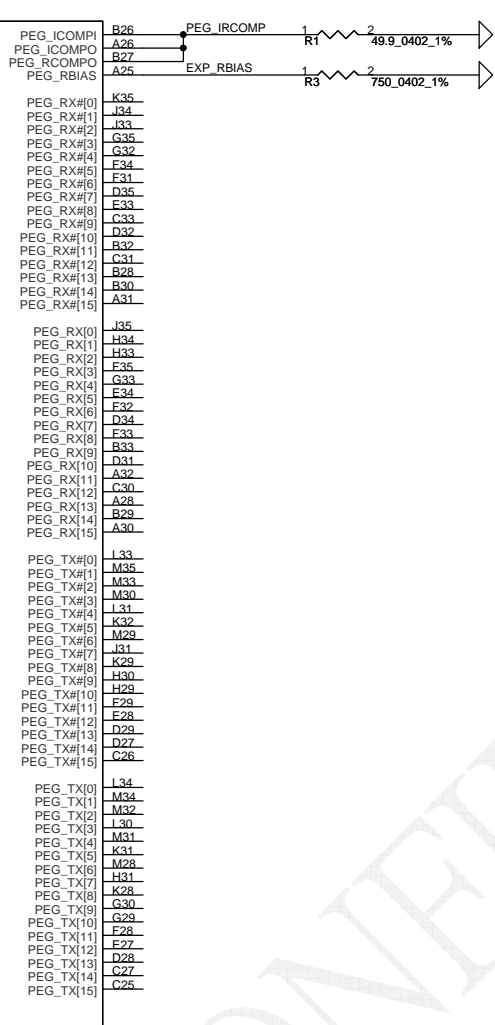
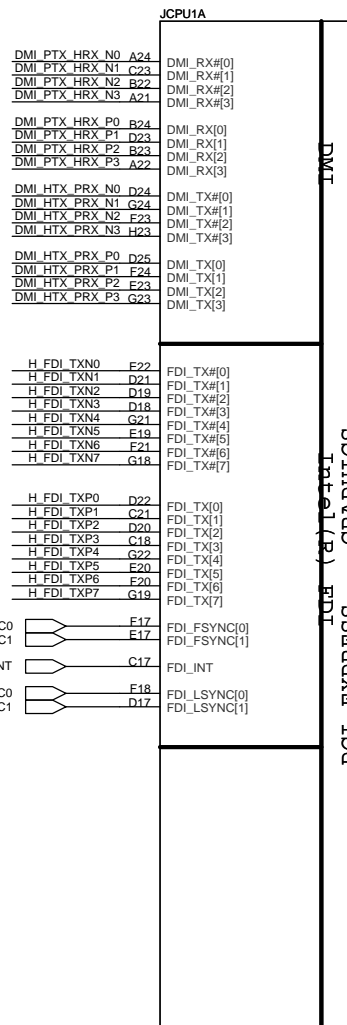
BTO Option Table

BTO Item	BOM Structure
HDMI	HDMI@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 Left Low USB	Ext1 Left Low USB
		1	Ext2 Left High USB	Ext2 Left High USB
		2	Ext3 Right USB	Ext3 Right USB
	UHCI1	3		
		4		
		5		
6				
EHCI2	UHCI3	7		
		8	Camera	Camera
	UHCI4	9	Card Reader	Card Reader
		10		
		11	Blue Tooth	Blue Tooth
		12	1st Min-Card	1st Min-Card
		13		

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Date:	Friday, July 02, 2010	Sheet	3	of	48



eDP Signals Mapping

eDP Signal	PEG Singals	Lane Reversal
eDP_TX0	PEG HTX_C GRX_P15	PEG HTX_C GRX_P0
eDP_TX#0	PEG HTX_C GRX_N15	PEG HTX_C GRX_N0
eDP_TX1	PEG HTX_C GRX_P14	PEG HTX_C GRX_P1
eDP_TX#1	PEG HTX_C GRX_N14	PEG HTX_C GRX_N1
eDP_TX2	PEG HTX_C GRX_P13	PEG HTX_C GRX_P2
eDP_TX#2	PEG HTX_C GRX_N13	PEG HTX_C GRX_N2
eDP_TX3	PEG HTX_C GRX_P12	PEG HTX_C GRX_P3
eDP_TX#3	PEG HTX_C GRX_N12	PEG HTX_C GRX_N3
eDP_AUX	PEG GTX_C HRX_P13	PEG GTX_C HRX_P2
eDP_AUX#	PEG GTX_C HRX_N13	PEG GTX_C HRX_N2
eDP_HPD#	PEG GTX_C HRX_P12	PEG GTX_C HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Buffering enabled

CFG3 - PCI-Express Static Lane Reversal

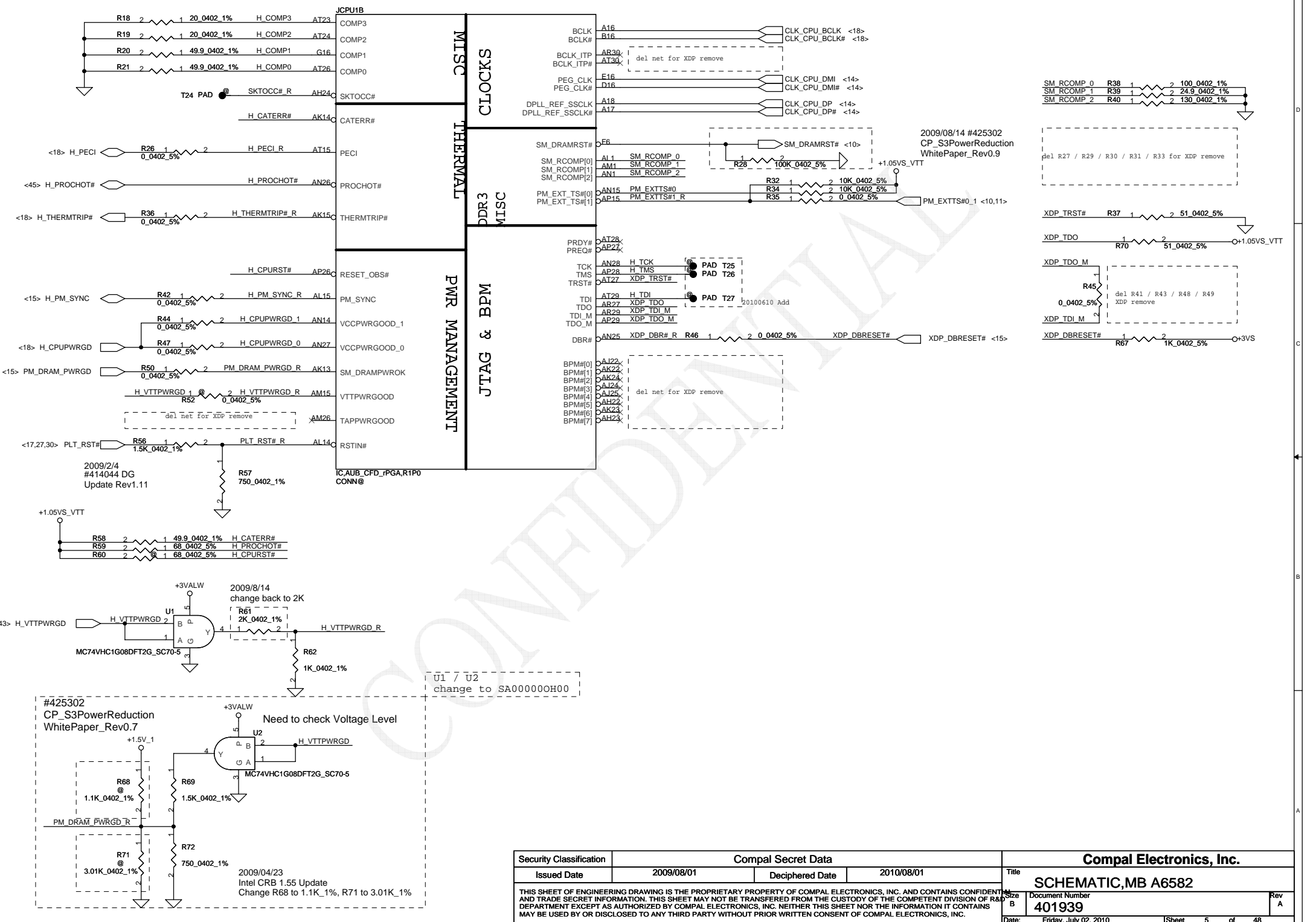
*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

**Default

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Date:	Friday, July 02, 2010	Sheet	4	of	48



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				401939	
Date:	Friday, July 02, 2010	Sheet	5	of	48

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 <10> DDR_A_DQS[0..7]
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 <10> DDR_A_MA[0..15]

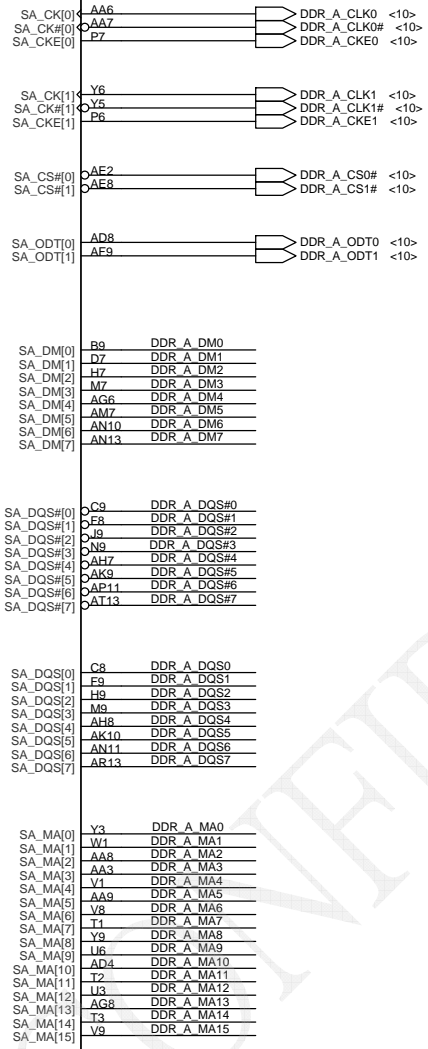
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- DDR A D0 A10
- DDR A D1 C10
- DDR A D2 C7
- DDR A D3 A7
- DDR A D4 B10
- DDR A D5 D10
- DDR A D6 E10
- DDR A D7 A8
- DDR A D8 D8
- DDR A D9 F10
- DDR A D10 E6
- DDR A D11 E7
- DDR A D12 E9
- DDR A D13 B7
- DDR A D14 E7
- DDR A D15 C6
- DDR A D16 H10
- DDR A D17 G8
- DDR A D18 K7
- DDR A D19 J8
- DDR A D20 G7
- DDR A D21 G10
- DDR A D22 J7
- DDR A D23 J10
- DDR A D24 L7
- DDR A D25 M6
- DDR A D26 M8
- DDR A D27 I9
- DDR A D28 L6
- DDR A D29 K8
- DDR A D30 SA
- DDR A D31 P9
- DDR A D32 AH5
- DDR A D33 AF5
- DDR A D34 AK6
- DDR A D35 AK7
- DDR A D36 AF6
- DDR A D37 AG5
- DDR A D38 A17
- DDR A D39 A16
- DDR A D40 A110
- DDR A D41 A19
- DDR A D42 AL10
- DDR A D43 AK12
- DDR A D44 AK8
- DDR A D45 A17
- DDR A D46 AK11
- DDR A D47 A18
- DDR A D48 AN8
- DDR A D49 AM10
- DDR A D50 AR11
- DDR A D51 AL11
- DDR A D52 AM9
- DDR A D53 AN9
- DDR A D54 AT11
- DDR A D55 AP12
- DDR A D56 AM12
- DDR A D57 AN12
- DDR A D58 AM13
- DDR A D59 AT14
- DDR A D60 AT12
- DDR A D61 AL13
- DDR A D62 AR14
- DDR A D63 AP14

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 <10> DDR_A_BS1
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 <10> DDR_A_WE#

DDR SYSTEM MEMORY A



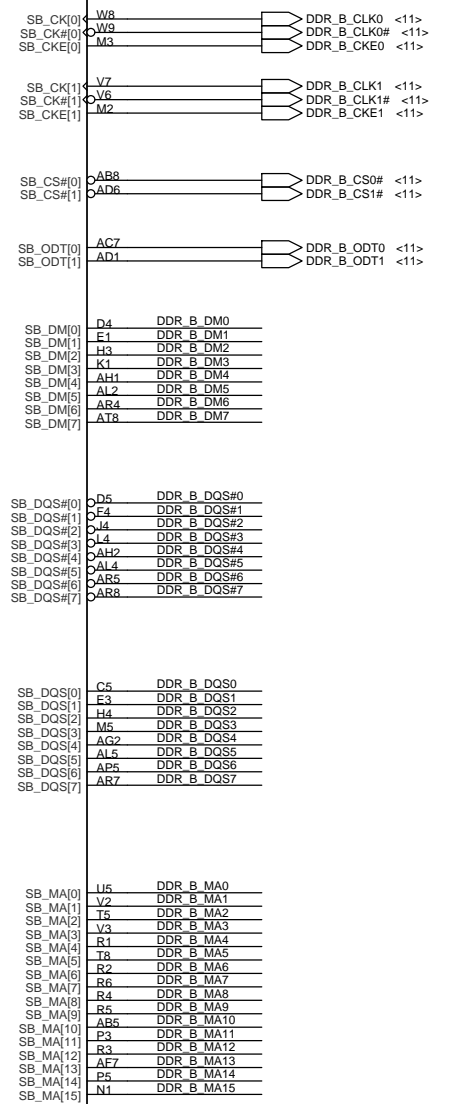
IC_AUB_CFD_rPGA_R1P0
 CONN@

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JCPU1D

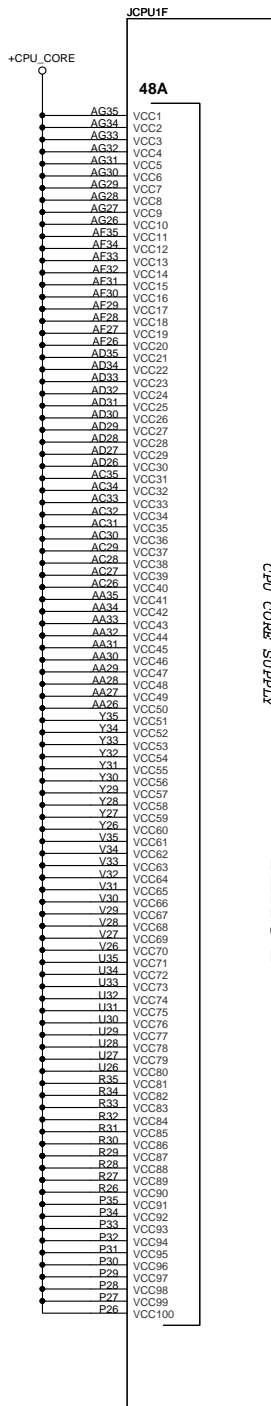
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- DDR B D1 A5
- DDR B D2 C3
- DDR B D3 B3
- DDR B D4 E4
- DDR B D5 A6
- DDR B D6 C4
- DDR B D7 D1
- DDR B D8 D1
- DDR B D9 D2
- DDR B D10 F2
- DDR B D11 E1
- DDR B D12 C2
- DDR B D13 E3
- DDR B D14 F3
- DDR B D15 G4
- DDR B D16 H6
- DDR B D17 G2
- DDR B D18 J6
- DDR B D19 J3
- DDR B D20 G1
- DDR B D21 G5
- DDR B D22 J2
- DDR B D23 J1
- DDR B D24 J5
- DDR B D25 L2
- DDR B D26 K1
- DDR B D27 M2
- DDR B D28 K4
- DDR B D29 K5
- DDR B D30 M4
- DDR B D31 N5
- DDR B D32 AG1
- DDR B D33 AG1
- DDR B D34 AG1
- DDR B D35 AK1
- DDR B D36 AG4
- DDR B D37 AG3
- DDR B D38 AJ4
- DDR B D39 AH4
- DDR B D40 AK4
- DDR B D41 AK4
- DDR B D42 AM6
- DDR B D43 AN2
- DDR B D44 AK5
- DDR B D45 AK2
- DDR B D46 AM4
- DDR B D47 AM3
- DDR B D48 AP3
- DDR B D49 AN5
- DDR B D50 AT4
- DDR B D51 AN6
- DDR B D52 AN4
- DDR B D53 AN3
- DDR B D54 AT5
- DDR B D55 AT6
- DDR B D56 AN7
- DDR B D57 AP6
- DDR B D58 AT9
- DDR B D59 AT9
- DDR B D60 AT7
- DDR B D61 AP9
- DDR B D62 AR10
- DDR B D63 AT10

DDR SYSTEM MEMORY - B



IC_AUB_CFD_rPGA_R1P0
 CONN@

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Date: Friday, July 02, 2010				Sheet	6 of 48



WW15 MOW
Peak 21A
Continuous 18A

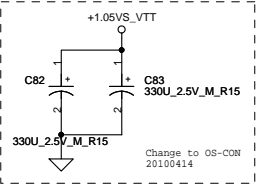
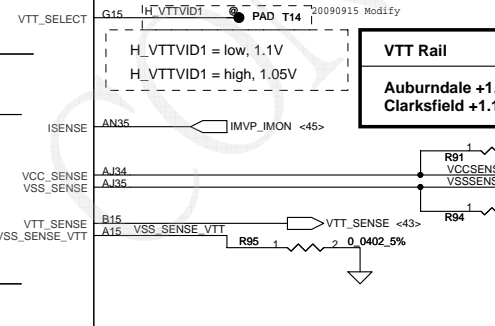
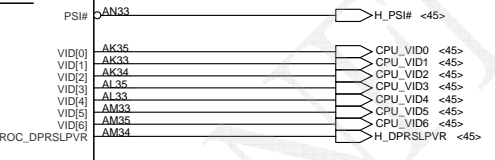
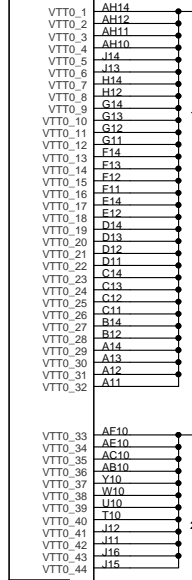
1.1V RAIL POWER

CPU CORE SUPPLY

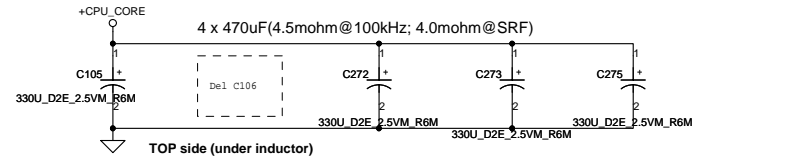
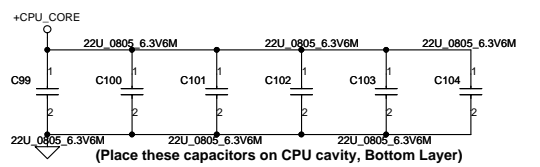
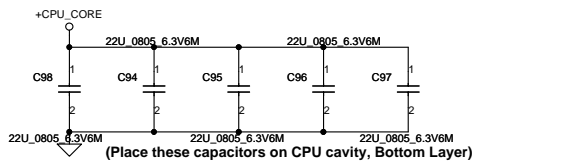
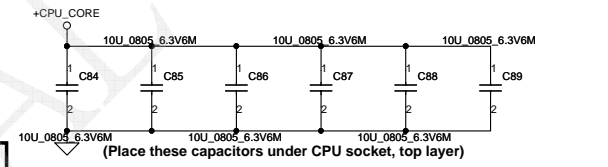
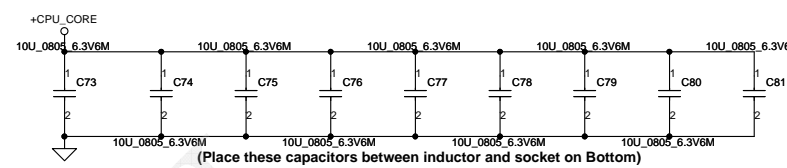
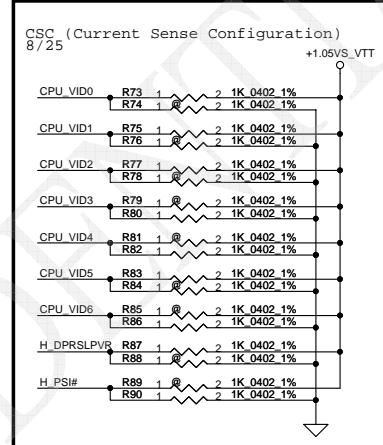
POWER

CPU VIDS

SENSE LINES



VTT Rail
Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

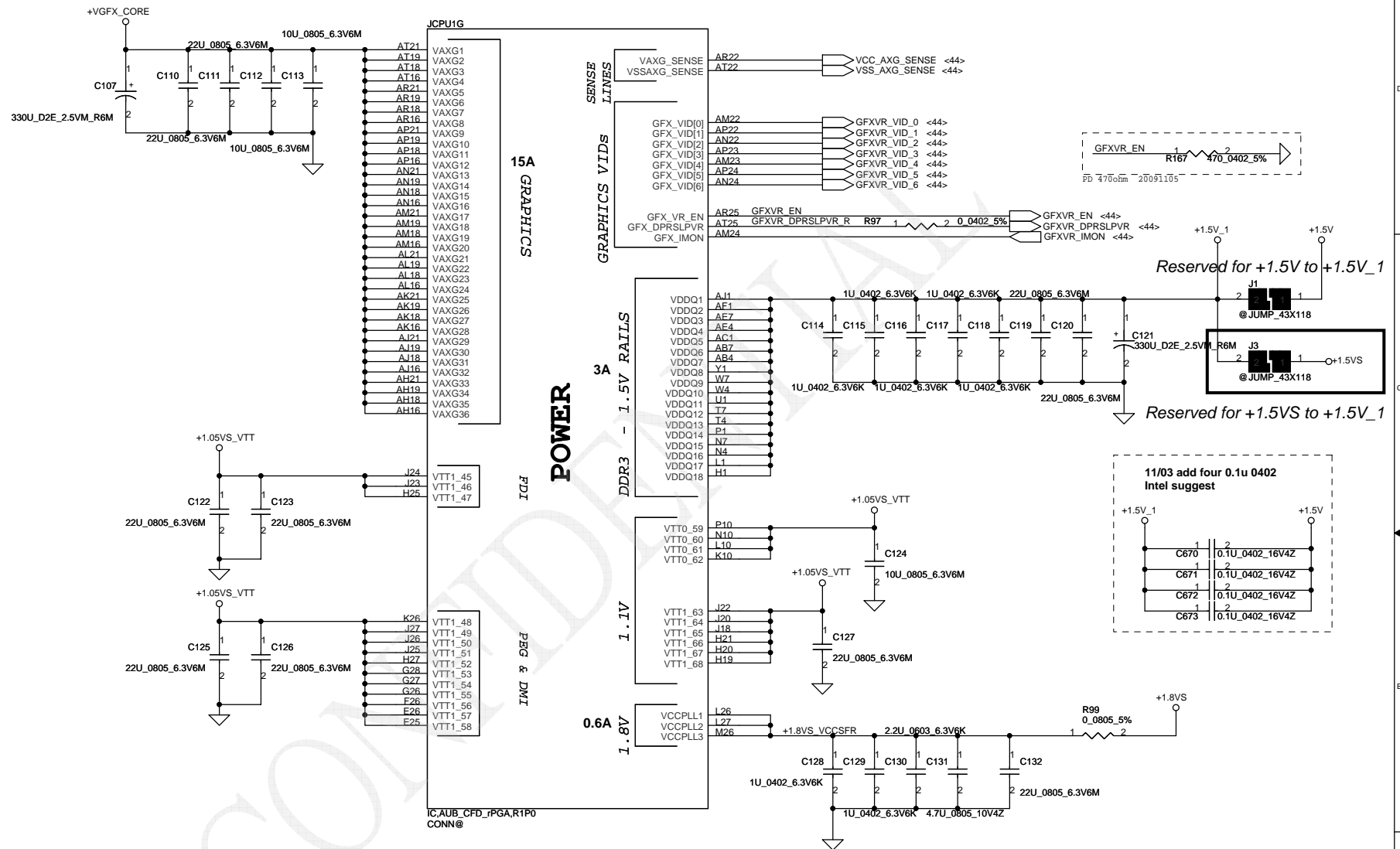


+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP, Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

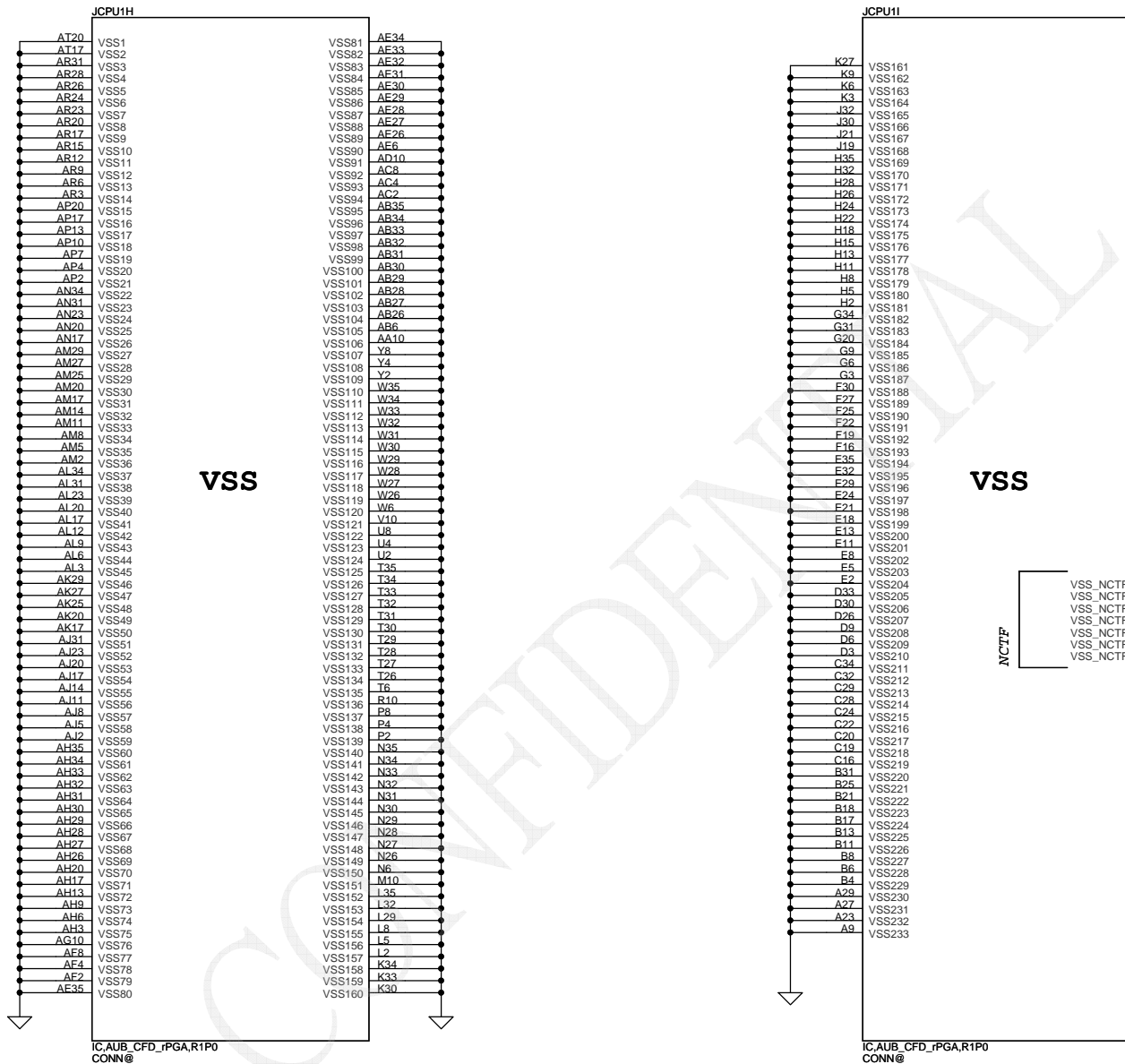
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CONN@

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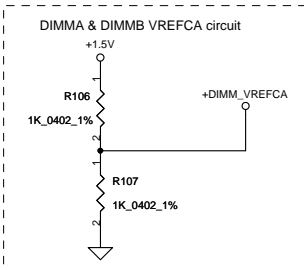
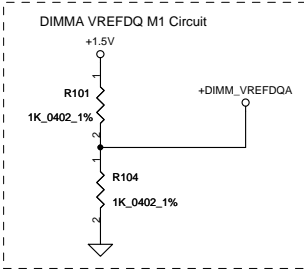
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Document Number	401939		
Date:	Friday, July 02, 2010	Sheet	7 of 48



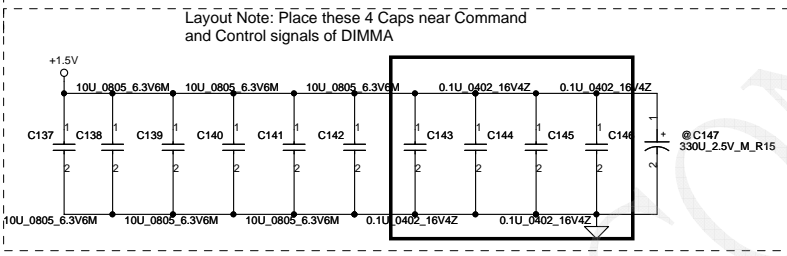
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Size	Document Number	Customer	Rev		
	401939		A		
Date:	Friday, July 02, 2010	Sheet	8	of 48	



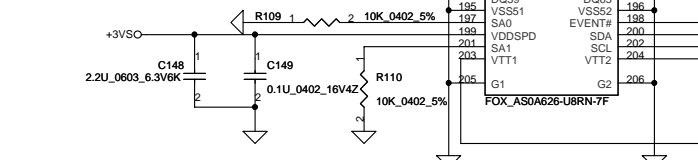
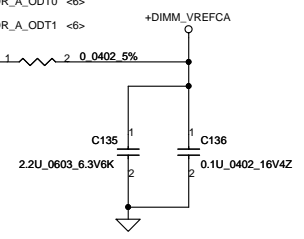
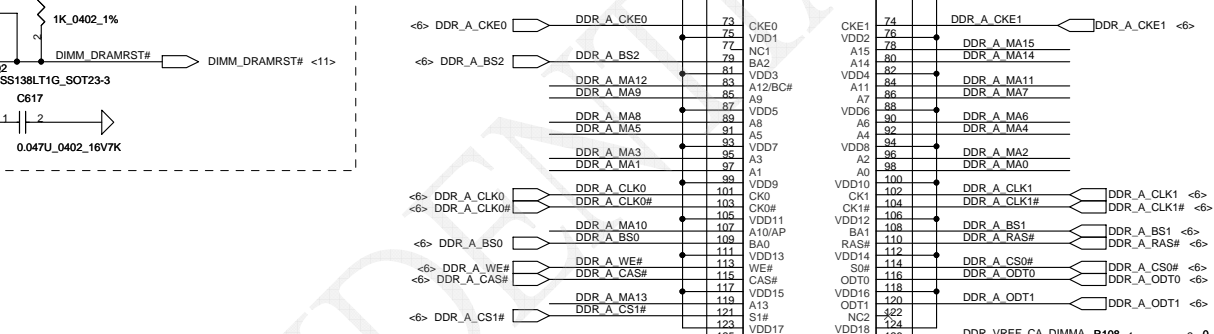
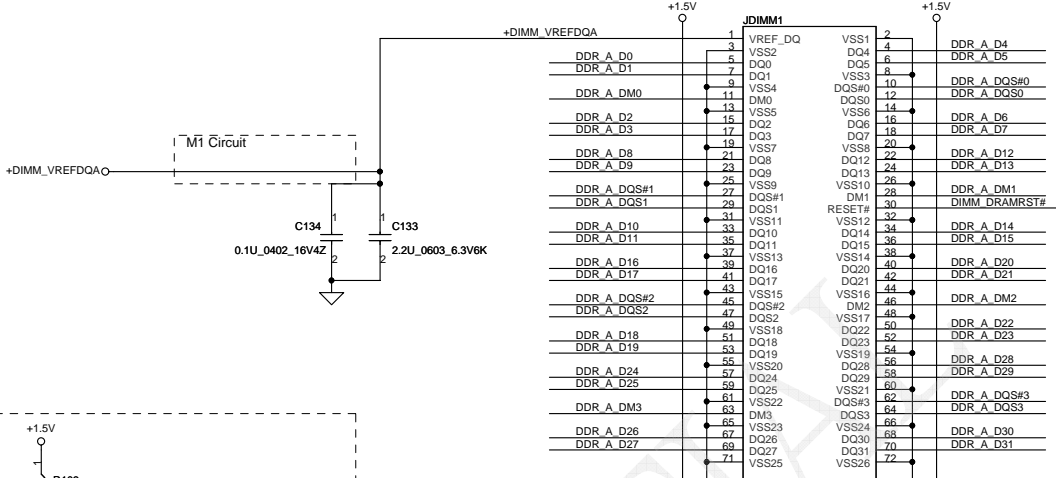
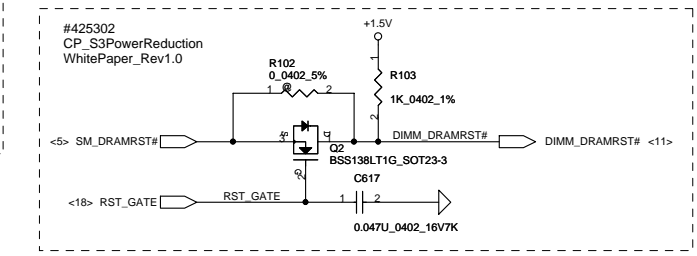
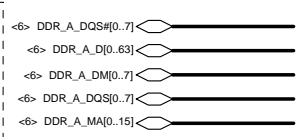
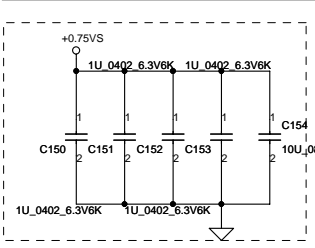
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				401939	A
Date:				Friday, July 02, 2010	Sheet 9 of 48



Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



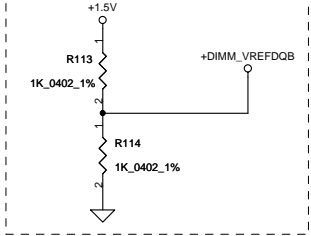
DDR3 SO-DIMM A
Change to Reverse Type
8mm High

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Date:	Friday, July 02, 2010	Sheet	10	of	48	

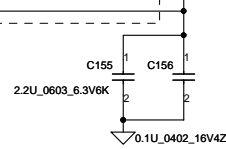
- <6> DDR_B_DQS#0[0..7]
- <6> DDR_B_D[0..63]
- <6> DDR_B_DM[0..7]
- <6> DDR_B_DQS#0[0..7]
- <6> DDR_B_MA[0..15]

2008/9/8 #400755
 Calpella Clarksville
 DDR3 SO-DIMM
 VREFDQ Platform
 Design Guide Change Details

DIMMB VREFDQ M1 Circuit

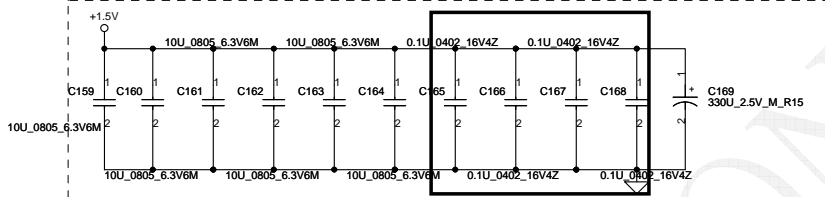


M1 Circuit

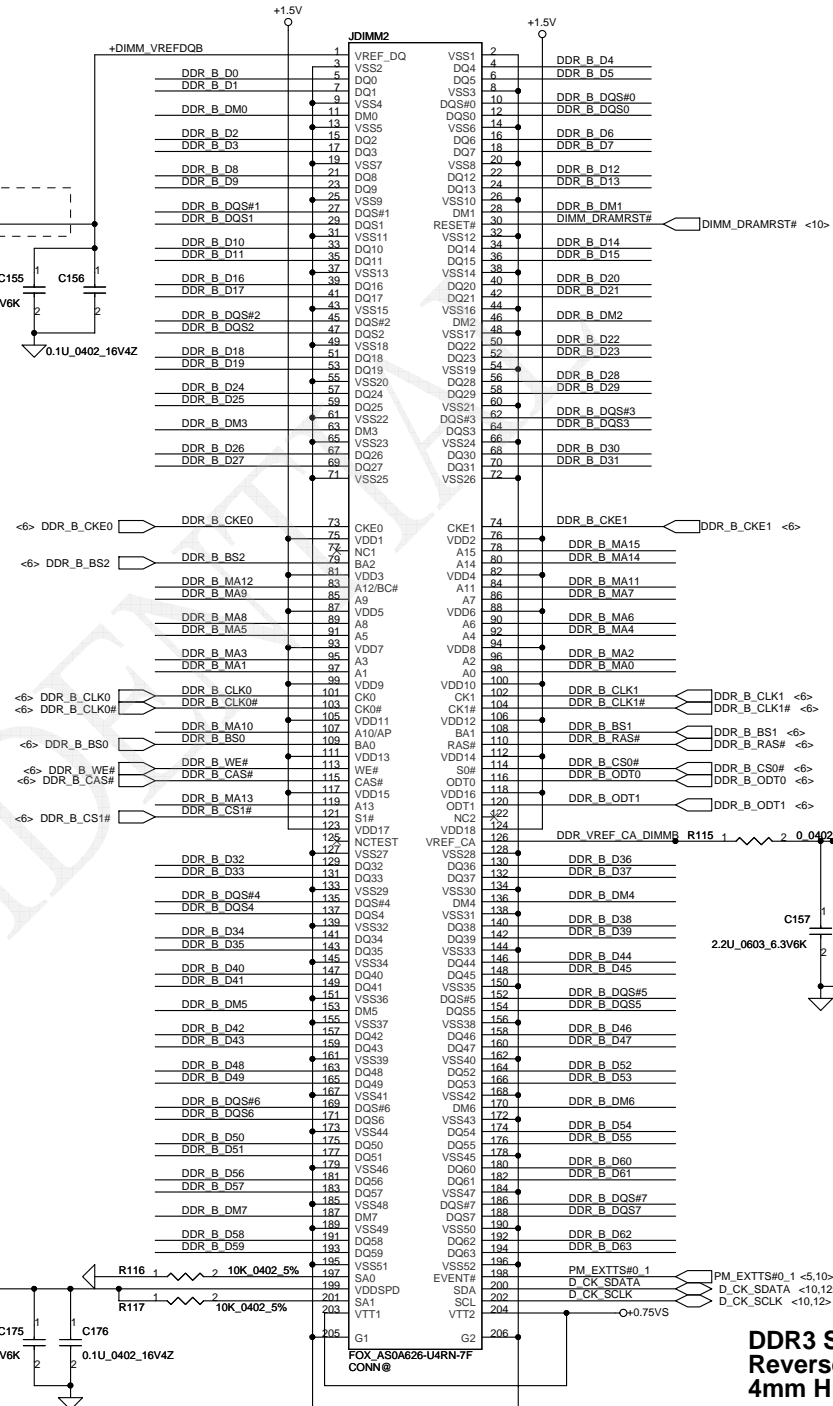
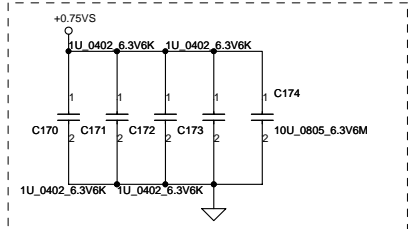


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

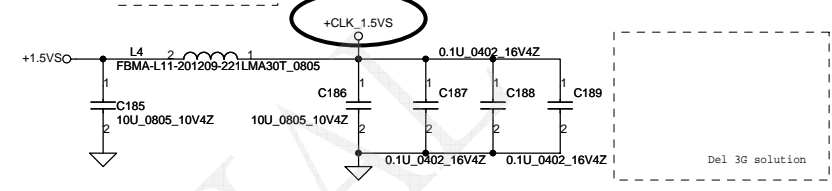
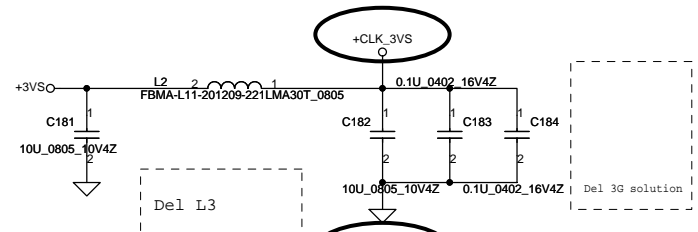
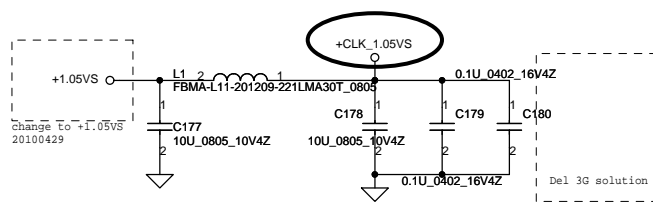


Layout Note:
Place near JDIMM2.203 & JDIMM2.204

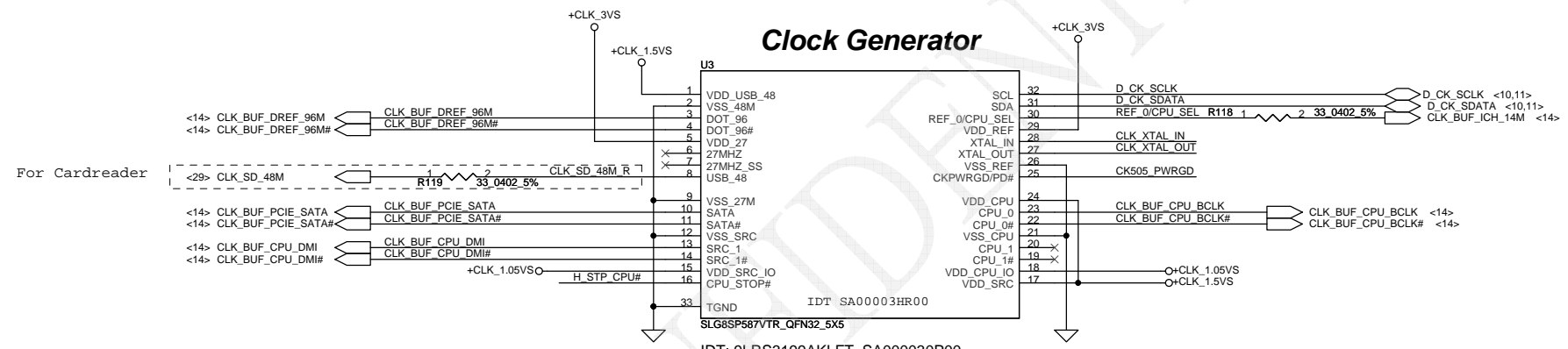


**DDR3 SO-DIMM B
Reverse Type
4mm High**

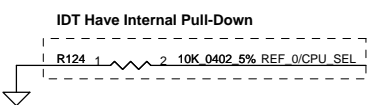
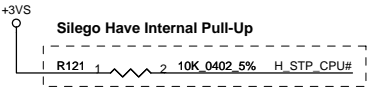
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				401939		A	
				Date: Friday, July 02, 2010		Sheet 11 of 48	



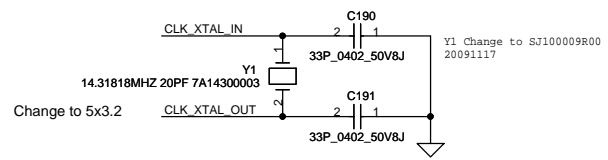
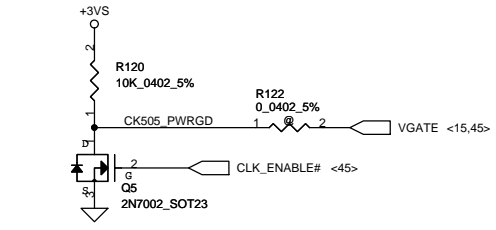
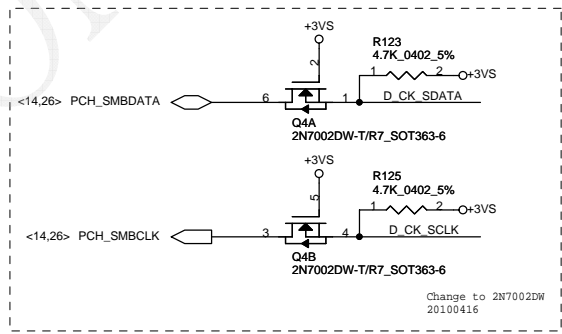
Clock Generator



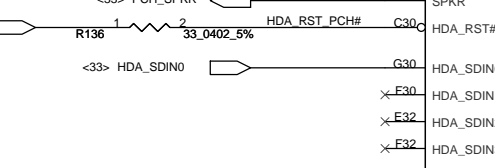
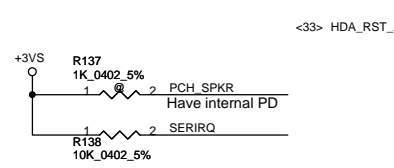
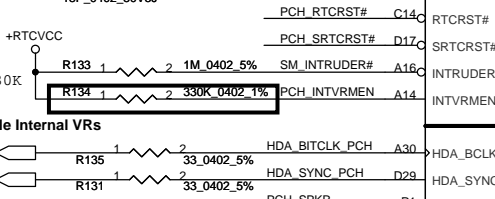
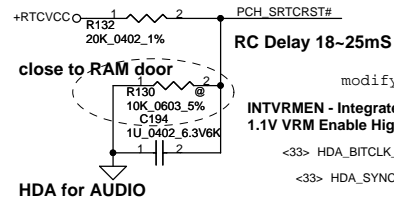
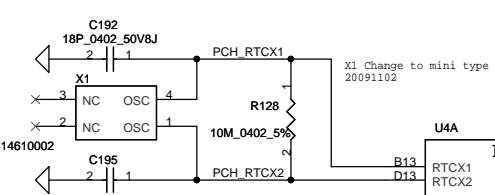
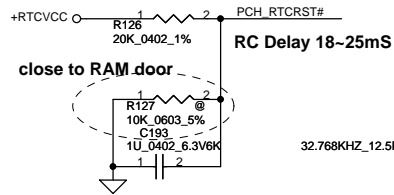
IDT: 9LRS3199AKLFT, SA00003P00
 SILEGO: SLG8SP587V(WF), SA00002XY10
 Low Power:
 IDT: 9LVS3199AKLFT, SA00003HR00
 Realtek: RTM890N-631-GRT, SA00003HQ00



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

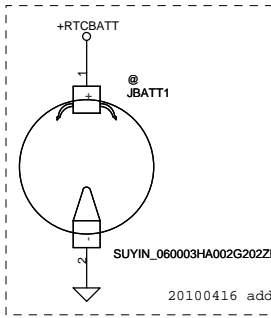
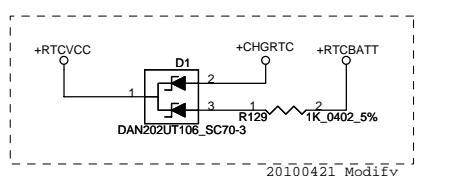
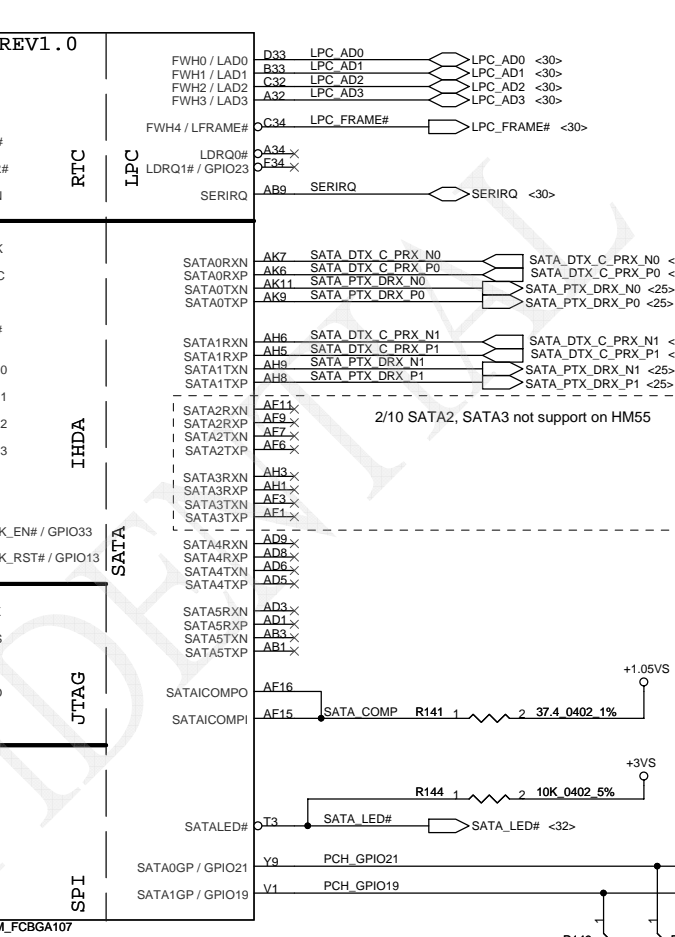
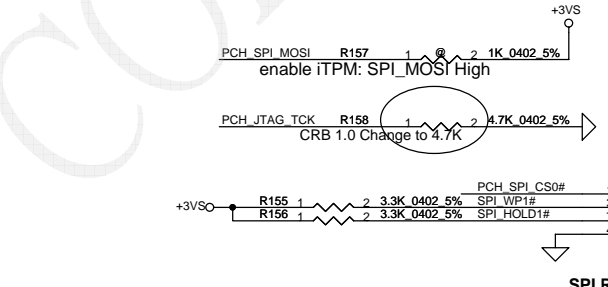
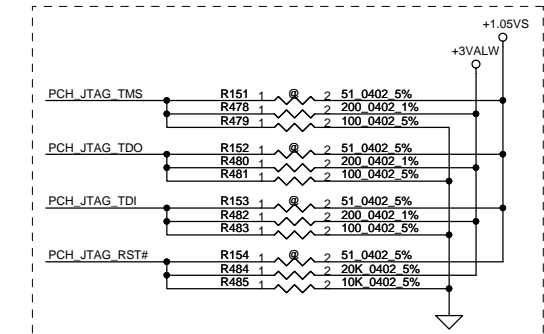
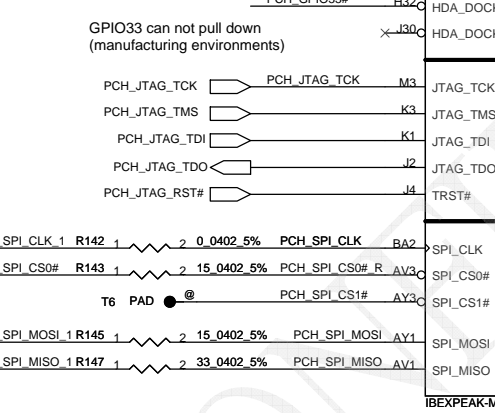


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				Customer	401939
				Date:	Friday, July 02, 2010
				Sheet	12 of 48



If GPIO33 pull down, ME will not working. For factory update ME, pull down resistor pull under door.

GPIO33 has a weak internal pull-up
NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.



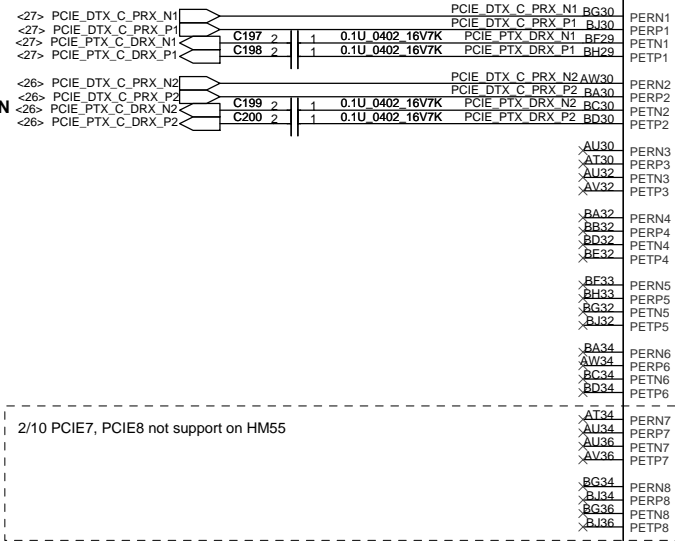
GPIO21	Project
0	NEW50/70/80/90
1	NEW71/91

	GPIO19	GPIO37
	PCH_GPIO19	VGA_PRSTN1_L#
dGPU	0	0
iGPU	0	1
SG	1	X

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				Customer	401939
				Date:	Friday, July 02, 2010
				Sheet	13 of 48

For PCIE LAN

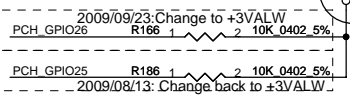
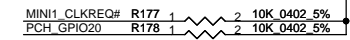
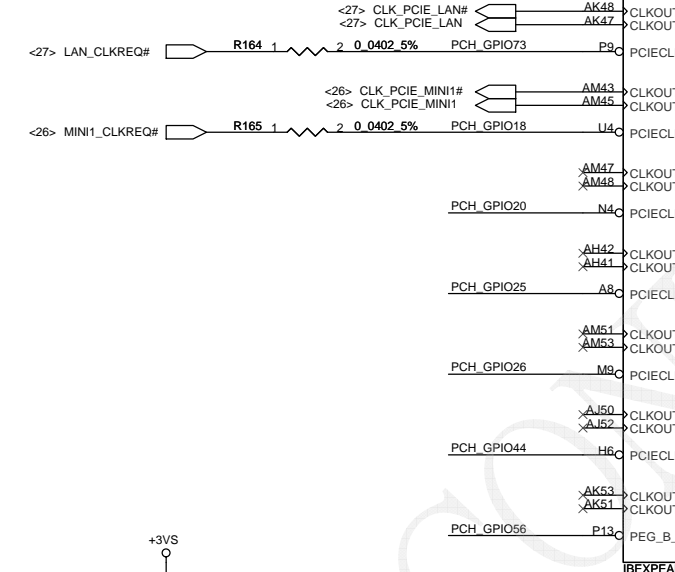
For Wireless LAN



2/10 PCIE7, PCIE8 not support on HM55

For PCIE LAN

For Wireless LAN



EC_LID_OUT#	R179	1	2	10K_0402_5%
PCH_SMBCLK	R180	1	2	2.2K_0402_5%
PCH_SMBDATA	R181	1	2	2.2K_0402_5%
PCH_GPIO60	R182	1	2	10K_0402_5%
PCH_SML1CLK	R183	1	2	2.2K_0402_5%
PCH_SML1DAT	R184	1	2	2.2K_0402_5%
PCH_GPIO74	R185	1	2	10K_0402_5%
PCH_GPIO44	R187	1	2	10K_0402_5%
PCH_GPIO56	R188	1	2	10K_0402_5%
PCH_GPIO73	R189	1	2	10K_0402_5%

U4B

REV1.0

PCI-E*

Controller

Link

PEG

From CLK BUFFER

CLKOUT_PEG_A_N

CLKOUT_PEG_A_P

CLKOUT_DMI_N

CLKOUT_DMI_P

CLKOUT_DP_N / CLKOUT_BCLK1_N

CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N

CLKIN_DMI_P

CLKIN_BCLK_N

CLKIN_BCLK_P

CLKIN_DOT_96M

CLKIN_DOT_96P

CLKIN_SATA_N / CKSSCD_N

CLKIN_SATA_P / CKSSCD_P

REFCLK14IN

CLKIN_PCIELOOPBACK

XTAL25_IN

XTAL25_OUT

XCLK_RCOMP

CLKOUTFLEX0 / GPIO64

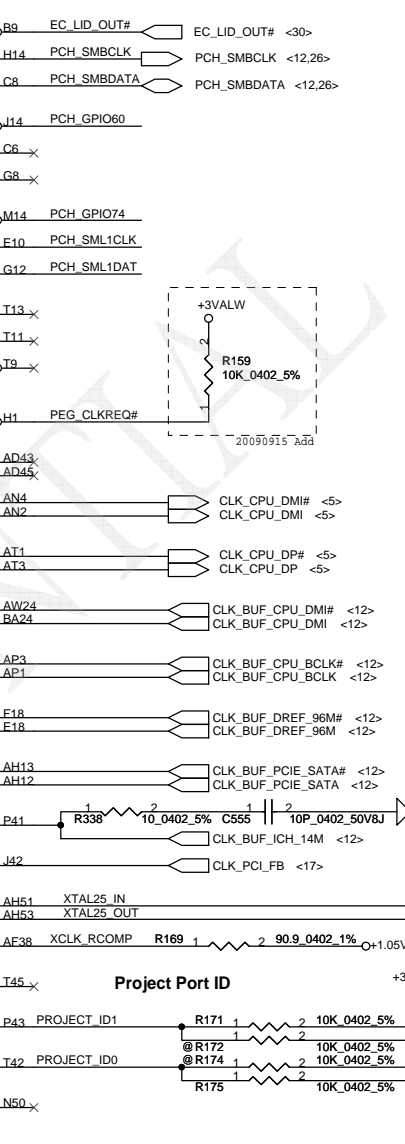
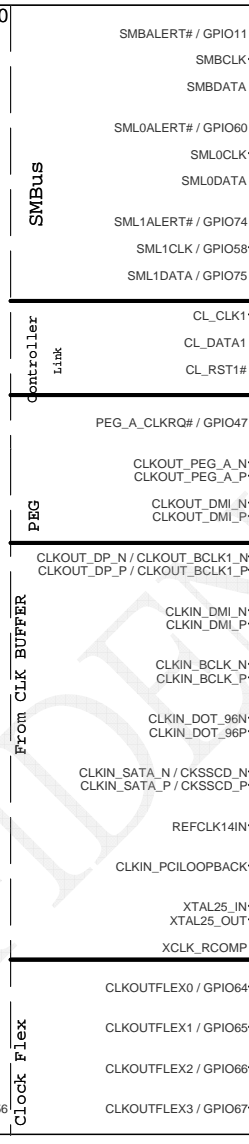
CLKOUTFLEX1 / GPIO65

CLKOUTFLEX2 / GPIO66

CLKOUTFLEX3 / GPIO67

PEG_B_CLKREQ# / GPIO56

IBEXPEAK-M_FCBGA107

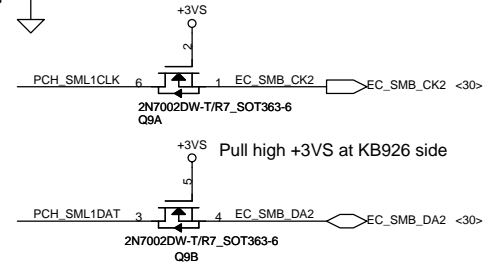
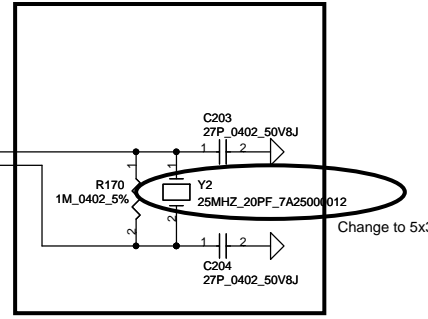


0602 GPIO65 no use
PULL HIGH:PVT
PULL DOWN:DVT

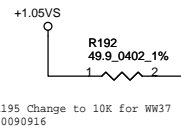
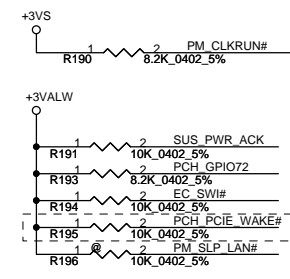
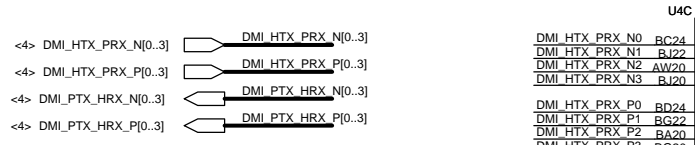
GPIO66 6L/8L	
SATA register spare	
GPIO66	0 6L *
	1 8L

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics



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Date:	Friday, July 02, 2010	Sheet	14	of	48

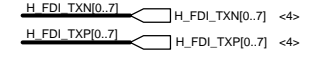


U4C

REV1.0

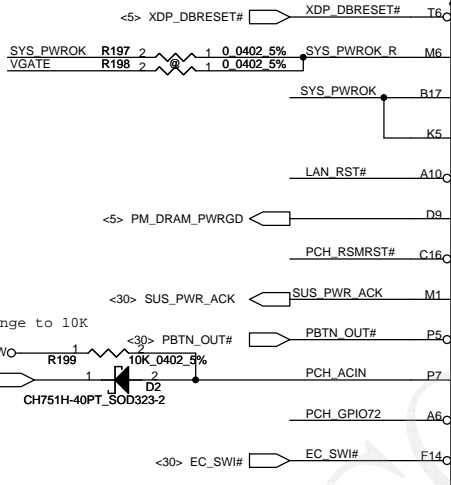
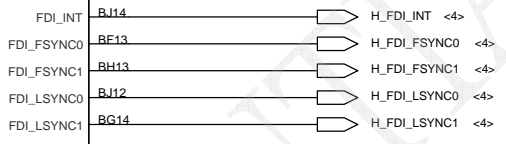
DMI HTX PRX N0	BC24	DMI0RXN
DMI HTX PRX N1	BJ22	DMI1RXN
DMI HTX PRX N2	AW20	DMI2RXN
DMI HTX PRX N3	BJ20	DMI3RXN
DMI HTX PRX P0	BD24	DMI0RXP
DMI HTX PRX P1	BC22	DMI1RXP
DMI HTX PRX P2	BA20	DMI2RXP
DMI HTX PRX P3	BG20	DMI3RXP
DMI PTX HRX N0	BE22	DMI0TXN
DMI PTX HRX N1	BE21	DMI1TXN
DMI PTX HRX N2	BD20	DMI2TXN
DMI PTX HRX N3	BE18	DMI3TXN
DMI PTX HRX P0	BD22	DMI0TXP
DMI PTX HRX P1	BH21	DMI1TXP
DMI PTX HRX P2	BC20	DMI2TXP
DMI PTX HRX P3	BD18	DMI3TXP

FDI_RXN0	BA18	H_FDI_TXN0
FDI_RXN1	BA17	H_FDI_TXN1
FDI_RXN2	BD16	H_FDI_TXN2
FDI_RXN3	BJ16	H_FDI_TXN3
FDI_RXN4	BA16	H_FDI_TXN4
FDI_RXN5	BE14	H_FDI_TXN5
FDI_RXN6	BA14	H_FDI_TXN6
FDI_RXN7	BC12	H_FDI_TXN7
FDI_RXP0	BB18	H_FDI_TXP0
FDI_RXP1	BE17	H_FDI_TXP1
FDI_RXP2	BC16	H_FDI_TXP2
FDI_RXP3	BG16	H_FDI_TXP3
FDI_RXP4	AW16	H_FDI_TXP4
FDI_RXP5	BD14	H_FDI_TXP5
FDI_RXP6	BB14	H_FDI_TXP6
FDI_RXP7	BD12	H_FDI_TXP7



DMI

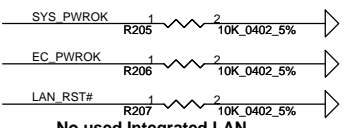
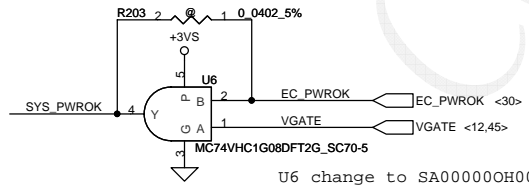
FDI



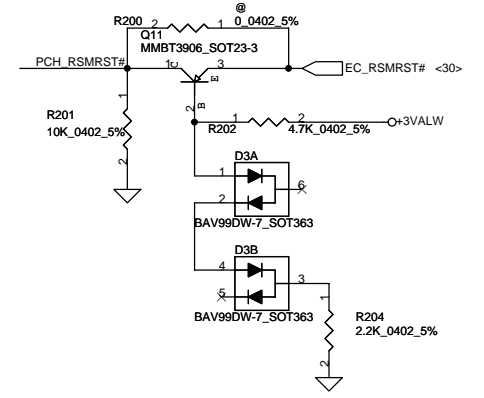
SYS_RESET#	T6	WAKE#	J12	PCH_PCIE_WAKE#	PCH_PCIE_WAKE# <26,27>
SYS_PWROK	M6	CLKRUN# / GPIO32	Y1	PM_CLKRUN#	PM_CLKRUN# <30>
PWROK	R17	SUS_STAT# / GPIO61	P8	PCH_GPIO61	@ PAD T7
MEPWROK	K5	SUSCLK / GPIO62	F3	PCH_SUSCLK	<30> 32.768KHZ ouput for remove EC crystal 20091103
LAN_RST#	A10	SLP_S5# / GPIO63	E4	PM_SLP_S5#	<30>
DRAMPWROK	D9	SLP_S4#	H7	PM_SLP_S4#	<30>
RSMRST#	C16	SLP_S3#	E12	PM_SLP_S3#	<30>
SUS_PWR_ACK	M1	SLP_M#	K8	PM_SLP_M#	@ PAD T9
SUS_PWR_DN_ACK / GPIO30		TP23	N2	PM_SLP_DS#	@ PAD T10
PWRBTN#	P5	PMSYNCH	BJ10	H_PM_SYNC	<5>
PCH_ACIN	P7	SLP_LAN# / GPIO29	E6	PM_SLP_LAN#	
ACPRESENT / GPIO31					
BATLOW# / GPIO72	A6				
PCH_GPIO72	A6				
EC_SWI#	F14				

System Power Management

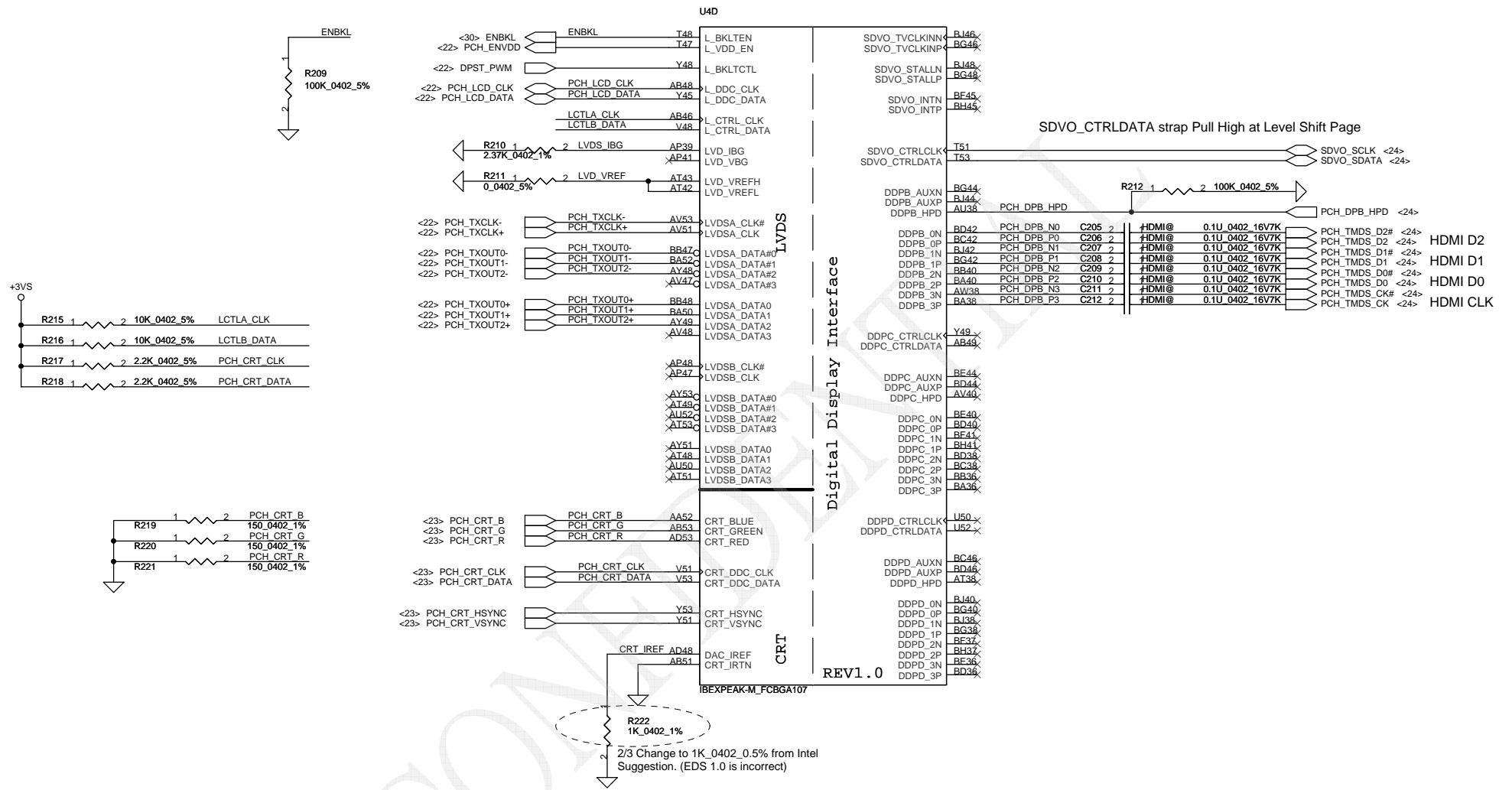
IBEXPEAK-M_FCBGA107



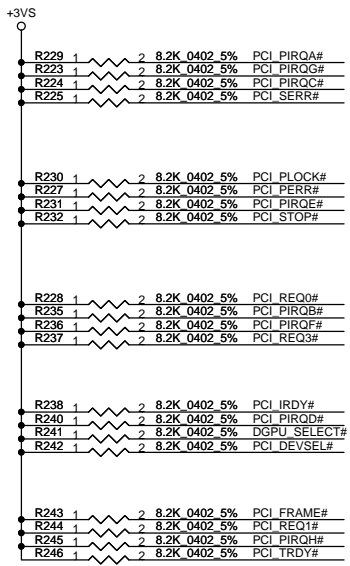
No used Integrated LAN, connecting LAN_RST# to GND



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Document Number	401939	Rev	A	Date	Friday, July 02, 2010
Sheet	15	of	48		



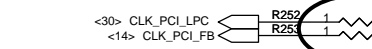
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Date:	Friday, July 02, 2010	Sheet	16	of	48



A16 swap override Strap/Top-Block Swap Override jumper

Low=A16 swap override/Top-Block Swap Override enabled
High=Default *

PCI_GNT3#

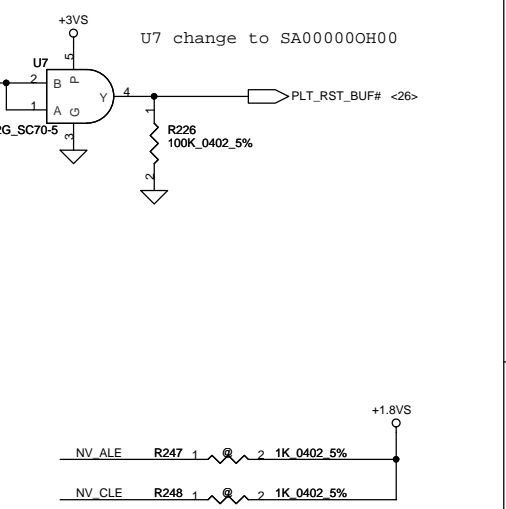
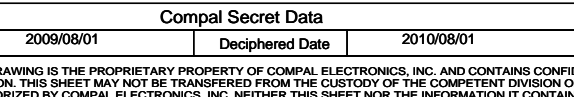
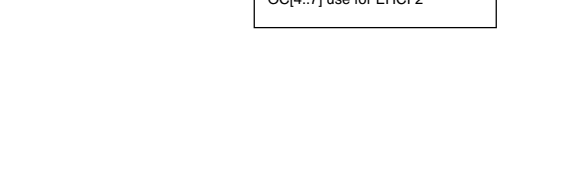
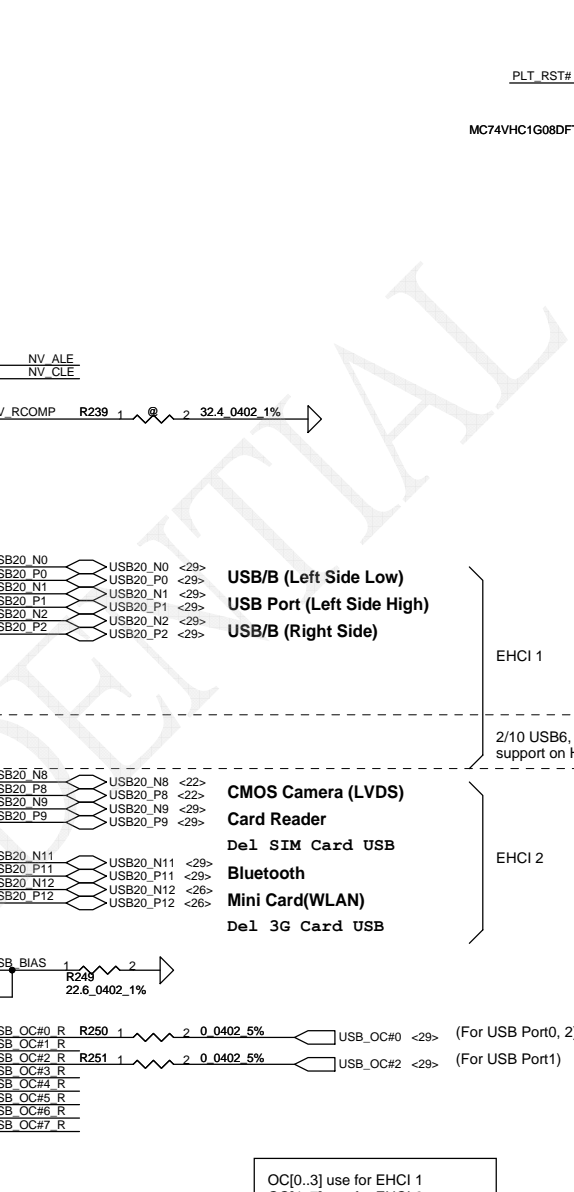
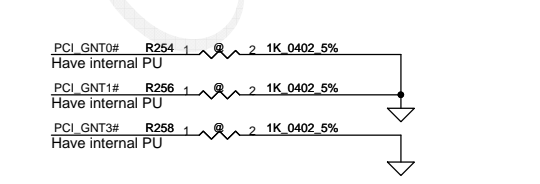
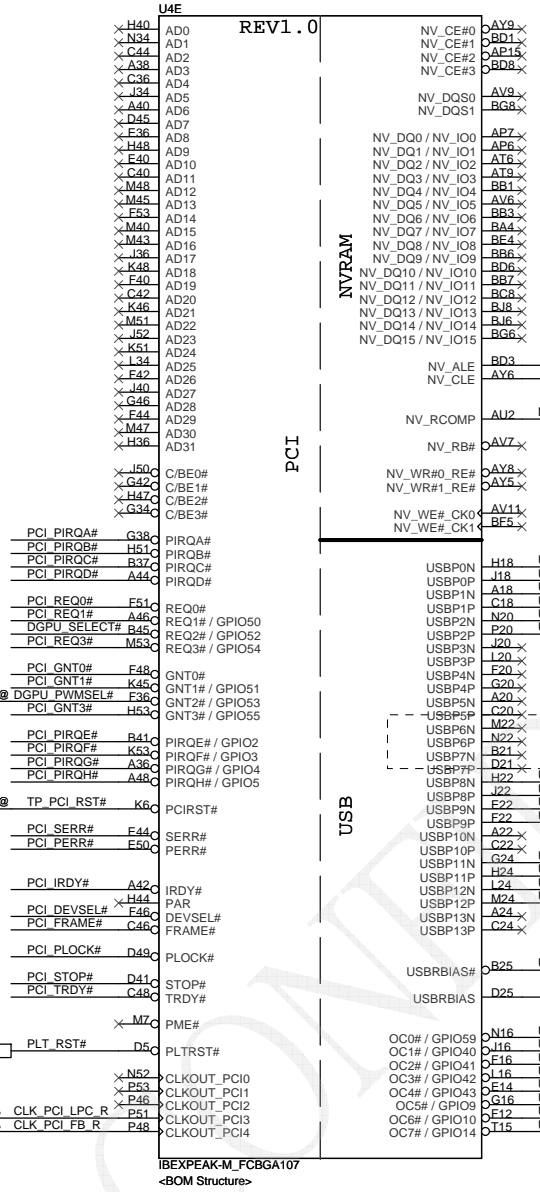


2008/1/6 2009MOW01 change to 22 ohm

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper

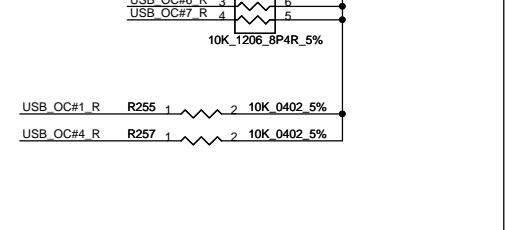
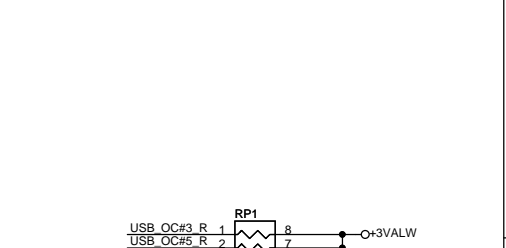
Low = A16 swap
High = Default



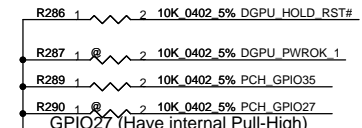
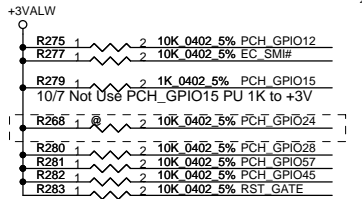
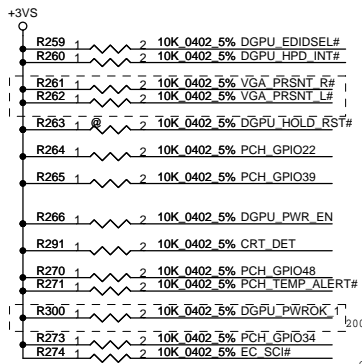
Intel Anti-Theft Technology	
NV_ALE	High=Enabled Low=Disableable(floating) *
DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH Set to Vss when LOW

NV_ALE
Enable Intel Anti-Theft Technology : 8.2K PU to +3VS

Disable Intel Anti-Theft Technology : floating(internal PD)
NV_CLE
DMI termination voltage.
weak internal PU, don't PD



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Date:	Friday, July 02, 2010	Sheet	17	of	48



High: VCCVRM VR Enable
Low: VCCVRM VR Disable

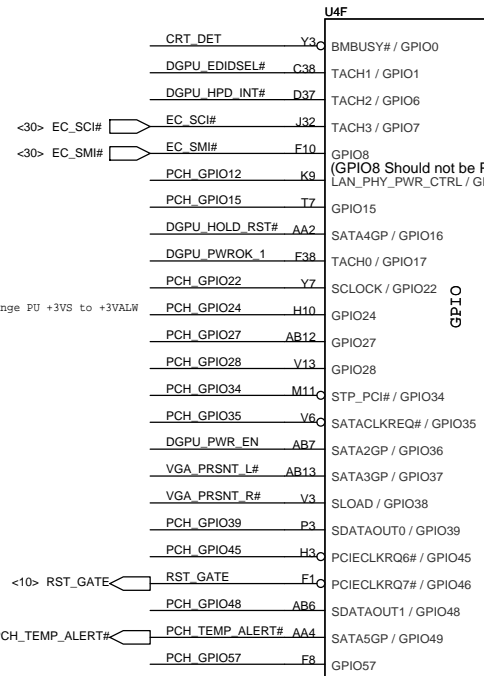
	GPIO19	GPIO37
	PCH_GPIO19	VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	0

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H: On-Die voltage regulator enable
L: On-Die PLL Voltage Regulator disable

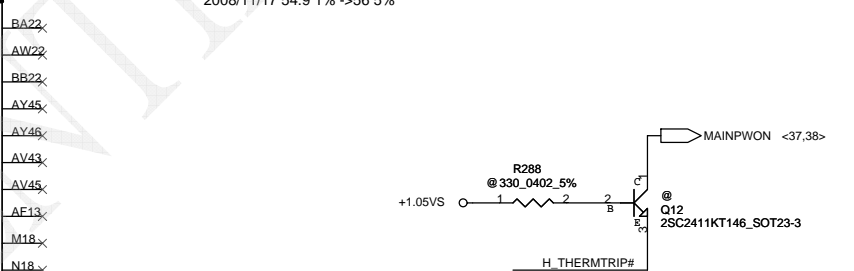
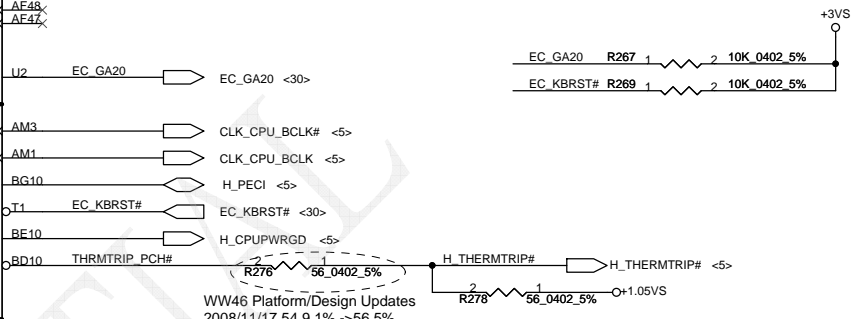
GPIO8
This signal has a weak internal pull up
can't Pull low

GPIO15
L: Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
H: Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality
It have weak internal PU 20K



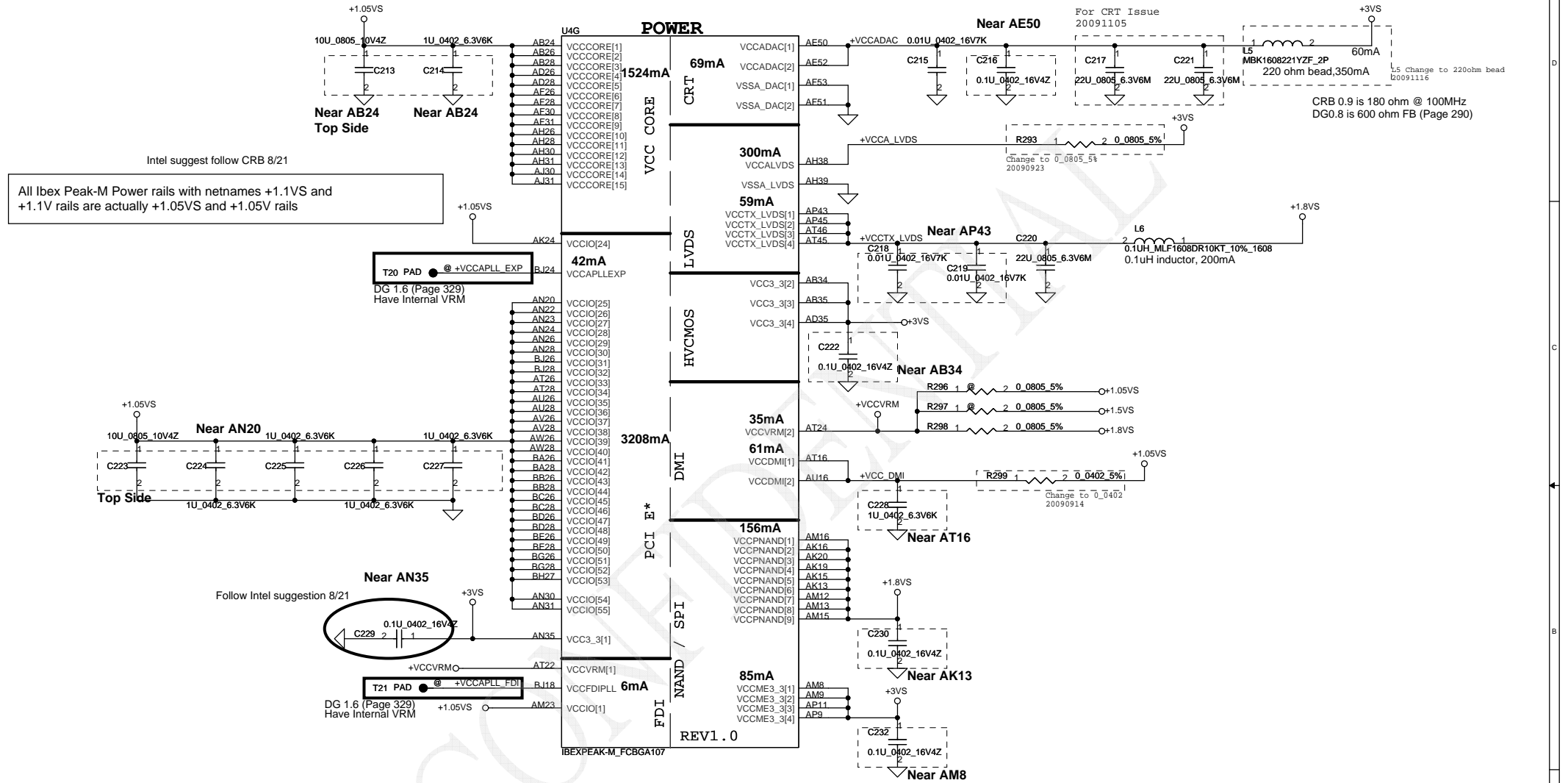
REV1.0

IBEXPEAK-M_FCBGA107



INIT3_3V#
This signal has weak internal PU, can't pull low

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				Customer	401939
				Date:	Friday, July 02, 2010
				Sheet	18 of 48



All IbeX Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

Intel suggest follow CRB 8/21

T20 PAD @ +VCCAPLL EXP
 DG 1.6 (Page 329)
 Have Internal VRM

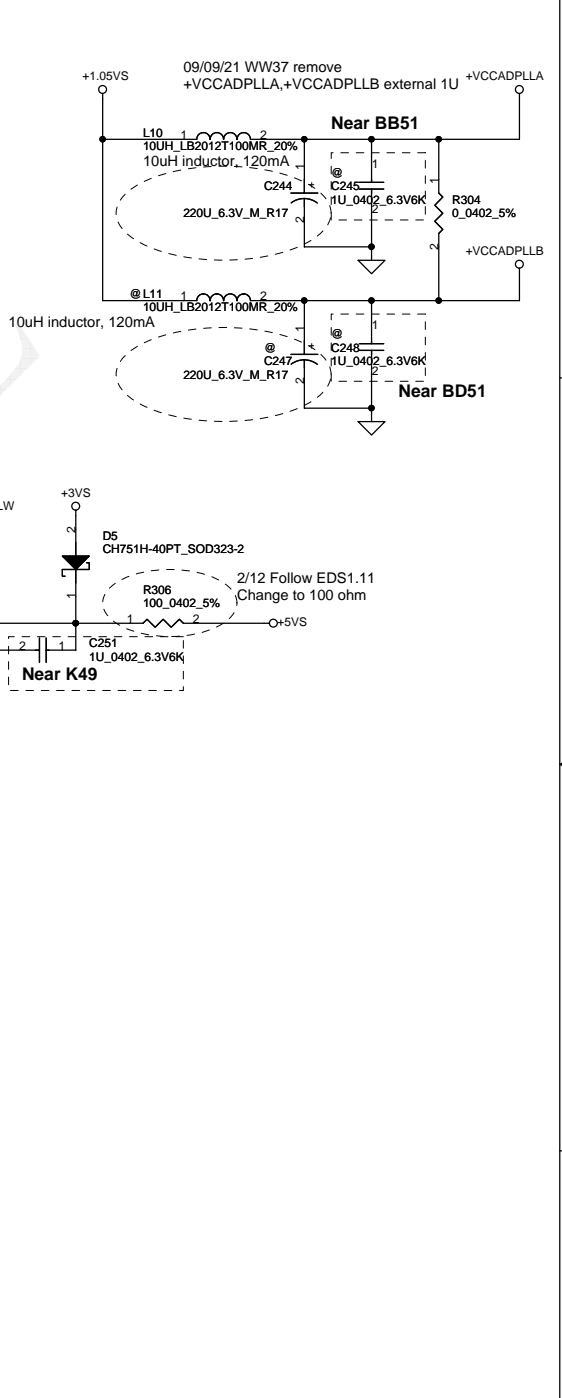
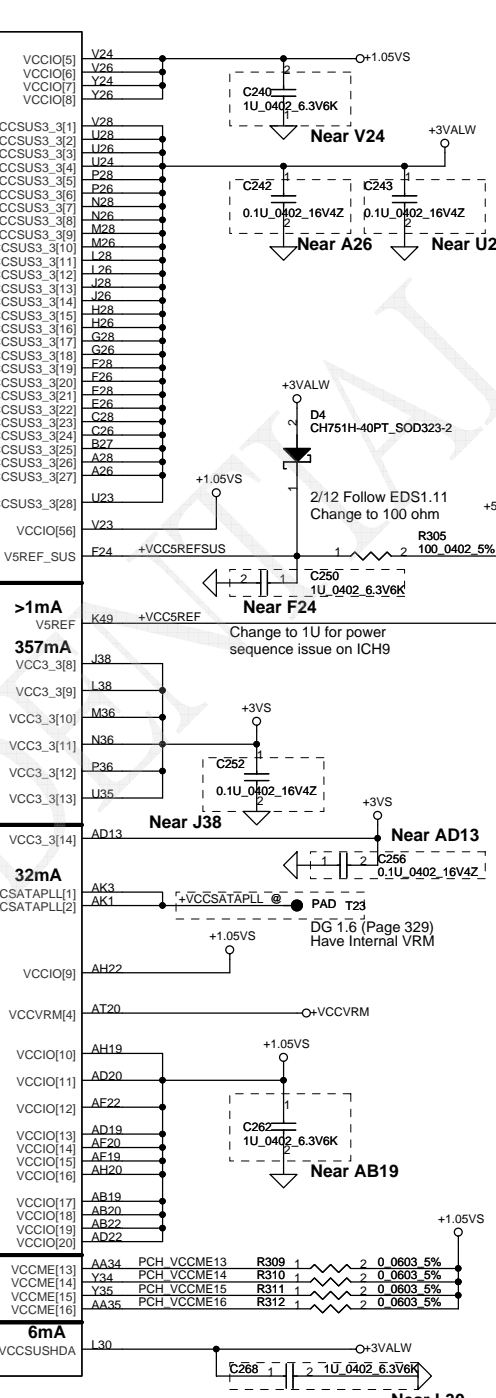
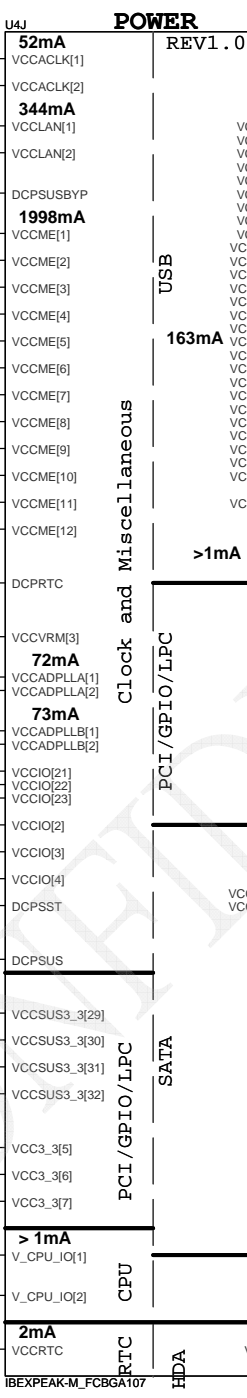
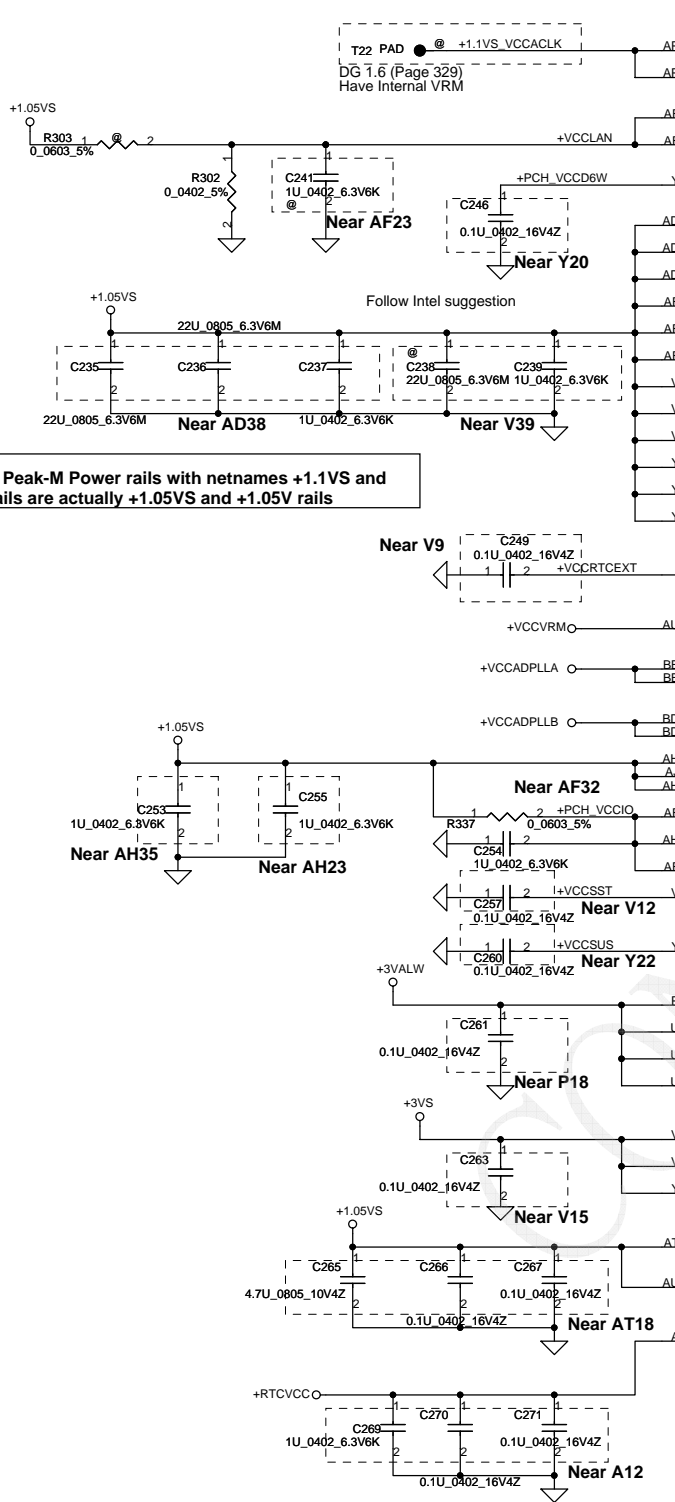
Follow Intel suggestion 8/21

Near AN35
 0.1U_0402_16V4Z
 T21 PAD @ +VCCAPLL FDI
 DG 1.6 (Page 329)
 Have Internal VRM

POWER	
VCC CORE	1524mA
CRT	69mA
VCC LVDS	300mA
HVCMOS	59mA
DMI	35mA
PCI E*	61mA
NAND / SPI	156mA
FDI	85mA

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Customer	401939	Date:	Friday, July 02, 2010	Sheet	19 of 48

All Ibox Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails



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Customer	401939	Date	Friday, July 02, 2010	Sheet	20 of 48

U4I

AY7	VSS159	H49
B11	VSS160	H5
B15	VSS161	J24
B19	VSS162	K11
B23	VSS163	K43
B31	VSS164	K47
B35	VSS165	K7
B39	VSS166	L14
B43	VSS167	L2
B47	VSS168	L18
B7	VSS169	L22
BG12	VSS170	L32
BB12	VSS171	L36
BB16	VSS172	L40
BB20	VSS173	L52
BB24	VSS174	M12
BB30	VSS175	M16
BB34	VSS176	M20
BB38	VSS177	M38
BB42	VSS178	M34
BB49	VSS179	M38
BB5	VSS180	M42
BC10	VSS181	M46
RC14	VSS182	M34
RC18	VSS183	M42
RC22	VSS184	M46
RC32	VSS185	M42
RC36	VSS186	M46
RC40	VSS187	M42
RC44	VSS188	M46
RC52	VSS189	M42
RH9	VSS190	M46
RD48	VSS191	M42
BD49	VSS192	M46
RD5	VSS193	M42
RE12	VSS194	M46
RE16	VSS195	M42
RE20	VSS196	M46
RE24	VSS197	M42
RE30	VSS198	M46
RE34	VSS199	M42
RE38	VSS200	M46
RE42	VSS201	M42
RE46	VSS202	M46
RE48	VSS203	M42
RE50	VSS204	M46
RE6	VSS205	M42
RE8	VSS206	M46
RF3	VSS207	M42
RF49	VSS208	M46
RF51	VSS209	M42
RG18	VSS210	M46
RG24	VSS211	M42
RG4	VSS212	M46
RG50	VSS213	M42
RH11	VSS214	M46
RH15	VSS215	M42
RH19	VSS216	M46
RH23	VSS217	M42
RH31	VSS218	M46
RH35	VSS219	M42
RH39	VSS220	M46
RH43	VSS221	M42
RH47	VSS222	M46
RH7	VSS223	M42
C12	VSS224	M46
C50	VSS225	M42
D51	VSS226	M46
E12	VSS227	M42
E16	VSS228	M46
E20	VSS229	M42
E24	VSS230	M46
E30	VSS231	M42
E34	VSS232	M46
E38	VSS233	M42
E42	VSS234	M46
E46	VSS235	M42
E48	VSS236	M46
E6	VSS237	M42
E8	VSS238	M46
F49	VSS239	M42
F5	VSS240	M46
G10	VSS241	M42
G14	VSS242	M46
G18	VSS243	M42
G2	VSS244	M46
G22	VSS245	M42
G32	VSS246	M46
G36	VSS247	M42
G40	VSS248	M46
G44	VSS249	M42
G52	VSS250	M46
AF39	VSS251	M42
H16	VSS252	M46
H20	VSS253	M42
H30	VSS254	M46
H34	VSS255	M42
H38	VSS256	M46
H42	VSS257	M42
	VSS258	M46

REV1.0

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U4H

AB16	VSS0	AK30
AA19	VSS1	AK31
AA20	VSS2	AK32
AA22	VSS3	AK34
AA19	VSS4	AK35
AA24	VSS5	AK38
AA26	VSS6	AK43
AA28	VSS7	AK46
AA30	VSS8	AK49
AA31	VSS9	AK5
AA32	VSS10	AK6
AB11	VSS11	AK8
AB15	VSS12	AK9
AB23	VSS13	AL52
AB30	VSS14	AM11
AB31	VSS15	BB44
AB32	VSS16	AD24
AB38	VSS17	AM20
AB43	VSS18	AM22
AB47	VSS19	AM22
AB5	VSS20	AM26
AB8	VSS21	AM28
AC2	VSS22	BA42
AC52	VSS23	AM30
AD11	VSS24	AM31
AD12	VSS25	AM32
AD16	VSS26	AM34
AD23	VSS27	AM35
AD30	VSS28	AM38
AD31	VSS29	AM39
AD32	VSS30	AM42
AD34	VSS31	AM46
AD42	VSS32	AV22
AD44	VSS33	AM49
AD46	VSS34	AM7
AD49	VSS35	AA50
AD7	VSS36	BB10
AE2	VSS37	AN52
AE4	VSS38	AN50
AE12	VSS39	AN52
Y13	VSS40	AP12
AH49	VSS41	AP42
AU4	VSS42	AP46
AE36	VSS43	AP49
AE13	VSS44	AP5
AF45	VSS45	AP8
AF46	VSS46	AR2
AF49	VSS47	AR52
AE5	VSS48	AT11
AE8	VSS49	AT12
AG2	VSS50	AH48
AG52	VSS51	AT32
AH11	VSS52	AT36
AH15	VSS53	AT41
AH16	VSS54	AT47
AH24	VSS55	AT7
AH32	VSS56	AV12
AV18	VSS57	AV16
AH43	VSS58	AV20
AH47	VSS59	AV24
AH7	VSS60	AV30
AJ19	VSS61	AV34
AJ2	VSS62	AV38
AJ20	VSS63	AV42
AJ22	VSS64	AV46
AJ23	VSS65	AV49
AJ26	VSS66	AV5
AJ28	VSS67	AV8
AJ32	VSS68	AW14
AJ34	VSS69	AW18
AJ5	VSS70	AW2
AJ4	VSS71	BF9
AK12	VSS72	AW32
Y28	VSS73	AW36
AN19	VSS74	AW40
AK26	VSS75	AW52
AK22	VSS76	AY11
AK23	VSS77	AY43
AK28	VSS78	AY47
	VSS79	

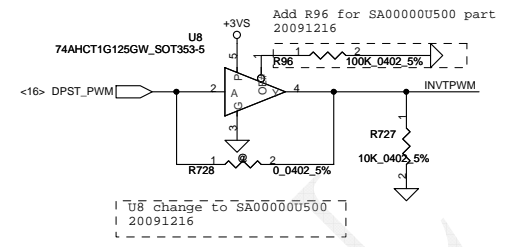
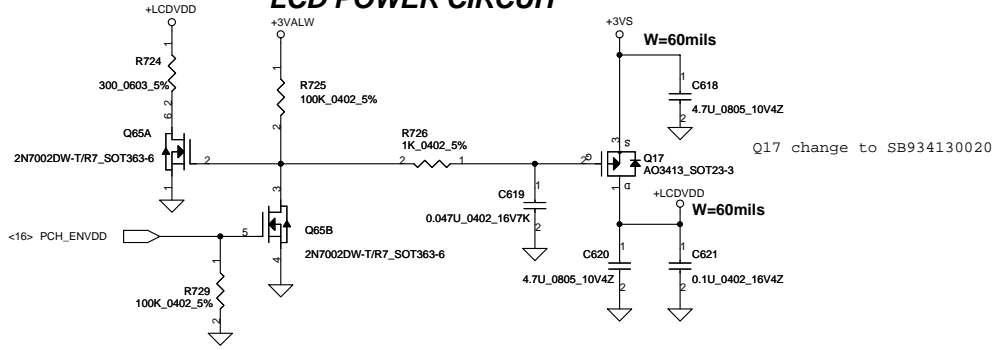
REV1.0

IBEXPEAK-M_FCBGA107

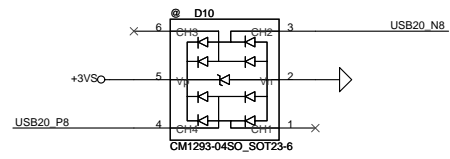
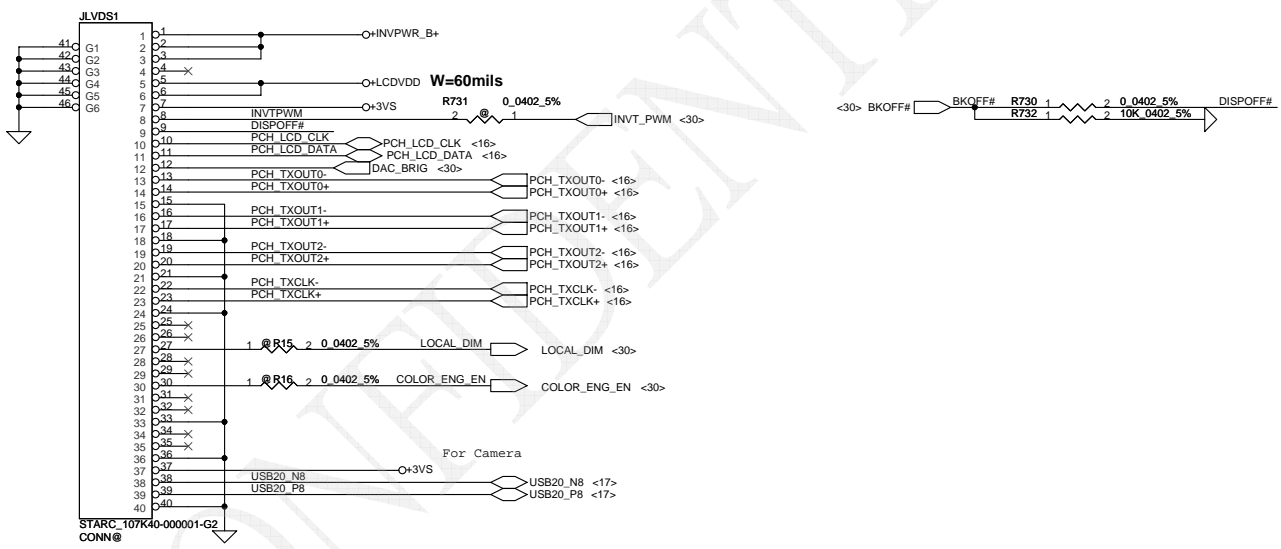
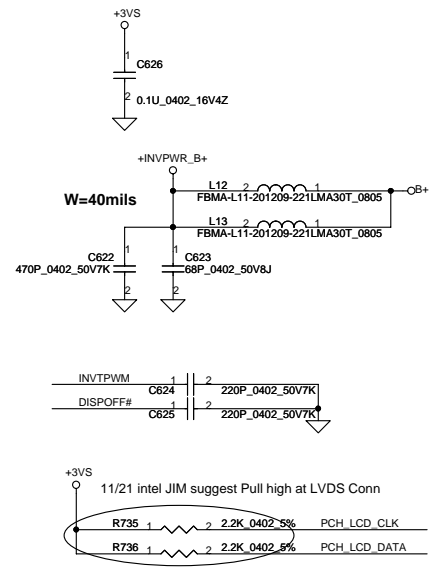
Del PCH XDP

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Document Number	401939	Rev	A	Date	Friday, July 02, 2010
Sheet	21	of	48		

LCD POWER CIRCUIT

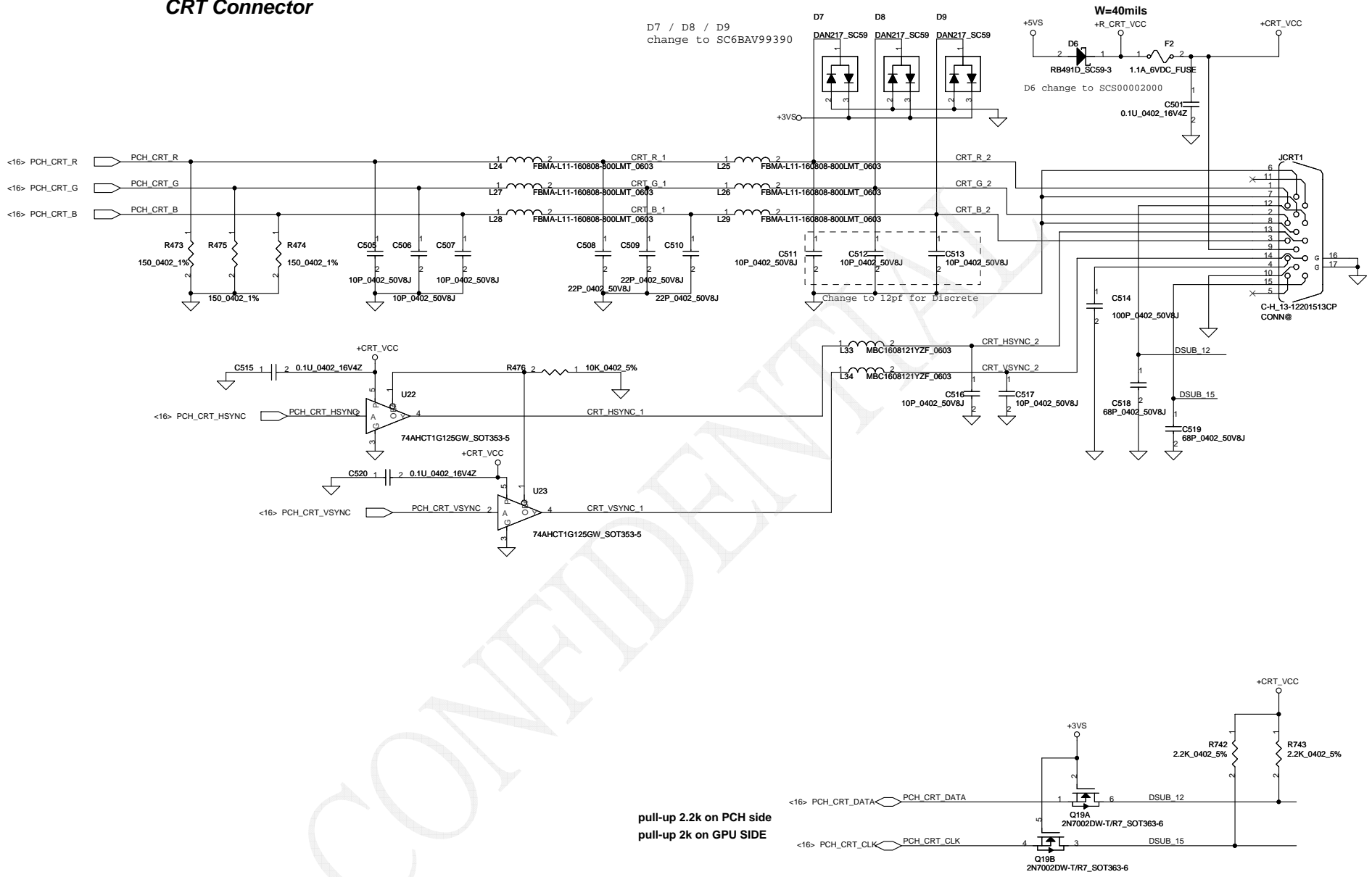


LED PANEL Conn.



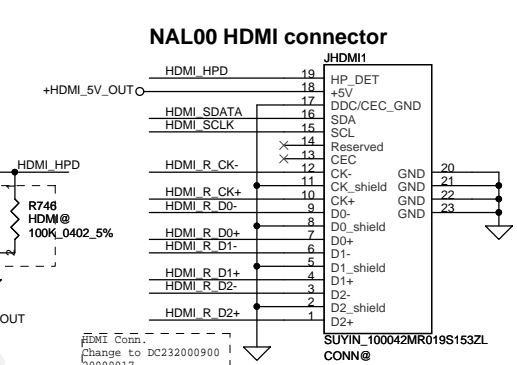
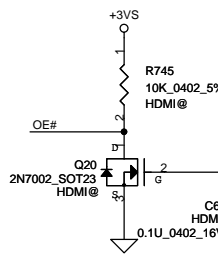
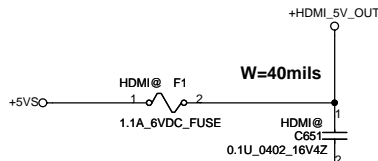
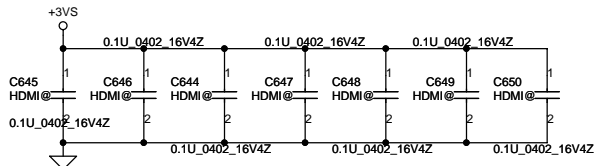
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				401939	A
				Date: Friday, July 02, 2010	Sheet 22 of 48

CRT Connector

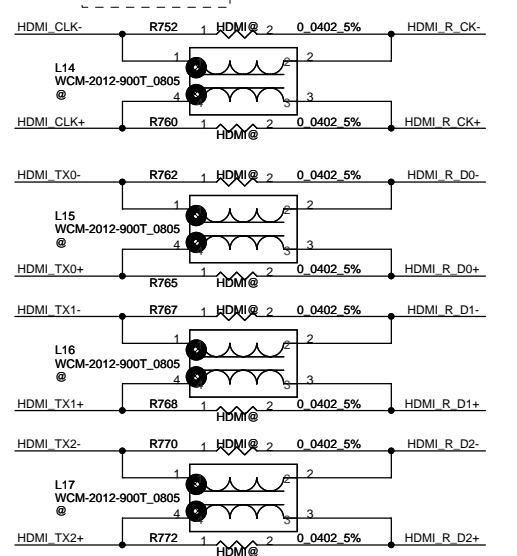
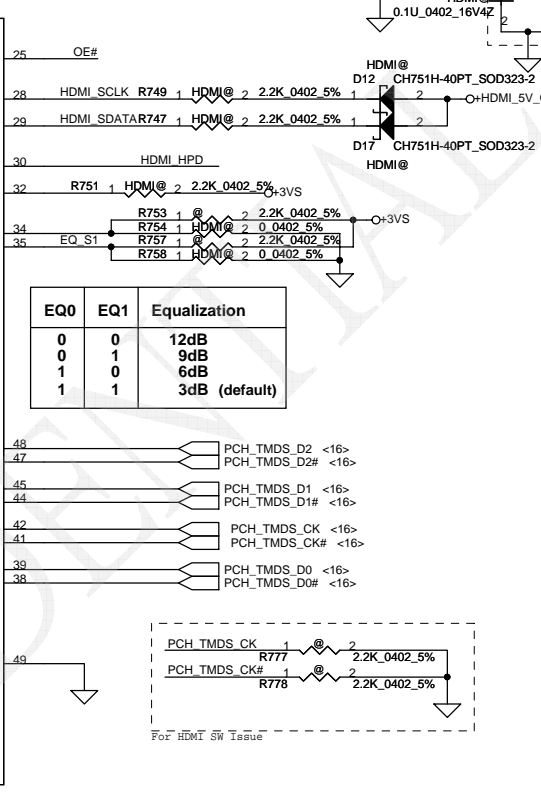
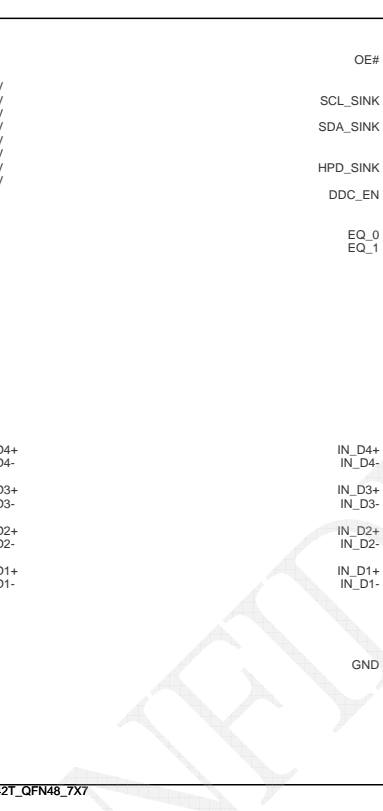
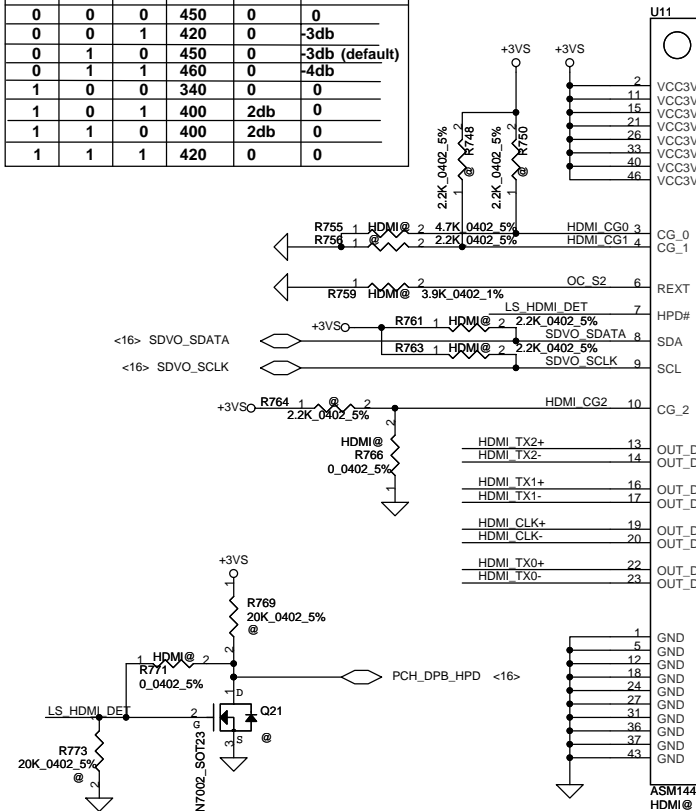


pull-up 2.2k on PCH side
pull-up 2k on GPU SIDE

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				401939	A
Date: Friday, July 02, 2010				Sheet	23 of 48

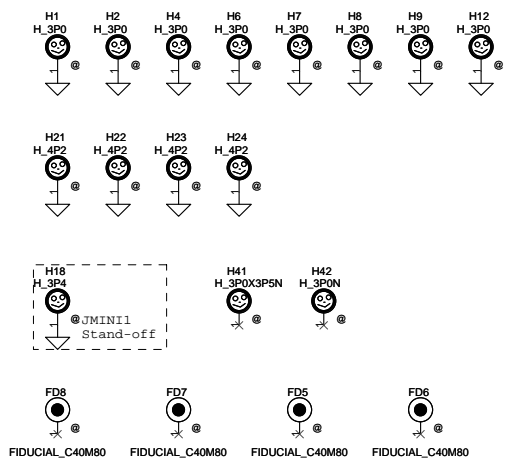


CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

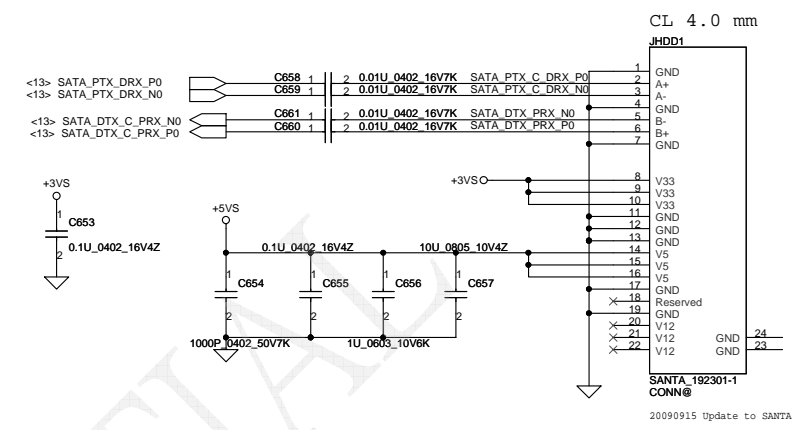


Change to TI P/N: SA00003DS00
20100608

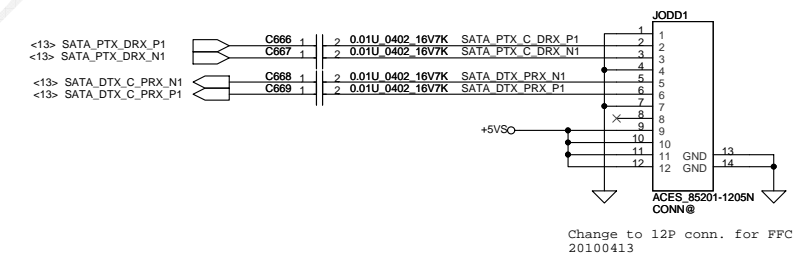
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				401939	A
Date:	Friday, July 02, 2010	Sheet	24	of	48



SATA HDD1 Conn.



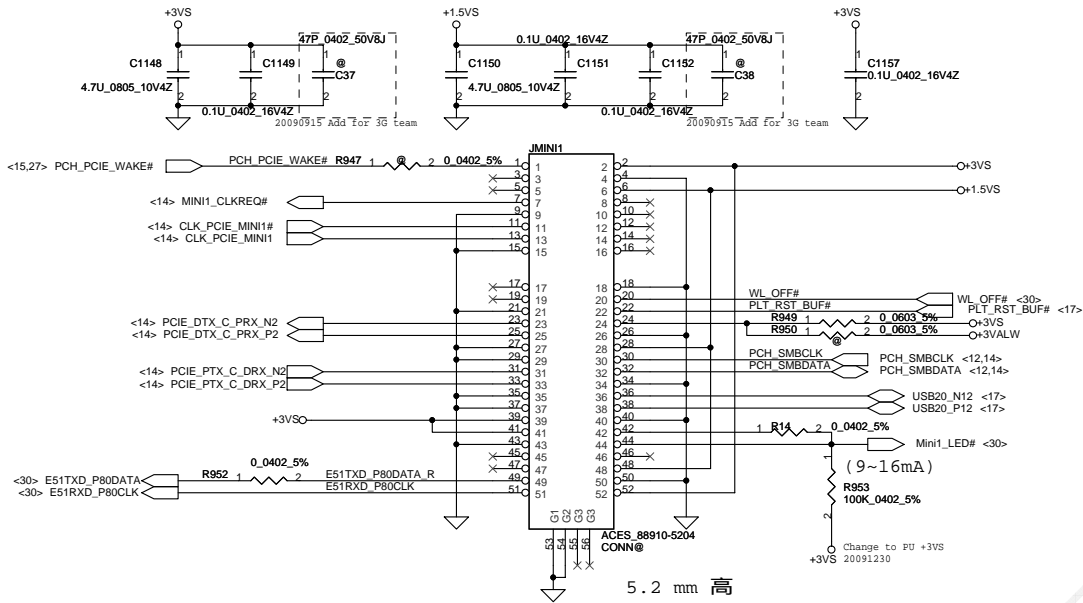
SATA ODD FFC Conn.



CONFIDENTIAL

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						Sheet	25 of 48	

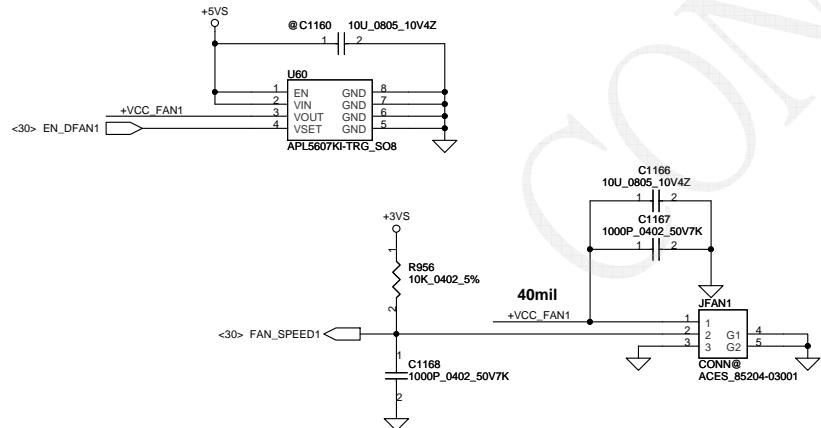
For Wireless LAN



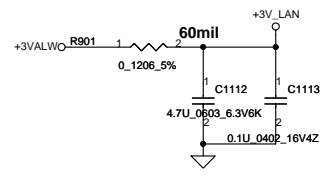
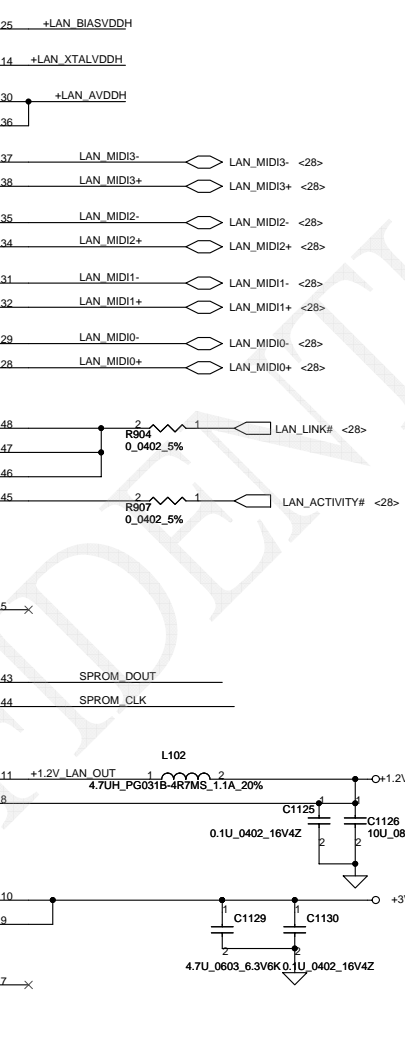
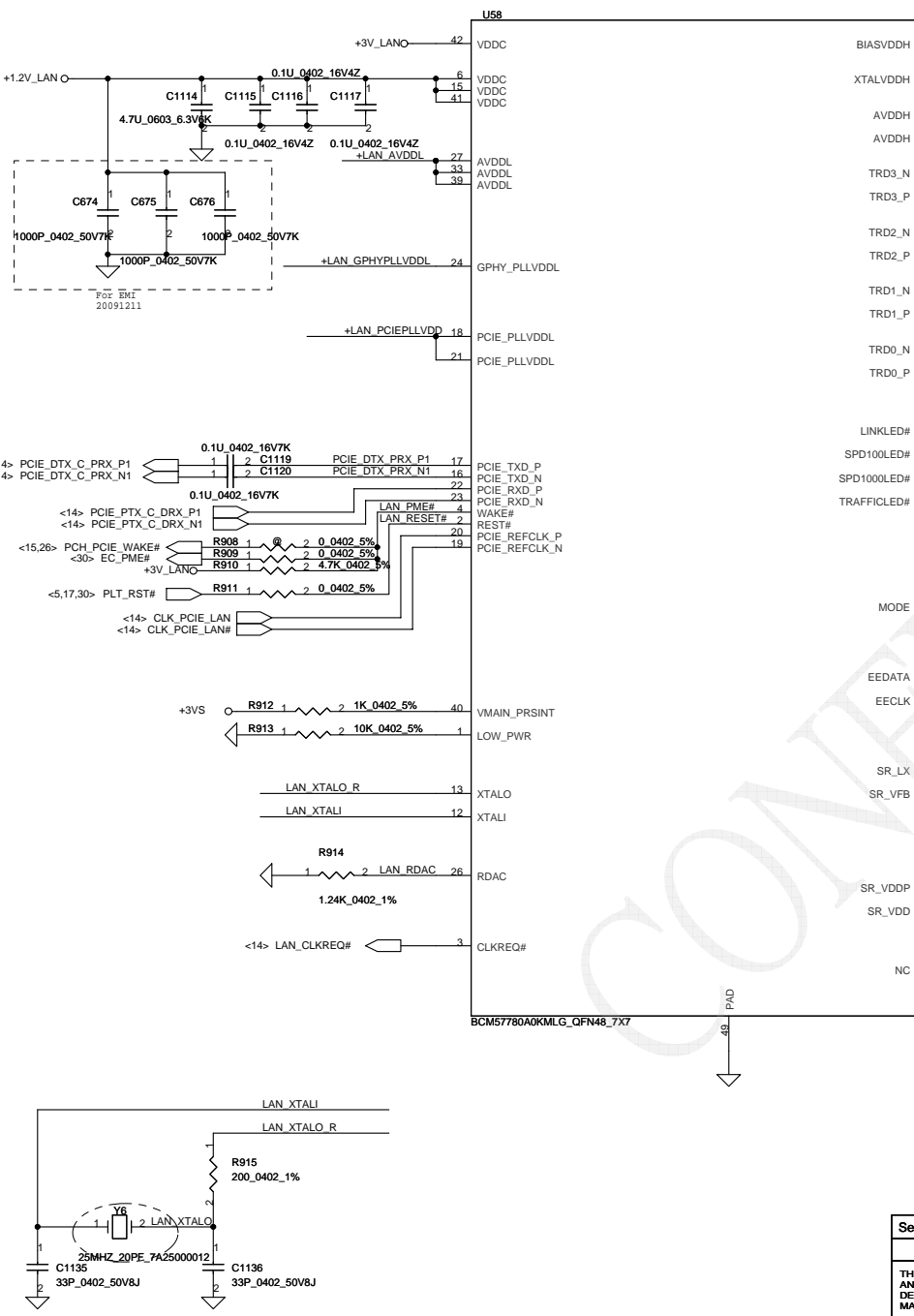
Del 3G / GPS Module Connect

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

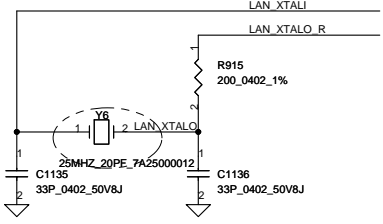
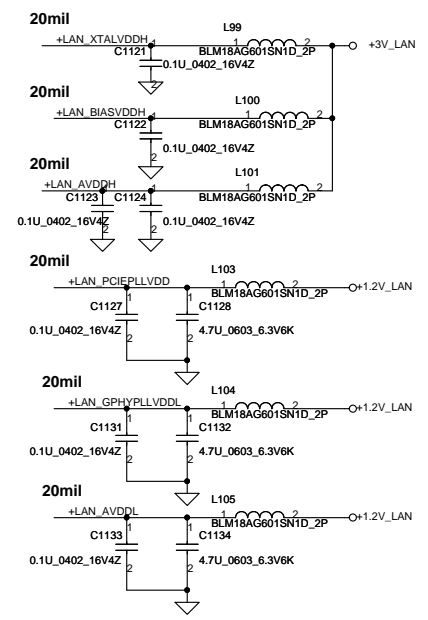
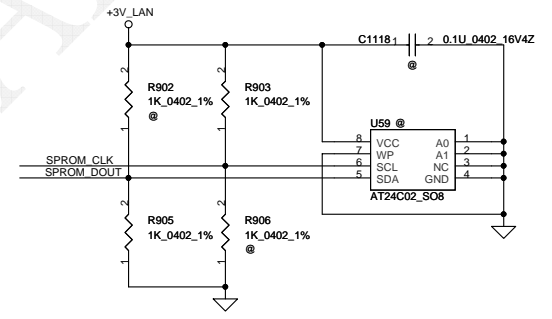
FAN1 Conn



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				Document Number	401939
				Date:	Friday, July 02, 2010
				Sheet	26 of 48

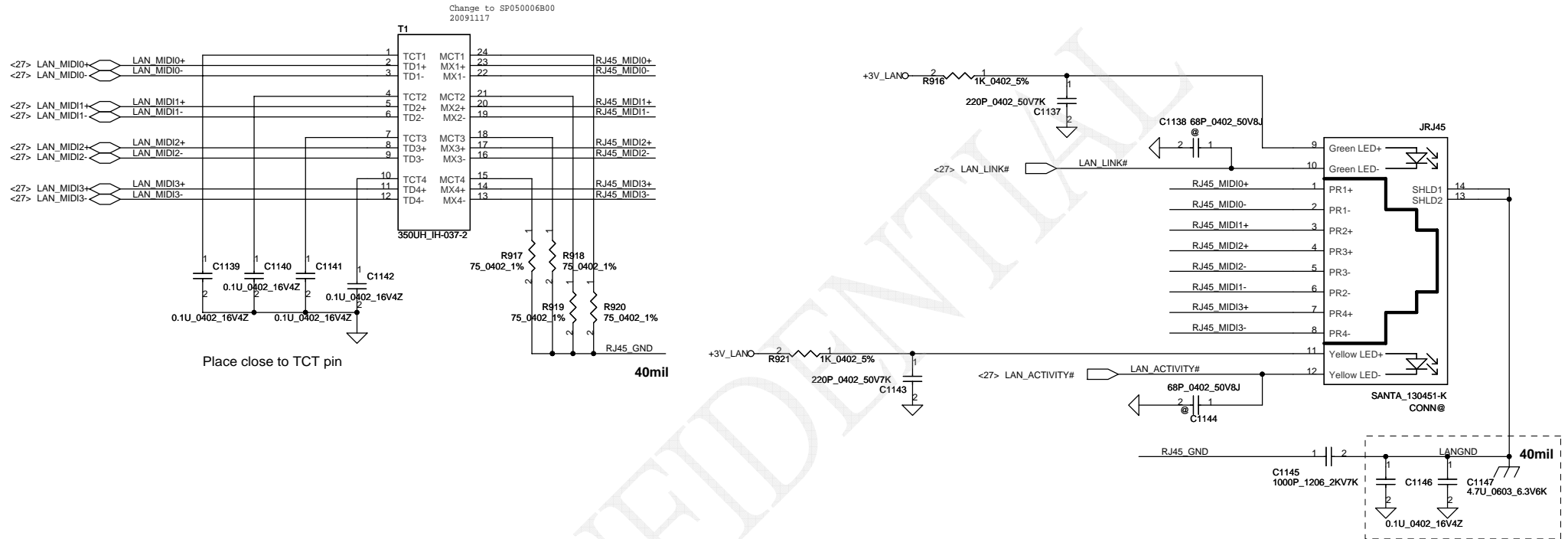


	SPROM_CLK (ECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1



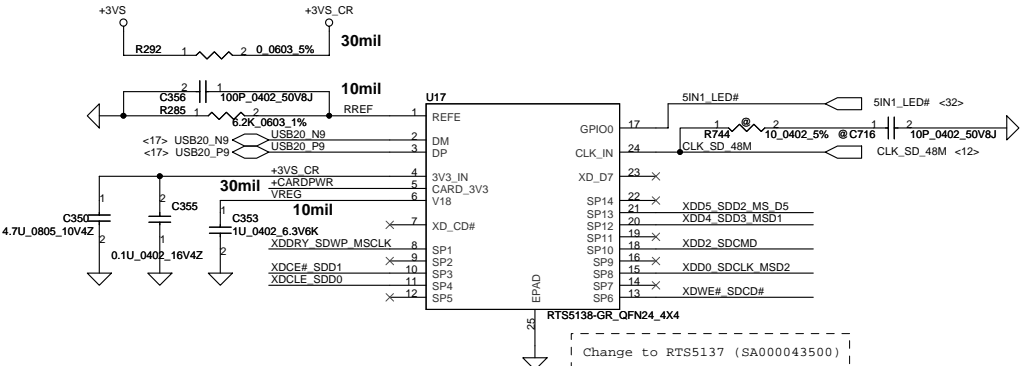
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Customer Document Number			Rev
401939			A
Date: Friday, July 02, 2010			Sheet 27 of 48

LAN Connector

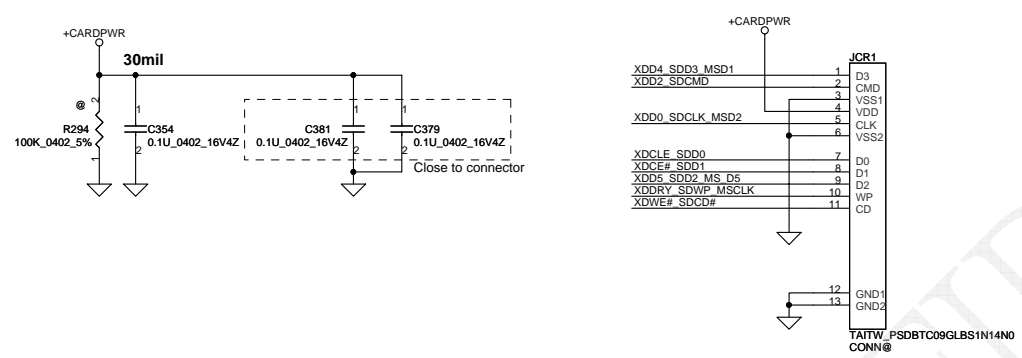


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Document Number	401939	Date	Friday, July 02, 2010	Sheet	28 of 48

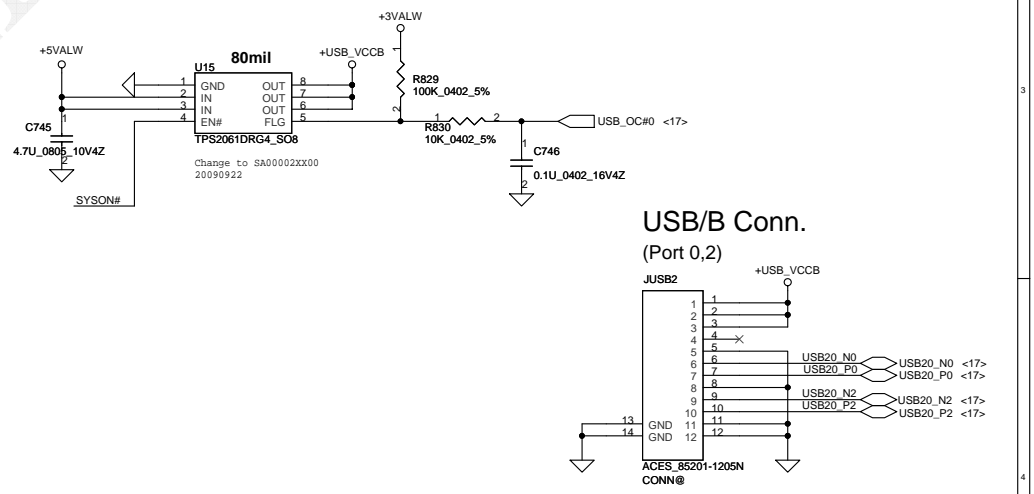
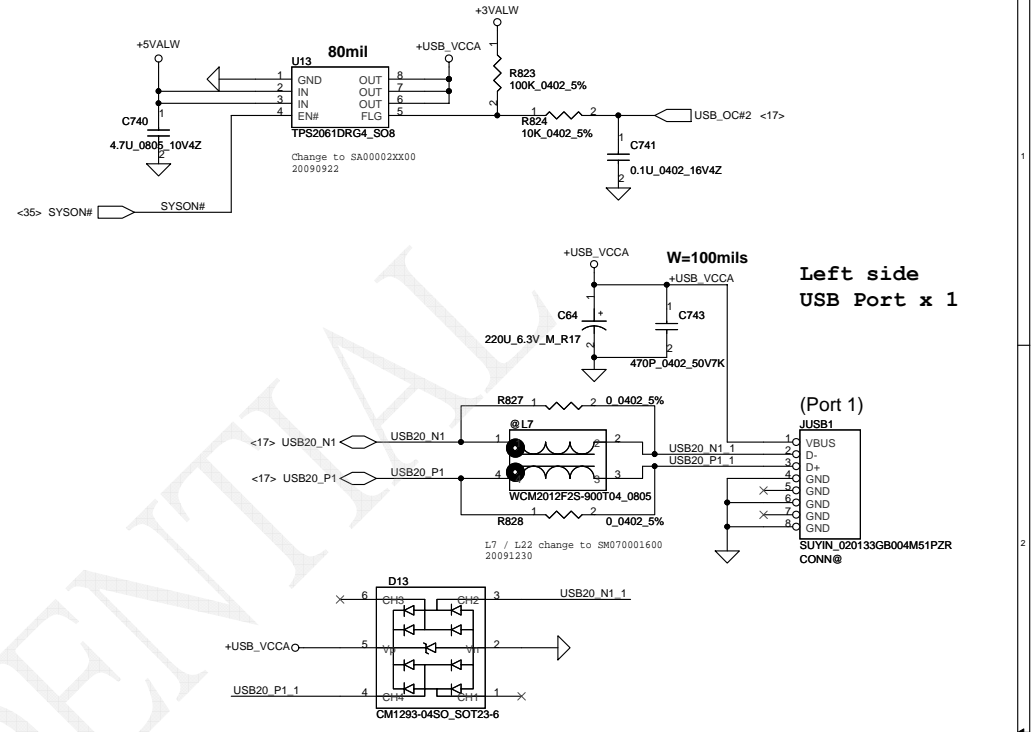
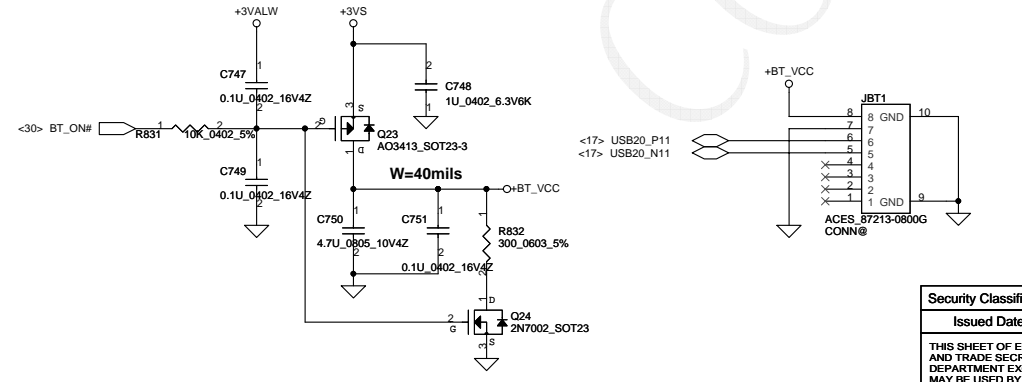
Card Reader RTS5138 / RTS5137 (only SD+MMC function)



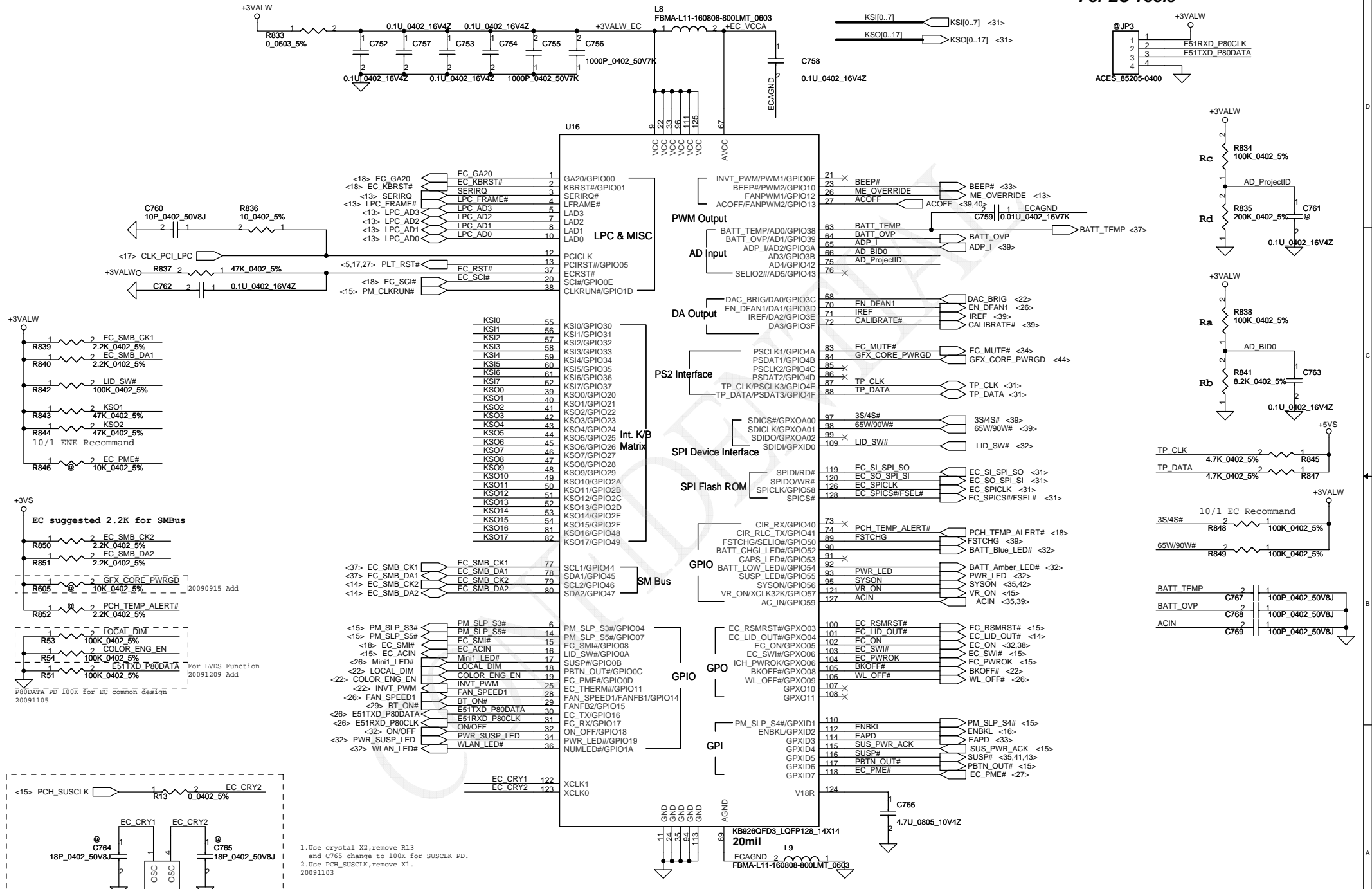
Card Reader Connector



Bluetooth Conn.



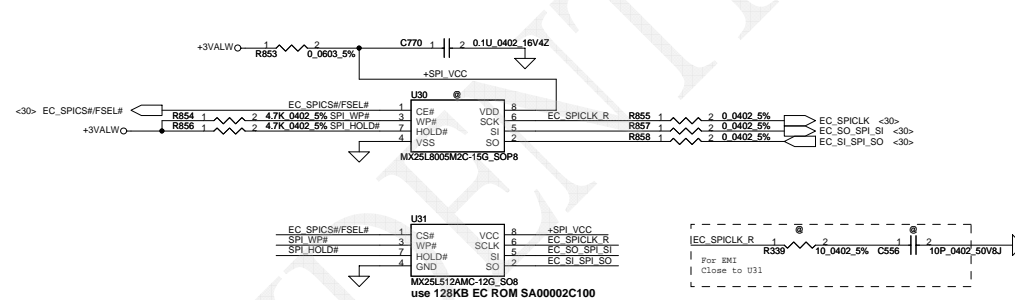
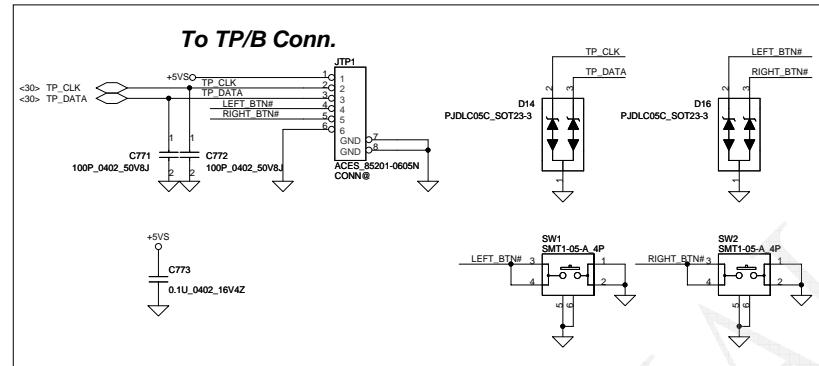
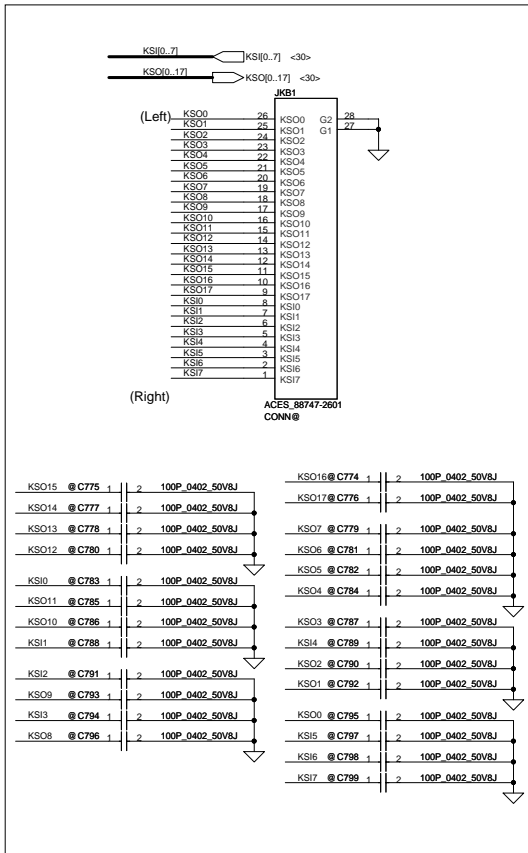
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Document Number	401939	Date	Friday, July 02, 2010	Sheet	29 of 48



1. Use crystal X2, remove R13 and C765 change to 100K for SUSCLK PD.
 2. Use PCH_SUSCLK, remove X1.
 20091103

For EC SUSCLK PD 100K

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Size	Document Number	Date	Friday, July 02, 2010	Sheet	30 of 48
B	401939				

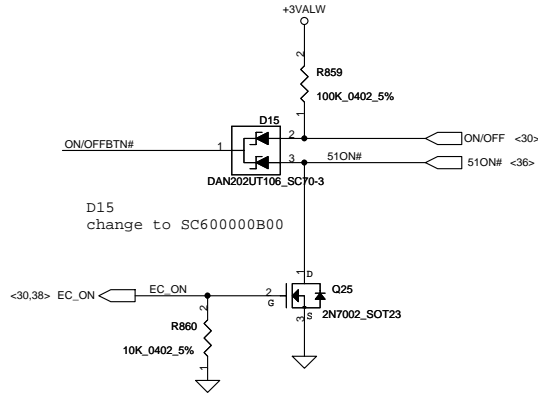


ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

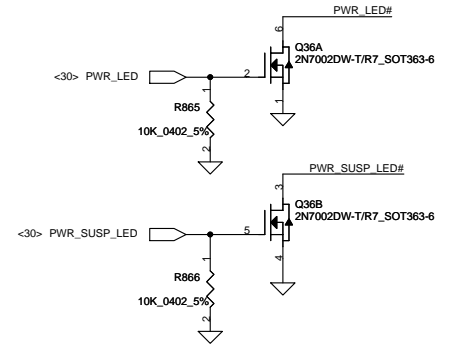
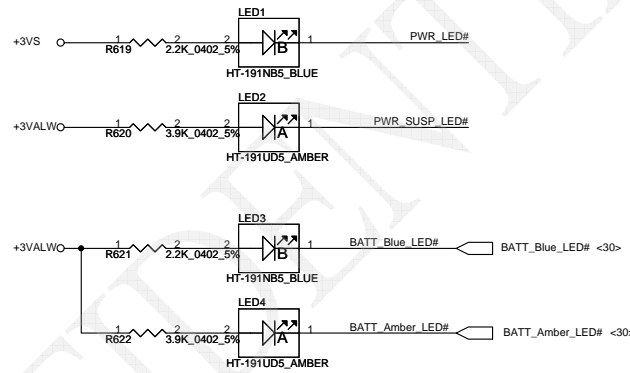
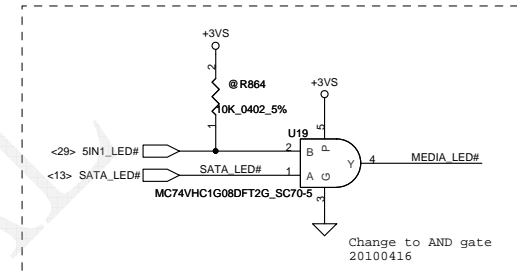
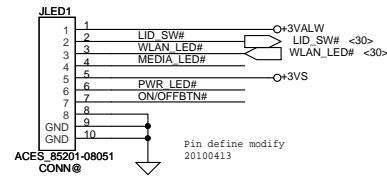
To BTN/B Conn.

	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN#
KSI4	BT_BTN#	Volum down_BTN#
KSI5	Power save_BTN#	

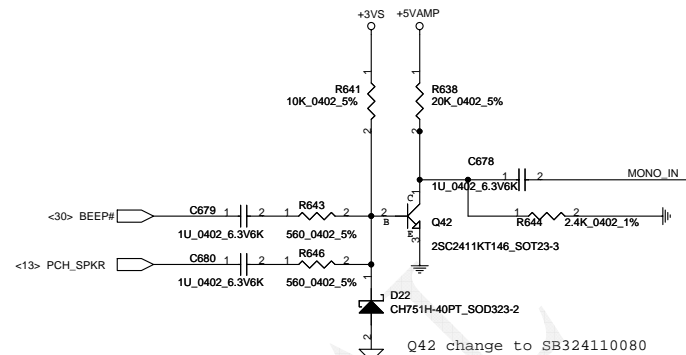
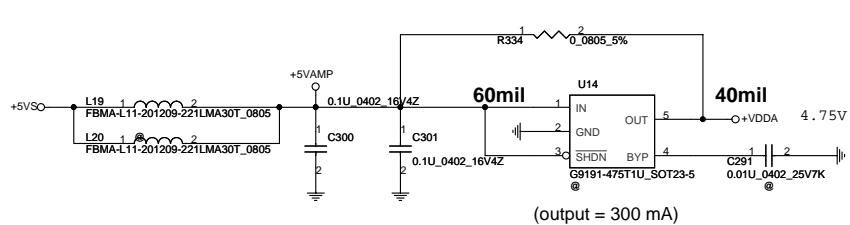
Power Button



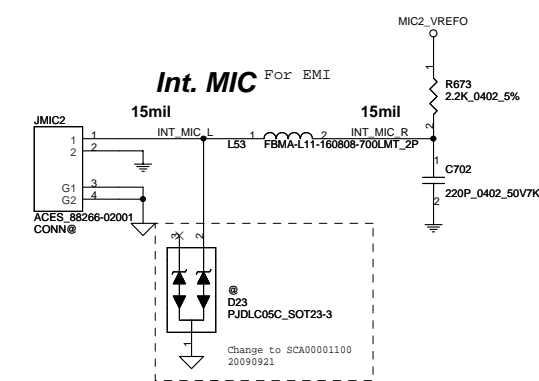
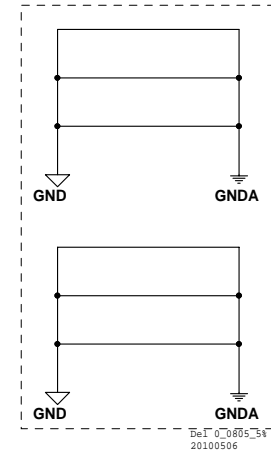
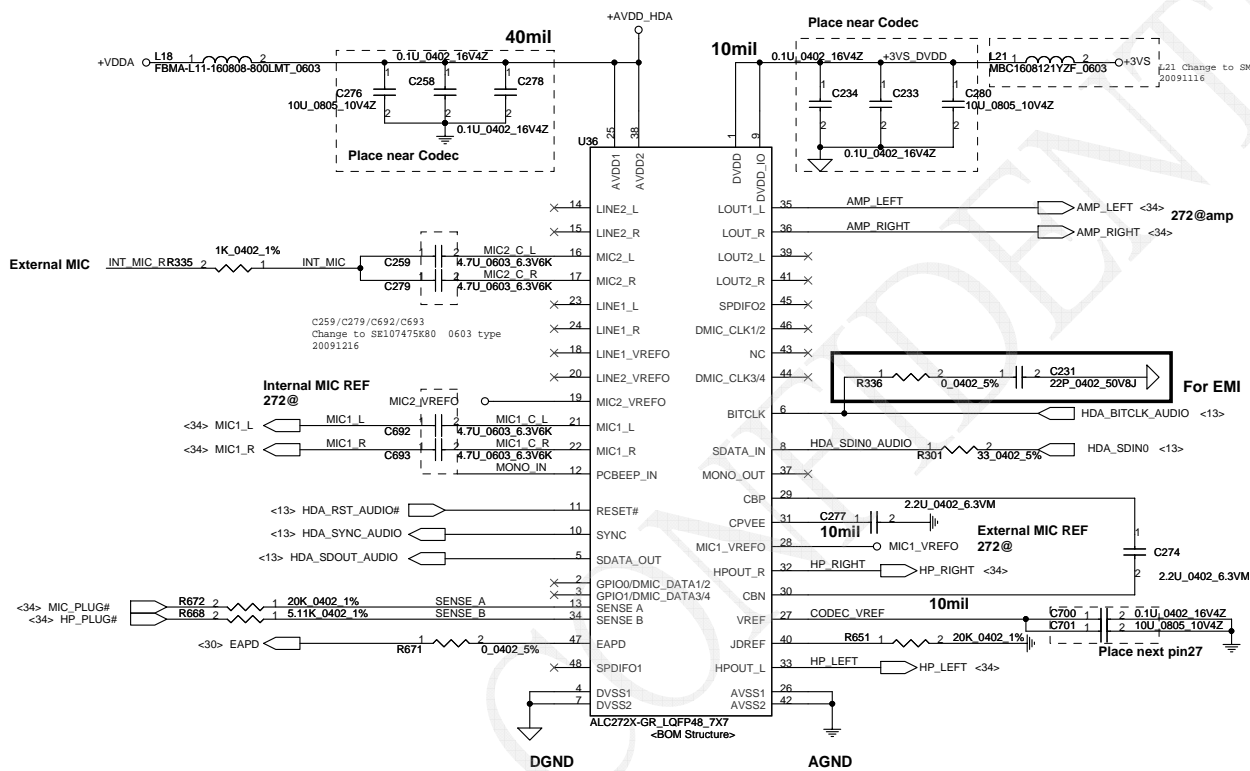
LED/B LEFT



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Date:	Friday, July 02, 2010	Sheet	32	of	48	

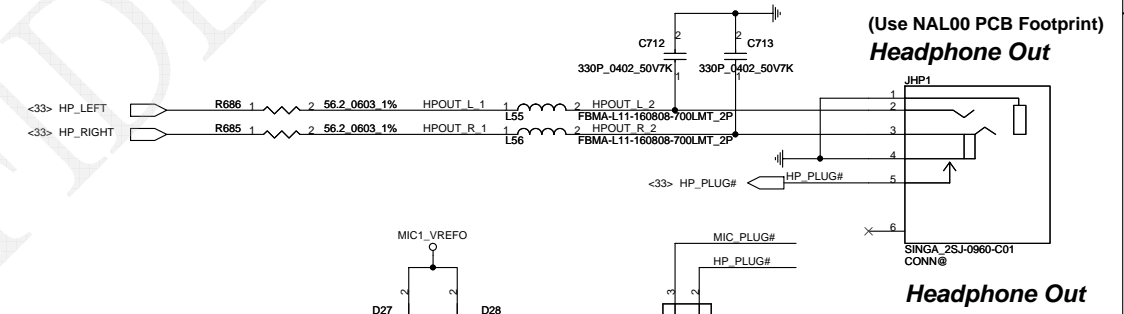
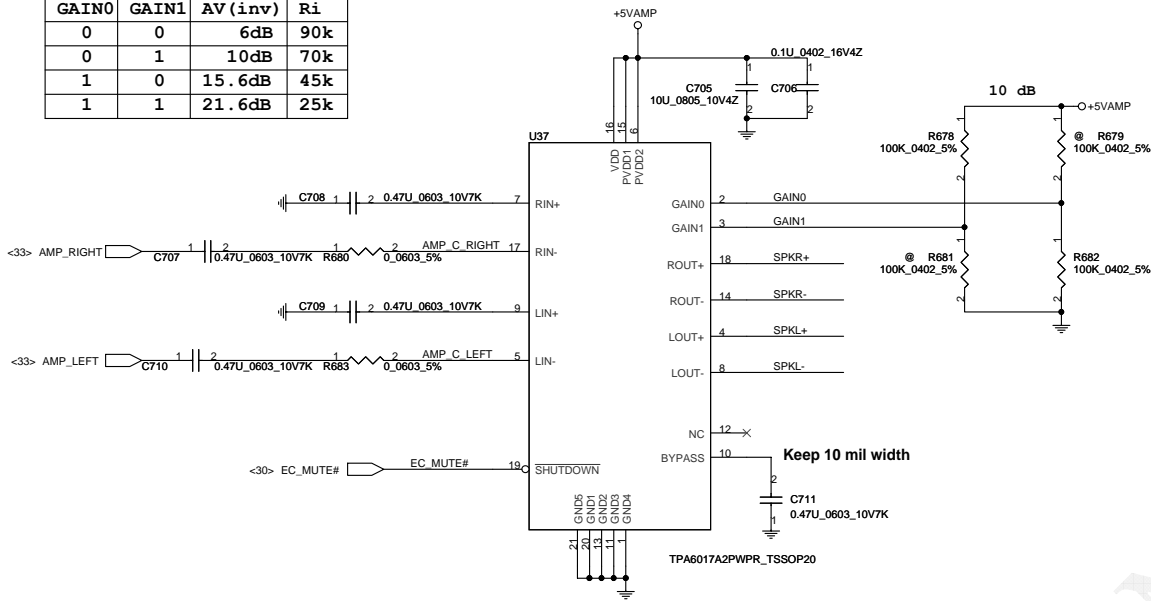


HD Audio Codec

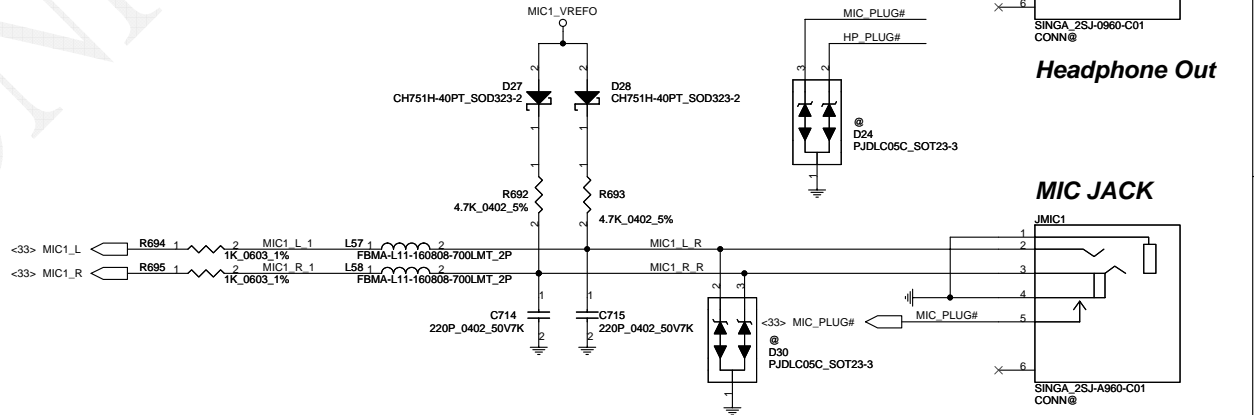
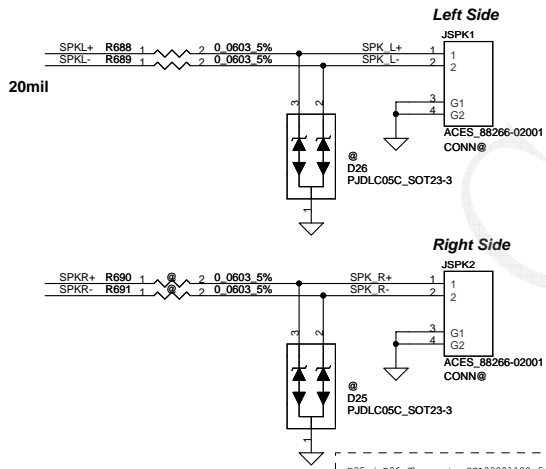


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				401939	A
Date: Friday, July 02, 2010				Sheet	33 of 48

GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



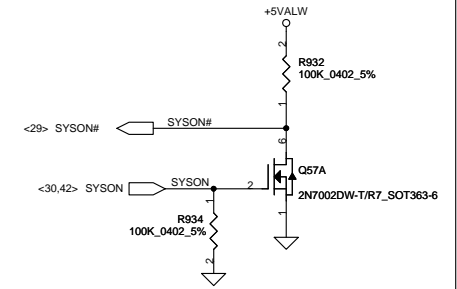
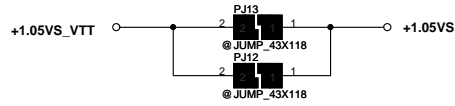
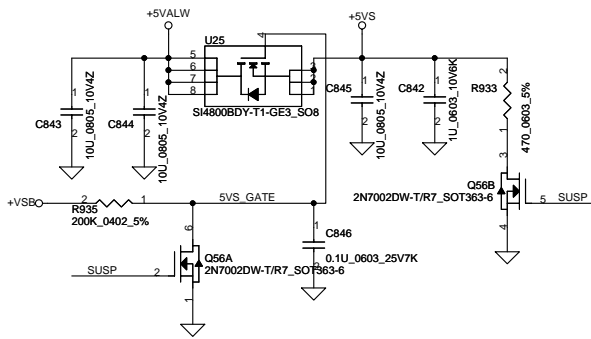
Int. Speaker Conn.



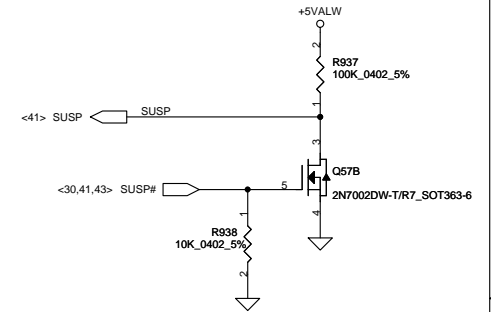
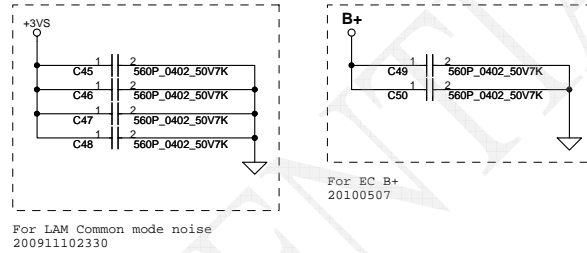
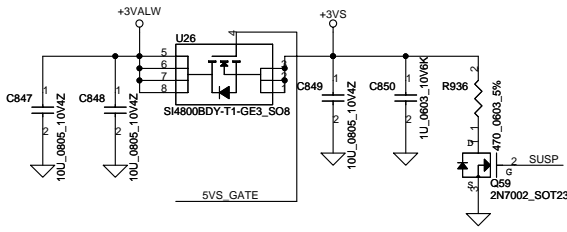
D25 / D26 Change to SCA00001100 for ESD 20090921

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				401939	A
Date: Friday, July 02, 2010				Sheet	34 of 48

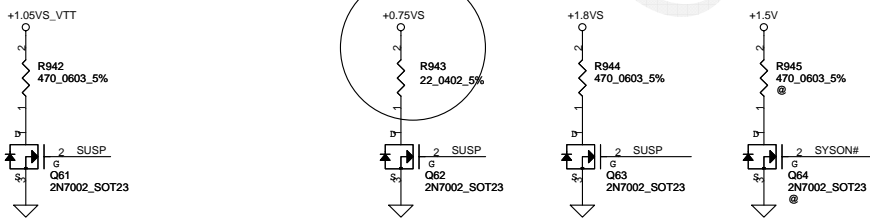
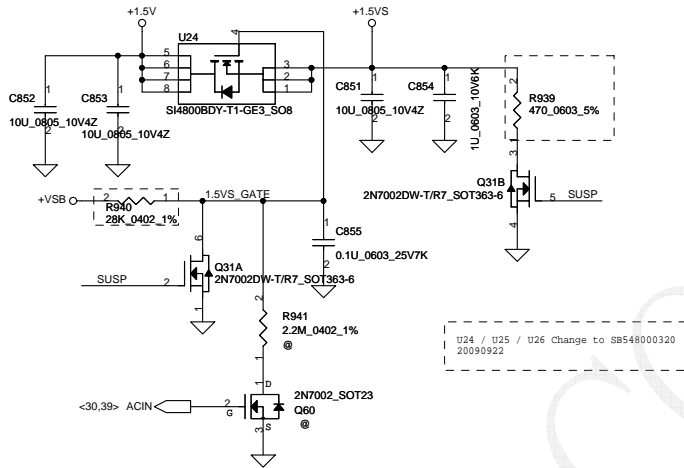
+5VALW TO +5VS



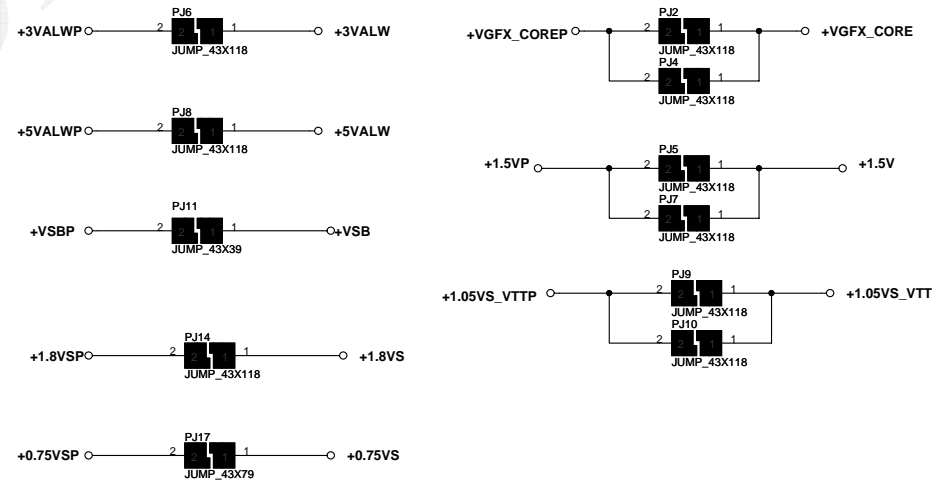
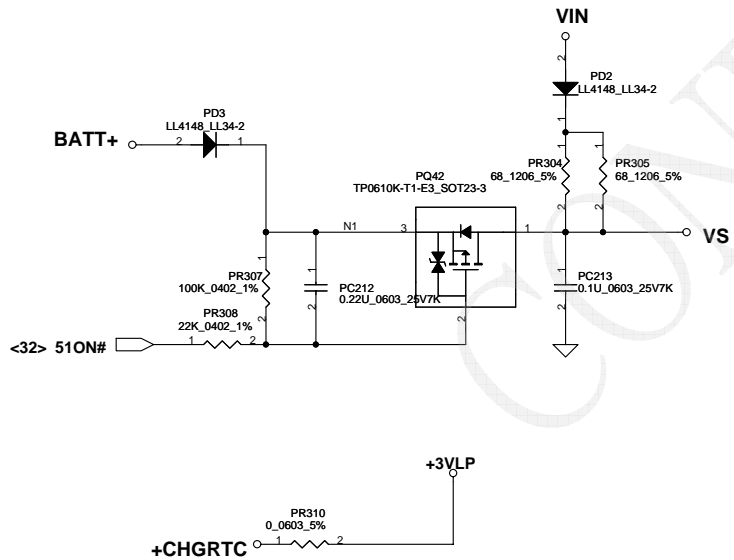
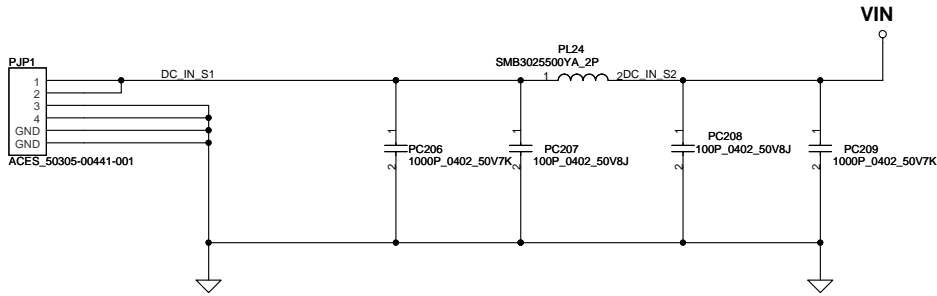
+3VALW TO +3VS



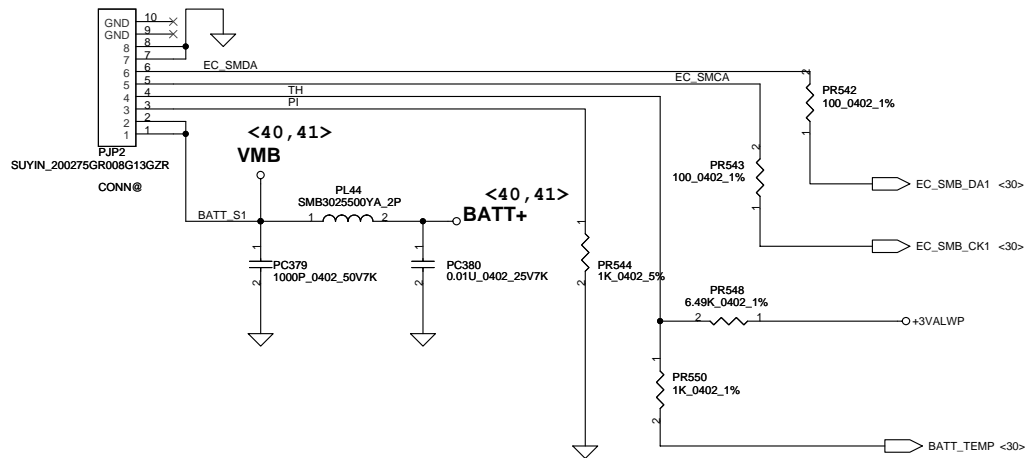
+1.5V to +1.5VS



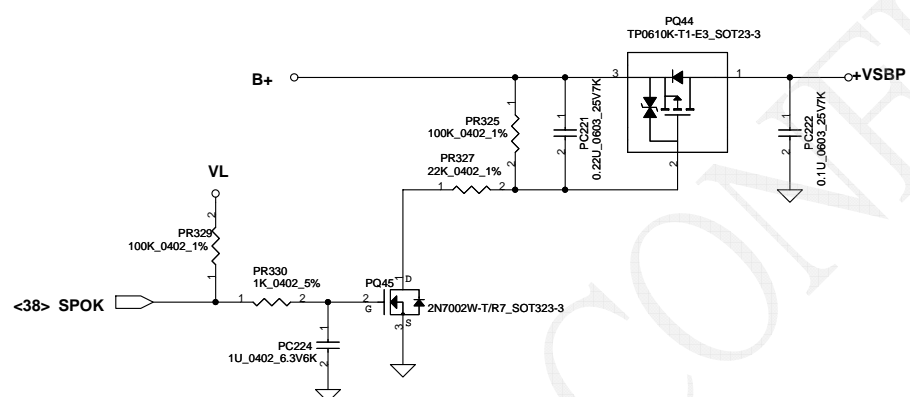
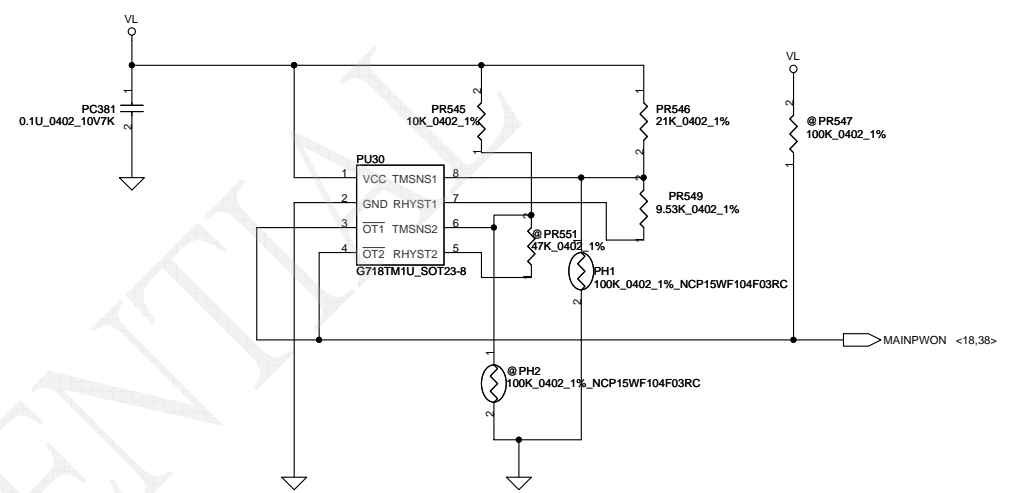
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Date:	Friday, July 02, 2010	Sheet	35 of 48			



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Customer Number	401939	Rev	A	Date:	Friday, July 02, 2010
				Sheet	36 of 48

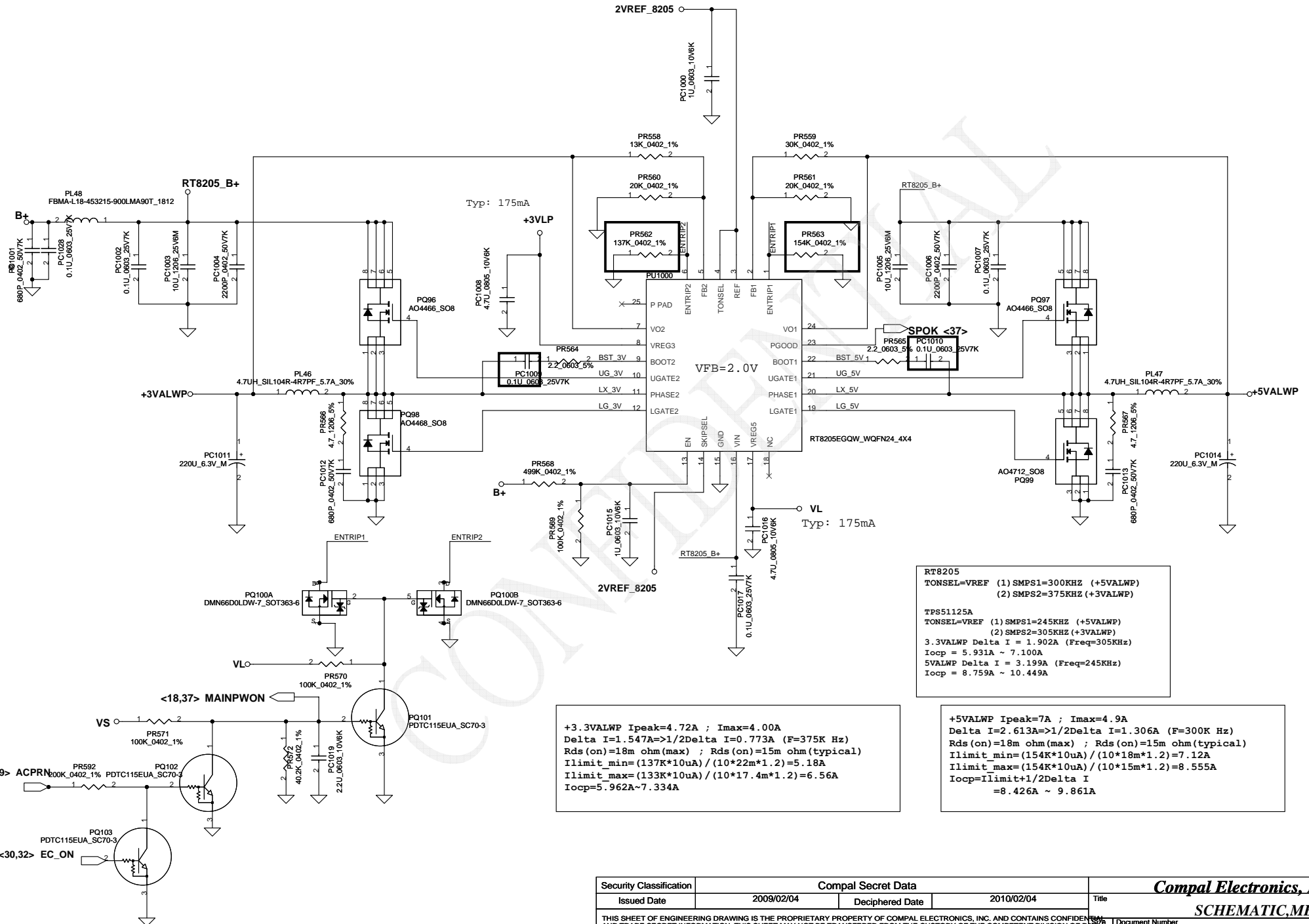


PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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				Rev A
Date: Friday, July 02, 2010				Sheet 37 of 48

Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



Typ: 175mA

VFB = 2.0V

Typ: 175mA

RT8205
 TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)

TPS51125A
 TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
 (2) SMPS2=305KHZ (+3VALWP)
 3.3VALWP Delta I = 1.902A (Freq=305KHz)
 Iocp = 5.931A ~ 7.100A
 5VALWP Delta I = 3.199A (Freq=245KHz)
 Iocp = 8.759A ~ 10.449A

+3.3VALWP Ipeak=4.72A ; Imax=4.00A
 Delta I=1.547A=>1/2Delta I=0.773A (F=375K Hz)
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Ilimit_min=(137K*10uA)/(10*22m*1.2)=5.18A
 Ilimit_max=(133K*10uA)/(10*17.4m*1.2)=6.56A
 Iocp=5.962A~7.334A

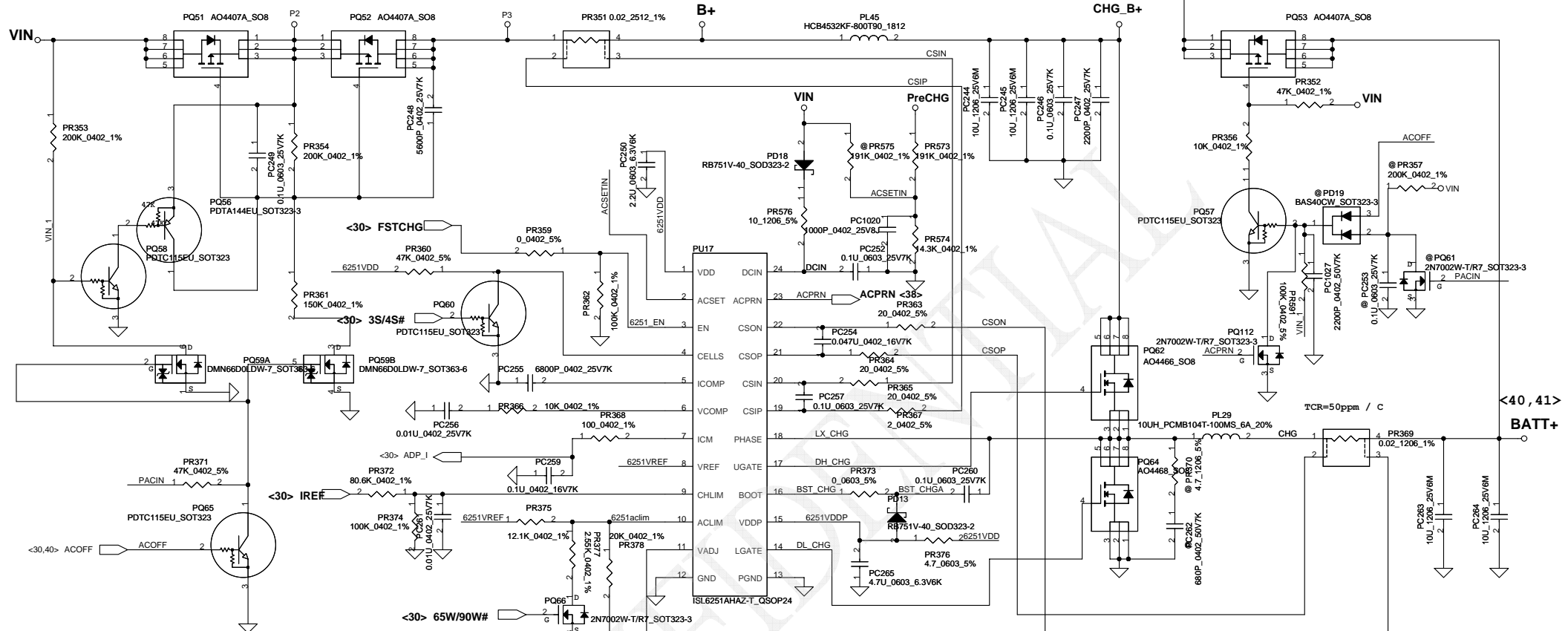
+5VALWP Ipeak=7A ; Imax=4.9A
 Delta I=2.613A=>1/2Delta I=1.306A (F=300K Hz)
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Ilimit_min=(154K*10uA)/(10*18m*1.2)=7.12A
 Ilimit_max=(154K*10uA)/(10*15m*1.2)=8.555A
 Iocp=Ilimit+1/2Delta I
 =8.426A ~ 9.861A

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Date:	Friday, July 02, 2010	Sheet	38	of 48	

Iada=0~4.74A (90W/19V=4.736A)
 Iada=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
 CP = 85%*Iada ; CP = 2.91A



CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

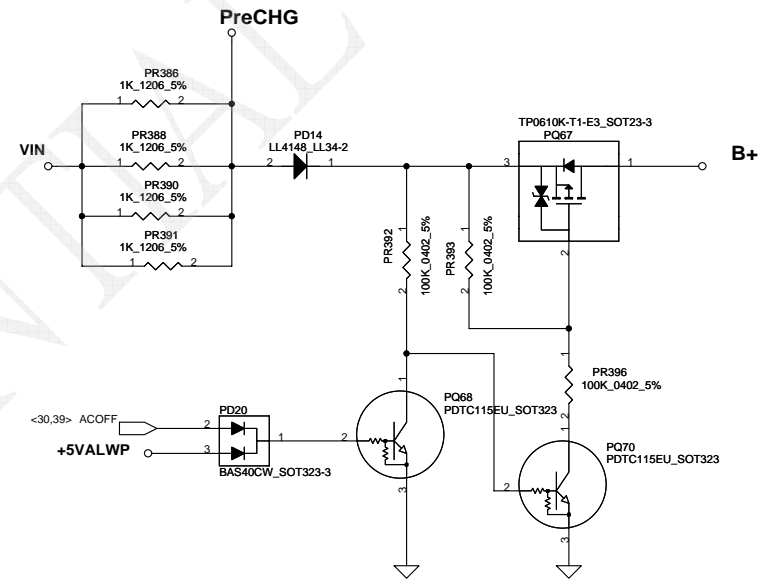
CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $K_i = 0.7224$
 $I_{REF} = 0.43V \sim 3.24V$

K_i
 $V_{chlim} = I_{ref} * (PR374 / (PR372 * PR374))$
 $= I_{ref} * (100K / (80.6K * 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow K_i = 0.7224$

K_v
 Internal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
 $R = 514K / 31.6K // (15.4K * 3K) = 11.372K$
 $r = 514K / 514K // 31.6K = 28.14K$
 $V_{cell0} = 1.75 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell0} + A * 0.175)) * K_v // (4.2 - (4.2 * A * 0.175)) * K_v$
 $A = V_{ref} * (R / (R + 514K)) + 0.052$
 $K_v = 9.451$

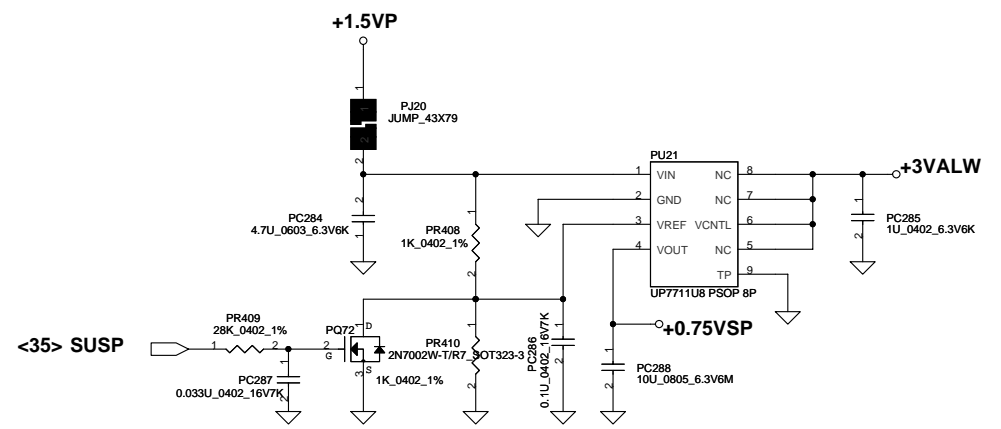
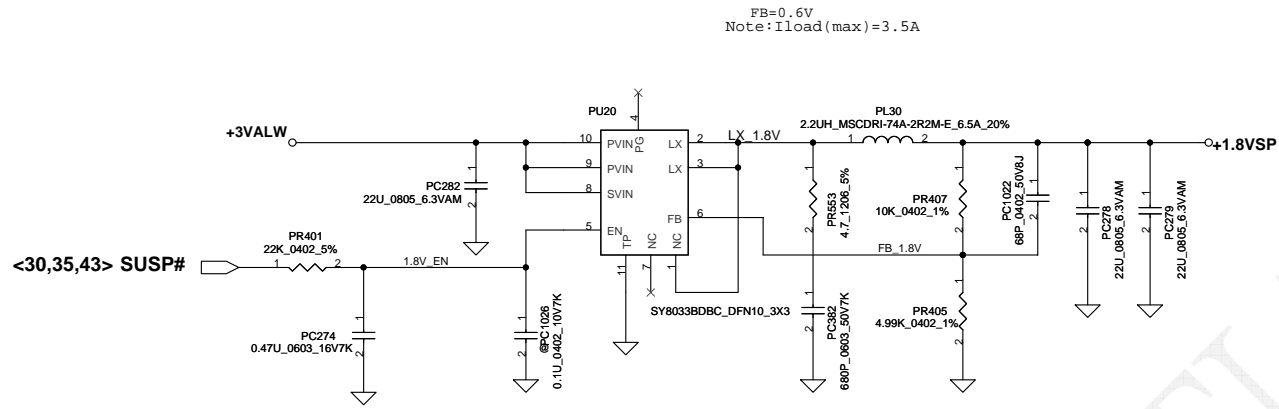
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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Date:	Friday, July 02, 2010	Sheet	39	of	48



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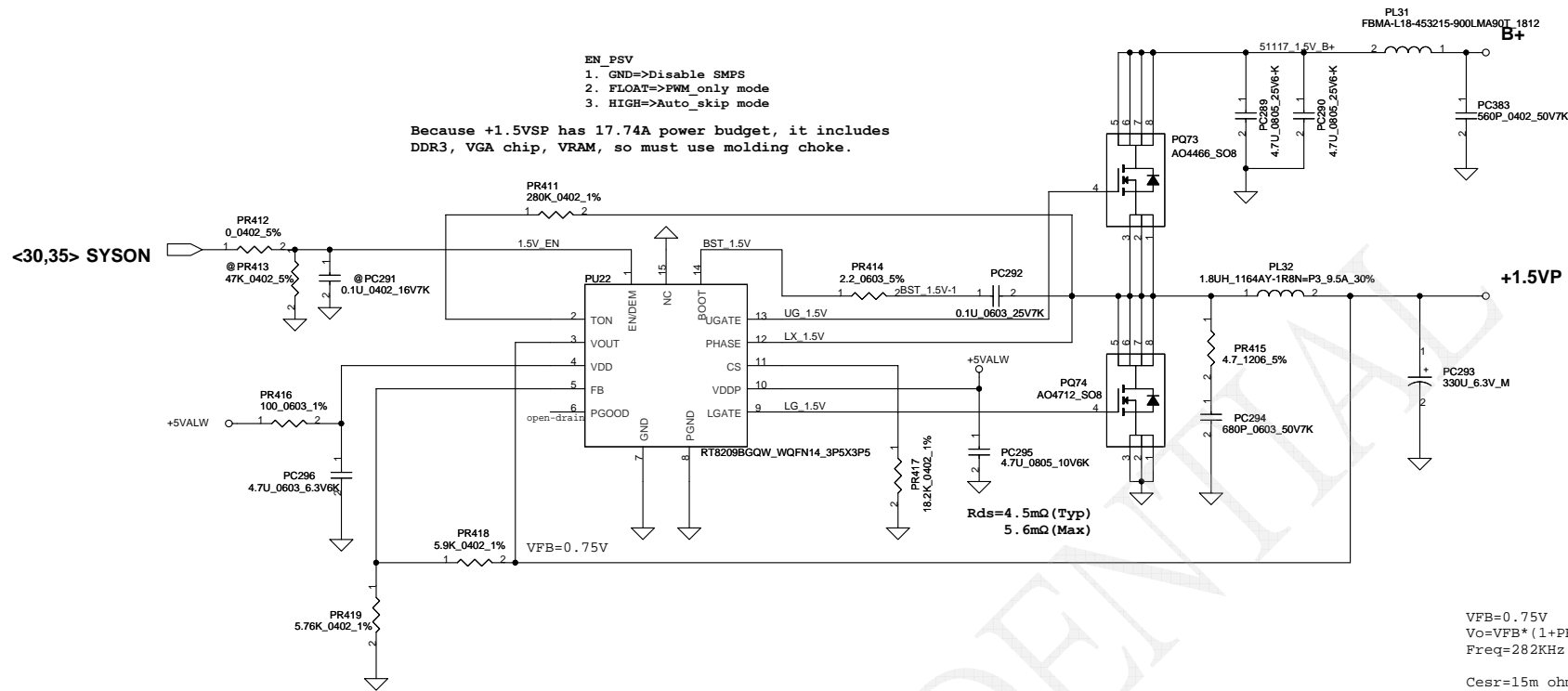
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Date:			Friday, July 02, 2010	Sheet 40 of 48



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Date: Friday, July 02, 2010				Rev A
Sheet 41 of 48				

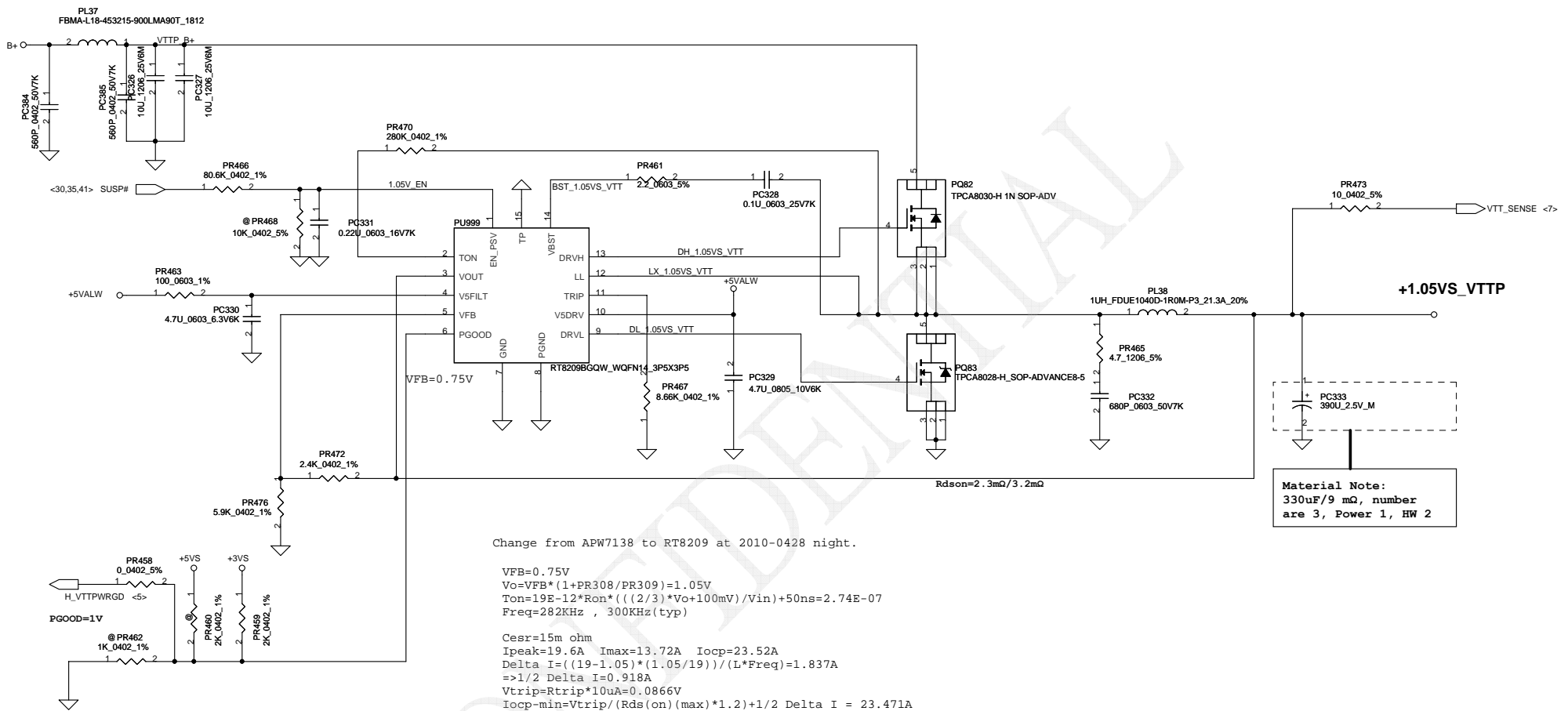
- EN_PSV
 1. GND=>Disable SMPS
 2. FLOAT=>PWM_only mode
 3. HIGH=>Auto_skip mode

Because +1.5VSP has 17.74A power budget, it includes DDR3, VGA chip, VRAM, so must use molding choke.



VFB=0.75V
 $V_o = V_{FB} * (1 + PR418 / PR419) = 1.52V$
 Freq=282KHz (min) , 300KHz (typ)
 Ccsr=15m ohm
 Iocp=9.94A~13A

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Doc No	Document Number	Rev			
401939	401939	A			
Date:	Friday, July 02, 2010	Sheet	42	of	48



Change from APW7138 to RT8209 at 2010-0428 night.

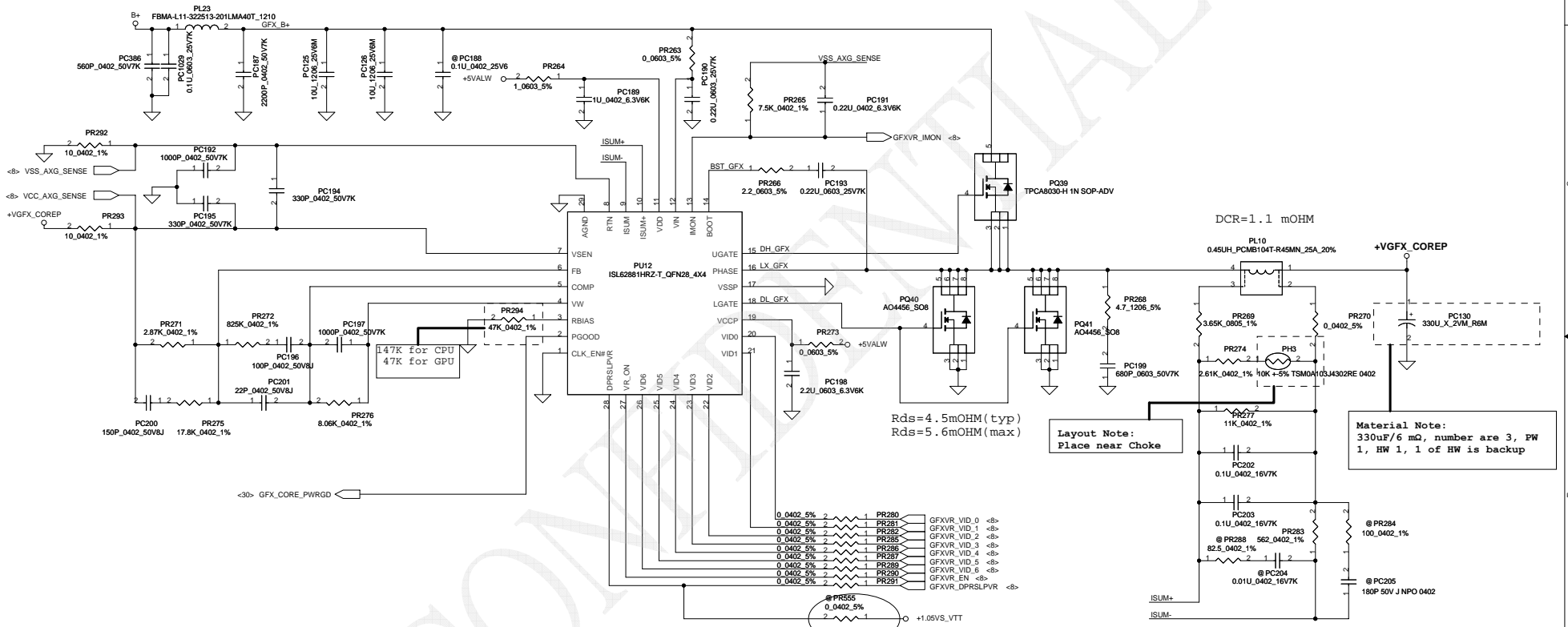
VFB=0.75V
 $V_o = VFB * (1 + PR308 / PR309) = 1.05V$
 $T_{on} = 19E-12 * R_{on} * ((2/3) * V_o + 100mV) / (V_{in}) + 50ns = 2.74E-07$
 $Freq = 282KHz, 300KHz (typ)$

Cesr=15m ohm
 $I_{peak} = 19.6A, I_{max} = 13.72A, I_{ocp} = 23.52A$
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * Freq) = 1.837A$
 $\Rightarrow 1/2 \Delta I = 0.918A$
 $V_{trip} = R_{trip} * I_{0uA} = 0.0866V$
 $I_{ocp_min} = V_{trip} / (R_{ds(on)}(max) * 1.2) + 1/2 \Delta I = 23.471A$
 $I_{ocp_max} = V_{trip} / (R_{ds(on)}(typ) * 1.2) + 1/2 \Delta I = 32.295A$
 $I_{ocp} = 22.4A \sim 30.8A$

Material Note:
 330uF/9 mQ, number
 are 3, Power 1, HW 2

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Date: Friday, July 02, 2010		Sheet 43 of 48		Rev A

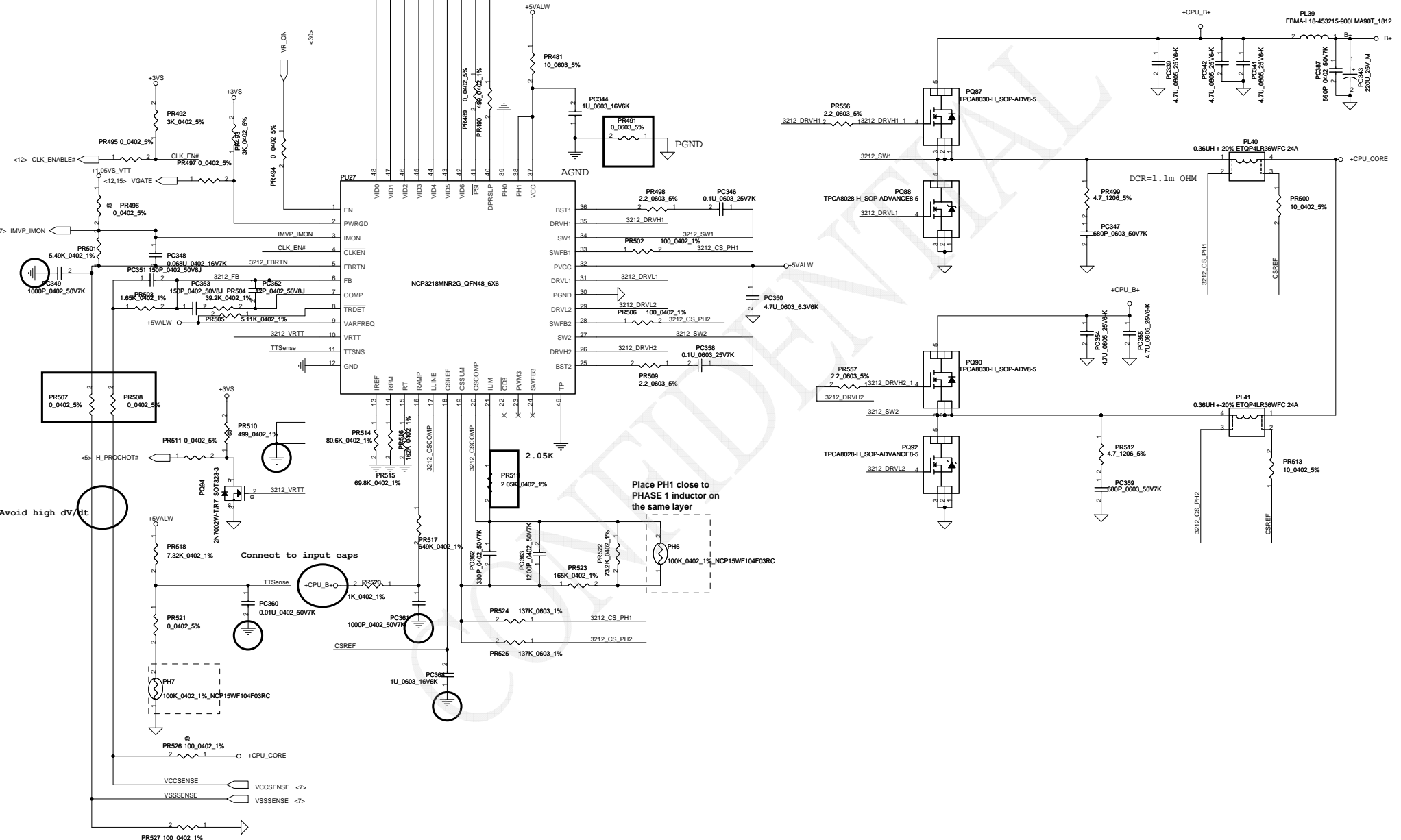
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
 OCP calculation : Assume DCR=1.1m ohm
 $G1=Rn/(Rn+Rsum)=0.617$
 where $Rn=PR277 // (PR274+PH3)=5.875k$ ohm
 $Rsum=PR269=3.65k$ ohm
 $LL=2*Rdroop*G1*DCR/Ri=6.96m$ V/A
 where $Rdroop=PR271=8.66k$ ohm, $Ri=PR283=1.69k$ ohm
 $Iocp=OCP$ Threshold*Rdroop/LL=24.89A



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				401939
				Rev
				A
Date: Friday, July 02, 2010				Sheet 44 of 48

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1					Change PR353 from SD034470280 to SD034200380.		
2	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	39	Change PR371 from SD034220280 to SD034470280. Change PR587 from SD034100380 to SD034470280. Change PR590 from SD034200280 to SD034143280. Change PR591 from SD028470280 to SD028100380.	2010/06/08	to PVT
3					Add PC1027 SE074222K80(S CER CAP 2200P 0402 50V7K) Change PQ111 from SB000006800 to SB301150200		
4	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	38	Add PQ102 and PQ103 SB301150200. Add PR592 SD034200380.	2010/06/08	to PVT
5	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	40	Change PR386 from SD011000080 to SD011100180. Add PR388, PR390, PR391 SD011100180. Add PD14 SC100001Y80 LL4148_LL34-2	2010/06/08	to PVT
6	EMI fail, add 3/5V snubber and Boost Resister to silve it.	EMI request to solve EMI issue.			Add PR566 and PR567 SD001470B80 S RES 4.7 1206 5% Add PC1012 and PC1013 SE074681K80 S CER CAP 680P 0402 50V7K		
7			0.1	38		2010/06/08	to PVT
8	EMI fail, add 1.5V snubber.	EMI request to solve EMI issue.	0.1	42	Change PR564 and PR565 from SD013000080 to SD013220B80 Add PR415 SD001470B80 4.7 1206 5%. Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603 Add PR465 SD001470B80 4.7 1206 5%.	2010/06/08	to PVT
9	EMI fail, add 1.05V snubber. and Boost Resister.	EMI request to solve EMI issue.	0.1	43	Add PC332 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
10					Change PR461 from SD013000080 to SD013220B80 Add PR268 SD001470B80 4.7 1206 5%.		
11	EMI fail, add GFX_CORE snubber.	EMI request to solve EMI issue.	0.1	44	Add PC199 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
12	HW power sequence modify.	HW request.	0.1	43	Change PR466 from SD034576280 S RES 1/16W 57.6K +-1% 0402 to SD034806280 S RES 80.6K 0402 1% Change PC331 from SE076104K80 S CER CAP .1U 16V K X7R to SE00000R700 S CER CAP 0.22U 16V K X7R 0402	2010/06/08	to PVT
13							
14	BOM unique.	BOM unique.	0.1	38	Chnage PQ101 from SB301150000 to SB301150200.	2010/06/08	to PVT
15	EMI request.	EMI request.	0.1	38	Add PC1028 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
16	EMI request.	EMI request.	0.1	44	Add PC1029 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
17	Sourcer request to change a common part.	Sourcer request.	0.1	38	Change PC1019 from SE00000GC00 S CER CAP 2.2U 10V K X7R 0603 to SE000003H00 S CER CAP 2.2UF 10V K X5R 0603	2010/06/08	to PVT
18	Per sourcer request.	Sourcer request to change PC331 from SE00000R700 to SE026224K80 for common part.	0.1	43	change PC331 from SE00000R700 to SE026224K80	2010/06/08	to PVT
19	CPU transient issue.	Need modify PC362 to 330P due to transient fail.	0.1	45	Change PC362 from SE074561K80 S CER CAP 560P 50V K X7R 0402 to SE074331K80 S CER CAP 330P 50V K X7R 0402	2010/06/08	to PVT
20	Per sourcer request.	Per sourcer request.	0.1	43 44	Chnage PQ39/PQ82 from SB000008L80 to SB00000HL00.	2010/06/08	to PVT
21	Cost down.	Cost down 3VALWP and Charger Low Side MOS.	0.1	38 39	Change PQ98 from SB00000AJ00 to SB000009580(AO4468). Change PQ64 from SB00000CG00 to SB000009580(AO4468).	2010/06/08	to PVT
22	Cost down.	Cost down +1.5VP Low side MOS and choke.	0.1	42	Chnage PQ74 from SB000009F80 to SB00000AJ00(AO4712). Chnage PL32 from SH000009U00 to SH000009680.	2010/06/08	to PVT
23	Cost down.	re-caculate 1.5VP OCP.	0.1	42	Change PR417 from SD034110280 to SD034182280.	2010/06/08	to PVT

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Document Number	401939	Rev	A	Date:	Friday, July 02, 2010
				Sheet	46 of 48

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Cost down.	re-caculate +3VALWP OCP.	0.1	38	Change PR562 from SD034107380 to SD034137380.	2010/06/08	to PVT
25							
26							
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Version change list (P.I.R. List)

Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1	EVT		04 / 08 04 / 16 04 / 21 04 / 26 04 / 27 04 / 29 04 / 29 05 / 03 05 / 03 05 / 06 05 / 07 05 / 10 05 / 11 05 / 12 05 / 13 06 / 01 06 / 02 06 / 03 06 / 04 06 / 10	<p>N/A</p> <p>Modify RTC SCH</p> <p>Change LAN to AR8152</p> <p>Update Power SCH</p> <p>Update AND Gate symbol - U1 / U2 / U6 / U7 / U19</p> <p>Update Power MOS symbol - U24 / U25 / U26</p> <p>C196 change to 1U for INTEL design</p> <p>CLK GEN del C35 / C36 / C30 / C31 / C32 / C33 / C34 / L3 (for 3G@ and @ function)</p> <p>O4+Q6 change to 2N7002DW</p> <p>Update U8 symbol</p> <p>Add DMIC function</p> <p>Modify USB define.</p> <p>Update Power SCH</p> <p>Add R17 for DMIC power</p> <p>Update Power SCH</p> <p>Change LAN to GIGA&10/100 co-lay</p> <p>Del R307 (LVDS conn.)</p> <p>Change +1.05VS_VTT to +1.05VS (CLK GEN)</p> <p>Change C842 / C850 / C854 / C656 to SE080105K80 1U_0603_10V6K</p> <p>Change R940 to 28K (S3 Power sequence)</p> <p>SW T1 pin define (LAN)</p> <p>Change R907 (0_0603) to 0_1206 5%</p> <p>Remove C40 / C41 / C42 / C43 / C44</p> <p>Change FAN Conn.</p> <p>Update Power SCH</p> <p>Change LAN to BCM57780 GIGA</p> <p>Del R637 / R639 / R640 / R645 / R647 / R648 (AUDIO)</p> <p>Del DMIC</p> <p>Update Power SCH</p> <p>Update Power SCH</p> <p>Add C49 / C50 (EC B+)</p> <p>Update Power SCH</p> <p>C764 / C765 change to 18P_0402_50V8J (EC)</p> <p>Reserve D13 / D24 / D30 (ESD)</p> <p>U17 change to RTS5137 (SA000043500) Card reader</p> <p>Update Power SCH</p> <p>Unpop L11 / C247 & Pop R304 for cost down</p> <p>Unpop C764 / X2 & Pop R13 & C765 Change to 100K for EC remove Crystal</p> <p>Pop R834 & R835 change to 200K for Project 1D</p> <p>Unpop D24 / D30</p> <p>Unpop R690 / R691</p> <p>Pop C49 / C50</p> <p>For HDMI</p> <p>Unpop R753 / R757 , Add R754 / R758 to 0 ohm.</p> <p>Change R759 to 3.9K.</p> <p>Change R755 to 4.7K ohm , Unpop R748.</p> <p>Unpop R778.</p> <p>R833 / R292 0_0805 change to 0_0603.</p> <p>C190 / C191 & C1135 / C1136 change to 33P 0402 50V8J for Vender test report</p> <p>Unpop C774-C799 for EMI cost down.</p> <p>Update Power SCH</p> <p>Add T25 / T26 / T27</p>	

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Date:				Friday, July 02, 2010	Sheet 48 of 48