

MODEL:	REV:	CHANGE LIST:	ECN NO	MODEL : ZR1 MB		
ZR1 MotherBoard	1A	FIRST RELEASE	E200604-0013 E200605-0194	PAGE	FROM	TO
	2A	PAGE 02 : ADD EMI SOLUTION PAGE 03 : MODIFY MDC NUT / UN-STUFF CPURST# PU R151 PAGE 06 : STUFF LIBG R430 FOR 940GML / MOVE TMDS PU AT NB SIDE PAGE 10 : ADD LCD PIN 31 & 33 TO GND FOR EMI / MODIFY S-VIDEO CONNECTOR P/N PAGE 11 : MODIFY RTC BATTERY CONNECTOR / ADD MB GPIO FOR FACTORY IDENTIFY / REMOVE SUSCLK FOR SMSC SIO PAGE 13 : MODIFY VMAIN AVAL TO +3V S5 / UN-STUFF R28 & R29 FOR LAN LED NO ACTIVE ISSUE PAGE 16 : ADD MINI-CARD BYPASS CAPACITOR BY ACER REQUEST / ALWAYS STUFF D11 FOR MINI-CARD W/L CAN'T ENABLE PAGE 17 : ADD L64 ON SPDIF FOR EMI / MODIFY BEEP NOISE (R281) / ADD C695,C696 FOR REDUCE LINE IN NOISE / MODIFY SPDIF CIRCUIT MODIFY R522,R524 FOR REDUCE DISTORTION / RESERVE R541,R542,R543 FOR NOISE REDUCTION / STUFF U41 / UN-STUFF D30 FOR POP ISSUE PAGE 18 : MODIFY RF LED ; EMAIL LED ; IDE LED CIRCUIT / MODIFY TP PIN DEFINE PAGE 20 : MODIFY SIO TO NS87383 / ADD RGB EMI SOLUTION / RESERVE DVI EMI SOLUTION / UN-STUFF TMDS PU AT DOCKING SIDE PAGE 21 : MODIFY PL2,PL5 TO 2R5 FOR REDUCE POWER RIPPLE & INCREASE POWER BUDGET PAGE 22 : SOLVE CPU VCORE UN-STABLE ISSUE TO CHANGE SERVAL COMPONENT VALUE PAGE 23 : MODIFY PL8 TO 2R5 FOR COST DOWN / ADD PC16,PC21 FOR PWM STABILITY / UN-STUFF PR21 FOR WRONG PU POWER LEVEL PAGE 24 : MODIFY PR30 FOR NVVDD POWER QUALITY	E200605-3569 E200605-6558	1	1A	
	3A	PAGE 02 : MODIFY C509,C503,C491,C498 to 4.7uF PAGE 03 : REMOVE R102 0 ohm PAGE 04 : Modify C187 to 330uF , remove C222 PAGE 06 : MODIFY C605,C590,C609 to 4.7uF / Add EMI solution C705 ~ C708 PAGE 08 : MODIFY L22,L23,Add PC166,C712-C715 for TV noise / Modify C327,C594 to 330uF;C158,C548 to 10uF / remove R449,R451 0 ohm PAGE 09 : Remove C76,C88 / modify C75 to 100uF PAGE 10 : Modify TV filter circuit / modify LCD VCC circuit PAGE 11 : Add media board GPIO pin PAGE 13 : Modify C99,C97,C98,C61,C79 to 4.7uF PAGE 14 : Remove R497,R222 0 ohm / modify C390,C391,C405,C412 to 4.7uF PAGE 15 : Modify C642,C409 to 4.7uF / modify R163,R164,R161,R153 to RN92,RN93 PAGE 16 : Modify R452,R454 to RN91, R389,R392 to RN90 PAGE 17 : Modify C651,C430,C440,C658,C666 to 4.7uF / Modify SPDIF circuit PAGE 18 : Remove R208,R510 for ODD / Remove R459,R106 0 ohm PAGE 20 : Modify SIO clock & strap R303 PAGE 21 : Remove PR110,PR155,PR114,PR106,PR153 0 ohm / Add PC167 for TV noise PAGE 22 : Remove PR149 0 ohm PAGE 23 : Remove PR24 0 ohm PAGE 24 : Remove NVVDD switching voltage circuit / remove PR135,PR100 0 ohm PAGE 25 : Remove PR28 0 ohm		2	2A	3A
				3	3A	



Quanta Computer Inc.

PROJECT : ZR1

APPROVE BY: JIM HSU

DRAWING BY:JACKY CHENG

REV 3A

COVER SHEET 1 OF 1

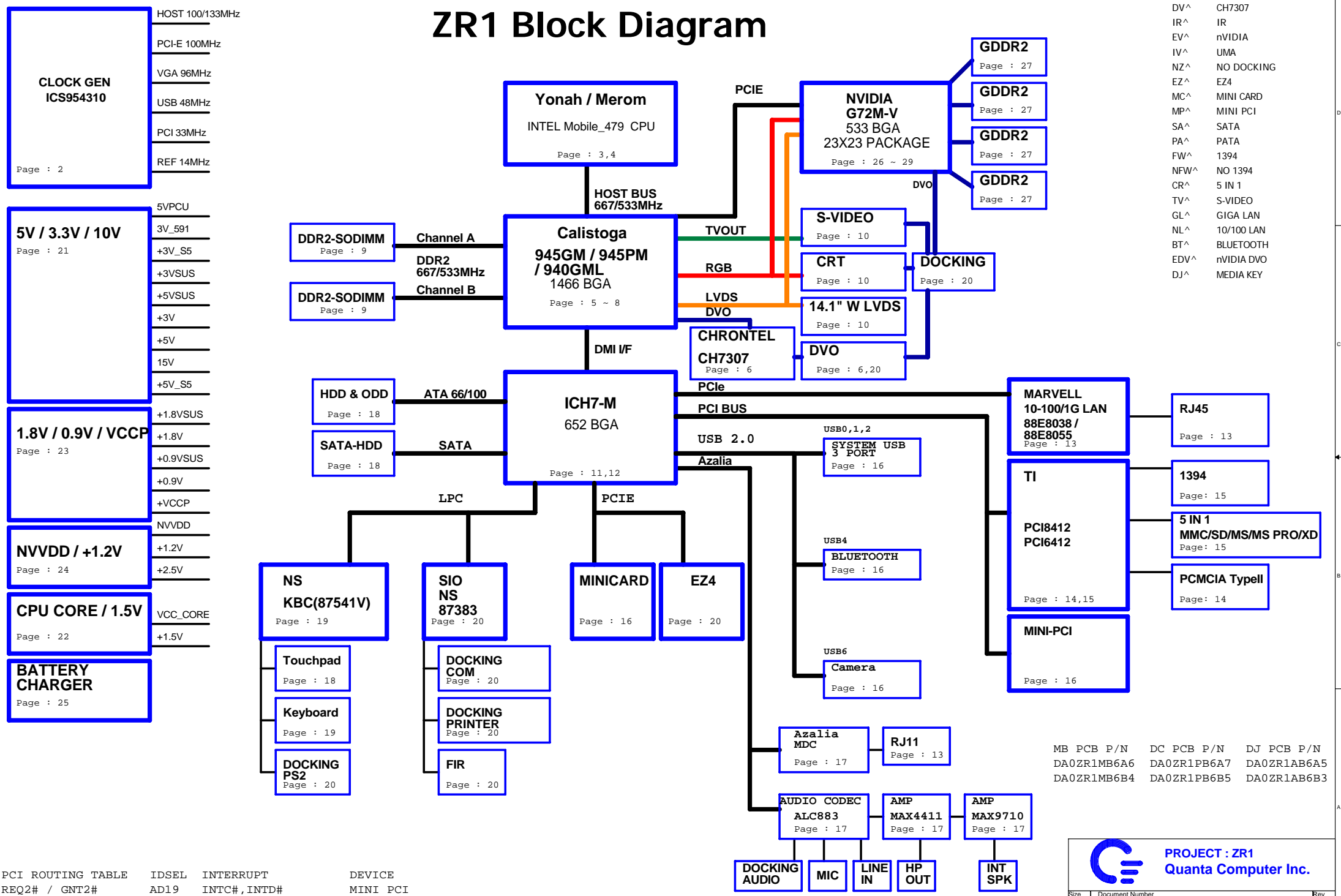
MB ASSY'S P/N :
31ZR1MB0008,16,24,32,41,59,83,91,B4

PROJECT LEADER: JIM HSU

DOCUMENT NO: 204

DATE :2006/06/26

ZR1 Block Diagram



- DV^ CH7307
- IR^ IR
- EV^ nVIDIA
- IV^ UMA
- NZ^ NO DOCKING
- EZ^ EZ4
- MC^ MINI CARD
- MP^ MINI PCI
- SA^ SATA
- PA^ PATA
- FW^ 1394
- NFW^ NO 1394
- CR^ 5 IN 1
- TV^ S-VIDEO
- GL^ GIGA LAN
- NL^ 10/100 LAN
- BT^ BLUETOOTH
- EDV^ nVIDIA DVO
- DJ^ MEDIA KEY

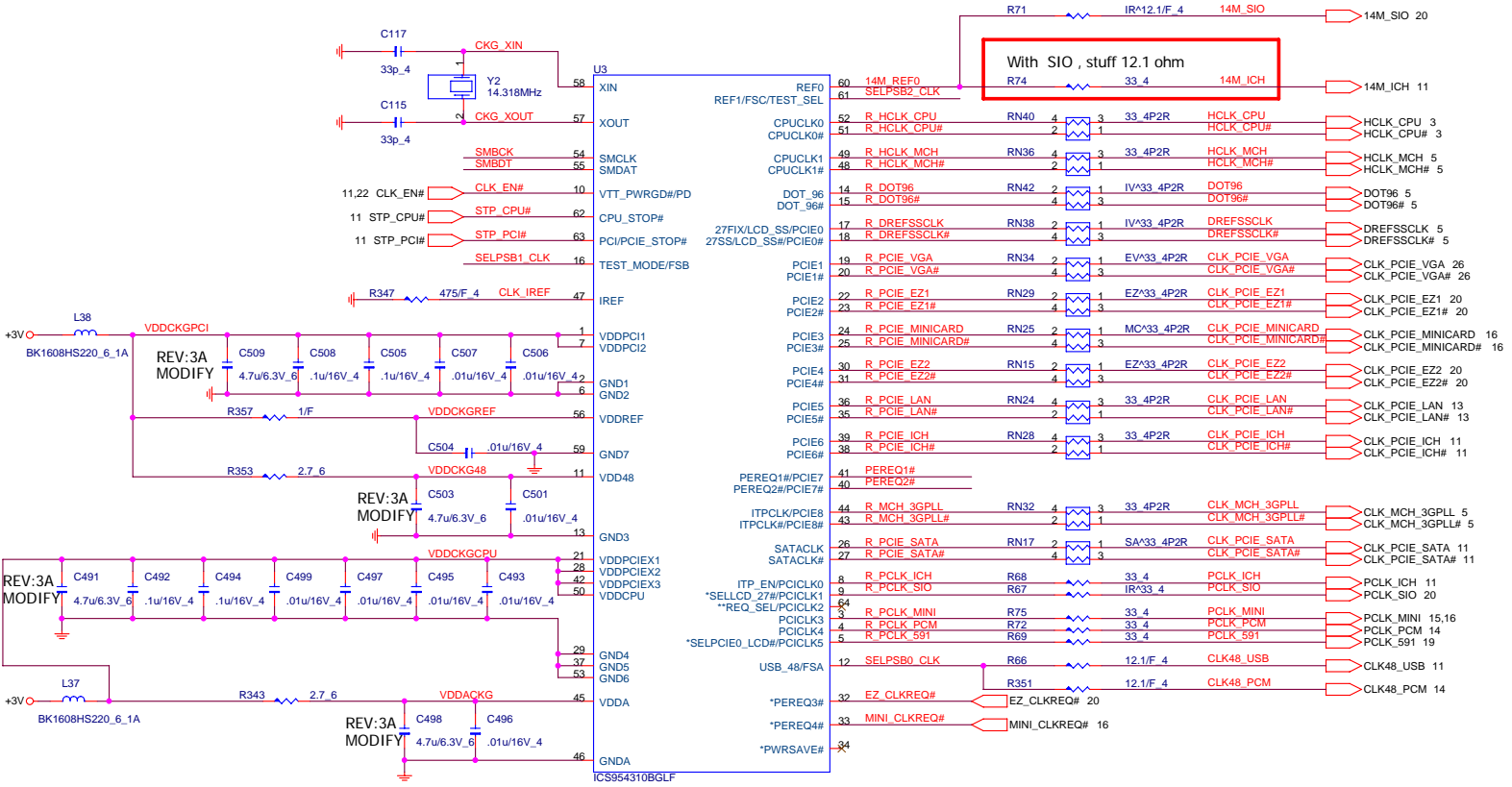
PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ2# / GNT2#	AD19	INTC#, INTD#	MINI PCI
REQ0# / GNT0#	AD25	INTE#, INTF#, INTG#	TI XX12

MB PCB P/N	DC PCB P/N	DJ PCB P/N
DA0ZR1MB6A6	DA0ZR1PB6A7	DA0ZR1AB6A5
DA0ZR1MB6B4	DA0ZR1PB6B5	DA0ZR1AB6B3

PROJECT : ZR1
Quanta Computer Inc.

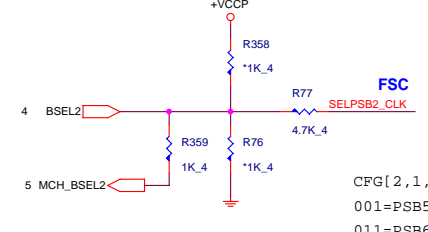
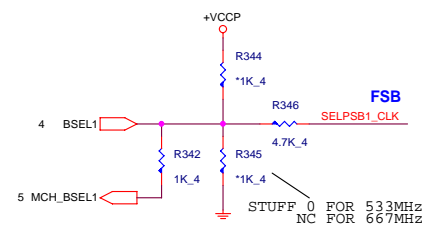
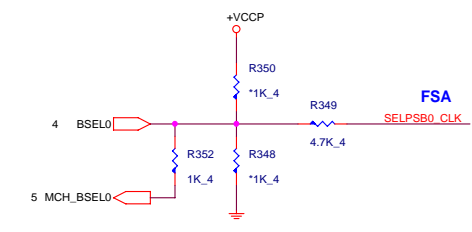
Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date:	Thursday, June 29, 2006	Sheet 1 of 29

CLOCK GENERATOR



PEREQ1# --> PCIE0 & PCIE6
 PEREQ2# --> PCIE1 & PCIE8
 PEREQ3# --> PCIE2 & PCIE4
 PEREQ4# --> PCIE3 & PCIE5 & PCIE7

SMBUS Address : D2 (read) , D3 (write)



CFG[2,1,0]
 001=PSB533
 011=PSB667

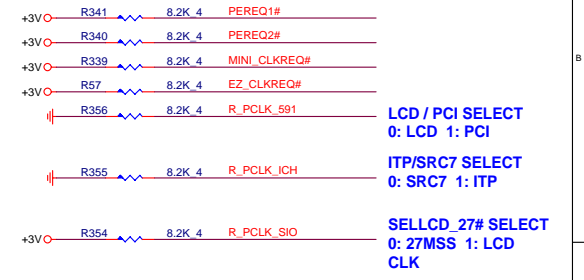
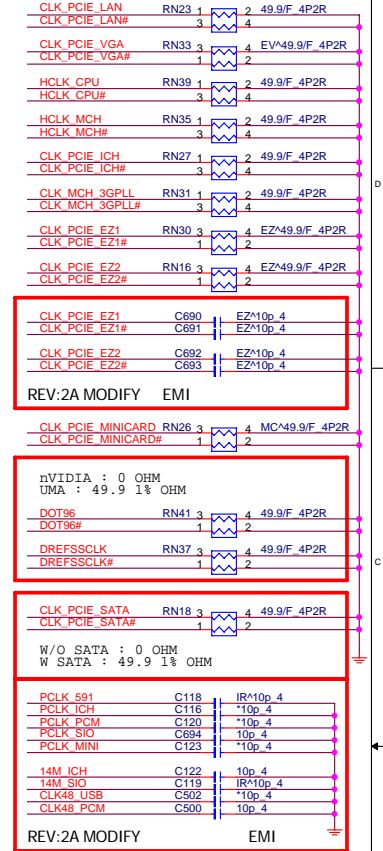
FSB SETTING

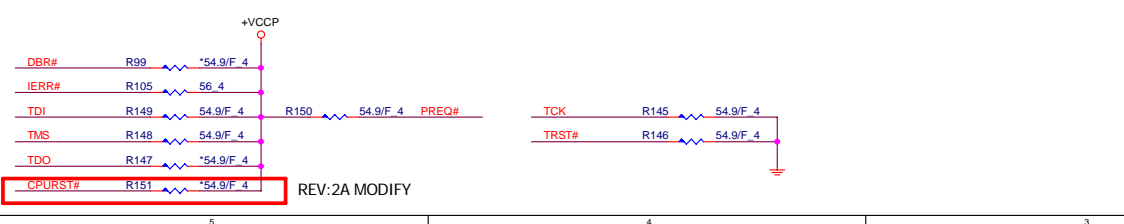
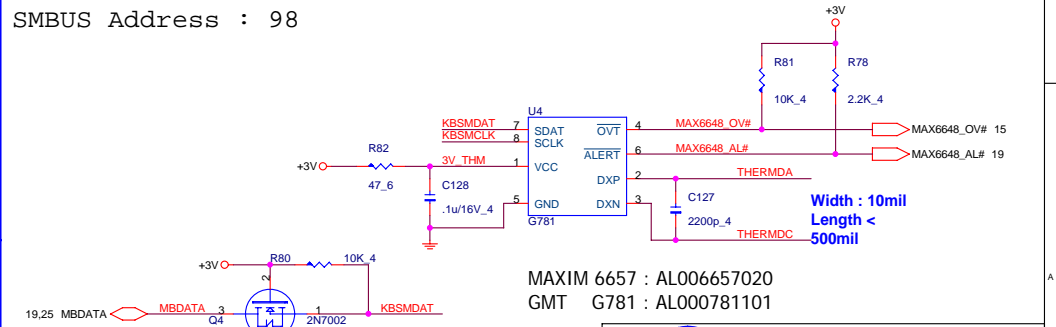
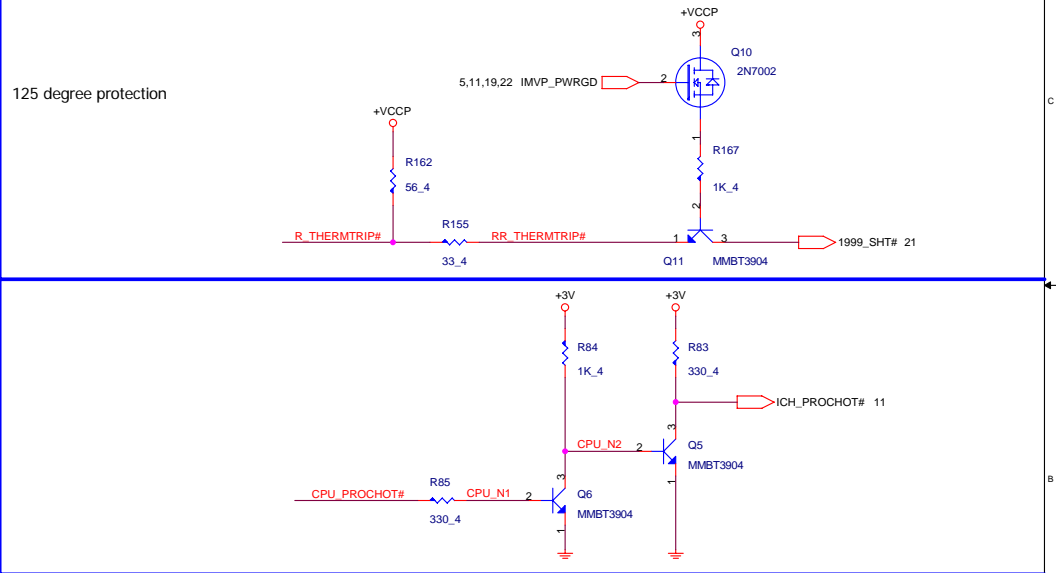
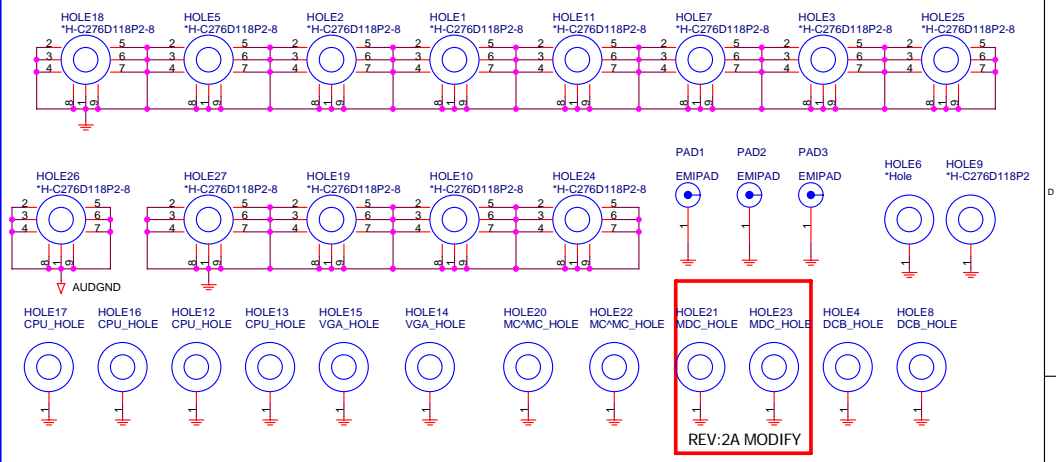
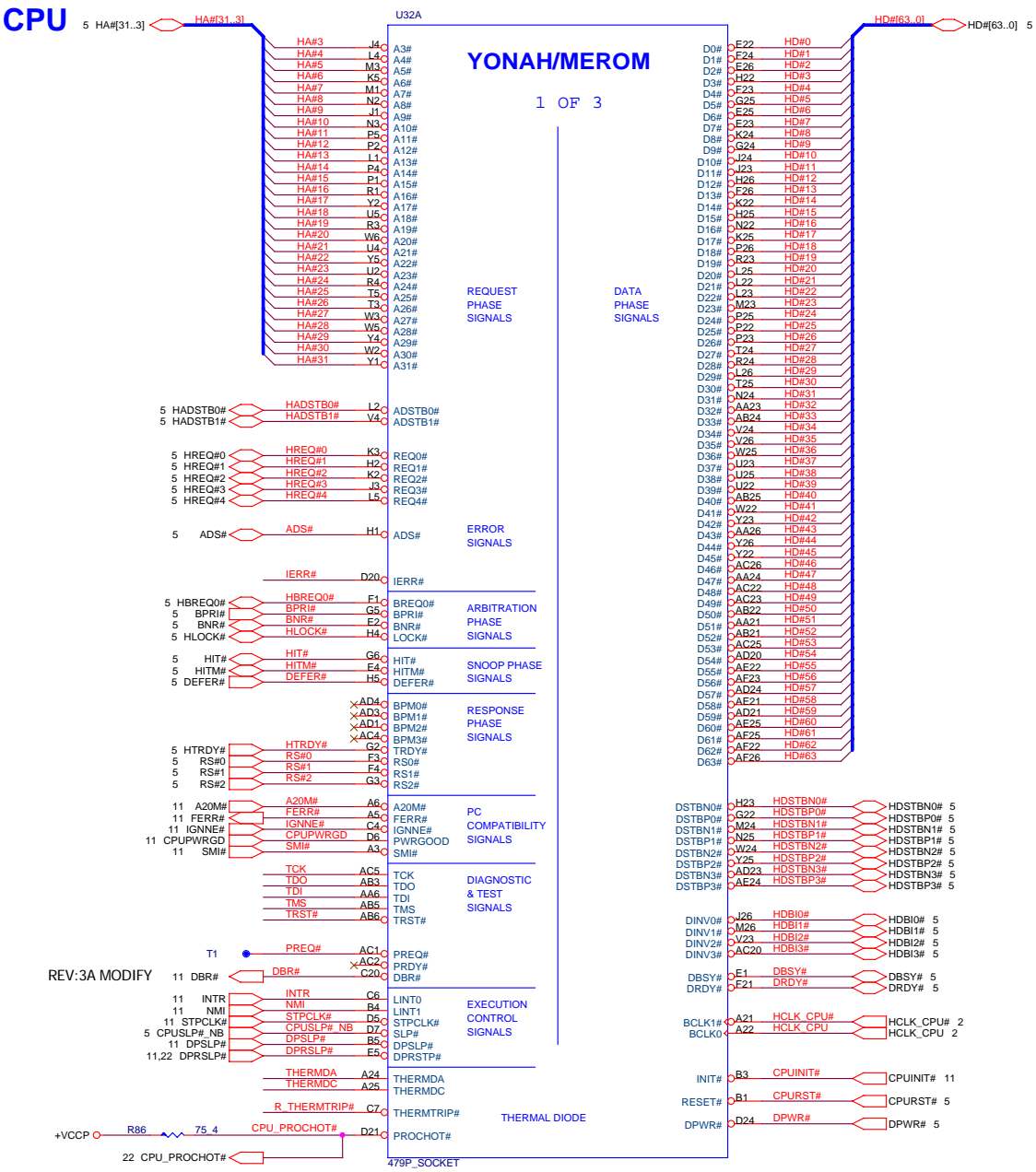
FSC	FSB	FSA	CPU	PCIE	PCI
0	0	0	266	100	33
0	0	1	133	100	33
0	1	0	200	100	33
0	1	1	166	100	33
1	0	0	333	100	33
1	0	1	100	100	33
1	1	0	400	100	33
1	1	1	200	100	33

PROJECT : ZR1
 Quanta Computer Inc.

Size Document Number
CLOCK GENERATOR

Date: Thursday, June 29, 2006 Sheet 2 of 29 Rev 3A





CPU

COMPO - COMP3
Width : 20mil
Length < 500mil

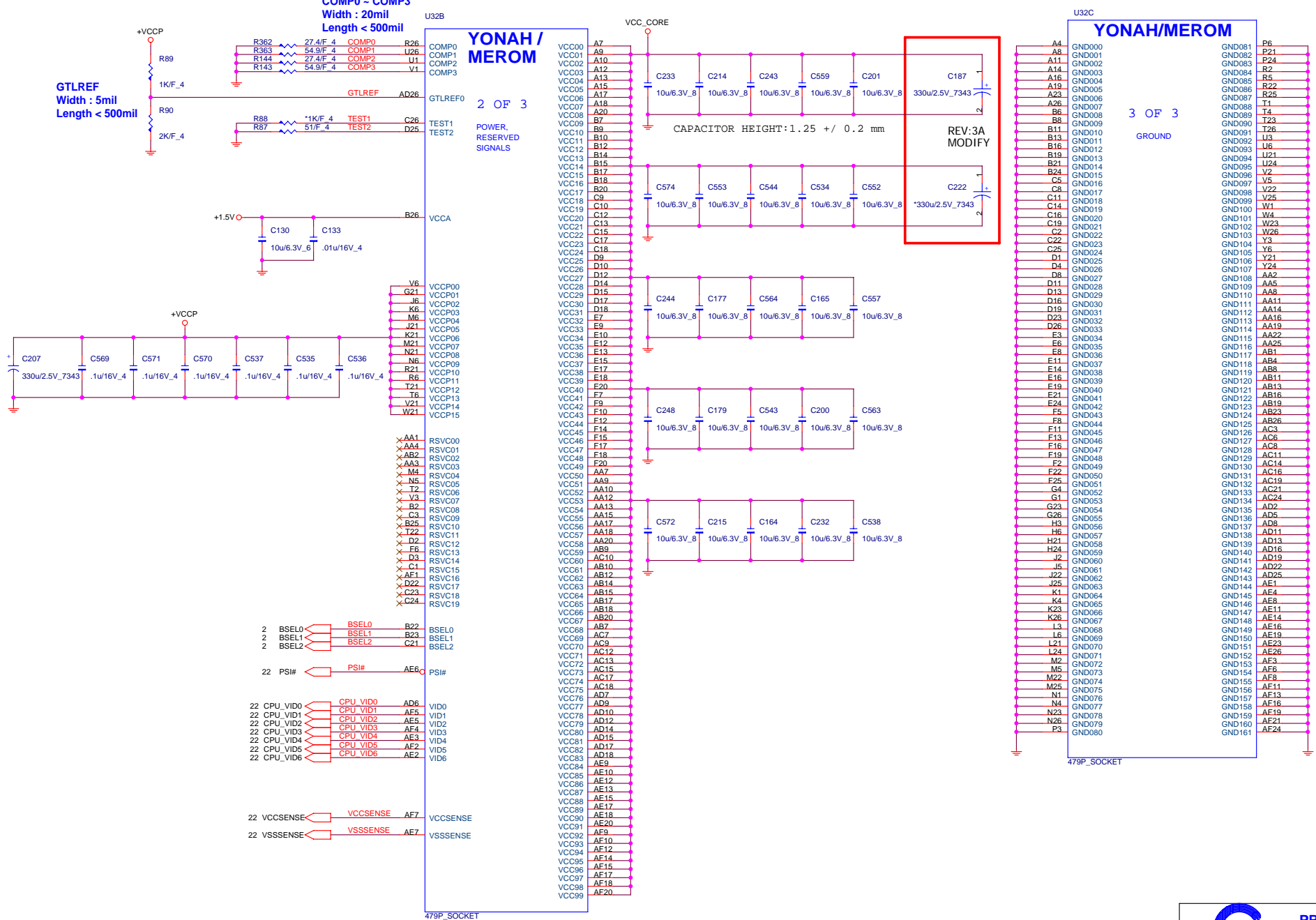
GTLREF
Width : 5mil
Length < 500mil

YONAH/
MEROM

2 OF 3
POWER,
RESERVED
SIGNALS

YONAH/MEROM

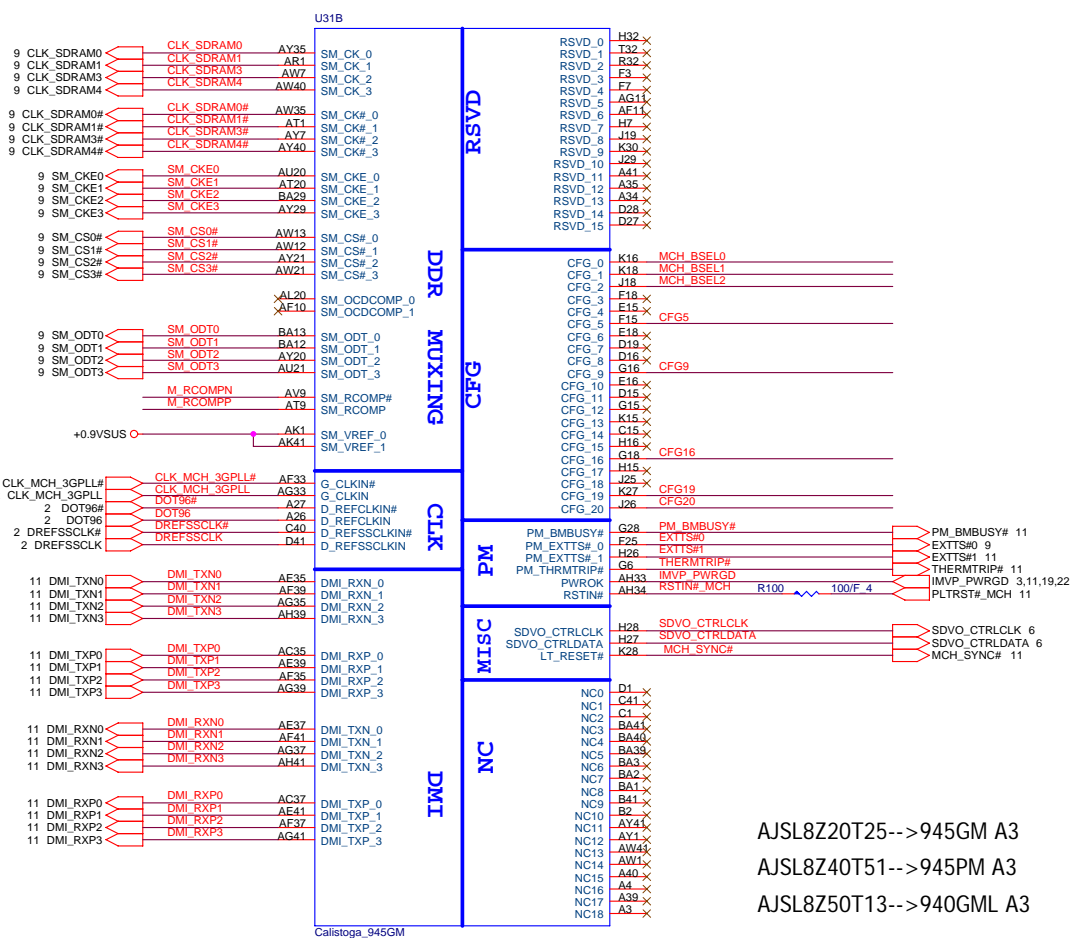
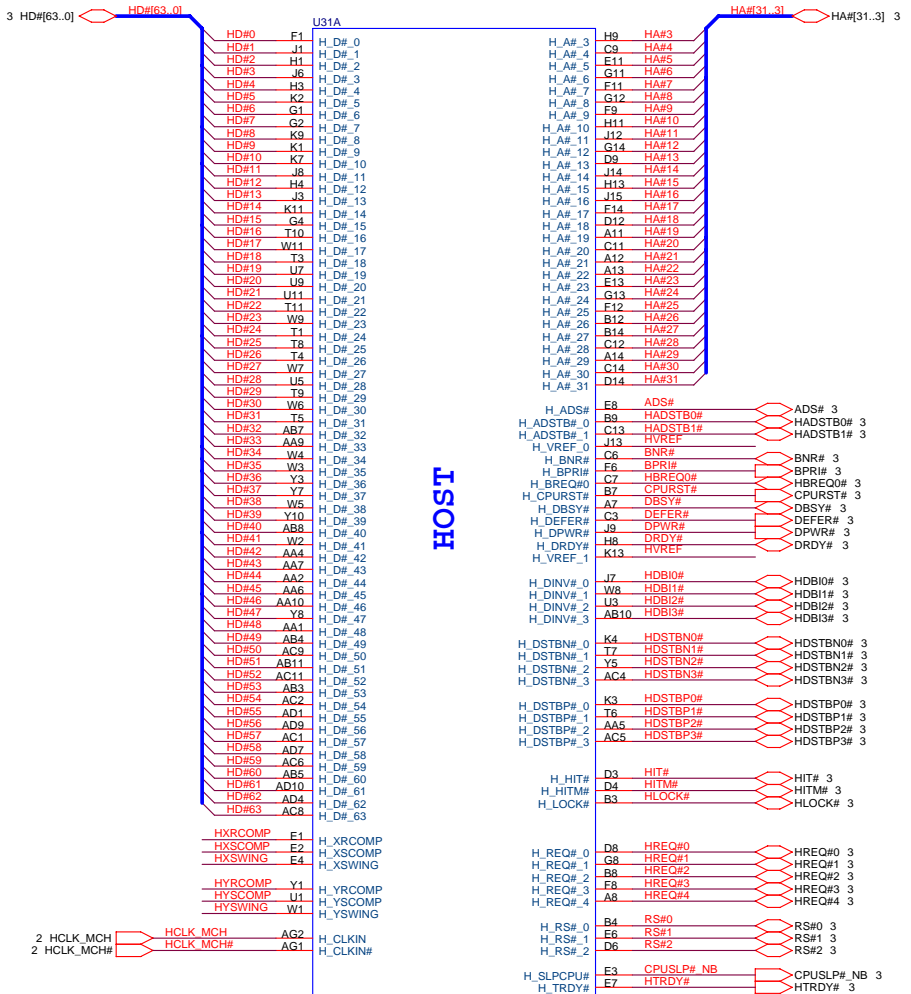
3 OF 3
GROUND



PROJECT : ZR1
Quanta Computer Inc.

Size Document Number Rev 3A
CPU (POWER)
Date: Thursday, June 29, 2006 Sheet 4 of 29

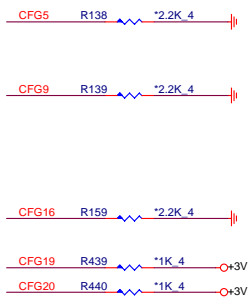
NB_945GM/PM/940GML



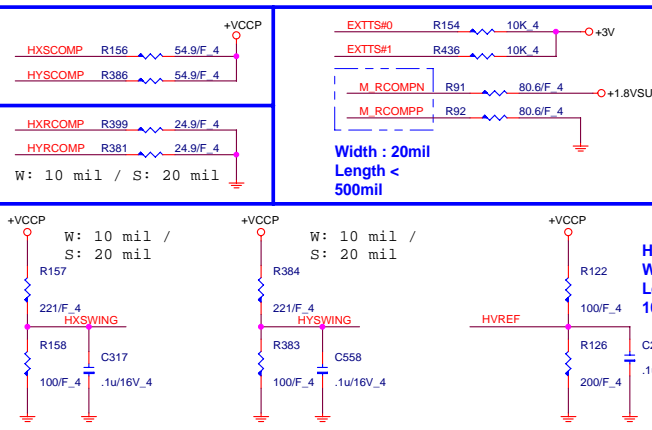
AJSL8Z20T25-->945GM A3
 AJSL8Z40T51-->945PM A3
 AJSL8Z50T13-->940GML A3

- MCH_CFG_5 : Low = DMI X2, High=DMIX4
- MCH_CFG_6 : Low = Moby Dick, High = Calistoga (Default)
- MCH_CFG_7 : Low = RSVD, High = Mobile CPU
- MCH_CFG_9 PCI Exp Graphics Lane: Low =Reverse lane ,High=Normal
- MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
- MCH_CFG_11: PSB 4x Enable : Low=Rsvd, High=Calistoga.
- MCH_CFG_16 FSB Dymnic ODT: Low = Dynamic ODT Disabled, High= Dynamic ODT Enabled.
- MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
- MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
- MCH_CFG_20 PCIe Backward interoperability mode: Low= only SDVO or PCIe x1 is operational (defaults) , High=SDVO and PCIe x1 are operation simultaneously via the PEG port.

GMCH Strap pin

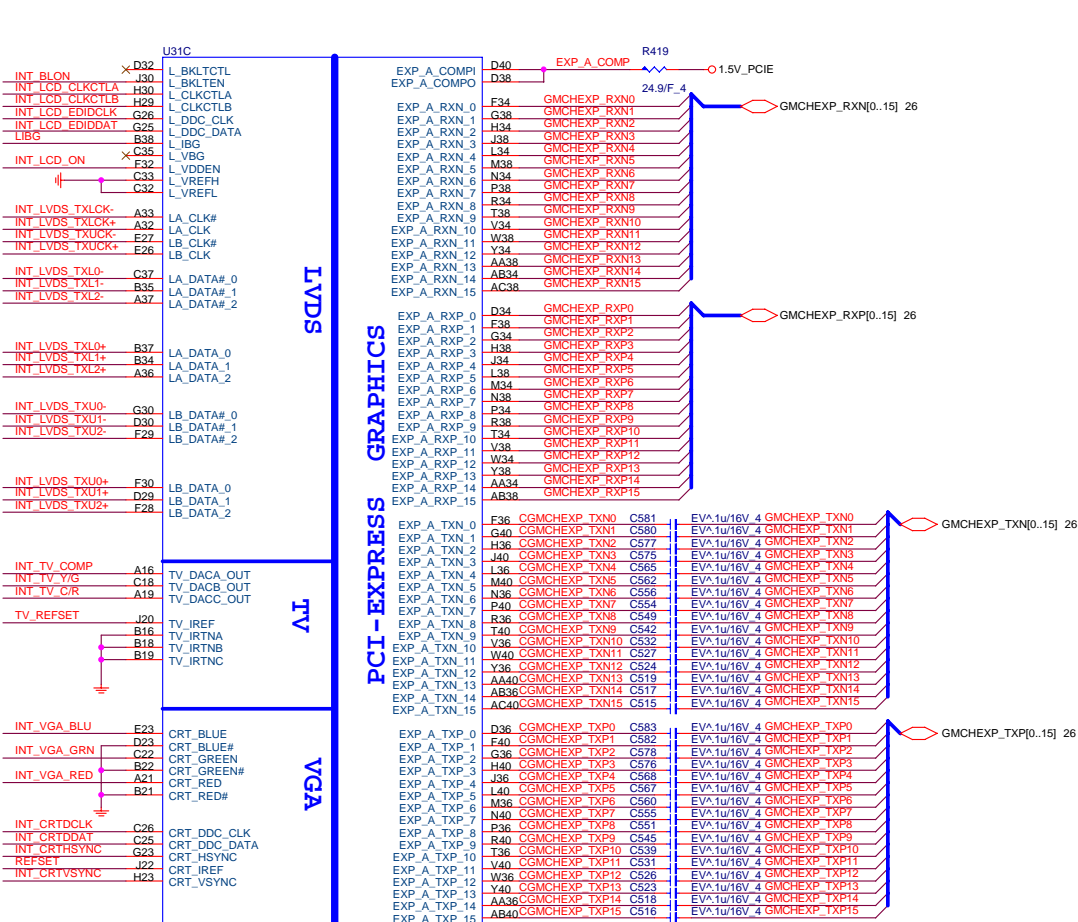


MCH_BSEL0 → MCH_BSEL0 2 CFG[2 , 1 , 0]
 MCH_BSEL1 → MCH_BSEL1 2 001=PSB533
 MCH_BSEL2 → MCH_BSEL2 2 011=PSB667

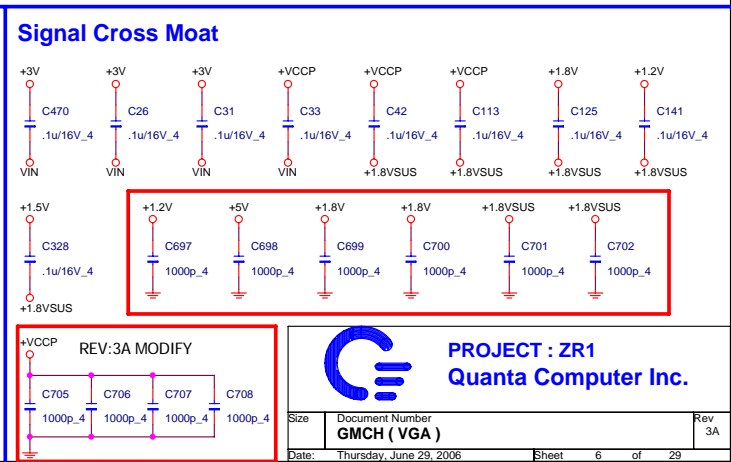
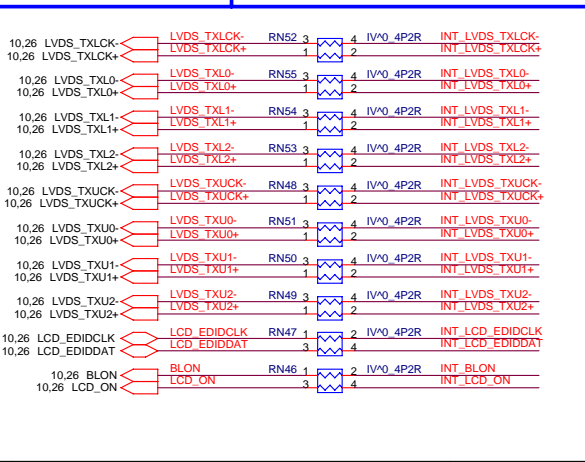
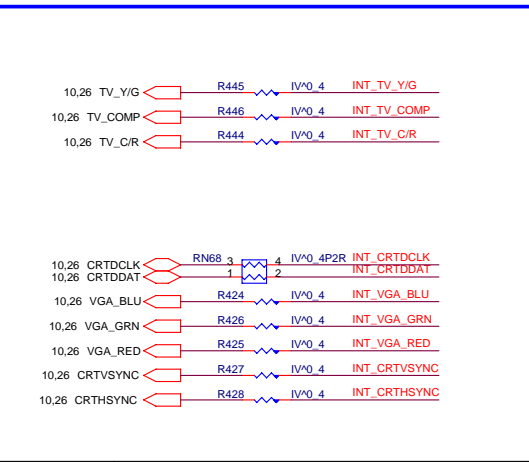
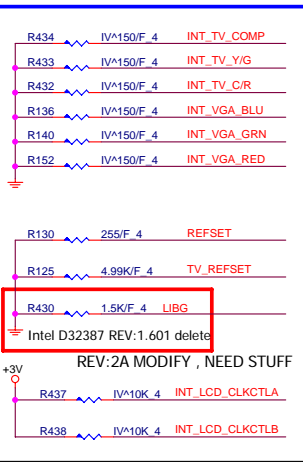
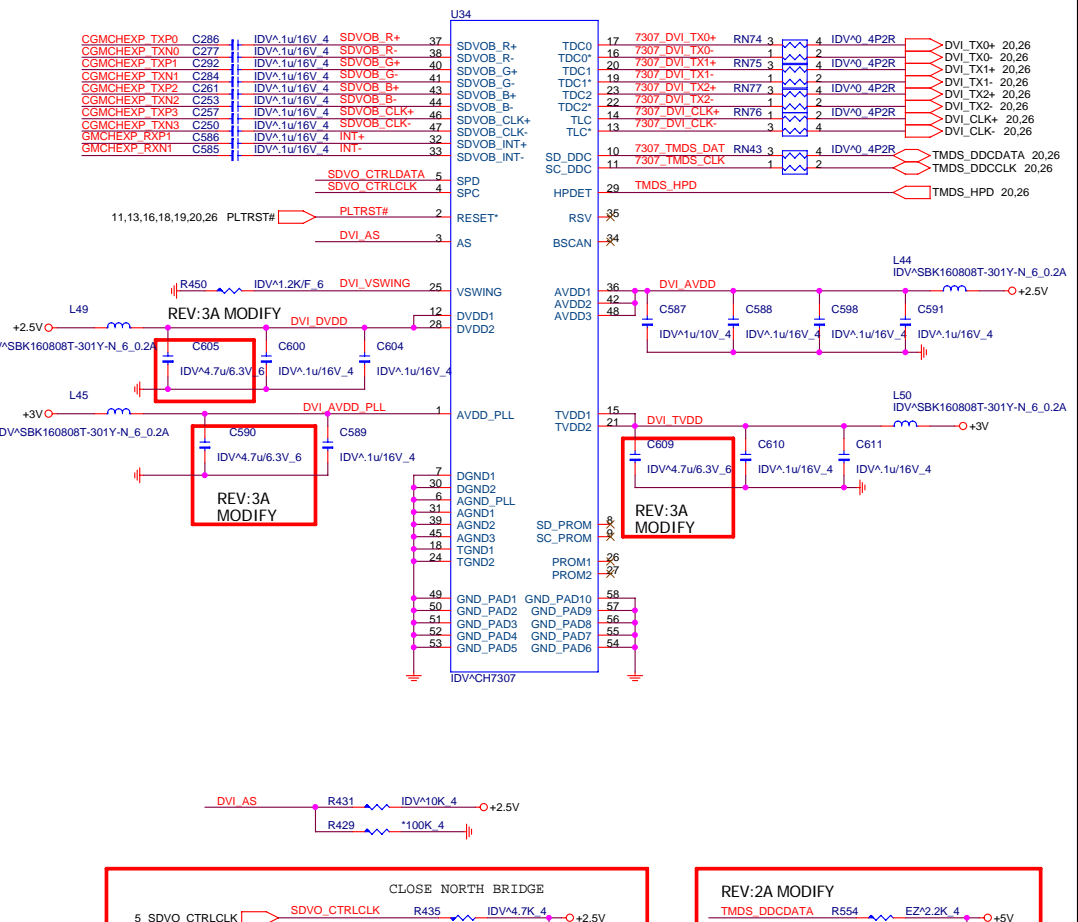


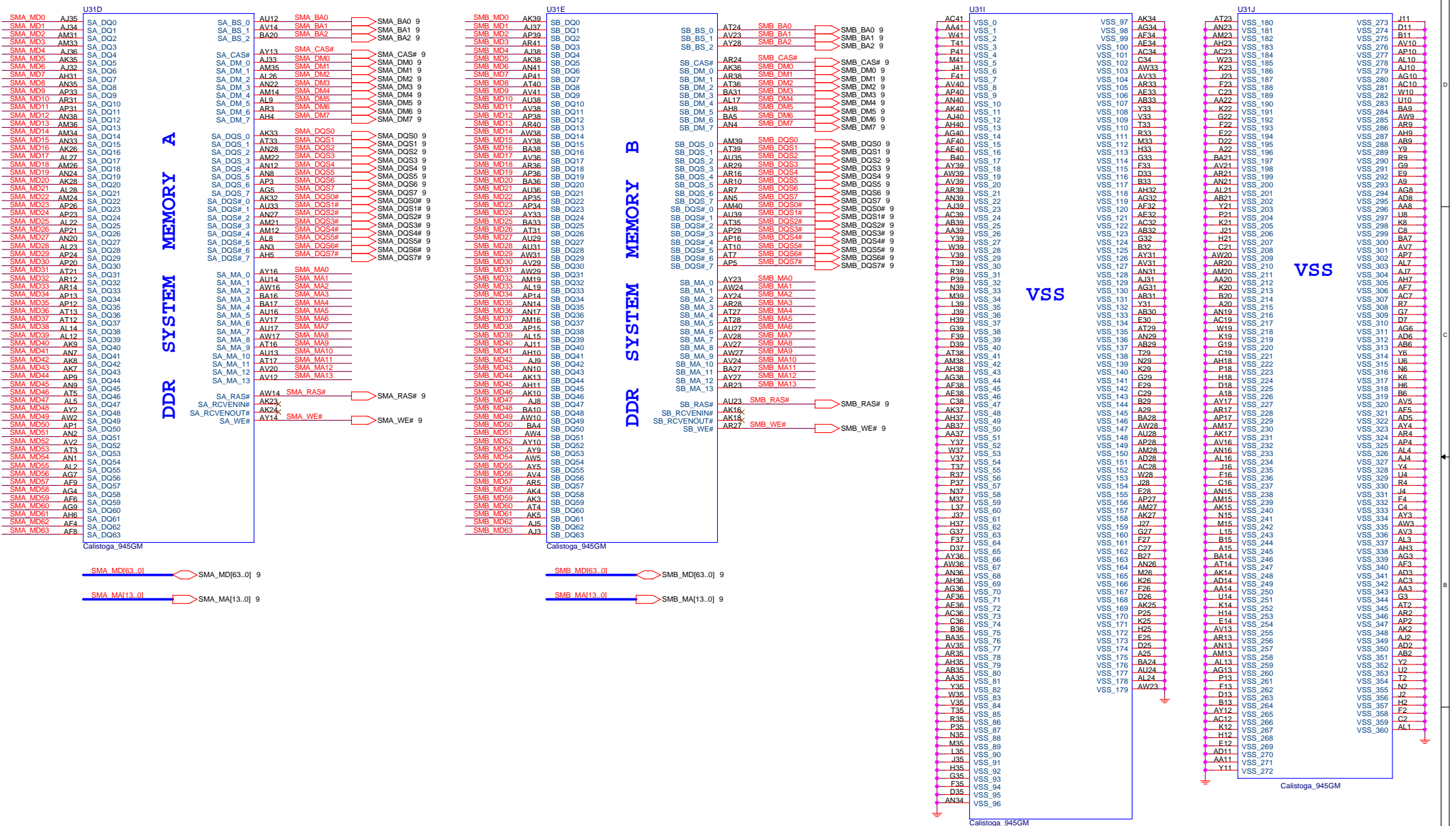
Size Document Number
GMCH (HOST / DMI)
 Date: Thursday, June 29, 2006 Sheet 5 of 29 Rev 1A

NB_945GM/PM/940GML

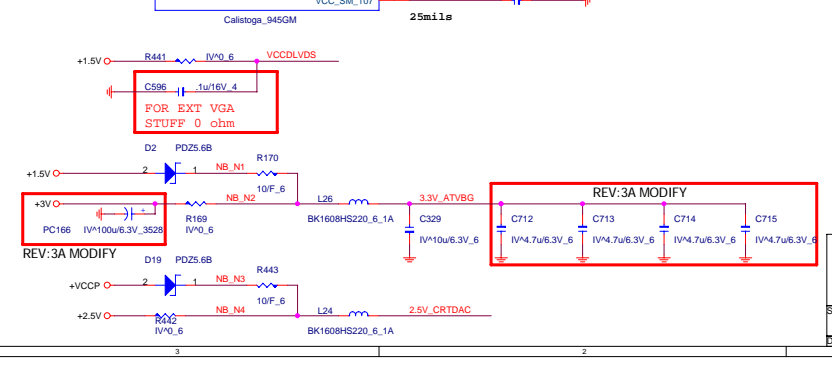
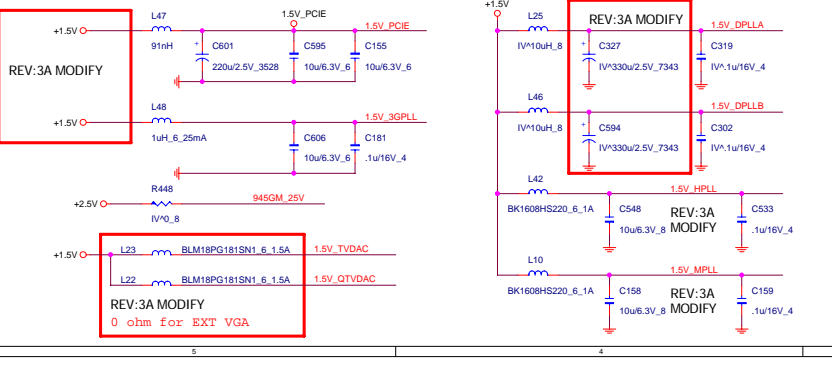
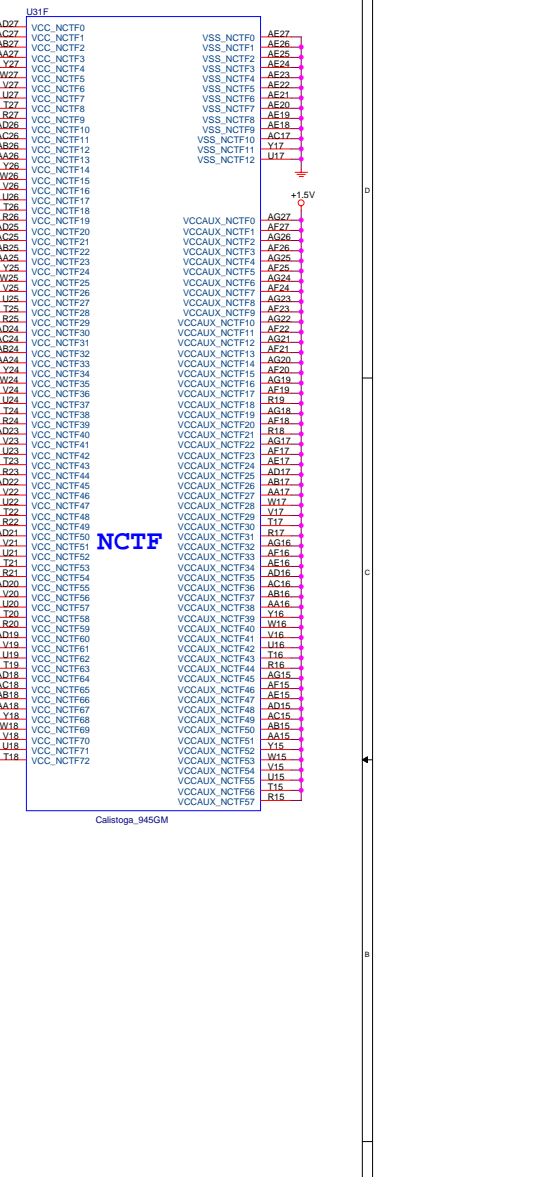
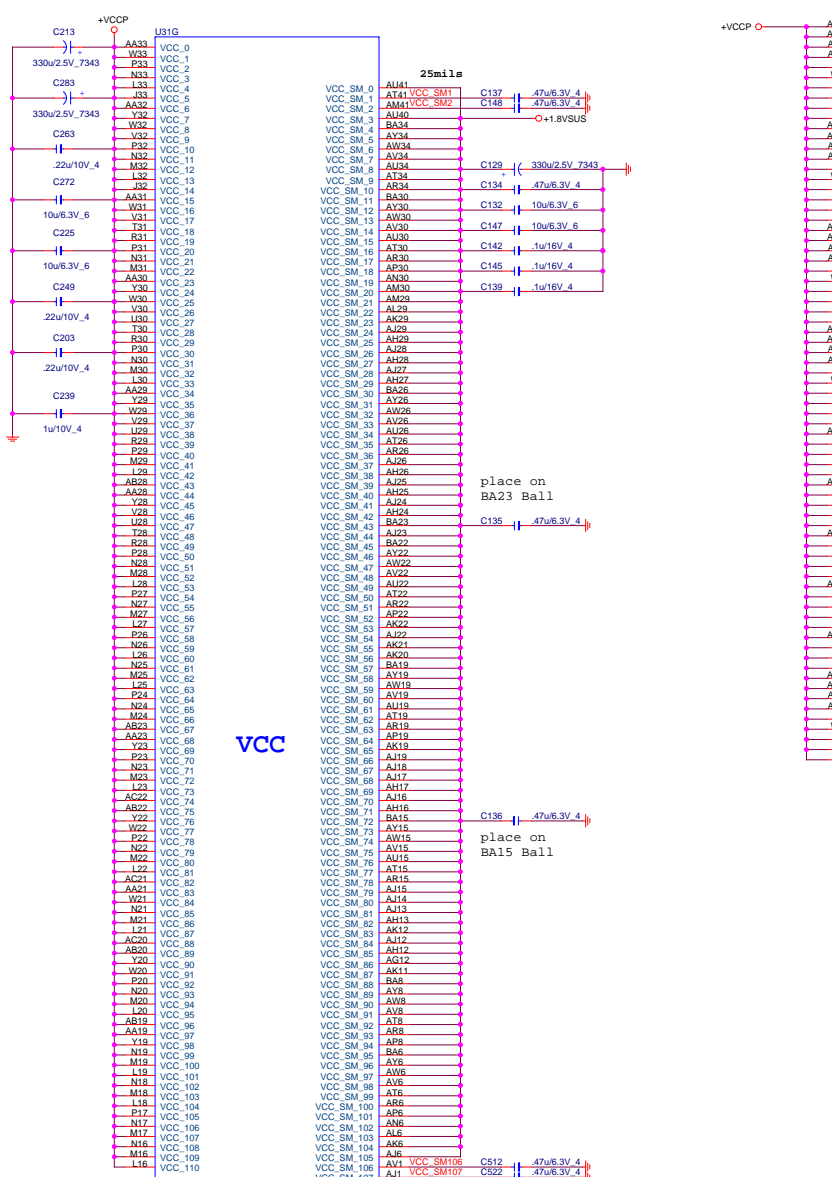
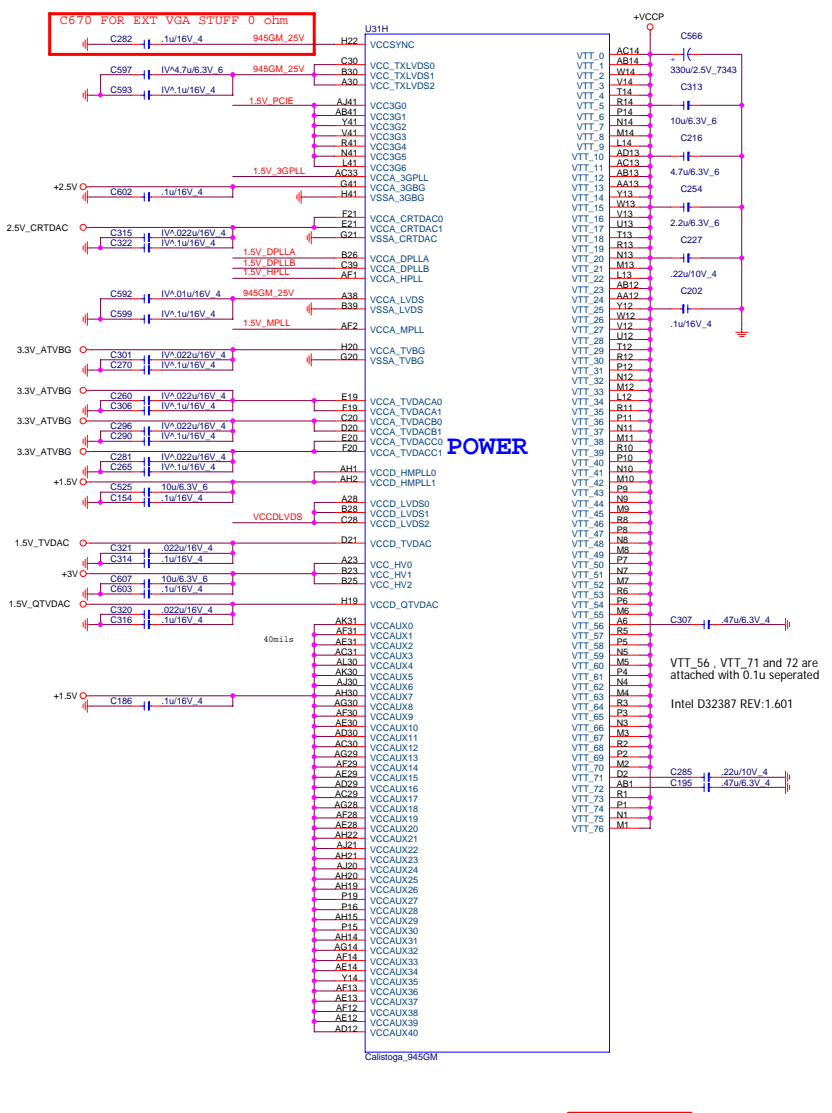


DVO_CH7307





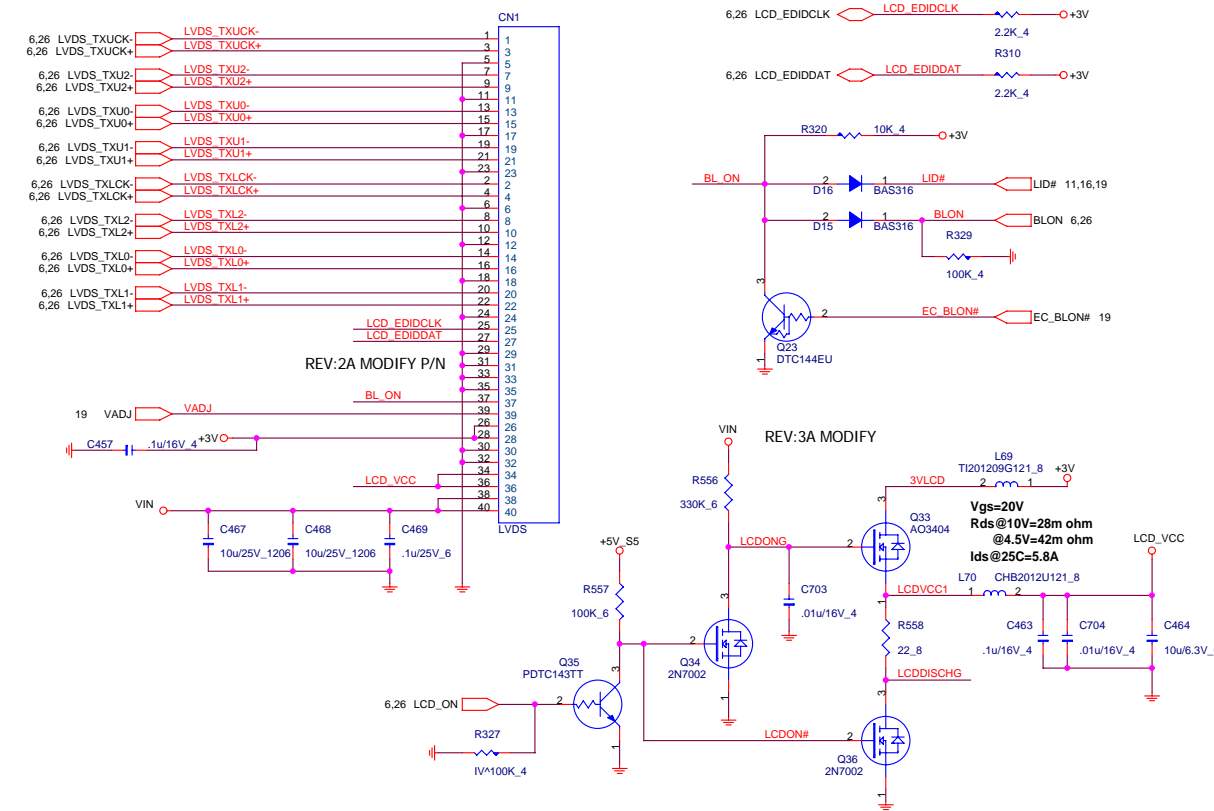
NB_945GM/PM/940GML



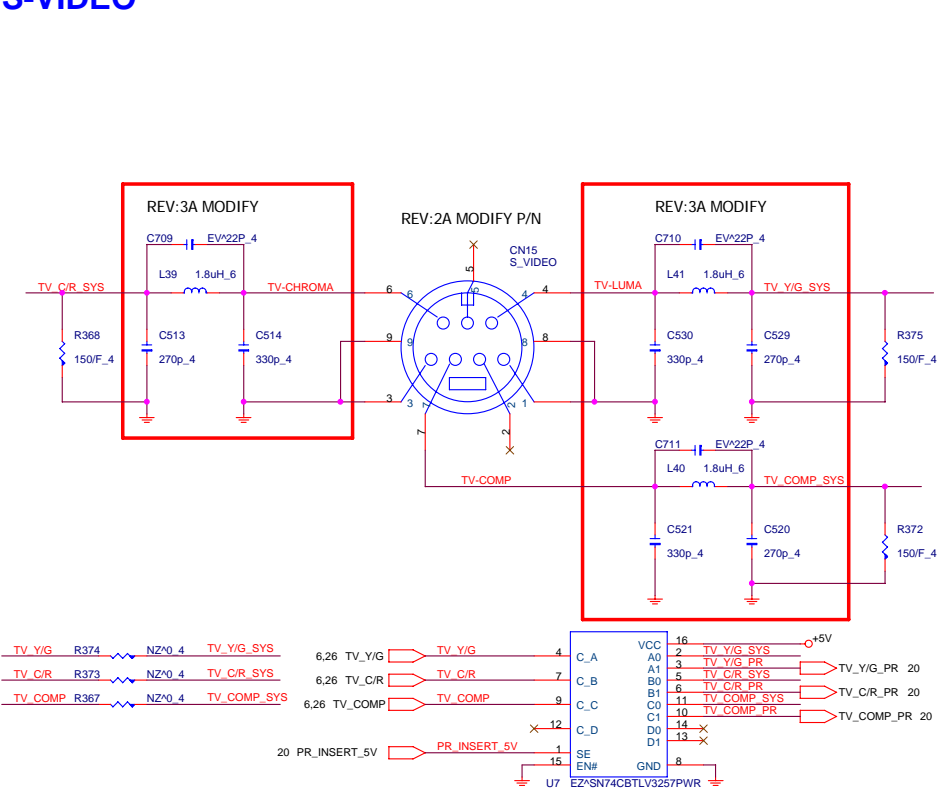
PROJECT: ZR1
Quanta Computer Inc.

Size: Document Number
GMCH (POWER)
Date: Thursday, June 29, 2006 | Sheet: 8 of 29

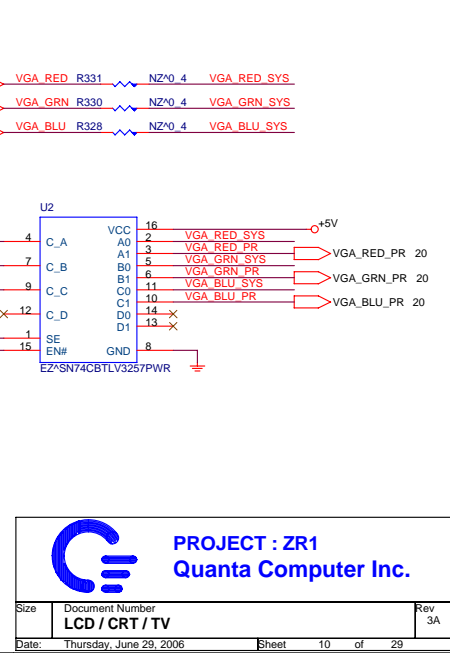
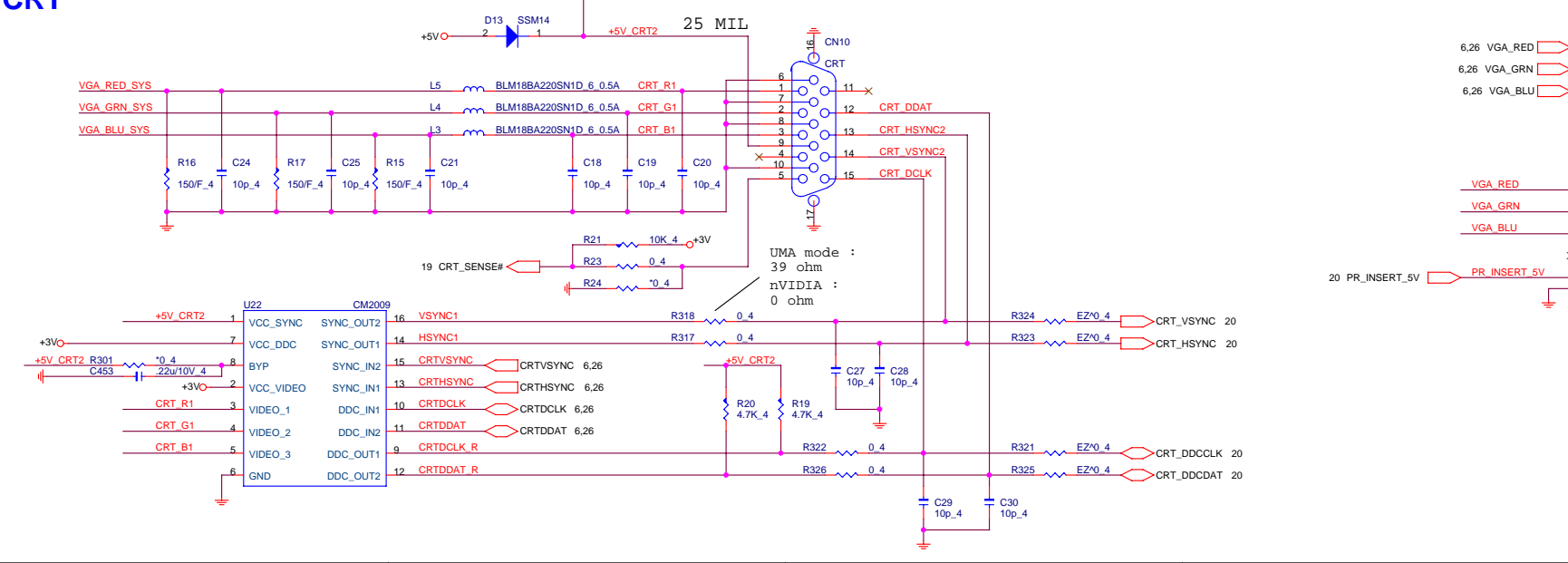
LVDS

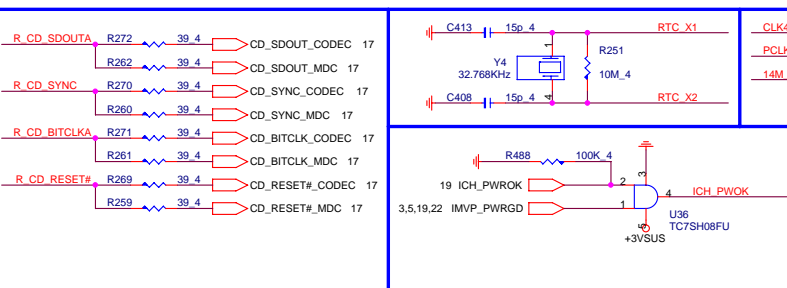
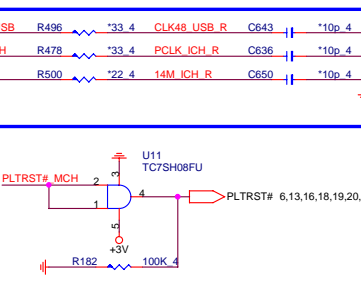
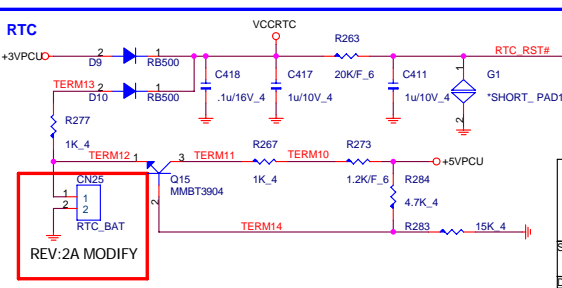
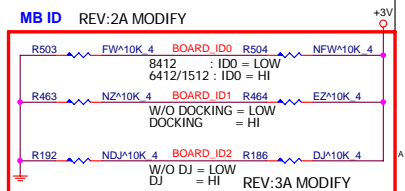
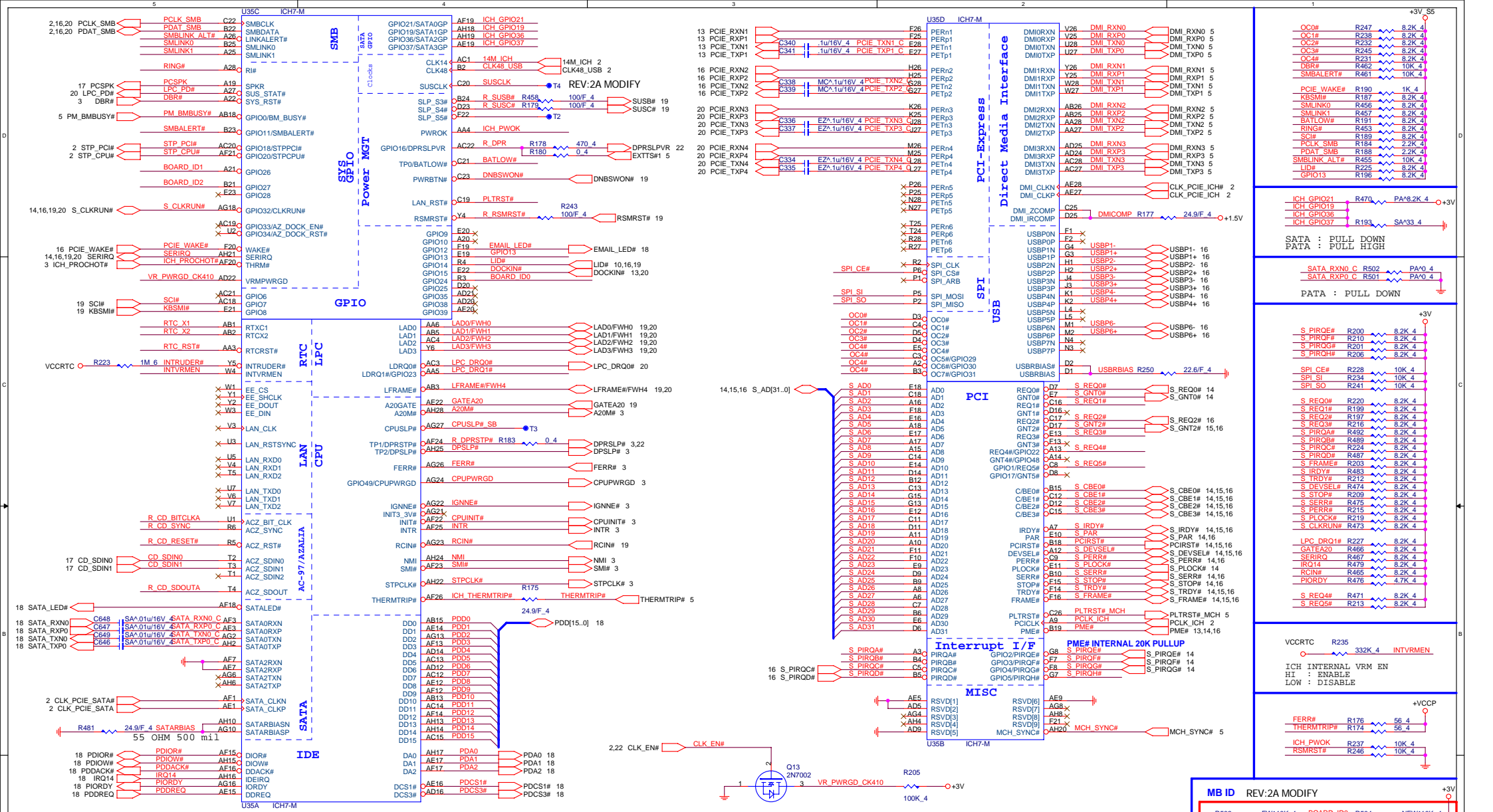


S-VIDEO



CRT





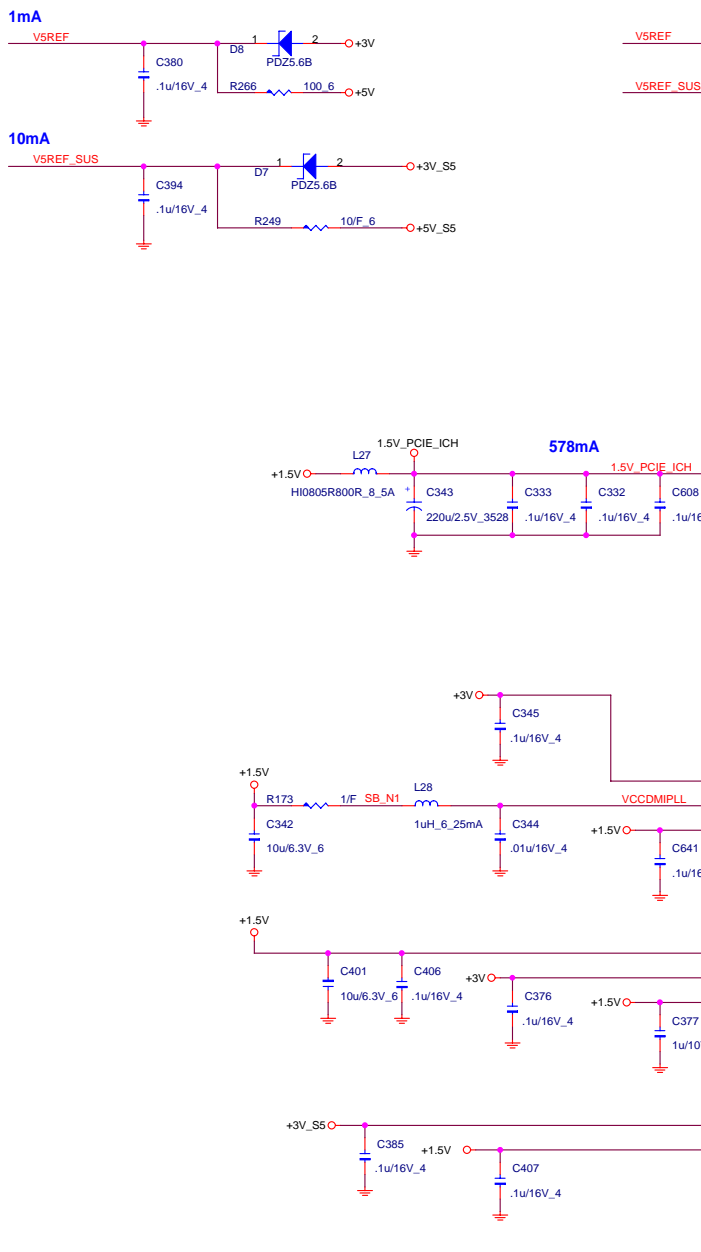
PROJECT : ZR1
Quanta Computer Inc.

Size: _____ Document Number: **IC7 (CPU/PCIE/IDE/USB)** Rev: 3A

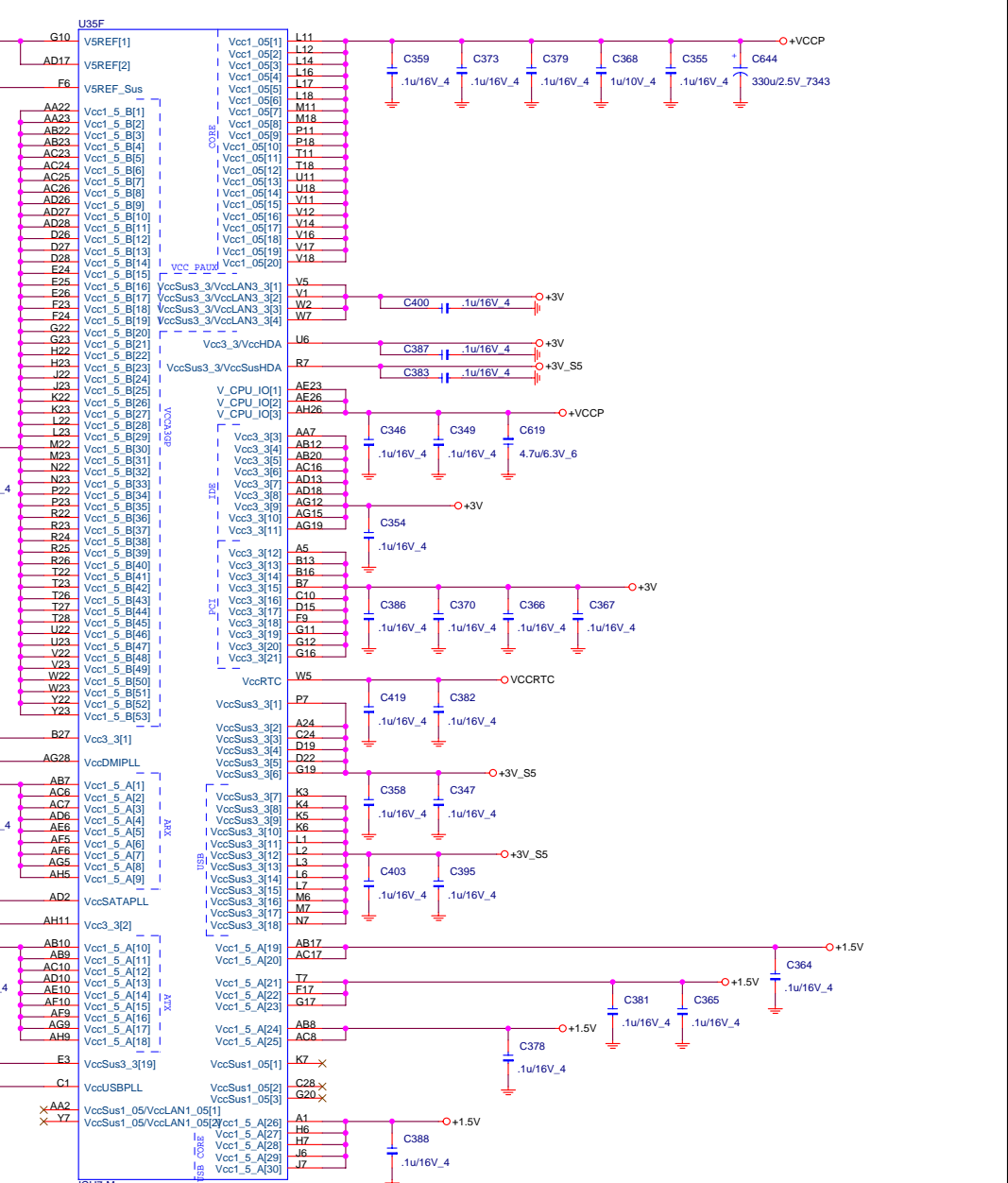
Date: Thursday, June 29, 2006 Sheet: 11 of 29


U35E	VSS	VSS	P28
A4	VSS[11]	VSS[98]	R1
A23	VSS[2]	VSS[99]	R11
B1	VSS[3]	VSS[100]	R12
B8	VSS[4]	VSS[101]	R13
B14	VSS[5]	VSS[102]	R14
B17	VSS[6]	VSS[103]	R15
B20	VSS[8]	VSS[105]	R16
B26	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U12
E1	VSS[19]	VSS[116]	U13
E2	VSS[20]	VSS[117]	U14
E4	VSS[21]	VSS[118]	U15
E8	VSS[22]	VSS[119]	U16
E16	VSS[23]	VSS[120]	U17
F3	VSS[24]	VSS[121]	U24
F4	VSS[25]	VSS[122]	U25
F8	VSS[26]	VSS[123]	U26
F12	VSS[27]	VSS[124]	V2
F27	VSS[28]	VSS[125]	V26
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V27
G5	VSS[32]	VSS[129]	V28
G6	VSS[33]	VSS[130]	V28
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W4
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G28	VSS[39]	VSS[136]	Y24
G28	VSS[40]	VSS[137]	Y27
H4	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	AA1
H5	VSS[43]	VSS[140]	AA24
H24	VSS[44]	VSS[141]	AA25
H28	VSS[45]	VSS[142]	AA26
H28	VSS[46]	VSS[143]	AB4
J1	VSS[47]	VSS[144]	AB6
J2	VSS[48]	VSS[145]	AB11
J5	VSS[49]	VSS[146]	AB14
J24	VSS[50]	VSS[147]	AB16
J25	VSS[51]	VSS[148]	AB19
J26	VSS[52]	VSS[149]	AB21
K24	VSS[53]	VSS[150]	AB24
K27	VSS[54]	VSS[151]	AB27
K28	VSS[55]	VSS[152]	AB28
L13	VSS[56]	VSS[153]	AC2
L18	VSS[57]	VSS[154]	AC5
L24	VSS[58]	VSS[155]	AC9
L25	VSS[59]	VSS[156]	AC11
L28	VSS[60]	VSS[157]	AD1
M3	VSS[61]	VSS[158]	AD3
M8	VSS[62]	VSS[159]	AD4
M5	VSS[63]	VSS[160]	AD7
M12	VSS[64]	VSS[161]	AD8
M13	VSS[65]	VSS[162]	AD11
M14	VSS[66]	VSS[163]	AD15
M15	VSS[67]	VSS[164]	AD19
M16	VSS[68]	VSS[165]	AD23
M17	VSS[69]	VSS[166]	AE2
M24	VSS[70]	VSS[167]	AE4
M27	VSS[71]	VSS[168]	AE8
N1	VSS[72]	VSS[169]	AE11
N2	VSS[73]	VSS[170]	AE13
N6	VSS[74]	VSS[171]	AE18
N8	VSS[75]	VSS[172]	AE21
N11	VSS[76]	VSS[173]	AE24
N12	VSS[77]	VSS[174]	AE25
N13	VSS[78]	VSS[175]	AF2
N14	VSS[79]	VSS[176]	AF4
N15	VSS[80]	VSS[177]	AF8
N16	VSS[81]	VSS[178]	AF27
N17	VSS[82]	VSS[179]	AF28
N18	VSS[83]	VSS[180]	AG1
N24	VSS[84]	VSS[181]	AG3
N25	VSS[85]	VSS[182]	AG7
N26	VSS[86]	VSS[183]	AG11
P3	VSS[87]	VSS[184]	AG14
P4	VSS[88]	VSS[185]	AG17
P12	VSS[89]	VSS[186]	AG20
P13	VSS[90]	VSS[187]	AG25
P14	VSS[91]	VSS[188]	AH1
P15	VSS[92]	VSS[189]	AH3
P16	VSS[93]	VSS[190]	AH7
P17	VSS[94]	VSS[191]	AH12
P24	VSS[95]	VSS[192]	AH23
P27	VSS[96]	VSS[193]	AH27
P27	VSS[97]	VSS[194]	AH27

1mA
10mA



U35F	VCC	VCC
AA22	Vcc1_5_B[1]	Vcc1_5_B[1]
AA23	Vcc1_5_B[2]	Vcc1_5_B[2]
AB22	Vcc1_5_B[3]	Vcc1_5_B[3]
AB23	Vcc1_5_B[4]	Vcc1_5_B[4]
AC23	Vcc1_5_B[5]	Vcc1_5_B[5]
AC24	Vcc1_5_B[6]	Vcc1_5_B[6]
AC25	Vcc1_5_B[7]	Vcc1_5_B[7]
AC26	Vcc1_5_B[8]	Vcc1_5_B[8]
AD26	Vcc1_5_B[9]	Vcc1_5_B[9]
AD27	Vcc1_5_B[10]	Vcc1_5_B[10]
AD28	Vcc1_5_B[11]	Vcc1_5_B[11]
D26	Vcc1_5_B[12]	Vcc1_5_B[12]
D27	Vcc1_5_B[13]	Vcc1_5_B[13]
D28	Vcc1_5_B[14]	Vcc1_5_B[14]
E24	Vcc1_5_B[15]	Vcc1_5_B[15]
E25	Vcc1_5_B[16]	Vcc1_5_B[16]
E26	Vcc1_5_B[17]	Vcc1_5_B[17]
F23	Vcc1_5_B[18]	Vcc1_5_B[18]
F24	Vcc1_5_B[19]	Vcc1_5_B[19]
G22	Vcc1_5_B[20]	Vcc1_5_B[20]
G23	Vcc1_5_B[21]	Vcc1_5_B[21]
H22	Vcc1_5_B[22]	Vcc1_5_B[22]
H23	Vcc1_5_B[23]	Vcc1_5_B[23]
I22	Vcc1_5_B[24]	Vcc1_5_B[24]
I23	Vcc1_5_B[25]	Vcc1_5_B[25]
K22	Vcc1_5_B[26]	Vcc1_5_B[26]
K23	Vcc1_5_B[27]	Vcc1_5_B[27]
L22	Vcc1_5_B[28]	Vcc1_5_B[28]
L23	Vcc1_5_B[29]	Vcc1_5_B[29]
M22	Vcc1_5_B[30]	Vcc1_5_B[30]
M23	Vcc1_5_B[31]	Vcc1_5_B[31]
N22	Vcc1_5_B[32]	Vcc1_5_B[32]
N23	Vcc1_5_B[33]	Vcc1_5_B[33]
P22	Vcc1_5_B[34]	Vcc1_5_B[34]
R22	Vcc1_5_B[35]	Vcc1_5_B[35]
R23	Vcc1_5_B[36]	Vcc1_5_B[36]
R24	Vcc1_5_B[37]	Vcc1_5_B[37]
R25	Vcc1_5_B[38]	Vcc1_5_B[38]
R26	Vcc1_5_B[39]	Vcc1_5_B[39]
T22	Vcc1_5_B[40]	Vcc1_5_B[40]
T23	Vcc1_5_B[41]	Vcc1_5_B[41]
T26	Vcc1_5_B[42]	Vcc1_5_B[42]
T27	Vcc1_5_B[43]	Vcc1_5_B[43]
T28	Vcc1_5_B[44]	Vcc1_5_B[44]
T29	Vcc1_5_B[45]	Vcc1_5_B[45]
U22	Vcc1_5_B[46]	Vcc1_5_B[46]
U23	Vcc1_5_B[47]	Vcc1_5_B[47]
V22	Vcc1_5_B[48]	Vcc1_5_B[48]
V23	Vcc1_5_B[49]	Vcc1_5_B[49]
W22	Vcc1_5_B[50]	Vcc1_5_B[50]
W23	Vcc1_5_B[51]	Vcc1_5_B[51]
Y22	Vcc1_5_B[52]	Vcc1_5_B[52]
Y23	Vcc1_5_B[53]	Vcc1_5_B[53]
B27	Vcc3_3[1]	Vcc3_3[1]
AG28	VccDMIPLL	VccDMIPLL
AB7	Vcc1_5_A[1]	Vcc1_5_A[1]
AC6	Vcc1_5_A[2]	Vcc1_5_A[2]
AD6	Vcc1_5_A[3]	Vcc1_5_A[3]
AE6	Vcc1_5_A[4]	Vcc1_5_A[4]
AF6	Vcc1_5_A[5]	Vcc1_5_A[5]
AG6	Vcc1_5_A[6]	Vcc1_5_A[6]
AH6	Vcc1_5_A[7]	Vcc1_5_A[7]
AH5	Vcc1_5_A[8]	Vcc1_5_A[8]
AD2	VccSATAPLL	VccSATAPLL
AH11	Vcc3_3[2]	Vcc3_3[2]
AB10	Vcc1_5_A[10]	Vcc1_5_A[10]
AC10	Vcc1_5_A[11]	Vcc1_5_A[11]
AD10	Vcc1_5_A[12]	Vcc1_5_A[12]
AE10	Vcc1_5_A[13]	Vcc1_5_A[13]
AF10	Vcc1_5_A[14]	Vcc1_5_A[14]
AG9	Vcc1_5_A[15]	Vcc1_5_A[15]
AH9	Vcc1_5_A[16]	Vcc1_5_A[16]
AH9	Vcc1_5_A[17]	Vcc1_5_A[17]
AH9	Vcc1_5_A[18]	Vcc1_5_A[18]
E3	VccSus3_3[19]	VccSus3_3[19]
C1	VccUSBPLL	VccUSBPLL
AA2	VccSus1_05/VccLAN1_05[1]	VccSus1_05/VccLAN1_05[1]
Y7	VccSus1_05/VccLAN1_05[2]	VccSus1_05/VccLAN1_05[2]



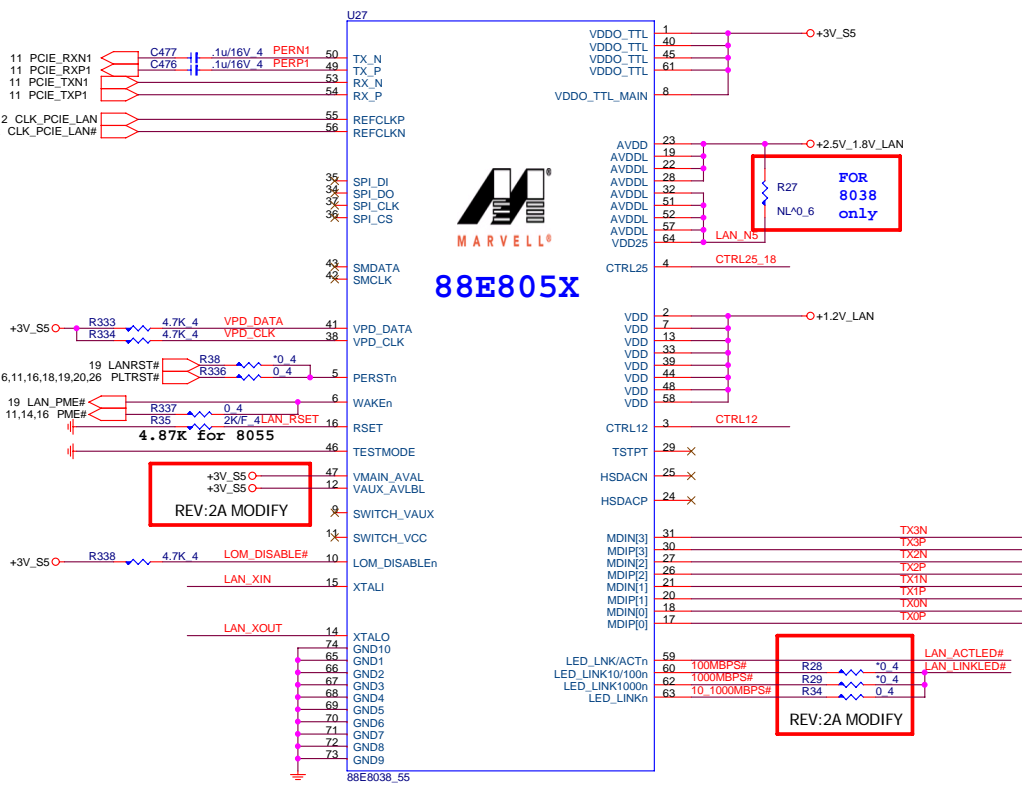


PROJECT : ZR1
Quanta Computer Inc.

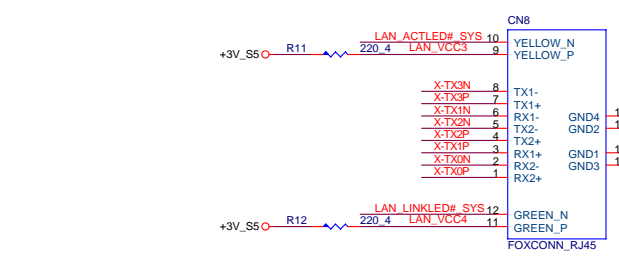
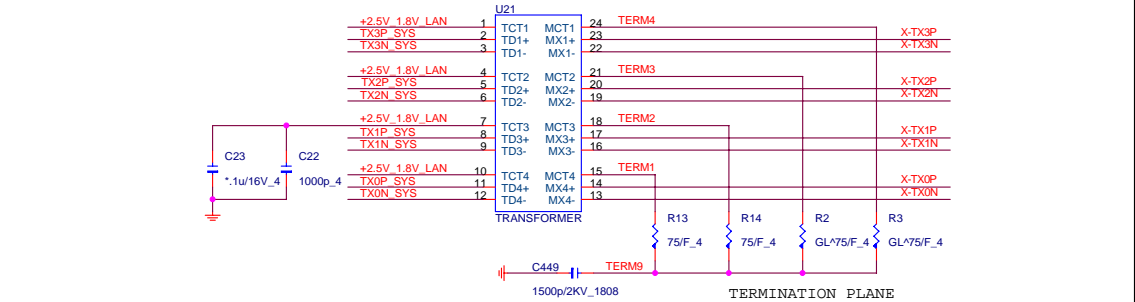
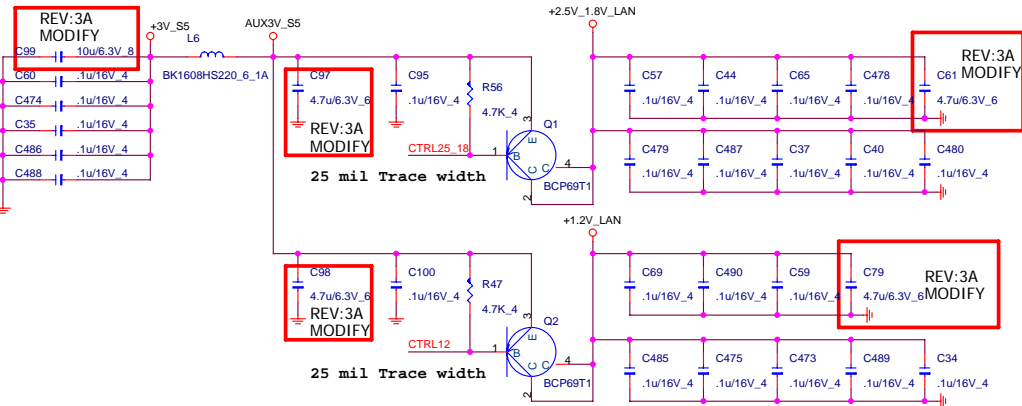
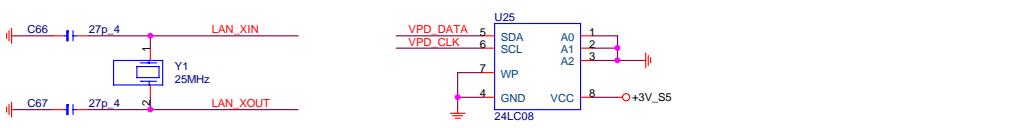
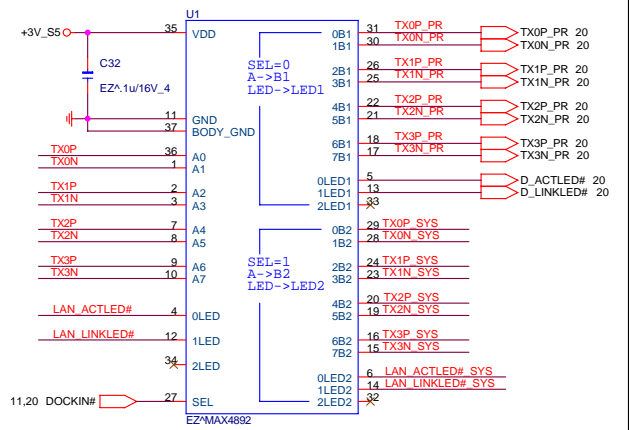
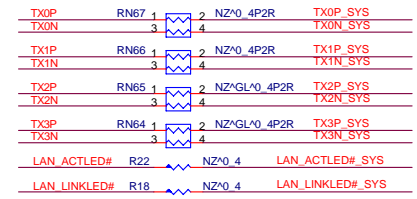
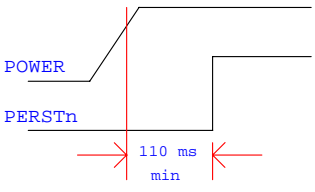
Size	Document Number	Rev
	ICH7 (POWER)	1A
Date:	Thursday, June 29, 2006	Sheet 12 of 29



88E805X



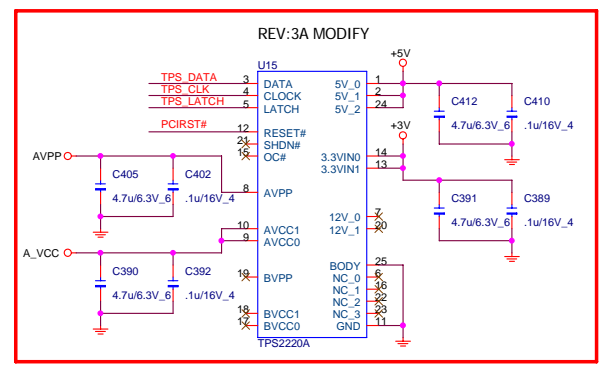
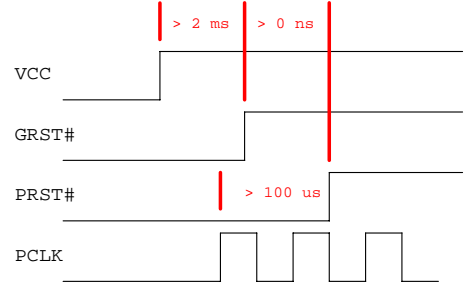
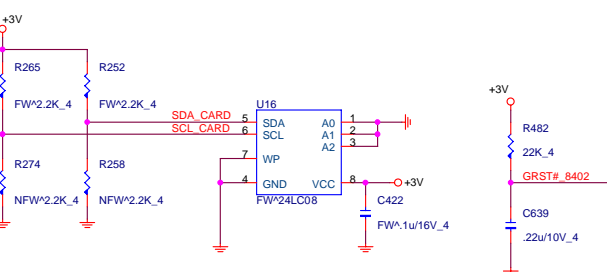
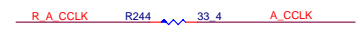
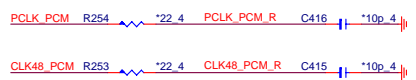
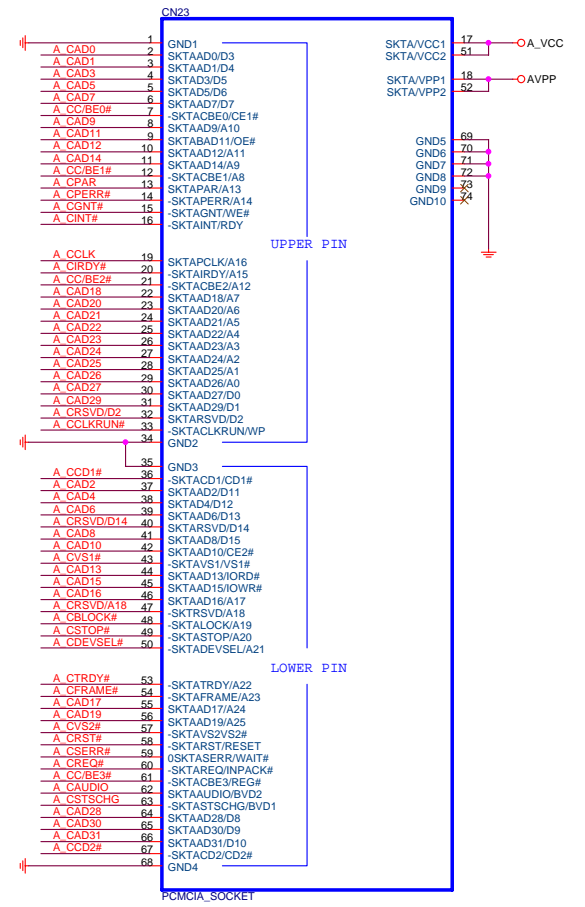
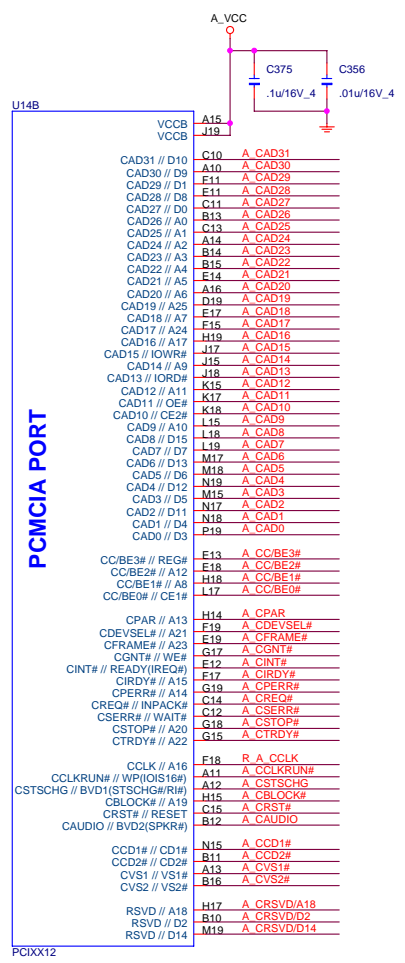
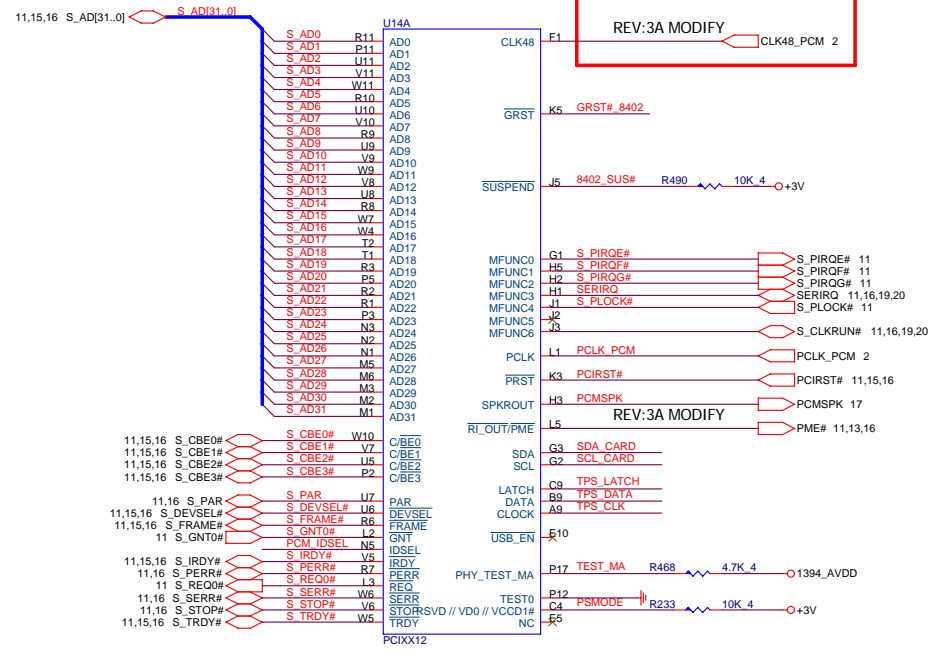
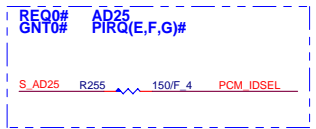
RESET TIMING



PROJECT : ZR1
Quanta Computer Inc.
Size Document Number
LAN (MARVELL 8038/8055)
Date: Thursday, June 29, 2006 1 Sheet 13 of 29

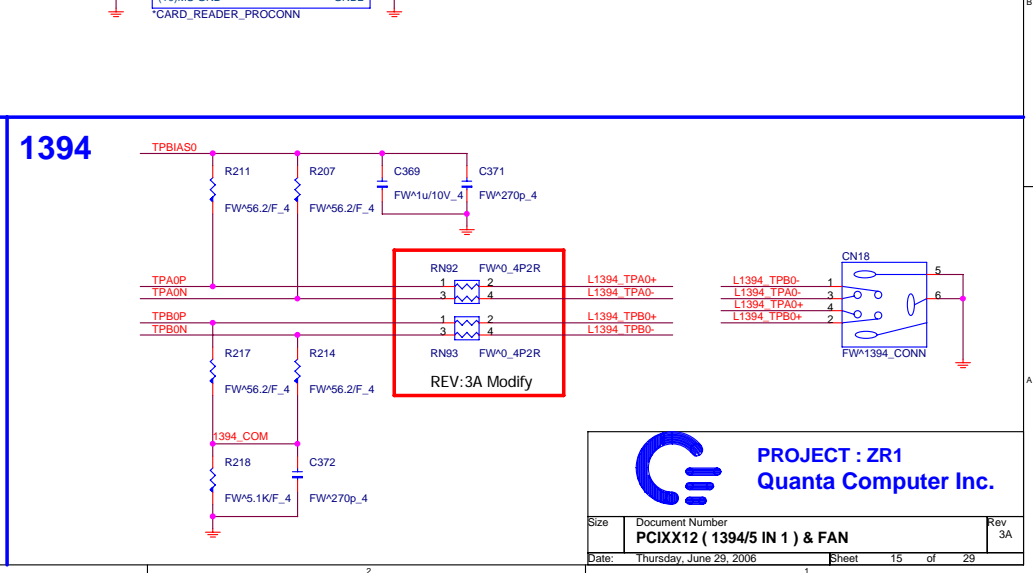
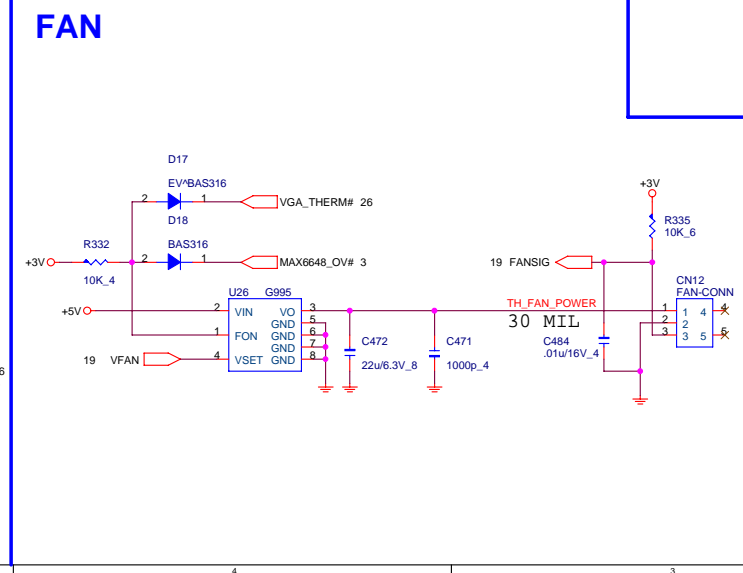
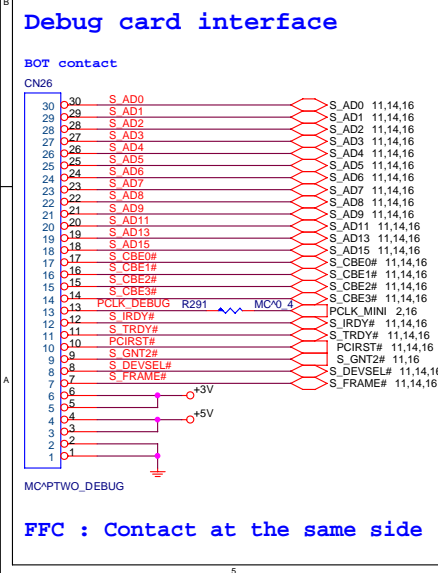
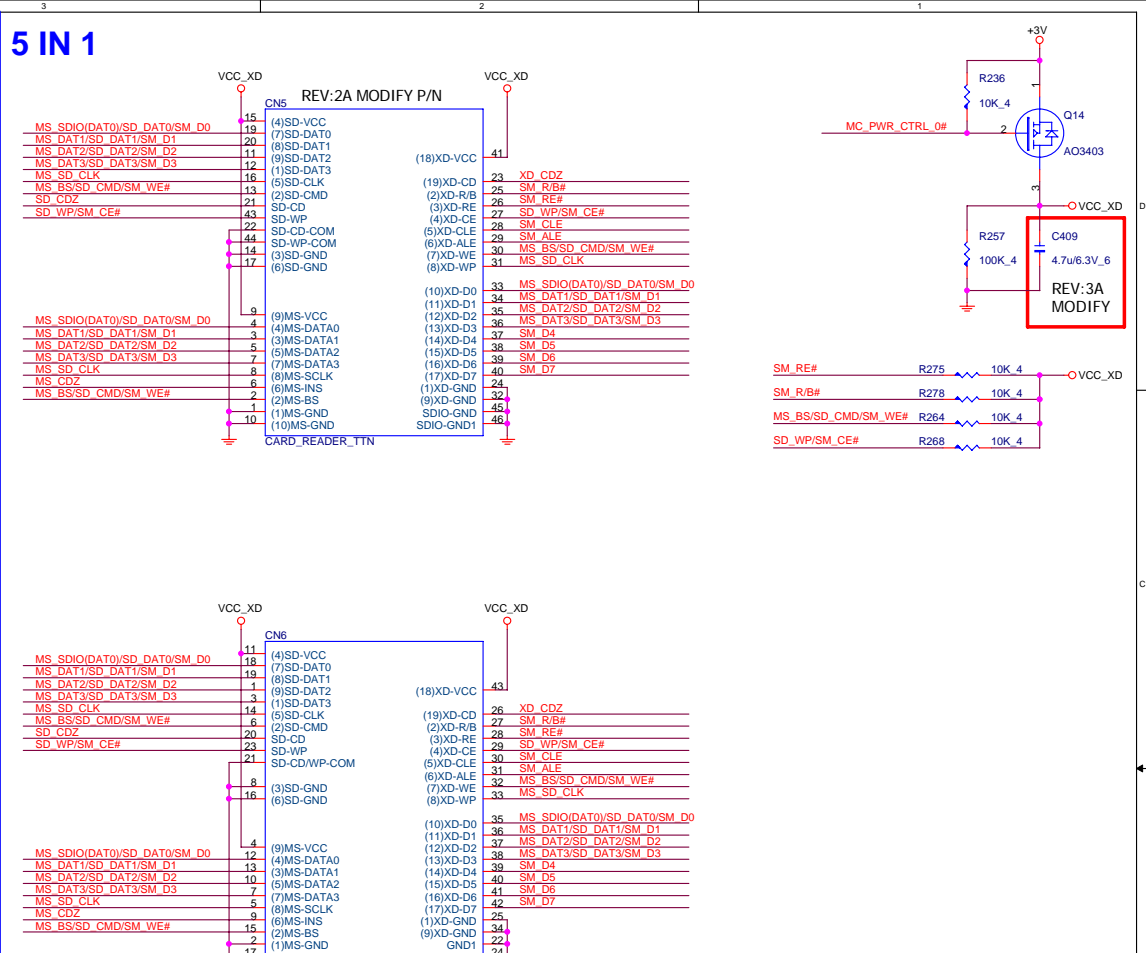
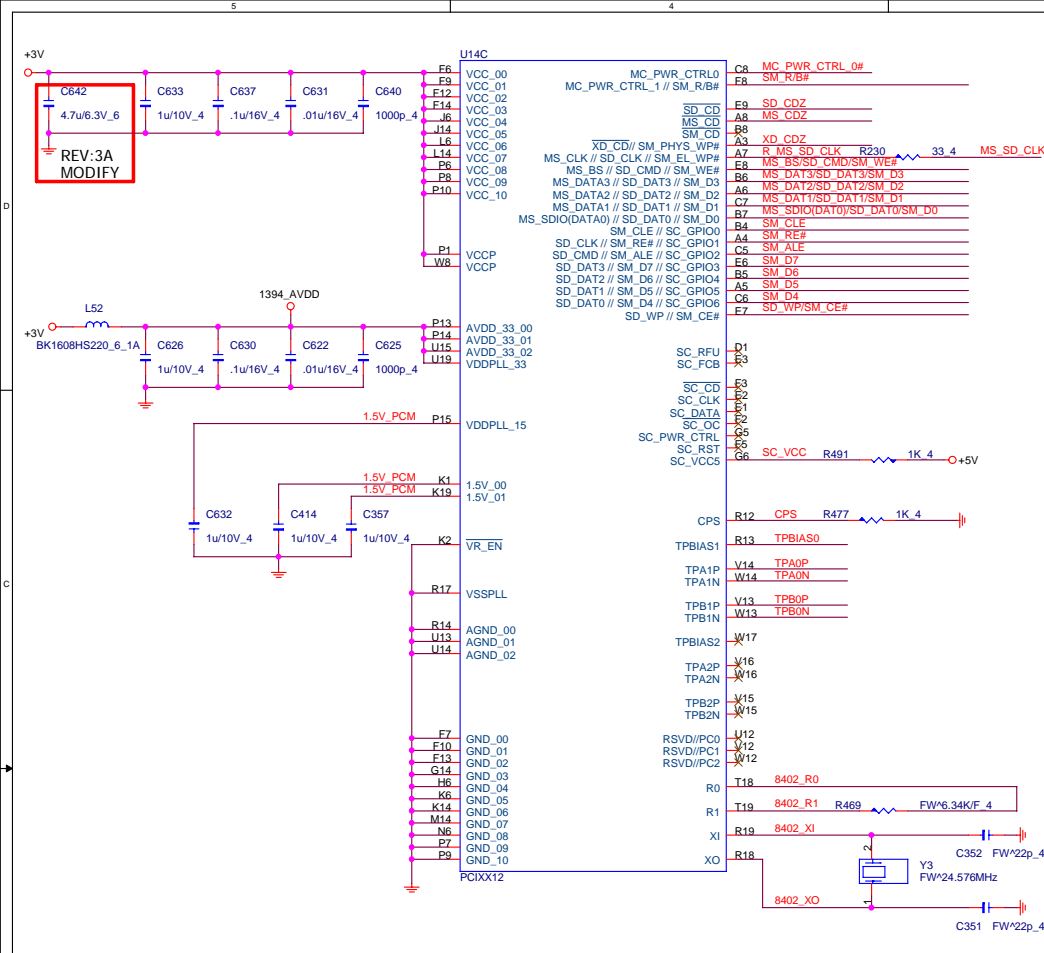
PCIXX12_PCMCIA

PCI8412 : AJ084120T08 PCMCIA / 1394 / 5 IN 1
 PCI6412 : AL064120T04 PCMCIA / 5 IN 1

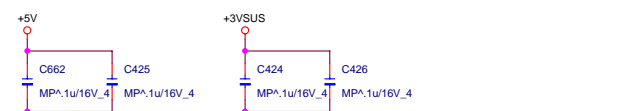
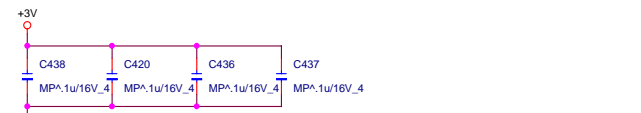
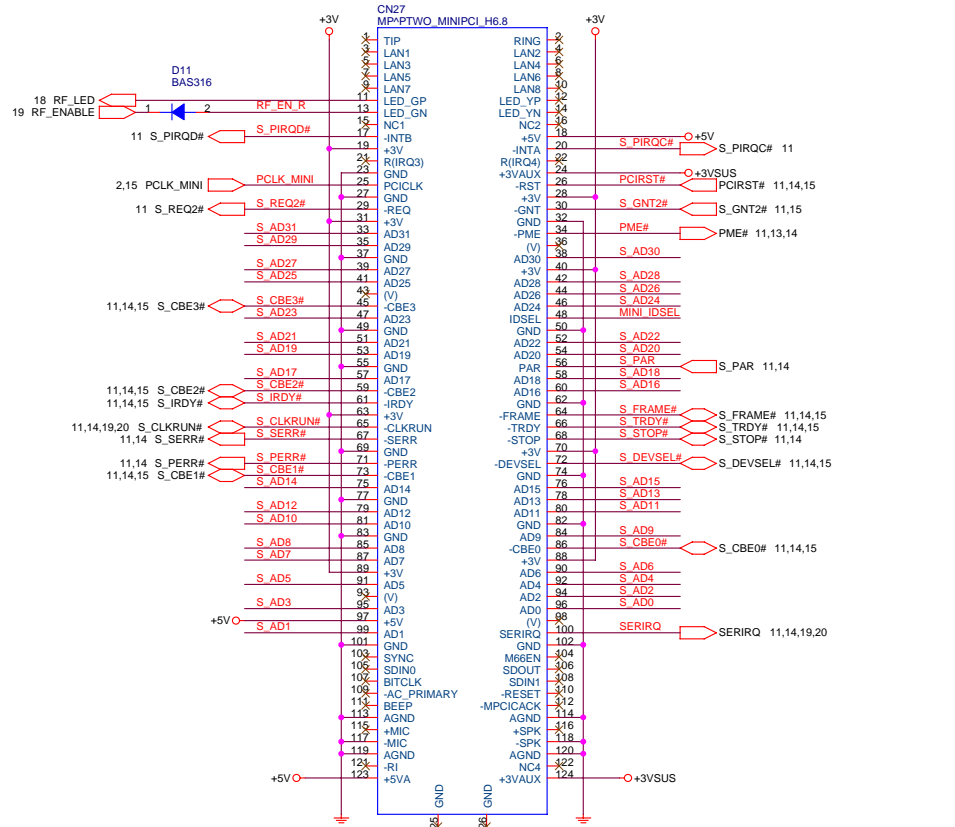
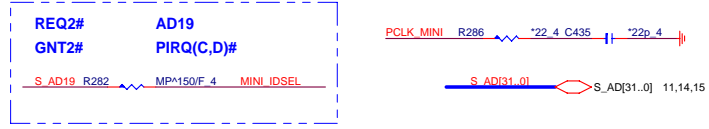


PROJECT : ZR1
Quanta Computer Inc.

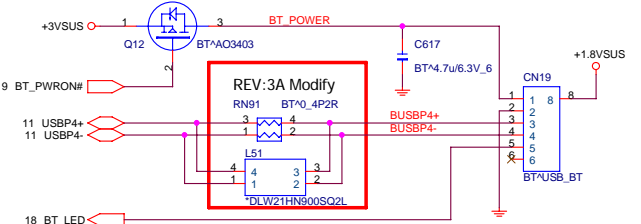
Size	Document Number	Rev
	PCIXX12 (PCMCIA)	3A
Date:	Thursday, June 29, 2006	Sheet 14 of 29



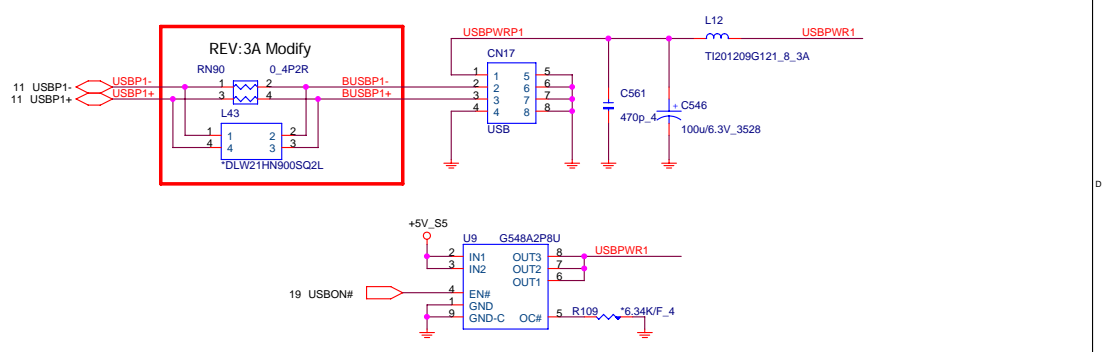
MINI-PCI



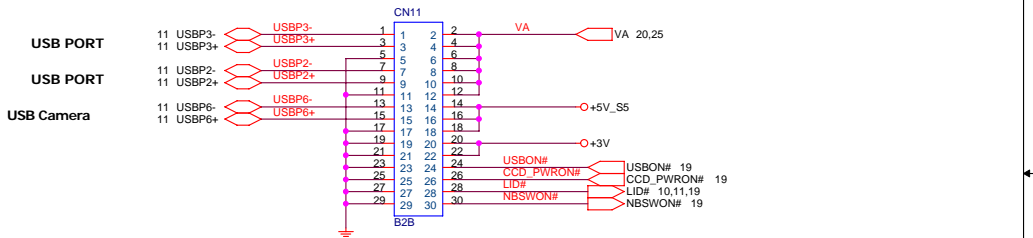
BLUETOOTH



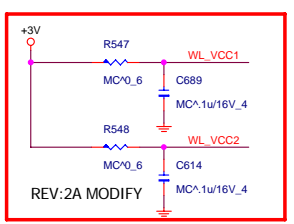
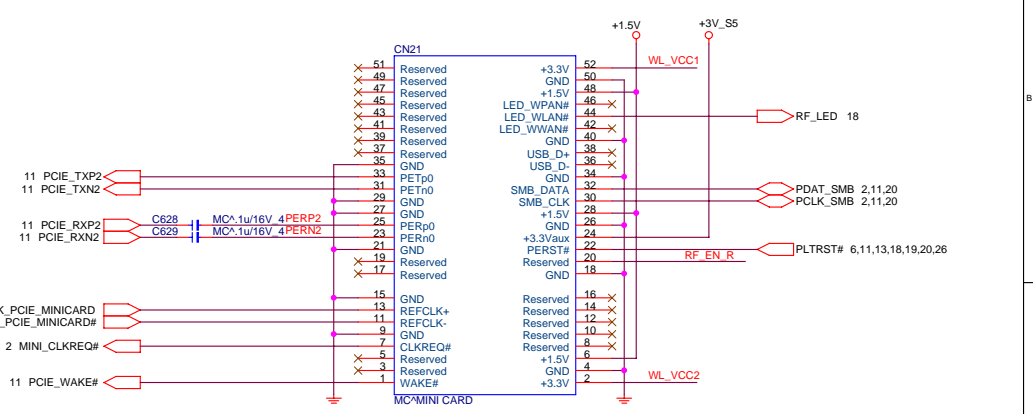
USB



DC/B CONNECTOR



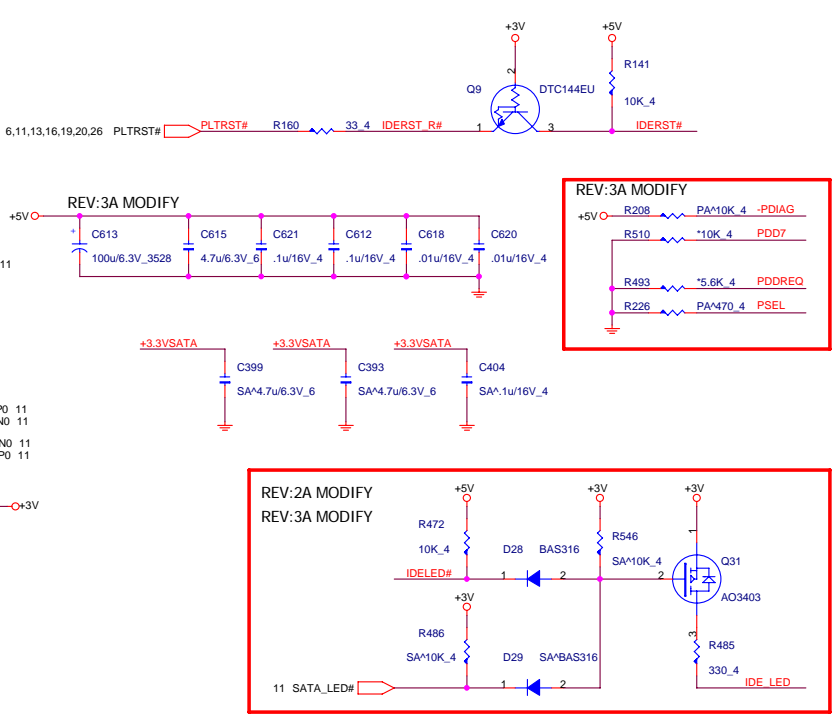
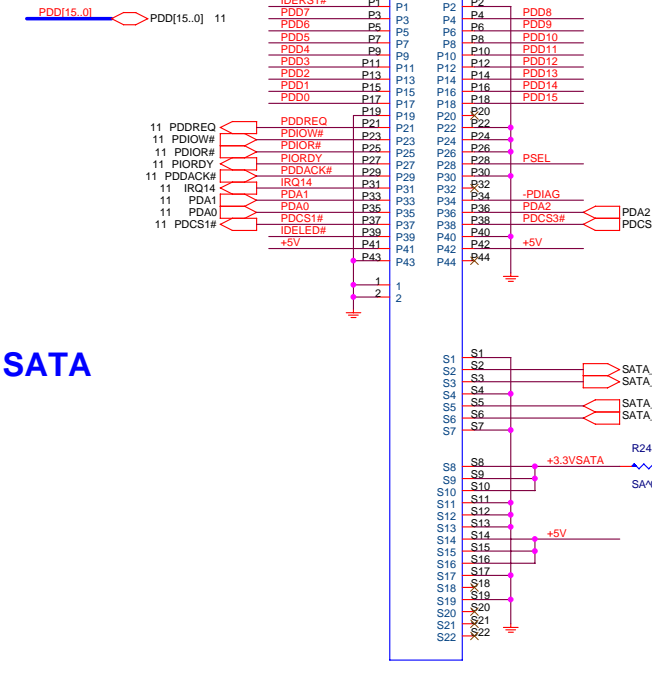
MINI-CARD



PROJECT : ZR1
Quanta Computer Inc.

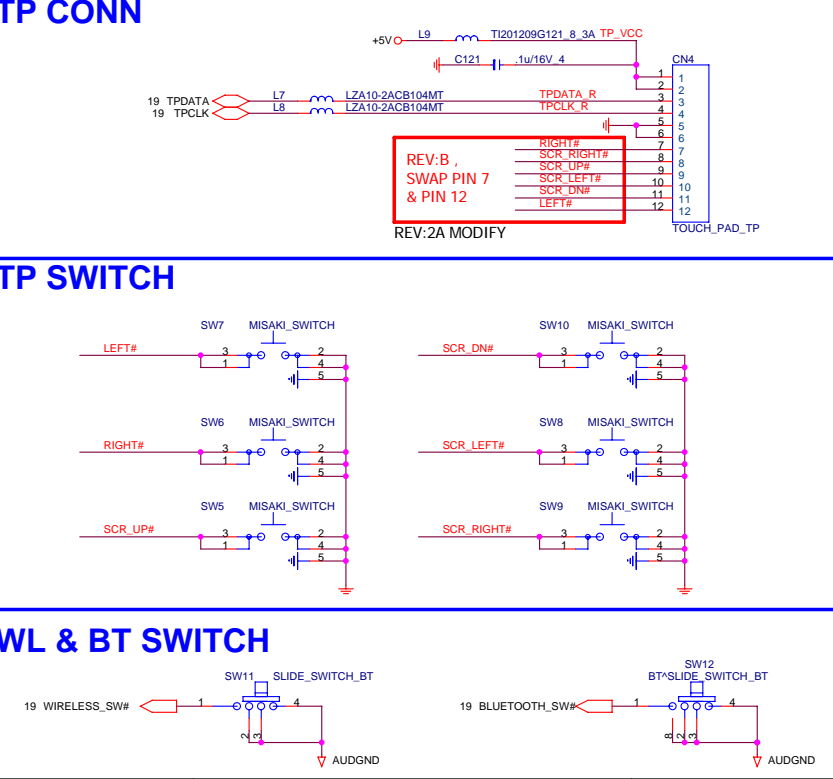
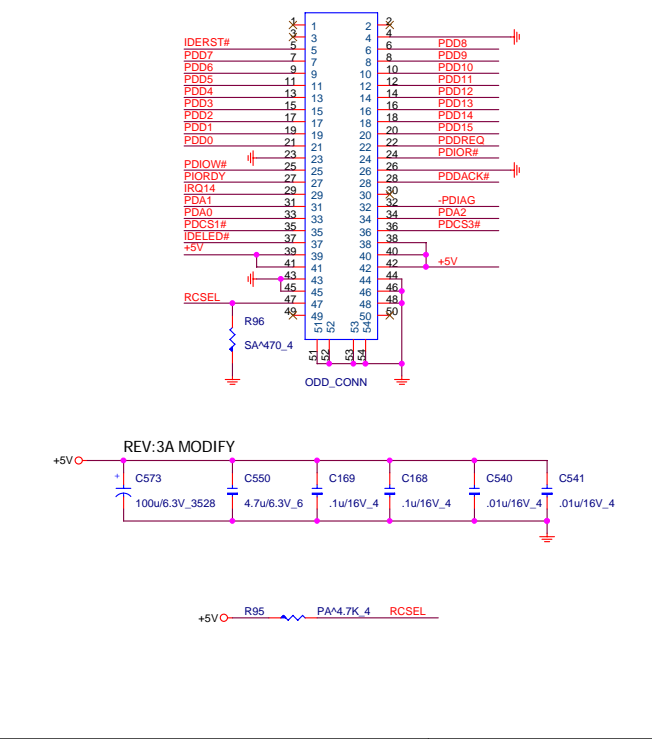
Size	Document Number	Rev
	MINI_CARDPCI/USB/BT/DC	3A
Date:	Thursday, June 29, 2006	Sheet 16 of 29

HDD

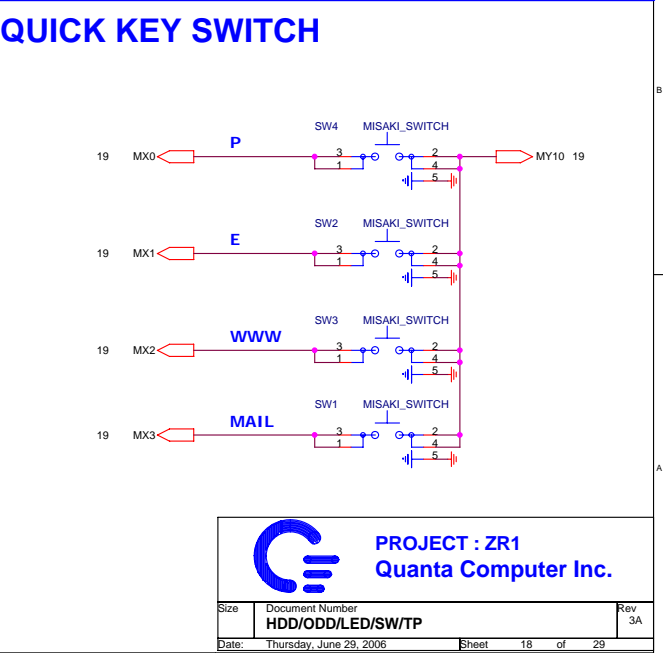
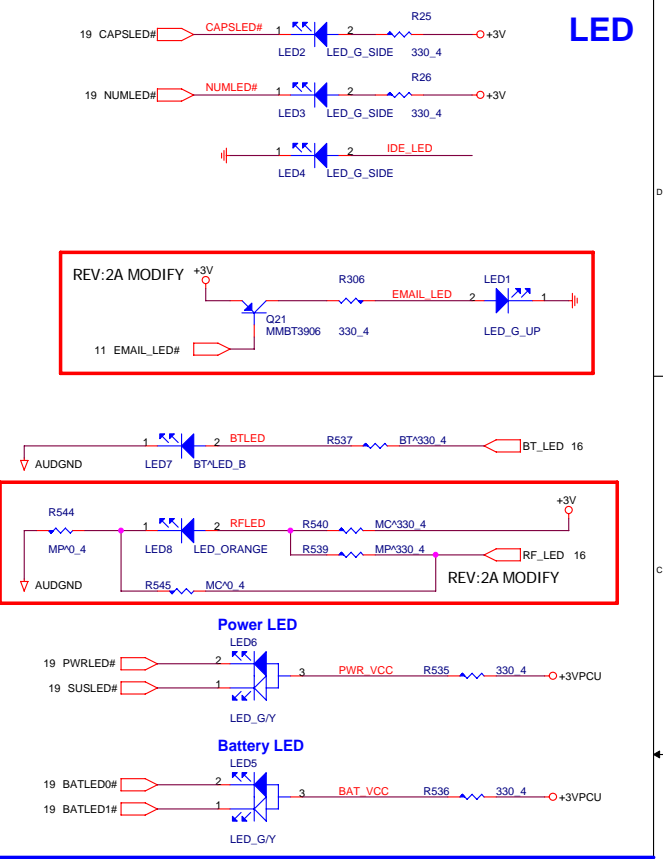


SATA

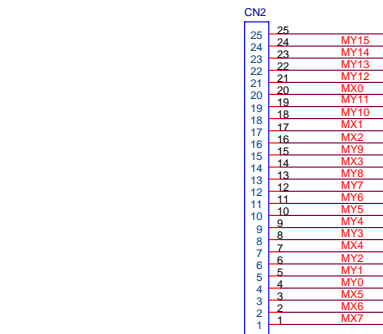
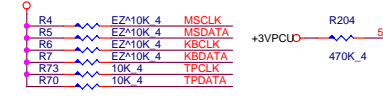
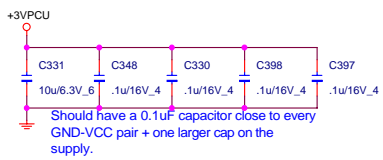
ODD



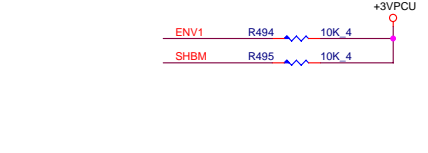
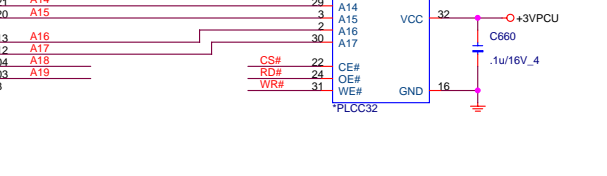
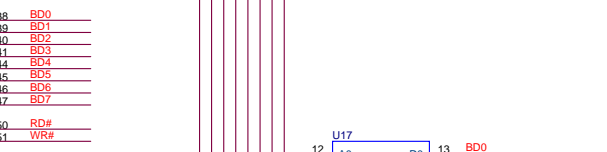
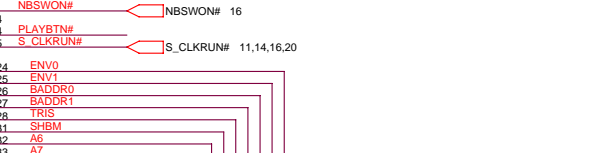
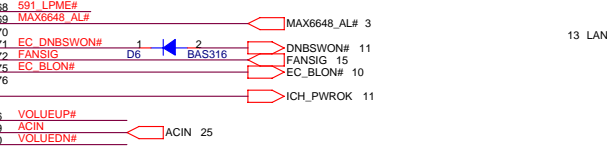
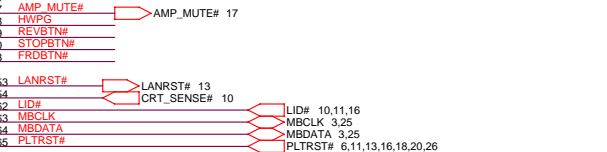
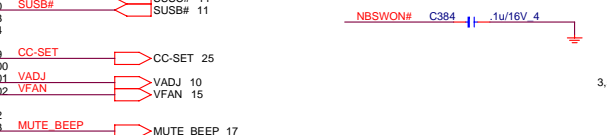
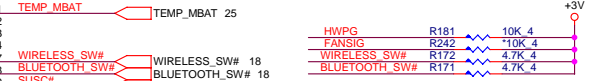
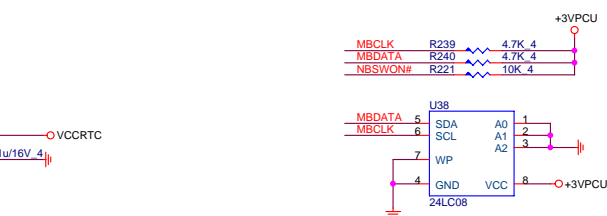
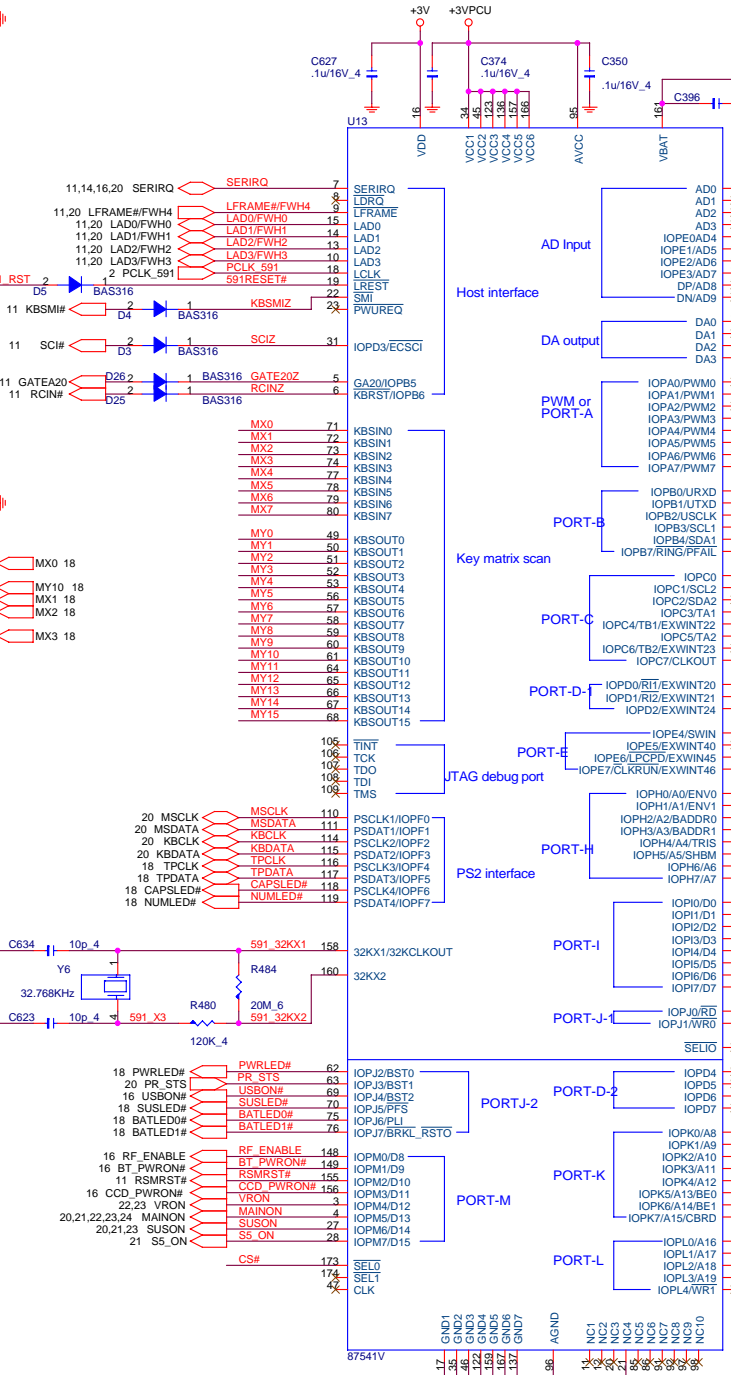
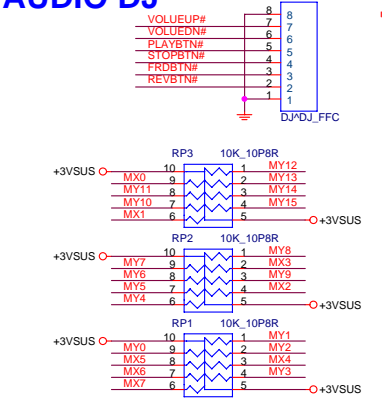
LED



K/B CONTROLLER

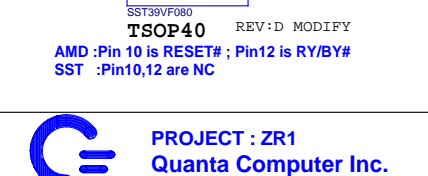
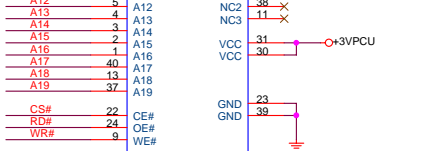
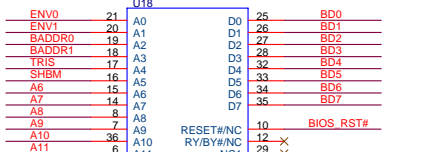
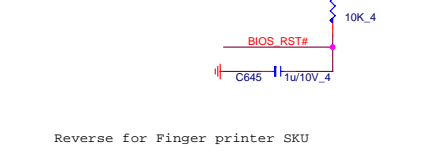
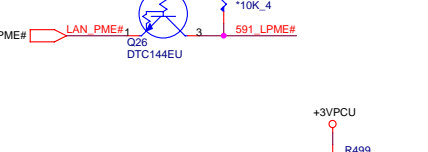
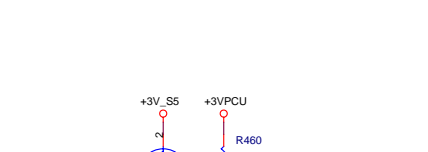
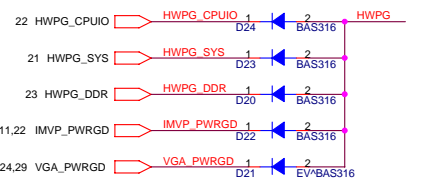


AUDIO DJ



SHBM=1: Enable shared memory with host BIOS

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	HCFGBAH, HCFGBAL	HCFGGBAH, HCFGGBAL
1 1	Reserved	



PROJECT : ZR1
Quanta Computer Inc.

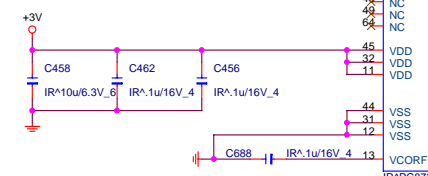
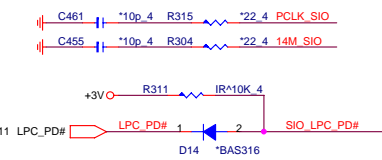
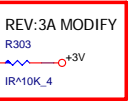
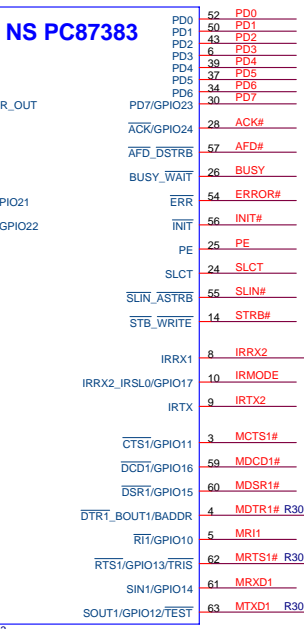
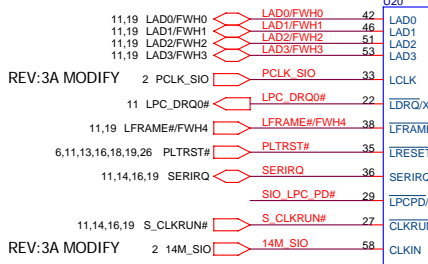
TSOP40
AMD : Pin 10 is RESET# ; Pin12 is RY/BY#
SST : Pin10,12 are NC

Size	Document Number	Rev
	EC PC87541V	1A
Date:	Thursday, June 29, 2006	Sheet 19 of 29

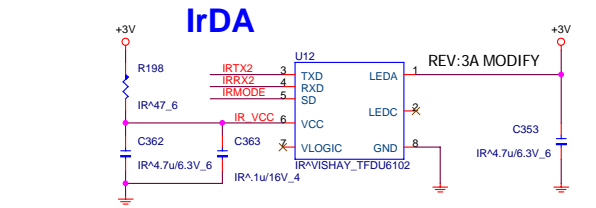
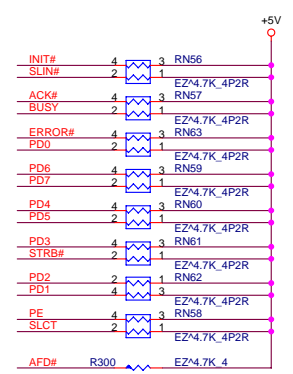
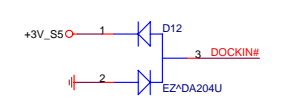
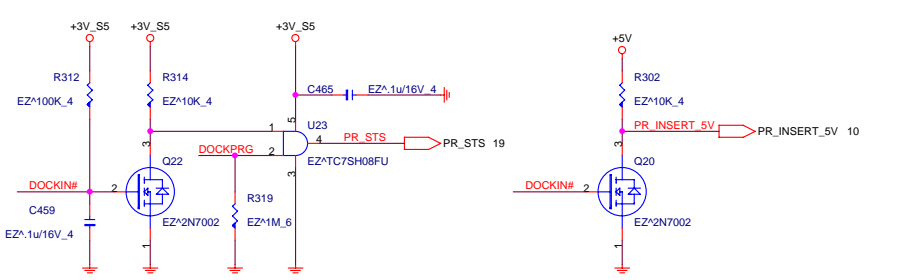
NS SIO 87383

REV:2A MODIFY

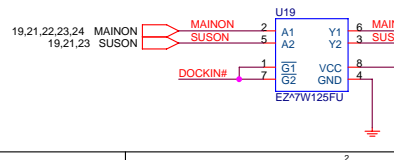
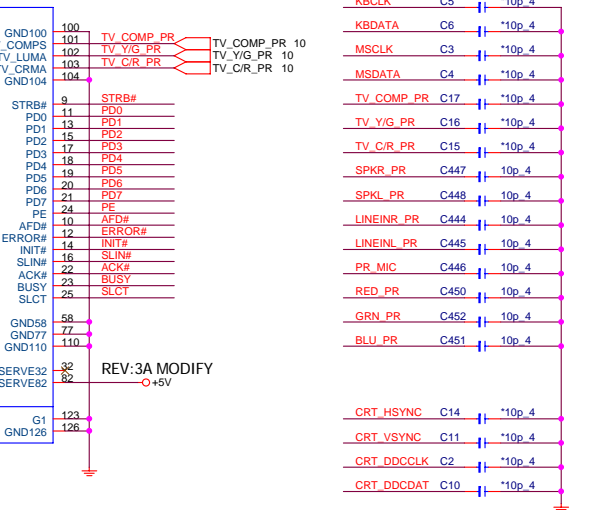
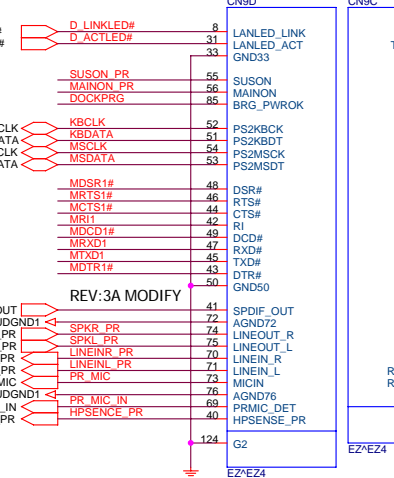
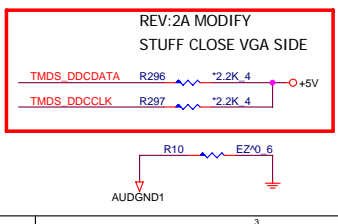
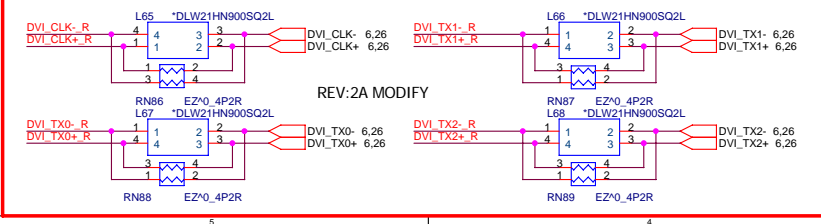
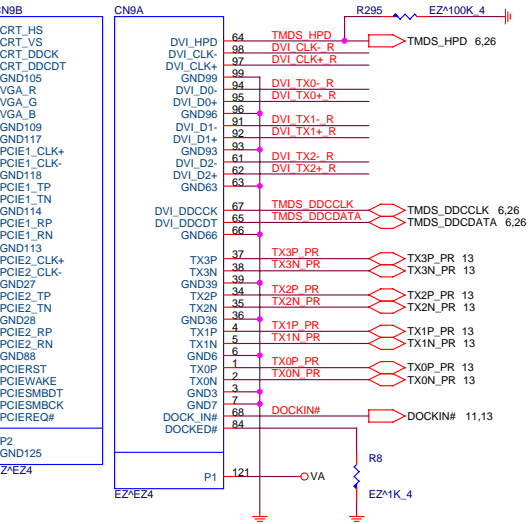
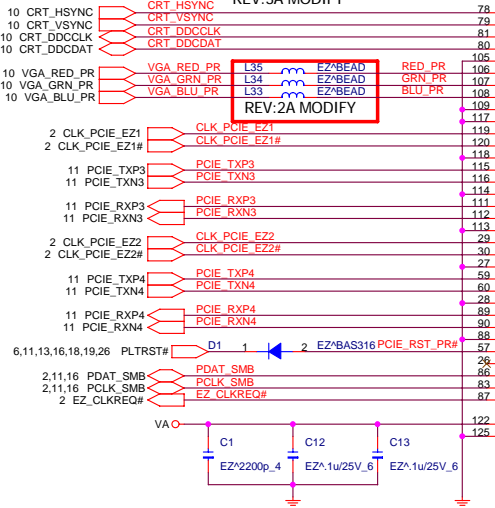
NS PC87383




OPEN : 164Eh-164Fh
 LOW : 2Eh-2Fh
 OPEN : normal pin operation
 LOW : float device pin
 OPEN : normal Device operation
 LOW : XOR pin tree



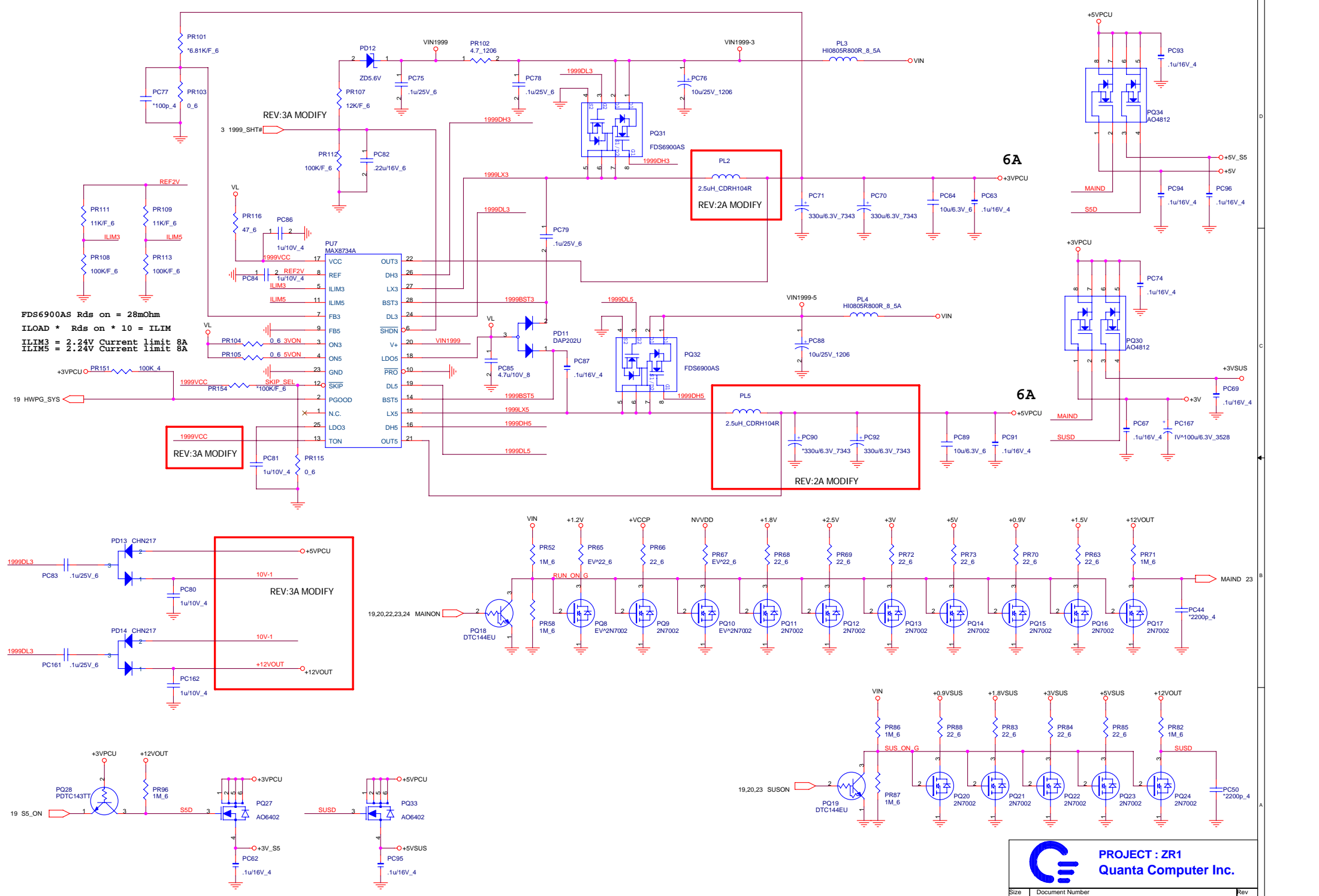
EZ4

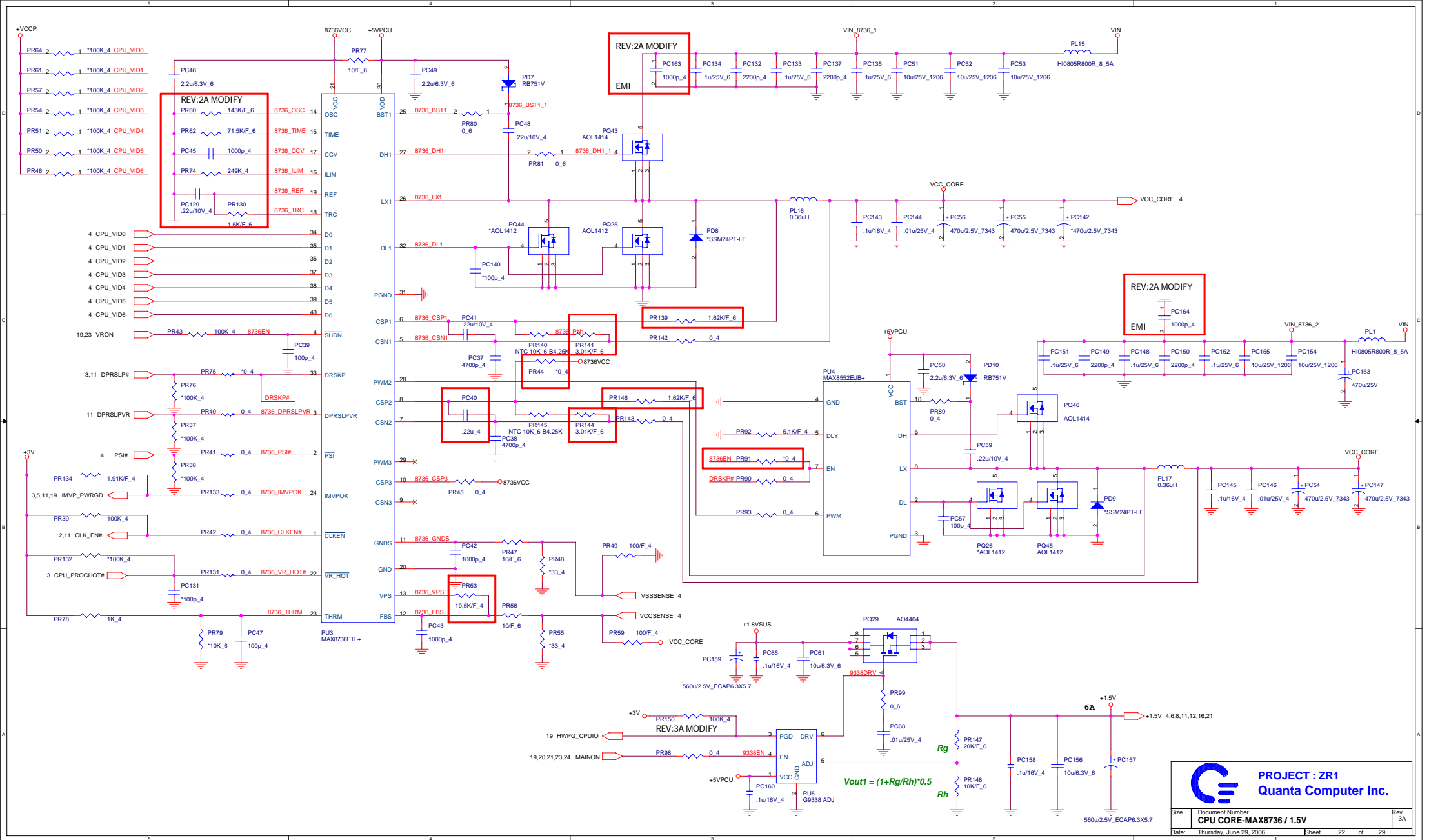





PROJECT : ZR1
Quanta Computer Inc.

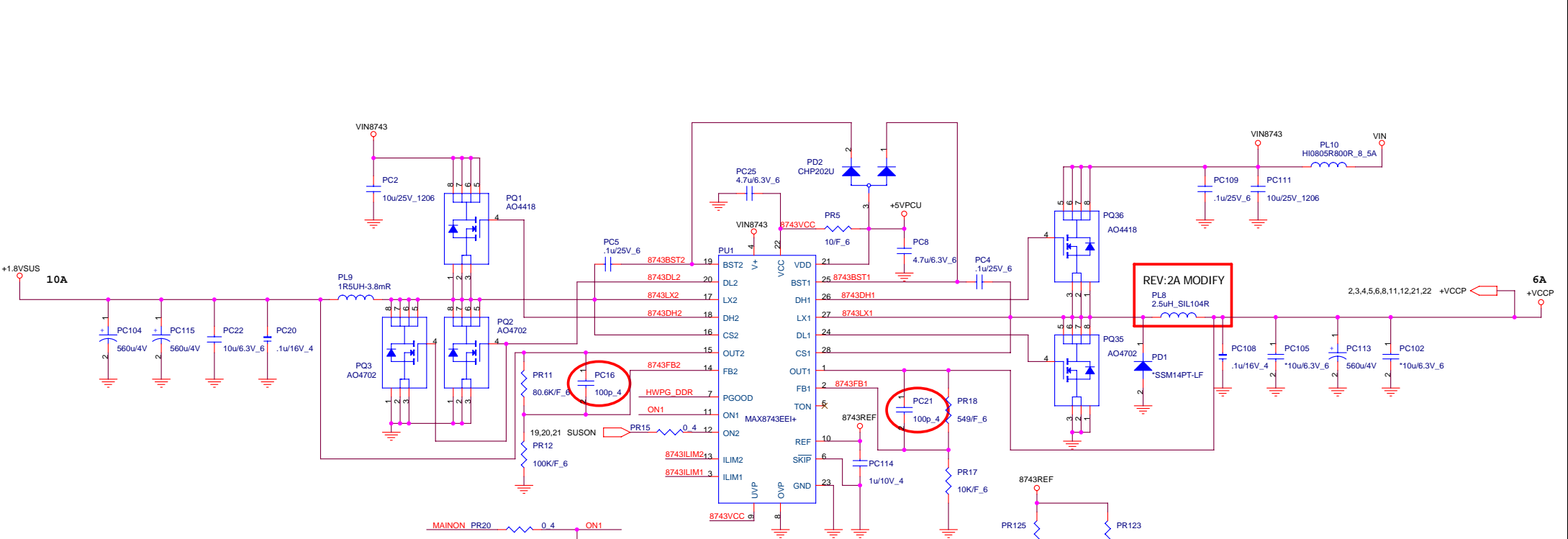
Size	Document Number	Rev
	SIO & EZ PORT4	3A
Date:	Thursday, June 29, 2006	Sheet 20 of 29





 PROJECT : ZR1 Quanta Computer Inc.		
Size	Document Number	Rev
	CPU CORE-MAX8736 / 1.5V	3A
Date:	Thursday, June 29, 2006	Sheet 22 of 29

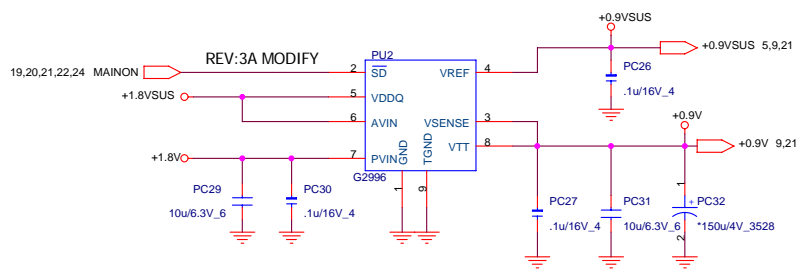
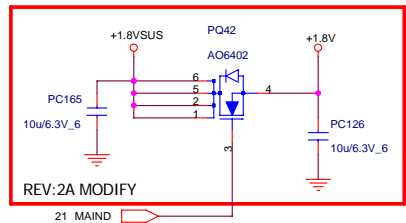
$$V_{out1} = (1 + R_g/R_h) * 0.5$$



REV:2A MODIFY
 PL8
 2.5uH_SIL104R

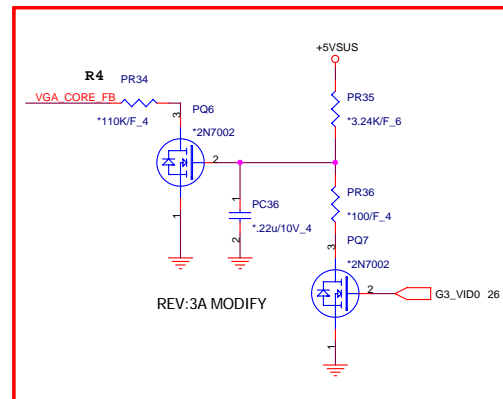
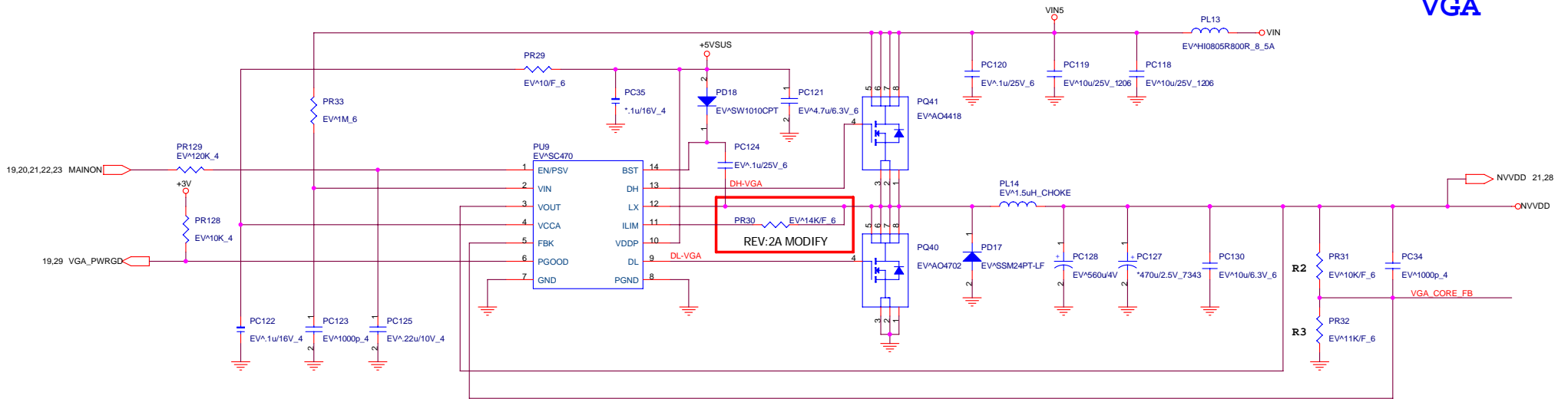
REV:2A MODIFY
 +3VSUS
 PR21
 *10K_4

AO4702 Rds on = 16mOhm
 ILOAD * Rds on * 10 = ILIM
 ILIM2 = 1.235V Current limit 15A
 ILIM1 = 0.91V Current limit 7A



PROJECT : ZR1
Quanta Computer Inc.

VGA



HI --> $V_{OUT} = (1 + R2/R3) * 0.5$

LO --> $V_{OUT} = (1 + R2 / (R3 // R4)) * 0.5$

M52P(G)

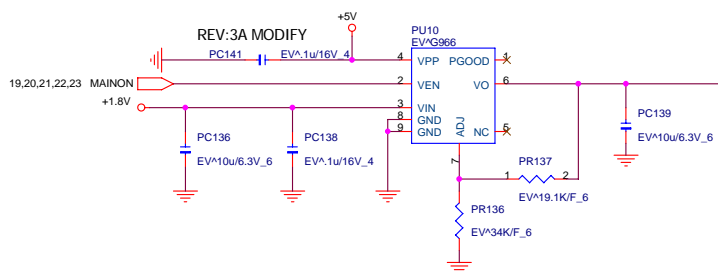
- PR1 : 10K
- PR4 : 11K
- PR2 : 110K

M54P

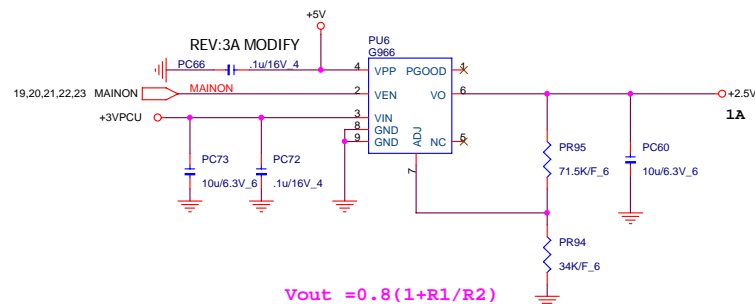
- PR1 : 12K
- PR4 : 12K
- PR2 : 60.4K

Power Play Mode

VGA_PWR_SW	VGA_CORE
HI	0.95V --M52P(G) 1.0V --M54P
Default LO	1.0V --M52P(G) 1.1V --M54P



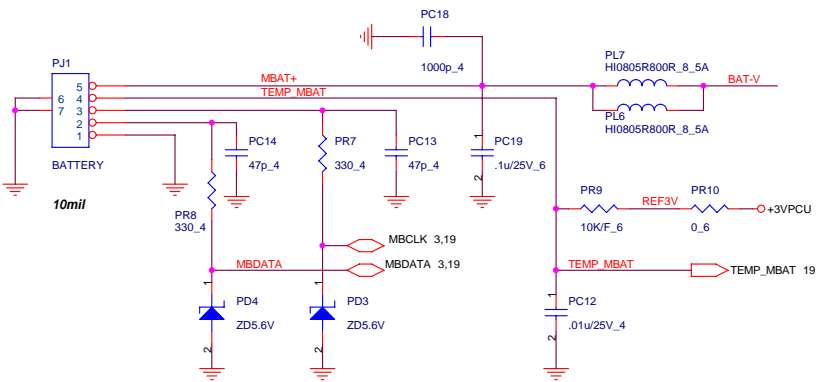
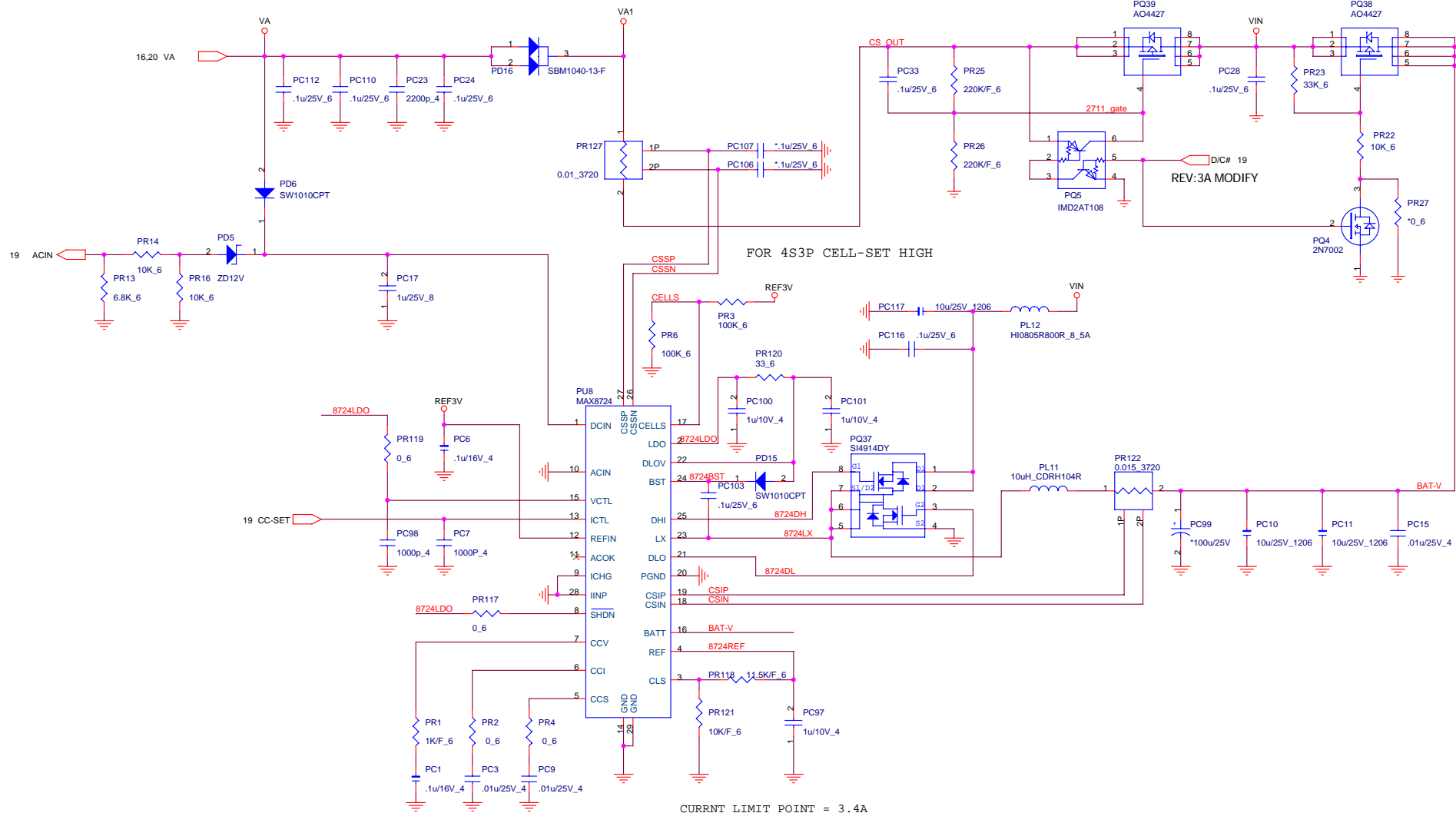
$V_{out} = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 1.2V$




$V_{out} = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 2.5V$



PROJECT : ZR1
Quanta Computer Inc.



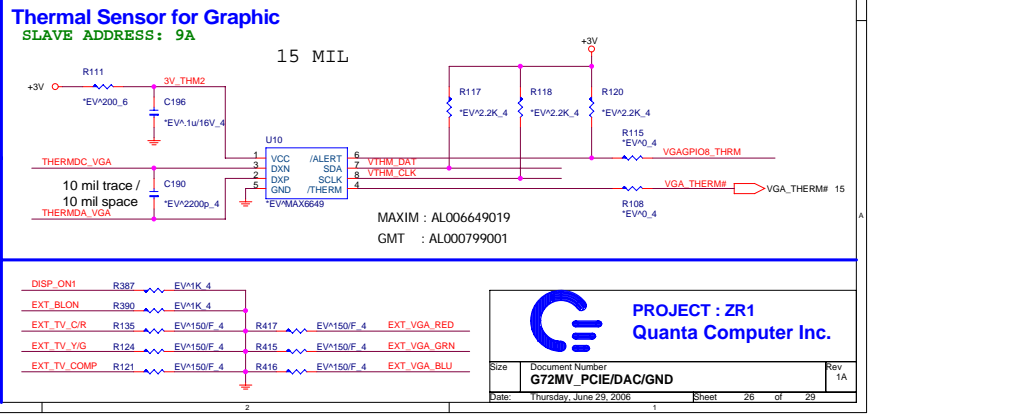
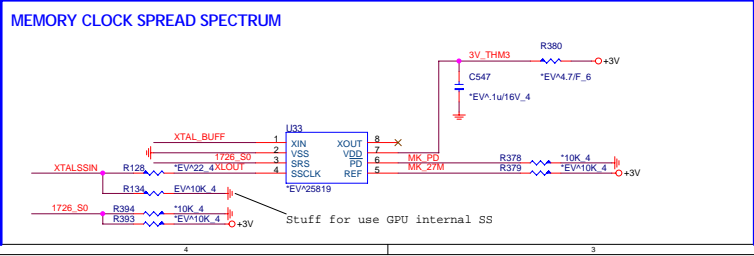
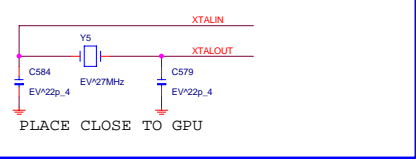
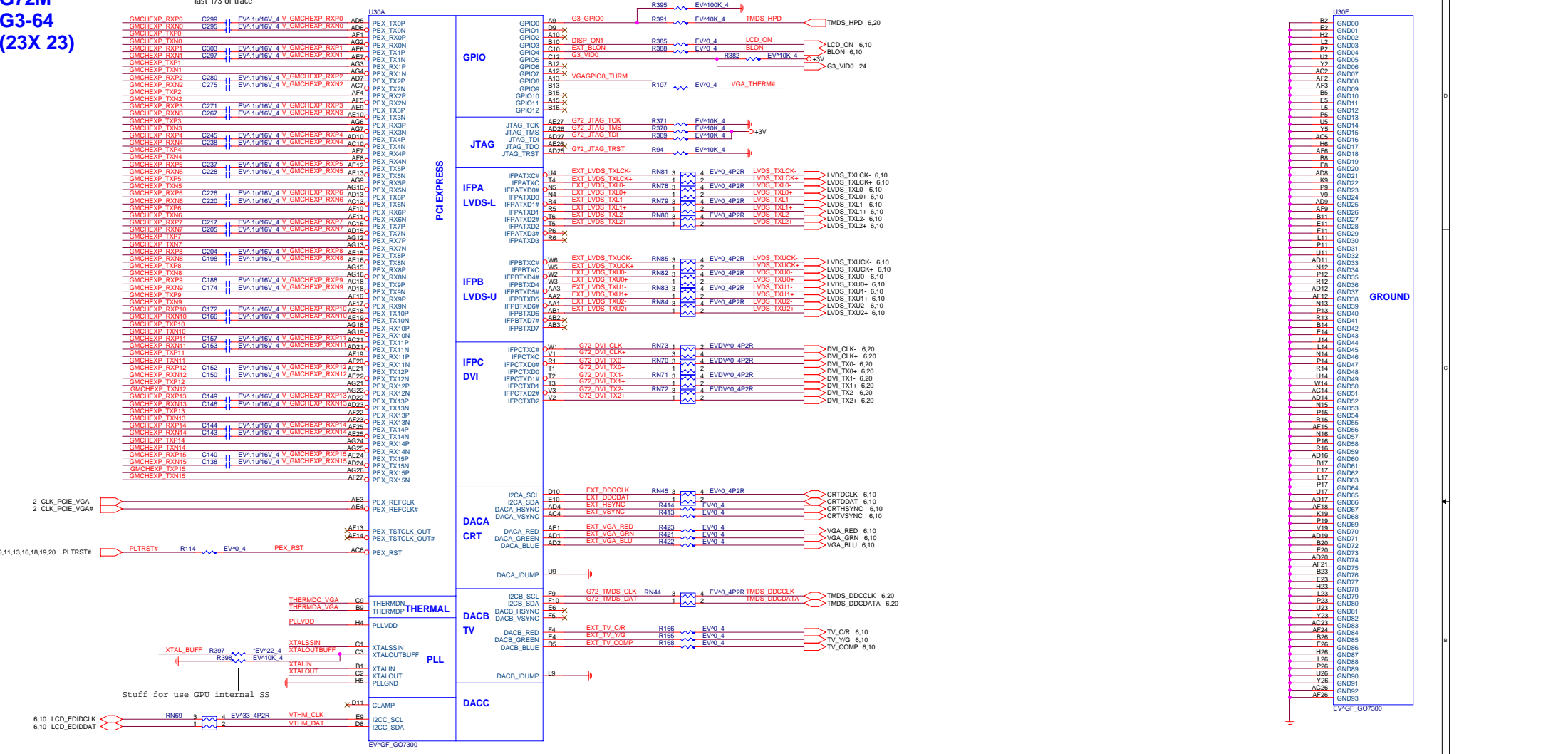


PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	BATTERY CHARGER	3A
Date:	Thursday, June 29, 2006	Sheet 25 of 29

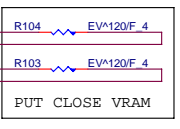
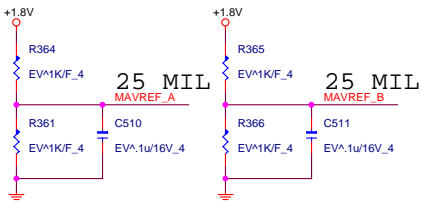
**NVIDIA
G72M
G3-64
(23X 23)**

0.1u Capacitors place at last 1/3 of trace

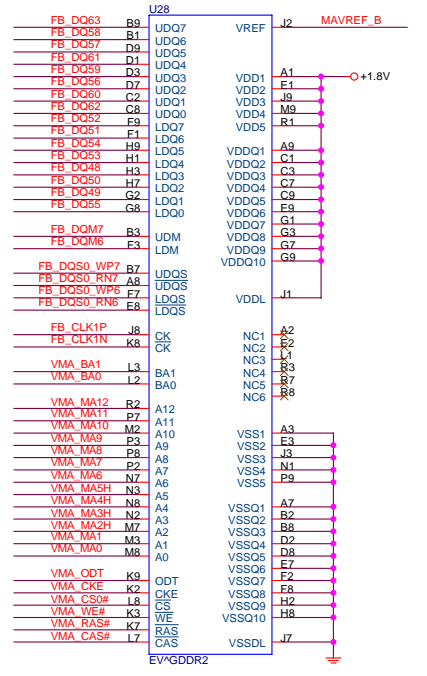
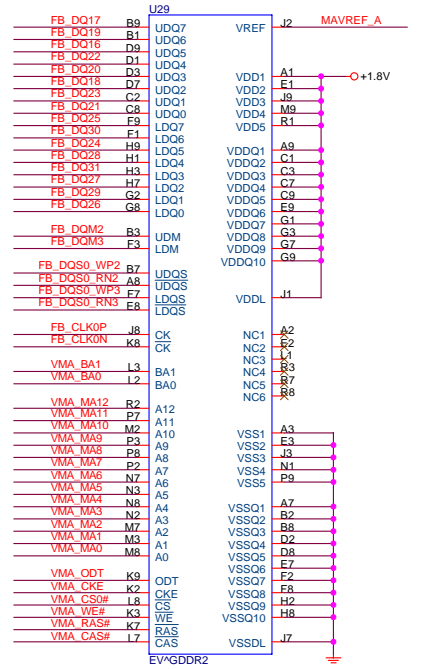
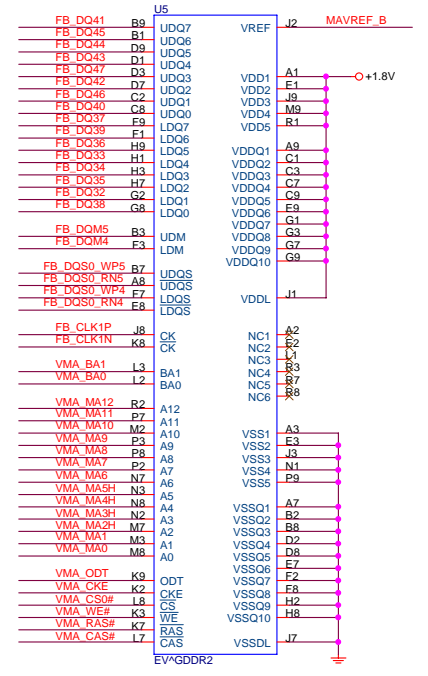
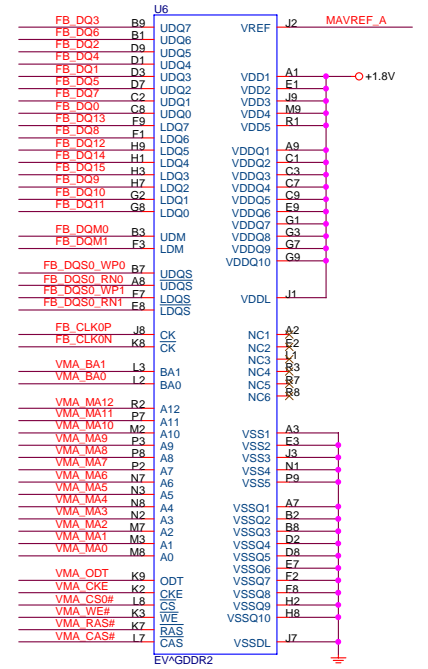
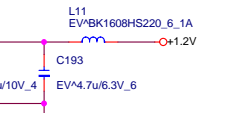


FB DO0	A26	FB DO0	FB_CMD0	G27	VMA_MA3
FB DO1	C24	FB DO1	FB_CMD1	D25	VMA_MA0
FB DO2	B24	FB DO2	FB_CMD2	F26	VMA_MA2
FB DO3	A24	FB DO3	FB_CMD3	F25	VMA_MA1
FB DO4	C22	FB DO4	G25	VMA_MA3H	
FB DO5	A25	FB DO5	FB_CMD4	J25	VMA_MA4H
FB DO6	B25	FB DO6	FB_CMD5	J27	VMA_MASH
FB DO7	D23	FB DO7	FB_CMD6	M26	VMA_CS0#
FB DO8	G22	FB DO8	FB_CMD7	C27	VMA_WE#
FB DO9	E22	FB DO9	FB_CMD8	D24	VMA_BA0
FB DO10	E22	FB DO10	FB_CMD9	D24	VMA_BA0
FB DO11	F23	FB DO11	FB_CMD10	N27	VMA_CKE
FB DO12	C22	FB DO12	FB_CMD11	G24	VMA_ODT
FB DO13	J24	FB DO13	FB_CMD12	J26	VMA_MA2H
FB DO14	G23	FB DO14	FB_CMD13	M27	VMA_MA12
FB DO15	H24	FB DO15	FB_CMD14	C26	VMA_RAS#
FB DO16	D16	FB DO16	FB_CMD15	M25	VMA_MA11
FB DO17	E16	FB DO17	FB_CMD16	D26	VMA_MA10
FB DO18	D17	FB DO18	FB_CMD17	D27	VMA_BA1
FB DO19	F18	FB DO19	FB_CMD18	K26	VMA_MA8
FB DO20	E19	FB DO20	FB_CMD19	K25	VMA_MA9
FB DO21	E18	FB DO21	FB_CMD20	K24	VMA_MA6
FB DO22	D19	FB DO22	FB_CMD21	F27	VMA_MA5
FB DO23	A18	FB DO23	FB_CMD22	K27	VMA_MA7
FB DO24	A18	FB DO24	FB_CMD23	G26	VMA_MA4
FB DO25	B18	FB DO25	FB_CMD24	B27	VMA_CAS#
FB DO26	A19	FB DO26	FB_CMD25	B27	VMA_CAS#
FB DO27	B19	FB DO27	FB_CMD26	N24	
FB DO28	D18	FB DO28			
FB DO29	C19	FB DO29			
FB DO30	C18	FB DO30	FB_CLK0	L24	FB_CLKOP
FB DO31	C18	FB DO31	FB_CLK#	K23	FB_CLKRN
FB DO32	N26	FB DO32	FB_CLK1		
FB DO33	N25	FB DO33	FB_CLK#	M22	FB_CLK1P
FB DO34	R26	FB DO34	FB_CLK1#	N22	FB_CLK1N
FB DO35	R25	FB DO35			
FB DO36	R26	FB DO36			
FB DO37	T25	FB DO37			
FB DO38	T26	FB DO38			
FB DO39	T26	FB DO39			
FB DO40	AB23	FB DO40			
FB DO41	Y24	FB DO41			
FB DO42	AB24	FB DO42			
FB DO43	AB22	FB DO43			
FB DO44	AC24	FB DO44			
FB DO45	AC22	FB DO45			
FB DO46	AA23	FB DO46			
FB DO47	AA22	FB DO47			
FB DO48	T24	FB DO48			
FB DO49	T24	FB DO49			
FB DO50	R24	FB DO50			
FB DO51	R23	FB DO51			
FB DO52	T22	FB DO52			
FB DO53	R22	FB DO53			
FB DO54	N23	FB DO54			
FB DO55	P24	FB DO55			
FB DO56	AA24	FB DO56			
FB DO57	AA27	FB DO57			
FB DO58	AA26	FB DO58			
FB DO59	AB25	FB DO59			
FB DO60	AB26	FB DO60			
FB DO61	AB27	FB DO61			
FB DO62	AA25	FB DO62			
FB DO63	W25	FB DO63			
FB DOM0	D21	FB DOM0	FB_PLLVDD	D14	FBA_PLLAVDD
FB DOM1	F22	FB DOM1	FB_PLLAVDD	D13	
FB DOM2	A20	FB DOM2			
FB DOM3	A21	FB DOM3			
FB DOM4	V27	FB DOM4			
FB DOM5	V22	FB DOM5			
FB DOM6	V22	FB DOM6			
FB DOM7	V24	FB DOM7			
FB DOS0_WP0	B22	FB DOS0_WP0	FB_DOS_RN0	A22	FB DOS0_RN0
FB DOS0_WP1	D22	FB DOS0_WP1	FB_DOS_RN1	E22	FB DOS0_RN1
FB DOS0_WP2	E21	FB DOS0_WP2	FB_DOS_RN2	F21	FB DOS0_RN2
FB DOS0_WP3	C21	FB DOS0_WP3	FB_DOS_RN3	D21	FB DOS0_RN3
FB DOS0_WP4	V25	FB DOS0_WP4	FB_DOS_RN4	V26	FB DOS0_RN4
FB DOS0_WP5	W24	FB DOS0_WP5	FB_DOS_RN5	W23	FB DOS0_RN5
FB DOS0_WP6	U24	FB DOS0_WP6	FB_DOS_RN6	V23	FB DOS0_RN6
FB DOS0_WP7	W26	FB DOS0_WP7	FB_DOS_RN7	W27	FB DOS0_RN7

NC_0	D12	
NC_1	E12	
NC_2	F12	
NC_3	C13	



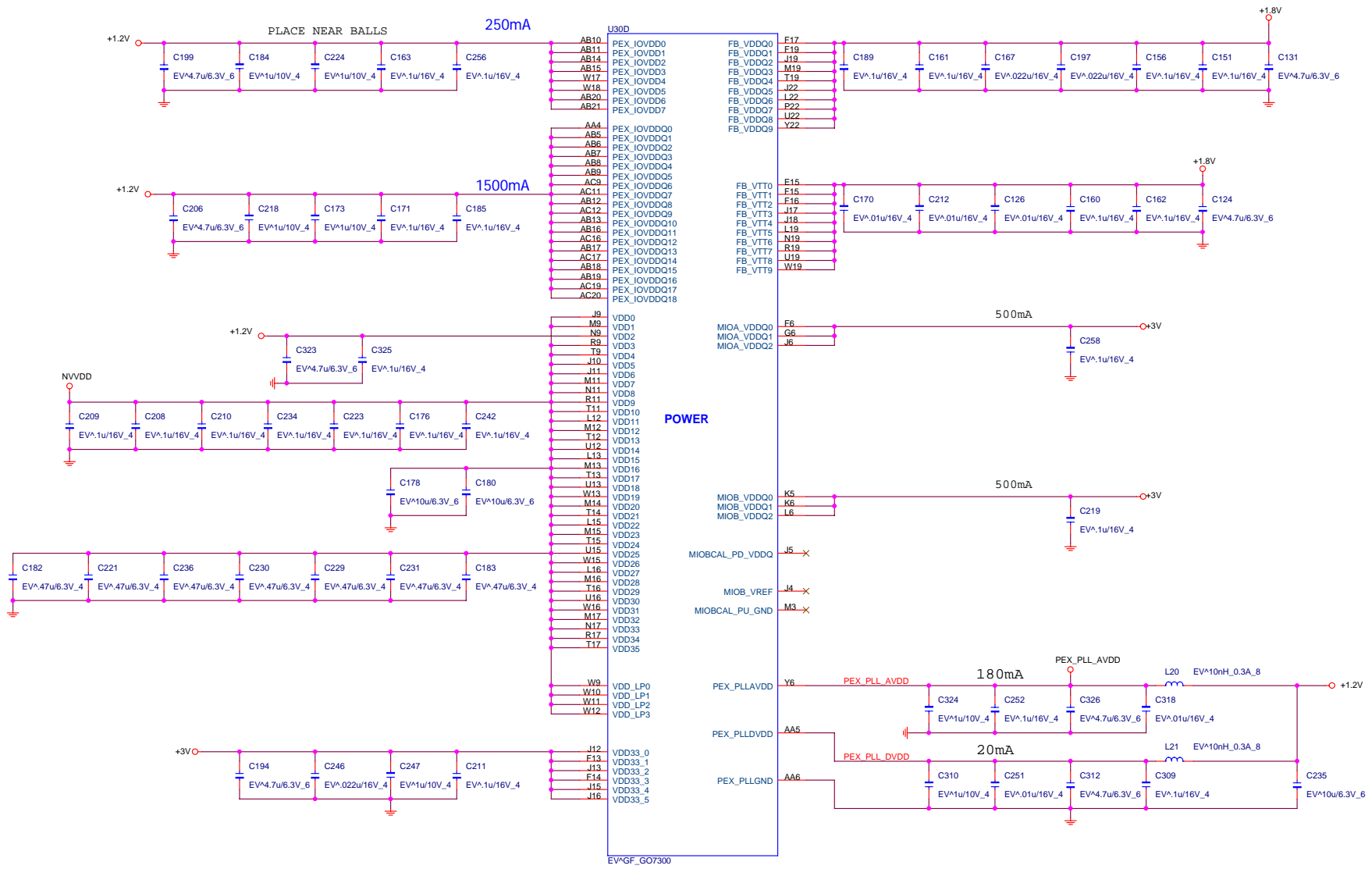
PLACE CLOSE TO BALLS



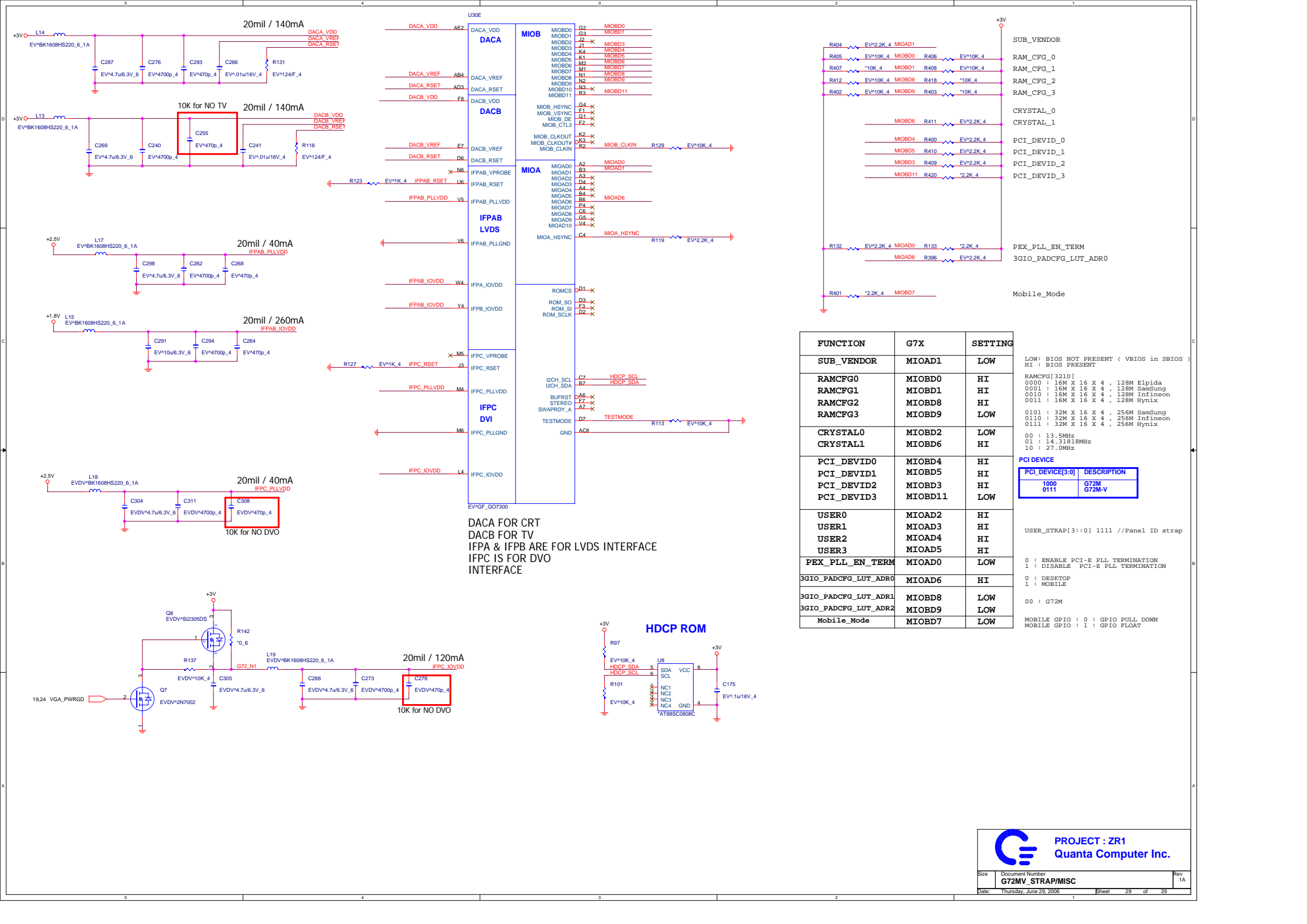
- SAMSUNG 16M*16 --> AKD5JGBT509
- SAMSUNG 32M*16 --> AKD5FGBT501
- INFI 16M*16 --> AKD5JG-T^00
- INFI 32M*16 --> AKD5FG-T^00
- HYNIX 16M*16 --> AKD5JG-TW12
- HYNIX 32M*16 --> AKD5FG-TW14

PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	G72MV_MEMORY A/B/C/D	1A
Date:	Thursday, June 29, 2006	Sheet 27 of 29



POWER



DACA FOR CRT
 DACB FOR TV
 IFPA & IFPB ARE FOR LVDS INTERFACE
 IFPC IS FOR DVO INTERFACE

FUNCTION	G7X	SETTING
SUB_VENDOR	MIOAD1	LOW
RAMCFG0	MIOBD0	HI
RAMCFG1	MIOBD1	HI
RAMCFG2	MIOBD8	HI
RAMCFG3	MIOBD9	LOW
CRYSTAL0	MIOBD2	LOW
CRYSTAL1	MIOBD6	HI
PCI_DEVID0	MIOBD4	HI
PCI_DEVID1	MIOBD5	HI
PCI_DEVID2	MIOBD3	HI
PCI_DEVID3	MIOBD11	LOW
USER0	MIOAD2	HI
USER1	MIOAD3	HI
USER2	MIOAD4	HI
USER3	MIOAD5	HI
PEX_PLL_EN_TERM	MIOAD0	LOW
3GIO_PADCFG_LUT_ADR0	MIOAD6	HI
3GIO_PADCFG_LUT_ADR1	MIOBD8	LOW
3GIO_PADCFG_LUT_ADR2	MIOBD9	LOW
Mobile_Mode	MIOBD7	LOW

LOW: BIOS NOT PRESENT (VBIOS in SBIOS)
 HI : BIOS PRESENT

RAMCFG[3210]
 0000 : 16M X 16 X 4 , 128M Elpida
 0001 : 16M X 16 X 4 , 128M Samsung
 0010 : 16M X 16 X 4 , 128M Infineon
 0011 : 16M X 16 X 4 , 128M Hynix

0101 : 32M X 16 X 4 , 256M Samsung
 0110 : 32M X 16 X 4 , 256M Infineon
 0111 : 32M X 16 X 4 , 256M Hynix

PCI DEVICE

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M
0111	G72M-V

USER_STRAP[3:1] 1111 //Panel ID strap

0 : ENABLE PCI-E PLL TERMINATION
 1 : DISABLE PCI-E PLL TERMINATION

0 : DESKTOP
 1 : MOBILE

00 : G72M

MOBILE GPIO : 0 : GPIO PULL_DOWN
 MOBILE GPIO : 1 : GPIO FLOAT

