PCI-EXPRESS EDGE CONNECTOR

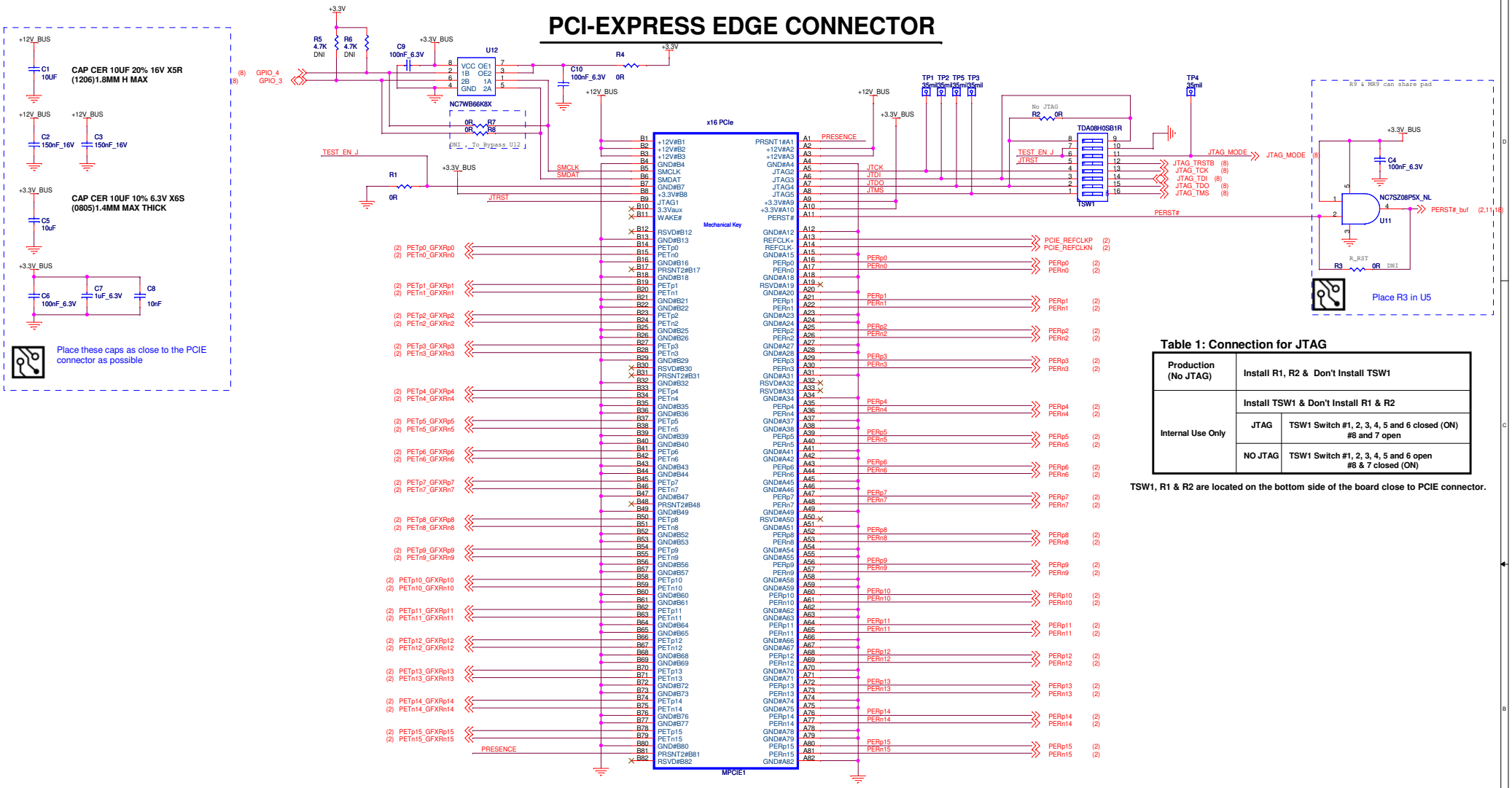

Table 1: Connection for JTAG

Production (No JTAG)	**Install R1, R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R1 & R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)**

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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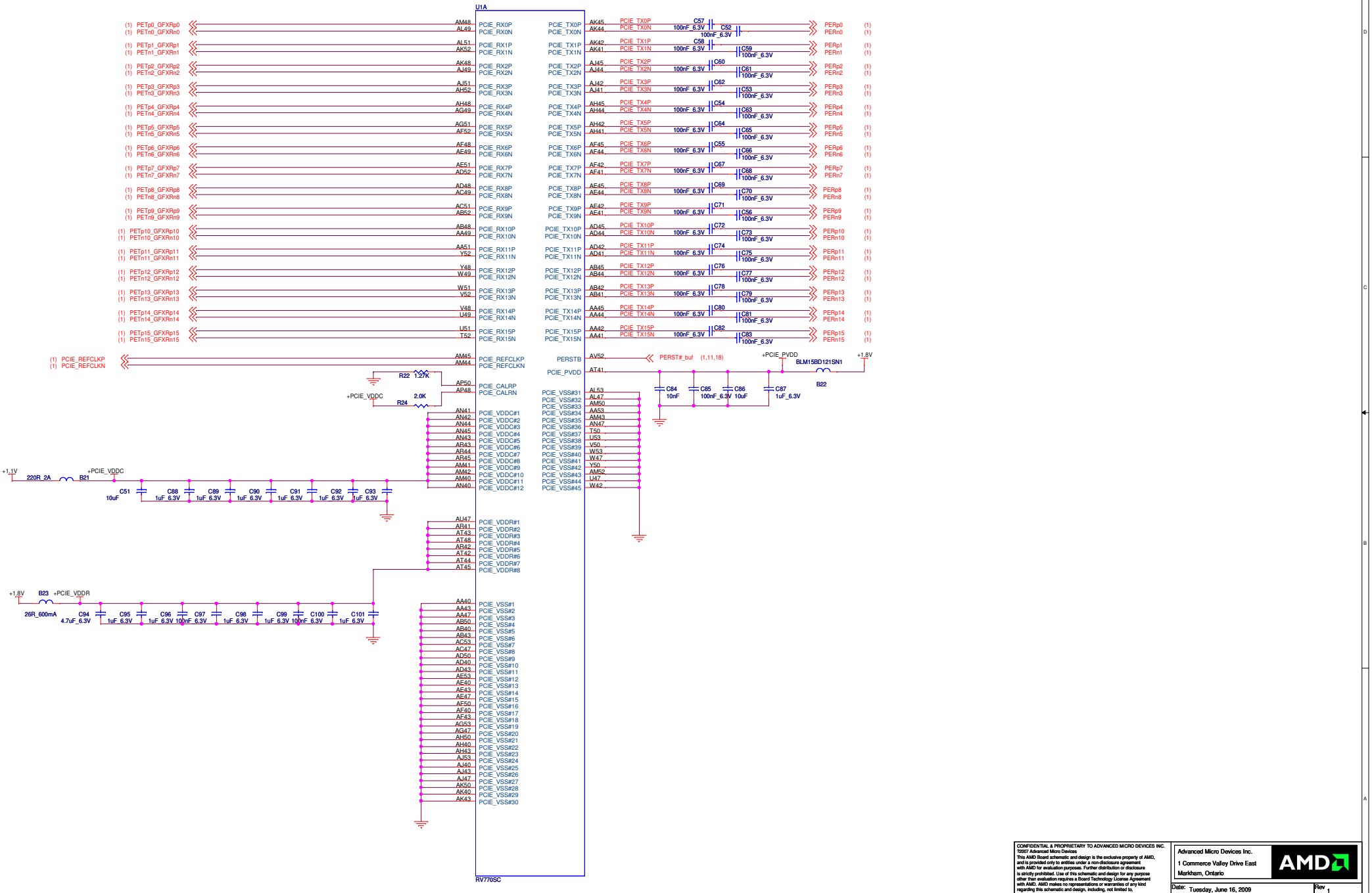
PN: 105-B790xx-00

NOTE: some of the PCIE testpoints will
be available trought via on traces.



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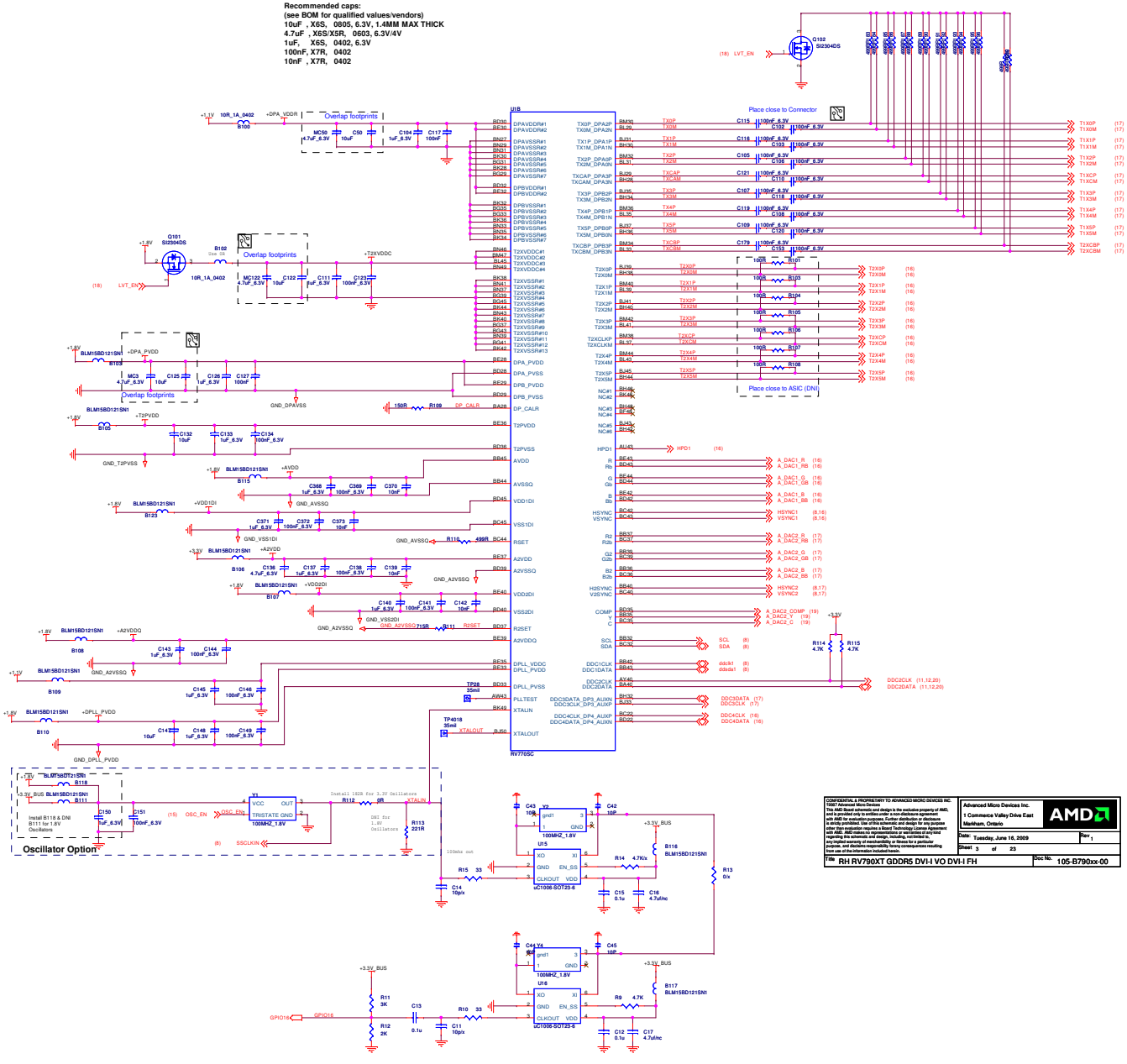
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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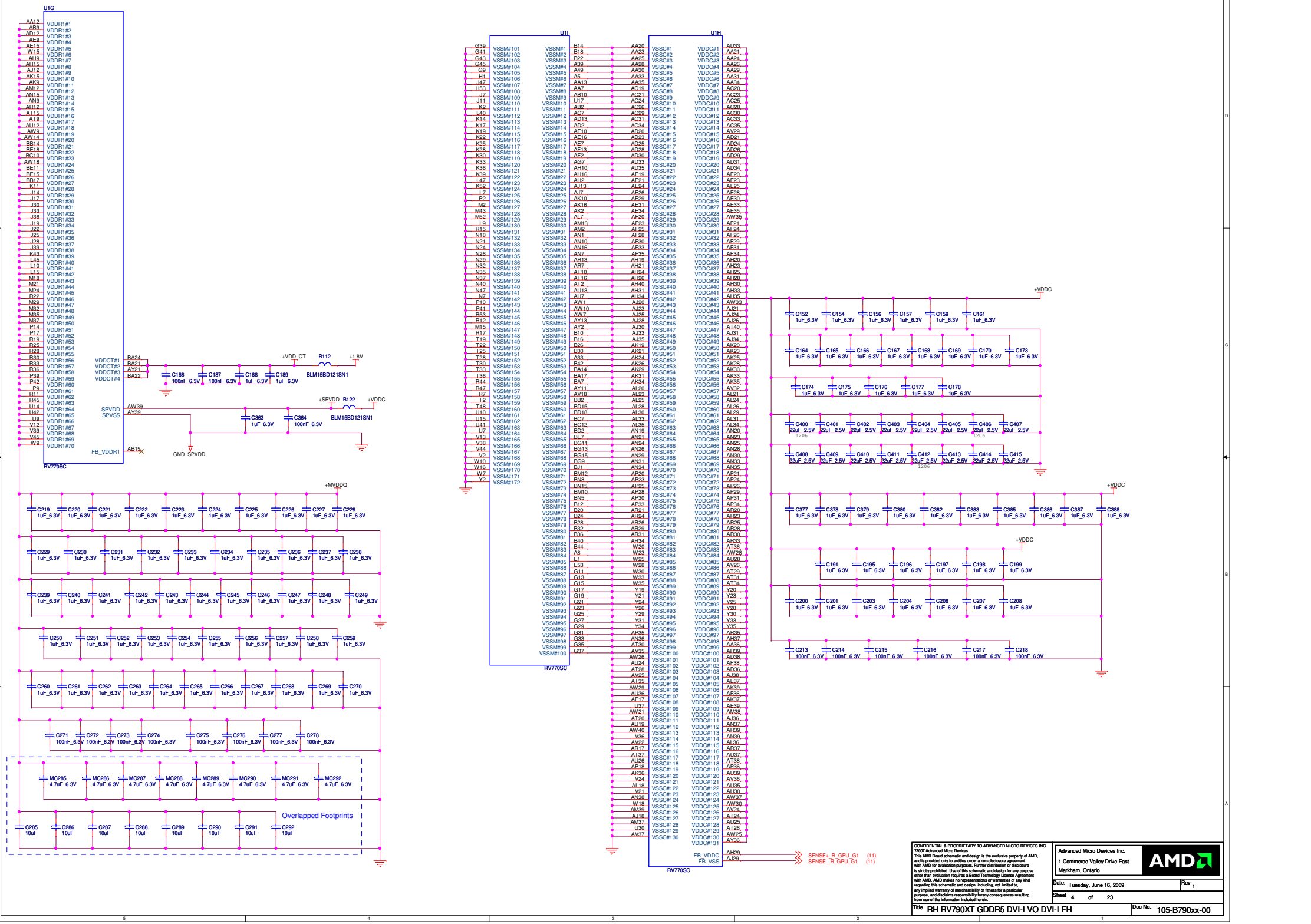

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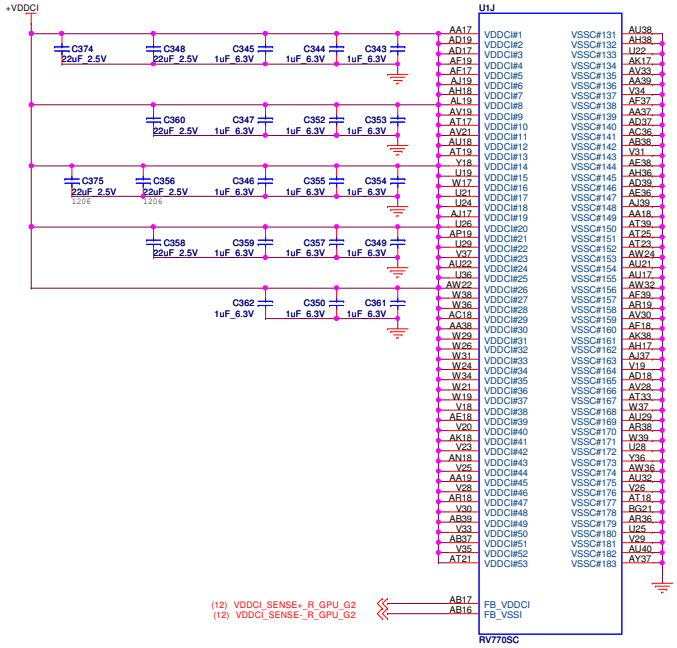

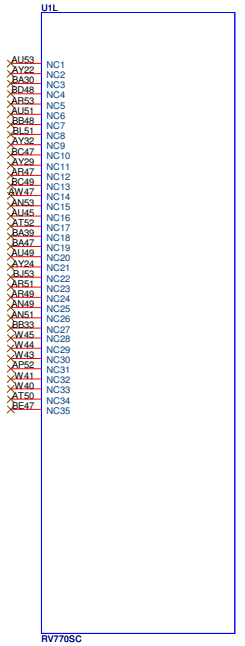

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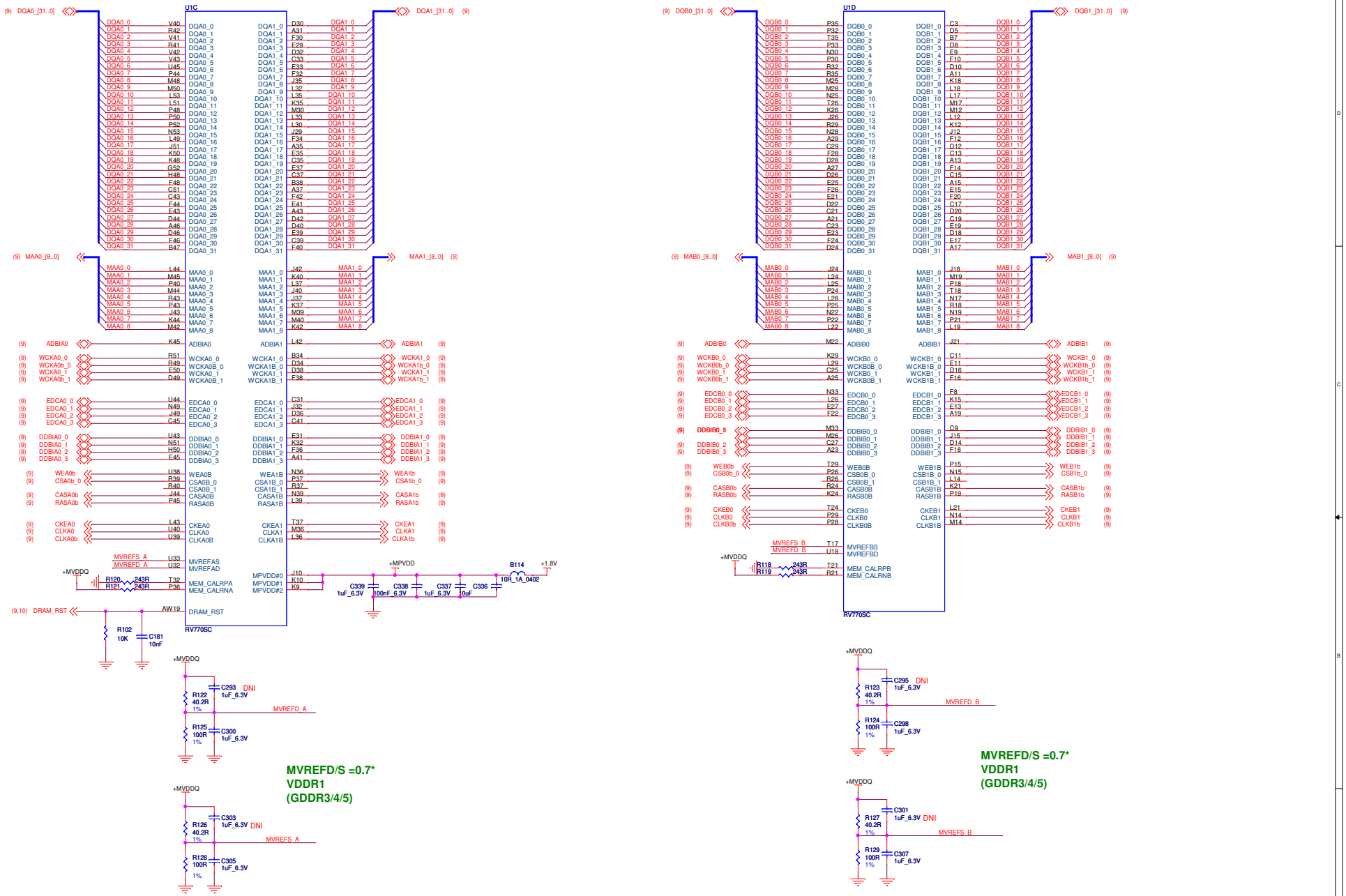

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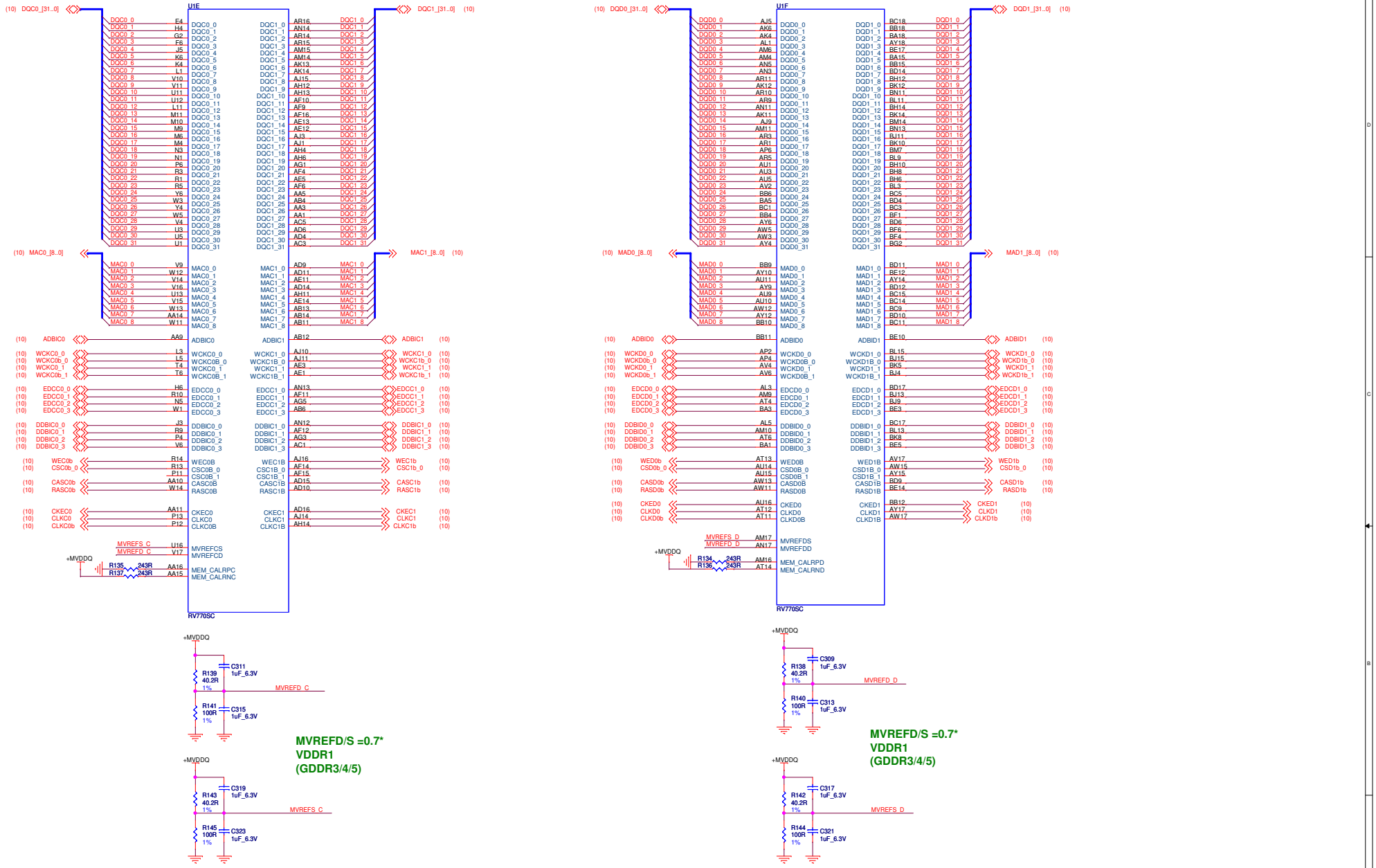

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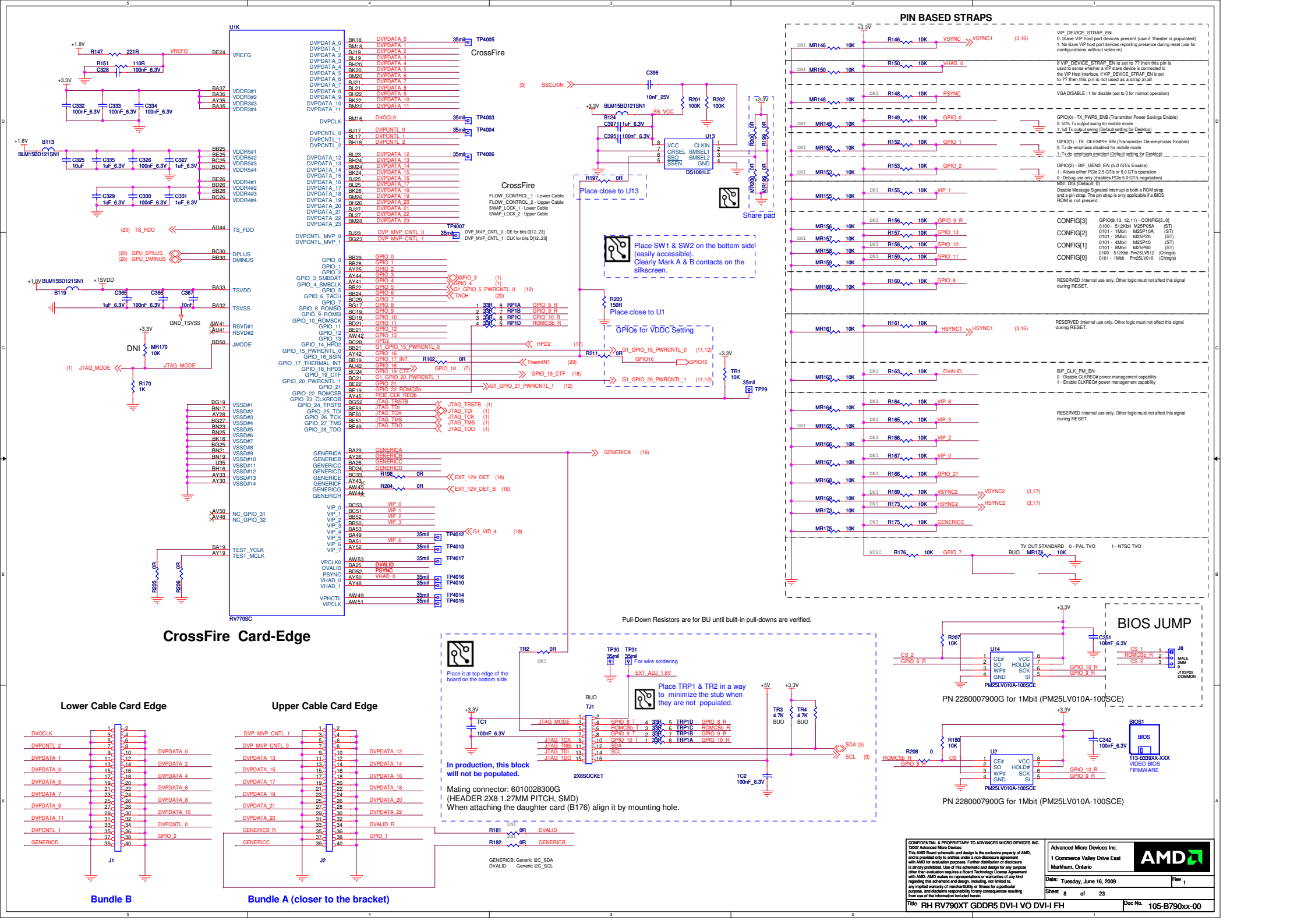
PIN BASED STRAPS
CrossFire Card-Edge
Lower Cable Card Edge
Upper Cable Card Edge
Bundle B
Bundle A (closer to the bracket)
BIOS JUMP
CrossFire
Share pad
Place close to U13
Place close to U1
Place SW1 & SW2 on the bottom side (easily accessible). Clearly Mark A & B contacts on the silkscreen.
GPIOs for VDDC Setting
Pull-Down Resistors are for BU until built-in pull-downs are verified.
Place it at top edge of the board on the bottom side.
Place TRP1 & TR2 in a way to minimize the stub when they are not populated.
In production, this block will not be populated.
Mating connector: 6010028300G
(HEADER 2X8 1.27MM PITCH, SMD)
When attaching the daughter card (B176) align it by mounting hole.
PN 2280007900G for 1Mbit (PM25LV010A-100SCE)
PN 2280007900G for 1Mbit (PM25LV010A-100SCE)
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Title RH RV790XT GDDR5 DVI-I VO DVI-I FH
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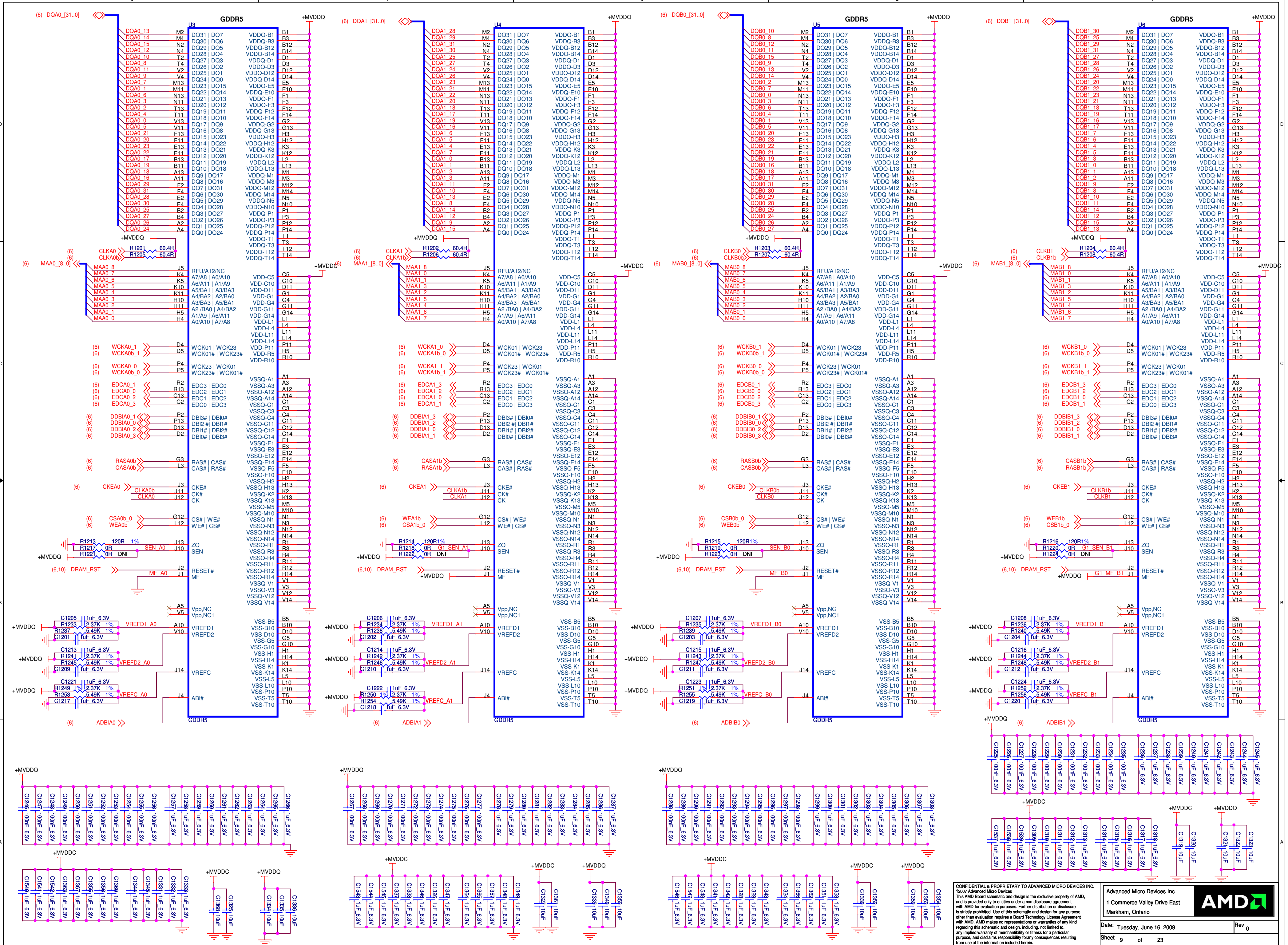

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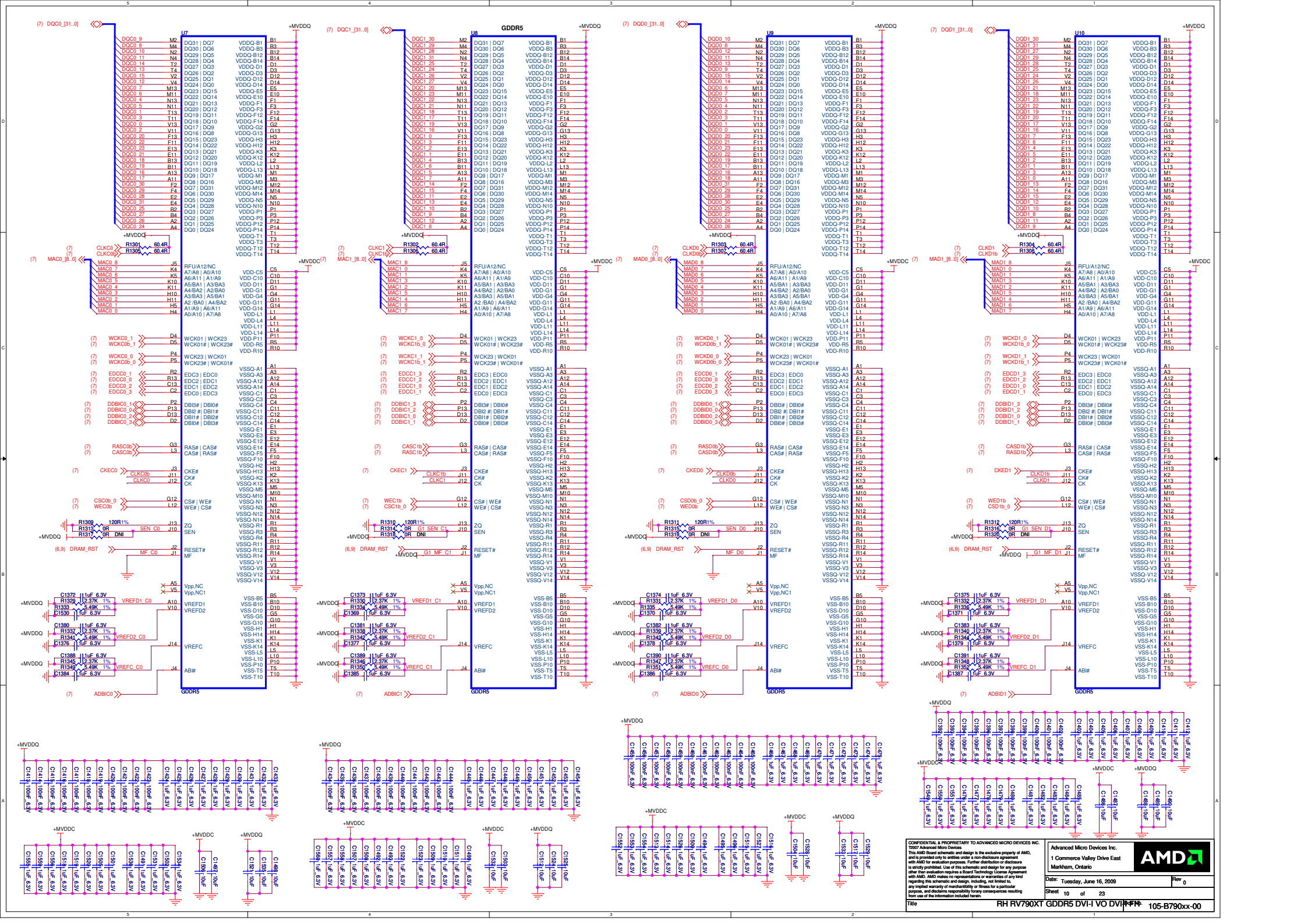
Title RH RV790XT GDDR5 DVI-I VO DVI-I FH | Doc No. 105-B790xx-00


GDDR5
U7
U8
U9
U10
+MVDDQ
+MVDDC
DQC0_[31..0]
DQC1_[31..0]
DQD0_[31..0]
DQD1_[31..0]
MAC0_[8..0]
MAC1_[8..0]
MAD0_[8..0]
MAD1_[8..0]
CLKC0
CLKC0b
CLKC1
CLKC1b
CLKD0
CLKD0b
CLKD1
CLKD1b
R1301 60.4R 1%
R1305 60.4R 1%
R1302 60.4R 1%
R1306 60.4R 1%
R1303 60.4R 1%
R1307 60.4R 1%
R1304 60.4R 1%
R1308 120R 1%
R1309 0R
R1317 0R DNI
R1310 120R 1%
R1314 0R G1_SEN_C1
R1318 0R DNI
R1311 120R 1%
R1315 0R
R1319 0R DNI
R1312 120R 1%
R1316 0R G1_SEN_D1
R1320 0R DNI
SEN_C0
SEN_D0
DRAM_RST
MF_C0
G1_MF_C1
MF_D0
G1_MF_D1
VREFD1_C0
VREFD2_C0
VREFC_C0
VREFD1_C1
VREFD2_C1
VREFC_C1
VREFD1_D0
VREFD2_D0
VREFC_D0
VREFD1_D1
VREFD2_D1
VREFC_D1
ADBIC0
ADBIC1
ADBID0
ADBID1
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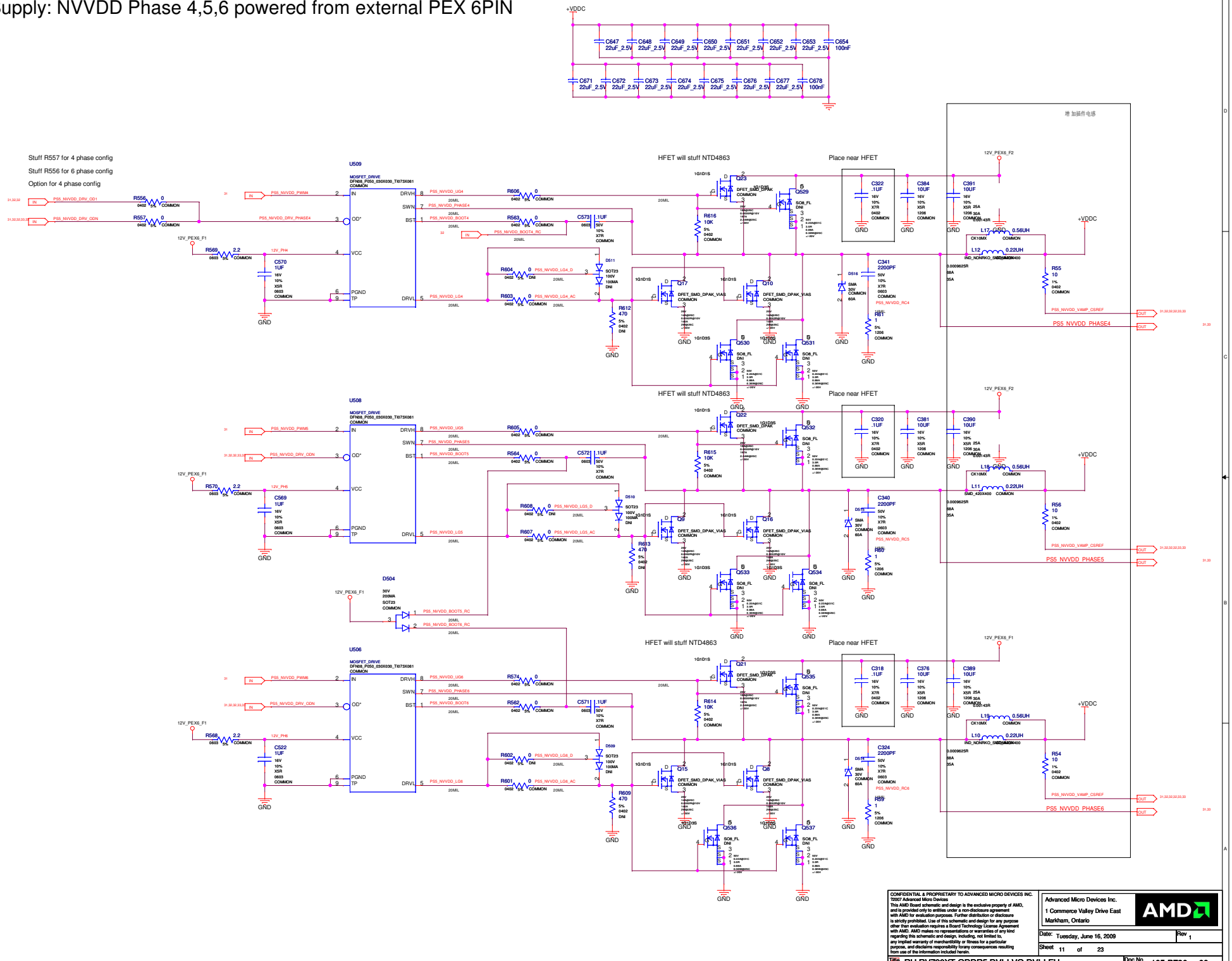
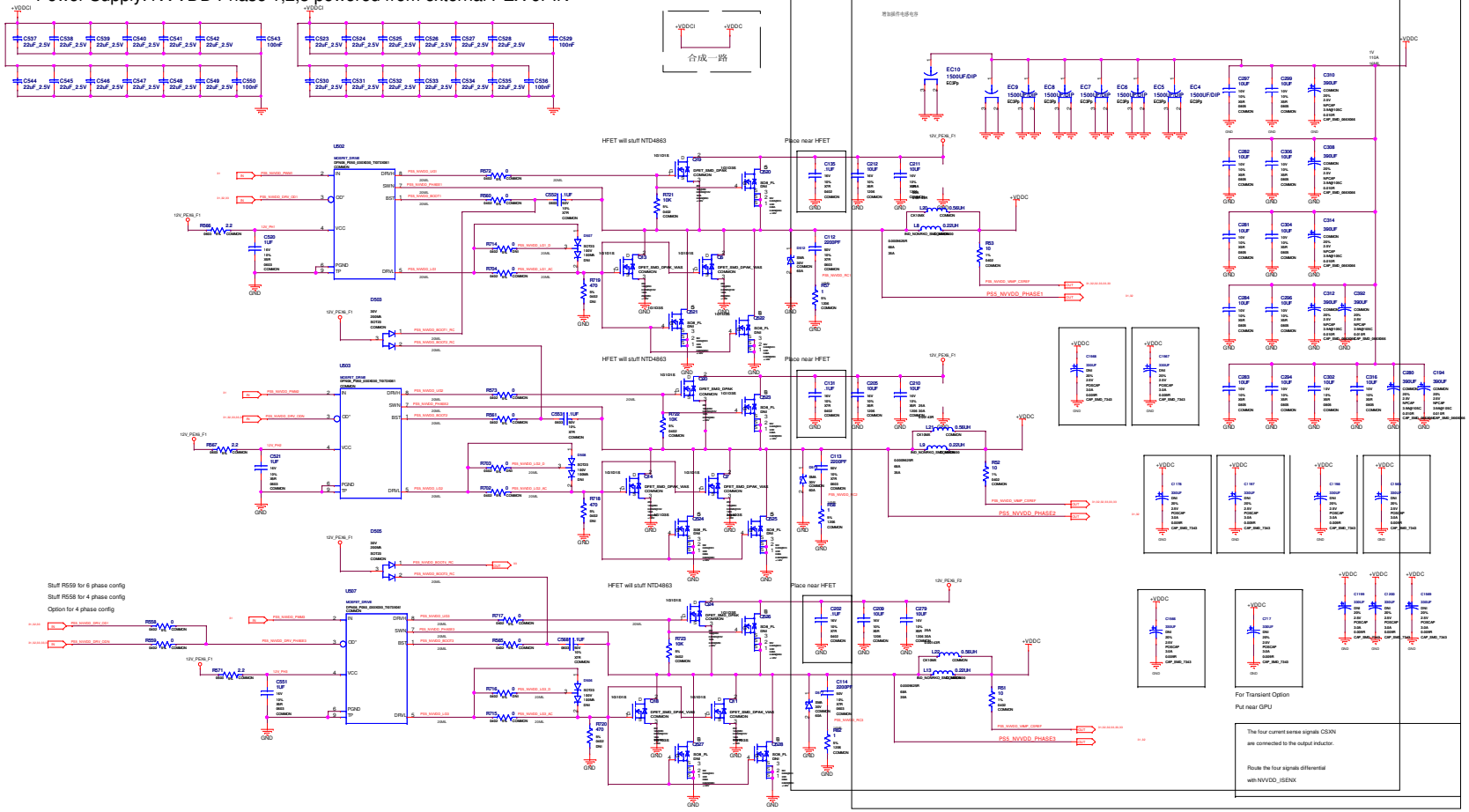
105-B790xx-00

Power Supply: NVVDD Phase 4,5,6 powered from external PEX 6PIN



Power Supply: NVVDD Phase 1,2,3 powered from external PEX 6PIN



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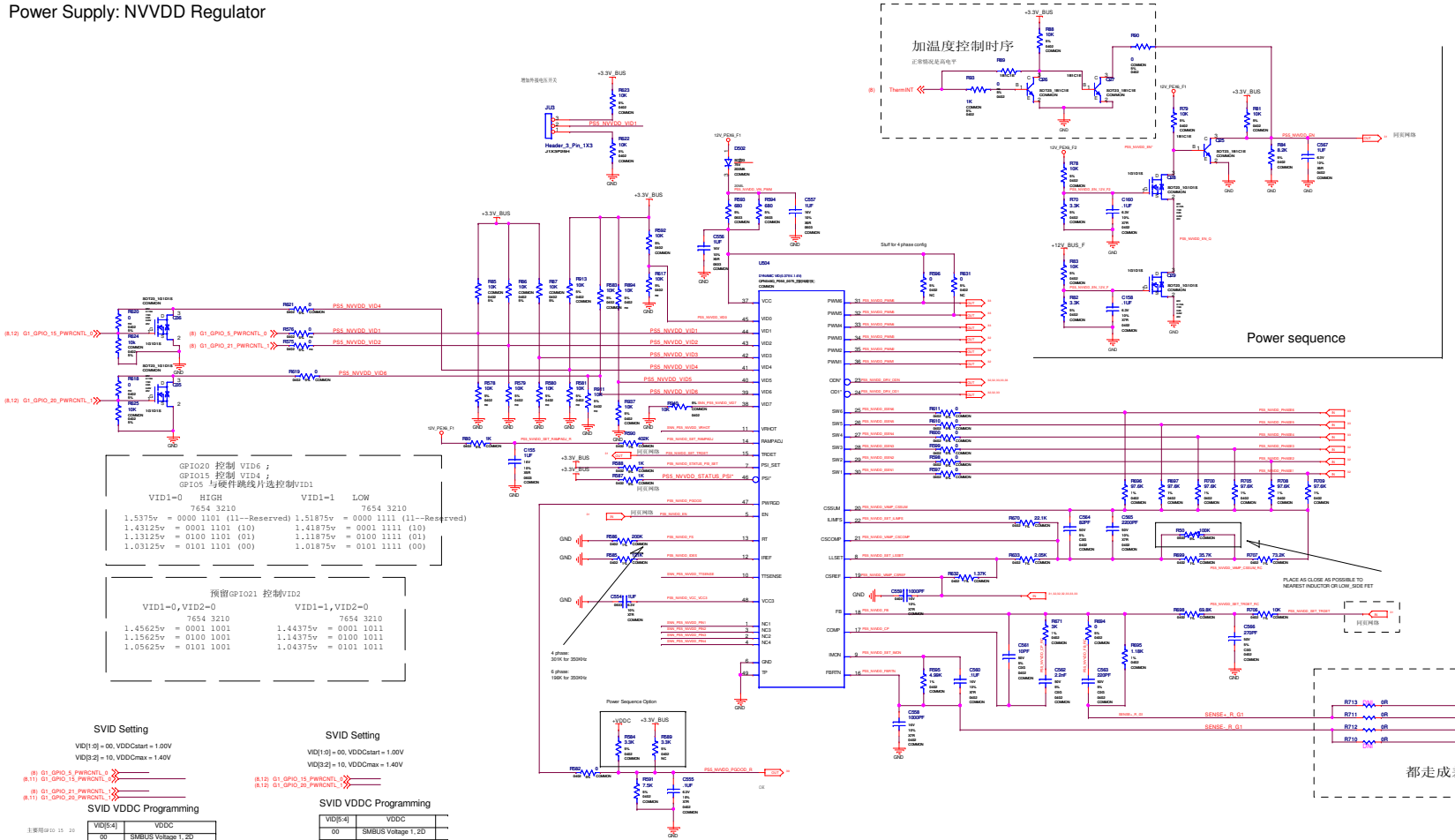
Power Supply: NVVDD Regulator



SVID Setting

VID[1:0] = 00, VDDCstart = 1.00V
VID[3:2] = 10, VDDCmax = 1.40V

SVID VDDC Programming

VID[5:4]	VDDC
00	SMBUS Voltage 1, 2D
01	SMBUS Voltage 2, 3D
10	SMBUS Voltage 3, OD
11	SMBUS Voltage 4, Reserved

SVID Setting

VID[1:0] = 00, VDDCstart = 1.00V
VID[3:2] = 10, VDDCmax = 1.40V

SVID VDDC Programming

VID[5:4]	VDDC
00	SMBUS Voltage 1, 2D
01	SMBUS Voltage 2, 3D
10	SMBUS Voltage 3, OD
11	SMBUS Voltage 4, Reserved

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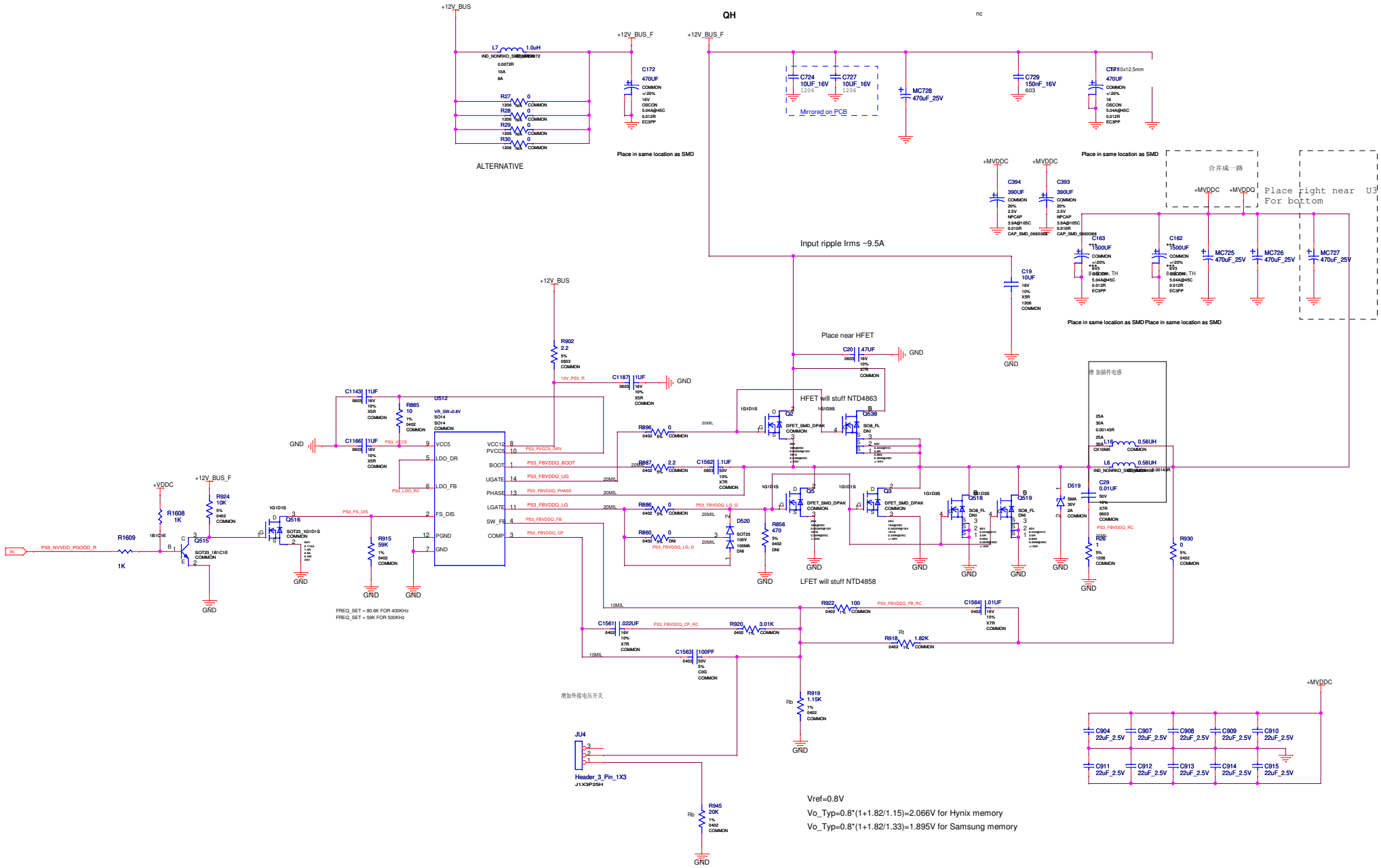

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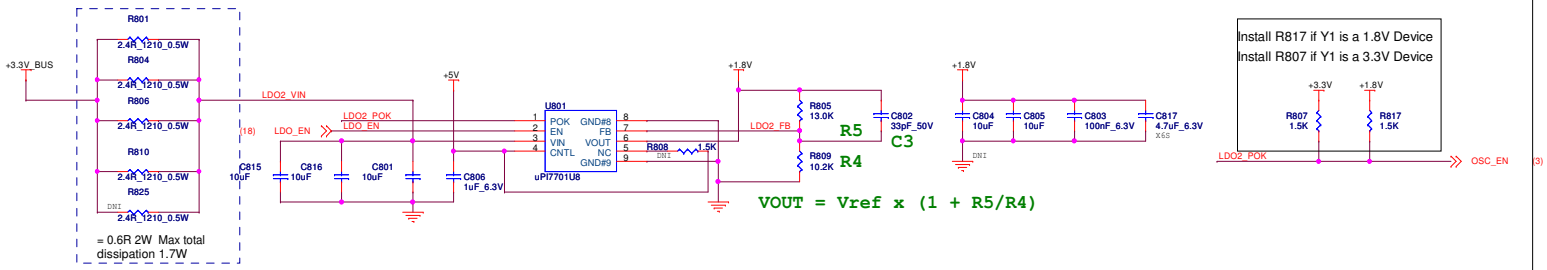
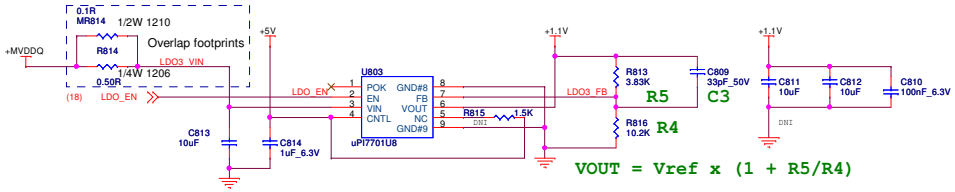
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX

PCB: Min 70mm sq. copper area for cooling

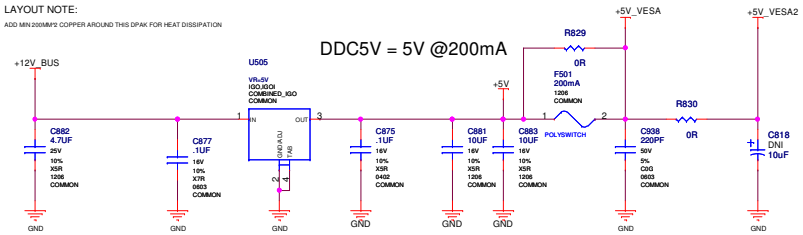


LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX

PCB: Min 70mm sq. copper area for cooling



5V and DDC5V Supply



F3V3 Supply

R819 << 15mA

R819+R818 << 30mA

Regulators for +5V, +5V_VESA and +5V_VESA2

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Title RH RV790XT GDDR5 DVI-I VO DVI-I FH

Doc No. 105-B790xx-00

See BOM for qualified filters

(3) A_DAC1_R — R1001 75R 402 — C1004 8.0pF 402 — L1001 47nH — ML1001 36NH — C1001 12pF_50V 402
(3) A_DAC1_RB — R1027 37.4R
(3) A_DAC1_G — R1002 75R 402 — C1005 8.0pF 402 — L1002 47nH — ML1002 36NH — C1002 12pF_50V 402
(3) A_DAC1_GB — R1028 37.4R
(3) A_DAC1_B — R1003 75R 402 — C1006 8.0pF 402 — L1003 47nH — ML1003 36NH — C1003 12pF_50V 402
(3) A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L100x and ML100x footprints are overlapped

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

For ESD Protection

+3.3V
+5V_VESA

+5V_VESA
C1010 68pF 603

MJ1001
1 R
2 G
3 B
11 MS0
12 MS1
4 MS2
15 MS3
9 NC
13 HS
14 VS
5 VSS
6 VSS#6
7 VSS#7
8 VSS#8
10 VSS#10
16 CASE
17 CASE#17
18 GND1
19 GND2
G3179C219-005

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

+5V
(3) DDC4DATA — R1005 2.2K — DDCDATA_DAC1_5V — R1006 33R 402 — DDCDATA_DAC1_R

+5V
(3) DDC4CLK — R1008 2.2K — DDCCLK_DAC1_5V — R1009 33R 402 — DDCCLK_DAC1_R

(3,8) HSYNC1 — U1999C 74VHC125 (9, 8, 10) — HSYNC_DAC1_B — R1010 10R 402 — HSYNC_DAC1_R
(3,8) VSYNC1 — U1999D 74VHC125 (12, 11, 13) — VSYNC_DAC1_B — R1011 10R 402 — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No Mechanical Key	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V
Q1021 MMBT3904 — R1022 10K — HPD_DVI2
(3) HPD1 — R1023 10K

+3.3V
R77 499 0402 1% COMMON
Q1259 MMBT3904 — R3026 10K
D1263 GREEN_LED

加符号标志

+5V_VESA
J1001
25 CASE
(3) T2X2M — 1 TMDS Data2-
(3) T2X2P — 2 TMDS Data2+
3 TMDS Data2/4 Shield
(3) T2X4M — 4 TMDS Data4-
(3) T2X4P — 5 TMDS Data4+
DDCCLK_DAC1_R — 6 DDC Clock
DDCDATA_DAC1_R — 7 DDC Data
VSYNC_DAC1_R — 8 Analog VSYNC
(3) T2X1M — 9 TMDS Data1-
(3) T2X1P — 10 TMDS Data1+
11 TMDS Data1/3 Shield
(3) T2X3M — 12 TMDS Data3-
(3) T2X3P — 13 TMDS Data3+
14 +5V Power
15 GND (for +5V)
16 Hot Plug Detect
(3) T2X0M — 17 TMDS Data0-
(3) T2X0P — 18 TMDS Data0+
19 TMDS Data0/5 Shield
(3) T2X5M — 20 TMDS Data5-
(3) T2X5P — 21 TMDS Data5+
22 TMDS Clock Shield
(3) T2XCP — 23 TMDS Clock+
(3) T2XCM — 24 TMDS Clock-
A_R_DAC1_F — C1 Analog Red
A_G_DAC1_F — C2 Analog Green
A_B_DAC1_F — C3 Analog Blue
HSYNC_DAC1_R — C4 Analog HYNC
C5 Analog GND
C5A Analog GND#C6
26 CASE#26
27 CASE#27
28 CASE#28
DVI_CONNECTOR

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Doc No. 105-B790xx-00

See BOM for qualified filters

(3) A_DAC2_R — R2027 37.4R — R2001 75R 402 — C2004 8.0pF 402 — L2001 47nH — ML2001 36NH — C2001 12pF_50V 402

(3) A_DAC2_RB — R2027 37.4R

(3) A_DAC2_G — R2028 37.4R — R2002 75R 402 — C2005 8.0pF 402 — L2002 47nH — ML2002 36NH — C2002 12pF_50V 402

(3) A_DAC2_GB — R2028 37.4R

(3) A_DAC2_B — R2029 37.4R — R2003 75R 402 — C2006 8.0pF 402 — L2003 47nH — ML2003 36NH — C2003 12pF_50V 402

(3) A_DAC2_BB — R2029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L200x and ML200x footprints are overlapped

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

+3.3V
+5V_VESA2

C2010 68pF 603

MJ2001 — G3179C219-005

MJ2001	
1	R
2	G
3	B
11	MS0
12	MS1
4	MS2
15	MS3
9	NC
13	HS
14	VS
5	VSS
6	VSS#6
7	VSS#7
8	VSS#8
10	VSS#10
16	CASE
17	CASE#17
18	GND1
19	GND2

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

(3) DDC3DATA — +5V — R2005 2.2K 402 — DDCDATA_DAC2_5V — R2006 33R 402 — DDCDATA_DAC2_R

(3) DDC3CLK — +5V — R2008 2.2K 402 — DDCCLK_DAC2_5V — R2009 33R 402 — DDCCLK_DAC2_R

C1999 100nF 6.3V

(3,8) HSYNC2 — U1999A 74VHC125 — HSYNC_DAC2_B — R2010 10R 402 — HSYNC_DAC2_R

(3,8) VSYNC2 — 74VHC125 U1999B — VSYNC_DAC2_B — R2011 10R 402 — VSYNC_DAC2_R

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

Q2031 MMBT3904 — R2032 10K — HPD_DPB — R2034 0 — HPD_DVI1

(7) GPIO_18 — R2033 10K

R75 499 0402 1% COMMON — Q1256 MMBT3904 — R2025 10K — D1257 GREEN_LED

R92 10k 0402 1% COMMON — Q7009 BSH111

R2007 2.2K 402 — R2014 33R

ddsda1 (8)

R91 10k 0402 1% COMMON — Q7010 BSH111

R2013 2.2K 402 — R2012 33R

ddclk1 (8)

C124 .1UF 16V 10% X5R 0402 COMMON

J504 HDMI HDMI COMMON

J504	
20	SHIELD1
21	SHIELD2
19	HP_DET
18	+5V
17	DDC/CEC_GND
16	SDA
15	SCL
14	RESERVED
13	CEC
12	CK-
11	CK_SHIELD
10	CK+
9	D0-
8	D0_SHIELD
7	D0+
6	D1-
5	D1_SHIELD
4	D1+
3	D2-
2	D2_SHIELD
1	D2+
22	SHIELD3
23	SHIELD4

DDC1DATA_R
DDC1CLK_R

(17) T2XCBM — T2XCBM — T2XCBP
(17) T2XCBP — T2XCBP

T1X3M — T1X3P — T1X4M — T1X4P — T1X5M — T1X5P

DDC1CLK_R — R2035 0 — DDCCLK_DAC2_R

DDC1DATA_R — R2036 0 — DDCDATA_DAC2_R

For ESD Protection Place Close to Connector

(3) T1X2M — T1X2P — T1X3M — T1X3P — T1X4M — T1X4P — T1X5M — T1X5P — T1X0M — T1X0P — T1X1M — T1X1P — T1XCP — T1XCM

J2001

J2001	
25	CASE
1	TMDS Data2-
2	TMDS Data2+
3	TMDS Data2/4 Shield
4	TMDS Data4-
5	TMDS Data4+
6	DDC Clock
7	DDC Data
8	Analog VSYNC
9	TMDS Data1-
10	TMDS Data1+
11	TMDS Data1/3 Shield
12	TMDS Data3-
13	TMDS Data3+
14	+5V Power
15	GND (for +5V)
16	Hot Plug Detect
17	TMDS Data0-
18	TMDS Data0+
19	TMDS Data0/5 Shield
20	TMDS Data5-
21	TMDS Data5+
22	TMDS Clock Shield
23	TMDS Clock+
24	TMDS Clock-
C1	Analog Red
C2	Analog Green
C3	Analog Blue
C4	Analog HYNC
C5	Analog GND
C5A	Analog GND#C6
26	CASE#26
27	CASE#27
28	CASE#28

DVI_CONNECTOR

DDCCLK_DAC2_R
DDCDATA_DAC2_R
VSYNC_DAC2_R
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
HSYNC_DAC2_R

HPD_DVI1

Q2021 MMBT3904 — R2022 10K — (8) HPD2 — R2023 10K

R76 499 0402 1% COMMON — Q1257 MMBT3904 — R2024 10K — D1258 GREEN_LED

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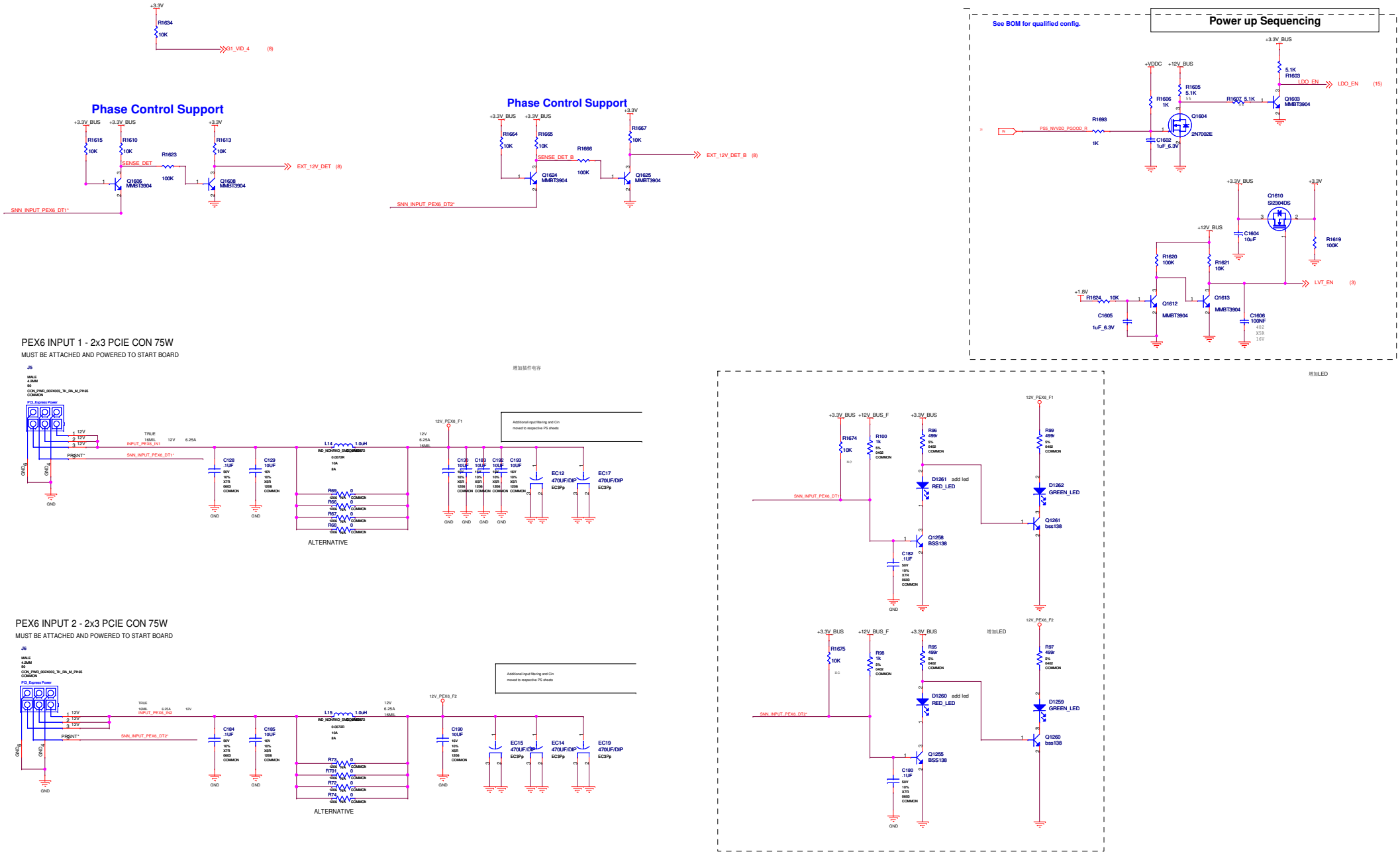
Title: RH RV790XT GDDR5 DVI-I VO DVI-I FH

Doc No. 105-B790xx-00



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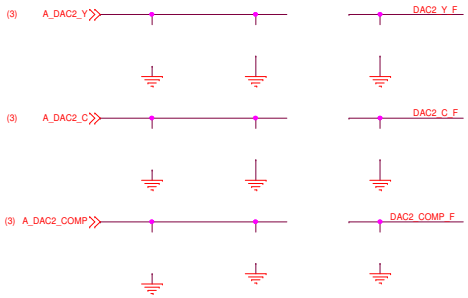
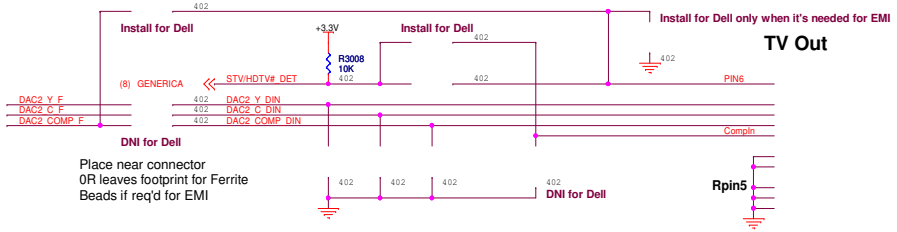
Title	RH RV790XT GDDR5 DVI-I VO DVI-I FH
Doc No.	105-B790xx-00





- 4-pin Svideo MiniDIN P/N 6070001000G

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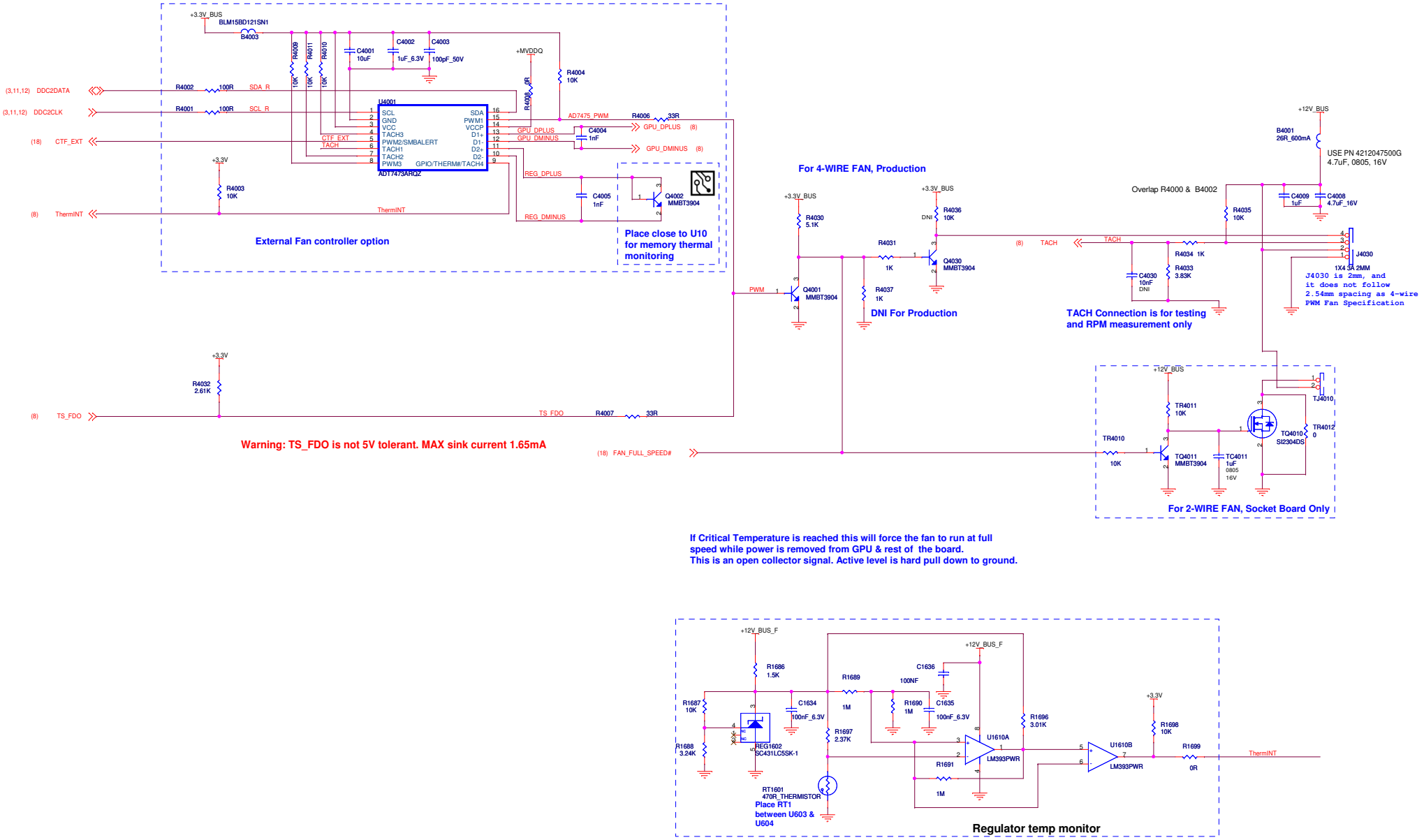

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ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY1
ANTISTATIC
BAG
6_X_11

BKT1
BRACKET
DUAL
80200388B0G

BKT1: DS, DVI - DIN - DVI

ASSY-SCREW5
SCREW
SCREW

SK1
Socket_RV770

MT2
MT_Hole_0.136_in_6VIA

PCB1
PCB
109-B33931-00A

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Title	Schematic No.	Date:
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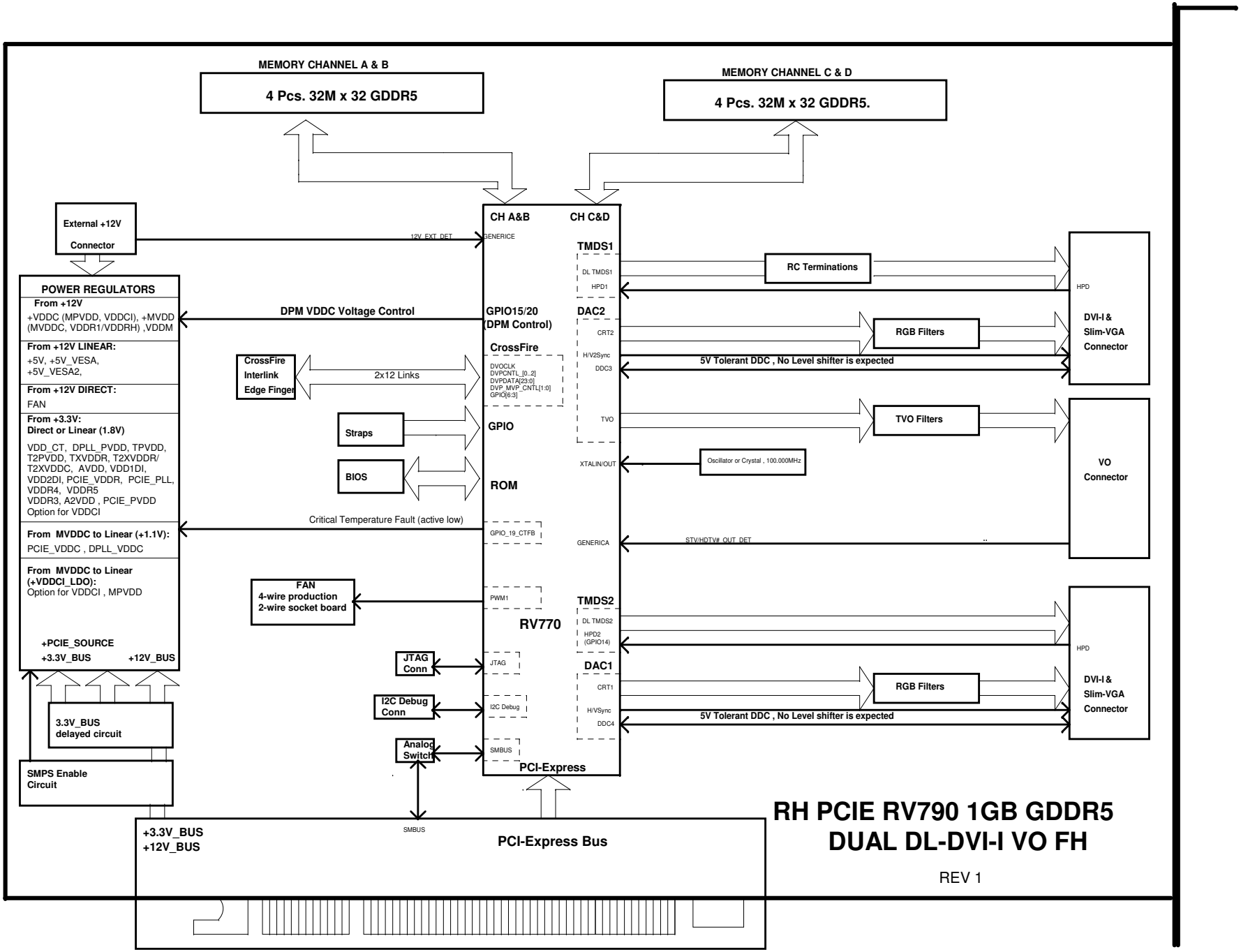
REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI扭, ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/01/04	Initial design for B790
	00	09/02/03	-00 Release with no Schematic change however C817 is refreshed to correct the footprint issue on rev A



RH PCIE RV790 1GB GDDR5
DUAL DL-DVI-I VO FH

REV 1

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