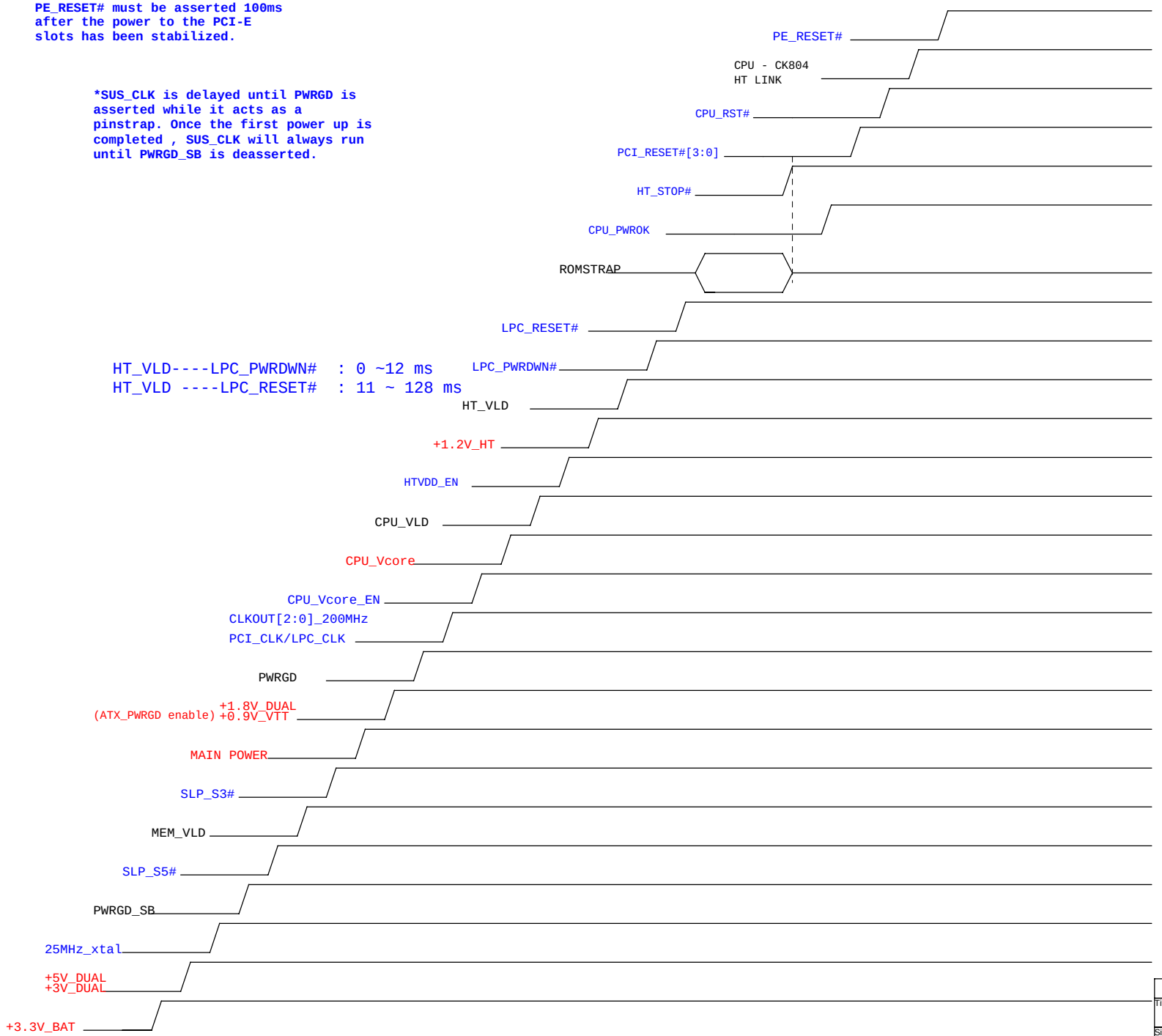
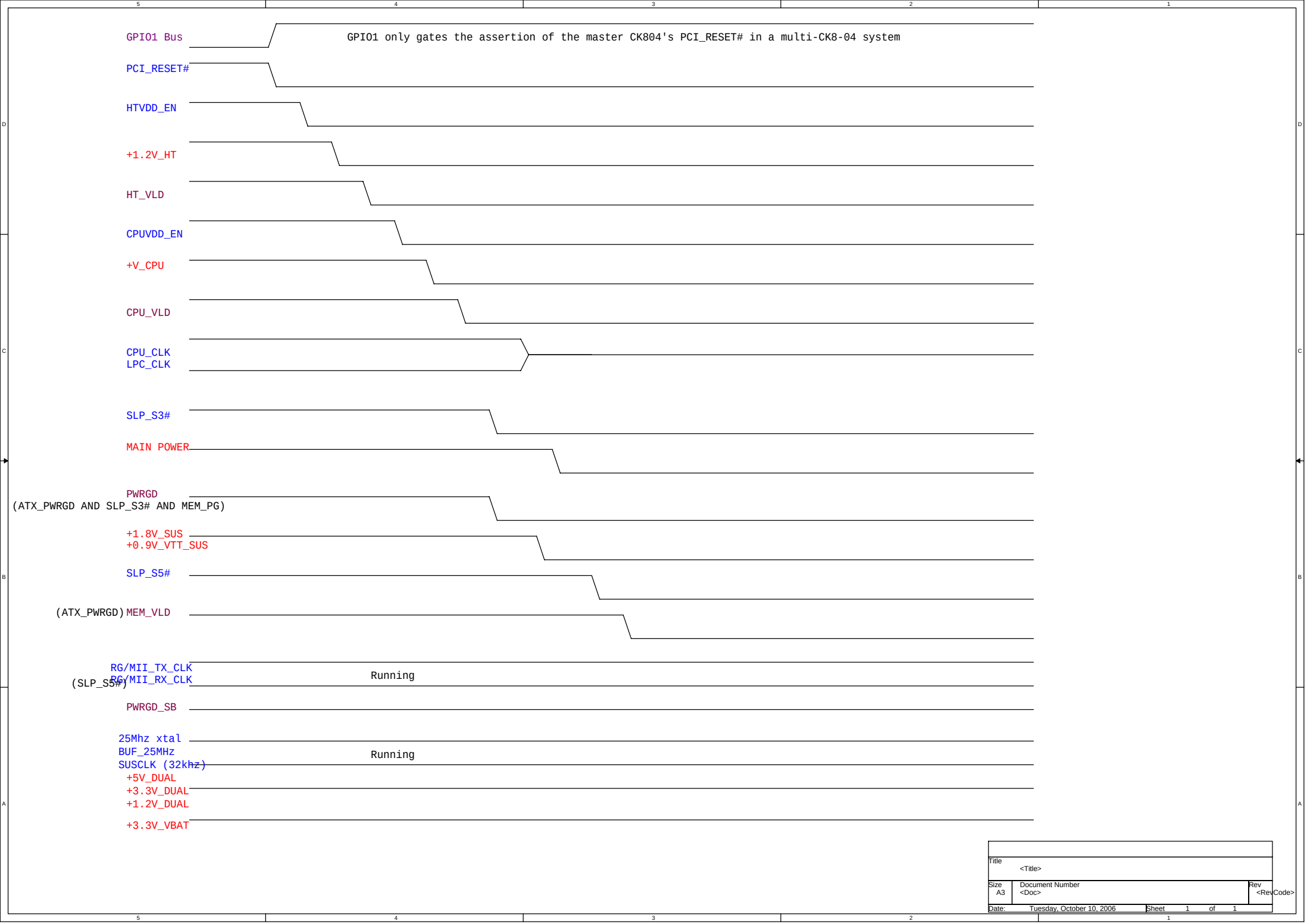
PE_RESET# must be asserted 100ms after the power to the PCI-E slots has been stabilized.

***SUS_CLK is delayed until PWRGD is asserted while it acts as a pinstrap. Once the first power up is completed , SUS_CLK will always run until PWRGD_SB is deasserted.**



Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, October 10, 2006	Sheet 1 of 1	



Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, October 10, 2006	Sheet 1 of 1	