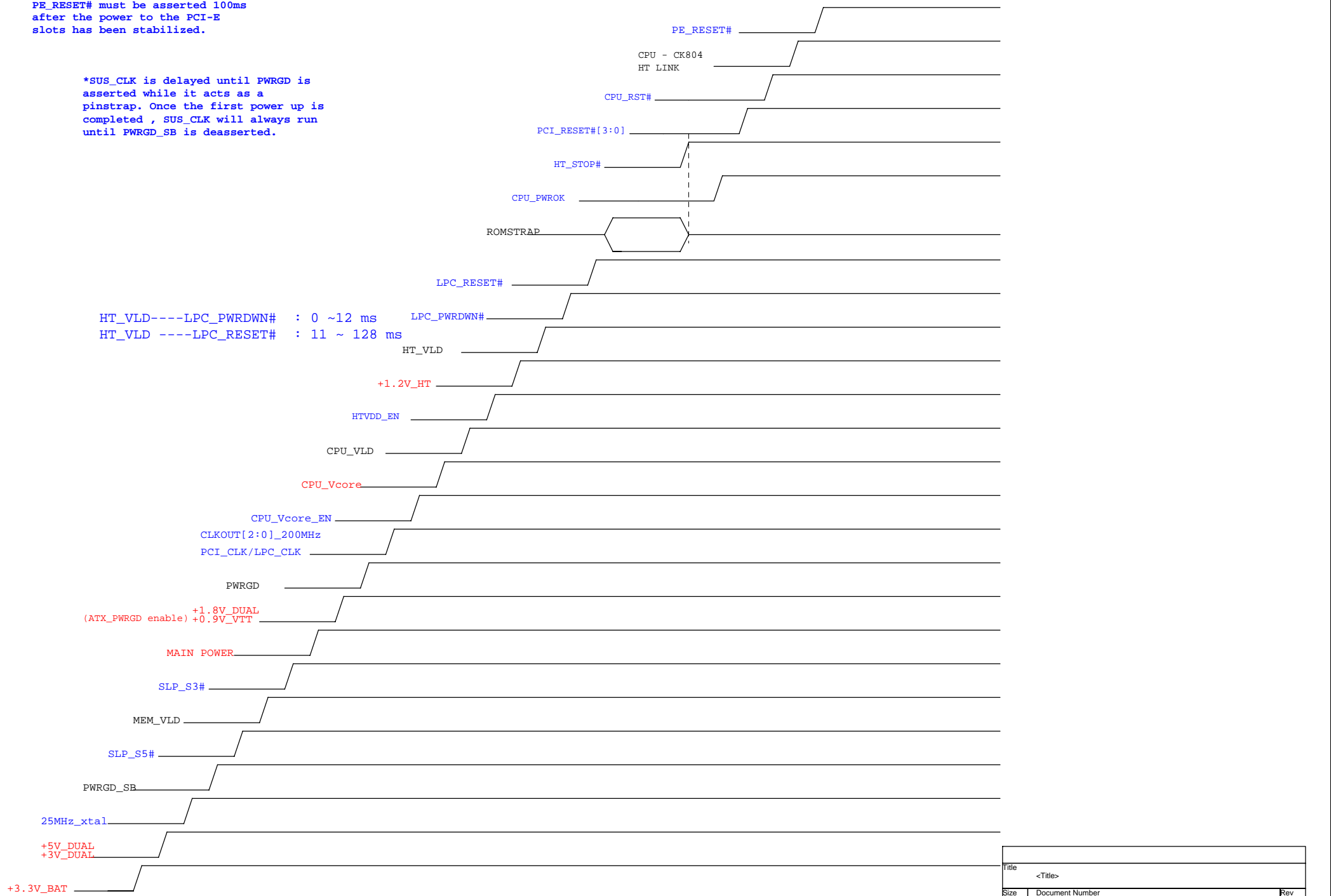


PE_RESET# must be asserted 100ms after the power to the PCI-E slots has been stabilized.

*SUS_CLK is delayed until PWRGD is asserted while it acts as a pinstrap. Once the first power up is completed, SUS_CLK will always run until PWRGD_SB is deasserted.



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GPI01 Bus GPI01 only gates the assertion of the master CK804's PCI_RESET# in a multi-CK8-04 system

PCI_RESET#

HTVDD_EN

+1.2V_HT

HT_VLD

CPUVDD_EN

+V_CPU

CPU_VLD

CPU_CLK
LPC_CLK

SLP_S3#

MAIN POWER

PWRGD

(ATX_PWRGD AND SLP_S3# AND MEM_PG)

+1.8V_SUS

+0.9V_VTT_SUS

SLP_S5#

(ATX_PWRGD) MEM_VLD

RG/MII_TX_CLK

Running

(SLP_S5#) RG/MII_RX_CLK

PWRGD_SB

25Mhz xtal

BUF_25MHz

SUSCLK (32khz)

Running

+5V_DUAL

+3.3V_DUAL

+1.2V_DUAL

+3.3V_VBAT

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