



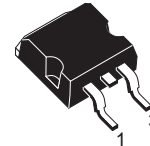
STB75NH02L

N-CHANNEL 24V - 0.0062Ω -75A - D²PAK STripFET™ III POWER MOSFET

TARGET DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB75NH02L	24V	< 0.008Ω	75A

- TYPICAL R_{DS(on)} = 0.0062Ω @ 10 V
- TYPICAL R_{DS(on)} = 0.008Ω @ 5 V
- R_{DS(ON)} * Q_g INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING D²PAK (TO-263) POWER PACKAGE IN TUBE (NO SUFFIX) OR IN TAPE & REEL (SUFFIX "T4")



**D²PAK
TO-263**
(Suffix "T4")

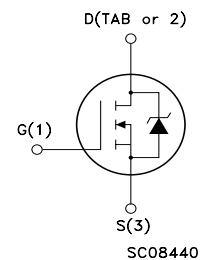
DESCRIPTION

The **STB75NH02L** utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB75NH02LT4	B75NH02L	D ² PAK	TAPE & REEL

STB75NH02L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{\text{spike(1)}}$	Drain-source Voltage Rating	30	V
V_{DS}	Drain-source Voltage ($V_{\text{GS}} = 0$)	24	V
V_{DGR}	Drain-gate Voltage ($R_{\text{GS}} = 20 \text{ k}\Omega$)	24	V
V_{GS}	Gate- source Voltage	± 20	V
I_{D}	Drain Current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	75	A
I_{D}	Drain Current (continuous) at $T_{\text{C}} = 100^{\circ}\text{C}$	53	A
$I_{\text{DM (5)}}$	Drain Current (pulsed)	300	A
P_{TOT}	Total Dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	85	W
	Derating Factor	1	W/ $^{\circ}\text{C}$
$E_{\text{AS (2)}}$	Single Pulse Avalanche Energy	TBD	mJ
T_{stg}	Storage Temperature	-55 to 175	$^{\circ}\text{C}$
T_{j}	Max. Operating Junction Temperature		

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1	$^{\circ}\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	$^{\circ}\text{C}/\text{W}$
T_{l}	Maximum Lead Temperature for Soldering Purpose	300	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{\text{CASE}} = 25^{\circ}\text{C}$ UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{(BR)DSS}}$	Drain-source Breakdown Voltage	$I_{\text{D}} = 25 \text{ mA}$, $V_{\text{GS}} = 0$	24			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{\text{GS}} = 0$)	$V_{\text{DS}} = 20\text{V}$ $V_{\text{DS}} = 20\text{V}$, $T_{\text{C}} = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{\text{DS}} = 0$)	$V_{\text{GS}} = \pm 20\text{V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\mu\text{A}$	1			V
$R_{\text{DS(on)}}$	Static Drain-source On Resistance	$V_{\text{GS}} = 10 \text{ V}$, $I_{\text{D}} = 30 \text{ A}$ $V_{\text{GS}} = 5 \text{ V}$, $I_{\text{D}} = 30 \text{ A}$		0.0062 0.008	0.008 0.014	Ω Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)
DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (3)	Forward Transconductance	$V_{DS} = 15\text{ V}$, $I_D = 30\text{ A}$		TBD		S
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		2000		pF
C_{oss}	Output Capacitance			420		pF
C_{rss}	Reverse Transfer Capacitance			210		pF
R_g	Gate Input Resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1		Ω

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 10\text{ V}$, $I_D = 37.5\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		TBD TBD		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 10\text{ V}$, $I_D = 75\text{ A}$, $V_{GS} = 10\text{ V}$		35 TBD TBD	47	nC nC nC
Q_{oss} (4)	Output Charge	$V_{DS} = 16\text{ V}$, $V_{GS} = 0$		TBD		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off-Delay Time Fall Time	$V_{DD} = 10\text{ V}$, $I_D = 37.5\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		TBD TBD		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				75	A
I_{SDM} (1)	Source-drain Current (pulsed)				300	A
V_{SD} (3)	Forward On Voltage	$I_{SD} = 37.5\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 75\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 15\text{ V}$, $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		TBD TBD TBD		ns nC A

1. Guaranteed when external $R_g = 4.7\Omega$ and $t_f < t_r$ max
2. Starting $T_j = 25^\circ\text{C}$, $I_D = 25\text{ A}$, $V_{DD} = 15\text{ V}$
3. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
4. $Q_{oss} = C_{oss} \cdot \Delta V_{in}$, $C_{oss} = C_{gd} + C_{ds}$. See Appendix A
5. Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit

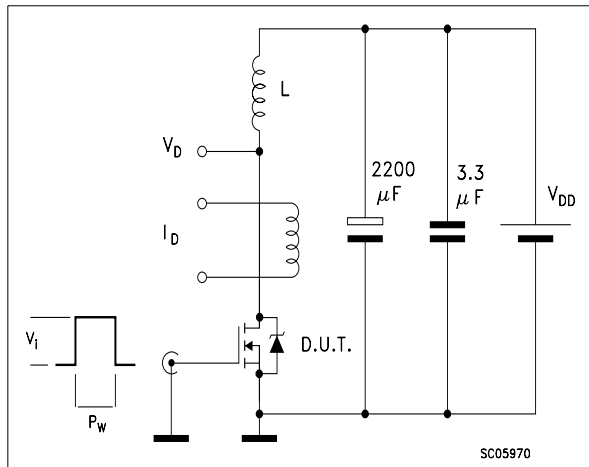


Fig. 2: Unclamped Inductive Waveform

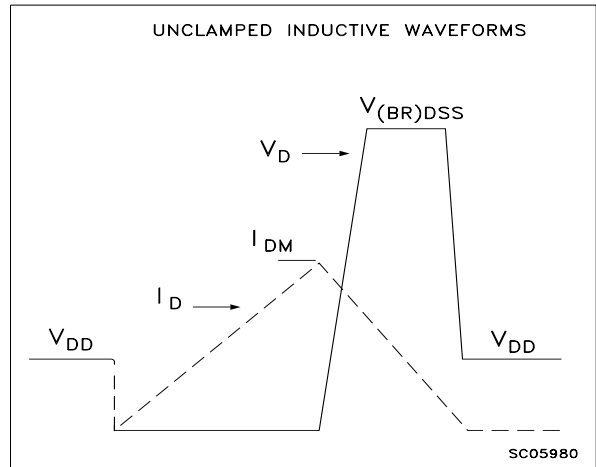


Fig. 3: Switching Times Test Circuit For Resistive Load

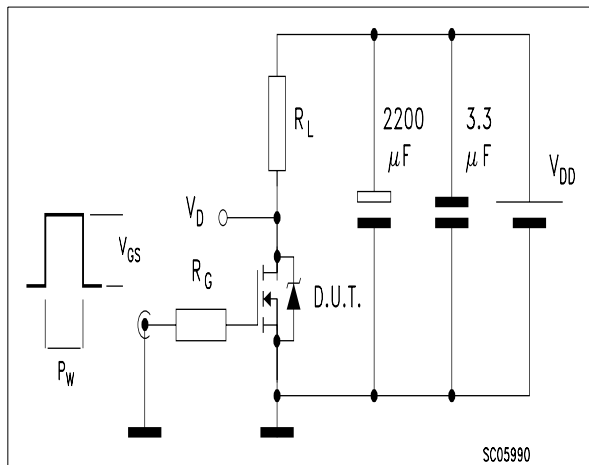


Fig. 4: Gate Charge test Circuit

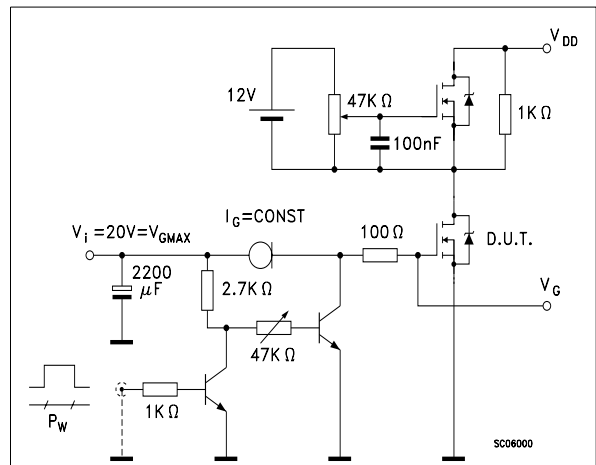
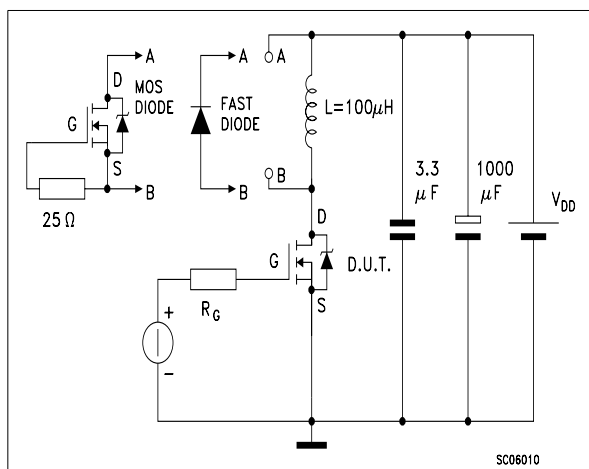
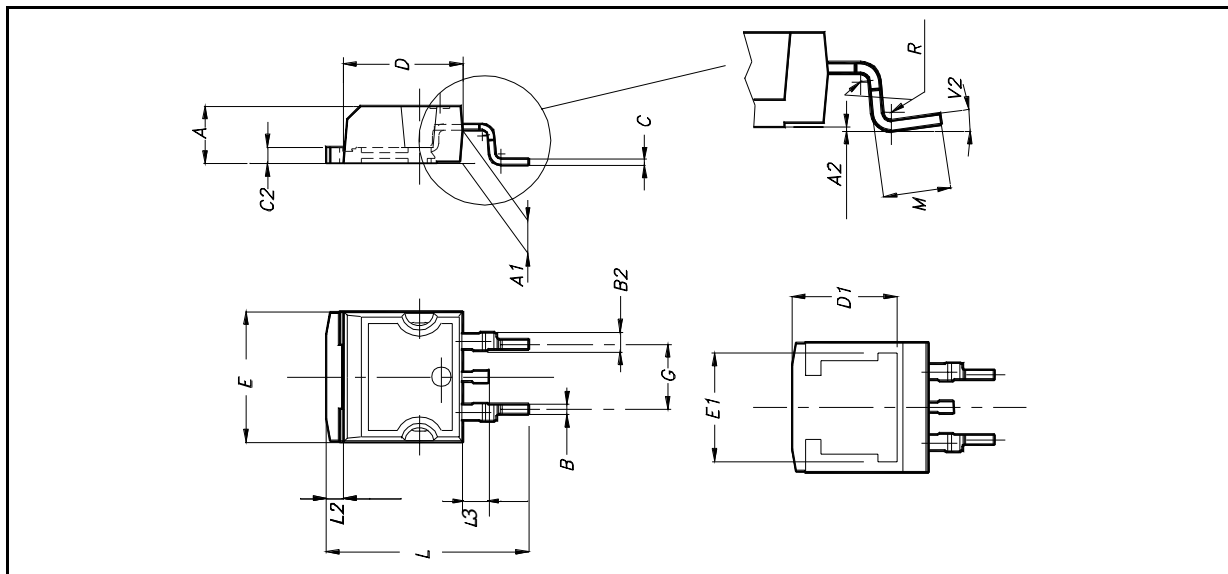


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

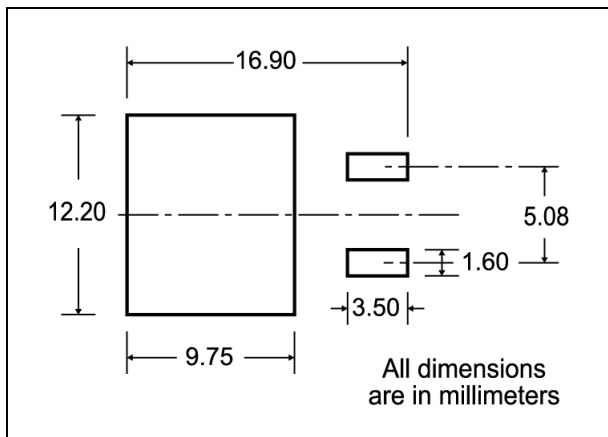


D²PAK MECHANICAL DATA

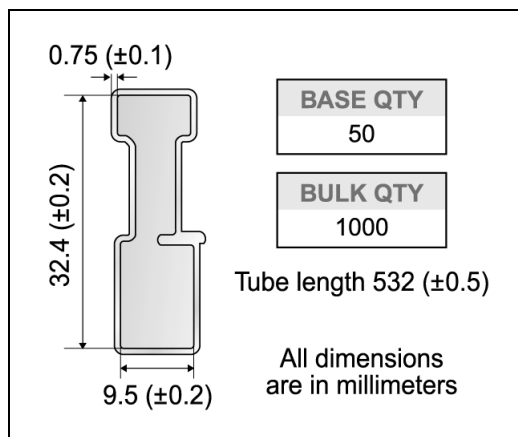
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

Diagram showing the tape mechanical data. It includes a circular view of the tape with dimensions A, B, C, D, and G. A 40 mm min. access hole is shown at the slot location. The tape slot in the core has a 2.5 mm min. width. The full radius is also indicated. A side view shows dimensions T, N, and G measured at the hub.

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

Diagrams showing the tape and reel shipment details. The top cover tape has dimensions K₀, T, D, P₂, P₀, E, F, W, B₀, D₁, A₀, P₁. A 10-pitch cumulative tolerance on tape is ±0.2 mm. The center line of the cavity is shown. The user direction of feed is indicated. The reel has a bending radius of R min. and a feed direction arrow.

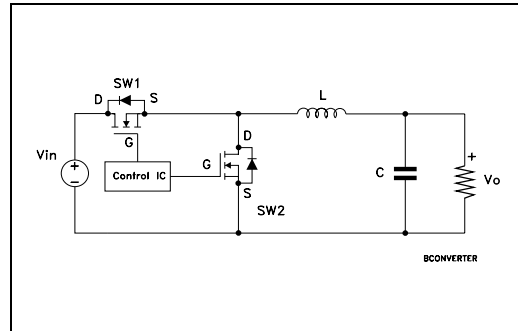
* on sales type



Appendix A: Buck Converter Power Losses Estimation

DESCRIPTION

The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.



The low side (SW2) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{OSS} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW1 during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{GG} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1-\delta)$
$P_{switching}$		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_n}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	$1 * V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q)}$		$Q_g(SW1) * V_{gg} * f$	$Q_{gl(SW2)} * V_{gg} * f$
P_{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
δ	Duty-Cycle
Q_{gsth}	Post Threshold Gate Charge
Q_{gls}	Third Quadrant Gate Charge
$P_{conduction}$	On State Losses
$P_{switching}$	On-off Transition Losses
P_{diode}	Conduction and Reverse Recovery Diode Losses
P_{diode}	Gate Drive Losses
P_{Qoss}	Output Capacitance Losses

¹ Dissipated by SW1 during turn-on

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