Integrated Circuit Systems, Inc.

ICS843021

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS843021 is a Gigabit Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS843021 uses a 25MHz crystal to synthesize 125MHz. The ICS843021 has excellent phase jitter performance, over the 1.875MHz – 20MHz integration range. The ICS843021 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- 1 differential 3.3V LVPECL output
- Crystal oscillator interface designed for 22.4MHz - 28MHz, 18pF parallel resonant crystal
- Output frequency range: 112MHz - 140MHz
- VCO range: 560MHz to 700MHz
- Output duty cycle range: 49% - 51%
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.37ps (typical)
- RMS phase noise at 125MHz (typical)

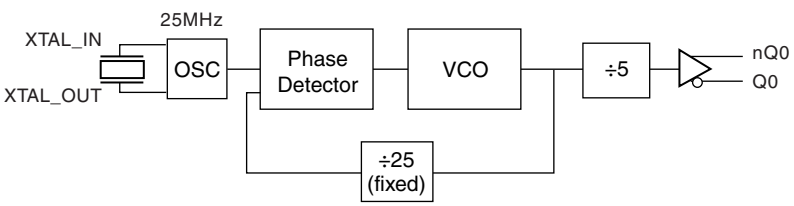
Offset	Noise Power
100Hz	-94.2 dBc/Hz
1KHz	-122.8 dBc/Hz
10KHz	-132.2 dBc/Hz
100KHz	-131.3 dBc/Hz

- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Lead-Free package fully RoHS compliant

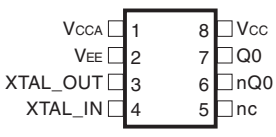
FREQUENCY TABLE - TYPICAL APPLICATIONS

Inputs	Output Frequency (MHz)
Crystal Frequency (MHz)	
25	125
26.6	133

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS843021
8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CCA}	Power		Analog supply pin.
2	V_{EE}	Power		Negative supply pin.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	nc	Unused		No connect.
6, 7	nQ0, Q0	Output		Differential clock outputs. LVPECL interface levels.
8	V_{CC}	Power		Core supply pin.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±10%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current				85	mA

TABLE 3B. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±10%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency; NOTE 1		14		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

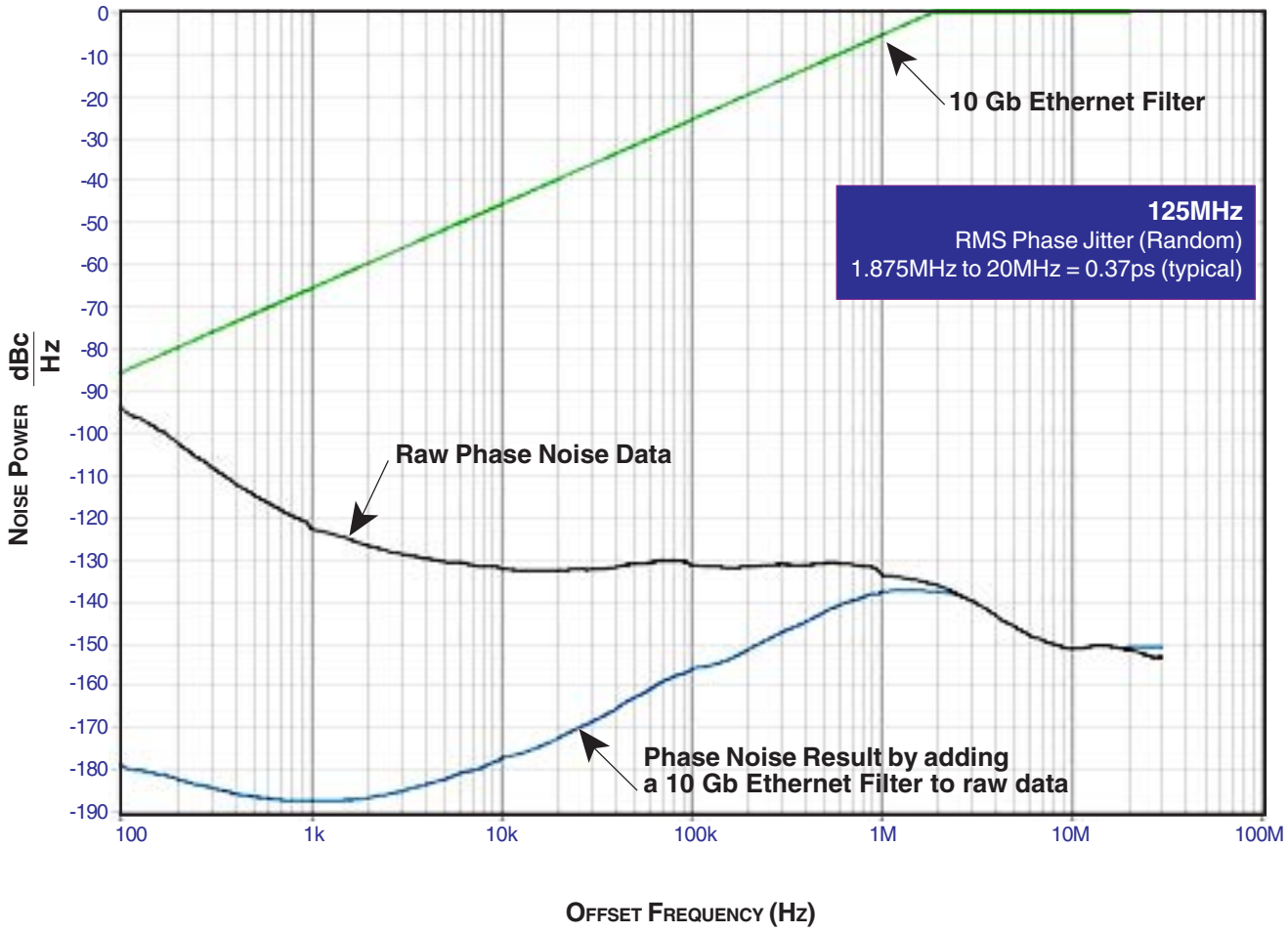
NOTE 1: Input frequency is limited to a range of 22.4MHz - 28MHz due to VCO range.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±10%, TA=0°C TO 70°C

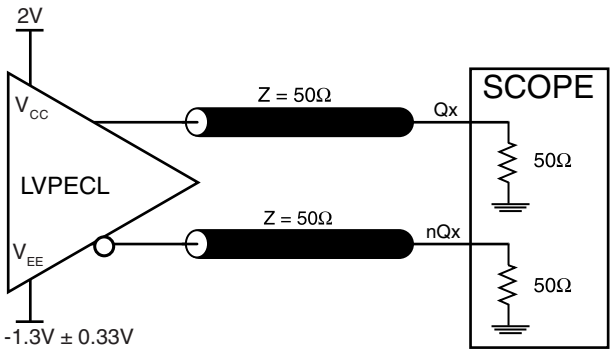
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		112		140	MHz
$t$jit(Ø)	RMS Phase Jitter, (Random); NOTE 1	125MHz (Intergration Range: 1.875MHz to 20MHz)		0.37		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle		49		51	%

NOTE 1: Please refer to the Phase Noise Plot.

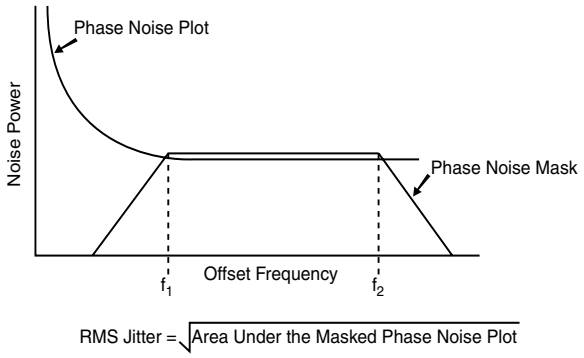
TYPICAL PHASE NOISE AT 125MHZ



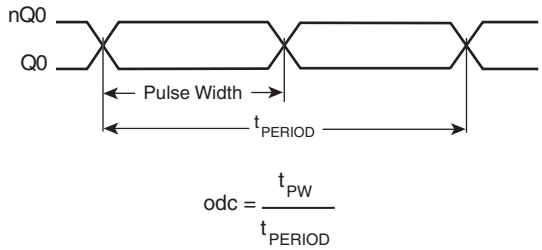
PARAMETER MEASUREMENT INFORMATION



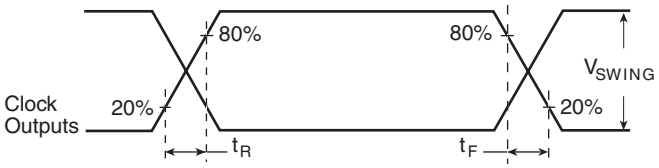
3.3V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843021 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, and V_{CCA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

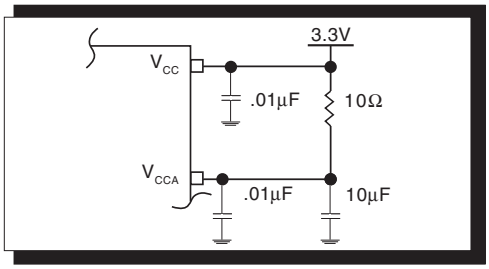


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843021 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

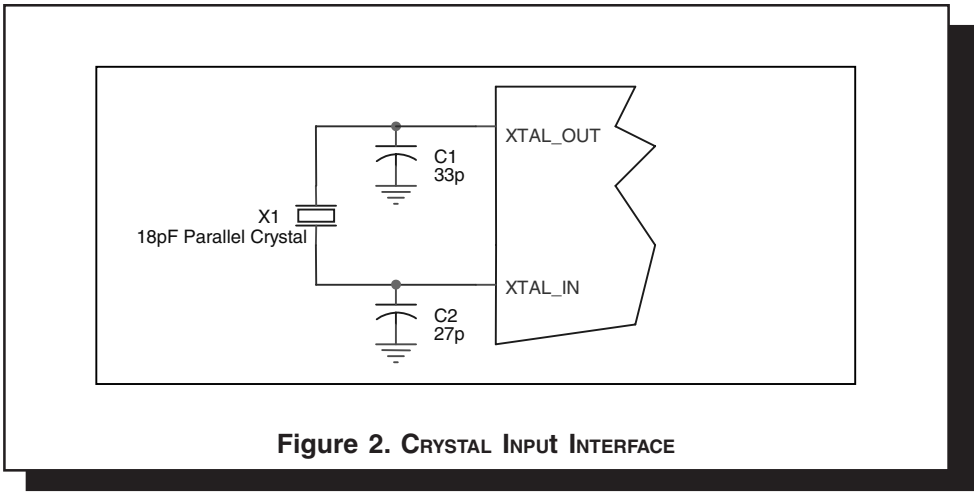


Figure 2. CRYSTAL INPUT INTERFACE

APPLICATION SCHEMATIC

Figure 3A shows a schematic example of the ICS843021. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF parallel resonant 25MHz crystal is used for generating 125MHz output frequency. The C1 = 27pF and C2 = 33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.

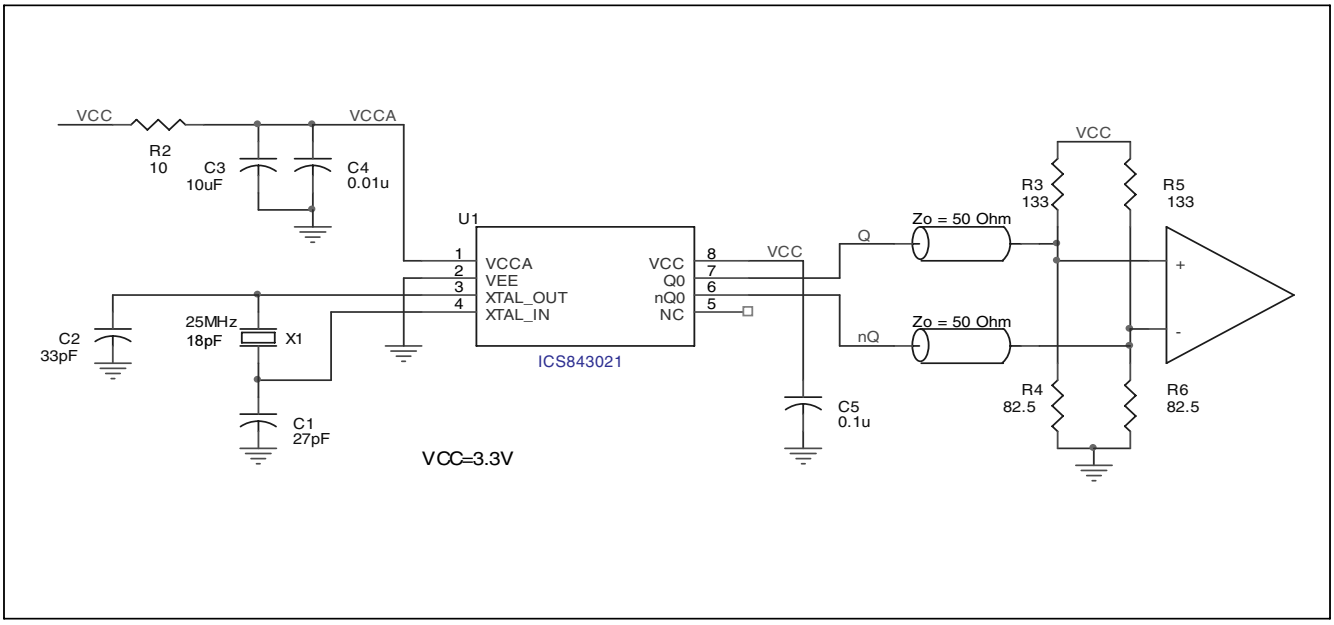


FIGURE 3A. ICS843021 SCHEMATIC EXAMPLE

PC BOARD LAYOUT EXAMPLE

Figure 3B shows an example of ICS843021 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 6.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

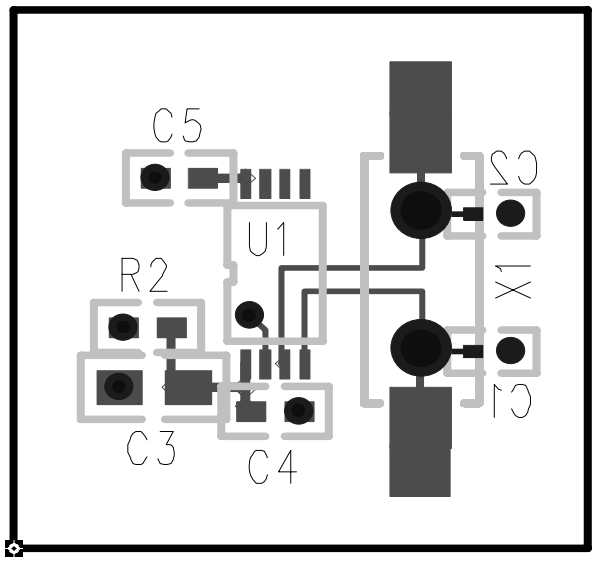


FIGURE 3B. ICS843021 PC BOARD LAYOUT EXAMPLE

TABLE 6. FOOTPRINT TABLE

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2	0603

NOTE: Table 6, lists component sizes shown in this layout example.

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843021.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843021 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.63V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.63V * 85mA = **308.6mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**

Total Power $_{\_MAX}$ (3.63V, with all outputs switching) = 308.6mW + 30mW = **338.6mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.339W * 90.5°C/W = 100.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

NOTE: Most modern PCB designs use multi-layered boards.

3. Calculations and Equations.
The purpose of this section is to derive the power dissipated into the load.
LVPECL output driver circuit and termination are shown in *Figure 3.*

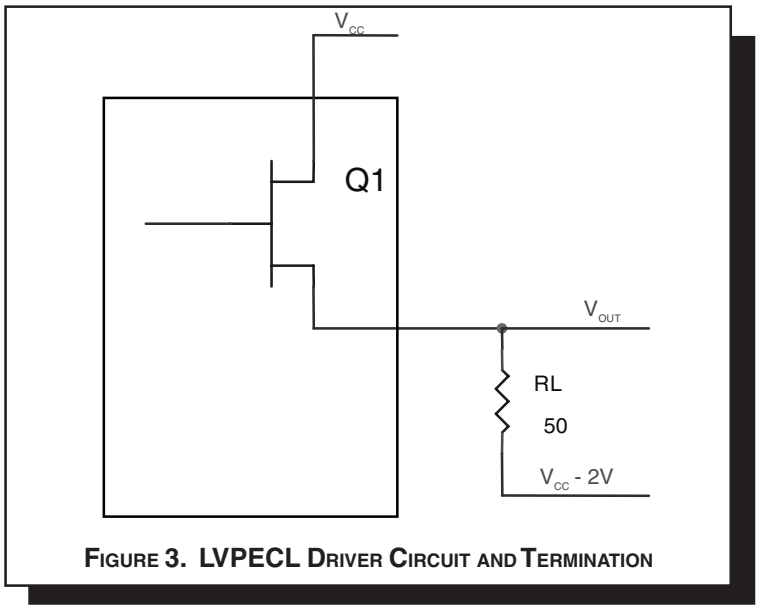


FIGURE 3. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS843021 is: 1928

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

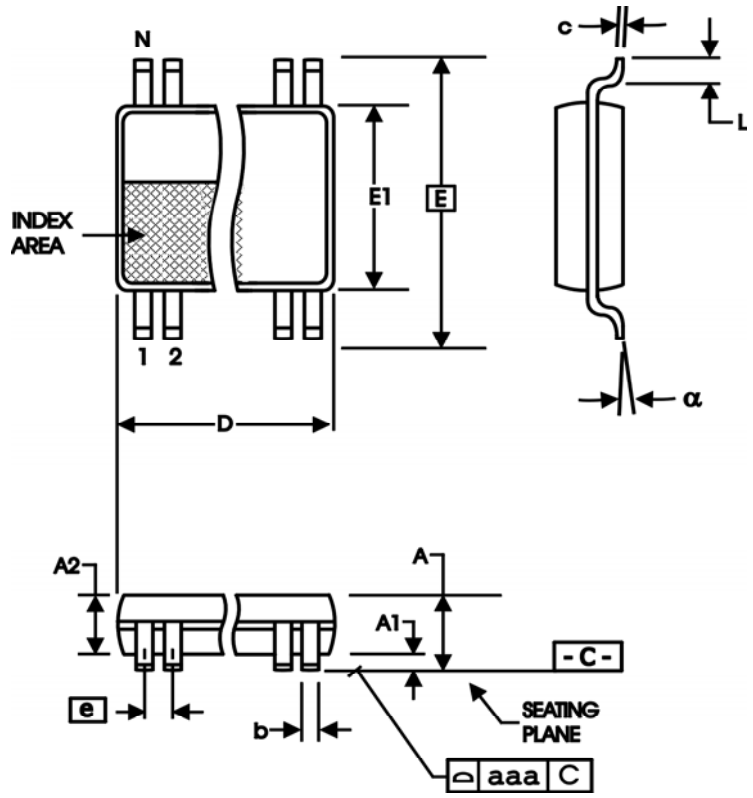


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843021AG	3021A	8 lead TSSOP	tube	0°C to 70°C
ICS843021AGT	3021A	8 lead TSSOP	2500 tape & reel	0°C to 70°C
ICS843021AGLF	021AL	8 lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS843021AGLFT	021AL	8 lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B		1	Added Function Table. Features section - updated Crystal, Output Frequency & VCO range bullets.	10/6/04
	T4	3	Crystal Characteristics Table - changed Frequency from 25MHz typical to 14MHz min. and 40MHz max. Added Note 1.	
	T5	3	AC Characteristics Table - changed Output Frequency from 125MHz typical to 112MHz min. and 140MHz max.	
B	T9	12	Ordering Information Table - corrected count from 154 per tube to 100	10/15/04
C	T3A	3	Power Supply Table - increased V_{CC} to 3.3V ± 10% from 5% and is reflected throughout the datasheet.	11/3/04
C		3	Absolute Maximum Ratings - corrected Package Thermal Impedance air flow.	11/30/04
	T6	8	Thermal Resistance Table - corrected air flow.	
	T7	10	Corrected air flow in table.	
	T9	12	Ordering Information Table - corrected marking.	
C		1	Features Section - added Lead-Free bullet.	3/31/05
	T9	12	Ordering Information Table - added Lead-Free part number.	