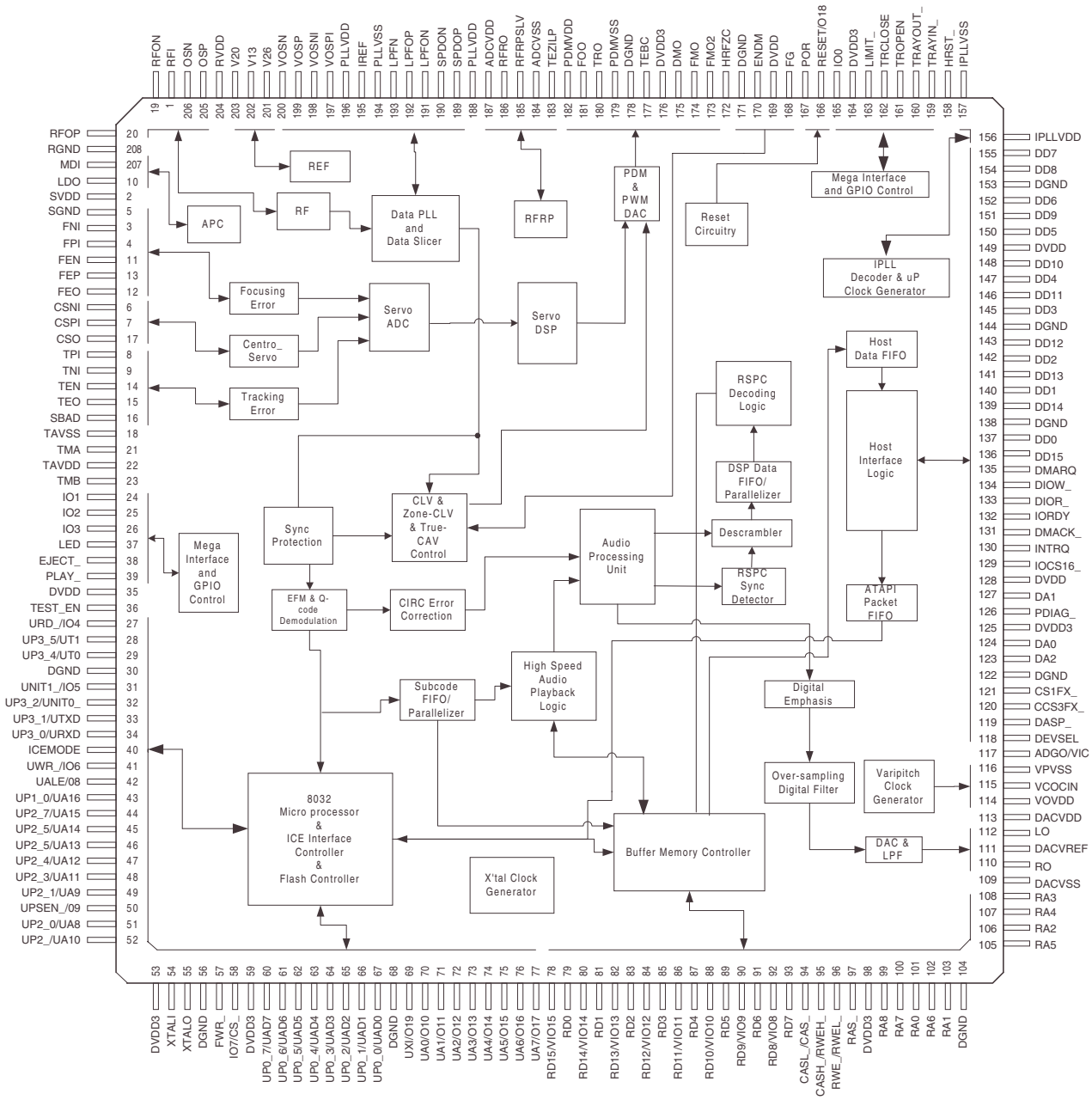
• IC501 (MT1199E) : RF+DSP+ATAPI DECODER+μ-COM

Block Diagram



• IC501 MT1199E

Pin Description

Pin Numbers	Symbol	Type	Description
RF Interface			
208	RGND	Ground	Ground pin for RF and related analog circuitry.
204	RVDD	Analog Power(3.3V)	Power for RFand related analog circuitry.
1	RFI	Analog Input	RF signal input.
2	SVDD	Analog Power(3.3V)	Power for servo signal generator and related analog circuitry.
3	FNI	Analog Input	Main beam I-V amplifier (A+C) input.
4	FPI	Analog Input	Main beam I-V amplifier (B+D) input.
5	SGND	Ground	Ground pin for servo signal generator and related analog circuitry.
6	CSNI	Analog Input	Central Servo input 1
7	CSPI	Analog Input	Central Servo input 2.
8	TPI	Analog Input	Sub beam I -V amplifier F input.
9	TNI	Analog Input	Sub beam I-V amplifier E input.
11	FEN	Analog Input	Negative input of focusing error amplifier.
12	FEO	Analog Output	Focusing error output.
13	FEP	Analog Input	Positive input of focusing error amplifier.
14	TEN	Analog Input	Negative input of tracking error amplifier.
15	TEO	Analog Output	Tracking error output.
16	SBAD	Analog Output	Sub beam adder signal output.
17	CSO	Analog Output	Central Servo control output.
19	RFON	Analog Output	Negative RF output.
20	RFOP	Analog Output	Positive RF output.
206	OSN	Analog Output	RF offset loop integrating capacitor connecting
205	OSP	Analog Output	RF offset loop integrating capacitor connecting
APC Interface			
10	LDO	Analog Output	Laser diode control output.
207	MDI	Analog Input	Voltage for monitoring the laser diode photo power.
21	TMA	Analog Input	Pin for laser power triming.
23	TMB	Analog Input	Pin for laser power triming.
18	TAVSS	Ground	Ground pin .
22	TAVDD	Analog Power(3.3V)	Power for trimming pads and related analog circuitry.
REF Interface			
203	V20	Analog output	2.0 V reference voltage output
202	V13	Analog output	1.3 V reference voltage output
201	V26	Analog output	2.6 V reference voltage output

Data Slicer & Data PLL Interface			
194	PLLVSS	Ground	Ground pin for data PLL and related analog circuitry.
189	SPDOP	Analog Output	Vco dac positive output.
190	SPDON	Analog Output	Vco dac negative output.
191	LPFON	Analog Output	The negative output of loop filter amplifier.
192	LPFOP	Analog Output	The positive output of loop filter amplifier.
193	LPFN	Analog Input	The negative input terminal of loop filter amplifier.
195	IREF	Analog Input	Current reference input. It generates reference current for data PLL. Connect an external 15K resistor between this pin and PLLVSS.
188,196	PLLVDD	Analog Power(3.3V)	Power for data PLL and related analog circuitry.
197	VOSPI	Analog Input	Positive input for analog slicer
198	VOSNI	Analog Input	Negative input for analog slicer
199	VOSP	Analog Output	Positive low pass filter output for analog slicer
200	VOSN	Analog Output	Negative low pass filter output for analog slicer
Turbo 8032 Interface			
27	URD_/IO4	TTL Input 50K pull_up	Read signal input from ICE to MT1199, active low. Alternate function : Programmable GPIO.
28	UP3_5/UT1	TTL I/O, Slew rate 50K pull_up	Programmable bi-directional I/O. Alternate function : T1. Timer 1 input.
29	UP3_4/UT0	TTL I/O, Slew rate 50K pull_up	Programmable bi-directional I/O. Alternate function : T0. Timer 0 input.
30	DGND	Ground	Ground pin for internal digital circuitry.
31	UINT1_/IO5	TTL Output	Host interrupt output, connected to INT1_ pin of ICE, low active. Alternate function : Programmable GPIO.
32	UP3_2 / UINT0_	TTL I/O, Slew rate 50K pull_up	Programmable bi-directional I/O. Alternate function : INT0_. External interrupt 0, low active.
33	UP3_1 / UTXD	TTL I/O, Slew rate 50K pull_up	Programmable bi-directional I/O. Alternate function : TXD. Serial transmit data.
34	UP3_0 / URXD	TTL I/O, Slew rate 50K pull_up	Programmable bi-directional I/O. Alternate function : RXD. Serial receive data.
35	DVDD	Power(5V)	Power pin for internal digital circuitry.
40	ICEMODE	TTL Input 50K pull_down	Internal or external P select. “1” indicates disable internal P and external P is used.
41	UWR_/IO6	TTL I/O, Slew rate SMT, 50K pull_up	WR_. Data write signal. Alternate function : Programmable GPIO.
42	UALE / O8	TTL I/O 50K pull_up	Address latch enable output, active high. Alternate function : Programmable output

43	UP1_0 / UA16	TTL I/O, Slew rate 50K pull_up	Programmable bi-directional I/O. Alternate function : A16. Address bit 16 output. Input 3.3V/5V tolerance, output 3.3V
44,45,46,47, 48,49,51,52	UP2_[7:0] / UA[15:8]	TTL I/O, Slew rate 50K pull_up	Programmable bi-directional I/O. Alternate function : A[15:8]. Upper address bus input/output. Input 3.3V/5V tolerance, output 3.3V
50	UPSEN_ / O9	TTL I/O 50K pull_up	Programmable store enable output, active low. PSEN_ enables the external ROM output port. Alternate function : Programmable output. Input 3.3V/5V tolerance, output 3.3V
53	DVDD3	Power(3.3V)	3.3V power pin for digital circuitry.
56	DGND	Ground	Ground pin for digital circuitry.
57	FWR_	TTL Output	output 3.3V, flash write enable.
59	DVDD3	Power(3.3V)	3.3V power pin for digital circuitry.
60,61,62,63, 64,65,66,67	UP0_[7:0] / UAD[7:0]	TTL I/O, Slew rate	Programmable bi-directional I/O. Alternate function : AD[7:0]. Lower address/data bus output for external device. Input 3.3V/5V tolerance, output 3.3V
68	DGND	Ground	Ground pin for digital circuitry.
69	UXI/O19	TTL Output Slew rate	P clock output for external system clock, connected to X1 of ICE. output 3.3V
70,71,72,73, 74,75,76,77	UA[7:0] / O[17 :10]	TTL Oouput, Slew rate	Lower address bus output for external device. Alternate function : Programmable output. output 3.3V
Xtal Interface			
54	XTALI	Input	Xtal input. The working frequency is 33.8688 MHz.
55	XTALO	Output	Xtal output.
DRAM Interface			
78,80,82,84, 86,88,90,92	RD[15:8] / VIO[15:8]	TTL I/O, Slew rate 50K pull_up	Buffer RAM Data / Versatile Input/Output. These pins are the bi-directional upper Buffer RAM data bus to the external buffer memory. When an 8-bit DRAM is used, the RD8–RD15 signals becomes Versatile I/O pins, VIO8–VIO15. Input 3.3V/5V tolerance, output 3.3V
79,81,83,85, 87,89,91,93	RD[7:0]	TTL I/O, Slew rate 50K pull_up	Bi-directional lower Buffer RAM data bus. Input 3.3V/5V tolerance, output 3.3V
94	CASL_ / CAS_	TTL Output Slew rate	Column Address Strobe Low / Column Address Strobe. When TWE63h.RW6 is 0, this pin is the Column Address Strobe Low signal for accessing the lower bytes of a two-CAS_ 16-bit DRAM. When TWE63h.RW6 is 1 or when an 8-bit DRAM is used, this pin shall be connected to CAS_ of the DRAM. output 3.3V

95	CASH_ / RWEH_	TTL Output Slew rate	Column Address Strobe High / RAM Write Enable High. When a 16-bit DRAM is used, this pin functions as Column address Strobe High for accessing the upper bytes of a two-CAS_ DRAM if TWE63h.RW6 is 0, or as Write Enable High for writing the upper bytes of a two-WE_ DRAM. output 3.3V
96	RWE_ / RWEL_	TTL Output	RAM Write Enable / RAM Write Enable Low. When TWE63h.RW6 is 0 or when an 8-bit DRAM is used, this pin is the active-low write strobe to the external buffer DRAM. When TWE63h.RW6 is 1, this pin is the Write Enable Low signal for writing the lower bytes of a two-WE_ 16-bit DRAM. output 3.3V
97	RAS_	TTL Output Slew rate	Row Address Strobe. This output is the Row Address Strobe signal to the buffer DRAM. output 3.3V
98	DVDD3	Power(3.3V)	3.3V power pin for digital circuitry.
99~103 105~108	RA[8:0]	TTL I/O, Slew rate 50K pull_down	Buffer RAM Address. These pins are the address bus to the external buffer DRAM. output 3.3V
104	DGND	Ground	Ground pin for internal digital circuitry.
Audio Interface			
117	ADGO / VIO0	TTL I/O, Slew rate SMT, 50K pull_up	Digital Audio Output / Versatile I/O 0. The signal is either the Digital Audio Output which supplies the IEC-958 digital audio data when A0SEL00h.RW7=1 and ADOE2Eh.RW0=1, or the Versatile I/O 0 pin otherwise.
Internal Audio DAC Interface			
109	DACVSS	Ground	Ground pin for internal DAC circuitry.
110	RO	Analog Output	Right channel of audio.
111	DACVREF	Analog Output	Reference voltage for external audio filter circuit.
112	LO	Analog Output	Left channel of audio.
113	DACVDD	Analog Power(3.3V)	Power pin for internal DAC circuitry.
Varipitch VCO Interface			
114	VPVDD	Analog power(3.3V)	Power pin for varipitch VCO circuitry.
115	VCOCIN	Analog Input	Connect capacitor for compensator loop filter.
116	VPVSS	Ground	Ground pin for varipitch VCO circuitry.
Host Interface			
118	DEVSEL	TTL Input 50K pull_up	Device Select. Cleared to zero indicates the MT1199 is master device. Set to one indicates the MT1199 is slave device.
119	DASP_	TTL I/O 50K pull_up	Device Active / Device 1 Present. This is a time-multiplexed signal which indicates that a device is active, or that Device 1 is present. A 10K-ohm pull-up resistor shall be connected to this signal externally.

120	CS3FX_	TTL Input, SMT 50K pull_up	Device Chip Select 1. This is the chip select signal from the host to select the Control Block Registers.
121	CS1FX_	TTL Input, SMT 50K pull_up	Device Chip Select 0. This is the chip select signal from the host to select the Command Block Registers.
122	DGND	Ground	Ground pin for internal digital circuitry.
123,127,124	DA[2:0]	TTL Input, SMT 50K pull_up	Device Address. This is the 3-bit binary coded address provided by the host to access an ATA register or data.
125	DVDD3	Power(3.3V)	3.3V power pin for digital circuitry.
126	PDIAG_	TTL Input, 50K pull_up	Passed Diagnostics. This signal is asserted by Device 1 to indicate to Device 0 that it has completed diagnostics.
128	DVDD	Power(5V)	Power pin for internal digital circuitry.
129	IOCS16_	TTL Output Open drain	Device 16-BIT I/O. In PIO transfer modes 0, 1, and 2, IOCS16_ indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word. The MT1199 will always assert IOCS16_ when the host reads the ATAPI Data Register.
130	INTRQ	TTL I/O Slew rate	Device Interrupt. This signal is used to interrupt the host system. INTRQ is driven only when the MT1199 is addressed, i.e., DRV101h.RW7=DRV16h.RW4. When not driven, INTRQ is in a high impedance state.
131	DMACK_	TTL Input, SMT 50K pull_up	DMA Acknowledge. This signal shall be used by the host in response to DMARQ to acknowledge that it is ready for DMA transfers.
132	IORDY	TTL Outout Slew rate	I/O Channel Ready. This signal is negated (pulled low) during PIO to extend the host transfer cycle of any host register access (Read or Write) when the MT1199 is not ready to respond to a data transfer request. When IORDY is not negated, it is in a high impedance state. In Ultra DMA transfers, the signal becomes either DDMARDY_ (Device Ultra DMA Ready) that is asserted by the MT1199 to indicate to the host that it is ready to receive data, or DSTROBE (Device Ultra DMA Data Strobe) whose rising edge and falling edge latch the data from DD0–DD15 into the host.
133	DIOR_	TTL Input, SMT 50K pull_up	Device I/O Read. This is the ATA read strobe signal. In PIO or multiword-DMA the falling edge of DIOR_ enables data from the MT1199 onto the host data bus, DD0–DD7 or DD0–DD15. The rising edge of DIOR_ then latches the data at the host. During Ultra DMA transfers the signal becomes either HDMARDY_ (Host Ultra DMA Ready), which is asserted by the host to indicate to the MT1199 that the host is ready to receive data, or HSTROBE (Host Ultra DMA Data Strobe), whose rising edge and falling edge latch the data from DD0–DD15 into the MT1199.
134	DIOW_	TTL Input, SMT 50K pull_up	Device I/O Write. This is the ATA write strobe signal. In PIO or multiword-DMA the rising edge of DIOW_ latches data from the host data bus, DD0–DD7 or DD0–DD15, into the ATA registers or the ATAPI Packet FIFO of the MT1199. In Ultra DMA transfers the signal becomes STOP (Stop Ultra DMA Data Transfer), which is negated by the host before data can be transferred by an Ultra DMA burst, and asserted by the host when it want to terminate an Ultra DMA burst.
135	DMARQ	TTL Output	DMA Request. This signal, used for DMA data transfer, is asserted by the MT1199 when it is ready to transfer data to or from the host.

136~137 139~143 145~148 150~152 154~155	DD[15:0]	TTL I/O pull_up / pull_down	Device Data. This is the 8-bit or 16-bit bi-directional data bus to the host. The lower 8 bits, DD0—DD7, are used for 8-bit data transfers. Note : All pins except DD7 may be selectively pull up/down with 20k resistant.
138	DGND	Ground	Ground pin for digital circuitry.
144	DGND	Ground	Ground pin for digital circuitry.
149	DVDD	Power(5V)	Power pin for digital circuitry.
153	DGND	Ground	Ground pin for digital circuitry.
Reset Interface			
158	HRST_	TTL Input, SMT	Host reset input. The active low input is used to reset MT1199.
166	RESET/O18	TTL Output	Reset signal output(combine HRST_ & POR), active high. Alternate function : Programmable output.
167	POR	TTL Input, SMT	Power on reset input, active high.
IPLL VCO Interface			
156	IPLLVDD	Analog power(3.3V)	Power pin for IPLL VCO circuitry.
157	IPLLVSS	Ground	Ground pin for IPLL VCO circuitry.
Extended GPIO Interface			
24,25,26	IO[3:1]	TTL I/O, Slew rate 50K pull_up	Programmable GPIO.
58	IO7/CS_	TTL I/O 50K pull_up	Programmable GPIO. Alternate function : Chip select signal for flash ROM selection, active low.
165	IO0	TTL I/O 50K pull_down	Programmable bi-directional I/O. Alternate function : Serial bus reserved for MT1136.
Mega Interface			
37	LED	TTL Output	LED control output. Controlled by P.
38	EJECT_	TTL input	Eject/stop key input, active low.
39	PLAY_	TTL input	Play/pause key input, active low.
159	TRAYIN_	TTL input	Tray_is_in input, A logical low indicates the tray is in. Feedback flag from tray connector.
160	TRAYOUT_	TTL input	Tray_is_out input. A logical low indicates the tray is out. Feedback flag from tray connector.
161	TROPEN	TTL output	Tray open output. Controlled by P.
162	TRCLOSE	TTL output	Tray close output. Controlled by P.
163	LIMIT_	TTL input	Sledge inner limit input, active low.
164	DVDD3	Power(3.3V)	Power pin for internal digital circuitry.

Motor and Actuator Driver Interface			
168	FG	TTL Input, SMT 50K pull-up	Motor Hall sensor input.
169	DVDD	Power(5V)	Power pin for internal digital circuitry.
170	ENDM	TTL Output	Enable/disable disk motor. A logical high enables disk motor.
171	DGND	Ground	Ground pin for internal digital circuitry.
172	HRFZC	Digital Input	High speed mirror signal input
173	FMO2	Analog Output	Feed motor control. PWM output.
174	FMO	Analog Output	Feed motor control. PWM output.
175	DMO	Analog Output	Disk motor control output. PWM output.
176	DVDD3	Power(3.3V)	Power pin for digital circuitry.
177	TEBC	Analog Output	Tracking error balance control. PWM output.
178	DGND	Ground	Ground pin for digital circuitry.
179	PDMVSS	Ground	Ground for PDM circuitry.
180	TRO	Analog Output	Tracking servo output. PDM output of tracking servo compensator.
181	FOO	Analog Output	Focus servo output. PDM output of focus servo compensator.
182	PDMVDD	Analog Power(3.3V)	Power for PDM circuitry.
Signal Amplifier Interface			
183	TEZILP	Analog Input	Tracking error zero crossing low pass input.
184	ADCVSS	Ground	Ground pin for ADC circuitry.
185	RFRPSLV	Analog Output	RF ripple slice level output.
186	RFRO	Analog Output	RF ripple detect output
187	ADCVDD	Analog Power(3.3V)	Power pin for ADC circuitry.
TEST mode			
36	TESTMODE	Digital Input	Enable test mode high active