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# MS-7392

Version: 1.2

## CPU:

**Intel Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.**

## System Chipset:

**Intel - MCH (North Bridge) P31/G31  
Intel ICH7 (South Bridge)**

## On Board Chipset:

**BIOS -- SPI EEPROM  
HD Codec -- ALC888  
LPC Super I/O -- F81182  
LAN-- REALTEK RTL8111C  
CLOCK -- ICS9LPRS906CGLF**

## Main Memory:

**DDR II \* 4 (Max 4GB)**

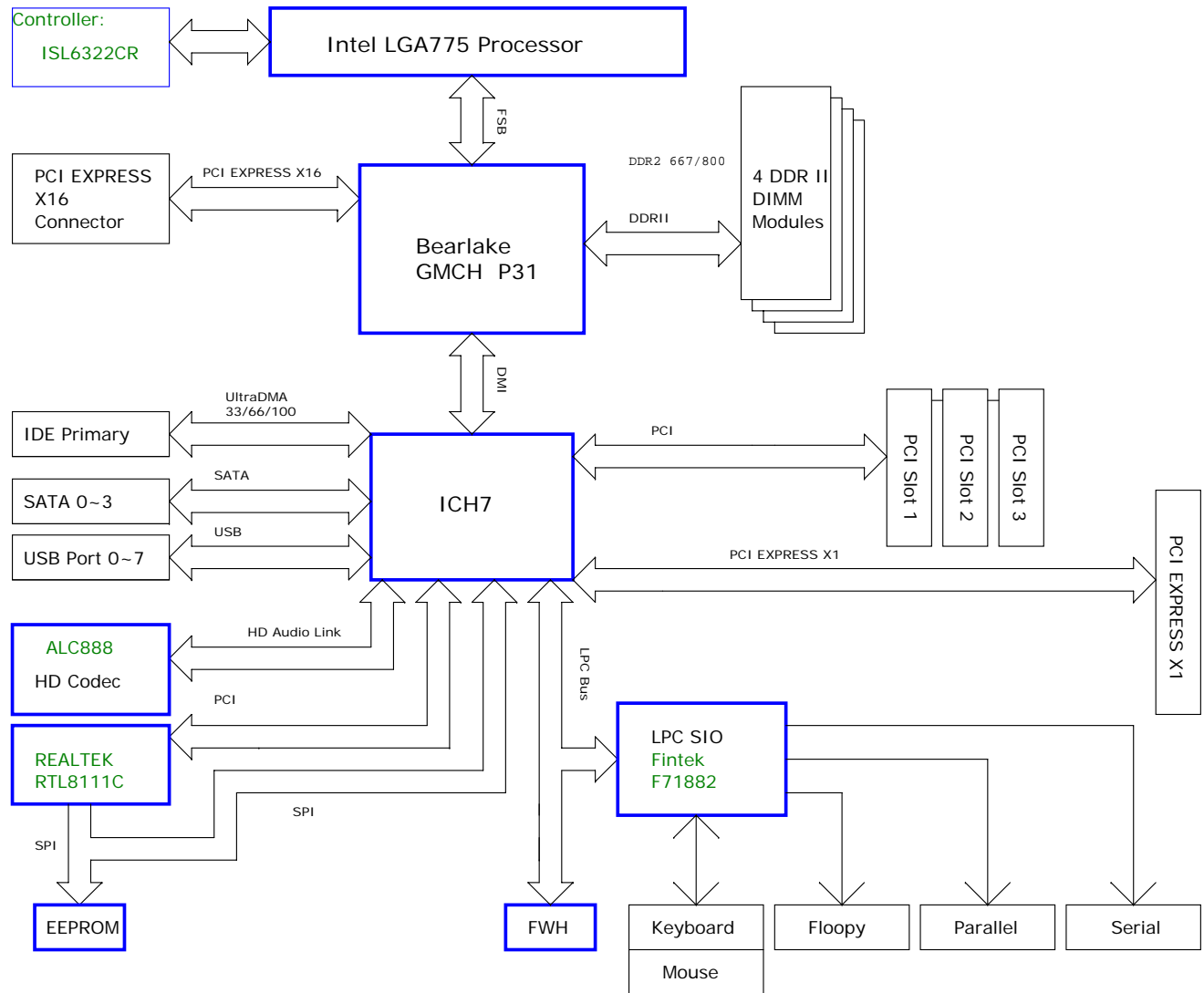
## Expansion Slots:

**PCI2.3 SLOT \* 3  
PCI EXPRESS X1 SLOT  
PCI EXPRESS X16 SLOT**

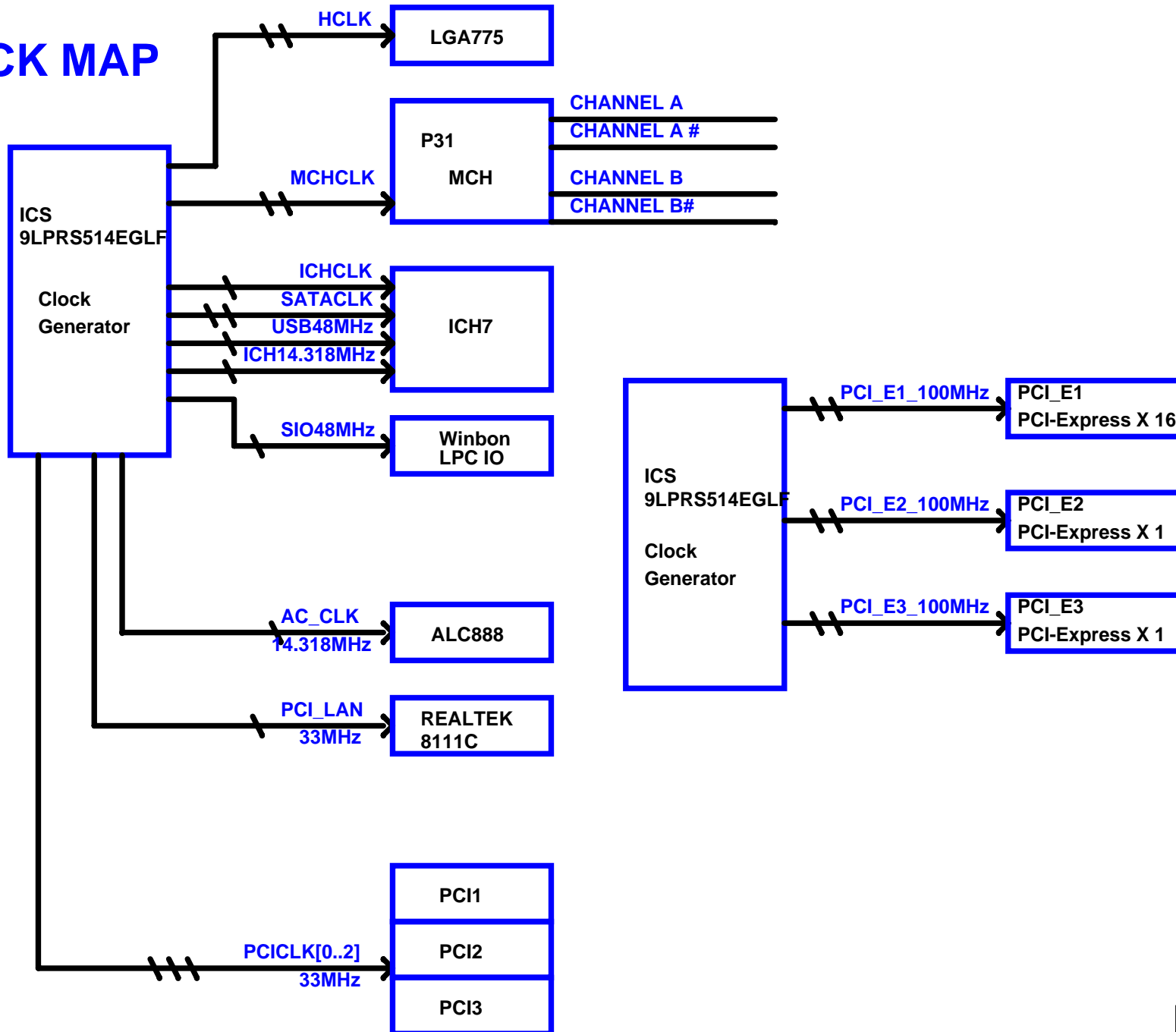
## INTELSIL PWM:

**Controller: INTELSIL - ISL6322CR**

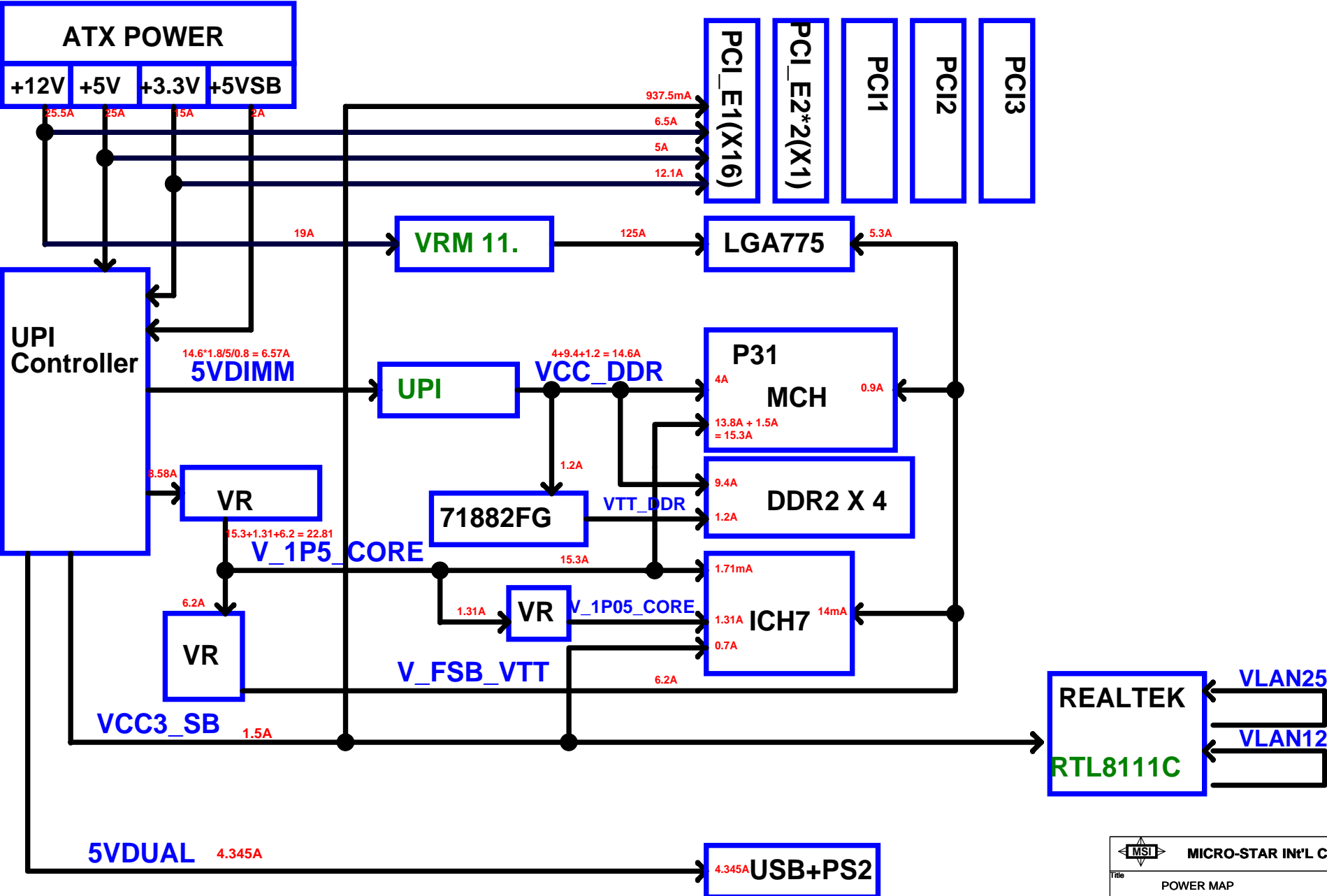
# Block Diagram



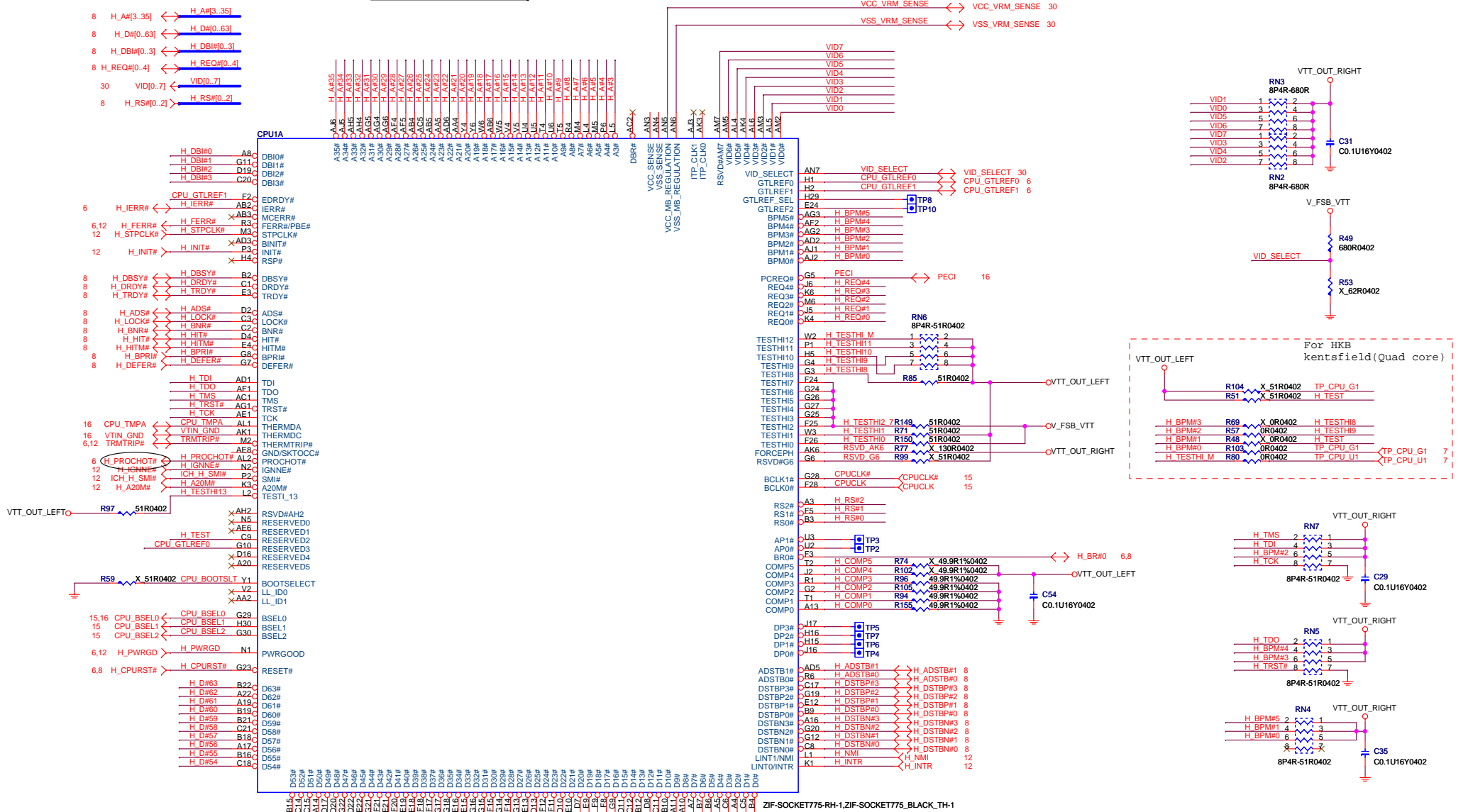
# CLOCK MAP



# POWER MAP



### CPU SIGNAL BLOCK



PLACE BPM/TCK/TDI/TMS TERMINATION NEAR CPU  
PLACE TDO TERMINATION NEAR CONNECTOR

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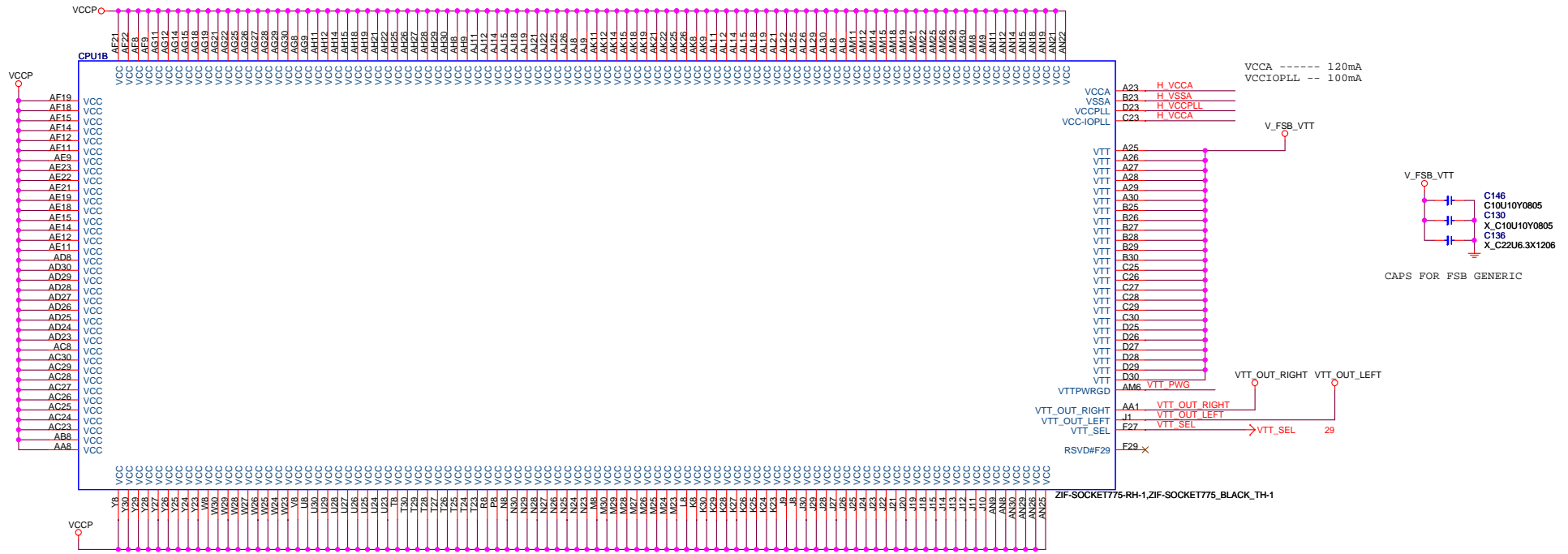
Title Intel LGA775 CPU - Signals

Size Document Number

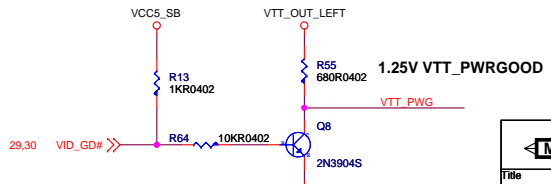
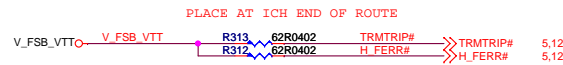
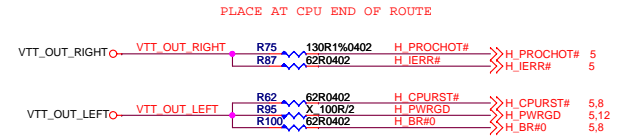
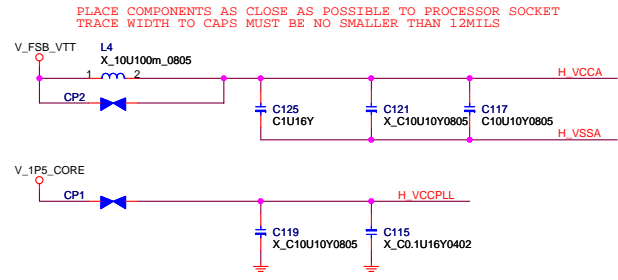
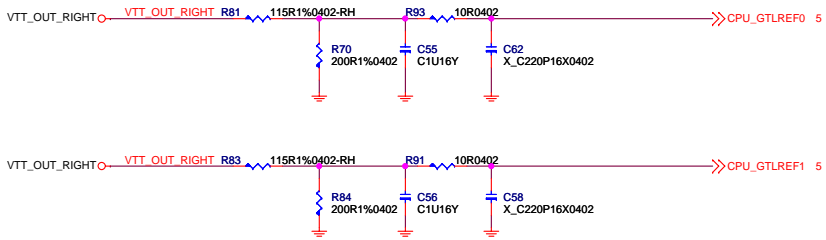
**MS-7392**

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1.2

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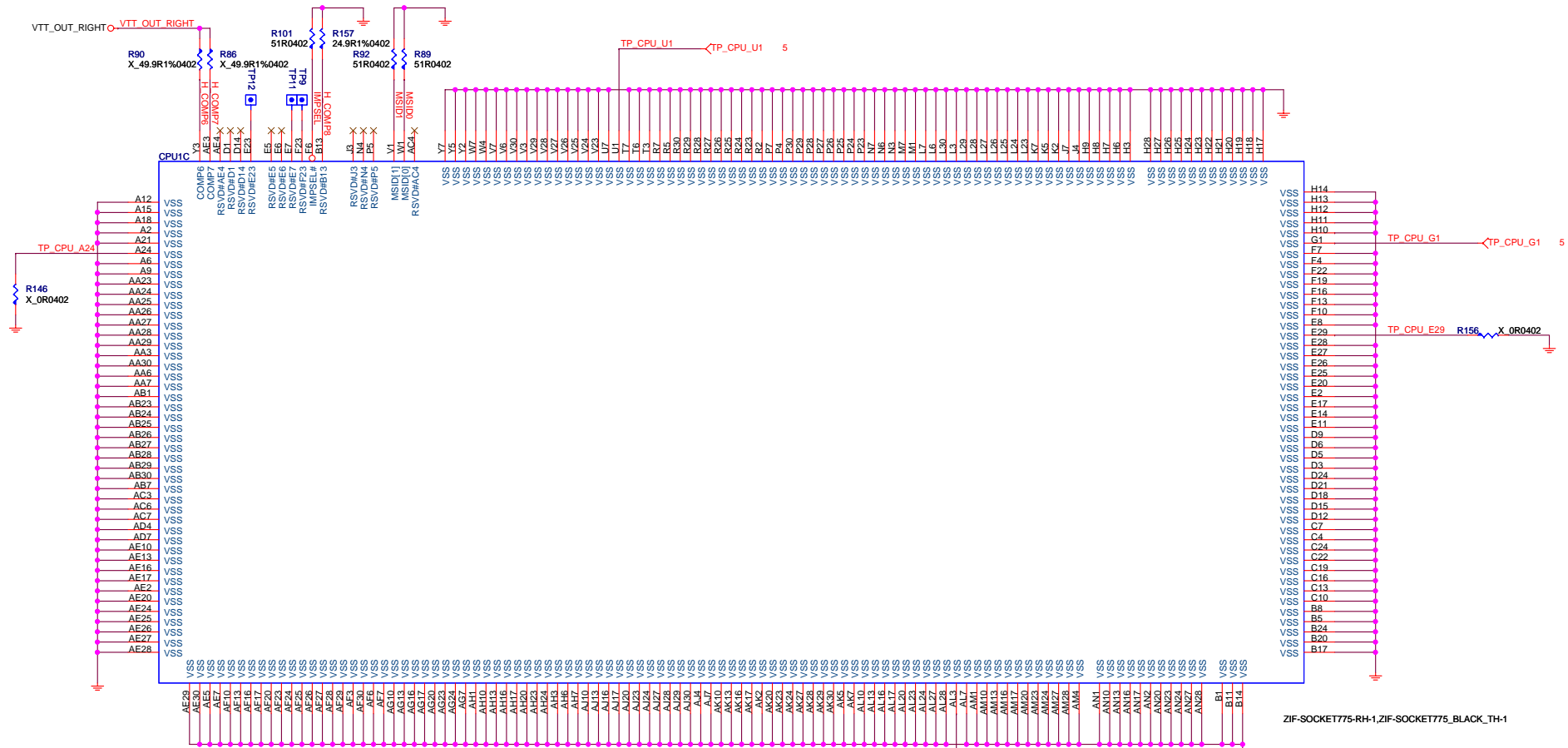
GTLRREF VOLTAGE SHOULD BE  $0.635 \cdot V_{TT}$   
 57.6ohm and 100ohm divider



VTT\_PWG SPEC :  
 High > 0.9v  
 Low < 0.3v  
 Trise < 150ns

<b>MSI</b>		
<b>MICRO-STAR INT'L CO., LTD.</b>		
Title Intel LGA775 CPU - Power		
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	2005 Performance PMB platform 1	2005 Mainstream/Value PMB platform 2	2006 65W PMB platform 3
MSID1	0	0	0
MSID0	0	NC	NC

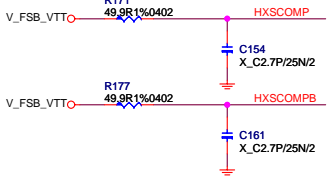
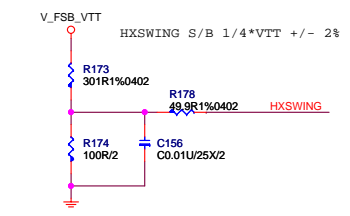
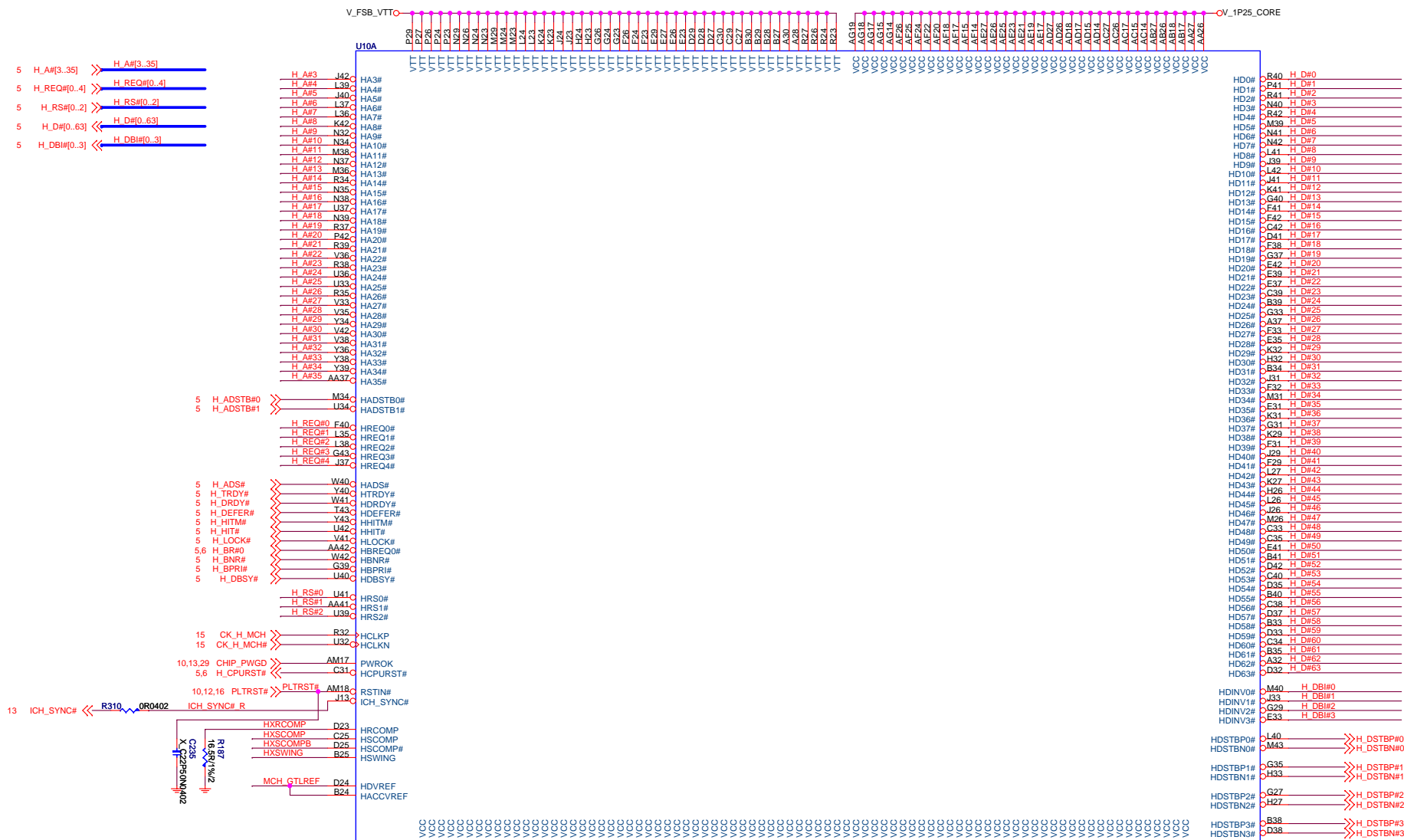


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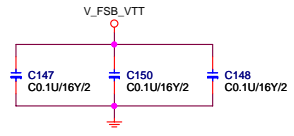
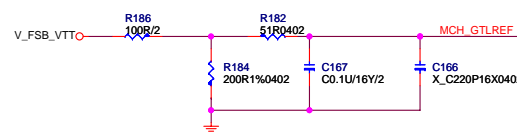
Title: Intel LGA775 CPU - GND

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GTLREF VOLTAGE SHOULD BE  $0.67 * V_{TT} = 0.804V$



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Title: Intel Bearlake G31 - CPU Signals

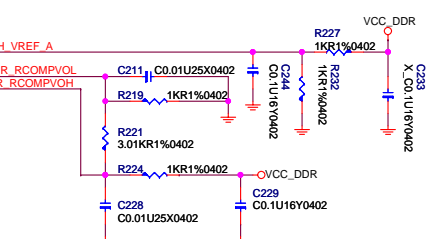
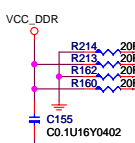
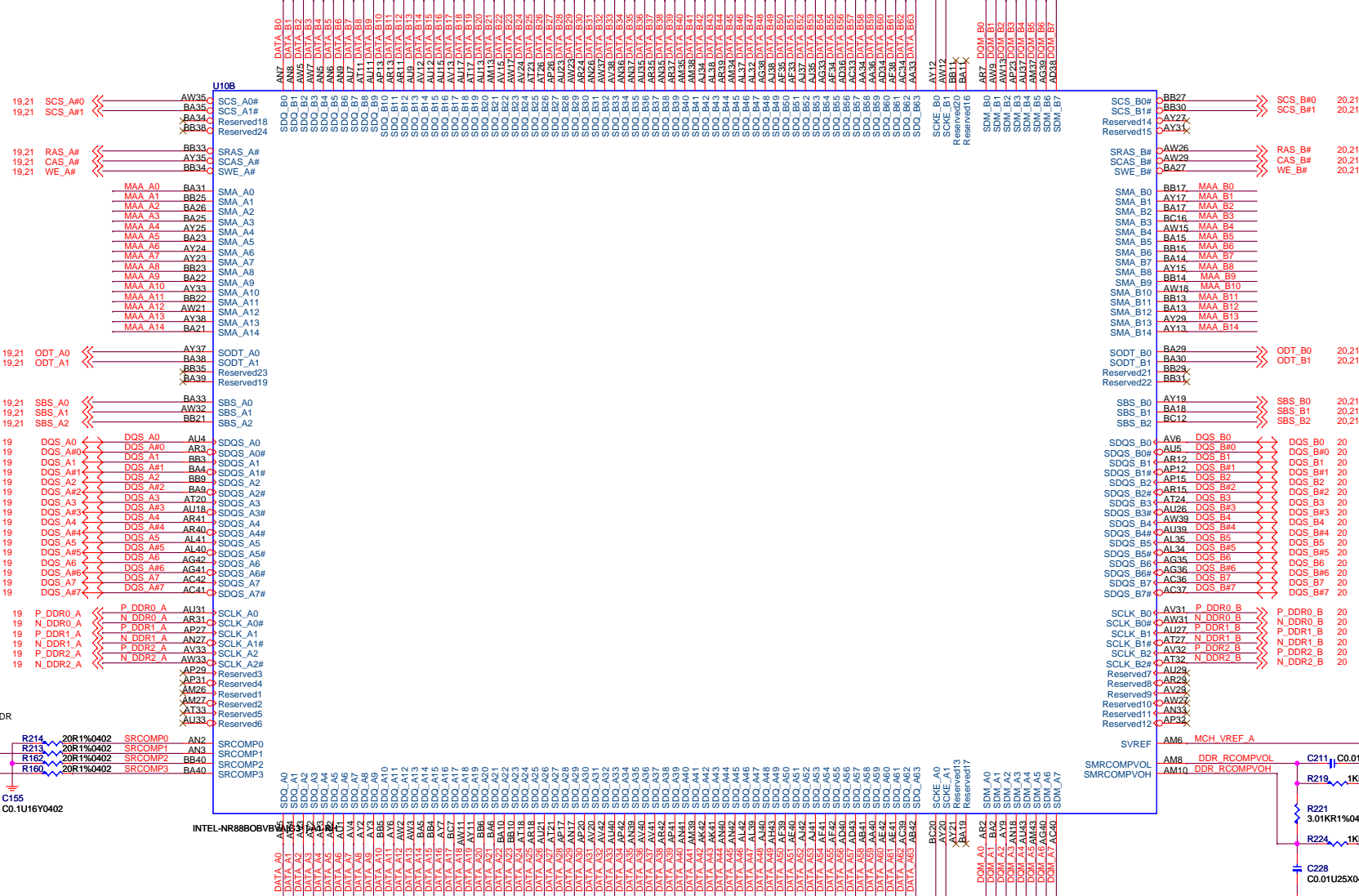
Size: Document Number: MS-7392

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DDR\_RCOMPVVOH = 0.8 \* VCC\_DDR  
 DDR\_RCOMPVOL = 0.2 \* VCC\_DDR

PLACE 0.1UF CAP CLOSE TO MCH

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Title: Intel Bearlake G31 - CPU Signals

Size: Document Number MS-7392 Rev 1.2

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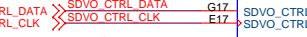
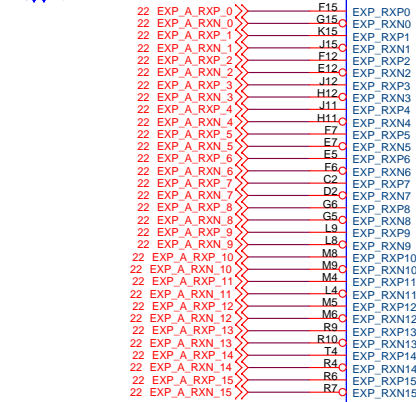
V\_1P25\_CORE

Close to MCH A.S.A.P

- R209 5.1KR0402 DMI\_MCH IT\_MR\_0\_DP
- R217 5.1KR0402 DMI\_MCH IT\_MR\_1\_DP
- R218 5.1KR0402 DMI\_MCH IT\_MR\_2\_DP
- R210 5.1KR0402 DMI\_MCH IT\_MR\_3\_DP

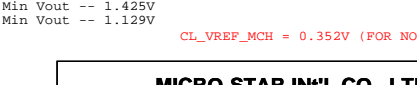
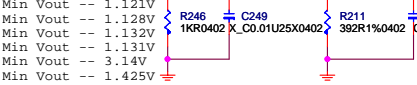
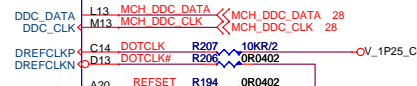
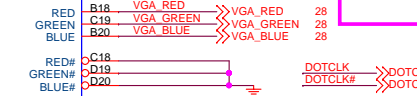
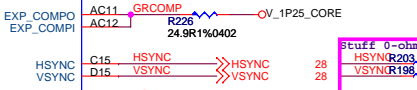
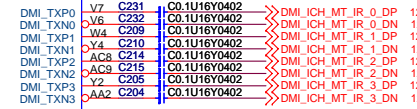
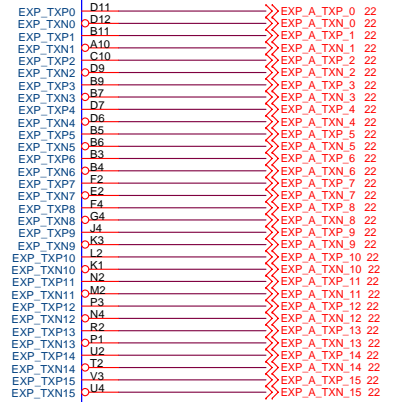
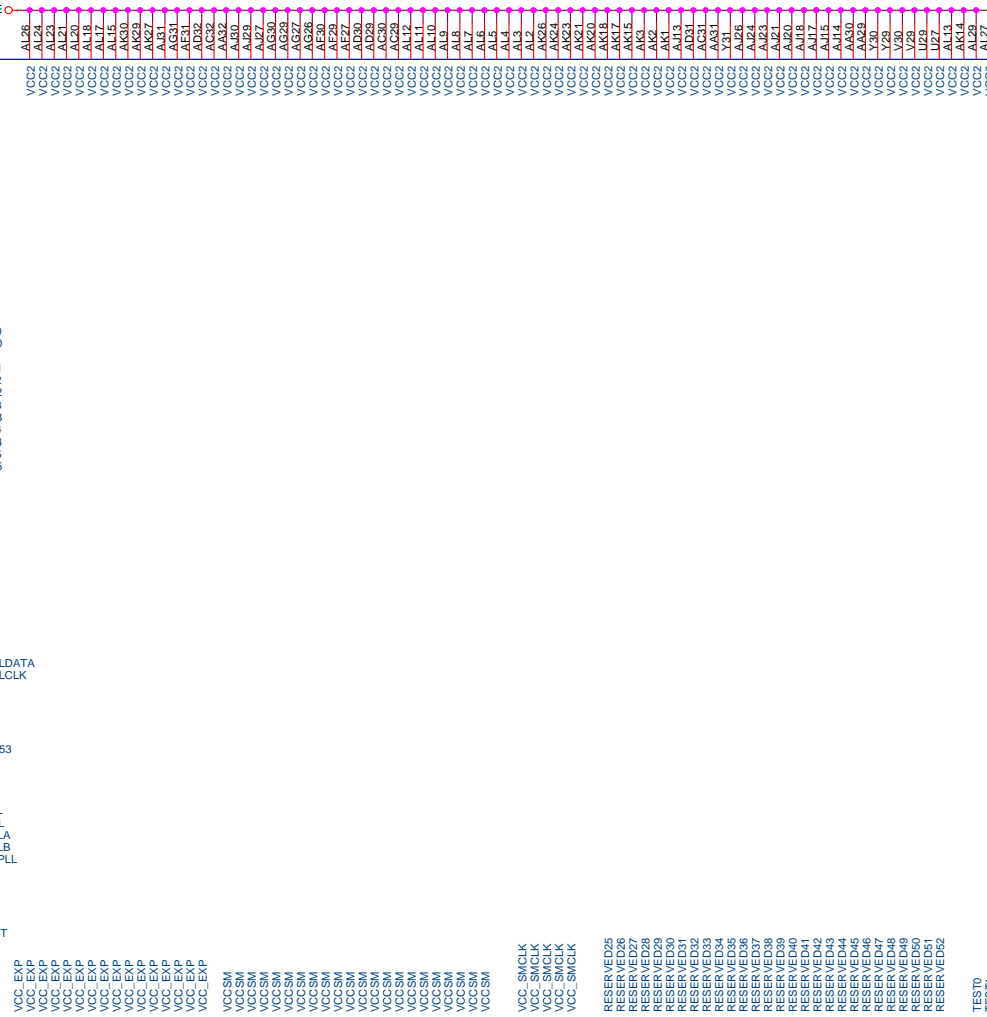
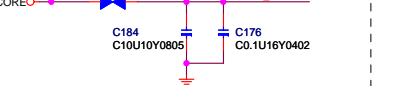
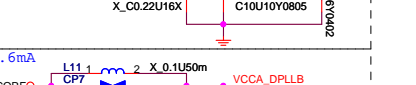
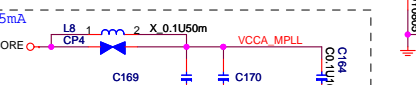
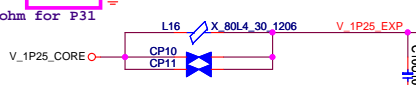
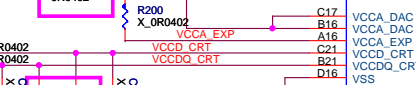
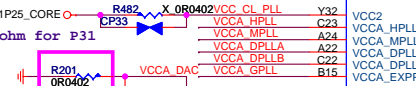
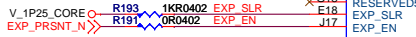
V\_1P25\_CORE

U10C



EXP\_SLR: PCI Express Static Lane Reversal

0: BTX 1: ATX



- VCC\_HPLL <<< 1.221V
- VCC\_MPLL <<< >130mA ; Min Vout <<< 1.128V
- VCC\_DPLLA <<< >80mA ; Min Vout <<< 1.132V
- VCC\_DPLLB <<< >80mA ; Min Vout <<< 1.131V
- VCC\_DAC <<< 70mA ; Min Vout <<< 3.14V
- VCCD\_CRT <<< 20mA ; Min Vout <<< 1.425V
- VCCDQ\_CRT <<< 0.5mA ; Min Vout <<< 1.425V
- VCCA\_EXPPLL <<< 50mA ; Min Vout <<< 1.129V
- VCC\_SMCLK <<< 250mA

CL\_VREF\_MCH = 0.352V (FOR NOW)

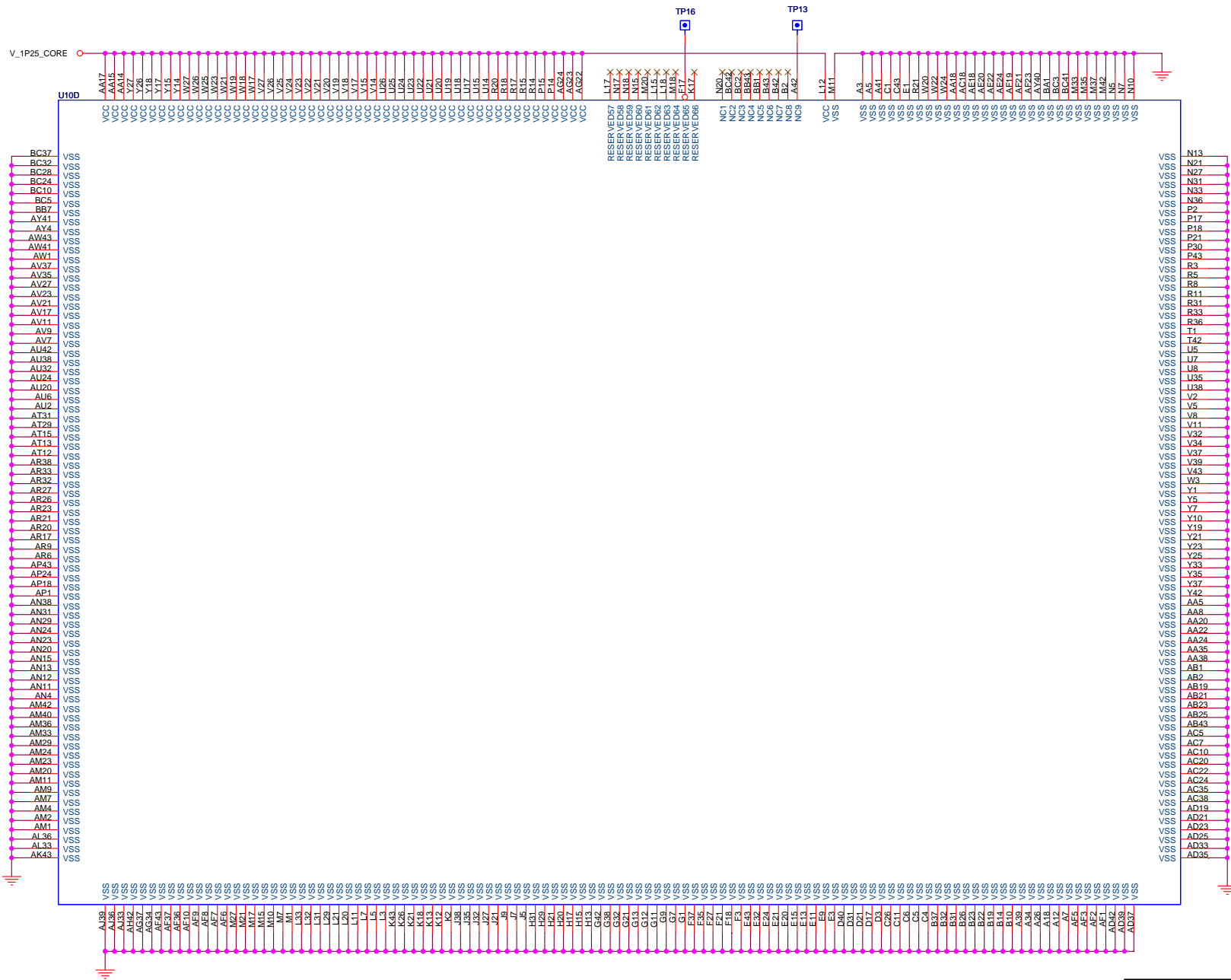
BSEL		TABLE	
2	1	0	PSB FREQUENCY
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

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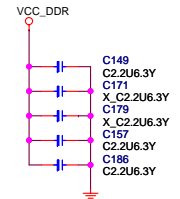
Title: Intel Bearlake G31 - CPU Signals

Size: Document Number: MS-7392 Rev: 1.2

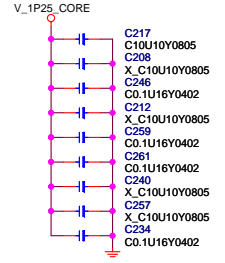
Date: Monday, May 12, 2008 Sheet: 10 of 35



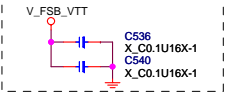
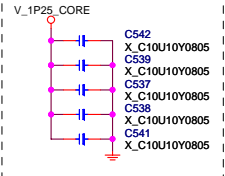
Place close to GMCH



MCH CORE DECOUPLING



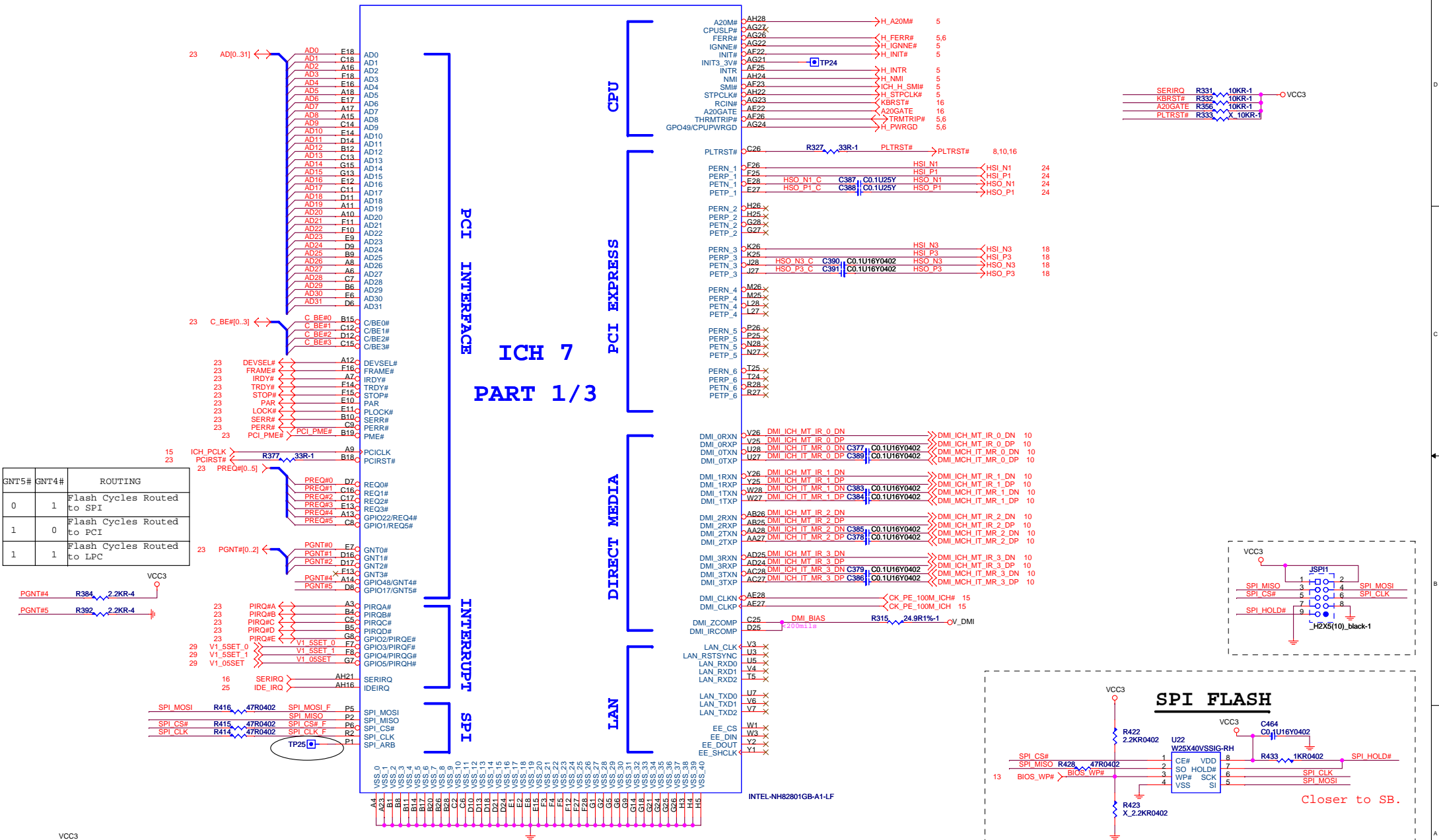
5020 Parts



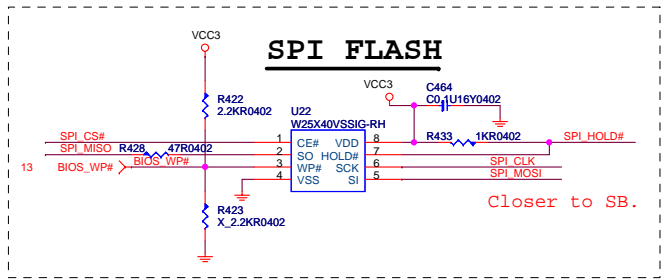
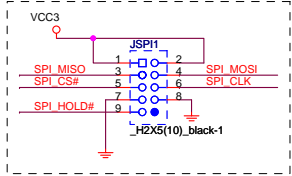
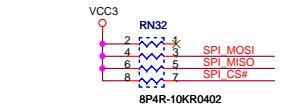
INTEL-NR88BOBVBVA[G31]-A1-RH

<b>MICRO-STAR INT'L CO., LTD.</b>		
Title <b>Intel Bearlake G31 - CPU Signals</b>		
Size	Document Number	Rev 1.2
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# ICH 7 PART 1/3



GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC

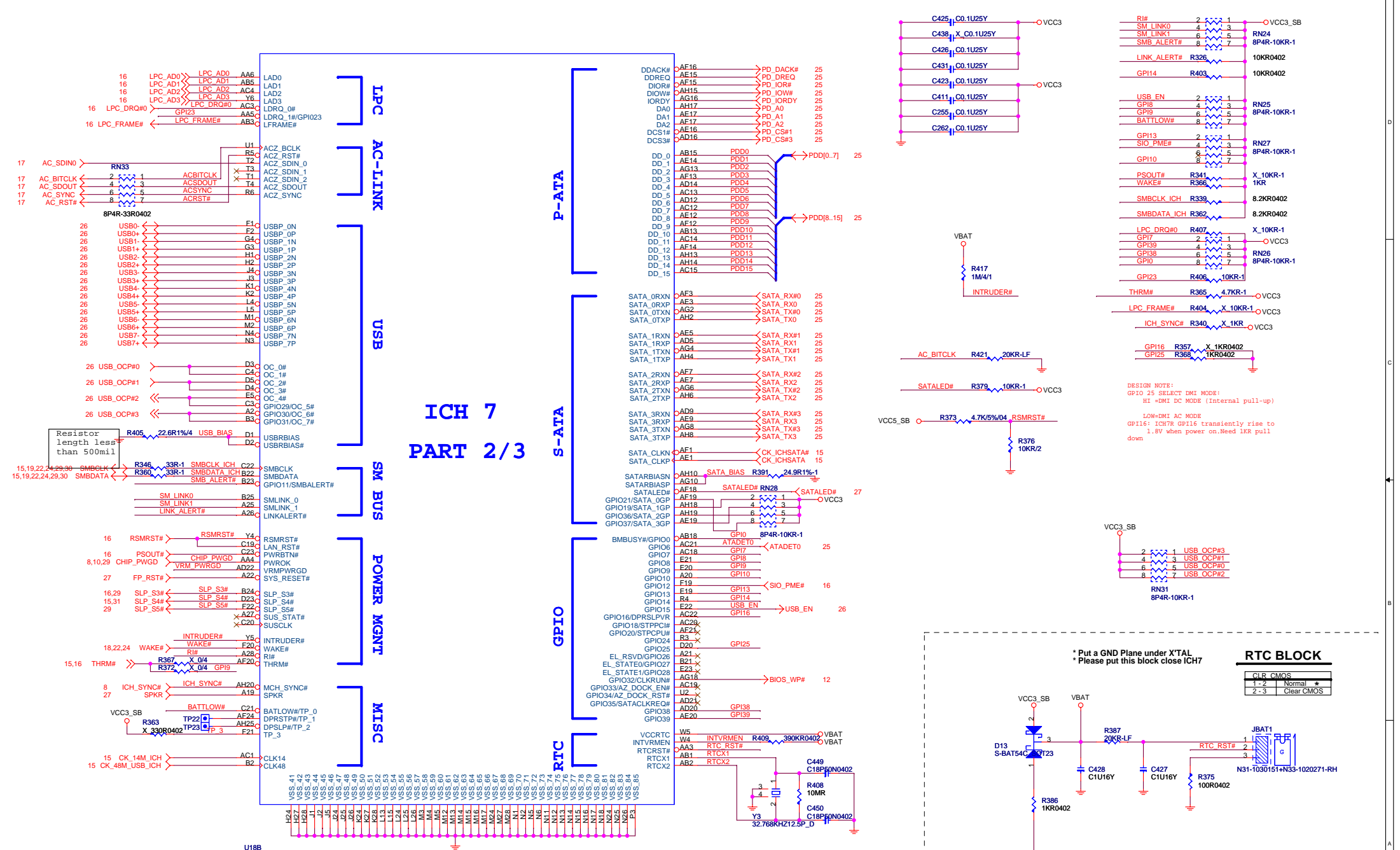


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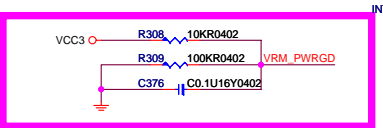
Title: Intel ICH7 - PCI & DMI & CPU & IRQ

Size: Document Number **MS-7392** Rev: 1.2

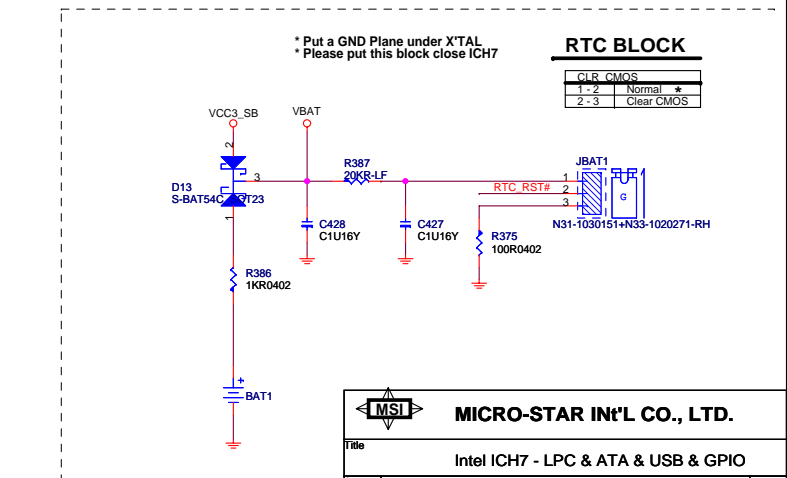
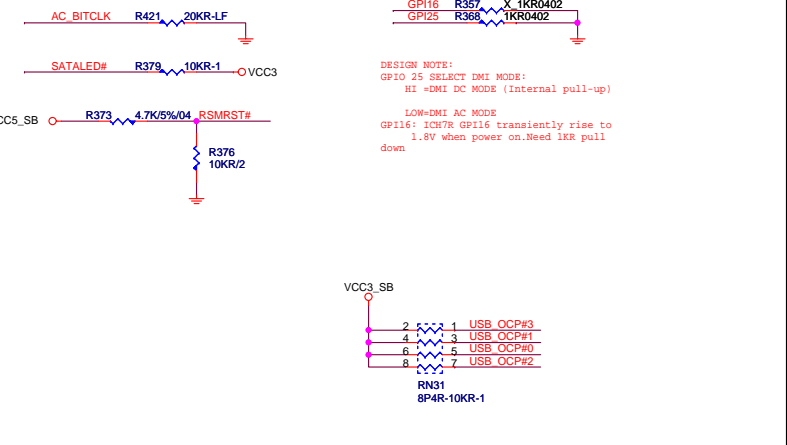
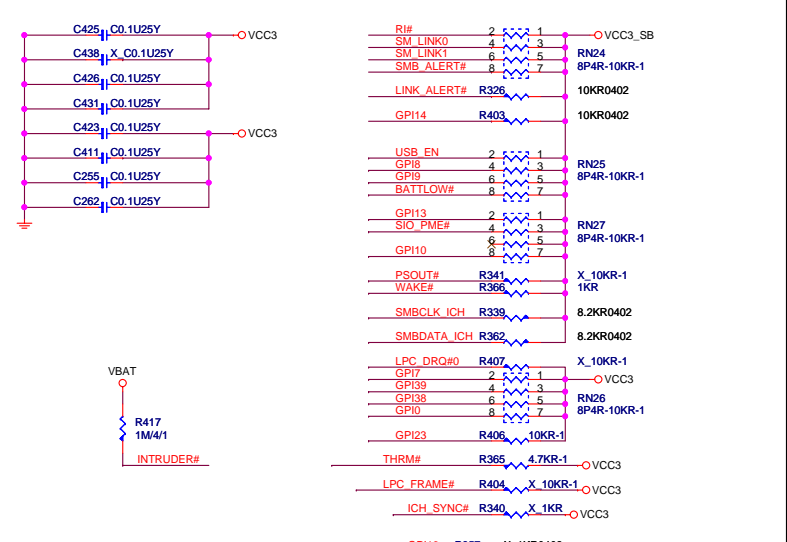
Date: Tuesday, May 06, 2008 Sheet: 12 of 35



# ICH 7 PART 2/3



Following are the GPIOs that need to be terminated properly if not used:  
 GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3\_3 if unused.  
 GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3\_3 if unused.

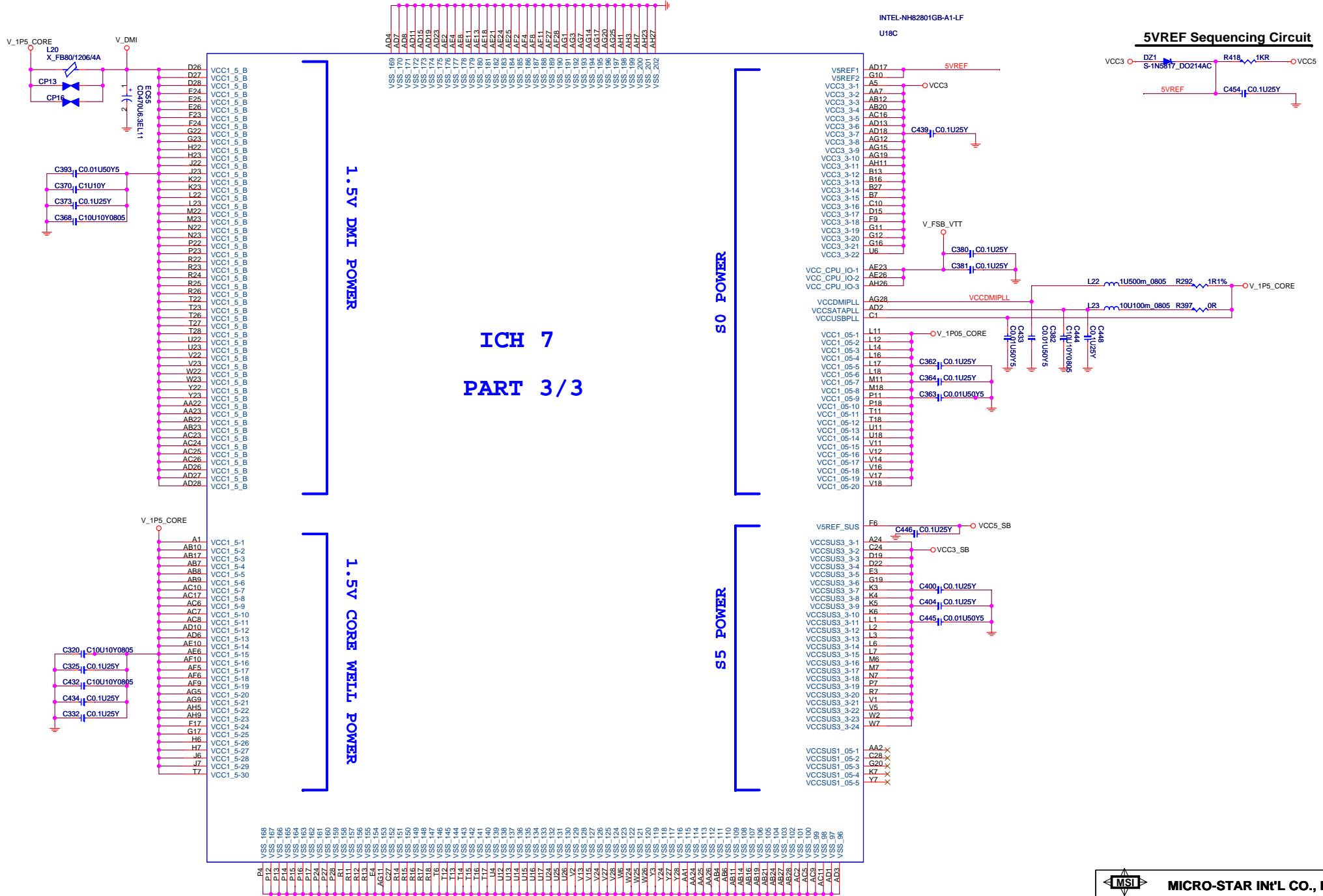


**MSI** MICRO-STAR INT'L CO., LTD.

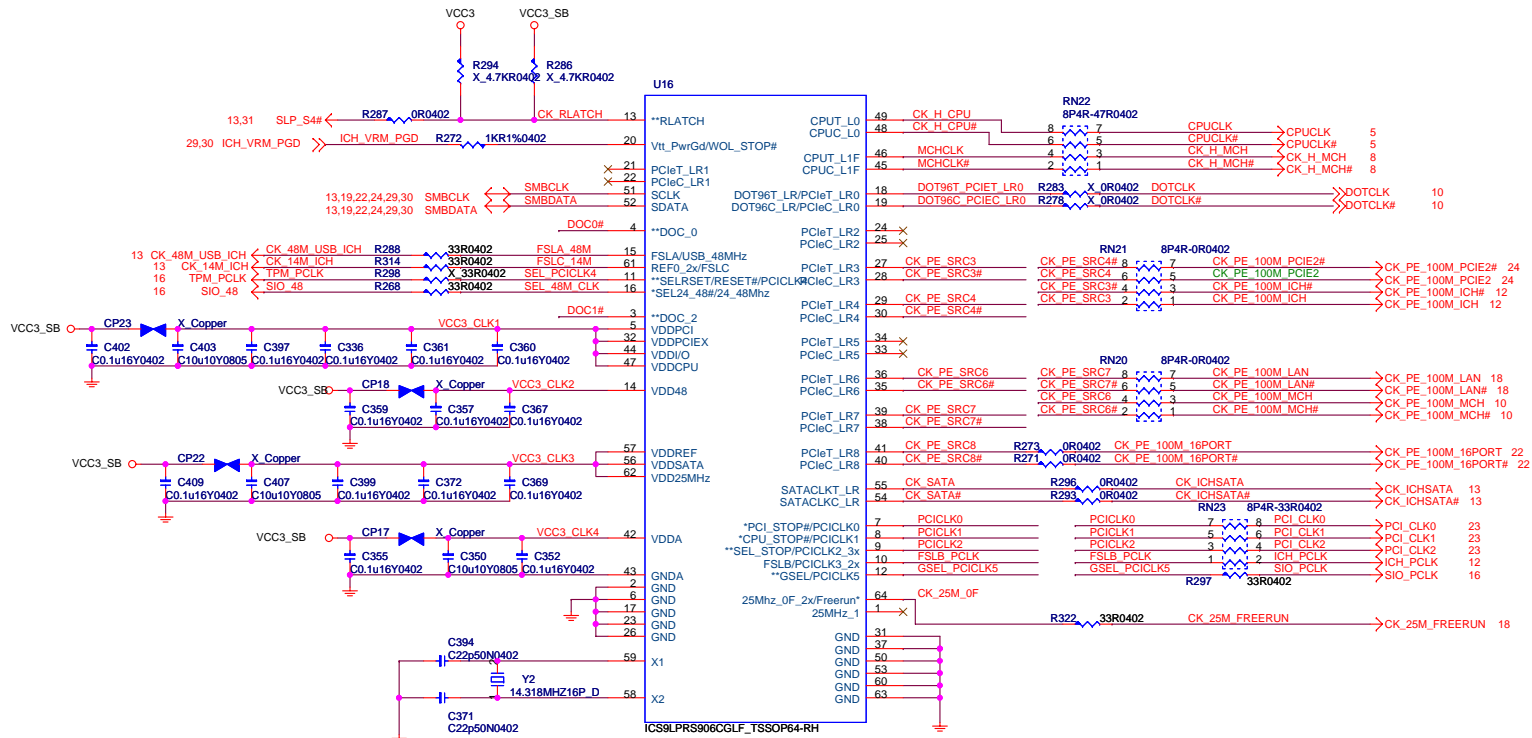
Title Intel ICH7 - LPC & ATA & USB & GPIO

Size Document Number MS-7392 Rev 1.2

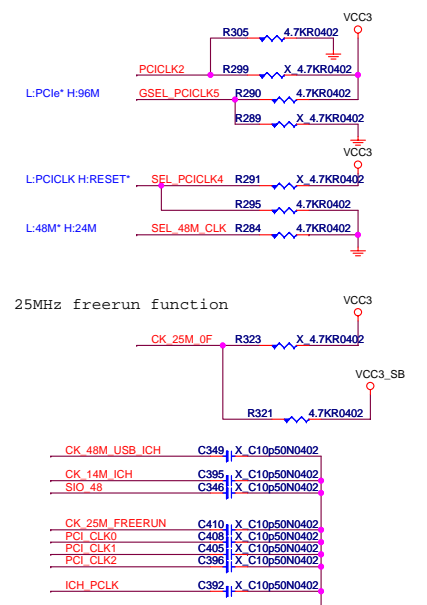
Date: Tuesday, May 06, 2008 Sheet 13 of 35



# Clock Generator - ICS9LPRS906CGLF



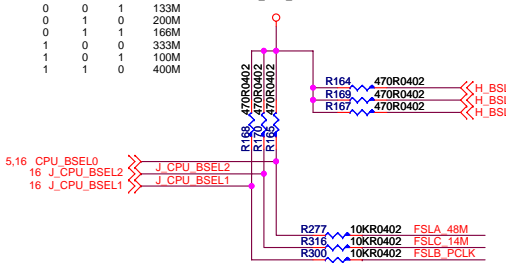
## CLOCK GEN STRAPING



## CPU Frequency Selection

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M

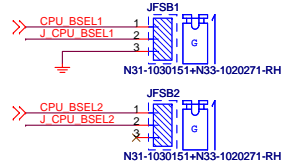
V\_FSB\_VTT



**JFSB1**  
 Plug 1--2  
 200MHZ-->200MHZ  
 Plug 2--3  
 200MHZ-->266MHZ

**JFSB2**  
 Plug 1--2  
 266MHZ-->266MHZ  
 Plug 2--3  
 266MHZ-->333MHZ

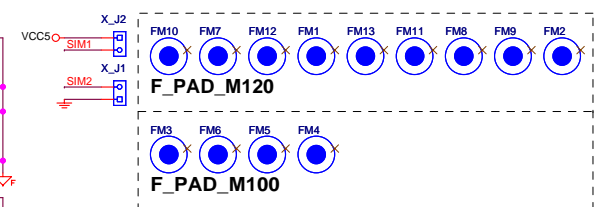
**JFSB1**  
 Open  
**JFSB2**  
 Plug 1--2 or 2--3 or Open  
 333MHZ-->400MHZ



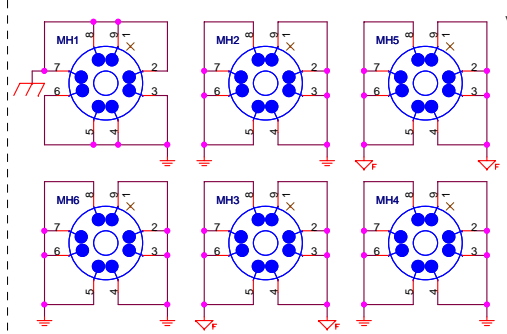
FSB	FS_C	FS_B	FS_A	CPU
800M	0	1	0	200M
1066M	0	0	0	266M
1333M	1	0	0	333M
1333M	1	0	0	400M

For 400MHz CPU Support

## Optics Orientation Holes



## Mounting Holes

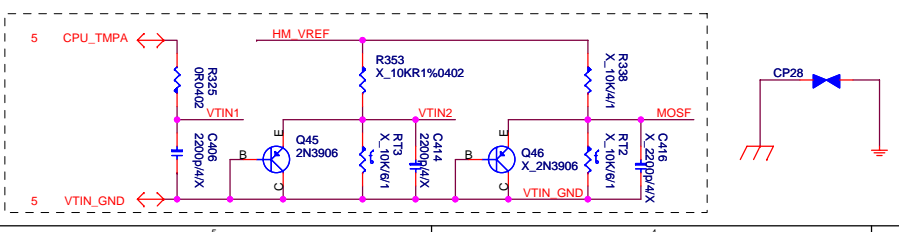
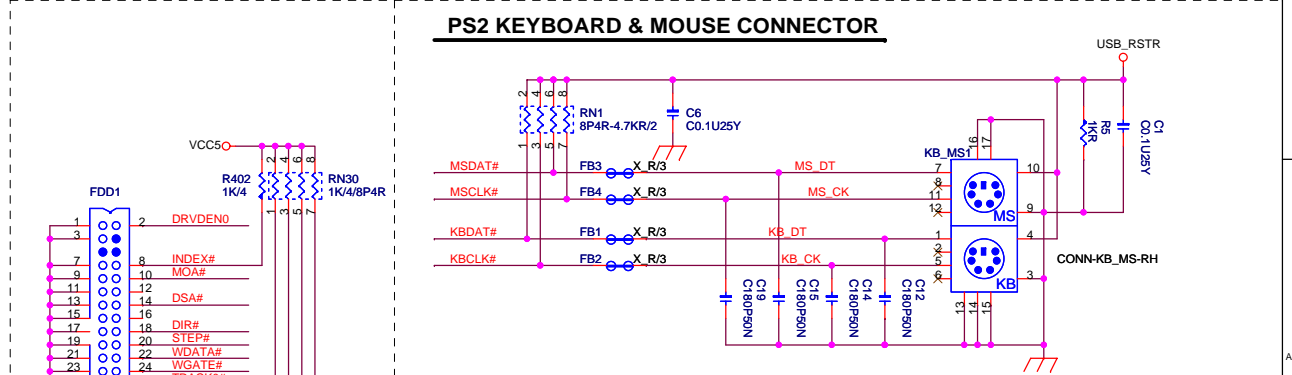
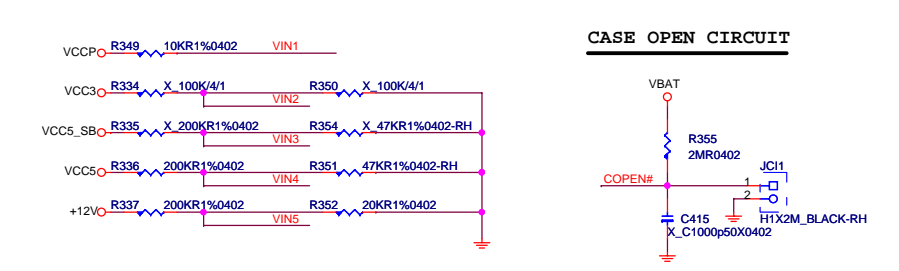
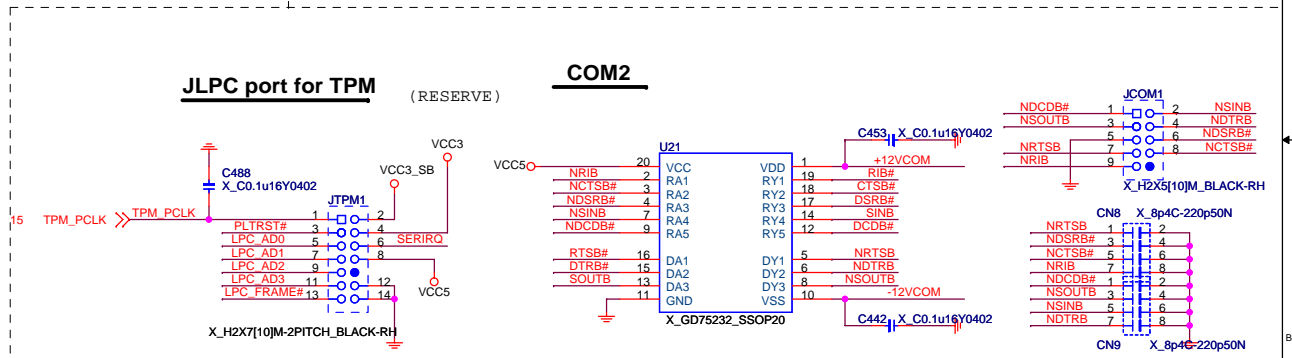
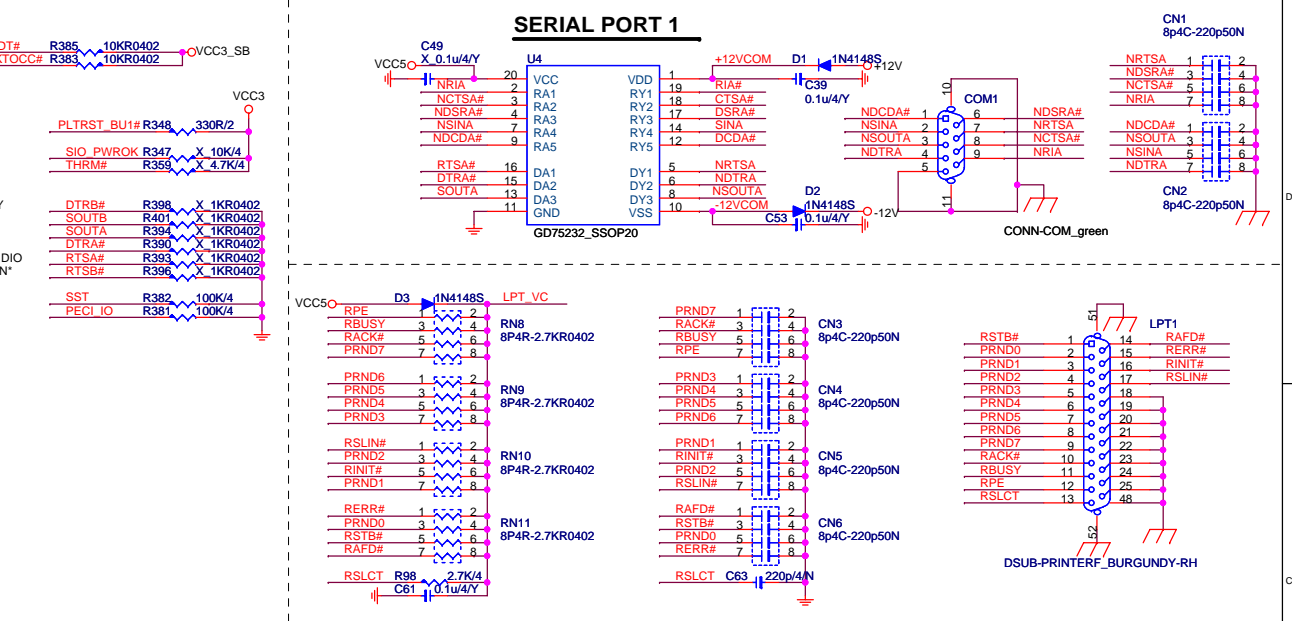
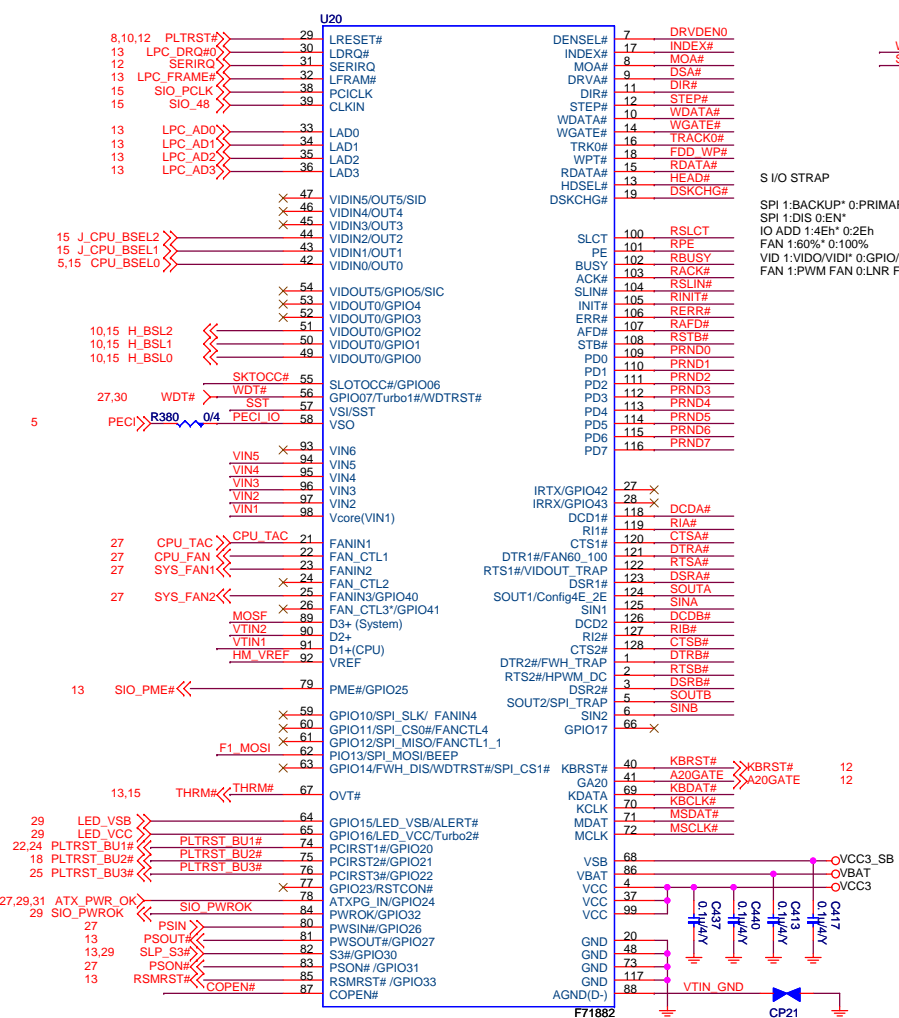


**MSI MICRO-STAR INT'L CO., LTD.**

Title: Clock - ICS9LPRS514EGLF

Size: Document Number: MS-7392

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**MICRO-STAR INT'L CO., LTD.**

Title: SIO

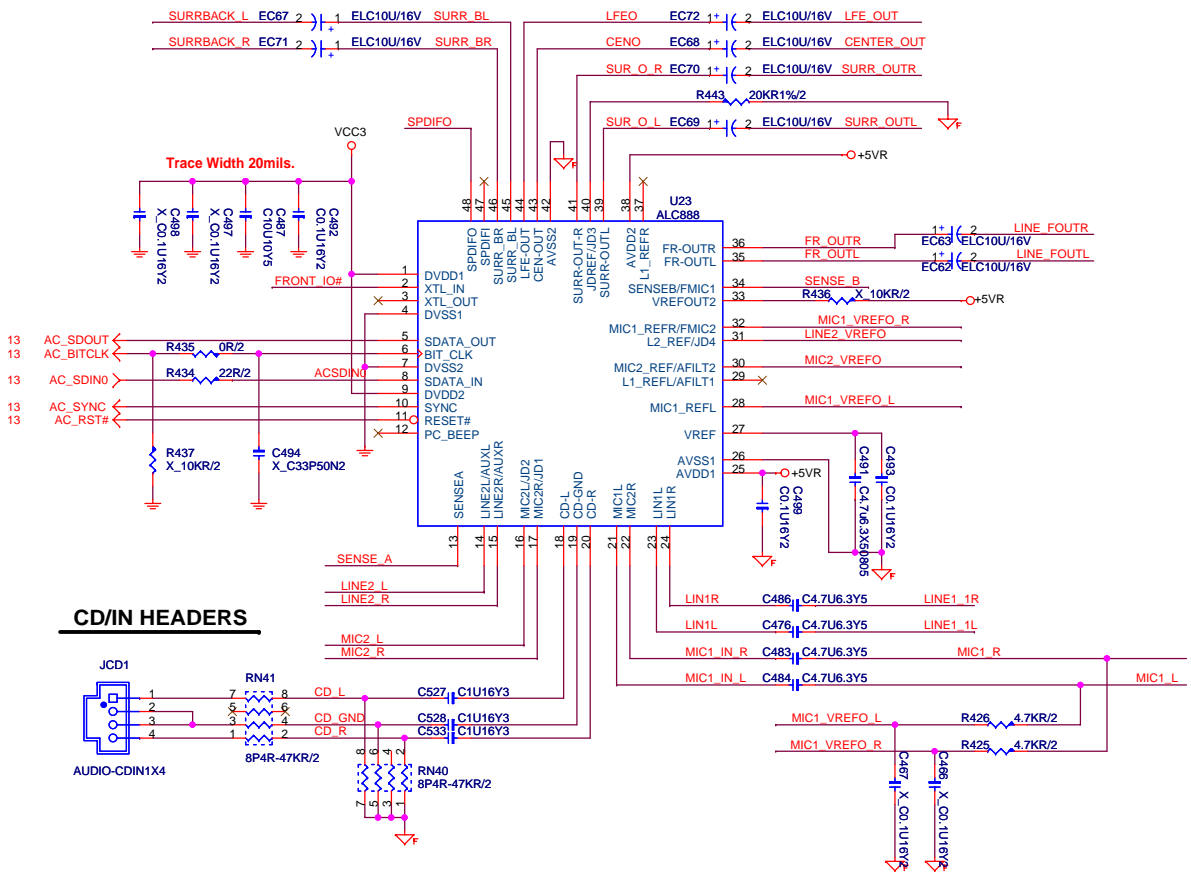
Size: Document Number MS-7392

Date: Tuesday, May 06, 2008

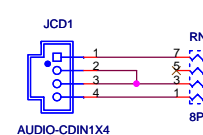
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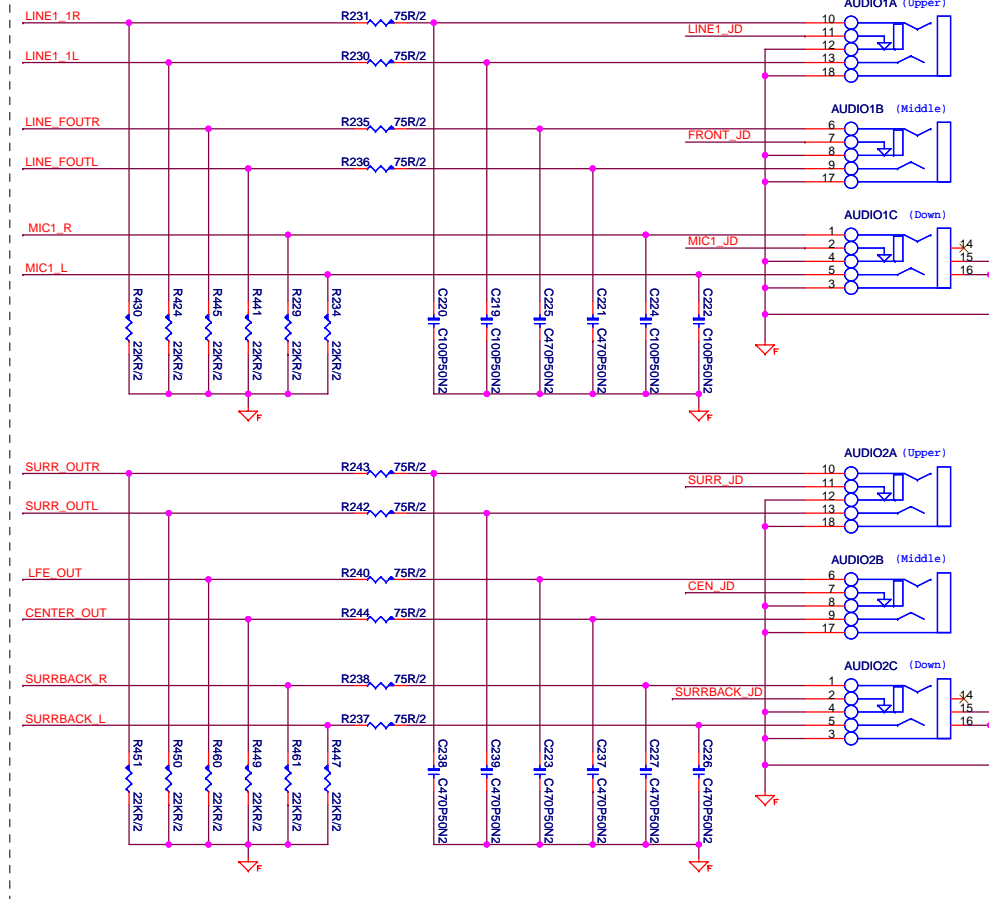
# ALC888 CODEC



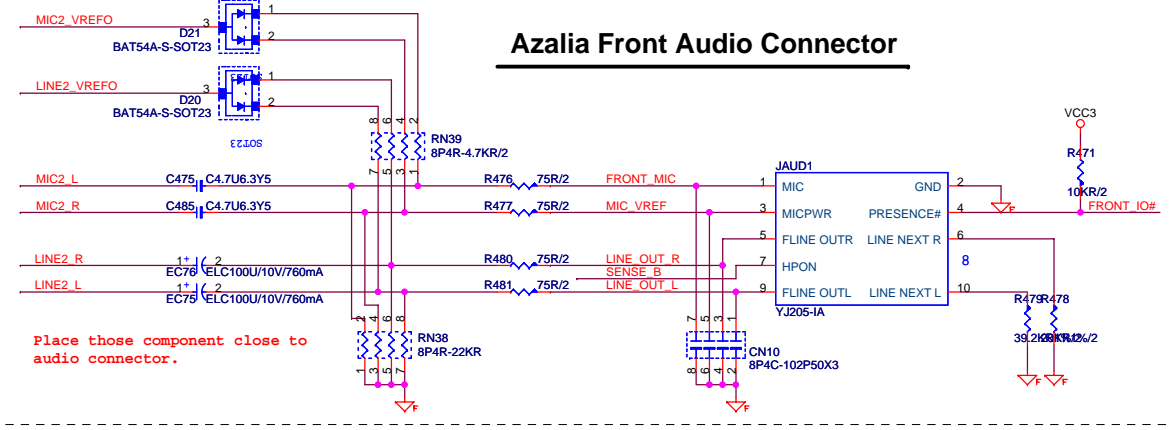
## CD/IN HEADERS



# ALC888 JACK

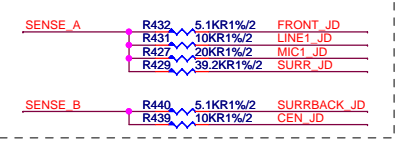


# Azalia Front Audio Connector

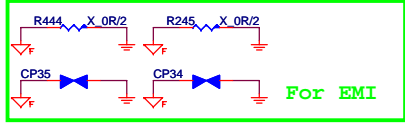
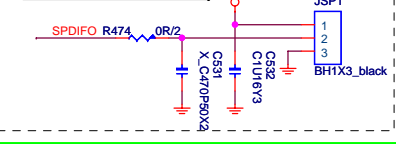


Place those component close to audio connector.

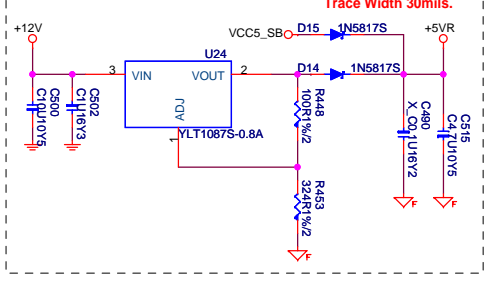
# ALC888 JACK DETECT



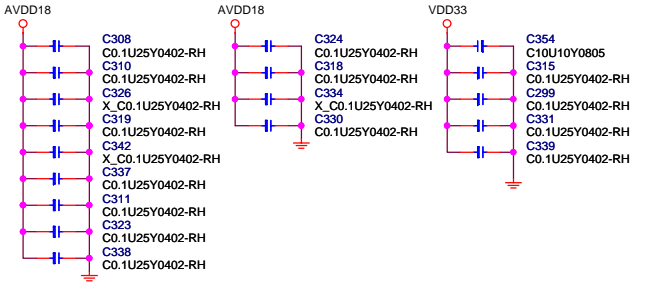
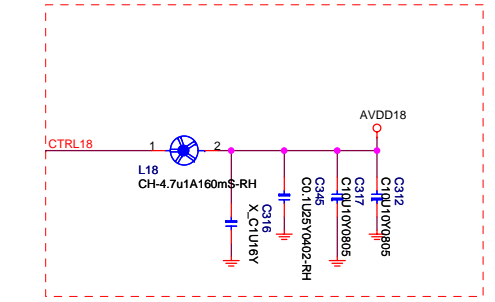
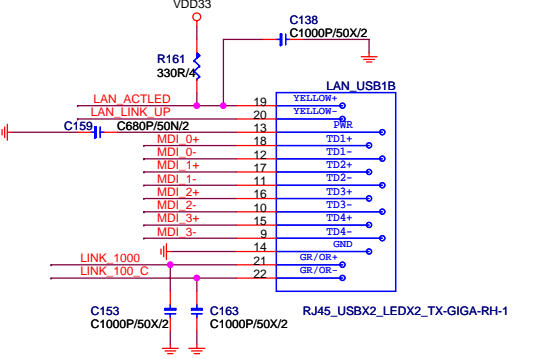
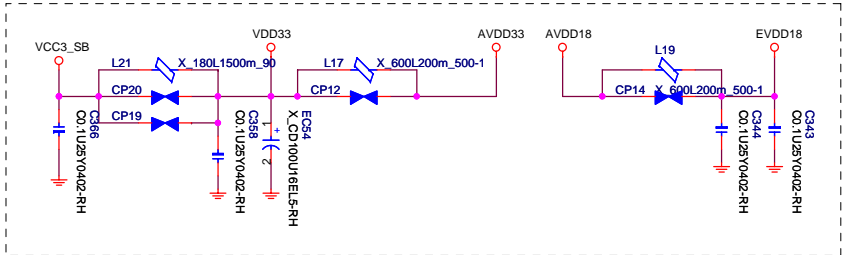
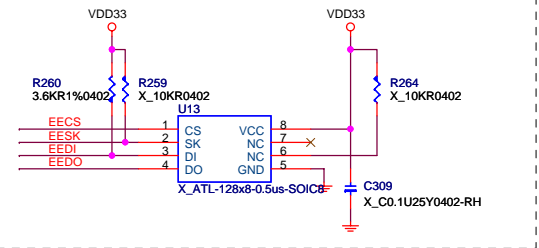
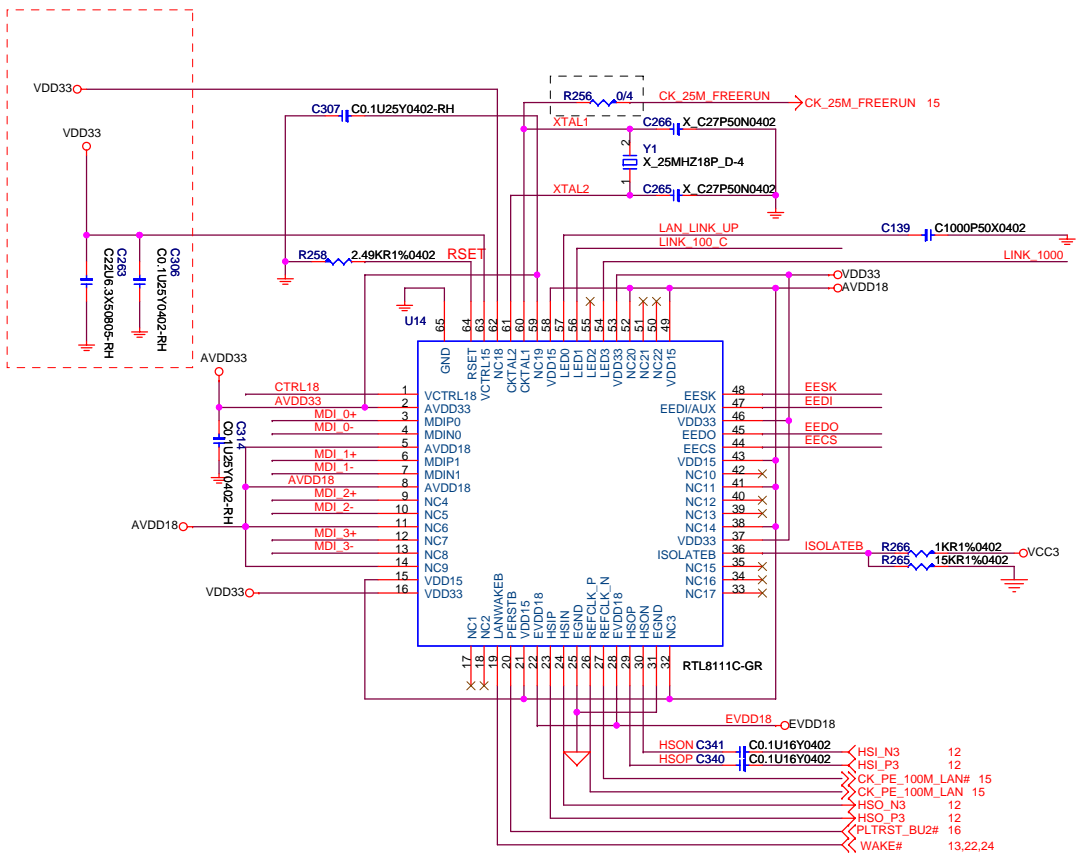
# SPDIF\_OUT



# AUDIO CODE REGULATORS



		<b>MICRO-STAR INT'L CO., LTD.</b>	
Title			
LPC SUPER I/O & CONNECTORS			
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Giga-Lan		10/100-Lan	
N58-22F0181-S42		N58-22F0201-S42	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green

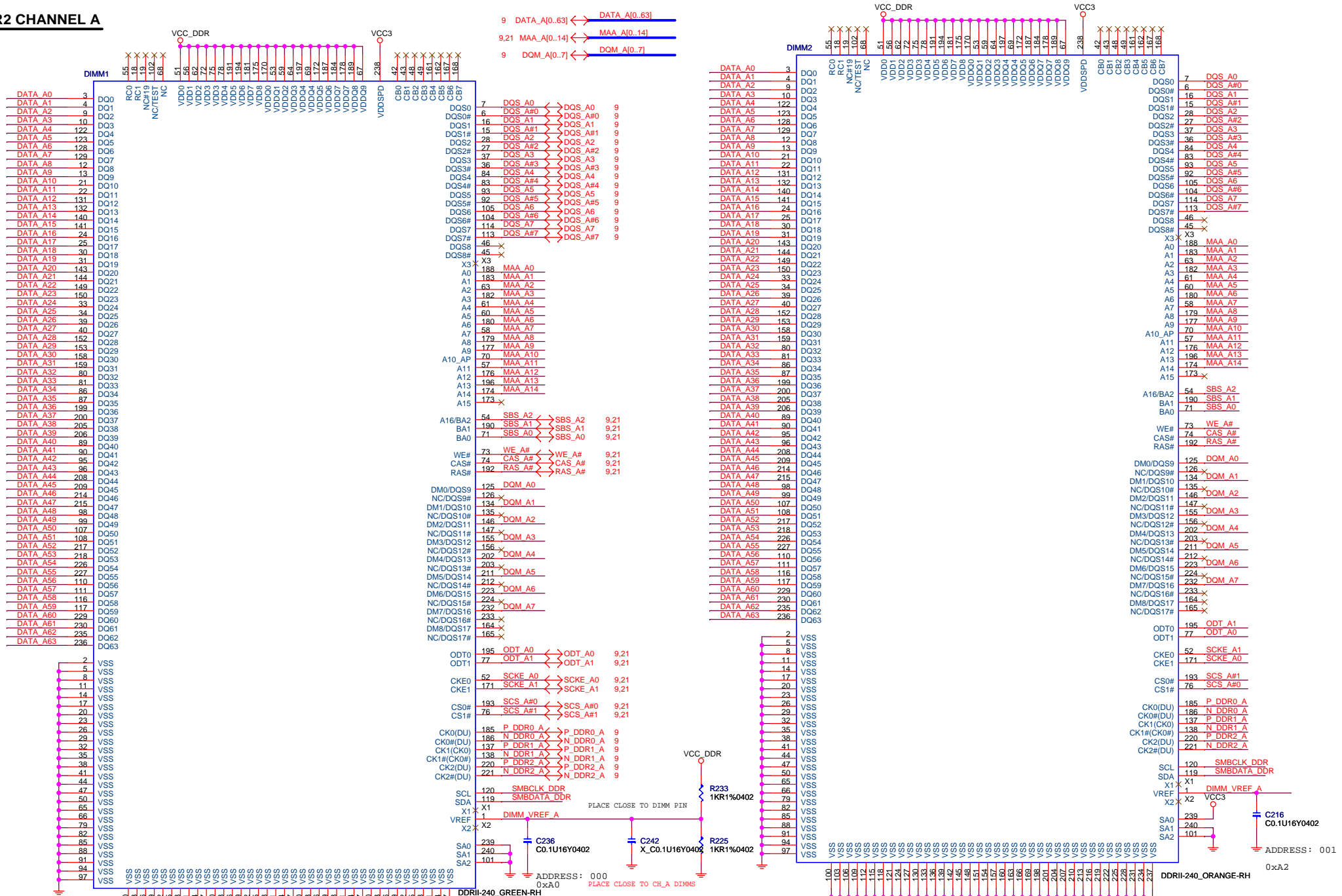
**MSI MICRO-STAR INT'L CO., LTD.**

Title: LAN RTL8111C

Size: Document Number: MS-7392 Rev: 1.2

Date: Tuesday, May 06, 2008 Sheet: 18 of 35

**DDR2 CHANNEL A**



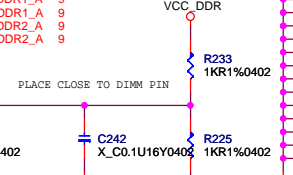
**MSI MICRO-STAR INT'L CO., LTD.**

Title: **DDR II DIMM 1&2**

Size: Document Number **MS-7392** Rev 1.2

Date: Tuesday, May 06, 2008 Sheet 19 of 35

13,15,22,24,29,30 SMBCLK 33R0402 SMBCLK\_DDR 20  
 13,15,22,24,29,30 SMBDATA 33R0402 SMBDATA\_DDR 20



ADDRESS: 000 0xA0  
 ADDRESS: 001 0xA2

DDR2 CHANNEL B

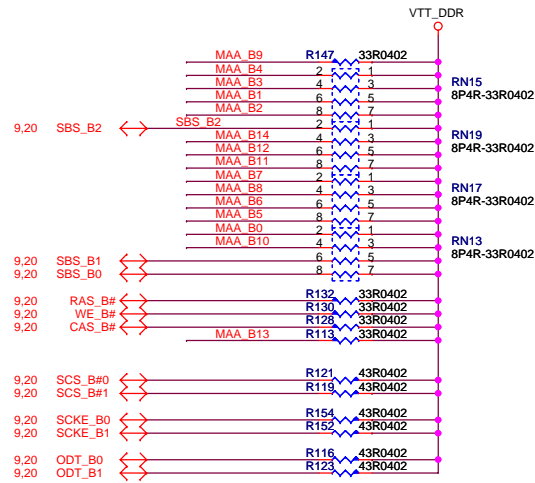
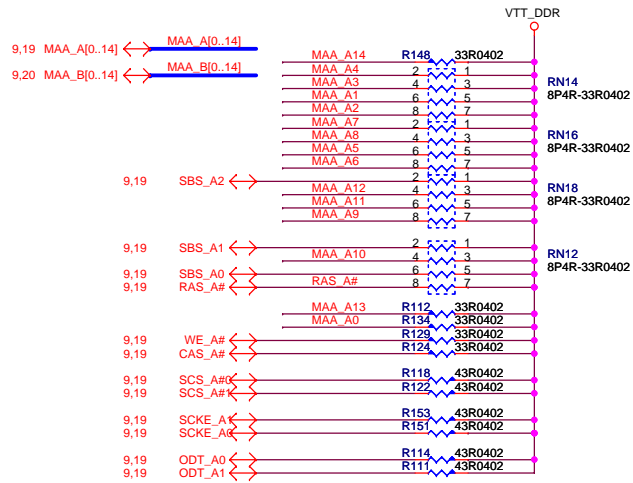


**MSI MICRO-STAR INT'L CO., LTD.**

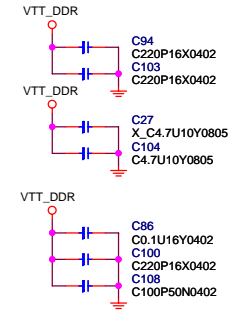
Title: **DDR II DIMM 3&4**

Size: Document Number **MS-7392** Rev: 1.2

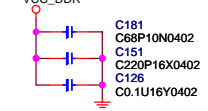
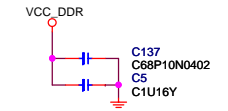
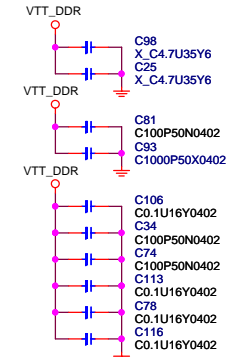
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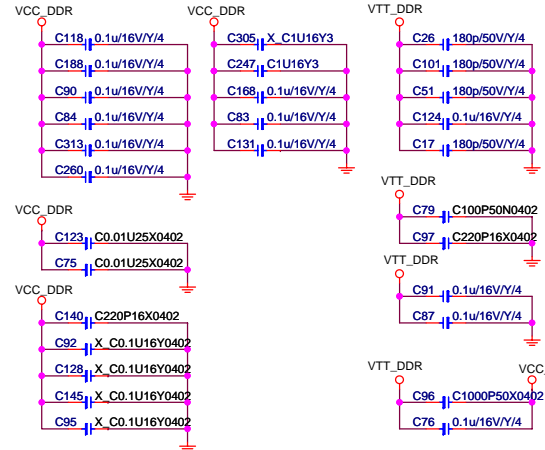
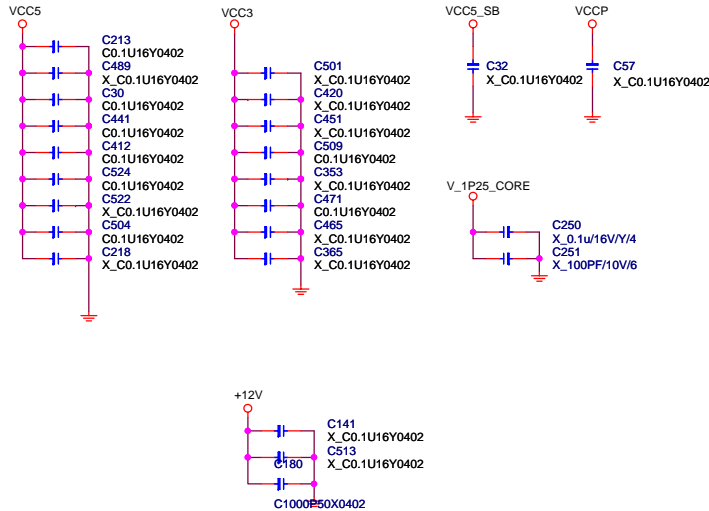
CHANNEL A V\_SM\_VTT DECOUPLING CAPS



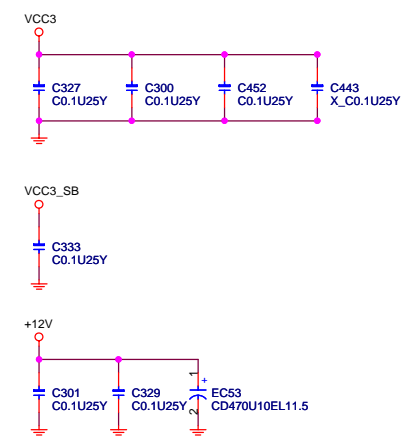
CHANNEL B V\_SM\_VTT DECOUPLING CAPS



**FOR EMI RESERVED**



**FOR EMI RESERVED**



**MICRO-STAR INT'L CO., LTD.**

Title: **PCI EXPRESS 16 PORT**

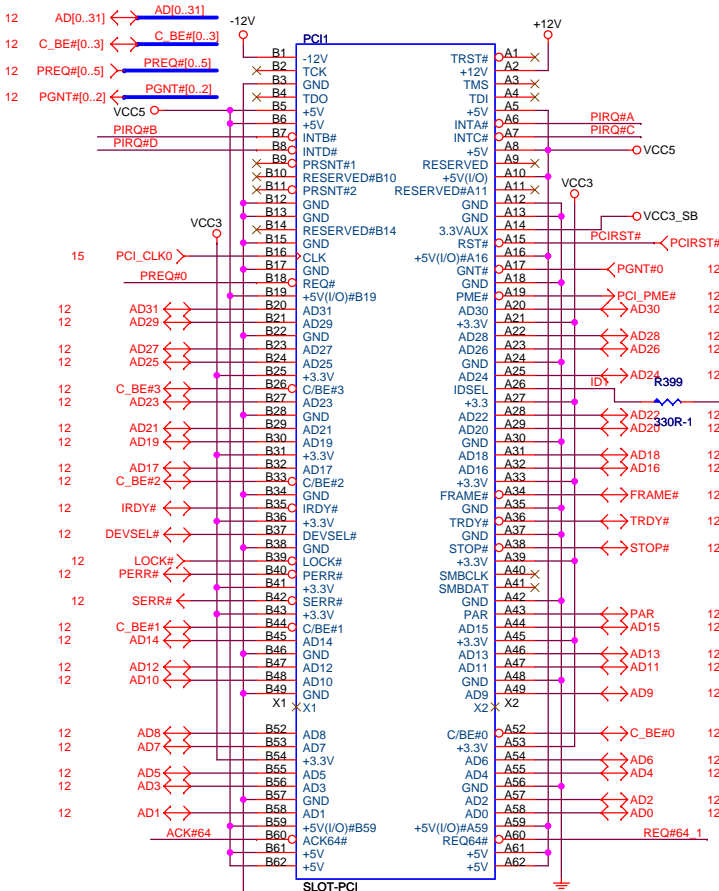
Size	Document Number	Rev
	<b>MSI HS-7392</b>	1.2

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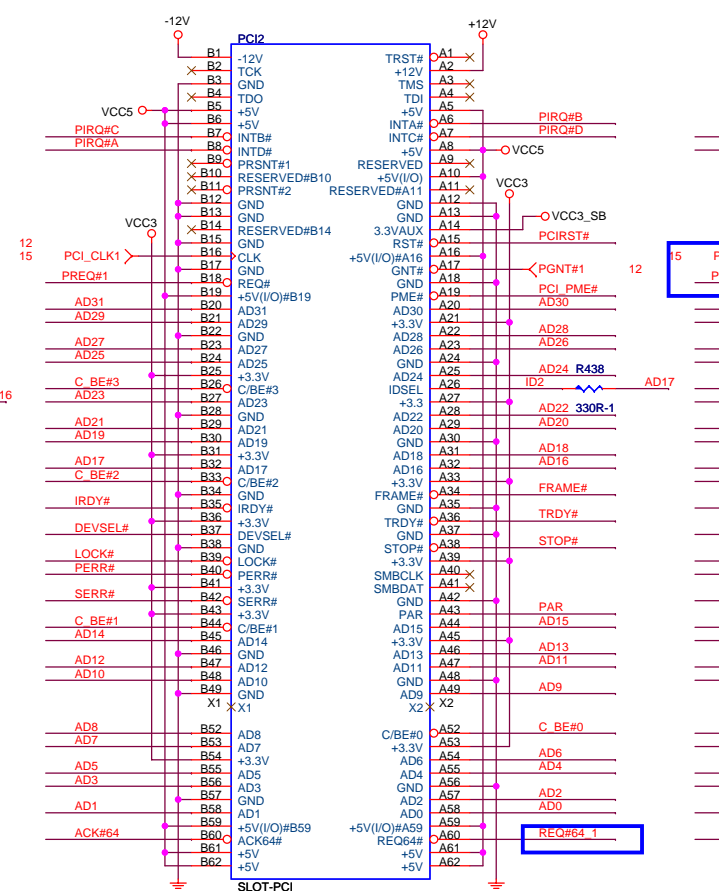
### PCI SLOT 1 (PCI VER: 2.2 COMPLY)

### PCI SLOT 2 (PCI VER: 2.2 COMPLY)

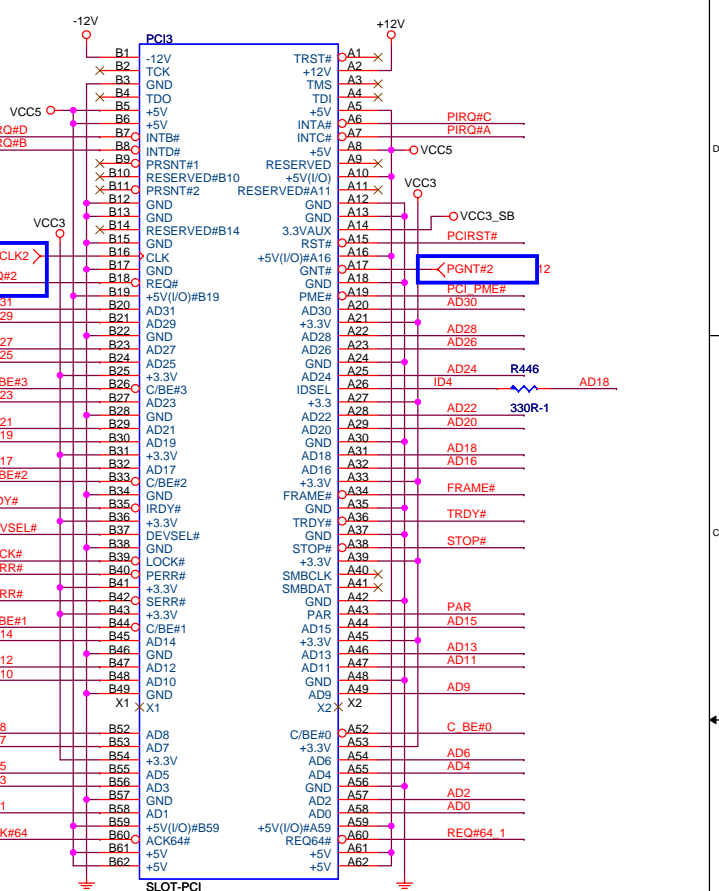
### PCI SLOT 3 (PCI VER: 2.2 COMPLY)



**IDSEL = AD16**  
**MASTER = PREQ#0**  
**PIRQ#A**

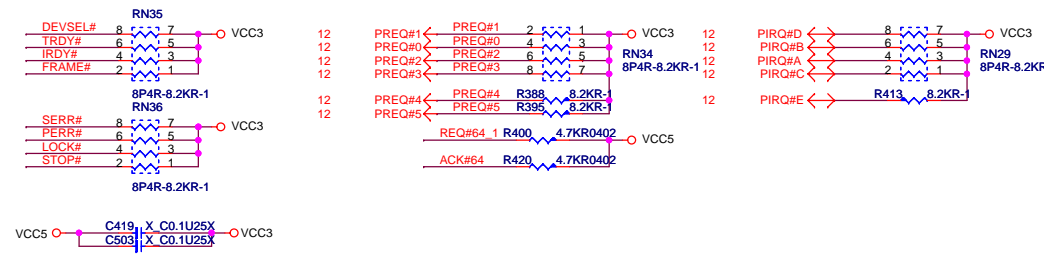


**IDSEL = AD17**  
**MASTER = PREQ#1**  
**PIRQ#B**

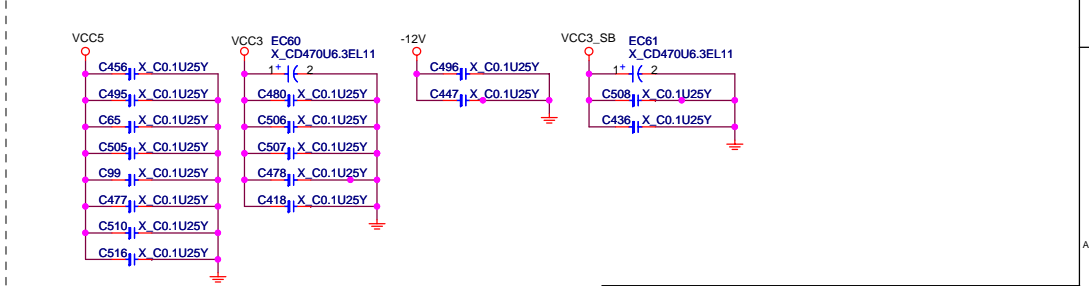


**IDSEL = AD18**  
**MASTER = PREQ#2**  
**PIRQ#C**

#### PCI PULL-UP / DOWN RESISTORS



#### PCI SLOT DECOUPLING CAPACITORS



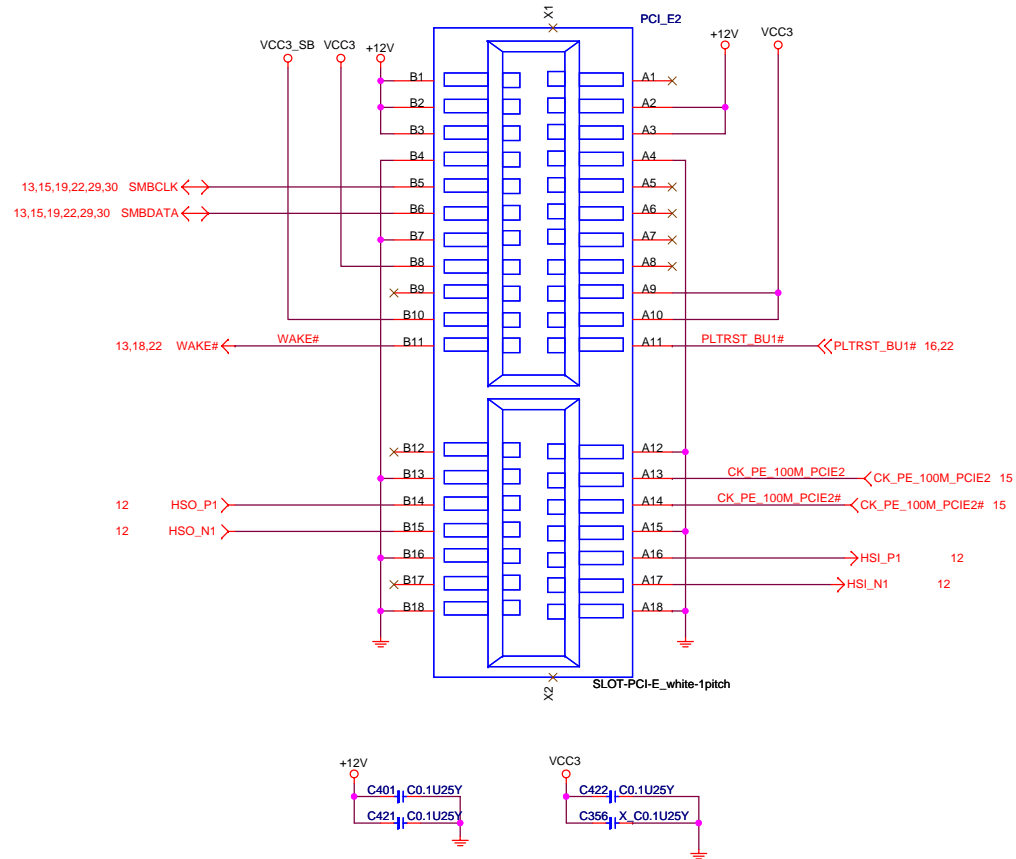
**MSI MICRO-STAR INT'L CO., LTD.**

Title: PCI 1~4 Slots

Size: Document Number MS-7392

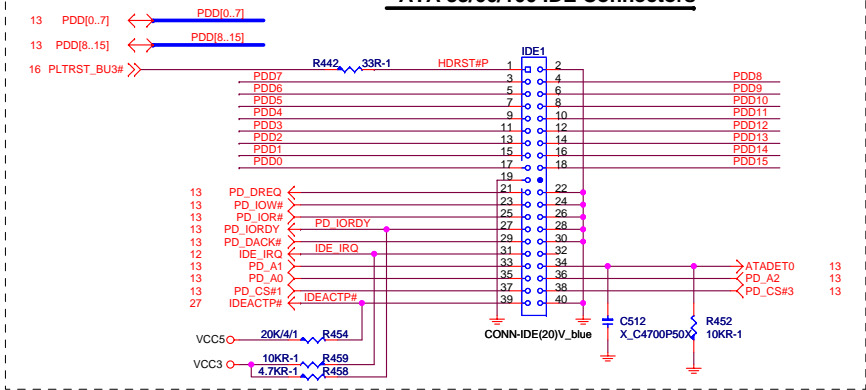
Date: Tuesday, May 06, 2008 Sheet 23 of 35

# PCI EXPRESS 1-PORT

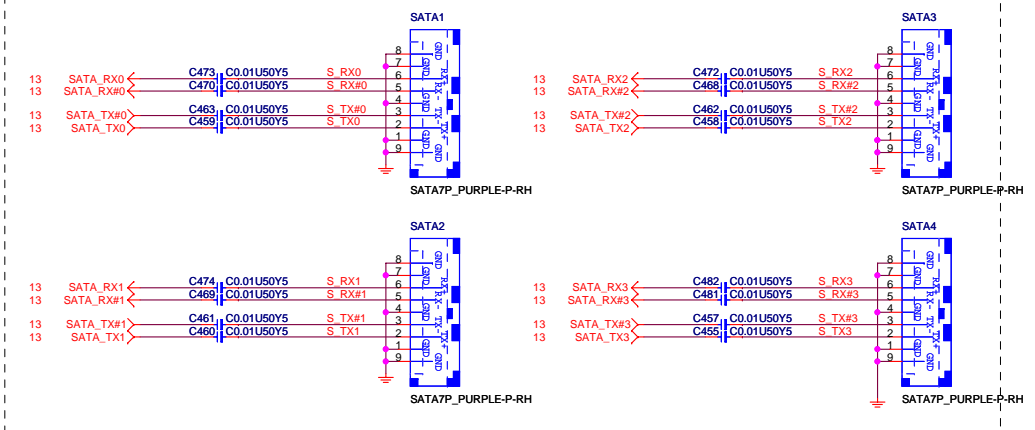




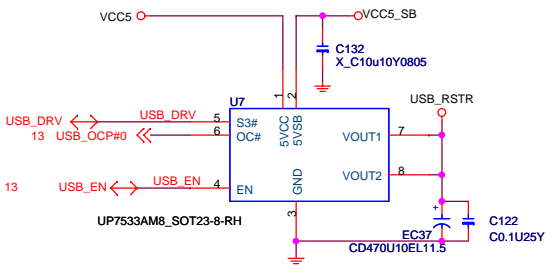
### ATA 33/66/100 IDE Connectors



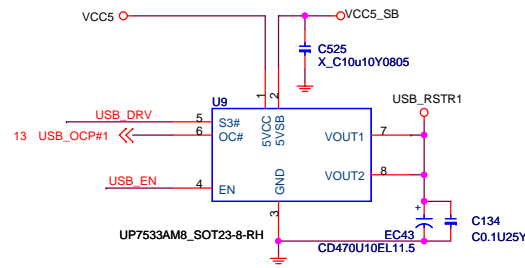
### SERIAL ATA CONNECTOR BLOCK



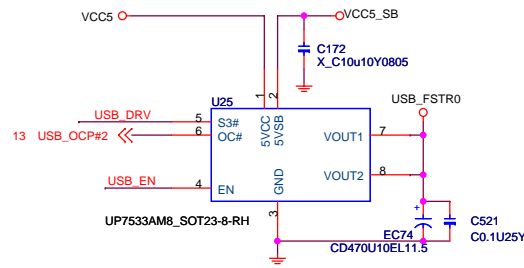
### POWER CIRCUIT FOR USB PORT 0,1



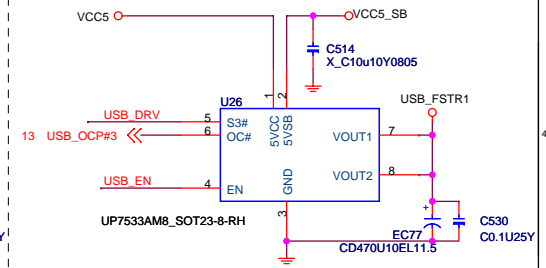
### POWER CIRCUIT FOR USB PORT 2,3



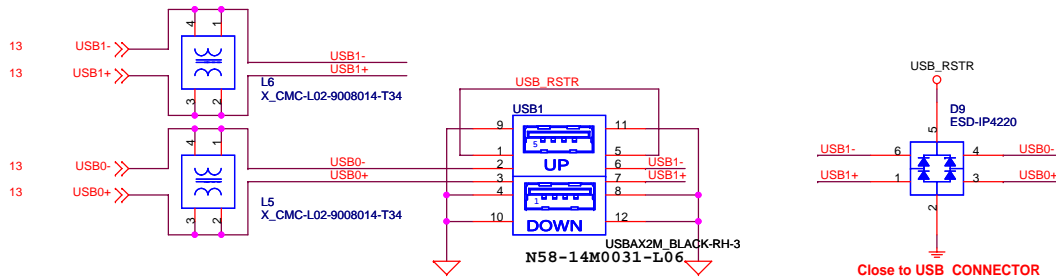
### POWER CIRCUIT FOR USB PORT 4,5



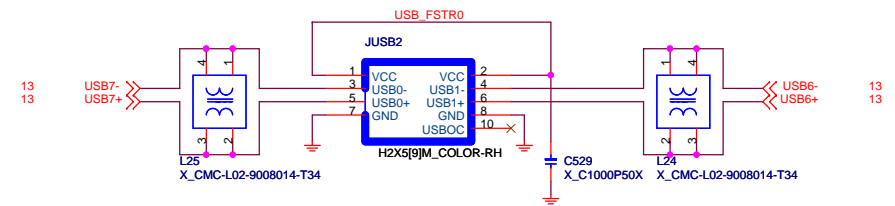
### POWER CIRCUIT FOR USB PORT 6,7



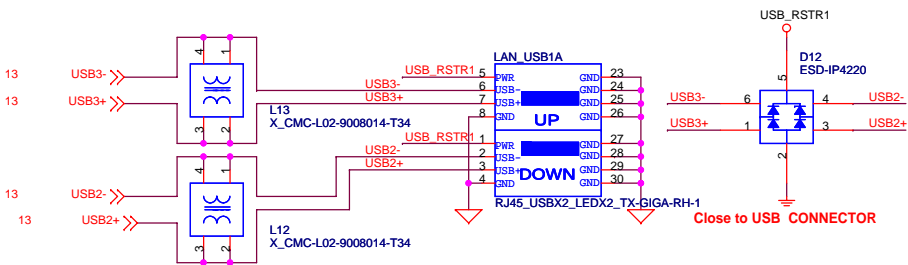
### REAR PANEL USB CONNECTOR FOR USB PORT 0,1



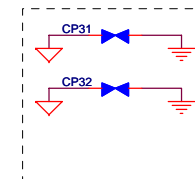
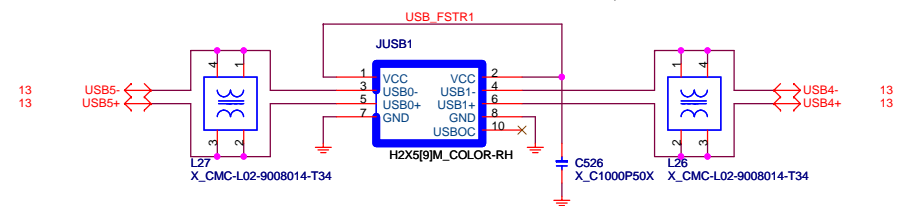
### FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



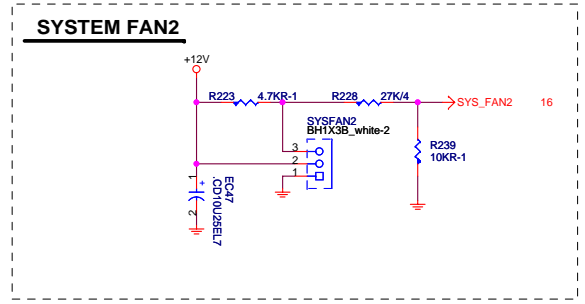
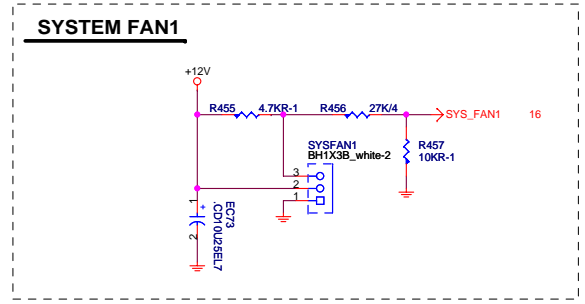
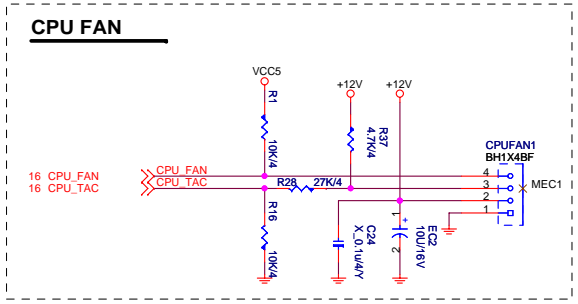
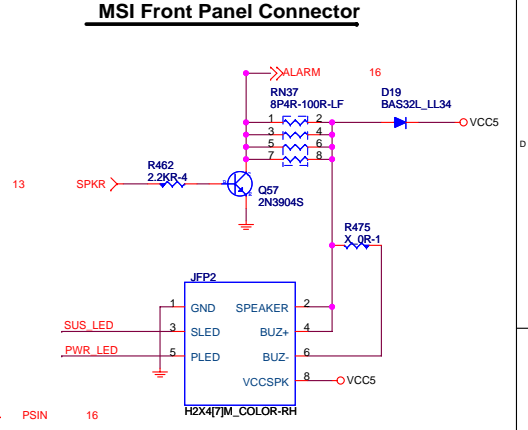
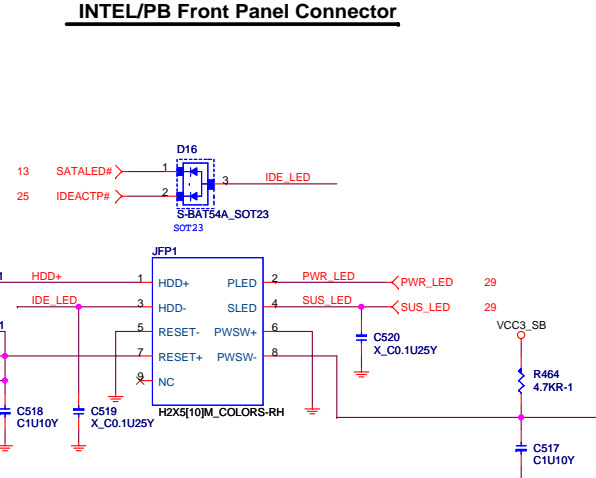
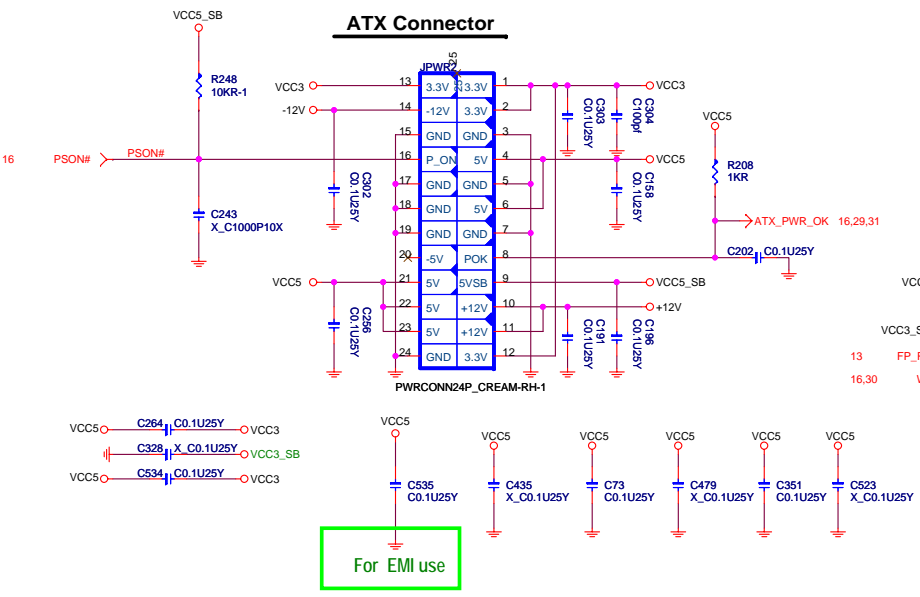
### REAR PANEL USB CONNECTOR FOR USB PORT 2,3



### FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



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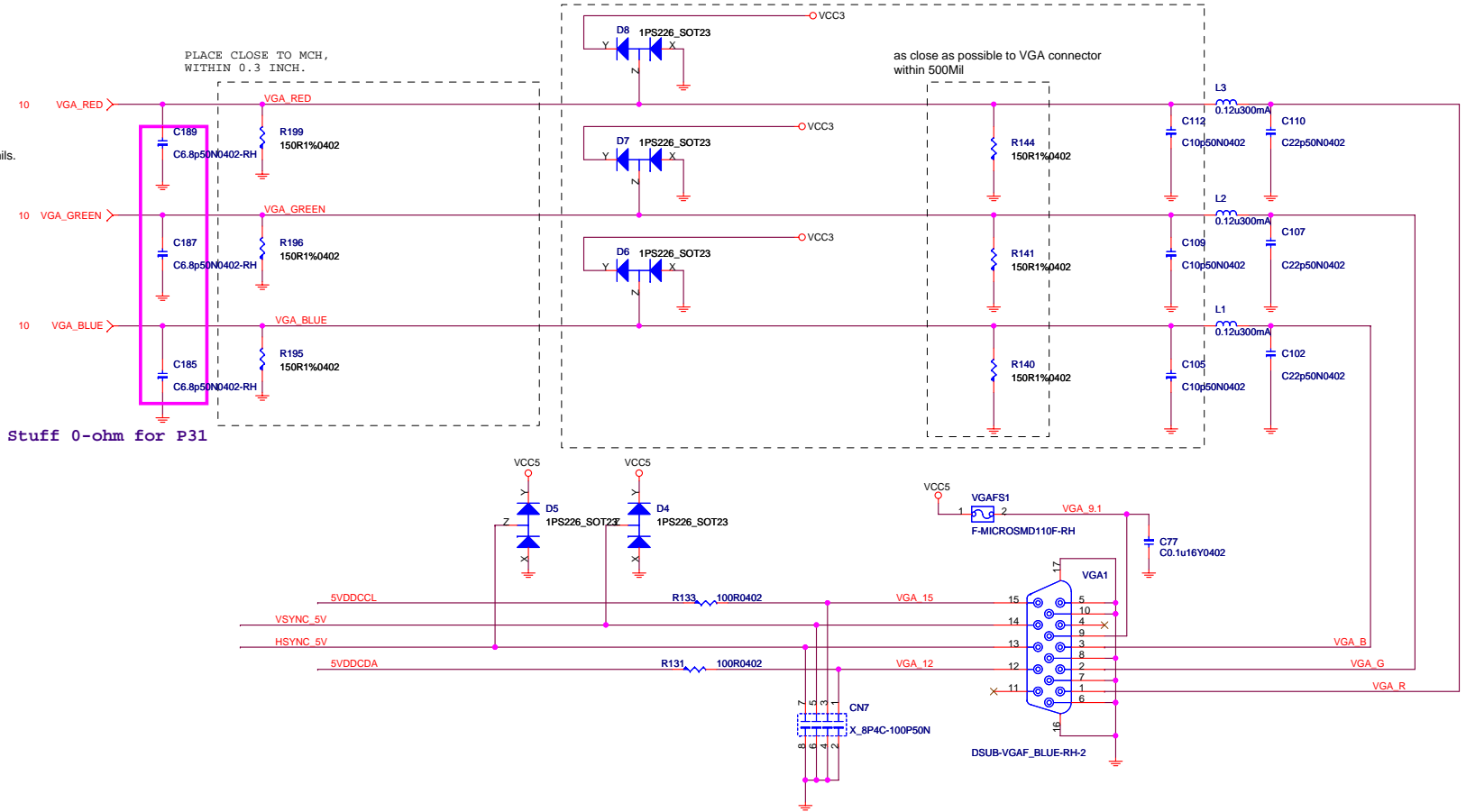
# Video Connector

PLACE CLOSE TO VGA CONNECTOR

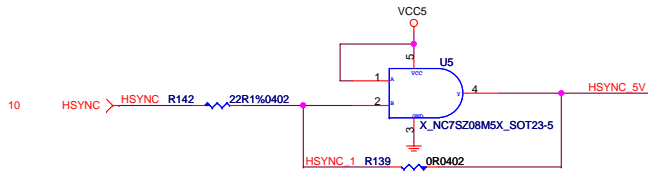
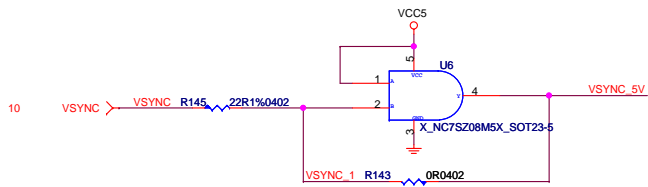
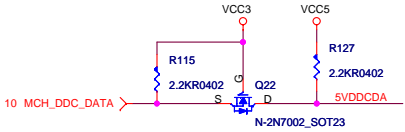
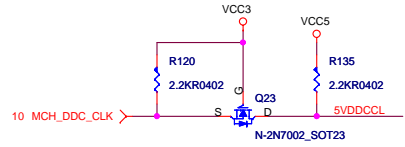
Thw R , G , B route lengths should be length match to 700mils.

PLACE CLOSE TO MCH,  
WITHIN 0.3 INCH.

as close as possible to VGA connector  
within 500Mil



Stuff 0-ohm for P31

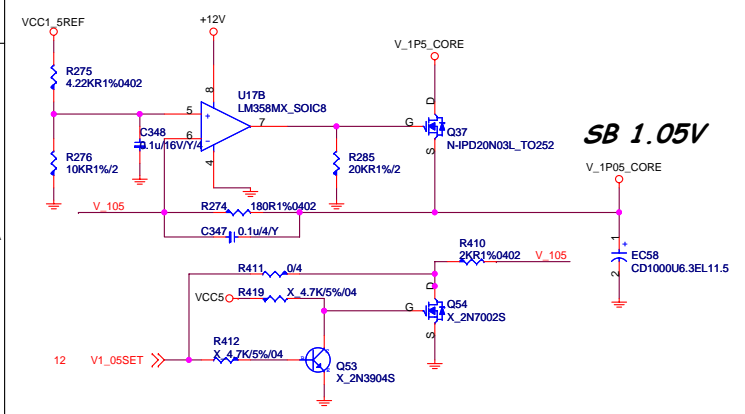
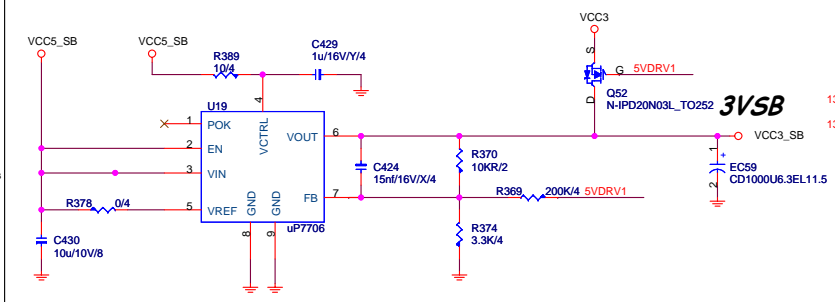
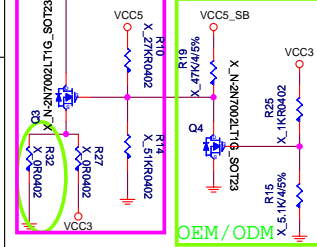


N51-15F0391-F02

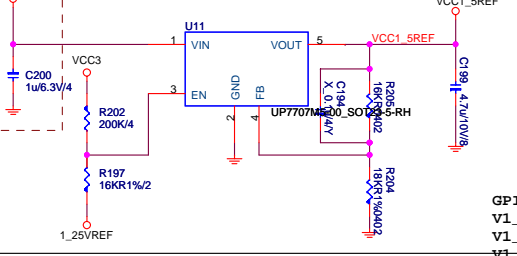
<b>MICRO-STAR INT'L CO., LTD.</b>		
Title: VGA		
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**5VDIMM FOR DDR**

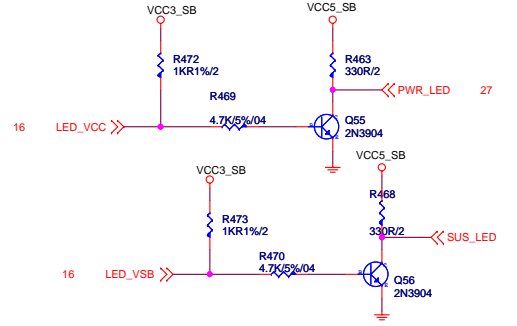
**COST DOWN**



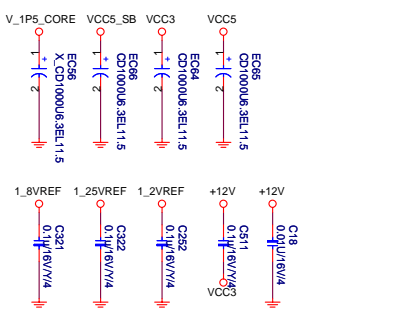
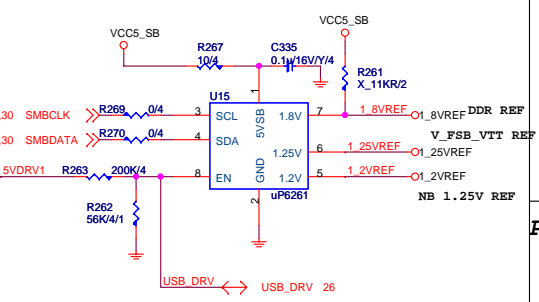
**VCC1\_5REF**



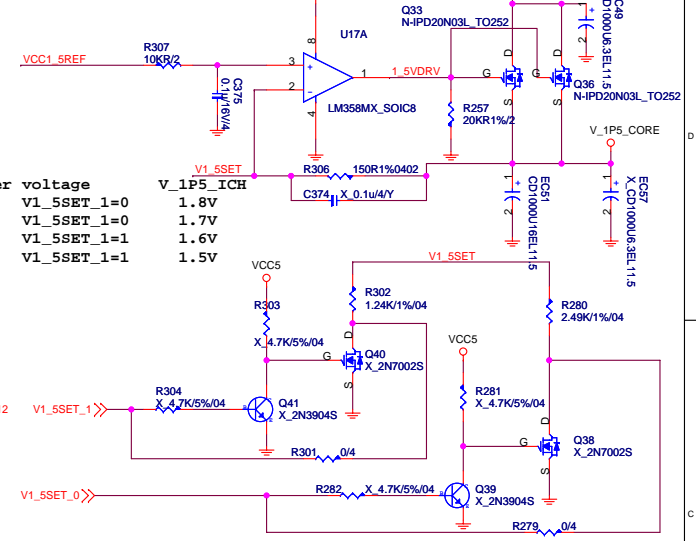
**LED ( for Fintek 71882 )**



**reference Voltage**

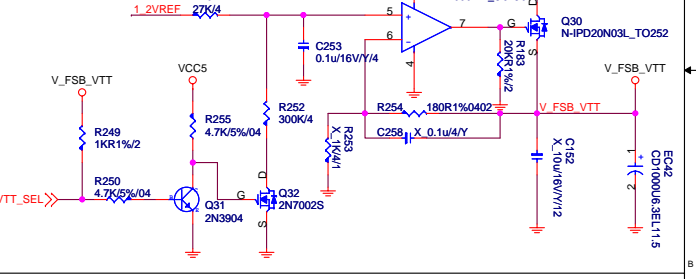


**SB 1.5V**

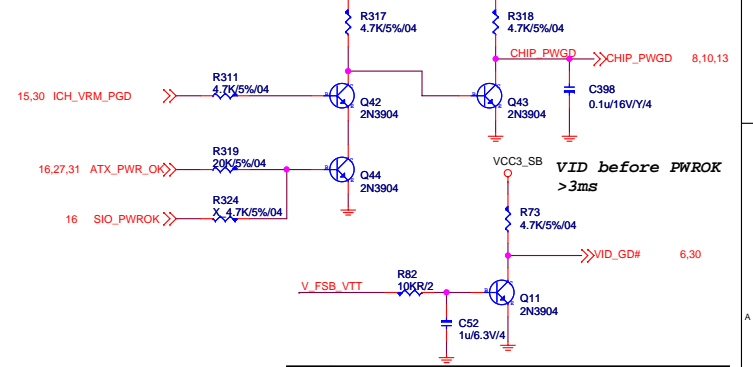


GPIO for over voltage  
V1\_5SET\_0=0 V1\_5SET\_1=0  
V1\_5SET\_0=1 V1\_5SET\_1=0  
V1\_5SET\_0=0 V1\_5SET\_1=1  
V1\_5SET\_0=1 V1\_5SET\_1=1

**1.2V**

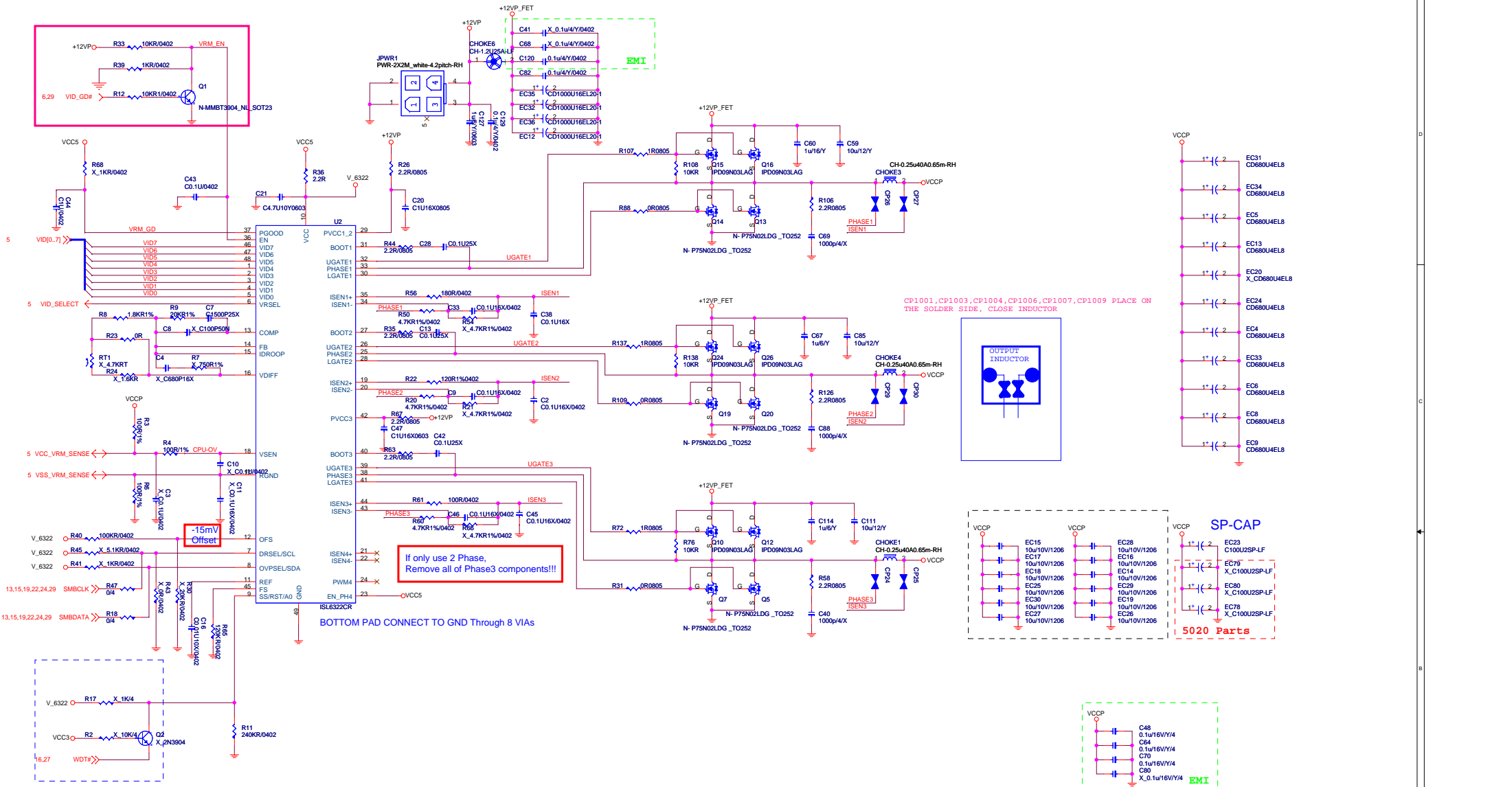


**PWROK DELAY 100ms**



<b>MSI MICRO-STAR INT'L CO., LTD.</b>	
Title ACPI CONTROLLER UPI	
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A B C D

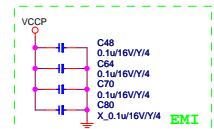
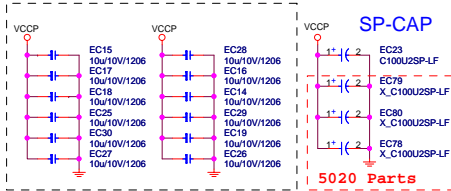
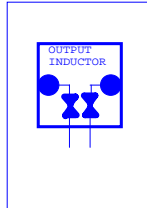


**-15mV Offset**

**If only use 2 Phase, Remove all of Phase3 components!!!**

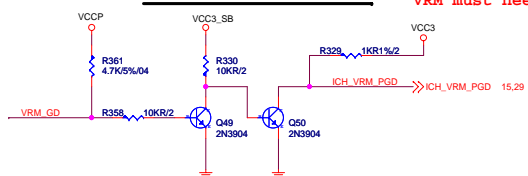
**BOTTOM PAD CONNECT TO GND Through 8 VIAs**

**CP1001,CP1003,CP1004,CP1006,CP1007,CP1009 PLACE ON THE SOLDER SIDE, CLOSE INDUCTOR**



**VRMPWRGD LEVEL SHIFT**

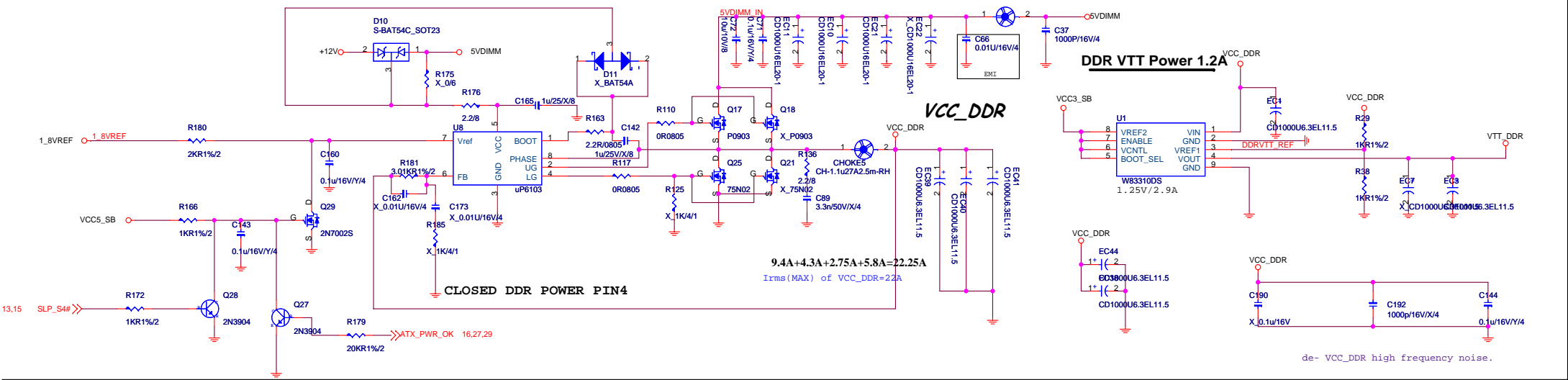
**For Intel DG VRM must need level shift**



**DDR II 1.8V POWER**

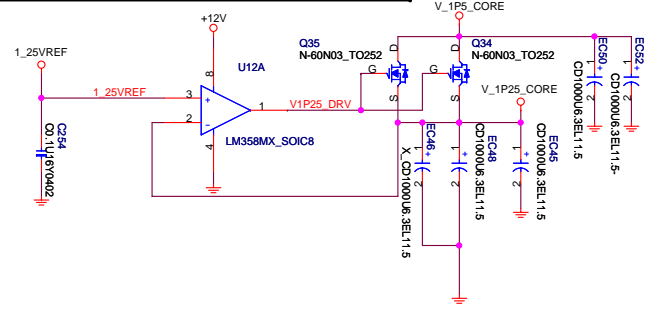
$I_{ripple} = 21 * 0.6 * 0.8 / 1 = 10.08A$   
 $2.22 * 3 * 1.7 = 11.322A > 10.08A$

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



**NB 1.25V POWER**

**V\_1P25\_CORE 18.1A + 2.47A + 2.94A**

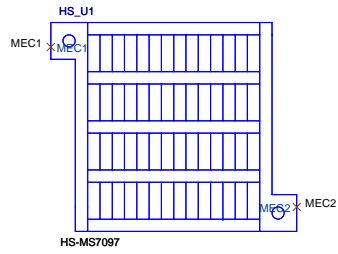


**Auto-BOM Manual Parts**

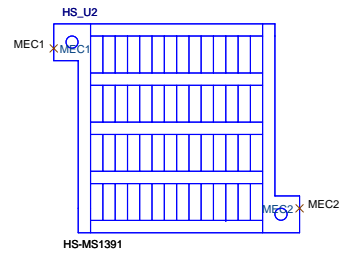
PCB1  
PCB  
PCB-7392



**P31 HEATSINK**



**ICH7 HEATSINK**



**Auto-BOM Option Parts**

ICH7  
OPT  
X\_ICH7

G31  
OPT  
X\_G31

P31-R1  
OPT  
X\_OR0402

OnVGA1.3  
OPT  
X\_1.3KR1%/2

G31-C1  
OPT  
X\_C0.1U16V0402



1.0 Change 1.1 list:

1. Co-lay G31 add COM2,change LTP to Connect
2. change USB power to UPI 7533
3. change LAN only to 8111C
4. change CLKGEN to 906
5. Add OC Jumper
6. change clk netname,swapVGA\_ 12/VGA\_ 15 and HSYNC/VSYNC
7. remove CP5,CP6,CP21
8. Change TestPIN footprint to TPC20B
9. Remove SMBus for PCI.
10. Rename,and add OC Jump

1.1 Change 1.2 list:

1. change CHOKE 2/5/6 to 方形CHOKE

Title		
<Title>		
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