DATA SHEET

MS-3 Rev 2.2

Product Specification Mar, 2001

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243

Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

MS-3 Specification MS-3

1. General Description

The MS-3 ASIC is designed as a general-purpose input/output IC or a jumperless IC for CPU frequency and voltage configuration. Ability to bit(s) accessibility by embedded write-mask provides easier configuration of registers and port's contents. MS-3 ASIC also can provides an interrupt when appointed transition (rising, falling or both) of port occurs.

2. Features

- 3.3V operation voltage.
- 56-pin, 300 mils SSOP package.
- Two wires serial bus interface.
- Programmable serial bus address **0 0 1 1 0 AD_1 AD_0**.
- There are two operation modes used to CPU frequency and voltage jumperless configuration.
  - Intel mode.
  - AMD mode.
- Programmable WatchDog timer for CPU jumperless configuration.
- Maximum 8 port's (41 pins) general purpose I/O pins.
- Level mode interrupt output when appointed transition of ports occurs.
- Flexible output type (Input/Output/Open-drain).
- Flexible output style (level or pulse mode) and pulse's width.
- Using configuration to make more flexible port utilization possible and regardless of current CPU mode selection.
- Ability to bit(s) accessibility through write-mask.
- Ability to pull down PWRGD pin for a programmable period by a simple configuration register write.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243

Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

3. MS-3 Pin Assignment

Pin #	Default Type	Power Rail	Pin Name	Description
01	Ground	-	VSS	Ground.
02	I	VCC3	P00/FIDI0	General purpose I/O port (P0[3:0]) or CPU FID input port (FIDI[3:0]) for CPU jumperless configuration.
03	I	VCC3	P01/FIDI1	
04	I	VCC3	P02/FIDI2	
05	I	VCC3	P03/FIDI3	
06	I	VCC3	P04/ICRST#	General purpose I/O pin (P0[4]) or CPU reset input pin (ICRST#) for Intel mode. In AMD mode, this pin is reversed for future CPU FID4 input.
07	OD	VCC3	P10/FIDO0	General purpose I/O port (P1[4:0]) or an open-drain output port for CPU jumperless configuration (FIDO[4:0]). In Intel mode: If pin P04/ICRST# is kept high, the data presented on this port is passed from P0[4:0]/FIDI[4:0] input directly. Otherwise, if pin P04/ICRST# is kept low, the output data presented on this port is passed from the content of port1 output register –POR1 (if control bit "FIDOSel" is set) or port A2[4:0]/BP[4:0] input (if control bit "FIDOSel" is not set). In AMD mode: The output data presented on this port is passed from the content of port1 output register –POR1[4:0] (if control bit "BPSel" is set) or P0[4:0]/FIDI[4:0] input (if control bit "BPSel" is not set). See "CPU Frequency and Voltage Configuration Registers" for FIDOSel and BPSel.
08	OD	VCC3	P11/FIDO1	
09	OD	VCC3	P12/FIDO2	
10	OD	VCC3	P13/FIDO3	
11	OD	VCC3	P14/FIDO4	
12	Power	-	AVCC	Power pin for A24/BP4~A20/BP0.
13	I	AVCC	A20/BP0	General-purpose I/O port (A2[4:0]) or jumperless configuration port for CPU bus ratio (BP[4:0]). In Intel mode: It is used as an external CPU bus ratio input port. In AMD mode: When a different bus ration is going to be applied, this port can be programmed as an output port for AMD BP[4:0] and the data presented on this port is passed from port1 output register –POR1. In order to recover from failed over-clock, once WatchDog timer overflow flag (WDTOV) is set, this port will turn into input mode to isolate itslef from AMD BP bus automatically regardless of current port type configuration.
14	I	AVCC	A21/BP1	
15	I	AVCC	A22/BP2	
16	I	AVCC	A23/BP3	
17	I	AVCC	A24/BP4	

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

Pin #	Default Type	Power Rail	Pin Name	Description
18	I	VCC3	P30	General-purpose I/O port P3[6:0].
19	I	VCC3	P31	
20	I	VCC3	P32	
21	I	VCC3	P33	
22	I	VCC3	P34	
23	I	VCC3	P35	
24	I	VCC3	P36	
25	I	VCC3	P37/STPCLK#	General-purpose I/O port (P37) or stop clock input pin (STOPCK#).
26	I	VCC3	I/SCK	Serial bus Clock line.
27	I	VCC3	I/SIO	Serial bus Data line.
28	Ground	-	VSS	Ground.
29	Power	VCC3	IVCC	Power Pin.
30	CLOCK	VCC3	OSCI	External 14MHz Clock Input Pin.
31	CLOCK	VCC3	OSCO	A 4K Ω resistor connected to OSCI to enable internal 14MHz oscillator.
32	I	VCC3	I/RST#	Reset input pin.
33	OD	VCC3	P40/VIDO0	General-purpose I/O port (P4[4:0]) or open-drain output port for CPU VID jumperless configuration (VIDO[4:0]).
34	OD	VCC3	P41/VIDO1	
35	OD	VCC3	P42/VIDO2	
36	OD	VCC3	P43/VIDO3	
37	OD	VCC3	P44/VIDO4	
38	I	VCC3	P50/VIDI0	General-purpose I/O port (P5[4:0]) or input port for CPU VID jumperless configuration (VIDI[4:0]).
39	I	VCC3	P51/VIDI1	
40	I	VCC3	P52/VIDI2	
41	I	VCC3	P53/VIDI3	
42	I	VCC3	P54/VIDI4	
43	I	VCC3	P60	General-purpose I/O port P6[7:0] .
44	I	VCC3	P61	
45	I	VCC3	P62	
46	I	VCC3	P63	
47	I	VCC3	P64	
48	I	VCC3	P65	
49	I	VCC3	P66	
50	I	VCC3	P67	

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

Pin #	Default Type	Power Rail	Pin Name	Description
51	O	VCC3	INT	Interrupt output pin.
52	OD	VCC3	PWRGD	Reset output pin. This pin will assert low when WatchDog timer overflow occurs or there is a write to configuration register index 2Ah.
53	I	VCC3	SEL	MS-3 operation mode selection. 0 = Intel mode. 1 = AMD mode.
54	I	VCC3	AD0	Serial bus Address[1:0] .
55			AD1	
56	Power	VCC3	IVCC	Power pin.

I - Input Pin.

O - Output Pin.

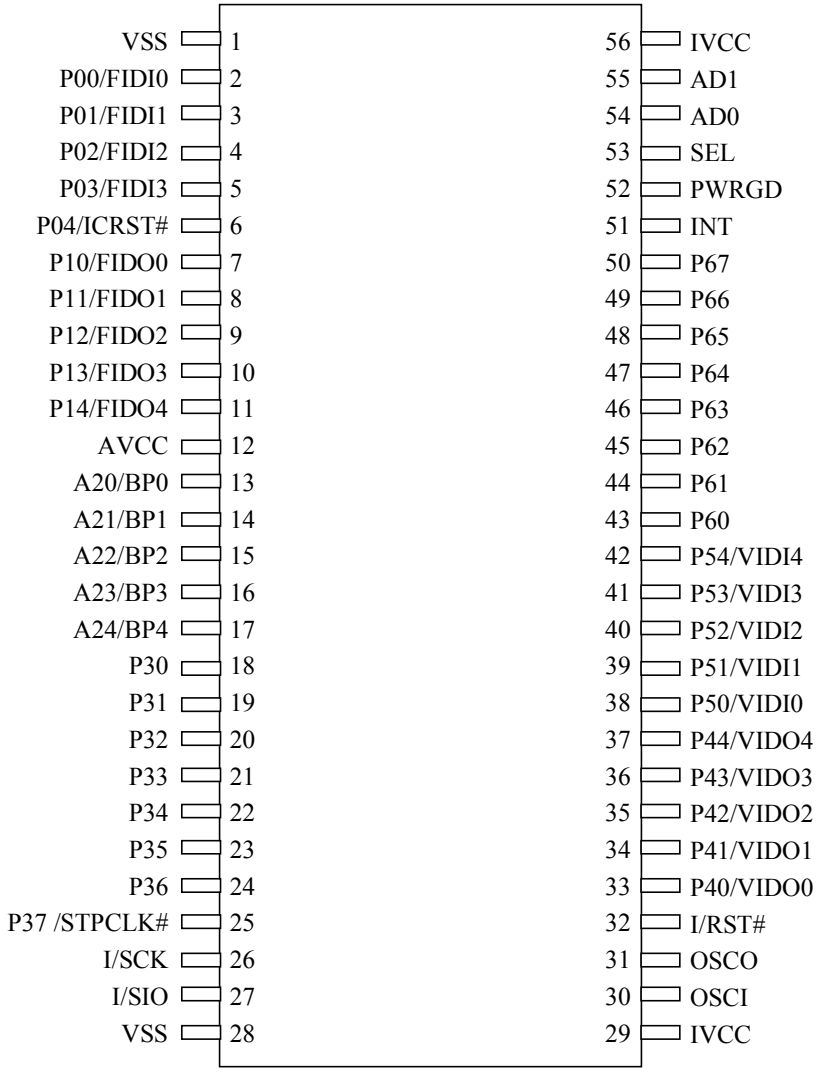
OD - Open-Drain Output Pin.

CPU mode – Intel mode, AMD mode.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243

Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

4. MS-3 Pin Diagram



MS-3 Pin Diagram (Top View)

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243

Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

5. MS-3 Configuration Registers Overview

Registers	Offset
Port Output Data Registers	00~06
Port Input Data Registers	08~0F
Port Type Configuration Registers	10~15
GP Port 3 Output Pulse Width Configuration Registers	16
GP Port3 Interrupt Triggered Condition Registers	17~18
GP Port3 Normal High Output Configuration Registers	19
GP Port3 Pulse Mode Configuration Registers	1A
GP Port3 Interrupt Registers	1B
GP Port3 Interrupt Configuration Registers	1C
GP Mode And Test Mode Configuration Register	1D
General Purpose I/O Port Data and Configuration Reset Mode Registers	1E
Port Latch Registers	1F~22
Latch Mode Configuration Register	23
CPU Frequency and Voltage Configuration Registers	24~25
WatchDog Configuration Registers	26
WatchDog Timer	27
STPCLK VID Registers	28
Write Mask	29
Power Good Registers	2A

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

6. MS-3 Configuration Registers Description

Port Output Data Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
00h	R/W	00h	**P04/ICRST#,P03/FIDI3~P00/FIDI0** Port 0 Output Data Register (POR0). Bit 4~0: P0[4:0] Output Data Register. Bit 7~5 : Reversed.
01h	R/W	00h	**P14/FIDO4~P10/FIDO0** Port 1 Output Data Register (POR1). Bit 4~0: P1[4:0] Output Data Register. Bit 7~5 : Reversed.
02h	R/W	00h	**A24/BP4~A20/BP0** Port 2 Output Data Register (POR2). Bit 4~0 : A2[4:0] Output Data Register. Bit 7~5 : Reversed.
03h	R/W	00h	**P37/STPCLK#,P36~P30** General-Purpose Port 3 Output Data Register (POR3).
04h	R/W	00h	**P44/VIDO4~P40/VIDO0** Port 4 Output Data Register (POR4). Bit 4~0: P4[4:0] Output Data Register. Bit 7~5 : Reversed.
05h	R/W	00h	**P54/VIDI4~P50/VIDI0** Port 5 Output Data Register (POR5). Bit 4~0: P5[4:0] Output Data Register. Bit 7~5 : Reversed.
06h	R/W	F0h	**P67 ~P60** General-Purpose Port 6 Output Data Register (POR6).

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

Port Input Data Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
08h	R	-	**P04/ICRST#,P03/FIDI3~P00/FIDI0** Port 0 Input Data Register (PIR0). Bit 4~0: P0[4:0] input data register. Bit 7~5 : Reversed.
09h	R	-	**P14/FIDO4~P10/FIDO0** Port 1 Input Data Register (PIR1). Bit 4~0 : P1[4:0] input data register. Bit 7~5 : Reversed.
0Ah	R	-	**P24/BP4~P20/BP0** Port A2 Input Data Register (PIR2). Bit 4~0 : A2[4:0] input data register. Bit 7~5 : Reversed.
0Bh	R	-	**P37/STPCLK#,P36~P30** General-Purpose Port 3 Input Data Register (PIR3).
0Ch	R	-	**P44/VIDI4~P40/VIDI0** Port 4 Input Data register (PIR4). Bit 4~0: P4[4:0] input data register Bit 7~5: Reversed.
0Dh	R	-	**P54/VIDO4~P50/VIDO0** Port 5 Input Data Register (PIR5). Bit 4~0: P5[4:0] input data register. Bit 7~5: Reversed.
0Eh	R	-	**P67~P60** General-Purpose Port 6 Input Data Register (PIR6).
0Fh	R	-	**AD1~AD0, SEL** Bit 0: Operation mode selection (SEL) input. Bit 2~1: Serial bus addresses AD[1:0] configuration input. Bit 7~3: Reversed.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

Port Type Configuration Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
10h	R/W	0Ch	Port 0, 1, 2, 5 Port Type Configuration Register. Bit 7~6 = P5 port type configuration. (Input default) Bit 5~4 = P2 port type configuration. (Input default) Bit 3~2 = P1 port type configuration. (Open-drain default) Bit 1~0 = P0 port type configuration. (Input default) 00 = Input. 01 = Output. 1x = Open-drain.
11h		03h	Port 4 Port Type Configuration Register. Bit 1~0 = P4 port type configuration. 00 = Input. 01 = Output. 1x = Open-drain. (default) Bit 7~2: Reversed.
12h		00h	General-Purpose Port 3 Port Type Configuration Register Low Byte. Bit 7~6 = P3[3] pin type configuration. Bit 5~4 = P3[2] pin type configuration. Bit 3~2 = P3[1] pin type configuration. Bit 1~0 = P3[0] pin type configuration. 00 = Input. (default) 01 = Output. 1x = Open-drain.
13h		00h	General-Purpose Port 3 Port Type Configuration Register High Byte. Bit 7~6 = P3[7] pin type configuration. Bit 5~4 = P3[6] pin type configuration. Bit 3~2 = P3[5] pin type configuration. Bit 1~0 = P3[4] pin type configuration. 00 = Input. (default) 01 = Output. 1x = Open-drain.
14h	R/W	55h	General-Purpose Port 6 Port Type Configuration Register Low Byte. Bit 7~6 = P6[3] pin type configuration. Bit 5~4 = P6[2] pin type configuration. Bit 3~2 = P6[1] pin type configuration. Bit 1~0 = P6[0] pin type configuration. 00 = Input. 01 = Output. (default) 1x = Open-drain.
15h	R/W	55h	General-Purpose Port 6 Port Type Configuration Register High Byte. Bit 7~6 = P6[7] pin type configuration. Bit 5~4 = P6[6] pin type configuration. Bit 3~2 = P6[5] pin type configuration. Bit 1~0 = P6[4] pin type configuration. 00 = Input. 01 = Output. (default) 1x = Open-drain.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

GP Port 3 Output Pulse Width Configuration Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
16h	R/W	00h	General-Purpose Port 3 Output Pulse Width Configuration Register. Bit 1~0 : 11 = 75ms. 10 = 37ms. 01 = 19ms. 00 = 9ms. (default) Bit 7~2 : Reversed.

GP Port3 Interrupt Triggered Condition Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
17h 18h	R/W	FFFFh	Bit 15~14 = P37 interrupt triggered condition register. Bit 13~12 = P36 interrupt triggered condition register. Bit 11~10 = P35 interrupt triggered condition register. Bit 9~8 = P34 interrupt triggered condition register. Bit 7~6 = P33 interrupt triggered condition register. Bit 5~4 = P32 interrupt triggered condition register. Bit 3~2 = P31 interrupt triggered condition register. Bit 1~0 = P30 interrupt triggered condition register. 00: Interrupt asserts only when positive edge occurs. 01: Interrupt asserts only when negative edge occurs. 10: Interrupt asserts when any transition occurs. 11: Disabled. (default)

GP Port3 Normal High Output Configuration Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
19h	R/W	00h	Bit 7 = P37 normal state. Bit 6 = P36 normal state. Bit 5 = P35 normal state. Bit 4 = P34 normal state. Bit 3 = P33 normal state. Bit 2 = P32 normal state. Bit 1 = P31 normal state. Bit 0 = P30 normal state. 0 = Normally low output. 1 = Normally high output.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

GP Port3 Pulse Mode Configuration Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
1Ah	R/W	00h	Bit 7 = P37 pulse mode configuration. Bit 6 = P36 pulse mode configuration. Bit 5 = P35 pulse mode configuration. Bit 4 = P34 pulse mode configuration. Bit 3 = P33 pulse mode configuration. Bit 2 = P32 pulse mode configuration. Bit 1 = P31 pulse mode configuration. Bit 0 = P30 pulse mode configuration. 0 = level mode. (default) 1 = pulse mode. A "1" write to port3 output register will trigger off a pulse at respective pin.

*GP Port3 Interrupt Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
1Bh	R/ WC	00h	GP Port 3 Interrupt Status Register. (STS3) Respective bit will be set if an appointed transition of port occurs. A "1" write can clear bit.

∗GP Port3 Interrupt Configuration Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
1Ch	R/W	02h	Bit 0 = Interrupt function enable bit. 0 = Interrupt function disabled. (default) 1 = Interrupt function enabled. Bit 1 = Interrupt active state. 0 = Interrupt high active (normal low). 1 = Interrupt low active (normal high). (default) Bit 2 = Interrupt output mode. 0 = Open-drain. (default) 1 = Output mode. Bit 7~3 Reversed

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

GP Mode And Test Mode Configuration Register			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
1Dh	R/W	00h	Bit 1 = Port1 Generous-Purpose I/O mode configuration register. Bit 2 = Port2 Generous-Purpose I/O mode configuration register. Bit 4 = Port4 Generous-Purpose I/O mode configuration register. 0 = GPIO mode disable. 1 = GPIO mode enable. When bit is set, respective port will behave like a GPIO port regardless of current CPU mode and status of WatchDog timer. This feature is useful to flexibility of port's utilization especially when only a part of CPU jumpless function (bus ratio or voltage) is employed. *Bit 7 = MS-3 test mode. Test mode is enabled if this bit is set. Bit 0,3,5,6: Reversed.

*General Purpose I/O Port Data and Configuration Reset Mode Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
1Eh	R/W	00h	Port 0~6 Configuration and Output Data Registers Reset Mode: Bit 6 = Port 6 reset mode. Bit 5 = Port 5 reset mode. Bit 4 = Port 4 reset mode. Bit 3 = Port 3 reset mode. Bit 2 = Port 2 reset mode. Bit 1 = Port 1 reset mode. Bit 0 = Port 0 reset mode. If bit is set, respective port's data and configuration register will be reset when I/RST# low, otherwise will not. 0 = I/RST# reset disable. (default) 1 = I/RST# reset enable. Bit 7: Reversed.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

Port Latch Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
1Fh	R	-	Port 0 Latched data Register. (LDR0) The data presented on port 0 can be latched while power-on reset or I/RST# low. Bit 7~5 : Reversed.
20h			Port 3 Latched data Register. (LDR3) The data presented on port 3 can be latched while power-on reset or I/RST# low.
21h			Port 5 Latched data Register. (LDR5) The data presented on port 5 can be latched while power-on reset or I/RST# low. Bit 7~5 : Reversed.
22H			AD[1:0] And SEL Latched data Register. (LDR7) The data presented on AD[1:0] and SEL can be latched while power-on reset or I/RST# low. Bit 0 : SEL. Bit 2~1 : AD[1:0]. Bit 7~3 : Reversed.

∗Latch Mode Configuration Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
23	R/W	0	Bit 0 : LDR0 latch data mode. Bit 1 : Reversed. Bit 2 : Reversed. Bit 3 : LDR3 latch data mode. Bit 4 : Reversed. Bit 5 : LDR5 latch data mode. Bit 6 : Reversed. Bit 7 : LDR7 latch data mode. 0: Data will be latched while power on reset only.(default) 1: Data will be latched while I/RST# is low or power on reset occurs.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

CPU Frequency and Voltage Configuration Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
24h	R/W	00h	Bit 0 : P1[4:0]/FIDO[4:0] output data selection for AMD mode. (BPSel) 0 = Output data presented on P1[4:0]/FIDO[4:0] is passed from P0[4:0]/FIDI[4:0] input directly. (default) 1 = Output datas presented on P1[4:0] / FIDO[4:0] and Port A2[4:0]/BP[4:0] are passed from port 1 output register (POR1). Bit 1 : Reversed. Bit 2 : CPU bus ratio selection for Intel mode. (FIDOSel) 0 = External CPU bus ratio on Port A2[4:0] is passed to P1[4:0]/FIDO[4:0] when P04/ICRST# input is low. (default) 1 = The content of POR1 is passed to P1[4:0]/FIDO[4:0] when P04/ICRST# input is low. Bit 3 : CPU VID selection for Intel and AMD mode. (VIDSel) 0 = Input data from P5[4:0]/VIDI[4:0] is passed to P4[4:0]/VIDO[4:0] directly.(default) 1 = The content of POR4 is passed to P4[4:0]/VIDO[4:0]. ∗Bit 4 : POR4 write control. 0 = The content of POR4 is programmable. (default) 1 = Only the last value written to POR4 can be applied when Power Good Register is written. So that, the new VID value is applied to POR4 only when system is reset by MS-3. Bit 7~5 : Reversed.
25h	R/W	00h	Control Signal Reset Mode. ∗Bit 0 : BPSel reset mode. ∗Bit 1 : Reversed. ∗Bit 2 : FIDOSel reset mode. ∗Bit 3 : VIDSel reset mode. ∗Bit 7~4 : Reversed. 0 = I/RST# reset disable. (default) 1 = I/RST# reset enable.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

WatchDog Configuration Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
26h	R/W	30h	Bit 0 : WatchDog Enable Bit. (WDTEN) 0: Disable. (default) 1: Enable. When WatchDog timer over-flow occurs, this bit will be cleared automatically.
	W		Bit 1 : WatchDog Timer Reset Bit. (WDTRST) When a "1" write to this bit will reset WatchDog timer.
	R/ WC		Bit 2 : WatchDog Timer Overflow Flag. (WDTOV) When WatchDog timer overflow occurs, WatchDog timer will be disabled and a reset pulse will be asserted at pin PWRGD. This means a safer configuration of frequency and voltage for processor will be applied. This bit only can be cleared when a "1" is written to this bit or when power-on reset occurs.
	R/W		*Bit 5~3: WatchDog Timer Selection. (WDTSel) 111 : 9.52s 110 : 4.77s (default) 101 : 2.38s 100 : 1.19s 011 : 600ms 010 : 298ms 001 : 148ms 000 : 74ms
	R/W		*Bit 7~6: PWRGD Output Pulse Width Selection. (WDTPGDSel) 11 : 585ms 10 : 145ms 01 : 36ms 00 : 9ms (default)

WatchDog Timer			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
27	R	0	WatchDog Timer High byte.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

∗STPCLK VID Registers			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
28	R/W	0	Bit 4~0: Stop clock VID register . Bit 5: 0 = Port3[7] is a general-purpose I/O pin. 1 = Port3[7] is a stop clock input pin(STPCLK#). Bit 7~6 : Reversed. This register can be reset while power-on only.

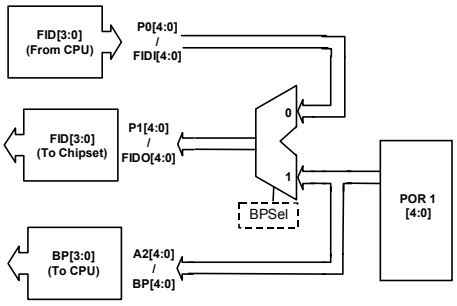
∗Write Mask			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
29	R/W	FF	Control and data registers write mask. This register can be reset while power-on only.

Power Good Register			
INDEX	**R/W**	**DEFAULT**	**REGISTERS DESCRIPTION**
2A	W	00	An any value, any bit write to this register will generate a low pulse at pin PWRGD.

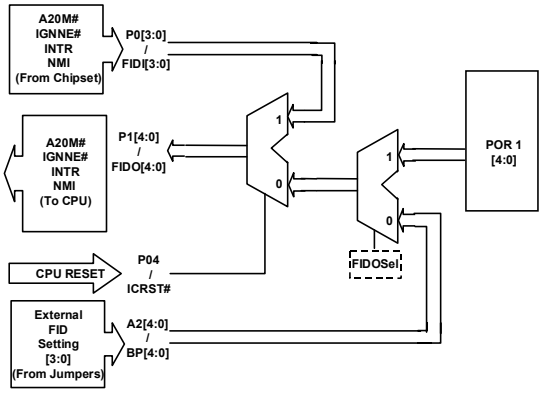
* Register or bit power-on reset only.

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243
Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585

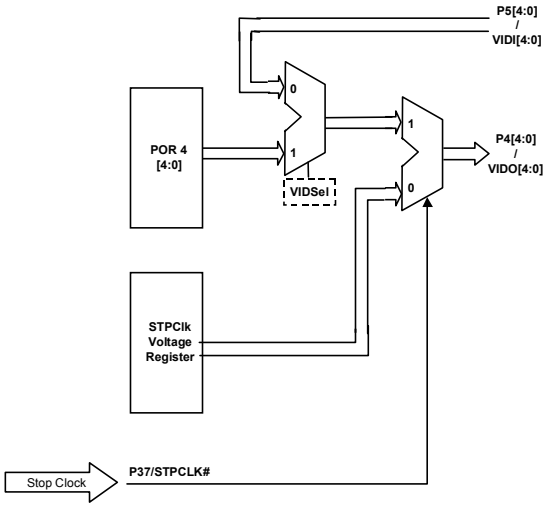
7. MS-3 Functional Block Diagram



MS-3 External Frequency Configuration Diagram For AMD CPU



MS-3 External Frequency Configuration Diagram For Intel CPU



MS-3 External CPU VID Configuration Diagram

Taipei Office:
Tel: (02) 2234-9245
Fax: (02) 2234-9243

Hsin-chu Office:
Tel: (03) 575-2577
Fax: (03) 575-2578 or (03) 575-2585