SANYO

4M-bit (512K x 8) Serial Flash Memory
LE25FW406

■ Outline

LE25FW406 is 512K x 8-bit Serial flash memory by 3.0V single power supply operation, and support serial peripheral interface (S.P.I.). There are two kinds of erase functions, Chip erase, Sector (64K bytes) erase. Moreover, Page program can program the arbitrary data to 1 byte from 256 bytes. Program time is 30us/byte(Typ.), 1.5ms/ 256bytes(Typ.), and high speed. It is best suited for application that requires re-programmable nonvolatile mass storage of program or data memory.

■ Feature

- Read / Write Operation by the 3.0V single power supply are possible: Power Supply Voltage Range 2.7-3.6V
- Clock frequency: 30 MHz / 50MHz (Planning)
- Temperature range: 0 ~ +70 °C / -40 ~ +85 °C (Planning)
- Serial interface: SPI Mode0 and Mode3 correspondence
- Sector size: 64 K bytes / sector
- Sector erase, Chip erase function
- Page program (256 bytes/page)
- Block protection
- A high reliability Read / Write

Endurance cycles:	100,000 times	
Sector erase time:	25ms (Typ.)	0.5s (Max.)
Chip erase time:	250ms (Typ.)	5s (Max.)
Page program time:	40 us/byte (Typ.)	1.5ms/256 bytes (Typ.) 2.5 ms/256 bytes (Max.)

- Status function:

  Ready / busy information, Erase time excess information, Protection information
- Data retention: 10 years
- Package available:

LE25FW406M	SOP8
LE25FW406T	MSOP8
LE25FW406H	VSON8

Figure 1: Pin Assignment

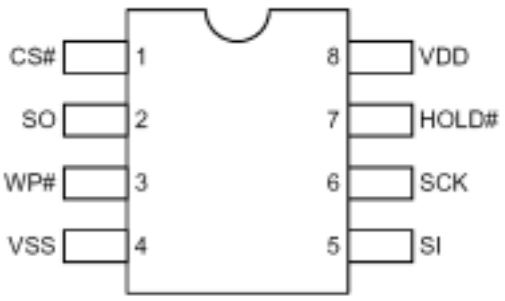

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Figure 2: Block diagram

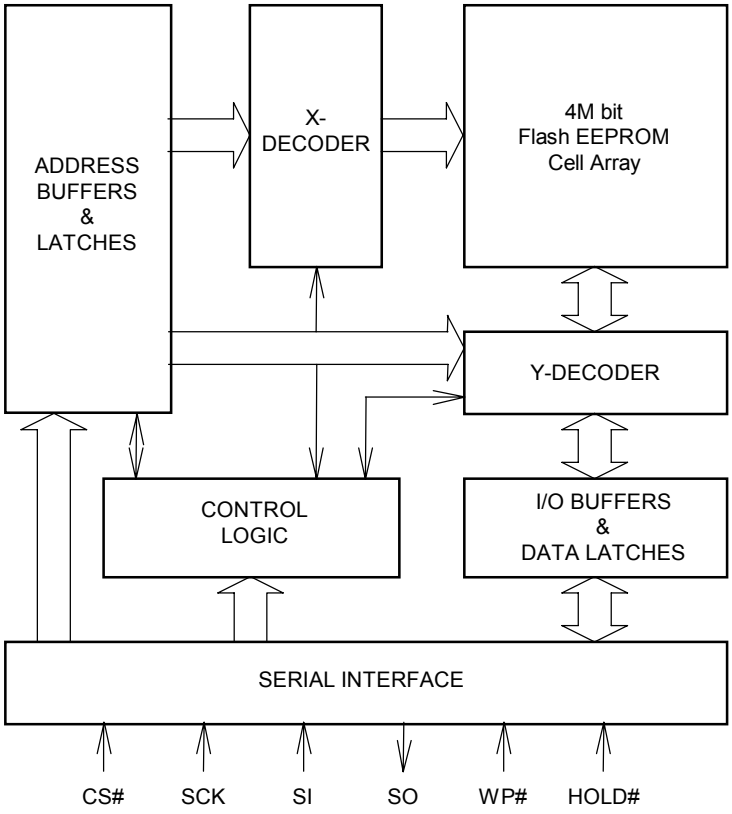


Table 1: Pin Description

Symbol	Pin Description	Function
SCK	Serial clock	To control the timing of serial data input and output. To latch input data and addresses synchronously at the rising edge of SCK, and read out Output data synchronously at the falling edge.
SI	Serial data input	To input data or addresses serially from MSB to LSB (Least Significant Bit).
SO	Serial data output	To output data serially from MSB to LSB.
CS#	Chip select	To activate the device when this pin is LOW. To deselect and put the device to standby mode when this pin is HIGH.
WP#	Write-protect	To write-protect the Block Protect bits (BP0, BP1, BP2) and the Status Register Write Protect bit (SRWP) of the Status Register in co-operation with the Status Register Write Protect bit (SRWP).
HOLD#	Hold	To pause any serial communications with the device without deselecting the device.
VDD	Power supply	To provide from 2.7V to 3.6V supply
VSS	Ground	

Table 2: Commands Summary

Command	The 1st bus cycle (OP-code)	The 2nd bus cycle	The 3rd bus cycle	The 4th bus cycle	The 5th bus cycle	The 6th bus cycle	The n-th bus cycle
Read	03h	A23-A16	A15-A8	A7-A0			
	0Bh	A23-A16	A15-A8	A7-A0	X		
Sector erase	D8h	A23-A16	X	X			
Chip erase	C7h						
Page program	02h	A23-A16	A15-A8	A7-A0	PD *1	PD *1	PD *1
Write Enable	06h						
Write disable	04h						
Power down	B9h						
Status register Read	05h						
Status register Write	01h	DATA					
Software reset	FFh						
Read ID	ABh	X	X	A7-A0 *2			
Release from power down							

Definition of Table 2:
X = don't care, h = hexadecimal notation, A23~A19 are don't care for all commands
*1. PD: page program data. The arbitrary numbers of data of 1~256 bytes of byte unit for input.
*2. Read ID A7~A1 are don't care. A read cycle from address A0='0' outputs the manufacture code (SANYO: 62h). A read cycle at address A0='1' outputs the device code (07h).

Table 3: Status register

Bit	Name	Logic	Function	Default at Power up
Bit0	RDY#	0	Ready state	0
		1	A erase / program state	
Bit1	WEN	0	Write prohibition state	0
		1	Write possible state	
Bit2	BP0	0	The block protect information Reference status registers	Non-volatile information
		1		
Bit3	BP1	0		Non-volatile Information
		1		
Bit4	BP2	0		Non-volatile Information
		1		
Bit5	ERROR	0	Erase / Program normal operation / normal end	0
		1	Erase / Program time excess state	
Bit6			Reserve bit	0
Bit7	SRWP	0	Status register Write enable state	Non-volatile Information
		1	Status register Write disable state	

Device operation

LE25FW406 is the product that supports the serial interface, and has the electric on-chip erase by the 3.0V single power supply and the function of standard EPROM for industrial. The interface and control are made easily by building a command register in a chip. Reading, erasing, programming, and a function required in addition to them are performed through a command register.

The address and data of command are latched for program and erase operation.

Figure3 and figure4 indicate the timing waveform of serial input and output.

While CS# is LOW, the device will be chosen and the input of a command, an address, etc. can be attained serially. Those inputs are performed from Bit7 (MSB) synchronizing with the rising edge of SCK. At this time, an output terminal (SO) is in a high impedance state.

It is that an output terminal (SO) will be in a low impedance state at the time of a Read, a status register Read, and Silicone ID, and data is outputted from Bit7 (MSB) synchronizing with falling edge of a clock.

LE25FW406 support the both sides of serial interface SPI mode0 and SPI mode3. In case CS# falling edge, if SCK is in a logic low level state and it is in SPI mode0, and if a high level state, SPI mode3 will be chosen automatically.

Command definition

Table2 contains a command list and a brief summary of the commands. The following is a detailed description of the options initiated by each command.

1. Read

Figure5 shows timing waveform of a Read operation.

There are two kinds of Read commands, 4th bus Read and 5th bus Read. The 4th bus read is constituted from the 1st bus cycle to the 4th bus cycle. If 24-bit address is inputted after OP-code (03h), the data of the specified address will be outputted synchronizing with SCK. A data is outputted from the falling edge clock of the 4th bus cycle Bit0.

5th bus Read is constituted from the 1st bus cycle by the 5th bus cycle, which consists of 24 bits address and 8-bit dummy bit after OP-code (0Bh). The data is outputted from the falling edge clock of the 5th bus cycle Bit0. The only one difference between these two commands is with or without a dummy bit input (5th bus cycle).

While having inputted SCK, the increment of the address is automatically carried out inside a device, and data is outputted in order until the top address (7FFFFh) up to. If the data is outputted and the input of SCK continues still more, it returns to the lowest address (00000h) and a data output is continued.

By making CS# into a logic high level, a device is deselecting, and read cycle is ended. Output terminal will be in a high impedance state.

2. Status Register

The status register's contents are shown in Table3.

The status register can perform detection state of a device and setup of protection.

2-1. Status register read

The status register's contents can be read by status register read, moreover it can read also during the following operation.

- Sectors erase
- Chips erase
- Page program
- Status register Write

Figure6 shows timing waveform of a status register Read.

Status register command consists of only the 1st bus, If OP-code (05h) dose writes in, synchronizing with falling edge of SCK, the status register's contents will be outputted from SRWP (Bit7).

If the data is outputted until RDY# (Bit0), and also SCK input continues still more, it returns to SRWP and data output is continued. Data is outputted from the falling edge clock of the 1st bus cycle Bit0.

Status register Read can be read always (also in case of inside of program cycle or erase cycle).

2-2. Status register Write

By Status register Write, BP0, BP1, BP2 and SRWP can be rewritten. BSY#, WEN, ERROR, and Bit6 are read-only, BP0, BP1, BP2 and SRWP are non-volatile.

A timing waveform is shown in Figure7 and a flow chart is shown in Figure18.

Status register Write command consists of the 1st bus cycle and the 2nd bus cycle, and internal Write operation starts with the rising edge of CS# after inputting data after OP-code (01h). Erase and program are automatically performed inside the device and a Status register Write rewrites BP0, BP1, BP2 and SRWP non-volatilized data. The write-in data to read-only bits (RDY#, WEN, ERROR, Bit 6) are don't care.

The end of a status register Write is detectable with RDY# of a status register Read.

The number of times of rewriting of a status register Write is 10,000 times (Min).

In order to perform a status register Write, it is necessary to change WEN of a status register into "1" state for WP# pin.

RDY#(Bit0)

The end of a Write (program, erase, status register Write) is detectable with RDY#. If device is in a busy state RDY# is in "1", and the Write will be ended in "0" states.

WEN (Bit1)

It is detectable whether a Write is possible with WEN. If WEN is in "0" state, even if it inputs a Write command, Device will not perform write operation. If WEN is in "1" state, Write is possible to the area by which block protection is not carried out.

WEN is controllable with a Write Enable command and a Write disable command. WEN will be in "1" state with a Write Enable command (06h), and will be in "0" states with a Write disable command (04h).

Moreover, in the following state, automatically, WEN will be in "0" states and an unprepared Write will be prevented.

- At the time of a power-up
- After sector erase, or chip erase is completed
- After a page program is completed
- After a status register Write is completed

BP0, BP1, BP2 (Bit 2,3,4)

Block protection BP0, BP1 and BP2 can set up the memory address area to be protected. Refer to Table 4 for setting conditions.

Table 4: Protection level setting conditions

Protection level	Status register bit			Protection area
	BP2	BP1	BP0	
0 (all area unprotect)	0	0	0	Nothing
1 (1/8 protection)	0	0	1	70000h-7FFFFh
2 (1/4 protection)	0	1	0	60000h-7FFFFh
3 (1/2 protection)	0	1	1	40000h-7FFFFh
4 (all area protection)	1	0	0	00000h-7FFFFh
4 (all area protection)	1	0	1	00000h-7FFFFh
4 (all area protection)	1	1	0	00000h-7FFFFh
4 (all area protection)	1	1	1	00000h-7FFFFh

* A chip erase is possible only when a protection level is 0.

ERROR (Bit5)

Erase / Program time excess flag ERROR will be in "1" state, if an erase / program exceeds regulation marginal time. The regulation marginal time of page program is 10ms (Typ.), sector erase is 2s (Typ.), and chip erase is 10s (Typ.). If an erase / program exceeds regulation marginal time, a device will be locked and an erase / program will not end it automatically (it continues being in a busy state). In order to make it end, it is necessary to perform software reset.

SRWP (Bit7)

Status register Write protection SRWP protects status register. When "1" state and WP# pin are logic low levels, as for a status register Write command, they are disregarded, and as for BP0, BP1 and BP2 of a status register, and SRWP is protected. When WP# pin is a logic high level, a status register is not protected irrespective of the state of SRWP. SRWP setting conditions are shown in Table 5.

Table 5: SRWP setting conditions

WP# pin	SRWP	Status register protection state
0	0	Unprotect
	1	Protection
1	0	Unprotect
	1	Unprotect

Bit6 are reserve bit.

3. Write Enable

Write Enable sets a status register WEN to "1" state. In order to perform the following operation, it is necessary to execute a Write Enable command first.

- Sector erase
- Chip erase
- Page program
- Status register Write

Figure8 shows timing waveform. A Write Enable command consists of only the 1st bus cycle. OP-code is 06h.

4. Write disable

Write disable sets a status register WEN to "0" states, and forbids an unprepared Write.

Figure9 shows timing waveform. Write Enable command consists of only the 1st bus cycle. OP-code is 04h.

To release from a Write disable state (WEN "0"), it should be performed the Write Enable command (06h).

5. Power Down

Power down states carry out the prohibition state of all the commands except Read ID and power down release command.

Figure10 shows timing waveform. Power down command consists of only the 1st bus cycle. OP-code is B9h.

For release from power down mode, Power down release command performs to abort.

Figure11 shows release from power down timing waveform. And figure15 shows Read ID timing waveform.

6. Sector Erase

Sector erase changes the memory cell data of arbitrary sectors into "1" state. A sector consists of 64 K bytes.

Figure12 shows timing waveform and a flow chart is shown in Figure19

Sector erase command is constituted from the 1st bus cycle to the 4th bus cycle, 24-bit address after OP-code (D8h). As for the address, A18 - A16 are effective, and the rest is don't care.

Erase operation begins from the rising edge of CS# after a command input end, and it ends automatically by control of an internal timer. Moreover, the end of an erase is detectable by using status register.

However, when it becomes an excess of an erase time (a status register ERROR is "1" state), sector erase mode is not ended automatically. In order to make it end, it is necessary to perform software reset input.

7. Chip Erase

Chip erase changes the memory cell data of all sectors into "1" state.

Figure13 shows timing waveform and a flow chart is shown in Figure20.

Chip erase command consists of only the 1st bus cycle. OP-code is C7h. After a command input end, by the rising edge of CS#, erase operation starts and it ends automatically by control of an internal timer. Moreover, the end of an erase is detectable by using status register.

However, when it becomes an excess of an erase time (a status register ERROR is "1" state), chip erase mode is not ended automatically. In order to make it end, it is necessary to perform software reset input.

8. Page program

Page program can program the arbitrary numbers of bytes of 1 to 256 bytes into the sector erased in advance.

Figure14 shows timing waveform and a flow chart is shown in Figure20.

24-bit address is inputted after OP-code (02H). As for an address A18-A0 are effective. Then, loading is possible for program data during CS# is low. When the data loaded exceeds 256 bytes, 256 bytes loaded at the end are programmed.

It is necessary to load program data per byte, and when it programs by loading the data below a byte unit, a normal page program is not performed.

For page program time, it is dependent on the amount of data, and if data is 32 bytes or under, program time is 30 us/byte (Typ.). In case of more than 32 bytes, program time is 1.5ms (Typ.).

However, when it becomes an excess of an program time (a status register ERROR is "1" state), page program mode is not ended automatically. In order to make it end, it is necessary to perform software reset input.

9. Read ID

Read ID can read the information on a manufacturer code and a device code.

Figure15 shows timing waveform and the silicone ID code table is shown in Table 6.

Read ID command is constituted from the 1st bus cycle to the 4th bus cycle. An address of 16bit dummy bit and 8 bits is inputted after OP-code (ABh), it can read Silicone ID. In address A0 ="0", A manufacturer code is read for 62h by the 5th bus cycle, and device code is read for 07h by the 6th bus cycle. When SCK input still continues more, manufacturer code and a device code are outputted by turns in bus cycle. In address A0 ="1", read-out begins from 07h of a device code in the 5th bus cycle.

Read ID cannot perform under write execution.

Table 6: The silicone ID code table

	Address A0	Output code
Manufacturer code	0	62h
Device code	1	07h

A data output is outputted from the falling edge clock of the 4th bus cycle Bit0, it is making CS# into a logic high level, and a Read ID is ended.

10. Software Reset

Software reset can release from an erase or program time excess state.

The timing waveform of software reset is shown in Figure16.

Software reset command consists of only the 1st bus cycle. OP-code is FFh. After a command input end, if CS# is rising edge, it will be reset.

It resets ERROR of status register information.

11. Hold function

HOLD# pin is used in order to pause serial communication (hold state).

The timing waveform is shown in Figure17.

If HOLD# starts to falling edge in the timing SCK on a logic low level, device will be in a hold state. And if HOLD# starts to rising edge, Device will release from hold state in same timing.

Changes of HOLD# are forbidden when CLK is High level.

If it is effective when CS# is a logic low level, and when CS# is rising edged, it will release from a hold state and serial communication will be reset.

In a hold state, SO is Hi-Z, SI and SCK is Don't Care.

12. Hardware data protection

In order to prevent the unprepared writing at power-up, LE25FW406 have the power-on reset function inside.

13. Decoupling capacitor

Ceramic capacitors (0.1uF) must be added between VDD and VSS to each device to assure stable flash memory operation.

Absolute Maximum Stress Ratings

Storage Temperature ..... -55 °C ~ 150 °C
Supply Voltage ..... -0.5 V ~ 4.6 V
D.C. Voltage on Any Pin to Grand Potential .....-0.5 V ~ VDD + 0.5 V

Operating Range

Ambient Temperature .....0 °C ~ 70 °C / -40 °C ~ 85 °C (Planning)
VDD .....2.7 V ~ 3.6 V

DC Operating Characteristics

Symbol	Parameter	Limit		Unit	Test Conditions
		Min.	Max.		
ICCR	Power Supply Current (Read)		4	mA	CS# = VIL, HOLD# = WP# = VIH, SO = open, SI = VIL/VIH, clock frequency = 25 MHz, VDD = VDD Max
			6	mA	CS# = VIL, HOLD# = WP# = VIH, SO = open, SI = VIL/VIH, clock frequency = 30 MHz, VDD = VDD Max
			8	mA	CS# = VIL, HOLD# = WP# = VIH, SO = open, SI = VIL/VIH, clock frequency = 50 MHz, VDD = VDD Max
ICCW	Power Supply Current (Write)		15	mA	VDD = VDD Max.
ISB1	TTL standby current		3	mA	CS# = HOLD# = WP# = VIH and SO = open, SI = VIH/VIL, VDD = VDD Max
ISB2	CMOS standby current		5	µA	CS# = HOLD# = WP# = VDD - 0.3V and SO = open, SI = VIH/VIL, VDD = VDD Max
ILI	Input Leakage Current		2	µA	VIN = VSS - VDD, and VDD = VDD Max
ILO	Output Leakage Current		2	µA	VIN = VSS - VDD, and VDD = VDD Max
VIL	Input Low Voltage	- 0.3	0.3VDD	V	VDD = VDD Max.
VIH	Input High Voltage	0.7VDD	VDD + 0.3	V	VDD = VDD Min.
VOL	Output low Voltage		0.2	V	IOL = 100 uA, VDD = VDD Min.
			0.4		IOL = 1.6 mA, VDD = VDD Min.
VOH	Output High Voltage	VDD - 0.2		V	IOH = - 100 uA, VDD = VDD Min.

Power-up Timing

Symbol	Parameter	Min.	Units
tPU_READ	Power-up to Read Operation	10	ms
tPU_WRITE	Power-up to Write Operation	10	ms

Capacitance (Ta = 25 °C, f = 1 MHz)

Symbol	Description	Max.	Unit	Test Condition
CDQ	DQ Pin Capacitance	12	pF	VDQ = 0V
CIN	Input Capacitance	6	pF	VIN = 0V

Note: These parameters are periodically sampled and are not 100% tested.

AC characteristic (fCLK=30MHz Operation)

Symbol	Parameter	Limit			Unit
		Min.	Typ.	Max.	
fCLK	Clock frequency			30	MHz
tRF	Input rising, falling time			20	ns
tCSS	CS# Setup time	10			ns
tCSH	CS# Hold time	10			ns
tCPH	CS# Standby pulse width	25			ns
tCHZ	CS# to High-Z output			15	ns
tDS	Data Setup time	5			ns
tDH	Data Hold time	5			ns
tCLS	SCK Setup time	10			ns
tCLH	SCK Hold time	10			ns
tCLHI	SCK High pulse width	16			ns
tCLLO	SCK Low pulse width	16			ns
tCLZ	SCK to Low-Z output	0			ns
tV	SCK to output valid		8	15	ns
tHO	Output data hold time	0			ns
tSE	Sector erase cycle time		0.025	0.5	s
tCHE	Chip erase cycle time		0.25	5	s
tPP	Page program cycle time per byte (1 byte - 32 bytes)		40	50	us
	Page program cycle time (33 bytes - 256 bytes)		1.5	2.5	ms
tSRW	Write status register cycle time		5	15	ms
tWPS	WP# Setup time	20			ns
tWPH	WP# Hold time	20			ns
tRB	Reset recovery time			100	ns
tPRB	Power down recovery time			25	ns
tHS	HOLD# Setup time	7			ns
tHH	HOLD# Hold time	3			ns
tHHZ	HOLD# Low to High-Z Output			9	ns
tHLZ	HOLD# High to Low-Z Output			9	ns

AC Test Conditions

Input Pulse Level ..... 0 V, 3.0 V
Input Rise/Fall Time .....5 ns
Input/Output Timing Level .....1/2 × VDD
Output Load ……..... 30 pF

AC characteristic (fCLK=50MHz Operation)

Symbol	Parameter	Limit			Unit
		Min.	Typ.	Max.	
fCLK	Clock frequency			50	MHz
tRF	Input rising, falling time			20	ns
tCSS	CS# Setup time	8			ns
tCSH	CS# Hold time	8			ns
tCPH	CS# Standby pulse width	25			ns
tCHZ	CS# to High-Z output			8	ns
tDS	Data Setup time	2			ns
tDH	Data Hold time	5			ns
tCLS	SCK Setup time	5			ns
tCLH	SCK Hold time	5			ns
tCLHI	SCK High pulse width	9			ns
tCLLO	SCK Low pulse width	9			ns
tCLZ	SCK to Low-Z output	0			ns
tV	SCK to output valid			9	ns
tHO	Output data hold time	0			ns
tSE	Sector erase cycle time		0.025	0.5	s
tCHE	Chip erase cycle time		0.25	5	s
tPP	Page program cycle time per byte (1 byte - 32 bytes)		40	50	us
	Page program cycle time (33 bytes - 256 bytes)		1.5	2.5	ms
tSRW	Write status register cycle time		5	15	ms
tWPS	WP# Setup time	20			ns
tWPH	WP# Hold time	20			ns
tRB	Reset recovery time			100	ns
tPRB	Power down recovery time			25	ns
tHS	HOLD# Setup time	7			ns
tHH	HOLD# Hold time	3			ns
tHHZ	HOLD# Low to High-Z Output			9	ns
tHLZ	HOLD# High to Low-Z Output			9	ns

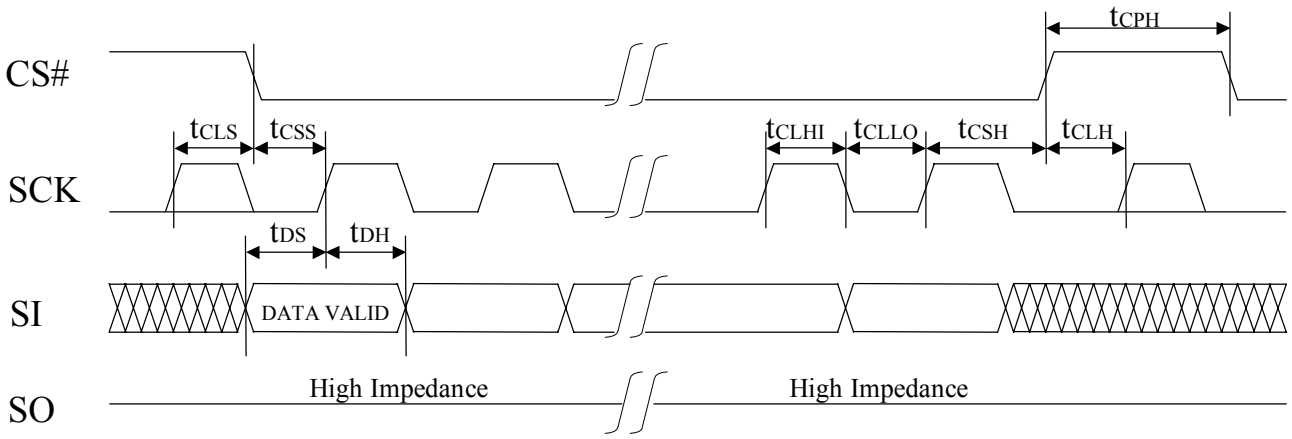
AC Test Conditions

Input Pulse Level ..... 0 V, 3.0 V
Input Rise/Fall Time .....5 ns
Input/Output Timing Level .....1/2 × VDD
Output Load ……..... 30 pF

Timing waveforms

Figure 3: Serial Input Timing Diagram

(SPI Mode 0)



(SPI Mode 3)

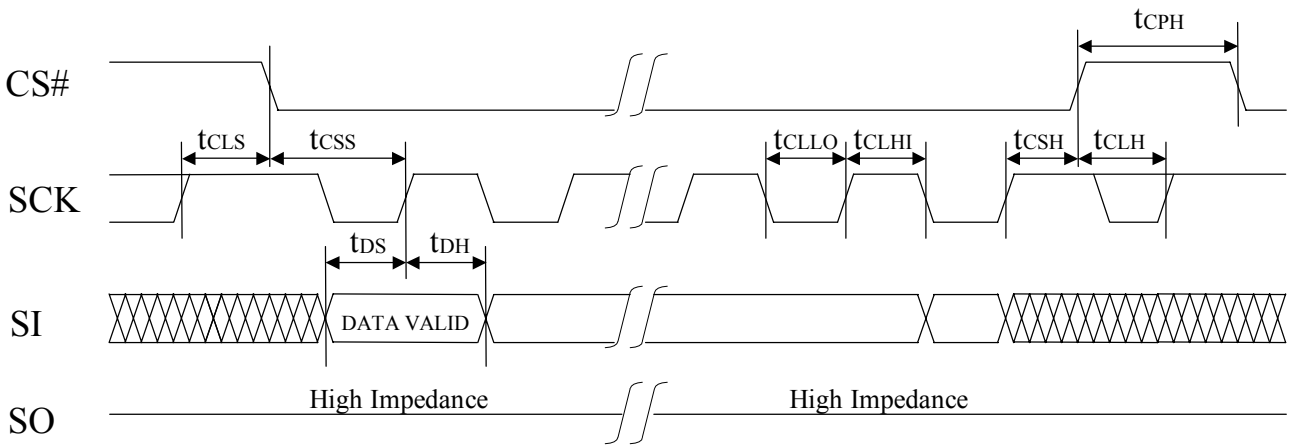
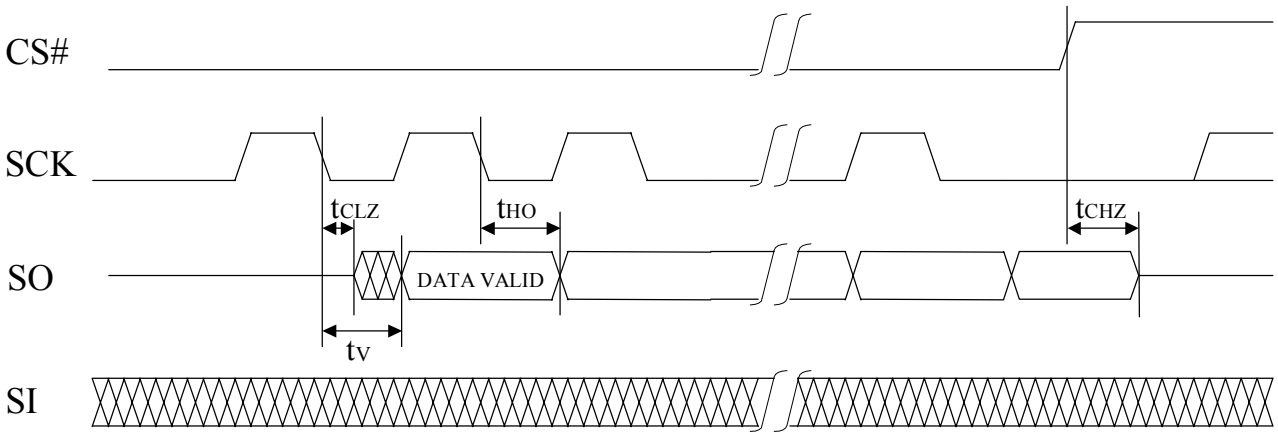


Figure 4: Serial Output Timing Diagram

(SPI Mode 0)



(SPI Mode 3)

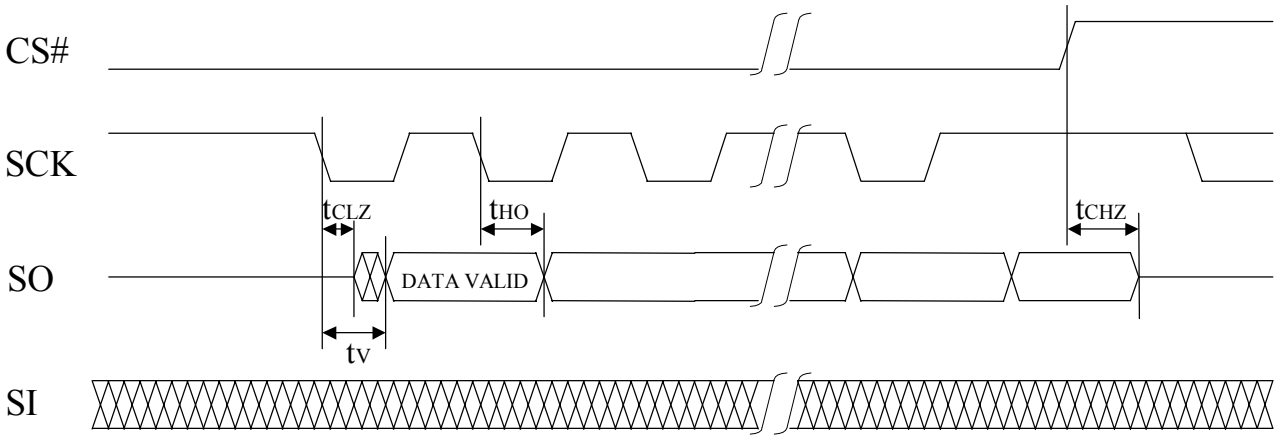
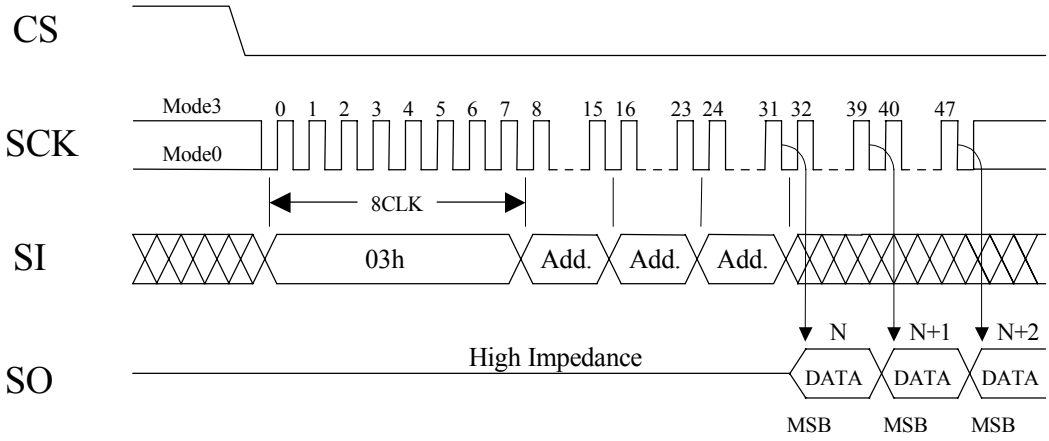


Figure 5: Read Cycle Timing Diagram

4th bus Read



5th bus Read

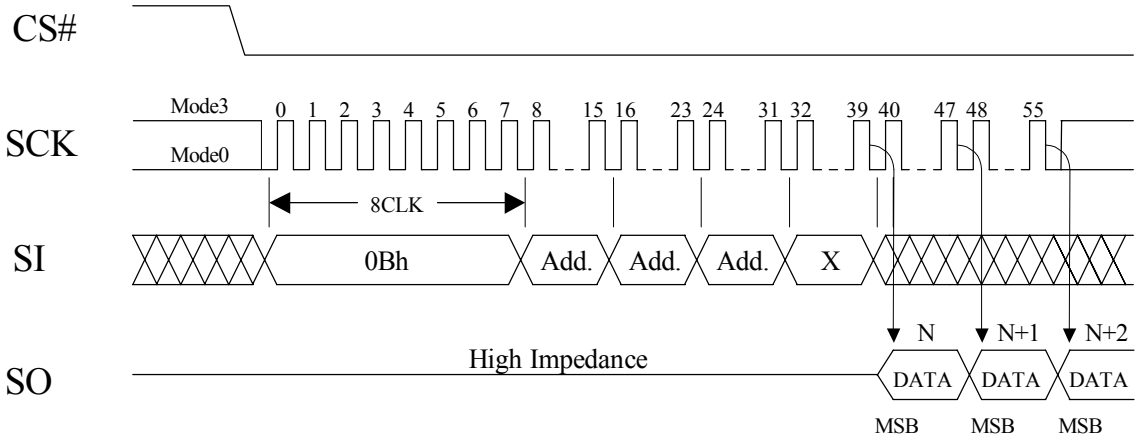


Figure 6: Read Status Register Diagram

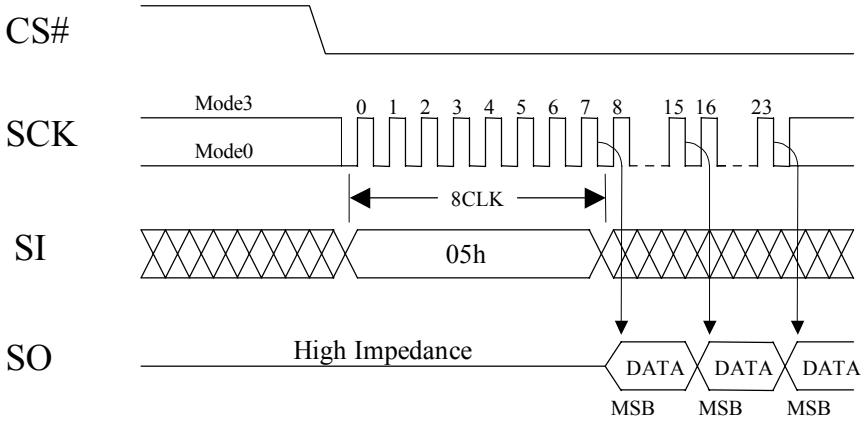


Figure 7: Write Status Register Diagram

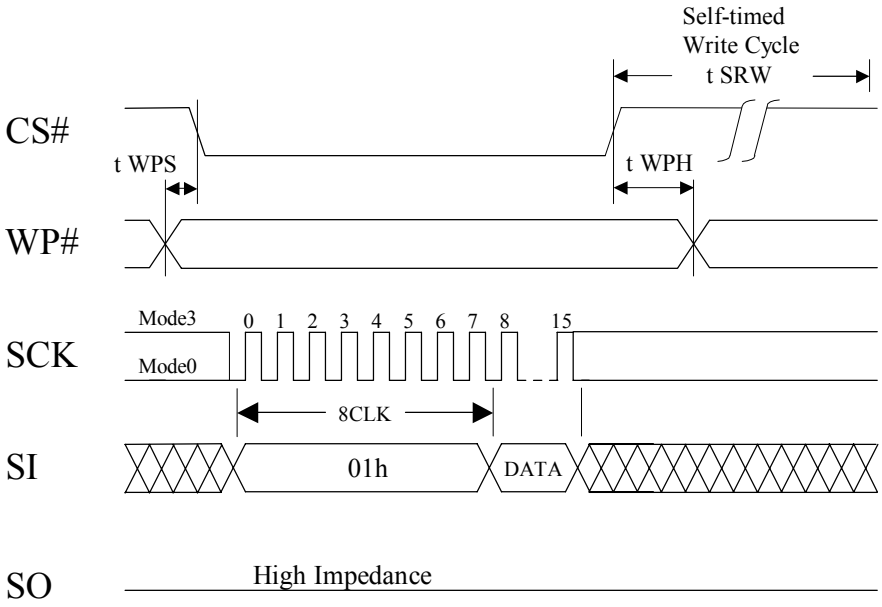


Figure 8: Write Enable Diagram

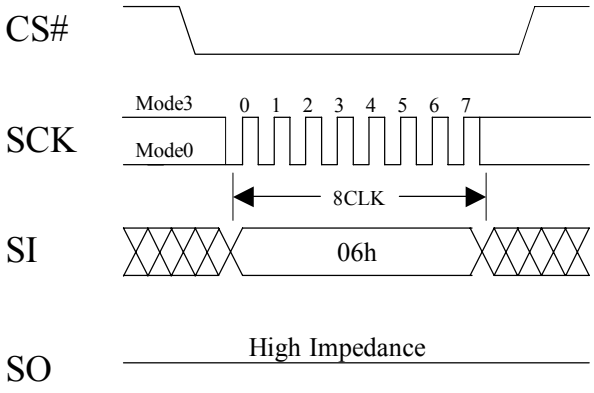


Figure 9: Write Disable Diagram

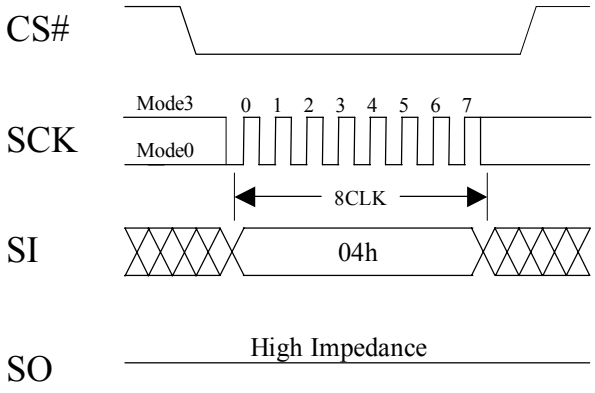


Figure 10: Power Down Diagram

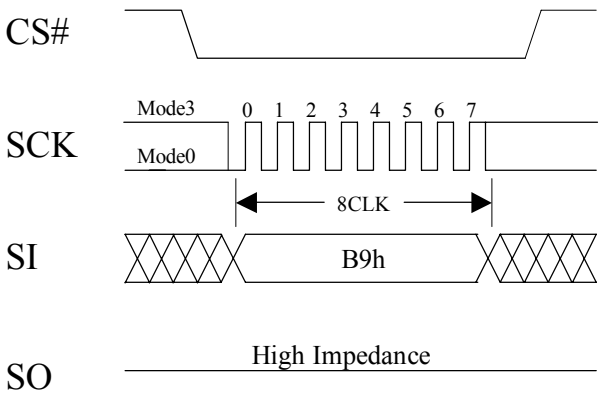


Figure 11: Escape From Power Down Diagram

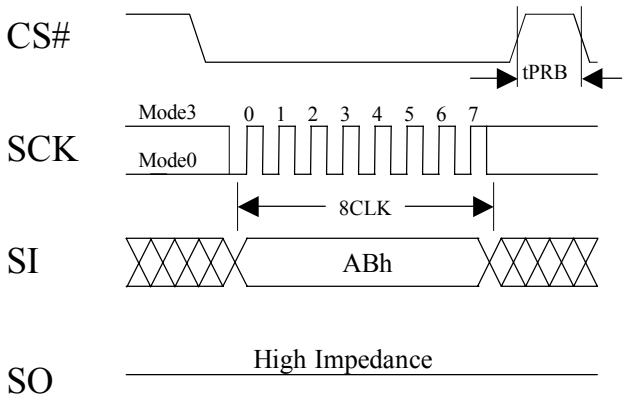


Figure 12: Sector Erase Diagram

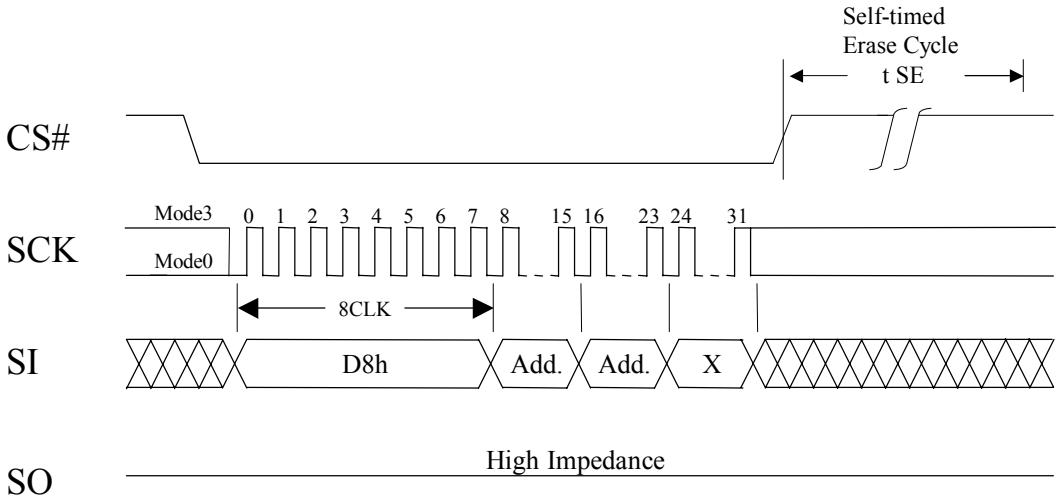


Figure 13: Chip Erase Diagram

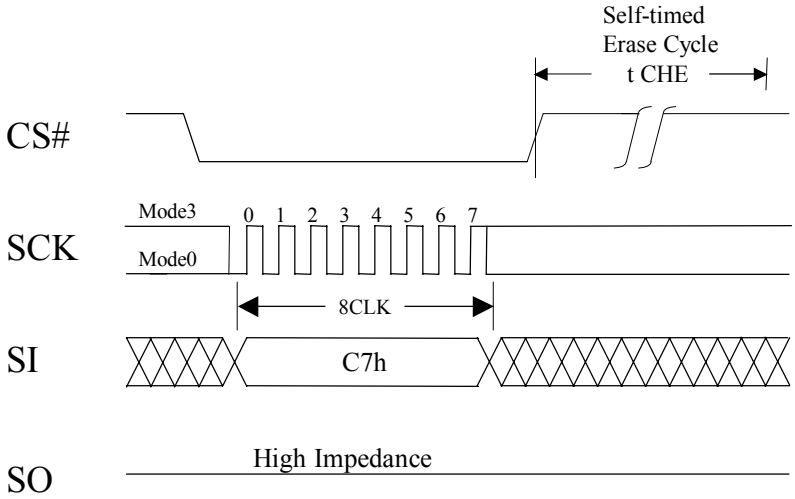


Figure 14: Page Program Diagram

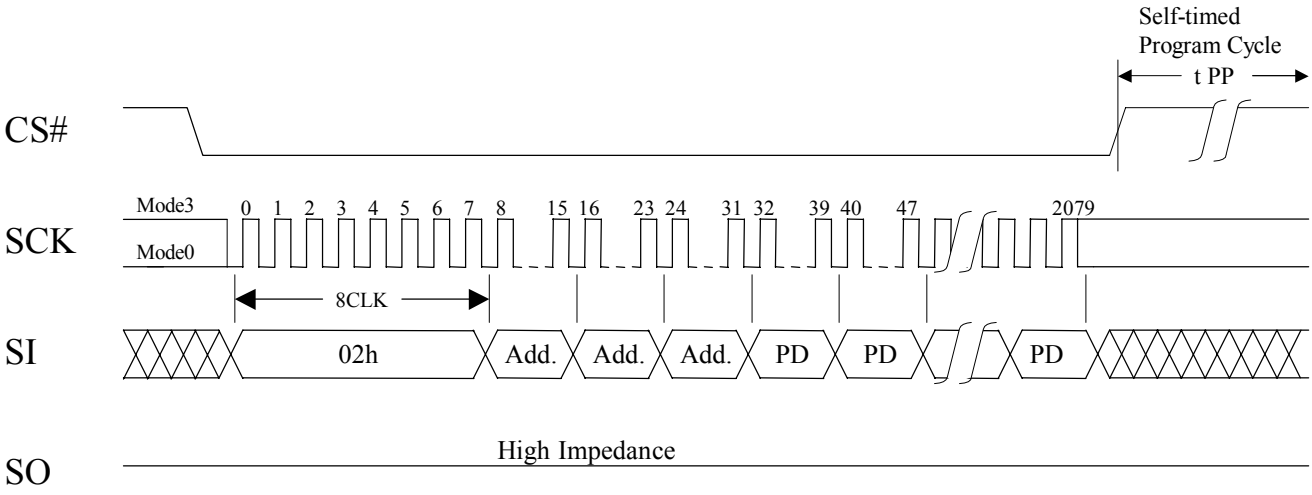


Figure 15: Read ID Diagram

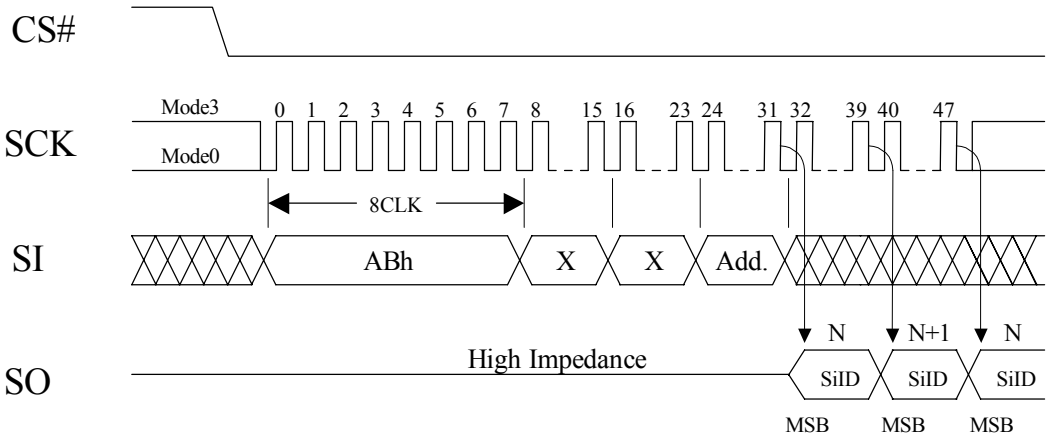


Figure 16: Software Reset Timing Diagram

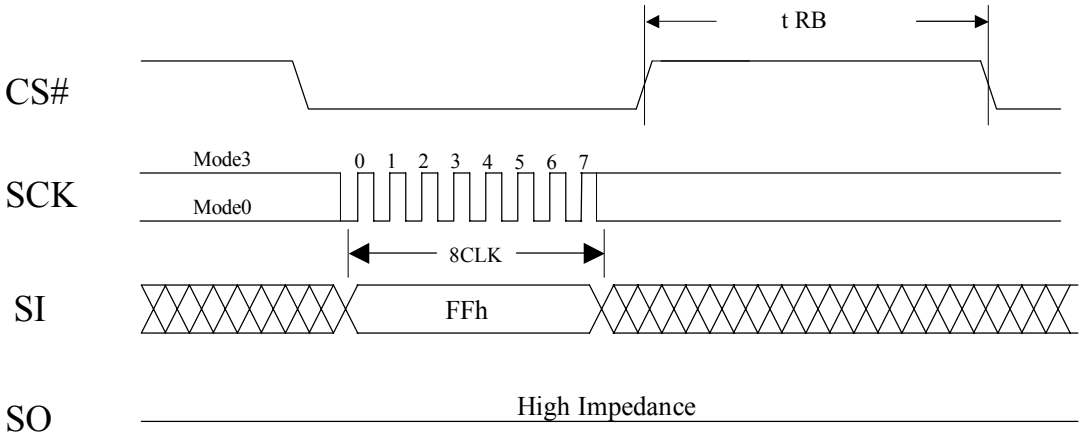


Figure 17: Hold Command Diagram

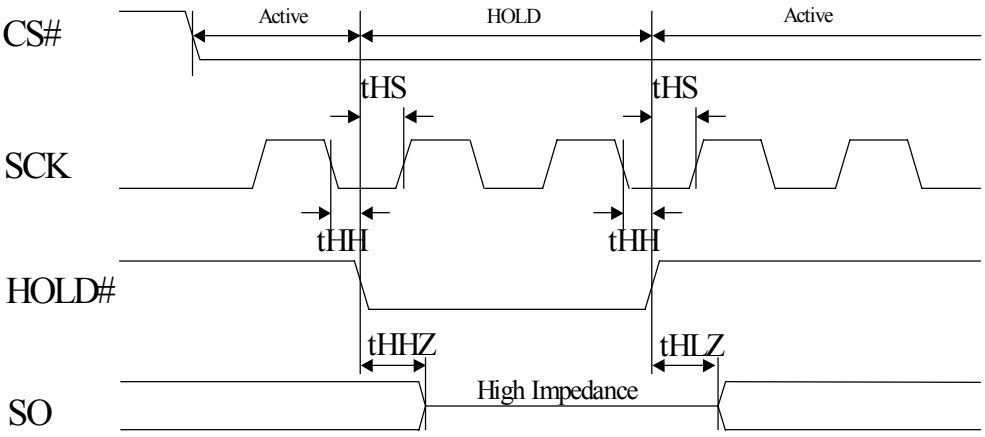
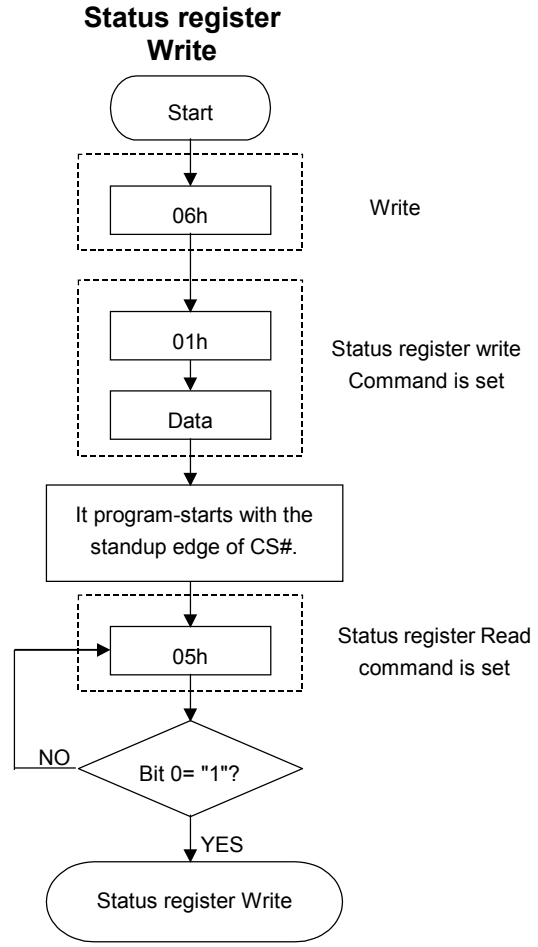


Figure 18: Status Register Write Flow Chart



It becomes a Write Disable automatically after status register Write end.

Figure 19: Erase Flow Chart

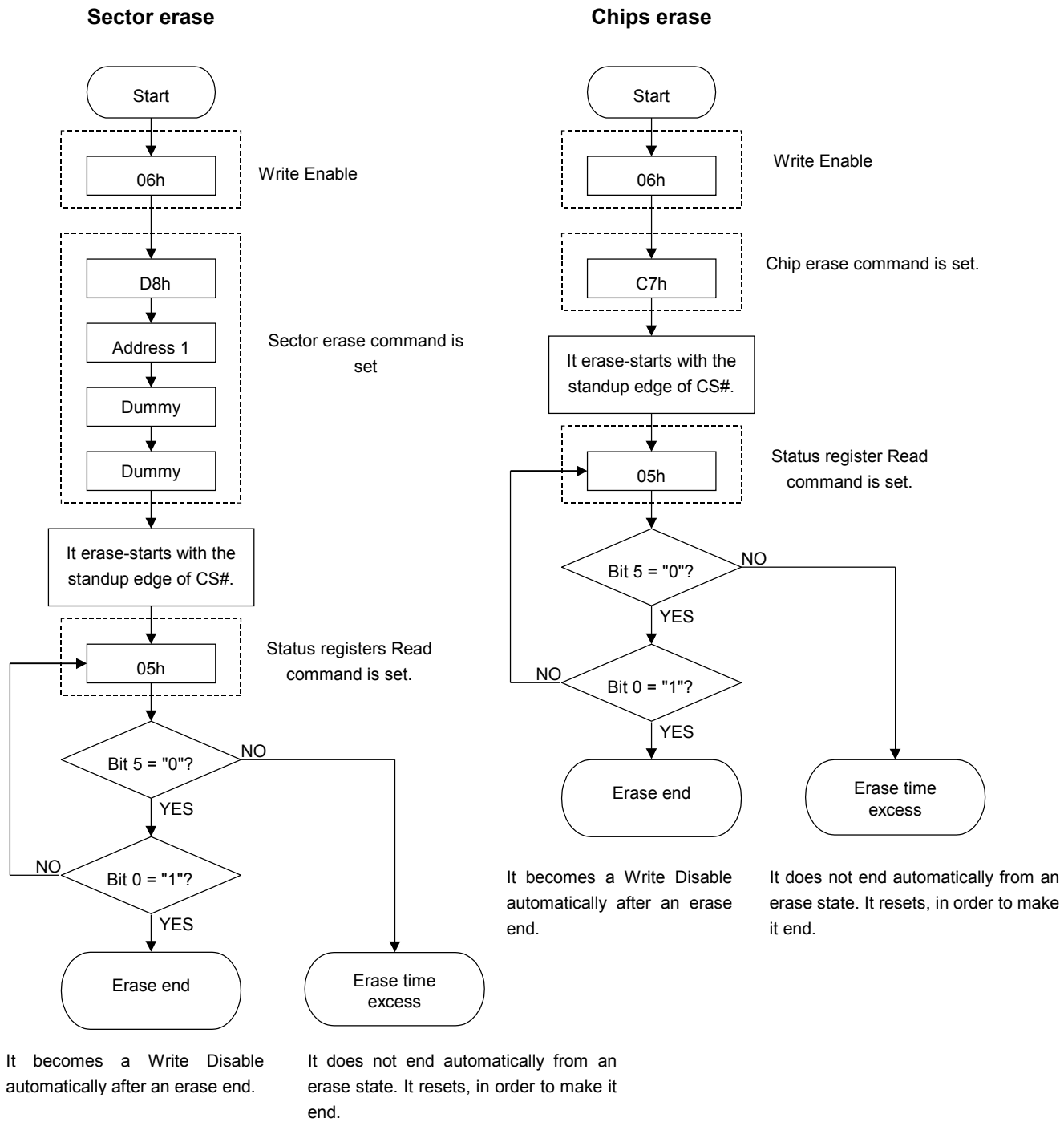
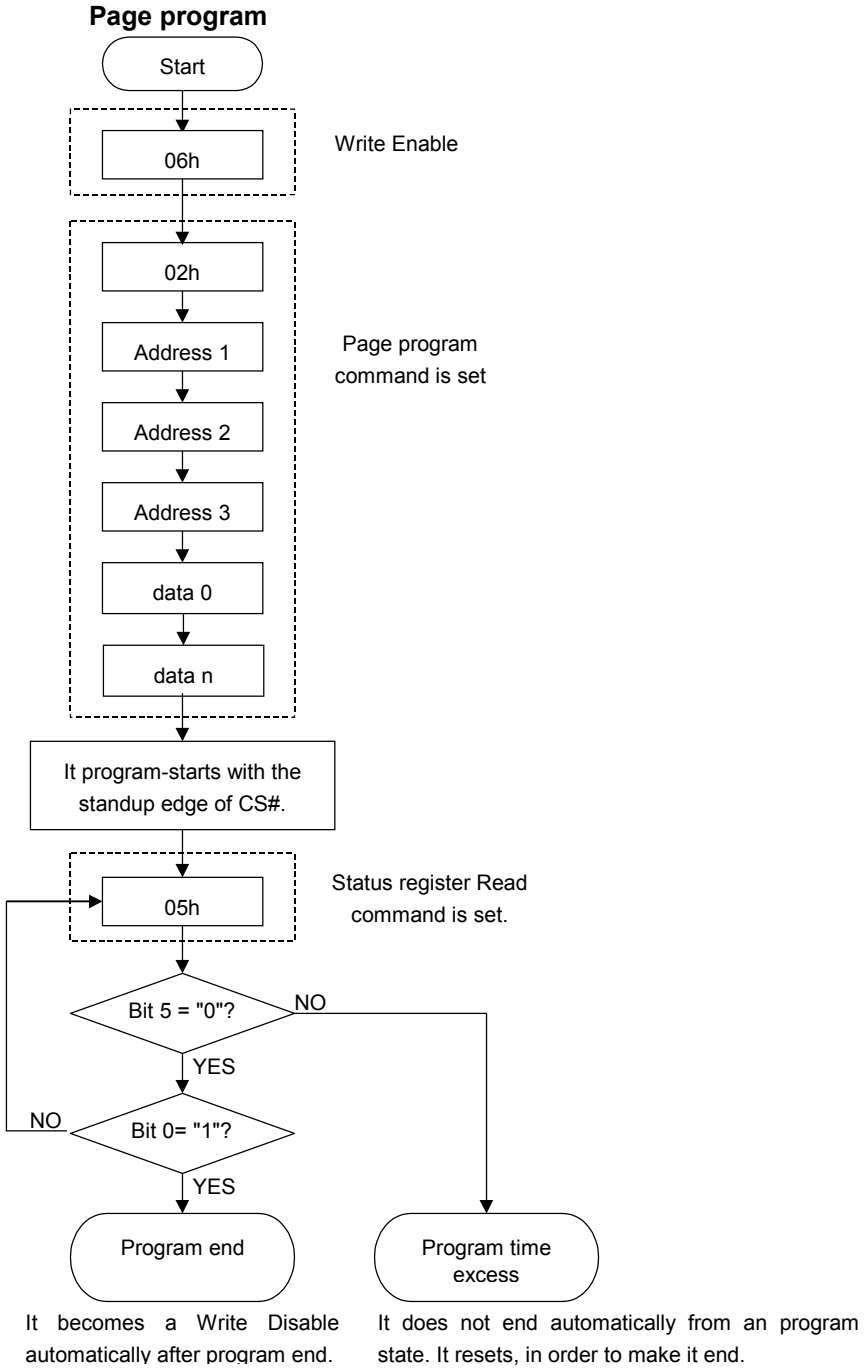


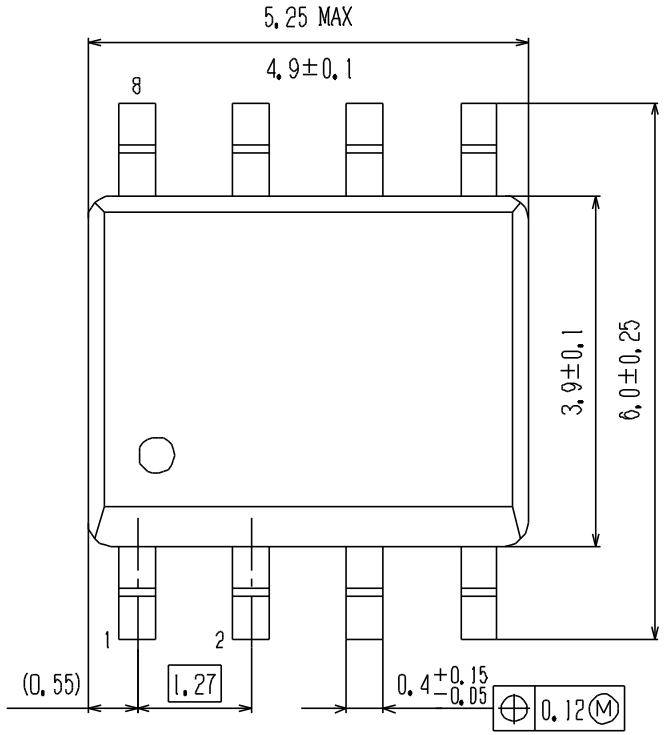
Figure 20: Program Flow Chart

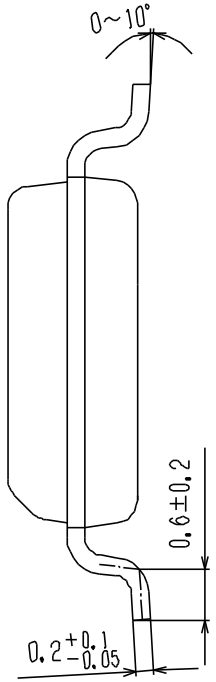


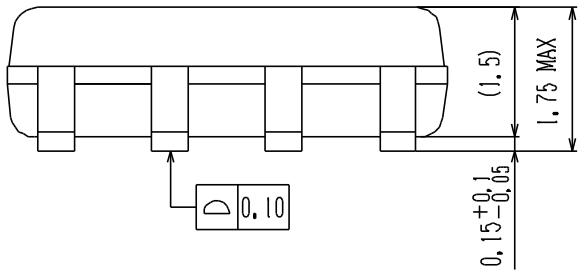
OUTLINE DRAWING

SANYO

SANYO Package Code	JEITA Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass(g)	Measure	Unit
SOP8(3.9X4.9)X01	———	———	———	———	———	12/1	mm







TENTATIVE

REVISION : 1

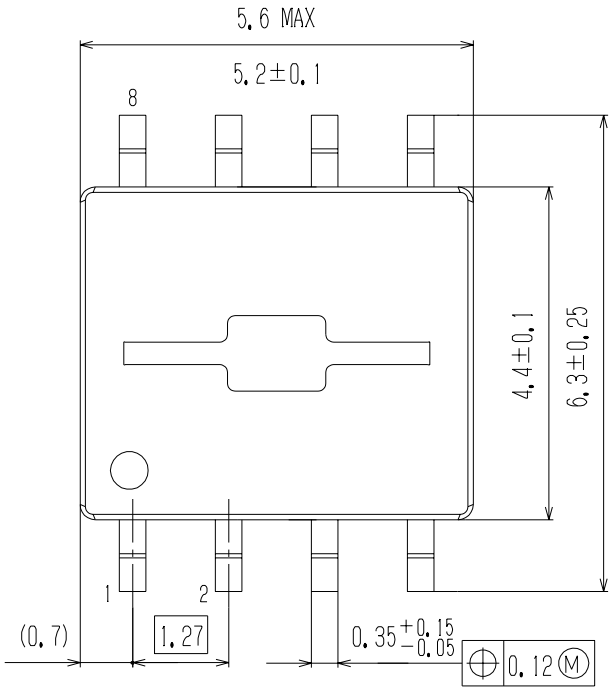
SANYO : Small Outline Package 8Pin Plastic

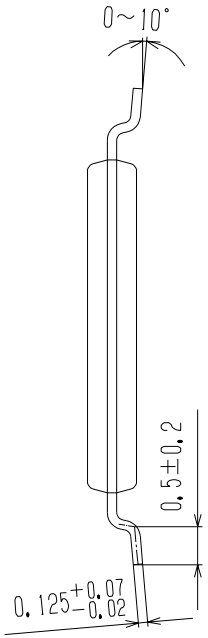
OUTLINE DRAWING

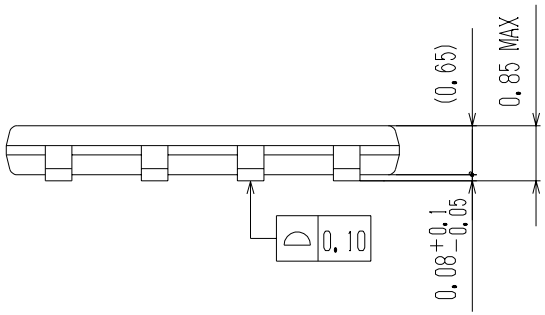
SANYO

SANYO Package Code	EIAJ Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass(g)
MSOP8(225mil)	———	———	———	S-222	0.04

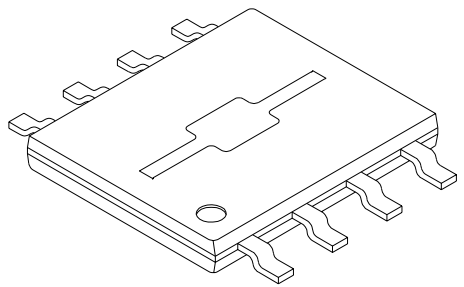
Measure	Unit
10/1	mm







Appearance



MSOP8(225mil)

REVISION : 1

SANYO : Micro Small Outline Package 8Pin Plastic

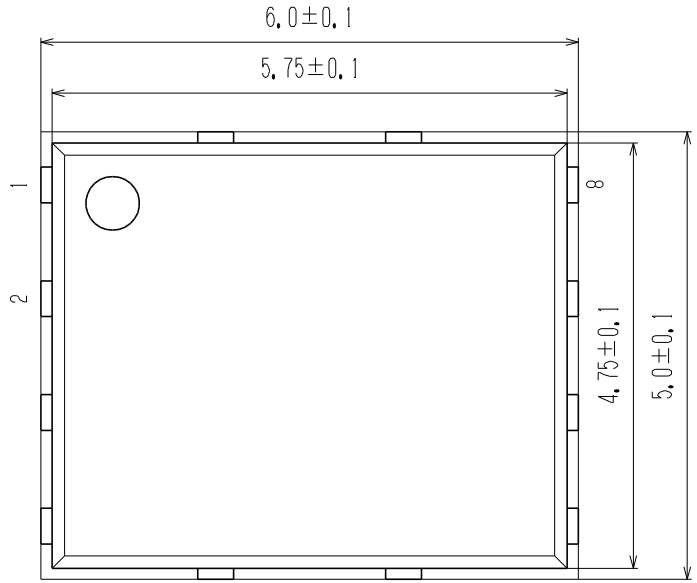
OUTLINE DRAWING

SANYO

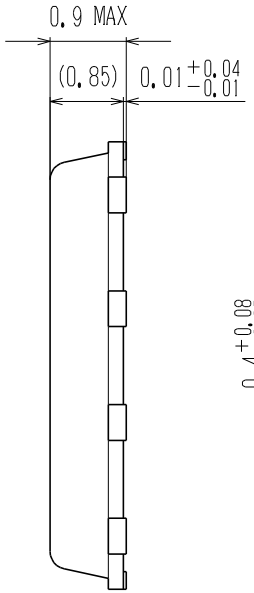
SANYO Package Code	JEITA Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass(g)
VSON8(5.0X6.0)X01	———	———	———	———	———

Measure	Unit
12/1	mm

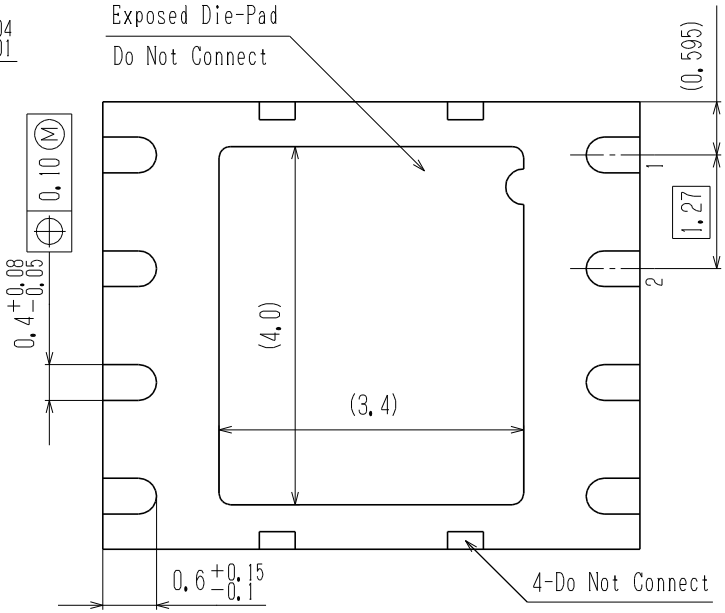
TOP VIEW



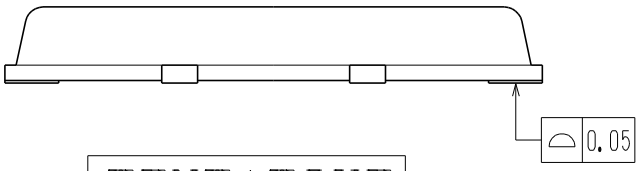
SIDE VIEW



BOTTOM VIEW

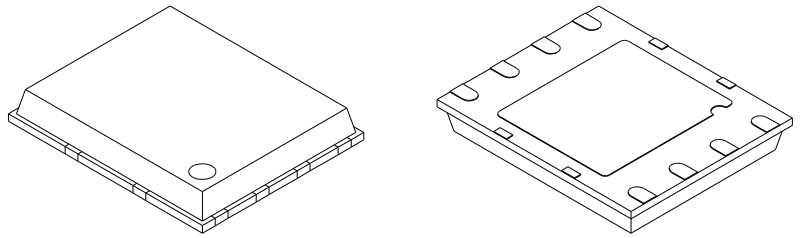


SIDE VIEW



TENTATIVE

Appearance



VSON8(5.0X6.0)X01

REVISION : 1

SANYO : Very Thin Small Outline Non-leaded Package