Data Sheet

VT1708S
High Definition Audio Codec

January 6, 2009
(Released under Creative Commons License)
Preliminary Revision 1.0

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1 Product Features

VT1708S

High Definition Audio Codec

- **High Definition Audio Codec**
  - Intel High Definition Audio Specification Rev.1.0 Compliant

- **High Audio Quality**
  - Exceeds Microsoft Windows Logo Program (WLP) Requirements
  - High-Performance DACs with 100 dB SNR, ADCs with 90 dB SNR

- **Various Output Format**
  - 4 Stereo DACs supporting 16/20/24-bit, 48/ 96/ 192/ 44.1/ 88.2 kHz sample rate
  - 2 Stereo ADCs supporting 16/20/24-bit, 48/ 96/ 192/ 44.1 kHz sample rate
  - 2 Independent S/PDIF TX Outputs Supporting 2 Output Pins with 16/20/24-bit, 48 / 96/ 192/ 44.1/ 88.2 kHz samples. The second one is for digital audio output to a HDMI transmitter.

- **Others**
  - Software Selectable Boost Gain (10dB/20dB/30dB) for Analog Microphone Input
  - HPF in ADC Path for DC Removal
  - Jack-detect Circuit with Unsolicited Response
  - Front Panel Jack Re-tasking
  - 2 GPIO (General Purpose Input and Output) Pins for Customized Use

- **Power Supply**
  - Digital: 3.3V
  - Analog: 5.0V
  - Support External Amplifier Power Down (EPAD)
  - Power Management and Enhanced Power Saving Features

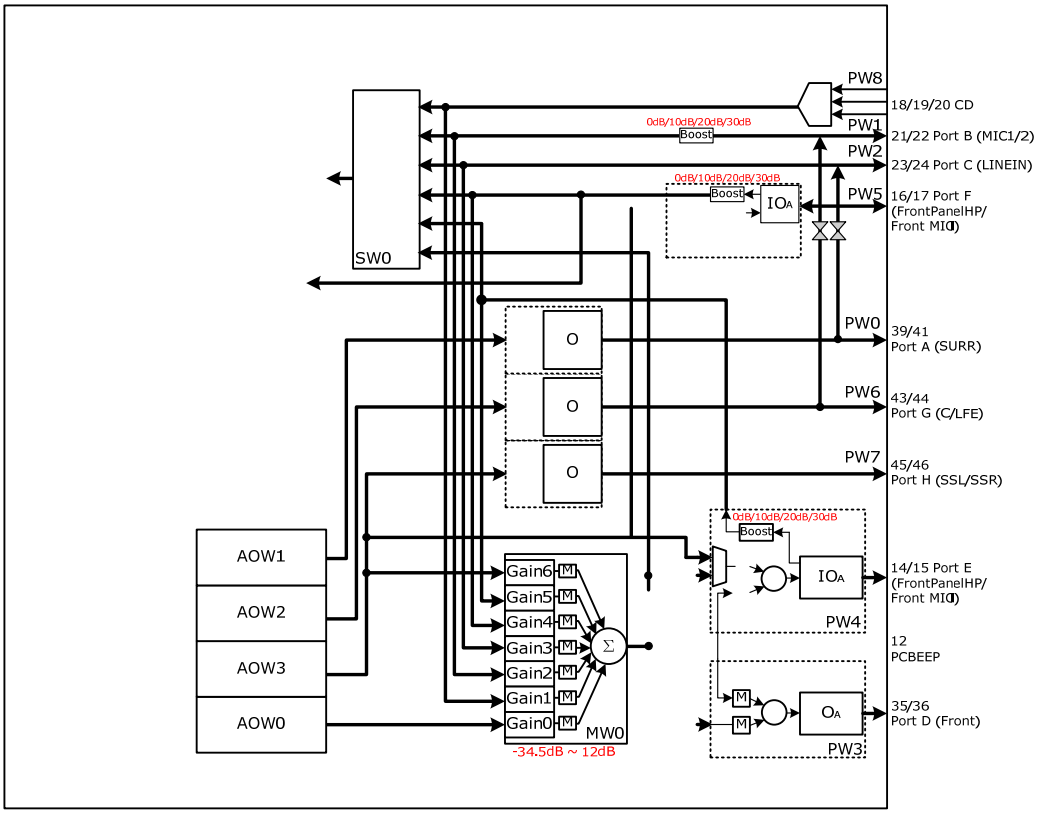
- **Package**
  - Available in 48-Pin LQFP Lead-Free Package

2 Overview

The VIA VT1708S is a quality High Definition Audio Codec that conforms to Intel High Definition Audio Specification Rev.1.0 and with performance exceeds Microsoft Windows Logo Program (WLP) Requirements. It supports 100-dB DAC SNR and 90-dB ADC SNR. VT1708S features four 24-bit stereo digital-to-analog converter (DAC) and two 24-bit analog-to-digital converter (ADC) channels, supporting audio sampling rates up to 192 kHz. VT1708S is capable of supporting various audio output stream formats.

The two independent 16-, 20-, 24-bit S/PDIF TX Output channels of VT1708S support sampling rates of 48 kHz, 96 kHz, 192 kHz, 44.1 kHz, and 88.2 kHz. The second S/PDIF TX Out is dedicated for digital audio output to a HDMI transmitter. The Analog Microphone Input supports software-selectable gain boost of 10-dB, 20-dB, and 30-dB. VT1708S features high-pass-filter (HPF) in analog-to-digital converter (ADC) path for removing DC offset signals.

The built-in Jack-detect Circuit allows to sense if an audio device is plugged in. The Front Panel Jack Re-tasking function facilitates flexible configurations. In addition, VT1708S provides two GPIO (General Purpose Input and Output) pins for customized applications. VT1708S is suitable for high performance and power efficient audio applications. VT1708S is available in the 7 mm × 7 mm 48-Pin LQFP lead-free and RoHS compliant package



3 Pinout

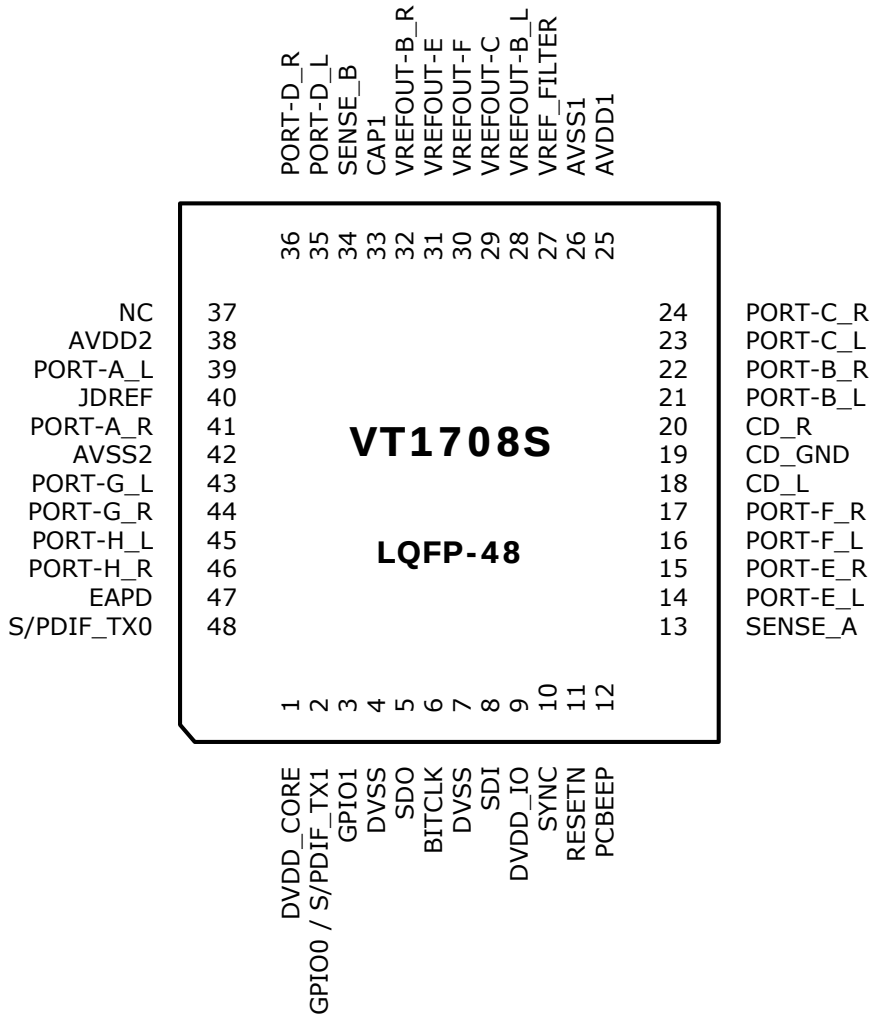


Figure 2 – VT1708S Pin Diagram for LQFP-48 (Top View)

4 Pin List

Table 1 – VT1708S Pin List

Pin	Pin Name	Pin	Pin Name
1	DVDD_CORE	25	AVDD1
2	GPIO0 / S/PDIF_TX1	26	AVSS1
3	GPIO1	27	VREF_FILTER
4	DVSS	28	VREFOUT-B_L
5	SDO	29	VREFOUT-C
6	BITCLK	30	VREFOUT-F
7	DVSS	31	VREFOUT-E
8	SDI	32	VREFOUT-B_R
9	DVDD_IO	33	CAP1
10	SYNC	34	SENSE_B
11	RESETN	35	PORT-D_L (Front Left)
12	PCBEEP	36	PORT-D_R (Front Right)
13	SENSE_A	37	NC
14	PORT-E_L (Front HP Left)	38	AVDD2
15	PORT-E_R (Front HP Right)	39	PORT-A_L (Surround Left)
16	PORT-F_L (Front MIC 1)	40	JDREF
17	PORT-F_R (Front MIC 2)	41	PORT-A_R (Surround Right)
18	CD_L	42	AVSS2
19	CD_GND	43	PORT-G_L (Center / LFE)
20	CD_R	44	PORT-G_R (LFE / Center)
21	PORT-B_L (Mic 1)	45	PORT-H_L (Side Surround Left)
22	PORT-B_R (Mic 2)	46	PORT-H_R (Side Surround Right)
23	PORT-C_L (Line in L)	47	EAPD
24	PORT-C_R (Line in R)	48	S/PDIF_TX0

5 Pin Description

Table 2 – Signal Type Definitions

Type	Description
I	**Input.** Standard input-only signal.
O	**Output.** Standard active output driver.
I/O	**Input/output.** An input/output signal.
T/S	**Tri-state.** Inactive bi-directional input/output pin.
OD	**Open drain.** Allows multiple devices to share as a wire-OR.
A_{DIFF}	**Analog differential.** Signal pair for the twisted-pair interface.
A_{BIAS}	**Analog bias or reference signal.** Must be tied to external resistor and/or capacitor bias network, as shown in the system schematic.

Digital I/O Pins

Pin Name	Pin #	I/O	Signal Description
GPIO0 / S/PDIF_TX1	2	IO	General Purpose Input/Output 0 / The Second S/PDIF Output
GPIO1	3	IO	General Purpose Input/Output 1
SDO	5	I	Serial Data Input from Controller
BITCLK	6	I	24MHz Bit Clock from Controller
SDI	8	IO	Serial Data Output to Controller
SYNC	10	I	Sample SYNC from Controller
RESETN	11	I	Hardware Reset from Controller
EAPD	47	O	External Amplifier Power-Down
S/PDIF_TX0	48	O	The First S/PDIF Output

Analog I/O Pins

Pin Name	Pin #	I/O	Signal Description
SENSE_A	13	I	Jack Detect Pin 1
SENSE_B	34	I	Jack Detect Pin 2
PORT-E_L	14	IO	Analog Output for Front Panel HP Out Left
PORT-E_R	15	IO	Analog Output for Front Panel HP Out Right
PORT-F_L	16	IO	Analog I/O. Default is input for Front MIC
PORT-F_R	17	IO	Analog I/O. Default is input for Front MIC
CD-L	18	I	CD Input Left Channel
CD-R	20	I	CD Input Right Channel
PORT-B_L	21	IO	Analog I/O. Default is input for MIC1 Left
PORT-B_R	22	IO	Analog I/O. Default is input for MIC1 Right
PORT-C_L	23	IO	Analog I/O. Default is input for Line-in Left
PORT-C_R	24	IO	Analog I/O. Default is input for Line-in Right
PORT-D_L	35	IO	Analog I/O. Default is output for Line-out Left
PORT-D_R	36	IO	Analog I/O. Default is output for Line-out Right
PORT-A_L	39	IO	Analog I/O. Default is output for Surround-out Left
PORT-A_R	41	IO	Analog I/O. Default is output for Surround-out Right
PORT-G_L	43	IO	Analog I/O. Default is output for Center
PORT-G_R	44	IO	Analog I/O. Default is output for LFE
PORT-H_L	45	IO	Analog I/O. Default is output for Side Surround Left
PORT-H_R	46	IO	Analog I/O. Default is output for Side Surround Right
PCBEEP	12	I	PC Beep Signal Input
VREF FILTER	27	IO	Reference Voltage Capacitor
VREFOUT-B_L	28	O	Reference Voltage Output for Port B Left
VREFOUT-C	29	O	Reference Voltage Output for Port C
VREFOUT-F	30	O	Reference Voltage Output for Port F
VREFOUT-E	31	O	Reference Voltage Output for Port E
VREFOUT-B_R	32	O	Reference Voltage Output for Port B Right
CAP1	33	IO	Optional Capacitor for ADC Reference
JDREF	40	I	External Resistor for Jack Detect Circuit

Power and Ground

Pin Name	Pin #	I/O	Signal Description
DVDD_CORE	1	P	Digital Core Power. 3.3V
DVDD_IO	9	P	Digital Power for HDA Link: 3.3V ~ 1.5V
DVSS	4	P	Digital VSS
DVSS	7	P	Digital VSS
AVDD1	25	P	Analog VDD
AVDD2	38	P	Analog VDD
AVSS1	26	P	Analog VSS
AVSS2	42	P	Analog VSS

6 High Definition Audio Link Protocol

6.1 Link Signaling

The link protocol defines the digital serial interface that connects High Definition Audio codec to the audio controller, and is not compatible with the previous AC97 protocol. The link is controller synchronous, based on a fixed 24MHz BITCLK and is purely isochronous without any flow control.

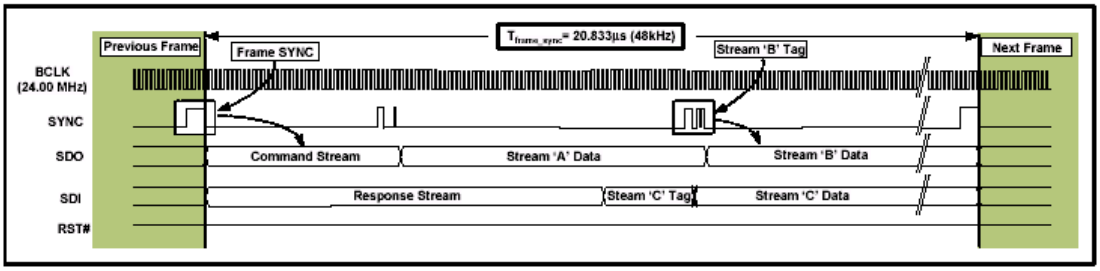


Figure 3 – High Definition Audio Link Conceptual View

6.2 Signal Definitions

Table 3 – High Definition Audio Link Conceptual View

Signal Name	Source	Type	Description
BITCLK	Controller	I	24 MHz clock
SYNC	Controller	I	Global 48KHz frame sync and outbound tag signal.
SDO	Controller	I	Bussed serial data output from controller.
SDI	Codec & controller	IO	Point-to-point serial data. Controller has a weak pull down.
RESETN	Controller	I	Global active low reset signal.

BITCLK is the 24MHz clock sourced from the controller and connecting to all codec on the link.

SYNC marks input and output frame boundaries (Frame Sync) as well as identifying outbound data streams (stream tags). SYNC is always sourced from the controller and connects to all codec on the link.

SDO is driven by the controller to all codec on the link. Compared with AC97, the SDO is double pumped with respect to both rising and falling edges of BITCLK in order to increase the bandwidth required for High Definition Audio link.

SDI is a point-to-point data signal driven by the codec to the controller. Because the bandwidth requirement is not that high compared to SDO, data is single pumped with respect to only the rising edge of BITCLK. The controller is required to implement weak pull-down on all SDI signals.

RESETN is sourced from the controller and connects to all codec on the link. Assertion of RESETN results in all link interface logic being reset to Default power on state.

The following figure shows the timing diagram of BITCLK, SYNC, SDO and SDI.

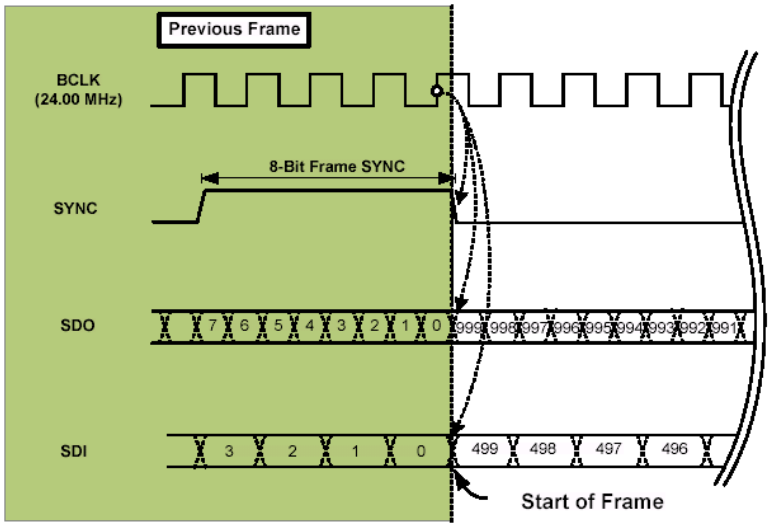


Figure 4 – Bit Timing Diagram

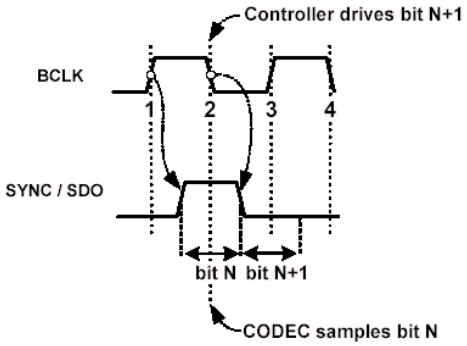


Figure 5 – SYNC and SDO Timing Relative to BITCLK

Figure 5 shows that both SYNC and SDO may be toggled with respect to either edge of BITCLK. In particular, bit cell n+1 is driven by the controller on SDO with respect to clock edge #2, and is sampled by the codec with respect to the subsequent clock edge, #3, and so forth.

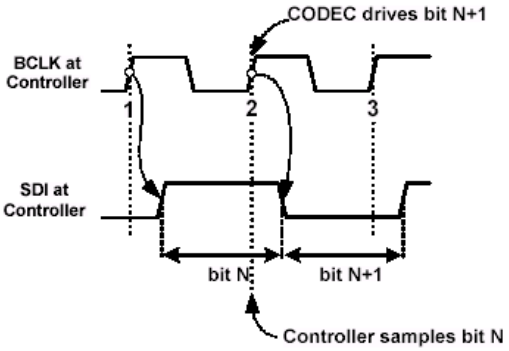


Figure 6 – SDI Timing Relative to BITCLK

Figure 6 shows that SID may only be toggled with respect to the rising edge of BITCLK. In particular, bit cell n+1 is driven by the codec on SDI with respect to rising clock edge #2 and is sampled by the controller with respect to the subsequent rising clock edge, #3, and so forth.

6.3 Signaling Topology

The following diagram shows a typical system with one controller and its associated codec.

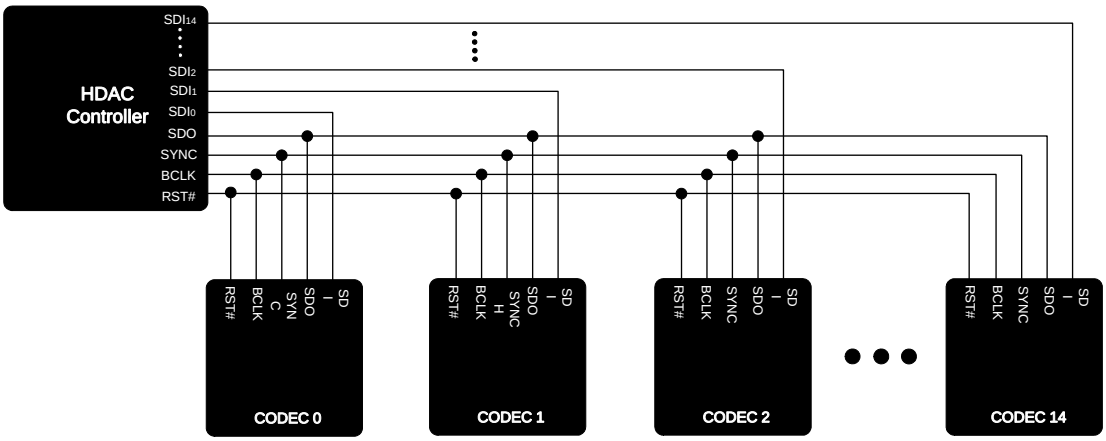


Figure 7 – Basic High Definition Audio System

6.4 Frame Composition

A frame is defined as a 20.833 µs window of time marked by the falling edge of the Frame Sync marker, which identifies the start of each frame. The controller is responsible for generating the Frame Sync marker, which is a high-going pulse on SYNC, exactly four BITCLK in width.

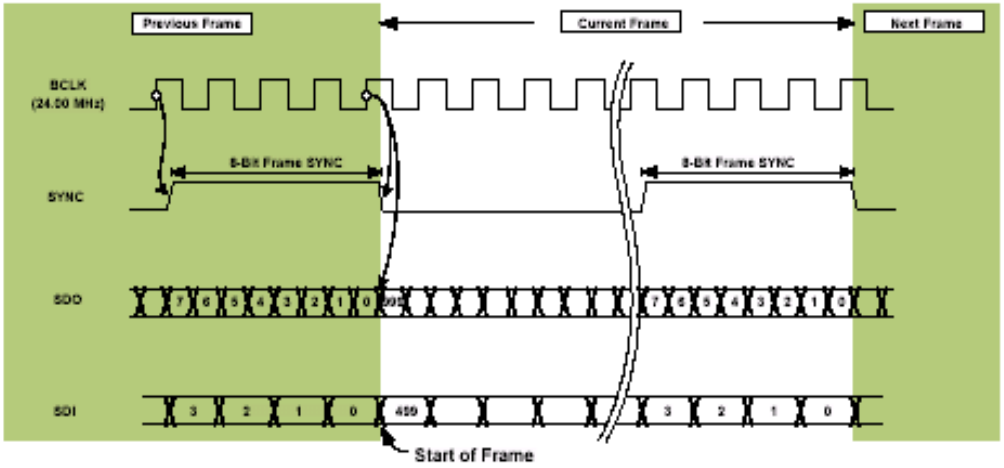


Figure 8 – Frames Demarcation

Both inbound and outbound frames are made up of three major components, specifically:

- A single Command / Response Field
- Zero or more Stream Packets
- A Null Field to fill out the frame

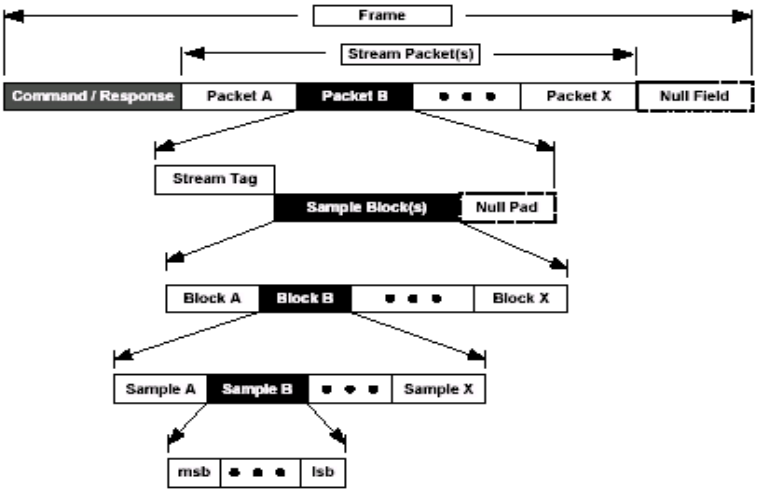


Figure 9 – Frame Composition

Command / Response Field is used for link and codec management. One of these fields appears exactly once per frame, MSB first, and is always the first field in the frame. It is composed of a 40-bit Command Field on each outbound frame from the controller and a 36-bit Response Field on each inbound frame from the codec.

Stream Tag is the label at the beginning of each stream packet that provides the associated stream ID. All data in one stream packet belongs to a single stream.

Sample Block is a set of one or more samples, the number of which is specified by the "Channels" field of the Stream Descriptor Format registers. Samples in a given sample block are associated with a single given stream, have the same sample size, and have the same time reference. And no padding is permitted between samples.

Ordering of samples within a block is always the same for all blocks in a given stream.

Sample is a set of bits providing a single sample point of a single analog waveform.

Null Field is used to fill up the remainder of the bits in each frame that are not used for Command / Response or packets. A null field must be transmitted as logical 0's.

6.5 Output Frame

6.5.1 Stream Tags

Outbound stream tags are 8 bits in length and are transmitted at a double pumped rate as side band information on SYNC. It is composed of a 4-bit preamble which is signaled as three SDO bit times high followed by one SDO bit time low. This is immediately followed by a 4-bit Stream ID. Outbound stream tags are transmitted on SYNC so as to align with the last eight data bits of the preceding stream packet or Command Field.

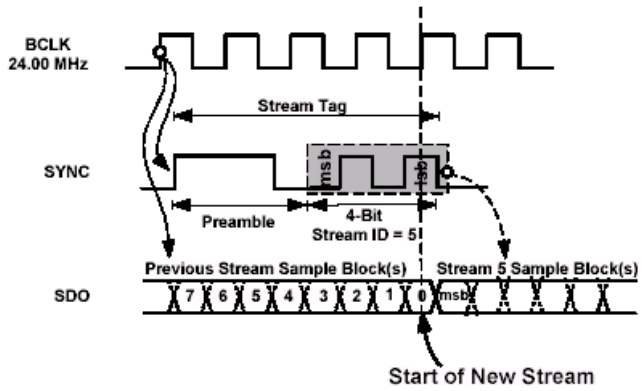


Figure 10 – Outbound Stream Tag Format and Transmission

6.5.2 Outbound Frames

Outbound frames start and end between the falling edges of successive Frame Syncs. The first 40 bits are dedicated for the Command field and are sued to send

6.6 Input Frame

6.6.1 Stream Tags

An inbound stream tag is 10 bits in length, and is transmitted "in-line" at a single pumped rate on SDI, immediately preceding the associated inbound sample blocks. It is composed of a 4-bit stream ID, followed by a 6-bit data length field that provides the length, in bytes, of all sample blocks with the given stream packet.

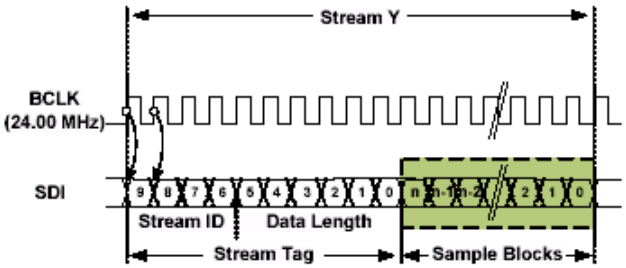


Figure 12 – Inbound Tag Format and Transmission

6.6.2 Inbound Frames

Inbound frames start and end between the falling edges of successive Frame Syncs. The first 36 bits of an inbound frame are dedicated for the Response Field, which codec use for sending responses to controller commands. The codec transmits the first stream packet on SID immediately following the Response Field. A stream tag indicating a packet length of zero must immediately follow the last stream packet to be transmitted. Such a stream tag marks the completion of data transmission within that frame, and the remaining valid bit positions are set to the null field. In the event there are less than 10 valid bit positions remaining in the frame after the last stream packet, then no termination tag is transmitted, and the remaining bits are the null field.

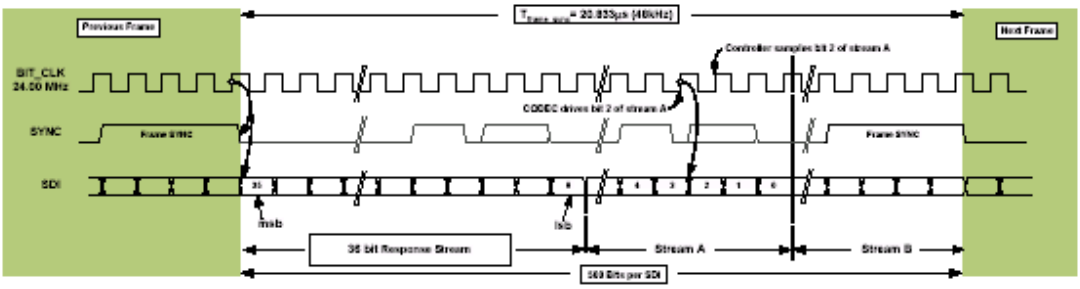


Figure 13 – Inbound Frame with No Null Field

6.7 Reset and Initialization

6.7.1 Link Reset

A link reset is signaled on the link by assertion of the RESETN signal, and results in all Link interface logic in both codec and controller, including registers, being initialized to their Default state. The controller drives all SDO and SYNC outputs low when entering or exiting link reset.

A controller may only initiate the link reset entry sequence after completing any currently pending initialization or state change requests.

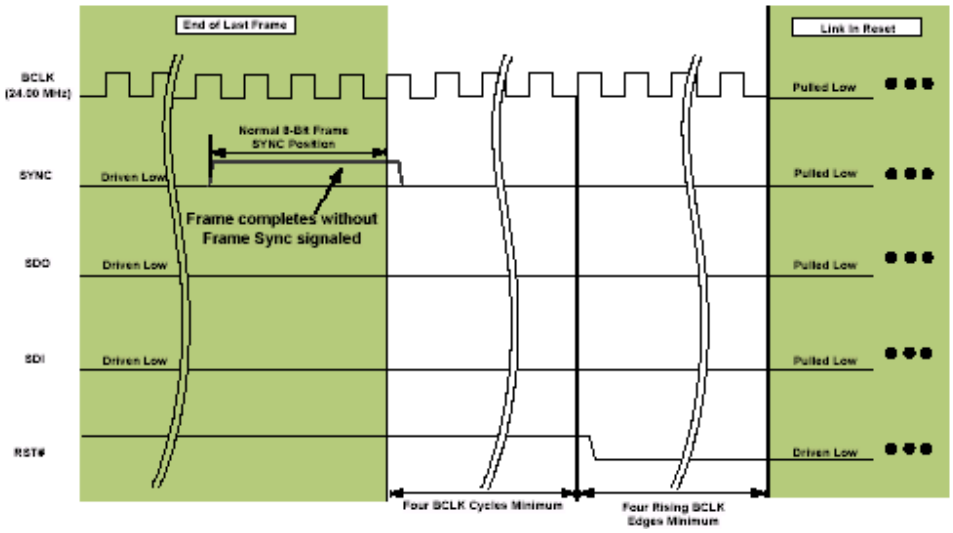


Figure 14 – Link Reset Entry Sequence

The sequence when entering link reset is described in the following.

1. The controller synchronously completes the current frame but does not signal Frame Sync during the last eight SDO bit times.
2. The Controller synchronously asserts RESETN four or more BITCLK cycles after the completion of the current frame.
3. BITCLK is stopped a minimum of four clocks after the assertion of RESETN.

In the event of a host bus reset, the above sequence does not complete, and RESETN is asynchronously asserted immediately and unconditionally.

Regardless of the reason for entering Link Reset, it may be exited only under software control and in a synchronous manner.

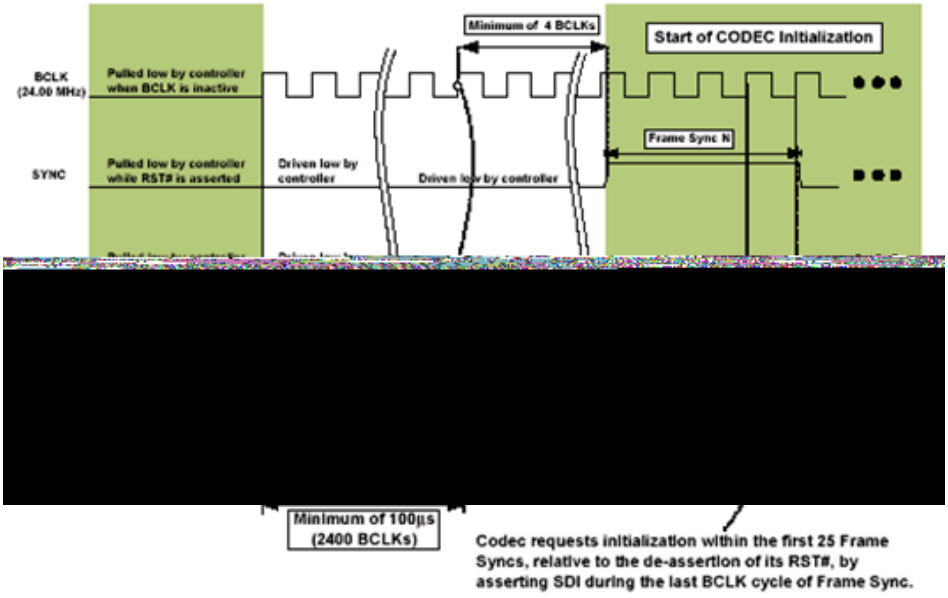


Figure 15 – Link Reset Exit Sequence

The sequence when exiting link reset is described in the following.

1. The controller provides a properly running BITCLK for a minimum of 100us (2400 BITCLK cycles or more) before the de-assertion of RESETN. This allows time for codec PLLs to lock.
2. The RESETN signal is de-asserted.
3. The SYNC commences signaling valid frames on the link with the first Frame Sync occurring a minimum of four BITCLK cycles after the de-assertion of RESETN.
4. Codec must signal an initialization request via SID within the first 25 Frame Syncs relative to the de-assertion of their respective RESETN signal.

6.7.2 Codec Function Group Reset

A codec function group reset is initiated via the Function_Reset verb and results in all logic within the targeted function group being driven to its Default or reset state. By Default VT1708S does not signal a state change and initialization request on SDI after the Function_Reset verb, and still keeps its codec address previously assigned by the controller. This behavior can be changed by setting a vendor defined register bit for backward compatible with the Rev. 0.7 Azalia Spec. See the Vendor Defined verbs in the Audio Function Group for the detail.

6.7.3 Codec Initialization

Immediately following the completion of Link Reset sequence (or Function_Reset verb, if enabled by the vendor-defined verb), VT1708S proceed through a codec initialization sequence, which is provide each codec with a unique address by which it can thereafter be referenced with Commands on the SDO signal. During this sequence, the controller provides each requesting codec with a unique address using its attached SDI signals.

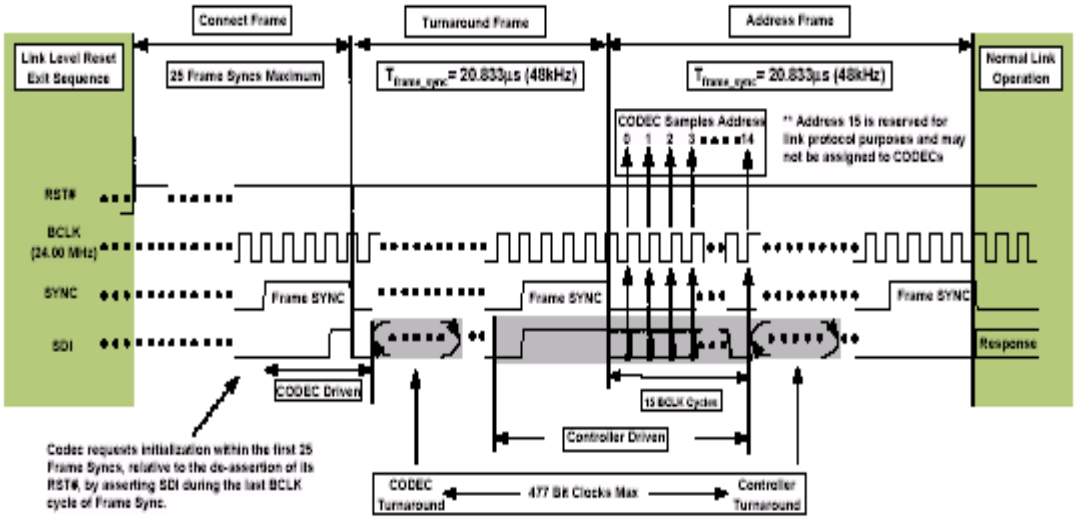


Figure 16 – Codec Initialization Sequence

The codec initialization sequence occurs across three contiguous frames immediately following any reset sequence. During these three frames, codec are required to ignore all outbound traffic present on SYNC & SDO. These three frames, labeled the “Connect Frame”, the “Turnaround Frame”, and the “Address Frame”, are described below.

6.7.3.1 Connect and Turnaround Frames

In the Connect and Turnaround Frames, the codec signals its request for initialization on SDI and then releases SDI (turnaround) to be driven by the controller in the subsequent address frame.

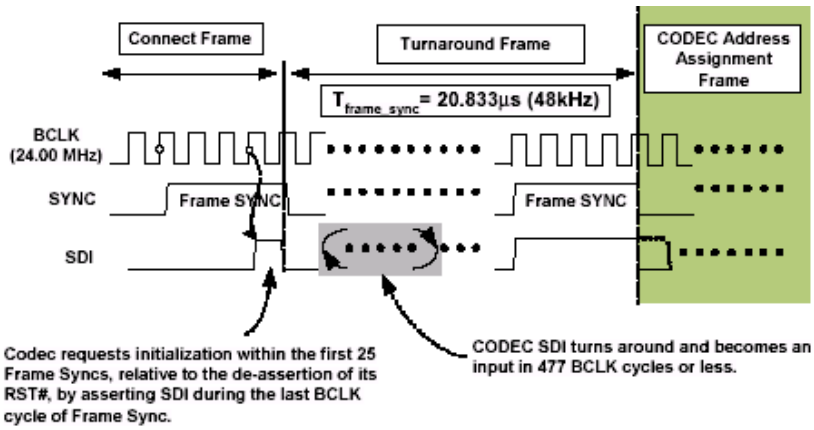


Figure 17 – Connect and Turnaround Frames

The codec signals an initialization request by synchronously driving SDI high during last bit clock cycle of Frame Sync. SDI must be asserted for the entire BITCLK cycle and must be synchronously de-asserted o the same rising edge of BITCLK as the de-assertion of the Frame Sync. Codec are only permitted to signal an initialization request on a null input frame, a frame in which no response stream or input streams are being sent.

In the Turnaround Frame, codec and controllers are required to turn SDI around upon the completion of the Connect Frame. To do this, the codec actively drives SDI low for one BITCLK cycle immediately following the de-assertion of SYNC at the end of the Connect Frame. The codec then puts its SDI drivers in a high impedance state at the end of the first BITCLK cycle in the Turnaround Frame. Four BITCLK cycles before the end of the Turnaround Frame, SYNC and SID are driven high by the controller. The SDI remains driven high through the end of the Turnaround Frame in preparation for the subsequent address frame.

6.7.3.2 Address Frames

During the Address Frame, SDI is a codec input and is driven by the controller beginning in the last four BITCLK periods (Frame Sync) of the Turnaround Frame. The falling edge of Frame Sync marks the start of codec address assignment. Address assignment is indicated by the controller holding each SDI high for the number of BITCLK cycles equal to the numeric ID of that particular SDI. Thus the unique address of the codec becomes the ID of its attached SDI.

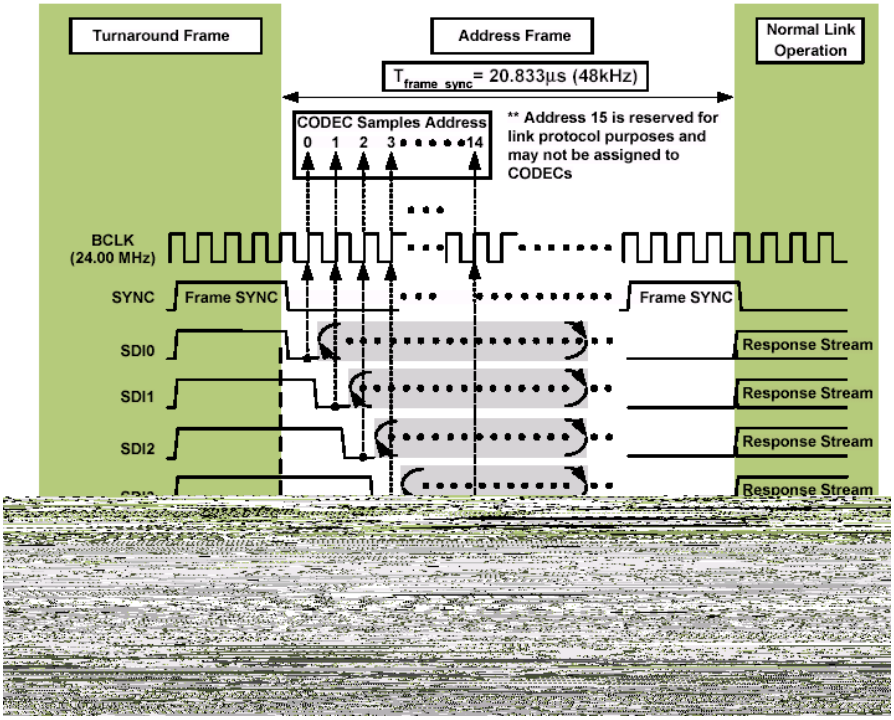


Figure 18 – Address Frame

Codec count from zero to fourteen starting on the rising edge of BITCKL following the de-assertion of Frame Sync, and sample the value of this count for their unique address on the first rising edge of BITCLK in which SYNC and SDI are both sampled low.

The controller must put its SDI drivers in a high impedance state by the rising edge of the 18th BITCLK of the address frame but not before driving each SDI low for at least one clock cycle. The SDI then becomes an input to the controller. Normal link operation starts on the frame following the completion of the Address Frame, and the codec is required to actively drive a valid response field and to be ready to accept commands in this and subsequent frames.

6.8 Handling Stream Independent Sample Rates

Unlike AC97, the Link is source synchronous and has no codec initiated flow control, the controller generates all sample transfer timing.

6.8.1 Codec Sample Rendering Timing

VT1708S supports the all the multiples and submultiples of the base rates of 48 kHz & 44.1 kHz, up to the maximum rate respectively of the DAC and ADC. For DAC, up to 192 kHz sample rate is supported. For ADC, the maximum rate is 96 kHz.

Table 4 – Sample Rate Supported

Multiple	Base Rate 48 kHz	Base Rate 44.1 kHz
1/6	8 kHz	
1/4		11.025 kHz
1/3	16 kHz	
1/2		22.05 kHz
2/3	32 kHz	
1	48 kHz	44.1 kHz
2	96 kHz	88.2 kHz
4	192 kHz	176.4 kHz

6.8.2 Link Sample Delivering Timing

For streams whose sample rate is a natural harmonic of 48 kHz, the timing is relatively straightforward. The rates in multiple (N) of 48 kHz are containing N sample blocks in one frame. For the rates in sub-multiple (1/N) of 48K, there must be one sample block transmitted every one in N frames, and the intervening N-1 frames will contain no sample for this stream.

Since the link frame rate is fixed at 48 kHz, streams using a base rate of 44.1 kHz must have samples transmitted on a cadence creating the slightly lower aggregate transmission rate to match the slightly lower rendering rate. For streams running at a sample rate of 44.1 kHz, there're occasional frames that will not contain a sample generating the following cadence.

12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)

The dashes indicate frames that do not contain a sample block. The cadence repeats continuously generating exactly 147 sample blocks every 160 frames, and avoids any long term drift between sample delivery and rendering clock.

Sample rates that are integral multiples of 44.1KHz apply the "12-11" cadence rule just as a 44.1KHz sample rate would, except that non-empty frames contain multiple (2 or 4) sample blocks, instead of just one.

For a sample rate of 22.05 kHz, the transmission pattern becomes:

{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{11}-* (repeat)
where
{12} = 1*1*1*1*1*1*1*1*1*1*1*1*
{11} = 1*1*1*1*1*1*1*1*1*1*1*

and the asterisks * represent a frame in which there is no sample block.

For a sample rate of 11.025 kHz, the transmission pattern becomes:

[12]-*[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[11]-*** (repeat)**
where
[12] = 1*1***1***1***1***1***1***1***1***1***1***1*****
[11] = 1*1***1***1***1***1***1***1***1***1***1*****

and the asterisks * represent a frame in which there is no sample block.

These framing sequences apply only to the outbound (SDO) data from the controller. Inbound (SDI) data transmitted by the codec is permitted to deviate for minimizing codec buffer management.

6.9 Power Management

Whenever the Link is commanded to enter a low power state, it enters the link-reset state. This state is only exited in response to a software command and follows all link rules for exiting the link reset state. The Audio Function Group and the analog input / output converter widgets support power control. Whole chip power states can be controlled through the Audio Function Group, while individual DACs and ADCs can also be controlled through the corresponding power state control verbs. The following table describes the definition of the power states.

Power States	Definitions	Referenced with AC97
D0	All power on. Individual ADCs & DACs can be controlled.	
D1	All amplifiers and analog converters are powered down. Register values maintained, and analog reference voltage is still on.	PR0 & PR1 & PR2
D2	Register values maintained, but analog reference voltage is also down.	PR3
D3	Same as D2 state.	PR3

6.10 Unsolicited Response Behavior Description

- As jack plug in, and jack pull out, "unsolicited response" occurs.
- As initial state (boot-up or wake-up), jack already plugged-in, 'unsolicited response does not report. Bit 31 of pin sense register needs to correctly report whether anything is plugged in.
- All pin widgets except SPDIF TX, only analog jacks externally exposed, and of the 3.55mm (1/8'') mini jack type need "unsolicited response".
- "Unsolicited response" is a capability that could be reported by any type of widgets. Microsoft class driver only takes advantage of pin widget on this because it's not clear to us what other widget types (AOW, AIW and MW) are going to use this response.
- While Microsoft spec. is not very clear about what its Default should be, Microsoft recommendation is set it to disabled by Default. Class driver will enable it before using unsolicited response.

7 Widget Description

7.1 Node ID List

Table 5 – Node ID List

Node ID	Name	Input Connection List	Note
00	Root Node	N/A	
01	AFG	N/A	Audio Function Group
10	AOW0	N/A	Analog Output Widget 0
11	AOW1	N/A	Analog Output Widget 1
12	DOW0	N/A	Digital Output Widget 0 for S/PDIF TX0
13	AIW0	17	Analog Input Widget 0
14	AIW1	1E	Analog Input Widget 1
15	DOW1	N/A	Digital Output Widget 1 for S/PDIF TX1
16	MW0	10, 1A, 1B, 1D, 1E, 1F, 25	Analog Mixer
17	SW0	16, 1A, 1B, 1D, 1E, 1F	ADC Input Selection
18	SW1	11	AOW1 Mute
19	PW0	18	Port A
1A	PW1	26	Port B
1B	PW2	18	Port C
1C	PW3	16	Port D
1D	PW4	16,25	Port E
1E	PW5	16,25	Port F
1F	PW8	N/A	Pin Widget 8 for CD Input
20	PW9	12	Pin Widget 9 for S/PDIF TX0
21	PW10	15	Pin Widget 10 for S/PDIF TX1
22	PW6	26	Port G
23	PW7	27	Port H
24	AOW2	N/A	Analog Output Widget 2
25	AOW3	N/A	Analog Output Widget 3
26	SW2	24	AOW2 Mute
27	SW3	25	AOW3 Mute

7.2 Root Node (Node ID = 00)

7.2.1 Get Parameter Verb (Verb ID = F00h)

Get Vendor ID (Payload = 00h) Response: 1106 0397h

Bit	Attribute	Description
31-16	R	Vendor ID 1106h
15-0	R	Device ID 0397~7397h (Default: 0397h)

Get Revision ID (Payload = 02h) Response: 0010 0000h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	MajRev The major revision number (left of the decimal) of the Azalia spec to which the codec is fully compliant. 0001b
19:16	R	MinRev The minor revision number (right of the decimal) of the Azalia spec to which the codec is fully compliant. 0000b
15:8	R	Revision ID 00000000b
7:0	R	Stepping ID 00000000b

Get Subordinate Node Count (Payload = 04h) Response: 0001 0001h

Bit	Attribute	Description
31:24	R	Reserved
23:16	R	Starting Node Number 01h
15:8	R	Reserved
7:0	R	Total Number of Nodes 01h (Only 1 Audio Function Group in the codec.)

7.3 Audio Function Group (Node ID = 01)

7.3.1 Get Parameter Verb (Verb ID = F00h)

Get Subordinate Node Count (Payload = 04h) Response: 0010 0018h

Bit	Attribute	Description
31:24	R	Reserved
23:16	R	Starting Node Number 10h
15:8	R	Reserved
7:0	R	Total Number of Nodes 18h

Get Function Group Type (Payload = 05h) Response: 0000 0001h

Bit	Attribute	Description
31:9	R	Reserved
8	R	Unsolicited Response (Not Supported) 0b
7:0	R	Audio Function Group 01h

Get Function Group Capabilities (Payload = 08h) Response: 0000 0306h

Bit	Attribute	Description
31:17	R	Reserved
16	R	Beep Gen 0b
15:12	R	Reserved
11:8	R	Input Delay 3h
7:4	R	Reserved
3:0	R	Output Delay 6h

Get Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	D3Sup
2	R	D2Sup
1	R	D1Sup
0	R	D0Sup

Get GPIO Capabilities (Payload = 11h) Response: 4000 0002h

Bit	Attribute	Description
31	R	GPIOWake=0
30	R	GPIOUnsol=1 GPIO unsolicited response supported.
29:24	R	Reserved
23:16	R	NumGPIs=00h No GPI pin supported.
15:8	R	NumGPOs=00h No GPO pin supported.
7:0	R	NumGPIOs=01h One GPIO pin supported, when pin 2 is not configured as SPDIF_TX1 (F83h, bit4=0), the number of GPIO will be 2.

7.3.2 Subsystem ID Control Verb (Verb ID = F20h & 720h-723h)

	Description	Verb ID	Payload
Get	Get Subsystem ID	F20h	8'b0
Set1	Set Subsystem ID[7:0]	720h	Subsystem ID [7:0]
Set2	Set Subsystem ID[15:8]	721h	Subsystem ID [15:8]
Set3	Set Subsystem ID[23:16]	722h	Subsystem ID [23:16]
Set4	Set Subsystem ID[31:24]	723h	Subsystem ID [31:24]

Response: 1106 0000

Bit	Attribute	Description
31:16	RW	Manufacturer ID 1106h (Default)
15:8	RW	Board SKU 00h (Default)
7:0	RW	Assembly ID 00h (Default)

Note: All 32 bits in the Subsystem ID register are writeable, with the power-on default value of 1106 0000h. The system board BIOS can change the values during power up sequence to precisely describe the information about the motherboard so that the OS can load the correct driver.

7.3.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00 : Power State is D0 8'h01 : Power State is D1 8'h02 : Power State is D2 8'h03 : Power State is D3

Note: For whole chip power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Same as PS-Set for AFG.
3:0	RW	PS-Set

7.3.4 GPIO Unsolicited Response (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response	F08h	8'b0
Set	Set Unsolicited Response	708h	Enable unsolicited response

GPIO Unsolicited Format

Bit	Attribute	Description
7	RW	0: Unsolicited Response Disabled (Default) 1: Unsolicited Response Enabled
6	R	Reserved
5:0	RW	Tag Used by software to determine which node generated the unsolicited response.

7.3.5 GPIO Data (Verb ID = F15h & 715h)

	Description	Verb ID	Payload
Get	Get GPIO data Response	F15h	8'b0
Set	Set GPIO data	715h	GPIO Data [7:0]

Set GPIO Data Format

Bit	Attribute	Description
7:2	R	Reserved
1	W	GPIO1 data, when GPIO1 pin is configured as GPO.
0	W	GPIO0 data, when GPIO0 pin is configured as GPO.

Get GPIO Data Response Format

Bit	Attribute	Description
31:2	R	Reserved
1	R	GPIO1 Data
0	R	GPIO0 Data

7.3.6 GPIO Enable Mask (Verb ID = F16h & 716h)

	Description	Verb ID	Payload
Get	Get GPIO Enable Mask Response	F16h	8'b0
Set	Set GPIO Enable Mask	716h	GPIO Enable Mask [7:0]

Get/ Set GPIO Enable Mask Format

Bit	Attribute	Description
31:2	R	Reserved
1	RW	0: GPIO1 pin is disabled and in Hi-Z state. (Default) 1: GPIO1 pin is enabled and the pin's behavior will be determined by the GPIO1 Direction control.
0	RW	0: GPIO0 pin is disabled and in Hi-Z state. (Default) 1: GPIO0 pin is enabled and the pin's behavior will be determined by the GPIO0 Direction control.

7.3.7 GPIO Direction (Verb ID = F17h & 717h)

	Description	Verb ID	Payload
Get	Get GPIO Direction Response	F17h	8'b0
Set	Set GPIO Direction	717h	GPIO Direction[7:0]

Get/Set GPIO Data Response Format

Bit	Attribute	Description
31:2	R	Reserved
1	RW	GPIO1 Direction 0:Input (default) 1:Output
0	RW	GPIO0 Direction 0:Input (default) 1:Output

7.3.8 GPIO Unsolicited Response Enable Mask (Verb ID = F19h & 719h)

	Description	Verb ID	Payload
Get	Get GPIO Unsolicited Response Enable Mask Response	F19h	8'b0
Set	Set GPIO Unsolicited Response Enable Mask	719h	GPIO Unsolicited Response Enable Mask[7:0]

Get/ Set GPIO Unsolicited Response Enable Mask Format

Bit	Attribute	Description
31:2	R	Reserved
1	RW	0: An unsolicited response will NOT be sent when a GPIO1 line changes state.(default) 1: An unsolicited response will be sent when a GPIO1 line changes state.
0	RW	0: An unsolicited response will NOT be sent when a GPIO0 line changes state.(default) 1: An unsolicited response will be sent when a GPIO0 line changes state.

7.3.9 Vendor Defined Verbs (Verb ID = F70h – F74h) – Reserved

7.3.10 Vendor Defined Verbs (Verb ID = F78h – F7Ch) - Reserved

7.3.11 Vendor Defined Verbs (Verb ID = F80h – F84h) – Reserved

7.3.12 Vendor Defined Verbs (Verb ID = F88h – F8Ch) - Reserved

7.3.13 Vendor Defined Verbs (Verb ID = F90h – F94h) - Reserved

7.3.14 Vendor Defined Verbs (Verb ID = F98h – F9Ch) - Reserved

7.3.15 Vendor Defined Verbs (Verb ID = FA0h – FA4h) - Reserved

7.3.16 Vendor Defined Verbs (Verb ID = FA8h – FACh) - Reserved

7.3.17 Function Reset Verb (Verb ID = 7FFh)

	Description	Verb ID	Payload
Function Reset	Function Reset	7FFh	8'b0

7.4 Audio Analog Output Converter Widget (Node ID = 10h, 11h, 24h, 25h)

7.4.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0000 041Dh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0000b: Audio output converter widget.
19:16	R	0000b: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	0: Connection list is not present.
7	R	0: Does not support unsolicited response.
6	R	0: No Processing control.
5	R	Reserved
4	R	1: Contains format information.
3	R	1: Contain amplifier parameter.
2	R	1: Out Amp presented.
1	R	0: In amp not present.
0	R	1: Stereo.

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 05E0h

Bit	Attribute	Description
31:21	R	Reserved
20	R	0: No 32-bit audio format support.
19	R	1: 24-bit audio format support.
18	R	1: 20-bit audio format support.
17	R	1: 16-bit audio format support.
16	R	0: No 8-bit audio format support.
15:12	R	Reserved
11	R	0: 384 kHz not supported.
10	R	1: 192 kHz supported.
9	R	0: 176.4 kHz not supported.
8	R	1: 96 kHz supported.
7	R	1: 88.2 kHz supported.
6	R	1: 48 kHz supported.
5	R	1: 44.1 kHz supported.
4	R	0: 32 kHz not supported.
3	R	0: 22.05 kHz not supported.
2	R	0: 16 kHz not supported.
1	R	0: 11.025 kHz not supported.
0	R	0: 8 kHz not supported.

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Description
31:3	R	Reserved
2	R	0: No AC3 support.
1	R	0: No Float32 support.
0	R	1: PCM supported.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

Output Amplifier Capabilities (Payload =12h) Response: 0005 2A2Ah

Bit	Attribute	Description
31	R	0: No mute capability.
30:23	R	Reserved
22:16	R	Step Size 0000101: Step size is 1.5dB.
15	R	Reserved
14:8	R	Number of Steps 0101010: Number of steps is 42 (-63dB – 0dB).
7	R	Reserved
6:0	R	Offset 0101010: Offset 2Ah is 0dB.

7.4.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Note: For DAC power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.4.3 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4], Channel bit[3:0]

7.4.4 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Converter Format

Bit	Attribute	Description
15	R	Stream Type 0: PCM 1: Non-PCM (Not supported)
14	RW	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	Sample Base Rate Multiple 000 = x1: 48 kHz, 44.1 kHz 001 = x2: 96 kHz, 88.2 kHz 010 = x3: 144 kHz (Not supported) 011 = x4: 192 kHz, 176.4 kHz 100-111: Reserved
10:8	RW	Sample Base Rate Divisor 000 = /1: 48 kHz Others: Not supported
7	R	Reserved
6:4	RW	Bits per Sample 000: 8-bit (Not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (Not supported)
3:0	RW	Number of Channels (CHAN) Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

7.4.5 Amplifier Gain / Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. (Ignored) 1: The output amplifier is being requested.
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved
3:0	W	Index

Get Response Format — Response: 0000 002Ah

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Amplifier is un-muted.
6:0	R	Amplifier Gain Setting 0101010: Offset 2Ah is 0 dB. (Default)

Set Payload Format — Response: 0000 0000h

Bit	Attribute	Description
15	W	1: The output amplifier is being set.
14	W	1: The input amplifier is being set. (Ignored)
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-muted.
6:0	W	Gain Setting

7.5 Audio Digital Output Converter (S/PDIF TX) Widget (Node ID = 12h, 15h)

7.5.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0000 0611h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0000: Audio output converter widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	1: Digital widget, not analog.
8	R	0: Connection list is not present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	1: Contains format information.
3	R	0: Contains amplifier parameter.
2	R	0: Out amp present.
1	R	0: In amp not present.
0	R	1: Stereo.

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 05E0h

Bit	Attribute	Description
31:21	R	Reserved
20	R	0: No 32-bit audio format support.
19	R	1: 24-bit audio format support.
18	R	1: 20-bit audio format support.
17	R	1: 16-bit audio format support.
16	R	0: 8-bit audio format support.
15:12	R	Reserved
11	R	0: 384 kHz not supported.
10	R	1: 192 kHz not supported.
9	R	0: 176.4 kHz not supported.
8	R	1: 96 kHz supported.
7	R	1: 88.2 kHz supported.
6	R	1: 48 kHz supported.
5	R	1: 44.1 kHz supported.
4	R	0: 32 kHz not supported.
3	R	0: 22.05 kHz not supported.
2	R	0: 16 kHz not supported.
1	R	0: 11.025 kHz not supported.
0	R	0: 8 kHz not supported.

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Description
31:3	R	Reserved
2	R	0: No AC3 support.
1	R	0: No Float32 support.
0	R	1: PCM supported.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

7.5.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Note: For S/PDIF TX power down control.

Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.5.3 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4], Channel bit[3:0]

7.5.4 S/PDIF Converter Control 1 & 2 Verbs (Verb ID = F0Dh & 70Dh, 70Eh)

	Description	Verb ID	Payload
Get	Get Converter Control State	F0Dh	8'b0
Set	Set Converter Control 1	70Dh	SIC[7:0]
Set	Set Converter Control 2	70Eh	SIC[15:8]

S/PDIF IEC Control Bits Format Response: 0000 0000h

Bit	Attribute	Description
15	R	Reserved
14:8	RW	CC[6:0] Category Code
7	RW	L: Generation Level
6	RW	PRO 0: Consumer mode. 1: Professional mode.
5	RW	AUDIO 0: Data is PCM format. 1: Data is non PCM format.
4	RW	Copy 0: Copyright is not asserted. 1: Copyright is asserted.
3	RW	Pre 0: Pre-emphasis is none. 1: Filter pre-emphasis is 50/ 15 μs
2	RW	VCFG Determine S/PDIF transmitter behavior when data is not being transmitted.
1	RW	Validity Flag
0	RW	DigEn 0: S/PDIF TX disabled. 1: S/PDIF TX enabled.

7.5.5 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Converter Format — Response: 0031h

Bit	Attribute	Description
15	RW	Stream Type 0: PCM 1: Non-PCM
14	RW	Sample Base Rate 0: 48KHz 1: 44.1KHz
13:11	RW	Sample Base Rate Multiple 000 = x1: 48 kHz, 44.1 kHz 001 = x2: 96 kHz, 88.2 kHz 010 = x3: 144 kHz (Not supported) 011 = x4: 192 kHz, 176.4 kHz (176.4 kHz not support) 100-111: Reserved
10:8	RW	Sample Base Rate Divisor 000 = /1: 48 kHz Others: Not supported
7	R	Reserved
6:4	RW	Bits per Sample 000: 8-bit (Not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (Not supported)
3:0	RW	Number of Channels (CHAN) Refers to number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

7.6 Audio Analog Input Converter Widget (Node ID = 13h, 14h)

7.6.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0010 051Bh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0001: Audio input converter widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	1: Contains format information.
3	R	1: Contains amplifier parameter.
2	R	0: Out amp not presented.
1	R	1: In amp present.
0	R	1: Stereo.

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 0560h

Bit	Attribute	Description
31:21	R	Reserved
20	R	0: No 32-bit audio format support.
19	R	1: 24-bit audio format support.
18	R	1: 20-bit audio format support.
17	R	1: 16-bit audio format support.
16	R	0: 8-bit audio format support.
15:12	R	Reserved
11	R	0: 384 kHz not supported.
10	R	1: 192 kHz supported.
9	R	0: 176.4 kHz not supported.
8	R	1: 96 kHz supported.
7	R	0: 88.2 kHz not supported.
6	R	1: 48 kHz supported.
5	R	1: 44.1 kHz supported.
4	R	0: 32 kHz not supported.
3	R	0: 22.05 kHz not supported.
2	R	0: 16 kHz not supported.
1	R	0: 11.025 kHz not supported.
0	R	0: 8 kHz not supported.

Supported Stream Formats (Payload = 0Bh)		Response: 0000 0001h
Bit	**Attribute**	**Description**
31:3	R	Reserved
2	R	0: No AC3 support.
1	R	0: No Float32 support.
0	R	1: PCM supported.

Input Amplifier Capabilities (Payload = 0Dh)		Response: 8005 1F0Bh
Bit	**Attribute**	**Description**
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0000101: Step size is 1.5dB.
15	R	Reserved
14:8	R	Number of Steps 0011111: Number of steps is 32 (-16.5 dB – 30 dB).
7	R	Reserved
6:0	R	Offset 0001011: Offset 0Bh is 0dB.

Connection List Length (Payload = 0Eh)		Response: 0000 0001h
Bit	**Attribute**	**Description**
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001: 1 input available.

Supported Power States (Payload = 0Fh)		Response: 0000 000Fh
Bit	**Attribute**	**Description**
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.6.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	**Verb ID**	**Payload**
Get	Get Connection List Entry	F02h	Offset index n

Response: 0000 0017h or 0000 001Eh

Bit	**Attribute**	**Description**
31:8	R	Reserved
7	R	0: Independent NID.
6:0	R	0010111: From SW0 (NID = 17h) for AIW0. 0011110: From SW5 (NID = 1Eh) for AIW1.

7.6.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Note: For ADC power down control.

Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.6.4 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4], Channel bit[3:0]

7.6.5 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Converter Format — Response: 0031h

Bit	Attribute	Description
15	R	Stream Type 0: PCM 1: Non-PCM (Not supported)
14	RW	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	Sample Base Rate Multiple 000: x1: 48 kHz, 44.1 kHz 001: x2: 96 kHz, 010: x3: 144 kHz (Not supported) 011: x4: 192 kHz 100~111: Reserved
10:8	RW	Sample Base Rate Divisor 000 = /1: 48 kHz Others: Not supported
7	R	Reserved
6:4	RW	Bits per Sample 000: 8-bit (Not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (Not supported)
3:0	RW	Number of Channels (CHAN) Refer to the number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

7.6.6 Amplifier Gain / Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested. (Ignored)
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved
3:0	W	Index Ignored

Get Response Format — Response: 0000 008Bh

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Amplifier is un-muted. 1: Amplifier is muted. (Default)
6:0	R	Amplifier Gain Setting 0001011: 0dB. (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set. (Ignored)
14	W	1: The input amplifier is being set.
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-mute 1: Mute
6:0	W	Gain Setting

7.7 Mixer Widget (Node ID = 16h)

7.7.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0020 050Bh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0010: Audio mixer widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: No format information.
3	R	1: Amplifier parameter.
2	R	0: Out amp not presented.
1	R	1: In amp not present.
0	R	1: Stereo.

Input Amplifier Capabilities (Payload = 0Dh) Response: 8005 1F17h

Bit	Attribute	Description
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 7'b0000101 : Step size is 1.5 dB
15	R	Reserved
14:8	R	Number of Steps 7'b0011111 : Number of steps is 31 (-34.5 dB – 12 dB)
7	R	Reserved
6:0	R	Offset 7'b0010111 : Offset 17h is 0dB

Connection List Length (Payload = 0Eh) Response: 0000 0007h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000111: 7 inputs available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.7.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response: 1B1A 1F10h (n=0) or 0025 1D1Eh (n=4)

Bits	Type	Description	
		Offset index n = 0	Offset index n = 4
31:24	R	Connection List Entry n+3 8'h1B (PW2, PortC)	8'h00
23:16	R	Connection List Entry n+2 8'h1A (PW1, PortB)	Connection List Entry n+2 8'h25 (AOW3)
15:8	R	Connection List Entry n+1 8'h1F (PW8, CD)	Connection List Entry n+1 8'h1D (PW4)
7:0	R	Connection List Entry n 8'h10 (AOW0)	Connection List Entry n 8'h1E (PW5, PortF)

7.7.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00 : Power State is D0 8'h01 : Power State is D1 8'h02 : Power State is D2 8'h03 : Power State is D3

Note: For mixer power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.7.4 Amplifier Gain / Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/ Mute	Bh	Format
Set	Set Amplifier Gain/ Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested. (Ignored)
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved
3:0	W	Index

Get Response Format — Response: 0000 0097h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	Amplifier Gain Setting 0010111: Offset 17h is 0dB (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set. (Ignored)
14	W	1: The input amplifier is being set.
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-mute 1: Mute
6:0	W	Gain Setting

7.8 Selector Widget SW0 (Node ID = 17h)

7.8.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0030 0501h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0011: Audio selector widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R Swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: No format information.
3	R	0: Amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not present.
0	R	1: Stereo.

Connection List Length (Payload = 0Eh) Response: 0000 0006h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000110: 6 inputs available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

7.8.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0. Default: 0000 0001h (MIC)
Set	Set Connection Select	701h	The connection index value to be set

7.8.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n
			Response: 1E1B 1A1Fh (n=0) or 0000 161Dh (n=4)

Bits	Type	Description	
		Offset index n = 0	
31:24	R	Connection List Entry n+3 8'h1E (PW5, PortF)	Connection List Entry n+3 8'h00
23:16	R	Connection List Entry n+2 8'h1B (PW2, PortC)	Connection List Entry n+2 8'h00
15:8	R	Connection List Entry n+1 8'h1A (PW1, PortB)	Connection List Entry n+1 8'h16 (MW)
7:0	R	Connection List Entry n 8'h1F (PW8, CD)	Connection List Entry n 8'h1D (PW4, PortE)

7.8.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00 : Power State is D0 8'h01 : Power State is D1 8'h02 : Power State is D2 8'h03 : Power State is D3

Note: For SW0 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	PS-Set

7.9 Selector Widget SW1-SW3 (Node ID = 18h, 26h, 27h)

7.9.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0030 050Dh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0011: Audio selector widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: No format information.
3	R	1: Amplifier parameter.
2	R	1: Out amp present.
1	R	0: In amp not present.
0	R	1: Stereo.

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001: 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

Output Amplifier Capabilities (Payload = 12h) Response: 0000 0000h

Bit	Attribute	Description
31	R	1: Mute capable
30:23	R	Reserved
22:16	R	Step Size 0000000: Step size is 0dB
15	R	Reserved
14:8	R	Number of Steps 0000000: Number of steps is 0
7	R	Reserved
6:0	R	Offset

7.9.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set

7.9.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response: 0000 0011h, or 0000 0024h, or 0000 0025h

Bit	Attribute	Description
31:24	R	Reserved (00h)
23:16	R	Reserved (00h)
15:8	R	Reserved (00h)
7:0	R	Connection List Entry N 11h: (AOW1) for SW1 24h: (AOW2) for SW2 25h: (AOW3) for SW3

7.9.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00 : Power State is D0 8'h01 : Power State is D1 8'h02 : Power State is D2 8'h03 : Power State is D3

Note: For SW1~SW3 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the Actual Power State of the Widget.
3:0	RW	PS-Set

7.9.5 Amplifier Gain / Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. (Ignored) 1: The output amplifier is being requested.
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved
3:0	W	Index Ignored

Get Response format — Response: 0000 0080h

Bit	Attribute	Description
31:8	R	Response
7	R	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	Amplifier Gain Setting 0000000 (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set.
14	W	1: The input amplifier is being set. (Ignored)
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-mute 1: Mute
6:0	W	Gain Setting

7.10 Pin Widget PW0 (Node ID = 19h)

7.10.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 05h) Response: 0000 0101h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable
7:0	R	0000 0001: Audio function group

Audio Widget Capabilities (Payload = 09h) Response: 0040 0581h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget
19:16	R	0000: Delay
15:12	R	Reserved
11	R	0: No L-R swap
10	R	1: Power control supported
9	R	0: Analog widget, not digital
8	R	1: Connection list is present
7	R	1: Support unsolicited response
6	R	0: No processing control
5	R	Reserved
4	R	0: Doesn’t contain format information
3	R	0: Contain amplifier parameter
2	R	0: Out amp not Present
1	R	0: In amp not present
0	R	1: Stereo

Pin Capabilities (Payload = 0Ch) Response: 0000 0014h

Bit	Attribute	Description	
31:24	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 00h.
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 0.
4	R	Output Capable	Read as 1.
3	R	Headphone Drive Capable	Read as 0
2	R	Presence Detect Capable	Read as 1.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001: Only 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup
0	R	1: Stereo

7.10.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h00000018

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Independent NID
6:0	R	0011000: From SW1

7.10.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00 : Power State is D0 8'h01 : Power State is D1 8'h02 : Power State is D2 8'h03 : Power State is D3

Note: For PW0 power down control.

Response: 0000 0000h

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.10.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format Response: 0000 0000h

Bit	Attribute	Description
7	RW	Headphone Enable 0: Disabled 1: Headphone enabled (Not supported)
6	RW	Output Enable 0: Disabled (Default) 1: Output enabled
5	R	Input Enable 0: Disabled 1: Input enabled (Not supported)
4:0	R	Reserved

7.10.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format

Bit	Attribute	Description
7	RW	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	Reserved
5:0	RW	Tag Used by software to determine which node generated the unsolicited response.

7.10.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Bit	Attribute	Description
31	R	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	Reserved

7.10.7 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config Bits Format Response: 0101 1012h

Bit	Attribute	Description
31:30	RW	Port Connectivity 00b (Connected to a jack)
29:24	RW	Location 000001b
23:20	RW	Default Device 0000b (Line-out)
19:16	RW	Connection Type 0001b
15:12	RW	Color 0001b
11:8	RW	Misc 0000b
7:4	RW	Default Association 0001b
3:0	RW	Sequence 0010b (Surround out in association # 1)

7.11 Pin Widget PW3 (Node ID =1Ch)

7.11.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 05h) Response: 0000 0101h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable.
7:0	R	0000 0001b: Audio function group.

Audio Widget Capabilities (Payload = 09h) Response: 0040 058Dh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100b: Pin widget.
19:16	R	0000b: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	1: Support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	1: Contain amplifier parameter.
2	R	1: Out amp Present.
1	R	0: In amp not present.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0001 001Ch

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 1.
15:8	R	VRef Control	Read as 8’h00.
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 0.
4	R	Output Capable	Read as 1.
3	R	Headphone Drive Capable	Read as 1.
2	R	Presence Detect Capable	Read as 1.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001b: Only 1 input available.

Supported Power States (Payload = 0Fh)		Response: 0000 000Fh
Bit	**Attribute**	**Description**
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

Output Amplifier Capabilities (Payload = 12h)		Response: 8000 0000h
Bit	**Attribute**	**Description**
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0000000b: Step size is 0dB.
15	R	Reserved
14:8	R	Number of Steps 0000000b: Number of steps is 0h.
7	R	Reserved
6:0	R	Offset 0000000b

7.11.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	**Verb ID**	**Payload**
Get	Get Connection List Entry	F02h	Offset index n
Response 32'h00000016			
Bit	**Attribute**	**Description**	
31:8	R	Reserved	
7	R	0: Independent NID.	
6:0	R	0010110b: From MW0	

7.11.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	**Verb ID**	**Payload**
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3
Note: For PW3 power down control. Response			
Bit	**Attribute**	**Description**	
31:8	R	Reserved	
7:4	R	PS-Act Reports the actual power state of the widget.	
3:0	RW	PS-Set	

7.11.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	RW	Headphone Enable 0: Disabled (Default) 1: Headphone enabled
6	RW	Output Enable 0: Disabled (Default) 1: Output enabled
5	R	Input Enable 0: Disabled 1: Input enabled (Not supported)
4:0	R	Reserved

7.11.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format

Bit	Attribute	Description
7	RW	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	Reserved
5:0	RW	Tag Used by software to determine the node that generated the unsolicited response.

7.11.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Bit	Attribute	Description
31	R	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	Reserved

7.11.7 EAPD Enable Verbs (Verb ID = F0C & 70Ch)

	Description	Verb ID	Payload
Get	EAPD Control	F0Ch	8'b0
Set		70Ch	Bit 1 is EAPD

7.11.8 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format — Response: 0101 4010h

Bit	Attribute	Description	
31:30	RW	Port Connectivity	00b
29:24	RW	Location	000001b
23:20	RW	Default Device	0000b
19:16	RW	Connection Type	0001b
15:12	RW	Color	0100b
11:8	RW	Misc	0000b
7:4	RW	Default Association	0001b
3:0	RW	Sequence	0000b

7.11.9 Amplifier Gain/ Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/ Mute	Bh	
Set	Set Amplifier Gain/ Mute	3h	

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. (Ignored) 1: The output amplifier is being requested.
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved
3:0	W	Index

Get Response Format — Response: 0000 0080h

Bit	Attribute	Description	
31:8	R	Reserved	
7	R	0: Amplifier is unmated.	1: Amplifier is muted. (Default)
6:0	R	Amplifier Gain Setting 0000000 (Default)	

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set.
14	W	1: The input amplifier is being set. (Ignored)
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	1: Mute 0: Un-mute
6:0	W	Gain Setting

7.12 Pin Widget PW4 (Node ID =1Dh)

7.12.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 05h) Response: 0000 0101h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable.
7:0	R	0000 0001b: Audio function group.

Audio Widget Capabilities (Payload = 09h) Response: 0040 058Fh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100b: Pin widget.
19:16	R	0000b: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	1: Support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	1: Contain amplifier parameter.
2	R	1: Out amp Present.
1	R	1: In amp present.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 233Ch

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 23h. (100% & 50% & Hi-Z)
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 1.
4	R	Output Capable	Read as 1.
3	R	Headphone Drive Capable	Read as 1
2	R	Presence Detect Capable	Read as 1.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Connection List Length (Payload = 0Eh) Response: 0000 0002h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000002b: 2 inputs available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

Input Amplifier Capabilities (Payload = 0Dh) Response: 0027 0300h

Bit	Attribute	Description
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0100111b: Step size is 10dB.
15	R	Reserved
14:8	R	Number of Steps 0000011b: Number of steps is 3h (0dB~30dB).
7	R	Reserved
6:0	R	Offset 0000000b: Offset 00h is 0dB.

Output Amplifier Capabilities (Payload = 12h) Response: 0000 0000h

Bit	Attribute	Description
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0000000b: Step size is 0dB.
15	R	Reserved
14:8	R	Number of Steps 0000011b: Number of steps is 0h.
7	R	Reserved
6:0	R	Offset 0000000b

7.12.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set 8'b0: from MW0. 8'b1: form AOW3.

Get Response Format

Bit	Attribute	Description
31:8	R	Reserved
7:0	R	Connection Index Currently Set. 0: Connection from MW0 1: Connection form AOW3

7.12.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response: 0000 2516h

Bit	Attribute	Description
31:16	R	Reserved
15:8	R	0010 0101b: From AOW3
7	R	0: Independent NID
6:0	R	001 0110b From MW0

7.12.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Note: For PW4 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	PS-Set

7.12.5 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	RW	Headphone Enable 0: Disabled (Default) 1: Headphone enabled
6	RW	Output Enable 0: Disabled (Default) 1: Output enabled
5	R	Input Enable 0: Disabled (Default) 1: Input enabled (Not supported)
4:3	R	Reserved
2:0	RW	VRef Enable These bits control the VRef signal associated with the pin widget. 000: Hi-Z 001: 50% (Half of AVdd) 010: 0V (Not supported) 101: AVdd Others: Reserved

7.12.6 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format — Response: 0000 0000h

Bit	Attribute	Description
7	RW	0: Unsolicited Response Disabled. 1: Unsolicited Response Enabled.
6	R	Reserved
5:0	RW	Tag Used by software to determine the node that generated the unsolicited response.

7.12.7 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Bit	Attribute	Description
31	R	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	Reserved

7.12.8 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config Bits Format — Response: 0221 401Fh

Bit	Attribute	Description	
31:30	RW	Port Connectivity	00b
29:24	RW	Location	000010b
23:20	RW	Default Device	0010b
19:16	RW	Connection Type	0001b
15:12	RW	Color	0100b
11:8	RW	Misc	0000b
7:4	RW	Default Association	0001b
3:0	RW	Sequence	1111b

7.12.9 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested.
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved
3:0	W	Index

Get Response Format

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Amplifier is un-muted. (Input default) 1: Amplifier is muted. (Output default)
6:0	R	Amplifier Gain Setting 0000000b (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set.
14	W	1: The input amplifier is being set.
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-mute 1: Mute
6:0	W	Gain Setting

7.13 Pin Widget PW6, PW7 (Node ID = 22h, 23h)

7.13.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 05h) Response: 0000 0701h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable
7:0	R	0000 0001b: Audio function group

Audio Widget Capabilities (Payload = 09h) Response: 0040 0581h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	1: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	1: Support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	0: Contain amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not presented.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 0014h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 8’b0.
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 0.
4	R	Output Capable	Read as 1.
3	R	Headphone Drive Capable	Read as 0.
2	R	Presence Detect Capable	Read as 1.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001: Only 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

7.13.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n
		Response	0000 0026h (for PW6), 0000 0027h (for PW7)

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Independent NID.
6:0	R	0100110b: (From SW2) for PW6. 0100111b: (From SW3) for PW7.

7.13.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Note: For PW6, PW7 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.13.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	R	Headphone Enable 0: Disabled
6	RW	Output Enable 0: Disabled (Default) 1: Output enabled
5	RW	Input Enable 0: Disabled 1: Input enabled (Not support)
4:0	R	Reserved

7.13.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format

Bit	Attribute	Description
7	RW	0: Unsolicited Response Disabled. 1: Unsolicited Response Enabled.
6	R	Reserved
5:0	RW	Tag Used by software to determine which node generated the unsolicited response.

7.13.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Bit	Attribute	Description
31	R	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	Reserved

7.13.7 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format Response: 0101 6011h for PW6, 0101 2014h for PW7

Bit	Attribute	Description		
31:30	RW	Port Connectivity	00b	
29:24	RW	Location	000001b	
23:20	RW	Default Device	0000b	
19:16	RW	Connection Type	0001b	
15:12	RW	Color	0110b: for PW6	0010b: for PW7
11:8	RW	Misc	0000b	
7:4	RW	Default Association	0001b	
3:0	RW	Sequence	0001b: for PW6	0100b: for PW7

7.14 Pin Widget PW1, PW2 (Node ID = 1Ah, 1Bh)

7.14.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 05h) Response: 0000 0101h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable
7:0	R	0000 0001b: Audio function group

Audio Widget Capabilities (Payload = 09h) Response: 0040 0058h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	1: Support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Not containing format information.
3	R	1: Contain amplifier parameter.
2	R	0: Out amp not presented.
1	R	1: In amp present.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 2334h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD capable	Read as 0
15:8	R	VRef Control	Read as 23h (100% & 50% & Hi-Z)
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0
5	R	Input Capable	Read as 1
4	R	Output Capable	Read as 1
3	R	Headphone Drive Capable	Read as 0
2	R	Presence Detect Capable	Read as 1
1	R	Trigger Required	Read as 0
0	R	Impedance Sense Capable	Read as 0

Input Amplifier Capabilities (Payload = 0Dh)		Response: 0027 0300h
Bit	**Attribute**	**Description**
31	R	0: Mute capable
30:23	R	Reserved
22:16	R	Step Size 0100111b: Step size is 10dB.
15	R	Reserved
14:8	R	Number of steps 0000011b: Number of steps is 3h (0dB – 30dB).
7	R	Reserved
6:0	R	Offset 0000000b: Offset 00h is 0dB.

Connection List Length (Payload = 0Eh)		Response: 0000 0001h
Bit	**Attribute**	**Description**
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001b: Only 1 input available.

Supported Power States (Payload = 0Fh)		Response: 0000 000Fh
Bit	**Attribute**	**Description**
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.14.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	**Verb ID**	**Payload**
Get	Get Connection List Entry	F02h	Offset index n
		Response: 0000 0026h (for PW1); 0000 0018h (for PW2)	
Bit	**Attribute**	**Description**	
31:8	R	Reserved	
7	R	0: Independent NID	
6:0	R	0100110b: (From SW2, NID = 26h) for PW1 0011000b: (From SW3, NID = 18h) for PW2	

7.14.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Note: For PW1, PW2 power down control.

Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	PS-Set

7.14.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	R	Headphone Enable 0: Disabled
6	RW	Output Enable (for Smart 5.1 Configuration) 0: Disabled (Default) 1: Output enabled
5	RW	Input Enable 0: Disabled (Default) 1: Input enabled
4:3	R	Reserved
2:0	RW	VRef Enable These bits control the VRef signal associated with the pin widget. 000: Hi-Z (Default) 001: 50% (Half of AVdd) 010: 0V (Not supported) 101: AVdd Others: Reserved

7.14.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
7	RW	0: Unsolicited response disabled. 1: Unsolicited response enabled.
6	R	Reserved
5:0	RW	Tag Used by software to determine which node generated the unsolicited response.

7.14.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31	R	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	Reserved

7.14.7 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format (Default: 01A1 9026h for PW1, 0181 302Eh for PW2)

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description		
31:30	RW	Port Connectivity	00b	
29:24	RW	Location	000001: for PW1	000001: for PW2
23:20	RW	Default Device	1010: for PW1	1000: for PW2
19:16	RW	Connection Type	0001b	
15:12	RW	Color	1001: for PW1	0011: for PW2
11:8	RW	Misc	0000b	
7:4	RW	Default Association	0010: for PW1	0010: for PW2
3:0	RW	Sequence	0110: for PW1	1110: for PW2

7.14.8 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested. (Ignored)
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved
3:0	W	Index

Get Response Format

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Amplifier is un-muted. (Input default) 1: Amplifier is muted.
6:0	R	Amplifier Gain Setting 0000000b (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set. (Ignored)
14	W	1: The input amplifier is being set.
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-mute 1: Mute
6:0	W	Gain Setting

7.15 Pin Widget PW5 (Node ID = 1Eh) HDMI Audio Output Pin

7.15.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 05h) Response: 0000 0101h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable.
7:0	R	0000 0001b: Audio function group

Audio Widget Capabilities (Payload = 09h) Response: 0040 0058h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	1: Support unsolicited response.
6	R	0: No Processing control.
5	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	1: Contain amplifier parameter.
2	R	1: Out Amp presented.
1	R	1: In Amp presented.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 0233h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0
15:8	R	VRef Control	Read as 23h (100% & 50% & Hi-Z)
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0
5	R	Input Capable	Read as 1
4	R	Output Capable	Read as 1
3	R	Headphone Drive Capable	Read as 1
2	R	Presence Detect Capable	Read as 1
1	R	Trigger Required	Read as 0
0	R	Impedance Sense Capable	Read as 0

Input Amplifier Capabilities (Payload = 0Dh) Response: 0027 0300h

Bit	Attribute	Description
31	R	0: Mute capable
30:23	R	Reserved
22:16	R	Step Size 0100111b: Step size is 10dB.
15	R	Reserved
14:8	R	Number of Steps 0000011b: Number of steps is 3h (0dB – 30dB).
7	R	Reserved
6:0	R	Offset 0000000b: Offset 00h is 0dB.

Connection List Length (Payload = 0Eh) Response: 0000 0002h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000002: 2 inputs available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

Output Amplifier Capabilities (Payload = 12h) Response: 0000 0000h

Bit	Attribute	Description
31	R	1: Mute capable
30:23	R	Reserved
22:16	R	Step Size 0000000b: Step size is 0dB.
15	R	Reserved
14:8	R	Number of steps 0000000b: Number of steps is 0h.
7	R	Reserved
6:0	R	Offset 0000000b

7.15.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set 8'b0: from MW0 8'b1: form AOW3

Get Response Format

Bit	Attribute	Description
31:8	R	Reserved
7:0	R	Connection Index Currently Set 0: Connection from MW0. 1: Connection form AOW3.

7.15.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response: 0000 2516h

Bit	Attribute	Description
31:16	R	Reserved
15:8	R	0010 0101b: From AOW3
7	R	0: Independent NID
6:0	R	0010110b: From MW0

7.15.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00 : Power State is D0 8'h01 : Power State is D1 8'h02 : Power State is D2 8'h03 : Power State is D3

Note: For PW5 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.15.5 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	RW	Headphone Enable 0: Disabled (default) 1: Headphone enabled
6	RW	Output Enable (for Smart 5.1 Configuration) 0: Disabled (Default) 1: Output enabled (Default)

5	RW	Input Enable 0: Disabled (Default) 1: Input enabled
4:3	R	Reserved
2:0	RW	VRef Enable These bits control the VRef signal associated with the pin widget. 000: Hi-Z 001: 50% (Half of AVdd) 010: 0V (Not supported) 101: AVdd Others: Reserved

7.15.6 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
7	RW	0: Unsolicited Response Disabled. 1: Unsolicited Response Enabled.
6	R	Reserved
5:0	RW	Tag Used by software to determine which node generated the unsolicited response.

7.15.7 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Bit	Attribute	Description
31	R	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	Reserved

7.15.8 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format (Default: 02A1 9027h)

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description	
31:30	RW	Port Connectivity	00
29:24	RW	Location	000010b

23:20	RW	Default Device	1010b
19:16	RW	Connection Type	0001b
15:12	RW	Color	1001b
11:8	RW	Misc	0000b
7:4	RW	Default Association	0010b
3:0	RW	Sequence	0111b

7.15.9 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested.
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved
3:0	W	Index

Get Response format

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Amplifier is un-muted (Input default) 1: Amplifier is muted (Output default)
6:0	R	Amplifier Gain Setting 0000000b (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set
14	W	1: The input amplifier is being set
13	W	1: The left amplifier is being set
12	W	1: The right amplifier is being set
11:8	W	Index Ignored
7	W	0: Un-mute 1: Mute
6:0	W	Gain Setting

7.16 Pin Widget PW8 (Node ID = 1Fh) CD Analog Input

7.16.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0040 0401h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	0: Connection list is not presented.
7	R	0: Not supporting unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	0: Doesn’t contain amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not presented.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 0020h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 00h
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0
5	R	Input Capable	Read as 1
4	R	Output Capable	Read as 0.
3	R	Headphone Drive Capable	Read as 0
2	R	Presence Detect Capable	Read as 0
1	R	Trigger Required	Read as 0
0	R	Impedance Sense Capable	Read as 0

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

7.16.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Note: For PW8 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.16.3 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	R	Headphone Enable 0: Disabled
6	R	Output Enable 0: Disabled
5	RW	Input Enable 0: Disabled 1: Input enabled
4:3	R	Reserved
2:0	R	VRef Enable 000b

7.16.4 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config Bits Format (Default: 32'h593311F8)

Bit	Attribute	Description	
31:30	RW	Port Connectivity	01b
29:24	RW	Location	011001b
23:20	RW	Default Device	0011b (CD)
19:16	RW	Connection Type	0011b
15:12	RW	Color	0001b
11:8	RW	Misc	0001b
7:4	RW	Default Association	1111b
3:0	RW	Sequence	1000b

7.17 Pin Widget PW9 (Node ID = 20h) S/PDIF TX Pin

7.17.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0040 0701h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	1: Digital widget.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Not containing format information.
3	R	0: Not containing amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not present.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 0010h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0
15:8	R	VRef Control	Read as 00h
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0
5	R	Input Capable	Read as 0
4	R	Output Capable	Read as 1
3	R	Headphone Drive Capable	Read as 0
2	R	Presence Detect Capable	Read as 0
1	R	Trigger Required	Read as 0
0	R	Impedance Sense Capable	Read as 0

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001b: 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

7.17.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response: 0000 0012h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Independent NID
6:0	R	0010010b: From DOW0 (NID = 12h)

7.17.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Note: For PW9 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.17.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
7	R	Headphone Enable 0: Disabled
6	RW	Output Enable 0: Disabled (Default) 1: Output enabled
5	R	Input Enable 0: Disabled
4:3	R	Reserved
2:0	R	VRef Enable 000b

7.17.5 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format — Response: 0744 11F0h

Bit	Attribute	Description	
31:30	RW	Port Connectivity	00b
29:24	RW	Location	000111b
23:20	RW	Default Device	0100b (SPDIF Out)
19:16	RW	Connection Type	0100b
15:12	RW	Color	0001b
11:8	RW	Misc	0001b
7:4	RW	Default Association	1111b
3:0	RW	Sequence	0000b

7.18 Pin Widget PW10 (Node ID = 21h) HDMI Audio Output Pin

7.18.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0040 0701h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	1: Digital widget.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Contain no format information.
3	R	0: Contain no amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not present.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 0010h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0
15:8	R	VRef Control	Read as 00h
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0
5	R	Input Capable	Read as 0
4	R	Output Capable	Read as 1
3	R	Headphone Drive Capable	Read as 0
2	R	Presence Detect Capable	Read as 0
1	R	Trigger Required	Read as 0
0	R	Impedance Sense Capable	Read as 0

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001b: 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.18.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 0000 0015h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Independent NID
6:0	R	0010101b: From DOW1, NID = 15h

7.18.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Note: For PW10 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.18.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
7	R	Headphone Enable 0: Disabled
6	RW	Output Enable 0: Disabled 1: Output enabled
5	R	Input Enable 0: Disabled
4:3	R	Reserved
2:0	R	Vref Enable 000b

7.18.5 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config Bits Format — Response: 9856 01F0h

Bit	Attribute	Description	
31:30	RW	Port Connectivity	10b
29:24	RW	Location	011000b
23:20	RW	Default Device	0101b (SPDIF Out)
19:16	RW	Connection Type	0110b
15:12	RW	Color	0000b
11:8	RW	Misc	0001b
7:4	RW	Default Association	1111b
3:0	RW	Sequence	0000b

8 Functional Descriptions

8.1 Clock Control

One of the major differences between Azalia and AC97 is the clock source. The Azalia controller provides a 24 MHz clock (BITCLK). An internal PLL (PLL1) in the codec uses BITCLK (24MHz) as the reference clock and generates 49.152 MHz clocks for internal use. A second PLL (PLL2) also takes the 24 MHz BITCLK and generates 22.5792 MHz clock for 44.1 kHz based rates. The PLLs can be powered down by the Power Widget for power management. **Both PLL output clocks can be routed to pin 48 by a vendor defined verb for testing**.

The interface signals between digital block and the 2 PLLs are listed below.

PLL1 (49.152 MHz)		
Pin Name	**Direction (From PLL)**	**Pin Description**
REFCLK	I	Connect to a 24-MHz clock input.
CLK49152	O	49.152-MHz clock output.
RST	I	When RST is high, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is high, the PLL enters a power-down mode.
VDD	IO	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	IO	Ground for PFD and Dividers.
VCOPWR	IO	Analog power supply for VCO. Nominally 3.3V.
VCOGND	IO	Ground for VCO.
CHGPPWR	IO	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	IO	Ground for Bias and Charge Pump.

22.5792 MHz		
Pin Name	**Direction (From PLL)**	**Pin Description**
REFCLK	I	Connect to a 24-MHz clock input.
CLK225792	O	22.5792-MHz clock output.
RST	I	When RST is high, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is high, the PLL enters a power-down mode.
VDD	IO	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	IO	Ground for PFD and Dividers.
VCOPWR	IO	Analog power supply for VCO. Nominally 3.3V.
VCOGND	IO	Ground for VCO.
CHGPPWR	IO	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	IO	Ground for Bias and Charge Pump.

8.2 Interpolation / Decimation

To take advantage the high bandwidth provided by the new audio interface, the hardware only supports native 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz sample rates, and the driver is responsible for converting the data to / from 192 kHz. This way the large area previously required for implementing the digital interpolation / decimation filters can be saved.

8.3 HPF for ADC DC Removal

The built-in high-pass filter for each ADC can remove the DC component in the ADC data.

8.4 Audio Jack Detection Circuits

Based on the jack detection circuit defined in the Azalia specification, the figure below summarizes the equivalent resistance values to the SENSE pin in different scenario.

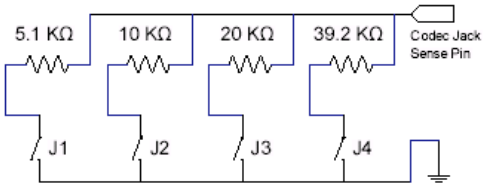


Figure 19 – Jack Detect Circuit

8.5 Internal Loop-back and Peak Detection for Low Cost Production Test

Internal loop-back paths can be used to test all DACs and ADCs functions. The output of each DAC can be routed back to the input of the ADC. The ADC output data is analyzed by a specially designed block to detect the zero-crossing point and the peak values. These information can be read back to decide whether the digital & analog functions are normal. Refer to the descriptions in the Vendor-Defined Verbs in the Audio Function Group.

8.6 GPIO Implementation

8.6.1 Pinout

- Pin 47: EAPD
  - DAC mode: SDMI[3]/ ADC mode: SDMO[3]
- Pin 48: SPDIF_TX0
- Pin 2: GPIO0/ SPDIF_TX1
  - DAC mode: SDMI[1]/ ADC mode: SDMO[1]
- Pin 3: GPIO1
  - DAC mode: SDMI[2]/ ADC mode: SDMO[2]
  - Pin out description with bold type is defined by vendor specific command. Otherwise it claims default function.

8.6.2 Usage

- GPI:
  - Front Panel Sense
  - Others
- GPO:
  - EAPD-like Control
  - Others

	NB 1	NB 2	NB 3	Desk Top 1	Desk Top 2	DAC Mode	ADC Mode	I/O
GPO for EAPD0 (Line Out)	√	√	√	-	-	-	-	-
GPO for EAPD1 (Head Phone)	√	√	√	-	-	-	-	-
SPDIF_TX0	√	√	√	√	√	-	-	-
SPDIF_TX1	-	-	-	√	√	-	-	-
GPI (Front Panel Sense)	√	√	-	√	-	-	-	-
Pin 47: EAPD	GPO	GPO	GPO	-	-	SDMI[3]	SDMO[3]	IO
Pin 48: SPDIF_TX0	SPDIF_TX0	SPDIF_TX0	SPFID_TX0	SPDIF_TX0	SPDIF_TX0	PLL CLK	PLL CLK	O
Pin 2: SPDIF_TX1	GPO	GPO	GPO	SPDIF_TX1	SPDIF_TX1	SDMI[1]	SDMO[1]	IO
Pin 3: GPIO1	GPI	GPI	-	GPI	-	SDMI[2]	SDMO[2]	IO

9 Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_S	Storage Temperature	-55	125	°C	—
T_A	Ambient Operating Temperature	0	85	°C	—
V_{ESD}	Electrostatic Discharge (human body model)	—	2	kV	—

Note: Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
DVDD	Digital Power Supplies	3.135	3.3	3.465	V
AVDD	Analog Power Supplies (preferred)	–	5	–	V
AVDD	Analog Power Supplies (for low-power apps)	–	3.3	–	V

Digital DC and AC Characteristics

DC Performance Characteristic

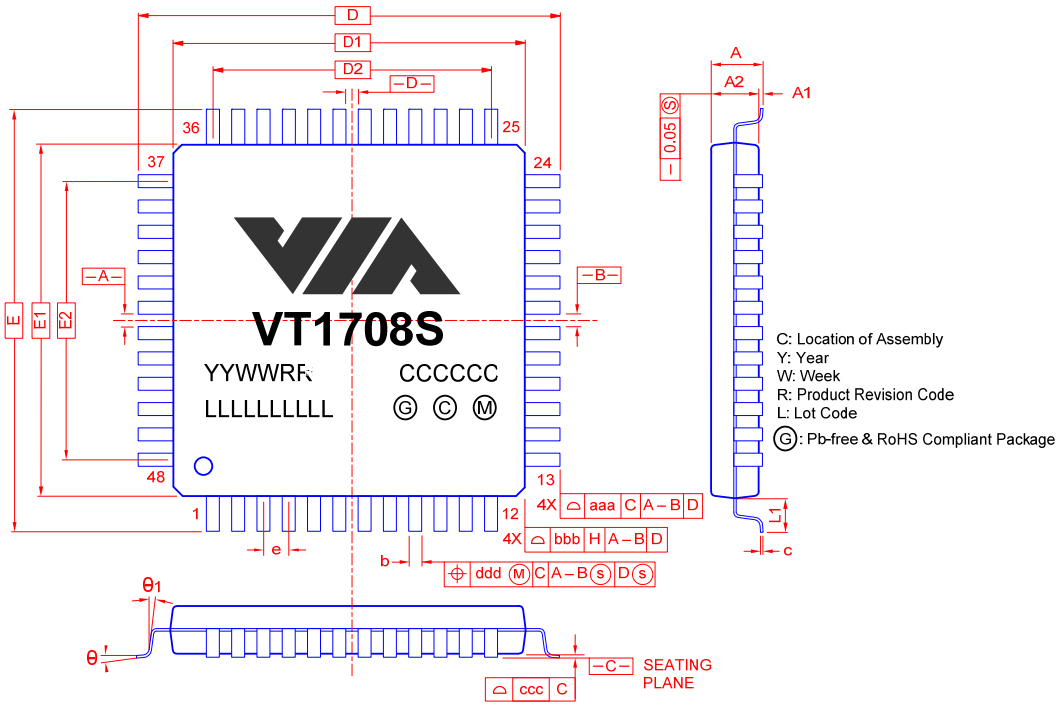
Symbol	Parameter	Min	Max	Unit	Note
V_{IN}	Input Voltage Range	-0.3	–	DVDD+0.3	V
V_{IL}	Low Level Input Voltage	–	–	0.35xDVDD	V
V_{IH}	High Level Input Voltage	0.65xDVDD	–	–	V
V_{OH}	High Level Output Voltage	0.9xDVDD	–	–	V
V_{OL}	Low Level Output Voltage	–	–	0.1xDVDD	V
	Input Leakage Current (AC-Link inputs)	-10	–	10	µA
	Output Leakage Current (Hi-Z'd AC-Link outputs)	-10	–	10	µA
	Input / Output Pin Capacitance	–	–	7.5	pF

Analog Performance Characteristics

Parameter	Min	Type	Max	Unit
Analog Input				
Full Scale Input Voltage	–		–	
Line Inputs		1.0		Vrms
Mic Inputs with 20 dB Gain		0.1		
Mic inputs with 0 dB Gain		1		
Input Impedance with 0dB Gain	–	30	–	kΩ
Input Capacitance	–	7.5		pF
Analog Output				
Full Scale Output Voltage	–			
Line Output			1.6	Vrms
Headphone Output		1.0		
Analog S/N	–		–	
Other to LINE_OUT		100		dB
Analog Frequency Response	20	–	20,000	Hz
Vrefout	–	2.25-2.75	–	V
ADC Converters				
Digital S/N	–	100	–	dB
Total Harmonic Distortion	–	–	0.003	%
Frequency Response	20	–	19,200	Hz
Transition Band	19,200	–	28,800	Hz
Stop Band	28,800	–	–	Hz
Stop Band Rejection	-74	–	–	dB
Out-of-Band Rejection	–	-40	–	dB
Spurious Tone Reduction	–	-100	–	dB
Attenuation, Gain Step Size	–	1.5	–	dB
DAC Converters				
Digital S/N	–	100	–	dB
Total Harmonic Distortion	–	–	0.003	%
Frequency Response	20	–	19,200	Hz
Transition Band	19,200	–	28,800	Hz
Stop Band	28,800	–	–	Hz
Stop Band Rejection	-74	–	–	dB
Out-of-Band Rejection	–	-40	–	dB
Channel Separation	–	-90	–	dB
Spurious Tone Reduction	–	-100	–	dB
Attenuation, Gain Step Size	–	1.5	–	dB

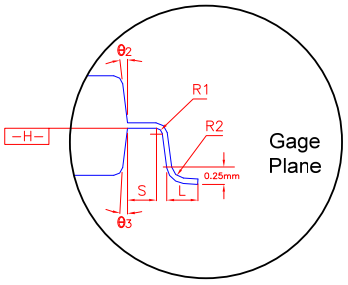
Note: The frequency response, transition band and stop band specified in the table is based on fs = 48 kHz, and scale with fs.

10 Mechanical Specification



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	—	—	0°	—	—
Θ2	11°	12°	13°	11°	12°	13°
Θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
48L						
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		



NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 20 – VT1708S LQFP-48 Package (7 mm×7 mm)

11 Application Circuit

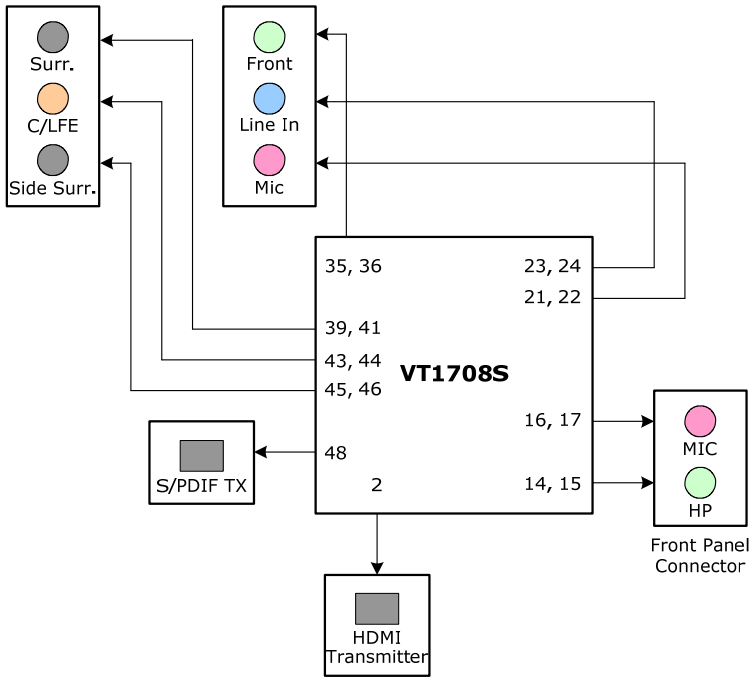


Figure 21 – The System with Front Panel Design

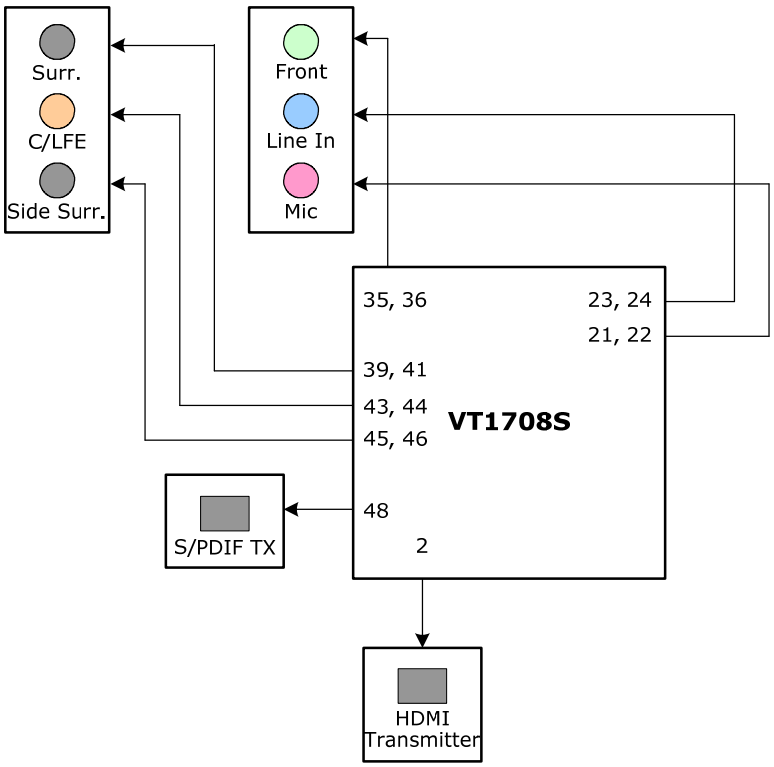


Figure 22 – The System without Front Panel Design

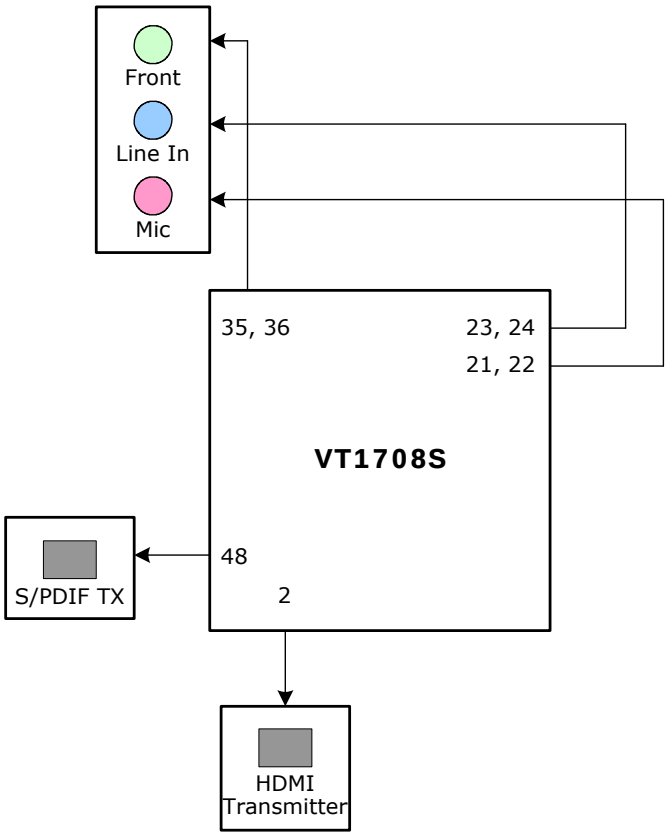


Figure 23 – The System with Only One Back Panel Connector Design

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